Instrumentation Lab V: JFET Circuits II

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Introduction

This lab deals primarily with JFET amplifiers. JFETs' primary function is to regulate the amount of current flowing between two terminals by way of a voltage imposed on a third terminal. By utilizing this fact, it is relatively easy to construct a circuit which takes in a signal and amplifies it in magnitude. This is different from a transformer which sacrifices current for voltage or voltage for current: JFET amplifiers increase the power of the signal by using a secondary source. This has numerous applications including simply powering a loud speaker, to modulating radio signals, to building the fundamental circuitry that makes ECG's go. Aside from the basic circuits that meet these needs, we will also be learning how to modify and design circuits that are more resistant to imperfections like temperature fluctuations and unmatched components, a skill which is essential to circuit design.

Exercises

Amplifiers

5.1 We built the amplifier circuit shown in figure 1 and tested its functionality. At first no signal was applied to V_{in} and the equilibrium values were measured and recorded in table 5.1. Then the amplifier was driven with a 10kHz 1 V p-p sine wave at Vin and the circuit's gain was measured at Vout for several different JFET components. The theoretical gain of this circuit for arbitrary component values is given by $G = -\frac{RD}{Rs+rs} \approx -\frac{RD}{Rs}$. So from this circuit we would expect a gain of about G ≈ 4.7k / 1k = 4.7.

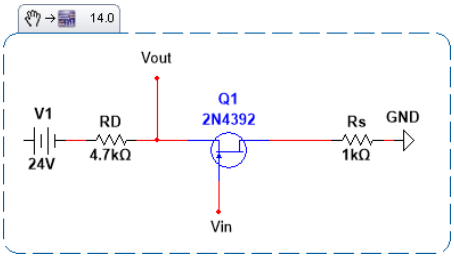

FIGURE 1 CIRCUIT 5.1

TABLE 1 EQUILIBRIUM VOLTAGES AND CURRENTS

V_{GS} = 0.2V	V_{DS} = 0.2V	V_{out} = 0V	I_{DS} = 0.004A

JFET	V_{in} (V)	V_{out} (V)	Gain (V_{out}/V_{in})
1	1.1	4.0	3.6
2	1.2	4.0	3.3
3	0.92	4.0	4.4
4	0.96	4.0	4.2
5	0.96	4.0	4.2
			Average: **3.9** STDEV: 0.5

This circuit has a maximum signal amplitude that can go undistorted by the JFET component. By varying the input voltage and monitoring the output voltage on the oscilloscope we determined this maximum to be an amplitude of 2.7 V p-p. Sine wave signals with amplitudes above this value have the top of each crest 'chopped' off.

This circuit has a gain of about 3.9, depending on which particular JFET is being used. This is less than the expected gain of 4.7. This discrepancy is expected as a result of the imperfections in the components and unavoidable inefficiencies caused by heating.

By cooling the JFET with circuit cooler, we were able to temporarily increase the circuit's gain. One JFET with a circuit gain of 3.9 temporarily increased the circuit gain to 4.0 when cooled.

5.2 It might be assumed from the expression $G = -\frac{RD}{Rs+rs} \approx -\frac{RD}{Rs}$ that simply increasing the resistor value RD in circuit 5.1 will increase the gain of the circuit. However, this is not viable strategy, as was demonstrated by the following exercise. Starting with circuit 5.1, we changed RD from 4.7k to 47k while keeping the same input signal. Naively you would hope that the gain would increase by a factor of ten. What actually happened is that the output signal disappeared from the previous scale. The amplitude of the output dropped to 10mV (compared to 4V before). The reason for this failure is that the current being supplied by the DC power supply is simultaneously reduced by a factor of ten as the resistance RD is increased. Thus most of the source of the amplification is lost.

5.3 Returning to the expression $G = -\frac{RD}{Rs+rs} \approx -\frac{RD}{Rs}$ we can also see that reducing Rs ought to increase the gain. Starting again with circuit 5.1, the resistor Rs was changed from 1kΩ to 500Ω. The new gain of the circuit for several different JFETs was measured and recorded in table 2.

TABLE 2

JFET	V_{in} (V)	V_{out} (V)	Gain (V_{out}/V_{in})
1	0.3	2.08	6.9
2	0.3	2.06	6.9
3	0.3	1.62	5.4
4	0.3	1.60	5.3
5	0.3	1.84	6.1
			Average: 6.1 STDEV: 0.8

The fractional deviation of the gain the same for this circuit than for circuit 5.1; both had a standard deviation of 13% of the average. When one of the JFETs was cooled with circuit cooler, the gain increased from 6.9 to 7.3. This is a significantly larger variance than that of circuit 5.1; this circuit is more sensitive to temperature, which is undesirable.

5.4 Instead of directly decreasing the value of the resistor in circuit 5.1, we can also bypass it with a capacitor in parallel. This will reduce the impedance as seen by the AC signal we are trying to amplify, but without reducing the impedance seen by the DC voltage source. In this exercise we started with circuit 5.1, then we added a 1μF capacitor in parallel with the Rs resistor (see figure 2). Theoretically the gain should now be $G = \frac{RD}{rs+Reff} = \frac{4.7k}{100+Reff}$ where Reff is the effective impedance of the 1k resistor and 1uF capacitor in parallel. The rs is the resistance caused by the JFET which cannot be ignored in this case. $Reff = \frac{Rs}{\sqrt{1+w^2C^2Rs^2}} = \frac{1k}{\sqrt{1+(2\pi*10k)^2*(1u)^2*(1k)^2}} = 16$. So then the gain is $G = \frac{4.7k}{100+16} = 40.5$. Note that this quantity is frequency dependent.

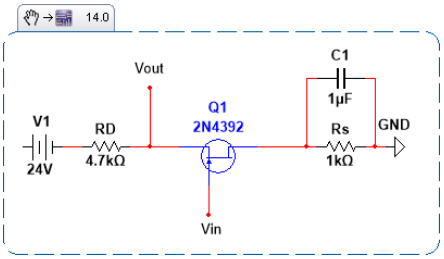

FIGURE 2 CIRCUIT 5.3

TABLE 3

JFET	V_{in} (V)	V_{out} (V)	Gain (Vout/Vin)
Room temperature	0.3	9.04	30.5
Cooled with circuit coolant	0.3	11.0	37.2

Notice that this circuit is still highly temperature dependent.

Differential Amplifiers

5.5 We built the differential amplifier circuit shown in figure 3 and tested is various outputs. Note that – as required – the circuit was built with a pair of matched JFETs. We drove the circuit using a 1kHz, 100mV p-p sin wave; first, driving the circuit only from V+, the output signal and phase was measured at Vout and Vinvout. Then, driving the circuit only from V- with the same signal, the output signal and phase was measured again at Vout and Vinvout. And finally, the circuit was driven at both V+ and V- simultaneously with the same signal, and the common mode gain was calculated from the ratio of Vout to V+ = V- = Vc. See tables 4 through 6.

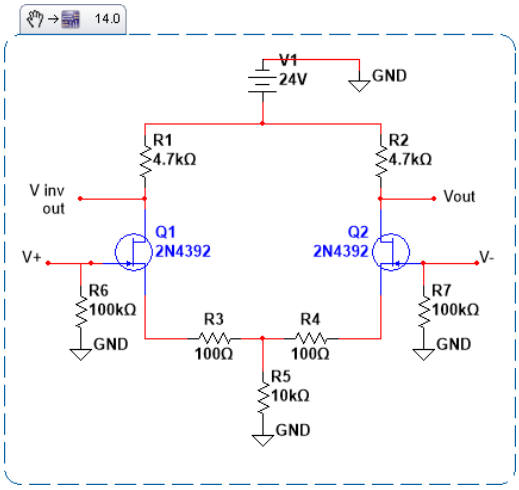

FIGURE 3 CIRCUIT 5.5

TABLE 4 CIRCUIT 5.6 DRIVEN AT V+ WITH 1KHZ, 0.2V P-P SINE WAVE

Input: V	Vout	Vinvout
Amplitude (mV)	560	580
Phase	0	180
Gain	2.9	3.0

TABLE 5 CIRCUIT 5.6 DRIVEN AT V- WITH 1KHZ, 0.2V P-P SINE WAVE

Input: V-	Vout	Vinvout

Amplitude (mV)	620	550
Phase	180	0
Gain	3.1	2.8

TABLE 6 CIRCUIT 5.6 DRIVEN AT V+ AND V+ WITH 1KHZ, 0.2V P-P SINE WAVE

Input: V+ and V-	Vout	Vinvout
Amplitude (mV)	60	-
Gain	0.3	-

The importance of having two JFETs which are as closely matched as possible was verified by swapping out one of the matched JFETs with an unmatched one. This change prevents the differential amplifier from working properly. The reason for this is that the potential drop across either drain resistor (RD: the 4.7k resistors; R1 and R2 in fig. 3) is no longer matched on either side of the amplifier, preventing equivalent and symmetric current flow on either side.

5.6 A differential amplifier's function depends on the fact that the current through both half of the circuit is the same. In circuit 5.5 this was accomplished by using symmetric circuitry and by then connecting the two halves near the drain. However, a more effective method is to replace the common source resistor by a current source. This is what we have done in circuit 5.6. Using the same procedure as in exercise 5.5, the performance of circuit 5.6 was tested and the results were recorded in tables 7 through 9.

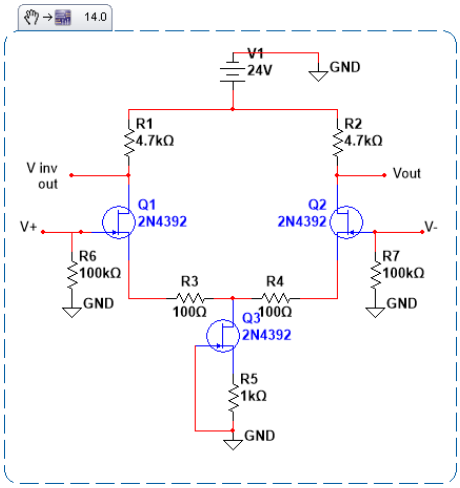

FIGURE 4 CIRCUIT 5.6

TABLE 7 CIRCUIT 5.6 DRIVEN AT V+ WITH 1KHZ, 0.1V P-P SINE WAVE

Input: V+	Vout	Vinvout
Amplitude (mV)	712	700
Phase (deg.)	0	180
Gain	7.1	7.0

TABLE 8 CIRCUIT 5.6 DRIVEN AT V- WITH 1KHZ, 0.1V P-P SINE WAVE

Input: V-	Vout	Vinvout
Amplitude (mV)	720	712
Phase (deg.)	180	0
Gain	7.2	7.1

TABLE 9 CIRCUIT 5.6 DRIVEN AT V+ AND V- WITH 1KHZ, 0.1V P-P SINE WAVE

Input: V+ and V+	Vout	Vinvout
Amplitude (mV)	10	-
Gain	0.1	-

Cleary this modification to the differential amplifier was effective: the gain was increased from 3 to 7.

JFET Attenuator

5.7 JFETs can be used to build an attenuator circuit, i.e. one whose output signal's amplitude is some fraction of its input signal's. In this exercise we built circuit 5.7, a JFET attenuator, and investigated its functionality.

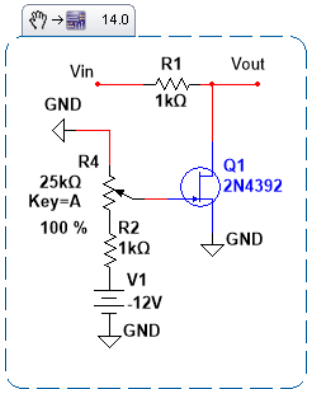

FIGURE 5 CIRCUIT 5.7 JFET ATENUATOR

We drove circuit 5.7 at Vin with a 1kHz, 100mV p-p triangular wave, and measure the output at Vout. By varying the value of the potentiometer, we were able to reduce the output signal to be ¾ as large as the input signal. This occurred at a resistance of 6.9kΩ. This circuit is not ideal, however, due to its nonlinear properties. **The signal is distorted for signal input amplitudes above 300mV**.

5.8 In order to improve the performance of the JFET attenuator, we added two 100k resistors as shown in figure 6. We drove the circuit as before with a 1kHz, 100mV p-p triangular wave and measure the output at Vout. With this circuit the output signal was reduced to be ¾ as large as the input signal when the potentiometer was set to 14.3kΩ. This setting was kept when in the following measurement we found the largest input signal for which the output was relatively undistorted. **The signal is distorted for input amplitudes above 1.5V**, 5 times higher than circuit 5.7.

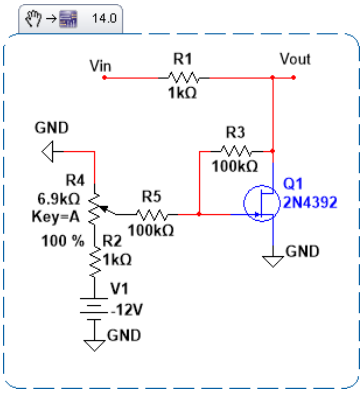

FIGURE 6 CIRCUIT 5.8 IMPROVED JFET ATTENUATOR

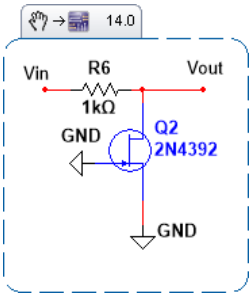

FIGURE 7 CIRCUIT 5.8.1 EFFECTIVE, WHEN POTENTIOMETER SET TO 0

Then, with the potentiometer set to maximize attenuation (this occurred as the potentiometer's resistance was set to 0Ω) we calculated the drain-source resistance corresponding to this setting. Since the potentiometer was set to 0Ω, all of the current and potential drop from the -12V DC source goes directly to ground after the 1k resistor. This means that the circuit effectively becomes a voltage divider (see Fig. 7).

Using simple voltage divider equations:

$$\frac{Vin}{Vout} = \frac{1k + RDS}{RDS} \; so \; RDS = 1k * \frac{Vout}{Vin - Vout}$$

we calculated the drain source resistance of this circuit (Fig.7). With V_{in} set to 1.5V p-p, V_{out} was measured to be 0.04V p-p. **Plugging in to the above equation we find that RDS = 27Ω**.

JFET Modulator

5.9 A slight modification of circuit 5.8 can be used to amplitude modulate (AM) a carrier wave. This modified circuit is shown in figure 8. This is similar to how AM radio signals are modulated. The input carrier wave: a 1V p-p, 1 MHz sine wave was inputted into Vin. This carrier wave was modulated by a 1kHz 1V p-p sine wave fed into the Vmodulate input. The resulting output signal measured at Vout is shown below in figure 9.

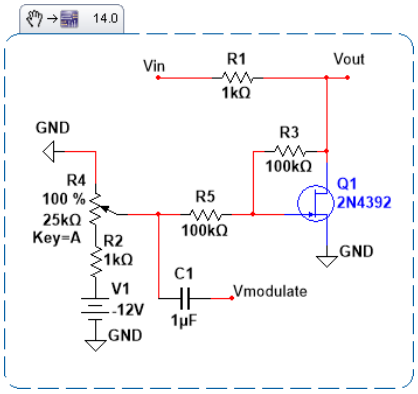

FIGURE 8 CIRCUIT 5.9 JFET MODULATOR

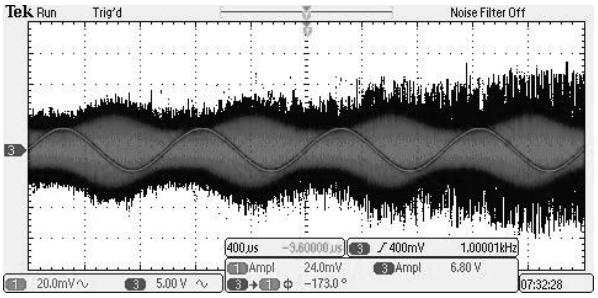

FIGURE 9 OUTPUT OF JFET MODULATOR

5.10 By attaching a long (2-meter) wire to Vout, we made a low power AM transmitter. We verified its functionality by tuning a radio to a low activity AM band and by then tuning the high frequency carrier signal until we could hear the 1kHz tone from the radio. This method was also used to transmit an audio signal provided by the lab's wave generator.

Analysis

5.11 A differential amplifier built with a current source – such as the one in 5.6 – has a common mode gain of zero. This is clearly seen to be the case from the following equation which gives the common mode gain of a differential amplifier:

$$G_{CM} = \frac{R_D}{2R_1 + R_s + r_s}$$

Where RD is the drain resistor, RS is the source resistor, rs is the transistor resistance, and R1 is the resistance of the object which was previously a resistor, but is now a current source. Since a current source effectively has infinite resistance, **the common mode gain tends towards zero**. The differential gain will be as before, Gdiff = RD / (RS+rs).

Mystery Circuit

5.12 We built the circuit shown in figure 9: circuit 5.12. The output of this circuit periodically falls-off, creating a sort of crude square wave output.

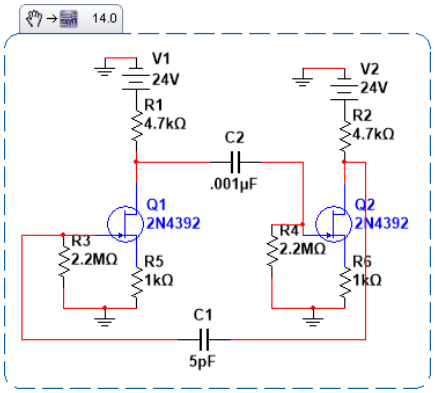

FIGURE 10 CIRCUIT 5.12

Phase Splitter

5.13 A relatively simple circuit can be used to split a signal into two output signals of equal magnitude and opposite phase. Using a unity gain amplifier as shown in figure 10, with outputs above and below the JFET, we get out two signals out of phase by 180 deg. And with equal amplitude. The capacitors just before the outputs remove the DC offset added by the amplifier source and the gate source voltage.

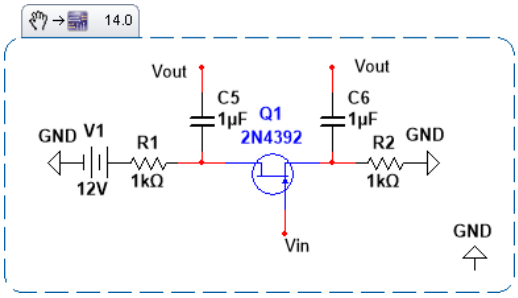

FIGURE 11 CIRCUIT 5.13 UNITY-GAIN PHASE SPLITTER

High gain Amplifier

5.14 In this exercise we attempted to build a high gain amplifier that is less sensitive to temperature changes and to the particular JFET's being used. Starting with the circuit shown in figure 11, we determined the resistor values R6 and R4 which maximized the circuits gain. These values were determined to be **R6 = 1MΩ and R4 = 1kΩ**, at which the circuit maintained a gain of 48.8. (Vin = 200mV, Vout = 1.76V).

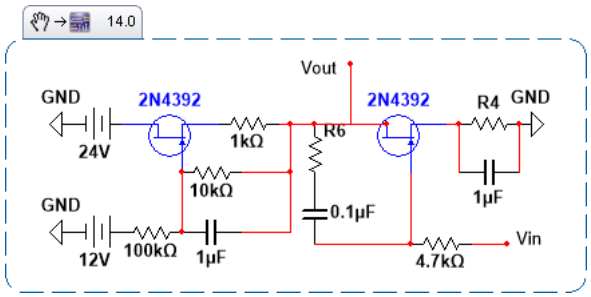

FIGURE 12 CIRCUIT 5.14 HIGH GAIN AMPLIFIER

The gain was also tested with one of the JFETs swapped out for another. The gain of the circuit was then (1) 9.68/0.2 = 48.1 and (2) 11.2/0.2 = 56. The circuit is still dependent on the particular JFETs in use, but less so. The circuit is still temperature dependents, given that one cools only one JFET at a time, but again, less so than for previous amplifier designs.

5.15 Circuit 5.14 has many components, each of which contributes towards the overall effectiveness of the circuit. Here are explanations of the various improvements that some of the components provide:

1. Sets the gain through feedback: the JFETs act by feedback to amplify their input signals.

2. Acts as a current source to increase the gain: the (left, Fig. 12) JFET closest to the 24V supply, feeds the second JFET as a current source, having very high resistance, this vastly increasing the gain of the amplifier.

3. Increases the open-loop gain by providing an AC bypass capacitor: the 1uF capacitor which feeds the secondary JFET removes most of the DC offset of Vout, which then controls the Vgs of the secondary JFET, hence again creating a feedback loop to increase the gain of the signal.

4. Sets the current through the JFETs: the 12V supply which feeds the gate of the (left) JFET.

5. Assures that the drain source voltage across both JFETs is approximately 12V, independent of the particular parameters of each JFET

6. Increases the stiffness of the current source by providing a bypass for AC signals: capacitor in parallel with grounded resistor (R4). This capacitor allows for AC signals to bypass the source resistor, increasing the gain for AC signals.

Conclusion

In this lab we learned how to build and optimize several important circuits: the simple amplifier, the differential amplifier, JFET attenuators, and the AM modulator, to name the more prominent of the lot. Being a circuit element that depends entirely on the principle of feedback, JFETs are also prone to introduce the possibility of parasitic oscillations: unwanted oscillations caused by noise which is amplified in feedback loops within the circuit. As a matter of necessity, we also learned how to deal with parasitic oscillations; how to design circuits or augment them in order to silence any parasitic oscillations (e.g. with a power decoupling capacitor, clean circuit design).