6 December 2019

All-I/O IO397_50K Manual

I/O pin mapping and driver configuration

I/O Module	IO397_50K
Minimum Required Speedgoat Library	8.27.1
Reference	speedgoat_IO397_50K_all_io

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Document Version History

Rev.	Description	Date
0.0	initial version of All-I/O IO397_50K Manual	19 May 2014
2.1	updated version of All-I/O IO397_50K Manual	6 December 2019

1 Introduction

This manual supplements the User Manual you received with your real-time target machine.

Your real-time target machine is equipped with at least one FPGA I/O module for which a default FPGA bitstream and Simulink Real-Time ™ driver blockset have been provided. Refer to your real-time target machine user manual for more information.

This manual explains how to install, configure, and use the specific (custom) FPGA bitstream and Simulink Real-Time driver blockset you ordered upon purchase of your real-time target machine. Note that the bitstream and driver blockset can also be purchased at a later date.

2 Implemented Functionality

This custom FPGA bitstream and Simulink Real-Time driver blockset implements the following functionality:

FPGA Code Module	Transceiver Type	No.of Modules/Channels	Version
Analog Input	Analog	4	1.0
Analog Output	Analog	4	1.0
Digital Input/Output	TTL	13	1.0
Interrupt Input	TTL	1	1.3

Table 1: IO397_50K front I/O implemented functionality

3 Software Installation

Install the custom FPGA bitstream and Simulink Real-Time driver blockset after installing the MathWorks software and the Speedgoat library (speedgoatlib). The steps are as follows:

1. Download the custom implementation for your I/O module and Matlab R2019a from the Speedgoat Customer Portal. The custom implementation is listed in the downloads/software section. If it is not available, please contact Speedgoat support.
2. The archive contains the custom implementation test model (*.slx) and bitstream (*.mat).
3. The content of this archive can be extracted to your current MATLAB workspace. The bitstream (MAT-file) must be part of the MATLAB path. For your convenience, you can copy the bitstream to the following directory, which is part of the MATLAB path. To obtain the predefined bitstream directory, in MATLAB type:
   » `fullfile(speedgoatroot,'sg_bitstream')`
4. After copying the MAT-file, type:
   » `rehash toolbox`

4 I/O Pin mapping

The I/O pin mapping for this custom FPGA bitstream implementation is shown below. This I/O pin mapping is specific to the FPGA I/O module for which it has been designed and shows how to connect the pins to your hardware under test.

Note: Speedgoat delivers real-time target machines together with terminal boards (refer to your target machine user manual). The terminal board for the FPGA I/O module must therefore be wired as described in section 7.2 of this document in order to execute the test model for this specific implementation.

4.1 Front I/O

Terminal board B: digital I/O

Pin	Code Module Channel	Functionality	Direction	Transceiver	Port	Pull Resistors
1b		0 V				
2b		5 V				
3b	1	GPIO	IN/OUT	TTL		
4b	2	GPIO	IN/OUT	TTL		
5b	3	GPIO	IN/OUT	TTL		
6b	4	GPIO	IN/OUT	TTL		
7b	5	GPIO	IN/OUT	TTL		
8b	6	GPIO	IN/OUT	TTL		
9b	7	GPIO	IN/OUT	TTL		
10b	8	GPIO	IN/OUT	TTL		
11b	9	GPIO	IN/OUT	TTL		
12b	10	GPIO	IN/OUT	TTL		
13b	11	GPIO	IN/OUT	TTL		
14b	12	GPIO	IN/OUT	TTL		
15b	13	GPIO	IN/OUT	TTL		
16b	1	Interrupt input	IN	TTL		
17b		GND				pull-up 3.3 VDC

Terminal board A: analog I/O

Pin	Single-ended	Differential	Analog
1a	Analog input 01	Analog input 01 (+)	
2a	GND	Analog input 01 (-)	
3a	Analog input 02	Analog input 02 (+)	
4a	GND	Analog input 02 (-)	
5a	Analog input 03	Analog input 03 (+)	
6a	GND	Analog input 03 (-)	
7a	Analog input 04	Analog input 04 (+)	
8a	GND	Analog input 04 (-)	ADC
9a	Analog Output 01	(-)	
10a	Analog output 02	(-)	
11a	Analog Output 03	(-)	
12a	Analog Output 04	(-)	DAC
13a	GND	(-)	
14a	GND	(-)	
15a	0V	(-)	
16a	5 VDC	(-)	
17a	GND	(-)	

Figure 1: IO397_50K front plug-in pin mapping

5 Simulink Driver Library

To open the library blocks for the custom FPGA bitstream, type:
» `speedgoatlib_IO397_50K_all_io`

at the MATLAB command line prompt. The blockset appears as follows:

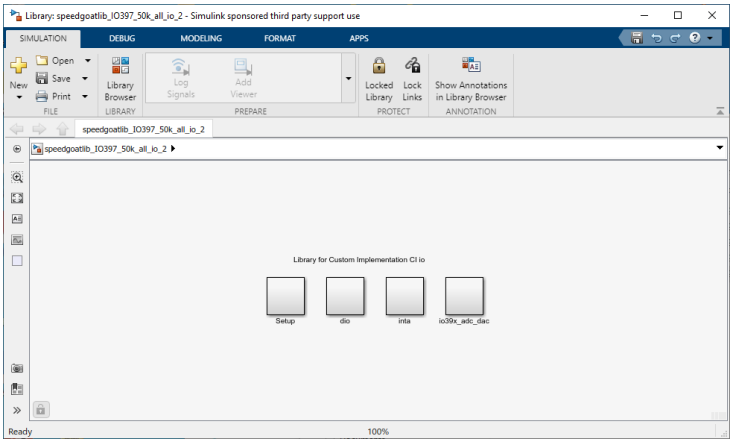

Figure 2: Library for All-I/O IO397_50K Manual

The custom FPGA bitstream library contains a subset of the Speedgoat FPGA library blocks implemented in this specific bitstream.

The Speedgoat Library may contain different versions of the driver blocks which are not compatible with your bitstream. We therefore highly recommend that you use this custom library whenever you start to build a new Simulink model.

Alternatively, ensure you select the right version of the respective driver blocks. The version of your implemented Code Module functionality is listed in Section 2, where the major version number signifies the driver block version.

6 Bitstream

The custom Speedgoat FPGA bitstream is configured in the setup driver block.

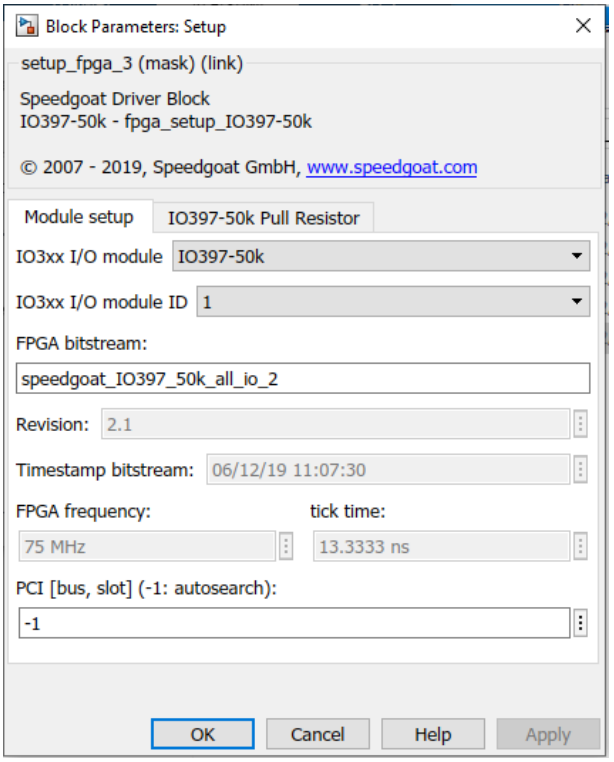

Figure 3: IO397_50K, select I/O module, front- / rear- I/O plug-in and All-I/O IO397_50K Manual bitstream

The FPGA frequency and the resulting tick time (see figure above) is used for time measurements and configuration in several FPGA code modules (like PWM, CAP) and for defining transmission frequencies for protocols (such as SPI, I2C).

7 Test Model

7.1 Test Model Description

A dedicated test model is included to test the All-IO set of DIO and Interrupt FPGA Code Modules.
To open the test model type:

```
» speedgoat_IO397_50K_all_io
```

at the MATLAB command line prompt. The model appears as follows:

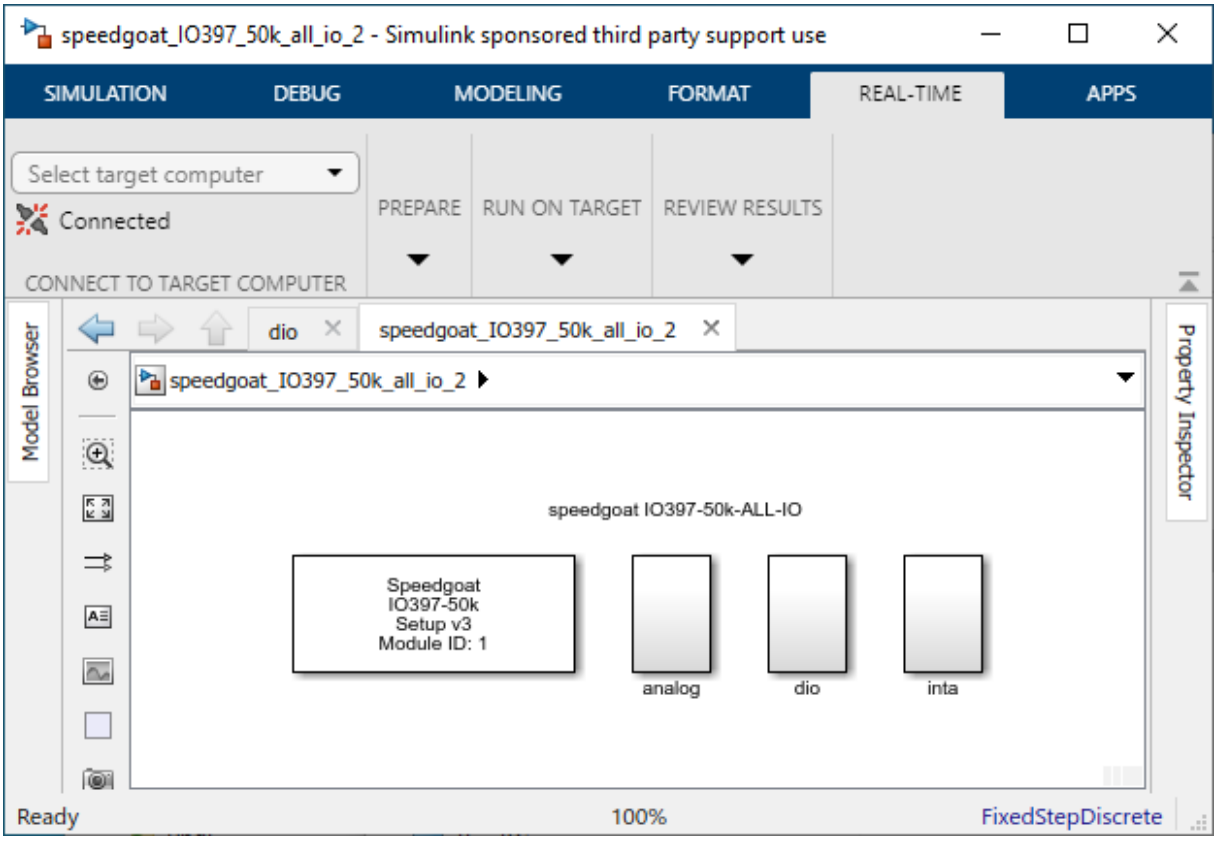

Figure 4: Test model speedgoat_IO397_50K_all_io

7.2 Required Test Wiring of the Terminal Board

Front I/O (Analog):

From Pin	To Pin	Tested Functionality
1a	9a	VOUT01 - VIN01 (+) ADC01
3a	10a	VOUT02 - VIN02 (+) ADC01
5a	11a	VOUT03 - VIN03 (+) ADC02
7a	12a	VOUT04 - VIN04 (+) ADC03
13a	2a	Ground - VIN01 (-) ADC01
13a	4a	Ground - VIN02 (-) ADC02
13a	6a	Ground - VIN03 (-) ADC03
13a	8a	Ground - VIN04 (-) ADC04

Table 2: IO397_50K- Front I/O analog terminal board wiring

Front I/O (Digital):

From Pin	To Pin	Tested Functionality
3b	9b	DO channel 1 to DI channel 7
4b	10b	DO channel 2 to DI channel 8
5b	11b	DO channel 3 to DI channel 9
6b	12b	DO channel 4 to DI channel 10
7b	13b	DO channel 5 to DI channel 11
8b	14b	DO channel 6 to DI channel 12
7b	15b	DO channel 5 to DI channel 13
8b	16b	DO channel 6 to Interrupt input

Table 3: IO397_50K- Front I/O digital terminal board wiring