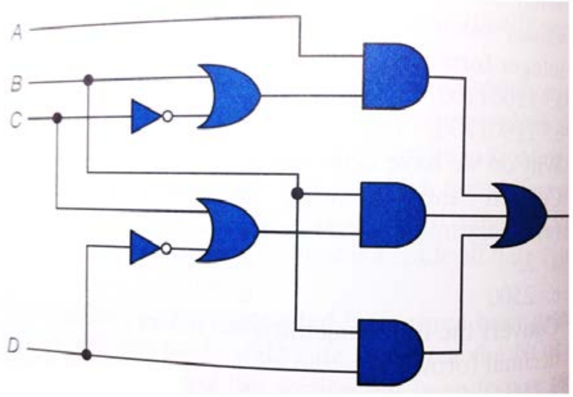
CISC 260 Machine Organization and Assembly Language
(Spring 2018)

Assignment # 2
(Due: March 1, 2018)

1. [25 points] Given the following truth table, where X, Y, and Z are input and W is output, write the canonical expression and generate gate-level logical circuit (draw the wire diagram).

X	Y	Z	W
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

2. [25 points] Write the Boolean expression and fill out the truth table for following logical circuit.



3. [25 points] You are asked to design a circuit to detect if an overflow occurs when ***adding*** two integers represented in two's complement: Z= X + Y. Let Sz, Sx, and Sy be the sign bit for Z, X, and Y respectively, and they are fed as input to the circuit. Let O be the output bit of the circuit, whose value is 1 if an overflow happens, and 0 if otherwise.

a) Build the truth table for O as a Boolean function of Sx, Sy, and Sz.
b) Write the canonical expression (sum-of-product) for the Boolean function defined in the part a.
c) Implement the Boolean expression defined in part b with a circuit by using AND, OR, and NOT gates. Draw the wiring diagram.

4. [25 points] Prove that NOR gate is universal, by showing how AND, OR, and NOT gates can be built by wiring a bunch of NOR gates. Draw the wire diagram for each case.