

CISC260 Machine Organization and Assembly Language

CISC 260 Machine Organization and Assembly Language

Spring 2018

Time & Place: 9:30AM-10:45AM, TR, Willard Hall 006

Instructor: Li Liao (Smith 424, 831-3500, liliao@udel.edu), Office Hours: 11:00PM-12:00PM Tuesdays and Thursdays or by appointment

TA: Jiefu Li, (Smith 201, lijiefu@udel.edu), Office Hours: 10AM-11AM, Wednesdays; 2-3PM, Thursdays.

Course Catalog Description:

Introduction to the basics of machine organization. Programming tools and techniques at the machine and assembly levels. Assembly language programming and computer arithmetic techniques.

COMPUTER ORGANIZATION AND DESIGN

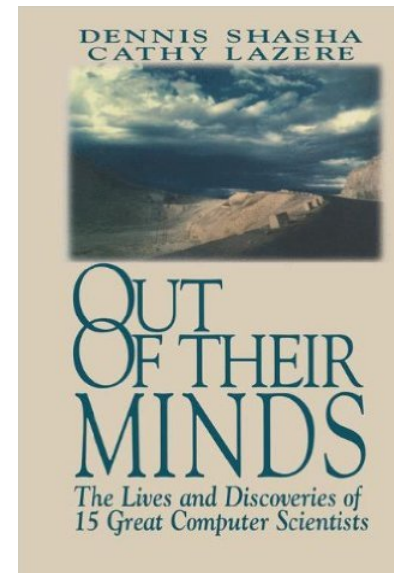
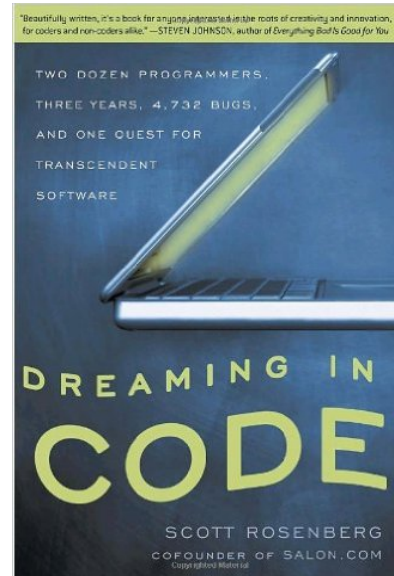
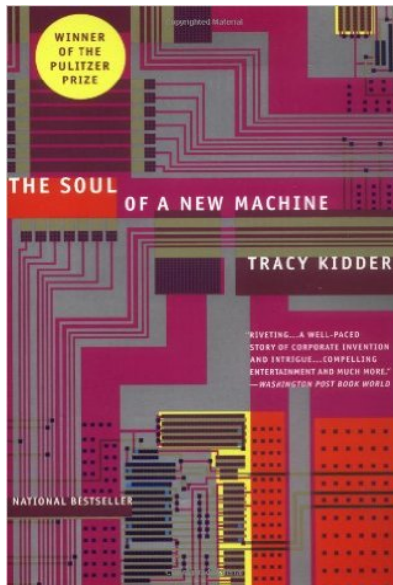
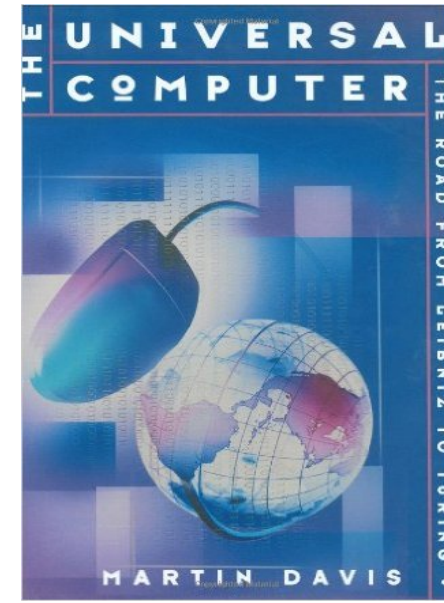
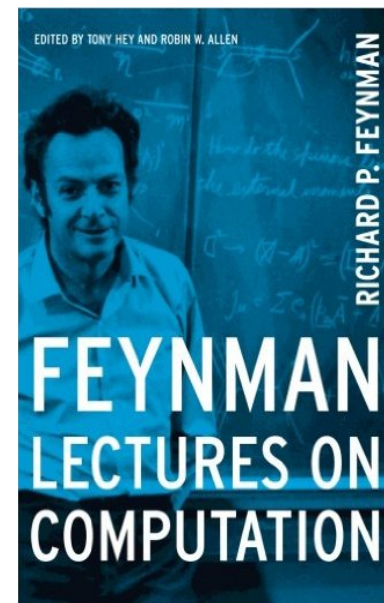
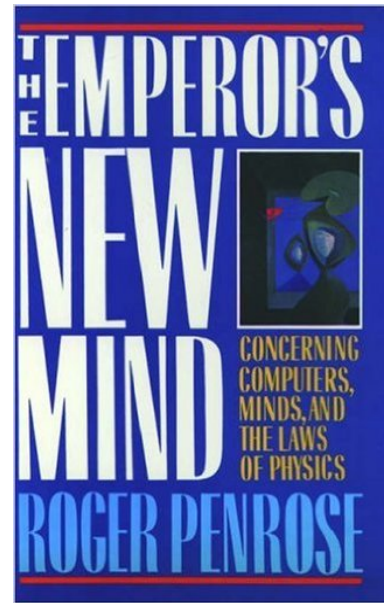
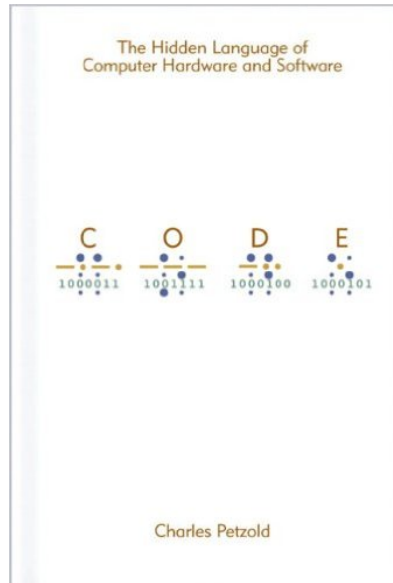
THE HARDWARE/SOFTWARE INTERFACE

ARM EDITION



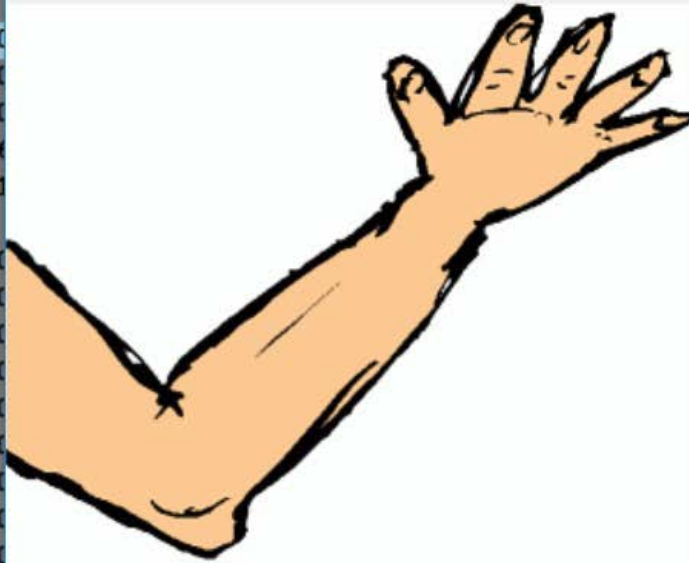
MK

DAVID A. PATTERSON
JOHN L. HENNESSY



About ARMSim#

ARMSim - the ARM Simulator



ARMSim# Version 1.9.1 (20500)

University of Victoria

Produced by:

Dr. Nigel Horspool

Dale Lyons

Dr. Micaela Serra

Department of Computer Science.

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Simulating ARMv5 instruction architecture with Vector
Floating Point support and a Data/Instruction Cache
simulation.

Docking Windows provided by:

[Crownwood Software](#)

File View Cache Debug Watch Help

RegistersView

General Purpose Floating Point

Hexadecimal

Unsigned Decimal

Signed Decimal

R0 :00000000
R1 :00000000
R2 :00000000
R3 :00000000
R4 :00000000
R5 :00000000
R6 :00000000
R7 :00000000
R8 :00000000
R9 :00000000
R10 (s1) :00000000
R11 (fp) :00000000
R12 (ip) :00000000
R13 (sp) :00005400
R14 (lr) :00000000
R15 (pc) :00001000

CPSR Register
Negative (N) :0
Zero (Z) :0
Carry (C) :0
Overflow (V) :0
IRQ Disable:1
FIQ Disable:1
Thumb (T) :0
CPU Mode :System

0x000000df

fact.s

```
00001000:      main:  
00001000:E3A01004      mov r1, #4  
00001004:EB000002      bl fact  
00001008:E3A00001      MOV r0, #1      @ Load 1 into register r0 (stdout handle)  
0000100C:EF00006B      SWI 0x6b      @ Print integer in register r1 to stdout  
00001010:EF000011      SWI 0x11      @ Stop program execution  
  
00001014:E24DD008      fact: sub sp, sp, #8  
00001018:E58DE000      str lr, [sp,#0]  
0000101C:E58D1004      str r1, [sp,#4]  
00001020:E3510001      cmp r1,#1  
00001024:AA000002      bge L1  
00001028:E3A01001      mov r1, #1  
0000102C:E28DD008      add sp, sp, #8  
00001030:E1A0F00E      mov pc, lr  
00001034:E2411001      L1: sub r1, r1, #1  
00001038:EBFFFFFF5      BL fact  
0000103C:E1A02001      mov r2, r1  
00001040:E59D1004      ldr r1, [sp, #4]  
00001044:E59DE000      ldr lr, [sp, #0]  
00001048:E28DD008      add sp, sp, #8  
0000104C:E0010192      mul r1, r2, r1  
00001050:E1A0F00E      mov pc, lr
```

OutputView

Console Stdin/Stdout/Stderr

Loading assembly language file C:\Users\Li Liao\Desktop\fact.s

OutputView WatchView

CISC260 Tentative Schedule (S18)

#	Week	Topic
1	Feb5	Overview and Data representation
2	Feb12	Boolean logic, gates
3	Feb19	Build a simple computer
4	Feb26	ARM, ISA, Assembly Language
5	Mar5	Assembly programming
6	Mar12	Procedure call, stack
7	Mar19	Assembly programming and Review1
Midterm March 22		
8	Mar23	Spring break (no classes)
9	Apr2	Floating point
10	Apr9	Assembly programming: Dynamic data structure
11	Apr16	Assembler, Linker, Compiler (Nov.8 Election Day. no class)
12	Apr23	Performance and optimization
13	Apr30	I/O
14	May7	Assembly language programming and security
15	May15	Review2

