Multi-Channel PMIC for TFT-LCD TV Panels

General Description

The RT6971 is a programmable multi-functional power solution with integrated 19-CH of level shifter for TFT-LCD panel. It contains three Buck converters (VCC1, VCC2 & HAVDD), one Boost converter (VGH), one Buck-Boost converter (VGL2), VCOM1, VGH and VGL2 all have the temperature compensation function. A negative OP regulator (VGL1), 14-CH gamma buffers and 3-CH VCOM and 19-CH level shifter. All channel output level and sequence (Delay time) can be programmable by I2C interface.

With its high current capabilities, the device is ideal for large screen monitor panels and LCD TV applications with widely supply voltage range. The RT6971 is available in a VQFN-76L 8x8 package.

Ordering and Marking Information

Part No.	Marking Information	Package Type
RT6971	RT6971	VQFN-76L 8x8 (V-Type)

Features

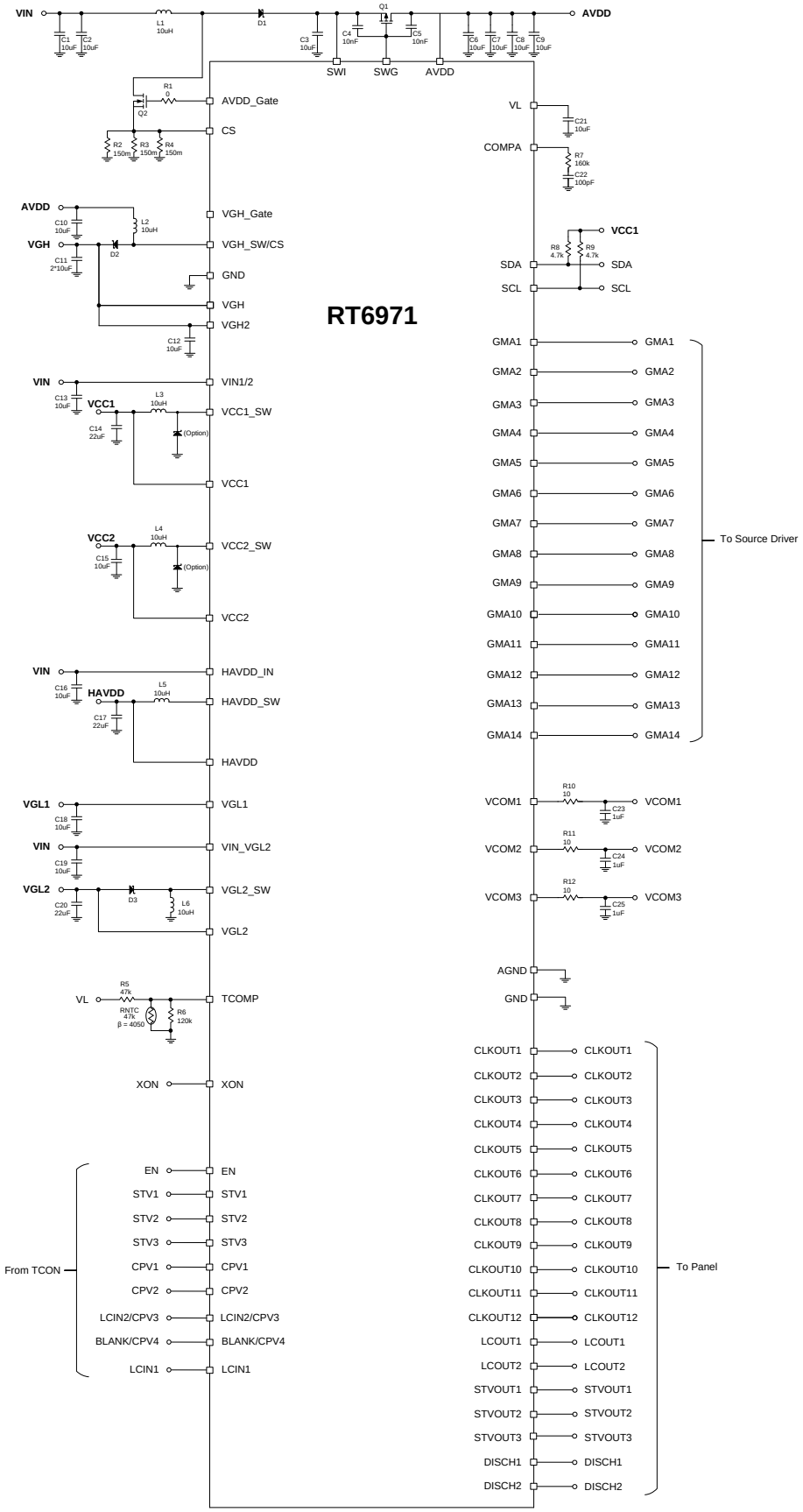
- **8.6V to 15.9V Input Supply Voltage**
- **Async. Boost Controller by 0.25/0.4V Over-Current Protection for AVDD with 13.8V to 20.0V Programmable Output**
- **1.5/3.2A Async. / Sync. Buck Converter for VCC1 with 0.8V to 2.36V Programmable Output**
- **1.2A Async. / Sync. Buck Converter for VCC2 with 0.8V to 3.7V Programmable Output**
- **2.0A Sync. Buck Converter for HAVDD with Programmable Output**
- **280mA Negative OP Regulator for VGL1 with -1.8V to -15V Programmable Output**
- **1.6A Async. Buck-Boost Converter for VGL2 with -4.5 to -20V Programmable Output**
- **1.6A Async. Boost Converter or Controller by 0.25V Over-Current Protection for VGH with 20 to 45V Programmable Output**
- **14-CH Gamma Buffers**
- **3-CH VCOM with Temp. Compensation (VCOM1)**
- **19-CH of Level Shifter Support 12 CLK's, STVOUT1, STVOUT2, STVOUT3, LCOUT1, LCOUT2, DISCH1, DISCH2**
- **Programmable Level Shifter OCP Level and Detection Time**
- **Suitable for 4/6/8/10/12-Phase Level Shifter Applications**
- **Over-Temperature Protection**
- **I^2C Compatible Interface for Register Control**

Applications

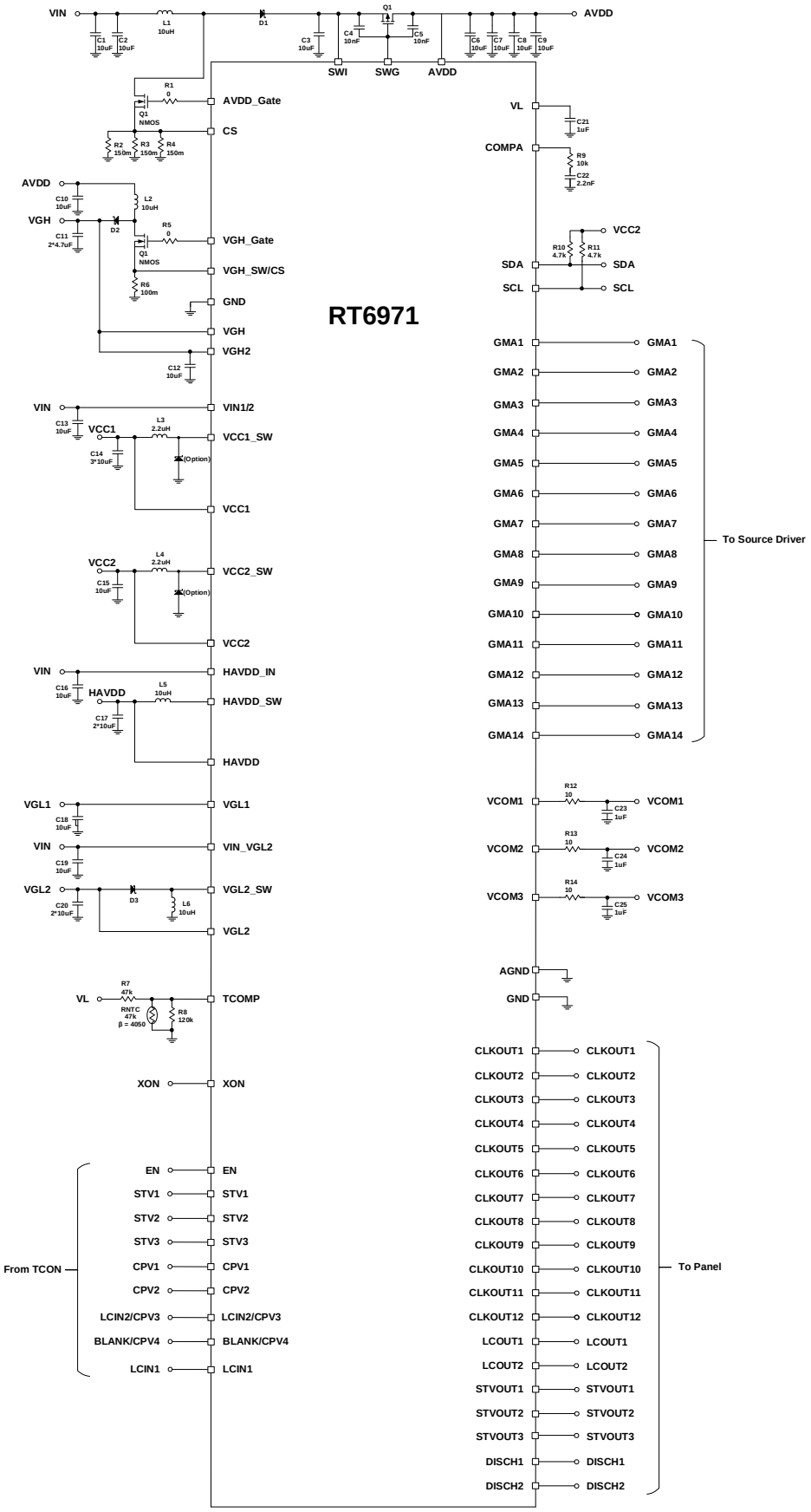
- TFT-LCD TV Panels
- TFT-LCD Monitor Panels

Typical Application Circuit

VGH Async. Converter

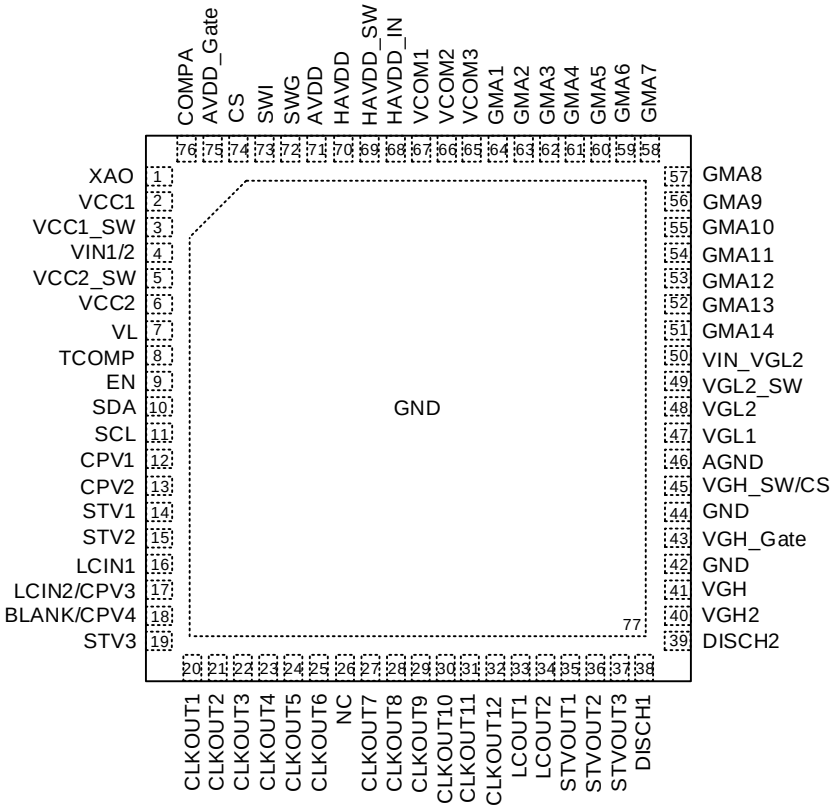


VGH Async. Controller



Pin Configuration

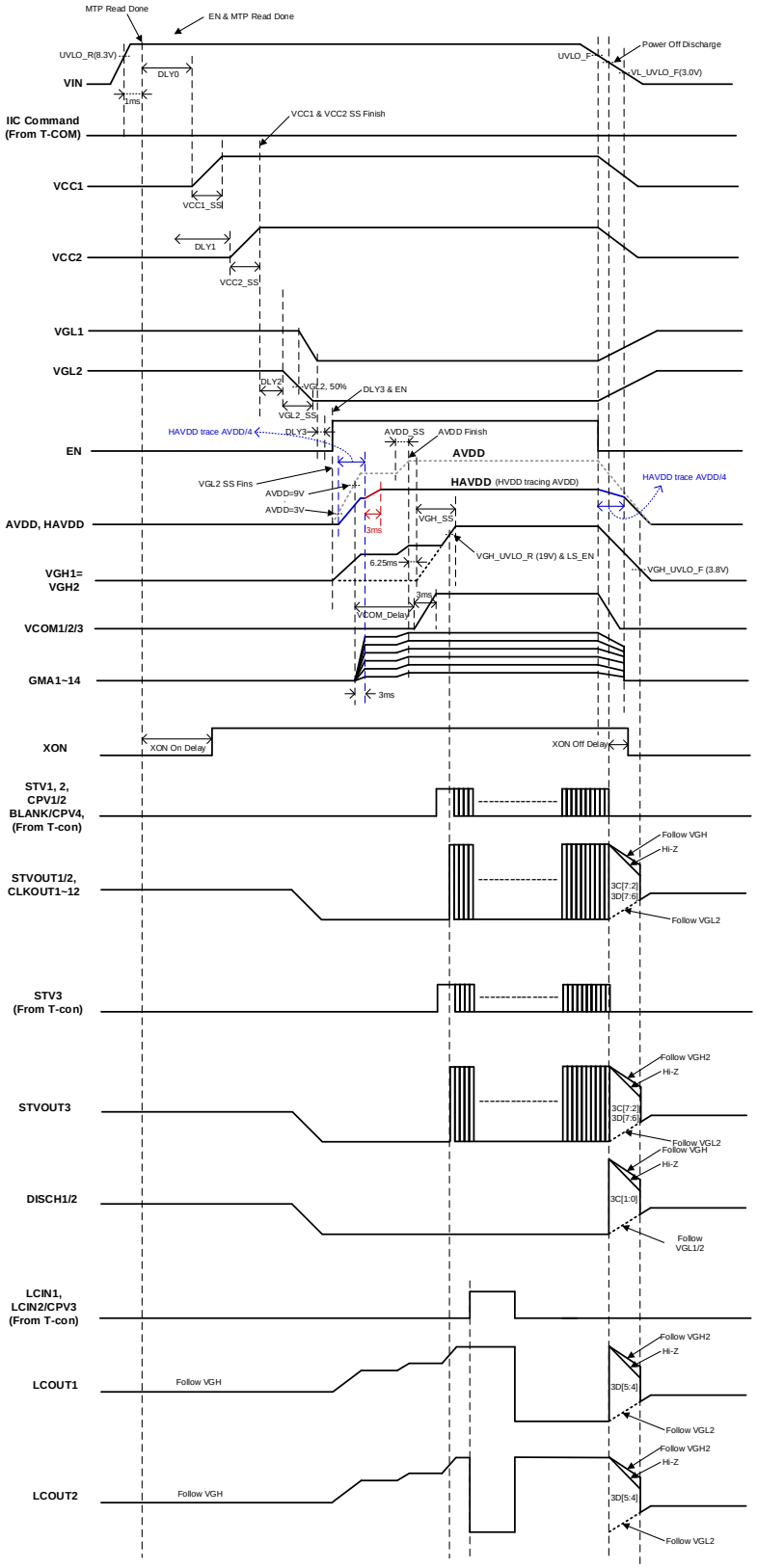
(TOP VIEW)



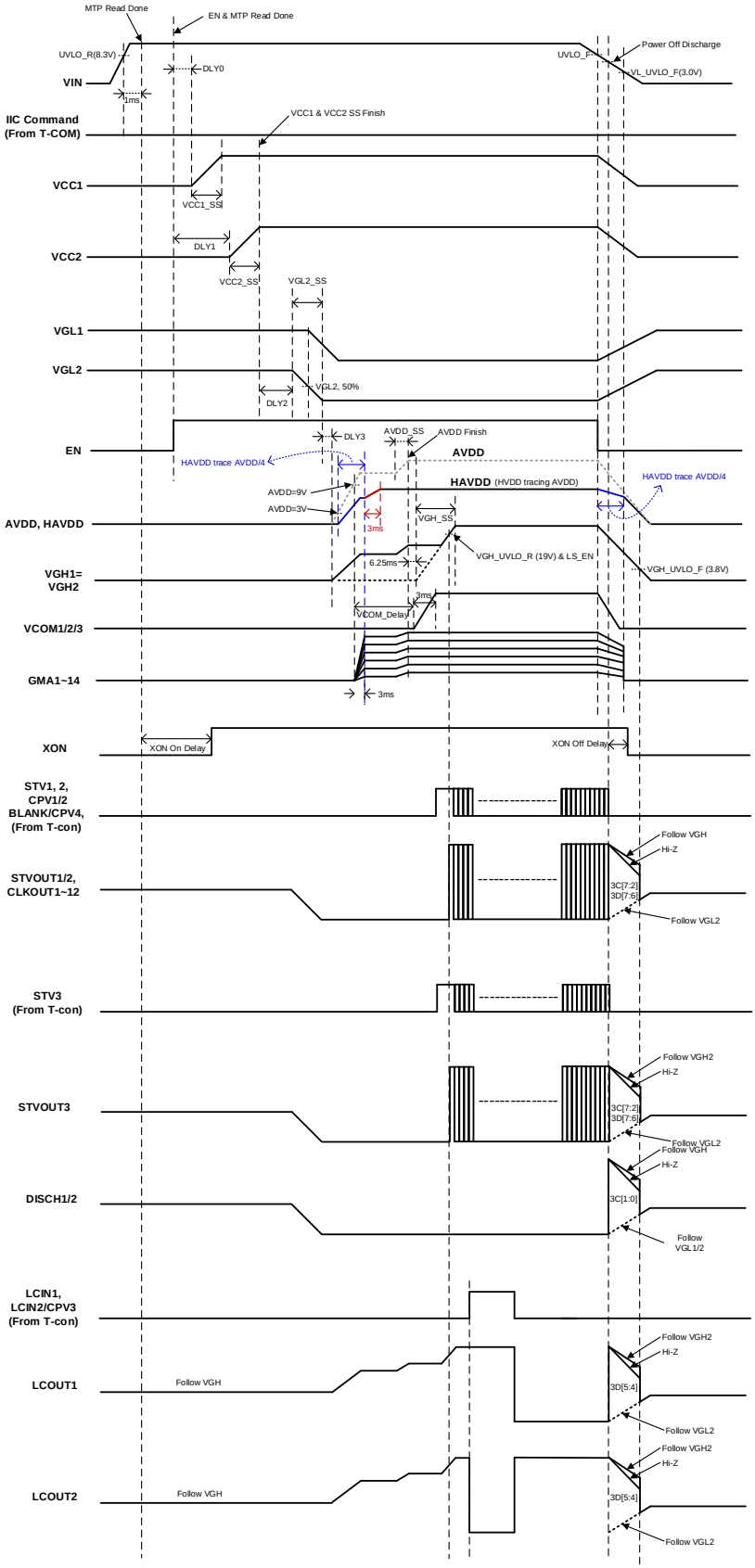
VQFN-76L 8x8

Timing Diagram

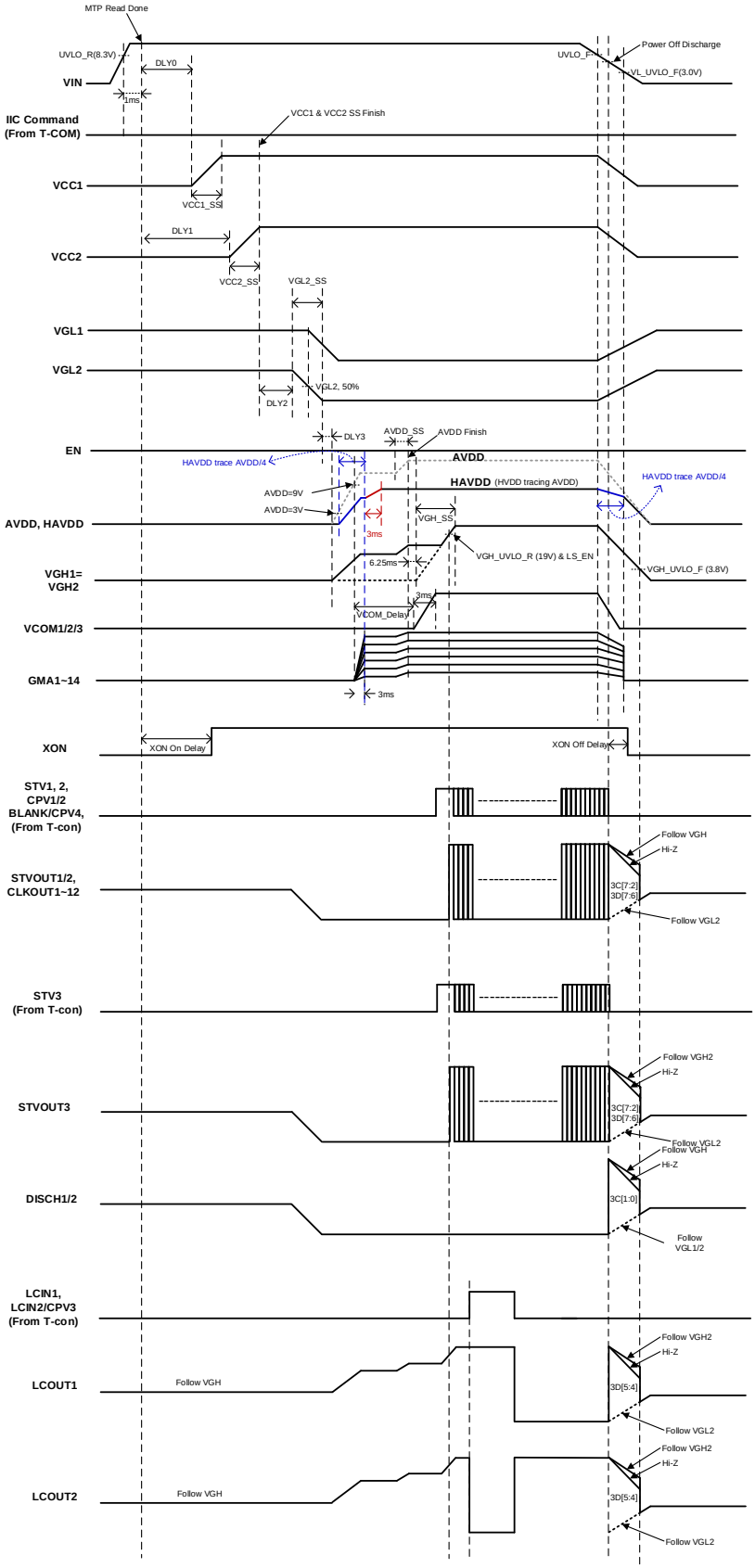
Power On/Off Timing Diagram



Case 1. EN_Type = 00



Case 2. EN_Type = 01



Case 3. EN_Type = 10 or 11

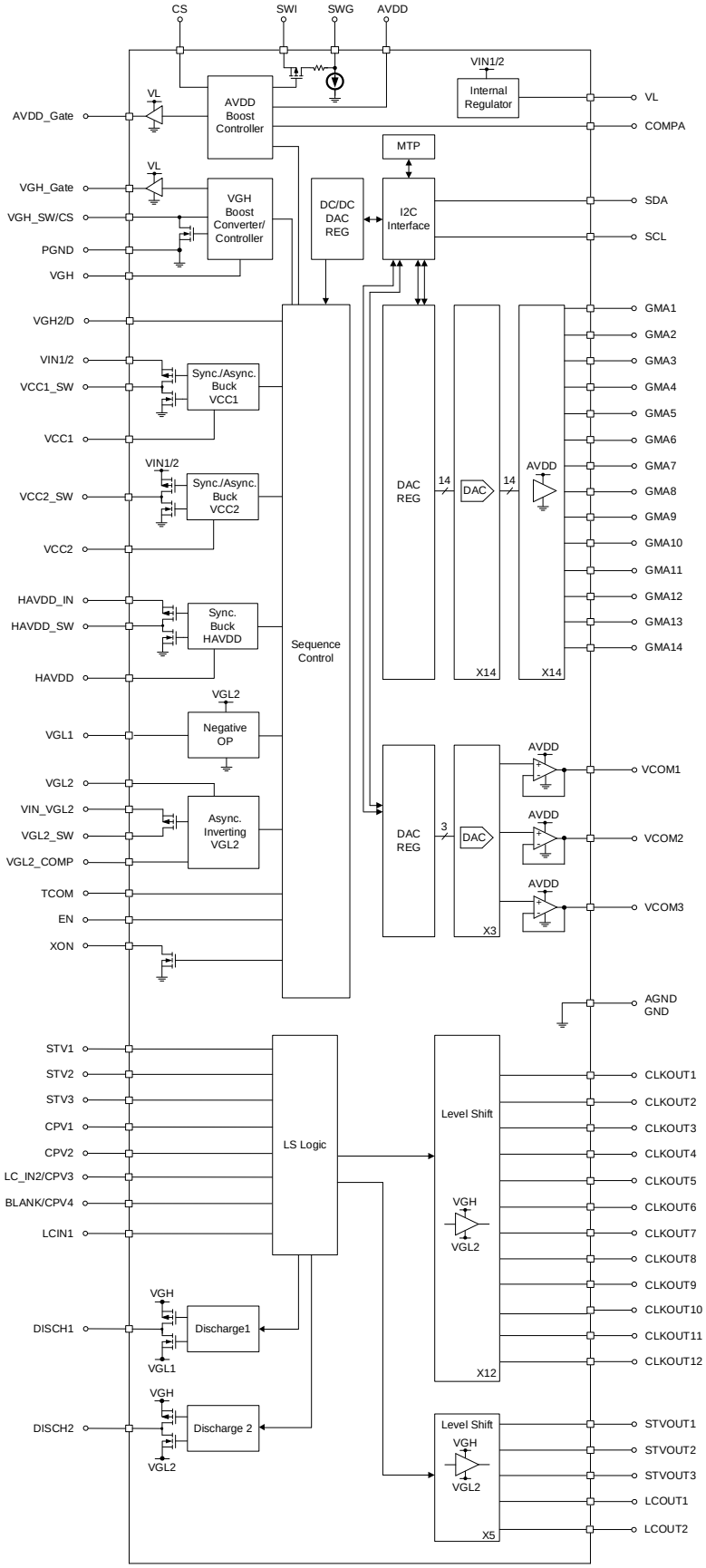
Functional Pin Description

Pin No.	Pin Name	Pin Function
1	XAO	Source driver / panel discharge signal.
2	VCC1	Output sensing for VCC1 buck converter.
3	VCC1_SW	VCC1 buck converter switch pin.
4	VIN1/2	Input supply pin (8.6V to 15.9V) for VCC1/2 output.
5	VCC2_SW	VCC2 buck converter switch pin.
6	VCC2	Output sensing for VCC2 buck converter.
7	VL	Internal regulator output pin.
8	TCOMP	Temperature compensation input pin for VGH & VGL2 & VCOM1.
9	EN	Enable signal input.
10	SDA	I2C DATA pin.
11	SCL	I2C CLOCK pin.
12	CPV1	Level shifter input signal.
13	CPV2	Level shifter input signal.
14	STV1	Level shifter input signal.
15	STV2	Level shifter input signal.
16	LCIN1	Level shifter input signal.
17	LCIN2/CPV3	Level shifter input signal.
18	BLANK/CPV4	Level shifter input signal.
19	STV3	Level shifter input signal.
20	CLKOUT1	Level shifter CLKOUT1 output.
21	CLKOUT2	Level shifter CLKOUT2 output.
22	CLKOUT3	Level shifter CLKOUT3 output.
23	CLKOUT4	Level shifter CLKOUT4 output.
24	CLKOUT5	Level shifter CLKOUT5 output.
25	CLKOUT6	Level shifter CLKOUT6 output.
26	NC	No internal connection.
27	CLKOUT7	Level shifter CLKOUT7 output.
28	CLKOUT8	Level shifter CLKOUT8 output.
29	CLKOUT9	Level shifter CLKOUT9 output.
30	CLKOUT10	Level shifter CLKOUT10 output.
31	CLKOUT11	Level shifter CLKOUT11 output.
32	CLKOUT12	Level shifter CLKOUT12 output.
33	LCOUT1	Level shifter LCOUT1 output.
34	LCOUT2	Level shifter LCOUT2 output.
35	STVOUT1	Level shifter STVOUT1 output.
36	STVOUT2	Level shifter STVOUT2 output.

Pin No.	Pin Name	Pin Function
37	STVOUT3	Level shifter STVOUT3 output.
38	DISCH1	Power Off Discharge output following VGL1.
39	DISCH2	Power Off Discharge output following VGL2.
40	VGH2	Positive voltage input for level shifter output terminal.
41	VGH	Output sensing for VGH boost converter and level shifter supply.
42, 44, 77 (Exposed Pad)	GND	Power ground, the exposed pad must be soldered to a large PCB and connected to PGND for maximum power dissipation.
43	VGH_Gate	Gate driver output for VGH boost converter. This pin is the output pin to driver and external N-MOSFET of VGH Boost Converter in case of using external switch.
45	VGH_SW/CS	Switching node or switch current sensing input of VGH boost converter. The pin is the drain of internal N-MOSFET in case of using internal switch and input of current sensing block of VGH Boost Converter in case of using external switch.
46	AGND	Analog ground.
47	VGL1	VGL1 output pin.
48	VGL2	Output sensing for VGL2 buck-boost converter. Input for level shift.
49	VGL2_SW	VGL2 buck-boost switching pin.
50	VIN_VGL2	Input supply pin (8.6V to 15.9V) for VGL2 output.
51	GMA14	P-gamma out CH14.
52	GMA13	P-gamma out CH13.
53	GMA12	P-gamma out CH12.
54	GMA11	P-gamma out CH11.
55	GMA10	P-gamma out CH10.
56	GMA9	P-gamma out CH9.
57	GMA8	P-gamma out CH8.
58	GMA7	P-gamma out CH7.
59	GMA6	P-gamma out CH6.
60	GMA5	P-gamma out CH5.
61	GMA4	P-gamma out CH4.
62	GMA3	P-gamma out CH3.
63	GMA2	P-gamma out CH2.
64	GMA1	P-gamma out CH1.
65	VCOM3	Output of VCOM amplifier 3.
66	VCOM2	Output of VCOM amplifier 2.
67	VCOM1	Output of VCOM amplifier 1.
68	HAVDD_VIN	HAVDD input supply (VIN or AVDD).
69	HAVDD_SW	HAVDD buck converter switch pin.
70	HAVDD	Output sensing for HAVDD buck converter.

Pin No.	Pin Name	Pin Function
71	AVDD	Output sensing for AVDD boost converter.
72	SWG	Gate input of the external Isolation MOSFET.
73	SWI	Input of the Isolation MOSFET.
74	CS	AVDD boost converter current sense.
75	AVDD_Gate	AVDD boost converter external NMOS gate driver.
76	COMPA	AVDD boost compensation pin.

Functional Block Diagram



Absolute Maximum Ratings (Note1)

- VIN1/2 , VIN_VGL2, HAVDD to GND ---------- –0.3V to 21V
- HAVDD_IN, VCOM_IN, AVDD, SWI, SWG, AVDD_CS to GND ---------- –0.3V to 22V
- EN, VL, TCOMP, VGL2_COMP, COMPA, SDA, SCL, AVDD_Gate, VGH_Gate, VCC1, VCC2, XAO, STV1, STV2, STV3, CPV1, CPV2, LCIN1, LCIN2/CPV3, BLANK/CPV4 to GND ---------- –0.3V to 6V
- VCC1_SW, VCC2_SW to GND ---------- –0.3V to (VIN1/2 + 0.3V)
- HAVDD_SW to GND ---------- –0.3V to (HAVDD_IN + 0.3V)
- VGH, VGH_SW/CS to GND ---------- –0.3V to 49V
- VGL2_SW to VIN_VGL2 ---------- –40V to 0.3V
- GMA1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14 to GND ---------- –0.3V to (AVDD + 0.3V)
- VCOM1, VCOM2, VCOM3 to GND ---------- –0.3V to (AVDD + 0.3V)
- VGL1 to GND ---------- –18V to 0.3V
- VGL2 to GND ---------- –24V to 0.3V
- VGH to VGL2 ---------- –0.3V to 58V
- VGH to VGL1 ---------- –0.3V to 58V
- (CLKOUT1 to CLK1OUT2), STVOUT1, STVOUT2, STVOUT3, DISCH2 to GND --- (VGL2 – 0.3V) to (VGH + 0.3V)
- DISCH1 to GND ---------- (VGL1 – 0.3V) to (VGH + 0.3V)
- LCOUT1, LCOUT2 to GND ---------- –0.3V to (VGH + 0.3V)
- Power Dissipation, P_D @ T_A = 25°C
  VQFN-76L 8x8 ---------- 4.01W
- Package Thermal Resistance (Note 2)
  VQFN-76L 8x8, θ_{JA} ---------- 24.9°C/W
  VQFN-76L 8x8, θ_{JC} ---------- 3.3°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Ambient Temperature Range ---------- –40°C to 85°C
- Junction Temperature Range ---------- –40°C to 125°C
- Case Temperature Range (Note 5) ---------- –40°C to 100°C

Electrical Characteristics

(V_{IN} =12.7V, V_{AVDD} =16V, V_{CC1} = 1.8V, V_{CC2} = 3.3V, V_{HAVDD} = 8V, V_{GH} = 28V, V_{GL1} = –5V, V_{GL2} = –10.1V, T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Current							
Input Voltage Range		V_{IN}		8.6	--	15.9	V
VIN Quiescent Current			All SW pins not switching	--	3.5	6.5	mA
VIN Under-Voltage Lockout Threshold		V_{IN_UVLO}	Hysteresis	--	0.8	--	V
			V_{IN} rising	6.5	--	8	
VL Output Voltage		V_L	No Load	4.8	5	5.2	V
VL Under-Voltage Lockout Threshold		V_{L_UVLO}	V_{IN} falling	--	3	--	V
Fault Detection							
Fault Trigger Duration				40	50	60	ms
Thermal Shutdown Threshold			Temperature rising	135	150	165	°C
Thermal Shutdown Hysteresis				13.5	15	16.5	°C
Logic Inputs (EN, SDA, SCL, STV1, STV2, STV3, CPV1, CPV2, LCIN2/CPV3, BLANK/CPV4, LCIN1)							
Input Voltage	Logic-High	V_{IH}		1.3	--	--	V
	Logic-Low	V_{IL}		--	--	0.8	
EN Pull Low Resistance		R_{EN}		--	400	--	kΩ
SDA, SCL Input Leakage Current		I_{IH}, I_{IL}	V_{IN} = 0 or 3.3V	–1	0.01	1	µA
SDA, SCL Input Capacitance				--	5	--	pF
SDA Output Low Voltage		V_{OL}	I_{SINK} = 6mA	--	0.3	0.45	V
I^2C Timing Characteristics							
Serial-Clock Frequency		f_{SCL}		1	--	400	kHz
Bus Free Time Between STOP and START Conditions		t_{BUF}		1.3	--	--	µs
Hold Time (Repeated) START Condition		$t_{HD,STA}$		0.6	--	--	µs
SCL Pulse-Width Low		t_{LOW}		1.3	--	--	µs
SCL Pulse-Width High		t_{HIGH}		0.6	--	--	µs
Setup Time for a Repeated START Condition		$t_{SU,STA}$		0.6	--	--	µs
Data Hold Time		$t_{HD,DAT}$		0	--	800	ns
Data Setup Time		$t_{SU,DAT}$		100	--	--	ns
SDA and SCL Receiving Rising Time		t_R		20 + 0.1C_B	--	300	ns

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SDA and SCL Receiving Falling Time	t_F		20 + 0.1C_B	--	300	ns
SDA Transmitting Fall Time	t_F		20 + 0.1C_B	--	250	ns
Setup Time for STOP Condition	t_{SU_STOP}		0.6	--	--	µs
Bus Capacitance	C_B		--	--	400	pF
Pulse Width of Suppressed Spike	t_{SP}		--	85	--	ns
FAULT Indicator						
FAULT Output Low Voltage	V_{OL_FAULT}	I_{FAULT} = 2mA	--	V_L x 0.12	--	V
Boost Controller (AVDD)						
Output Voltage Range	V_{AVDD}	AVDD > VIN + 2V	13.8		20	V
Maximum Duty Cycle	D_{MAX_AVDD}		--	90	--	%
Output Voltage Accuracy	V_{AVDD_ACC}	AVDD=16V, No load	-1.5	--	1.5	%
Operating Frequency	f_{SW_AVDD}	2Ah[4]=1h	450 (–10%)	500	550 (+10%)	kHz
		2Ah[4]=0h	675 (–10%)	750	825 (+10%)	kHz
Load Regulation	ΔV_{AVDD_LOAD}	AVDD = 16V, 0A < I_{LOAD} < 1A	--	0.2	--	%/A
Line Regulation	ΔV_{AVDD_LINE}	VIN = 8.6V to 15.9V (I_{LOAD} = 1mA)	--	0.1	--	%/V
Output Resolution	Res	100mV/Step	--	0.1	--	V
A_CS Threshold Voltage	V_{CSA}	AVDD_CS Resistor = 0.05Ω	--	5	--	A
			--	8	--	
AVDD_Gate Output Voltage	V_{GATE}		0	--	VL	V
Soft Start Period	t_{SS_AVDD}	Programmable Soft-Start Time, t_{SS_AVDD} 2Ah[6:5], 5m/10m/15m/20ms, Default=00h	5	--	20	ms
Fault Trip Level		AVDD falling	--	AVDD x 80%	--	V
Short Circuit Level	V_{SC_AVDD}	AVDD falling	--	4	--	V
OVP Level		AVDD rising	20	21	22	V
OVP Hysteresis				1.5		V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Off Discharge Resistance	R_{DISCHG_AVDD}			0.8		kΩ
Isolation Switch (GD)						
GD Pull Down Voltage	V_{GD}	V_{SWI} - V_{SWG}	5	6	7	V
SWG to SWI Pull Up Resistance	R_{UP_GD}		8	12	16	kΩ
SWG Sink Current	I_{SNK_SWG}		10	20	30	μA
Sync./Async. Buck Converter (VCC1)						
Output Voltage Range	V_{CC1}	Register address: “01h” 6bits, V_{CC1} = (0.8V to 2.36V) [00h to 4Eh], Resolution: 0.02V	0.8	--	2.36	V
Output Accuracy		No load, default output	-2	--	2	%
Operating Frequency	f_{SW_VCC1}	27h[3]=0h	675 (−10%)	750	825 (+10%)	kHz
		27h[3]=1h	450 (−10%)	500	550 (+10%)	
Maximum Duty Cycle	D_{MAX_VCC1}		--	90	--	%
VIN_VCC1 to VCC1_SW P-MOSFET On-Resistance	$R_{DSON\_HS\_VCC1}$	I_{VCC1_SW} = 500mA	--	300	--	mΩ
VCC1_SW to GND N-MOSFET On-Resistance	$R_{DSON\_LS\_VCC1}$	I_{VCC1_SW} = 500mA	--	400	--	mΩ
VCC1_SW Positive Current Limit	I_{LIM_VCC1}	0x40h[7]=0	1.5	--	--	A
		0x40h[7]=1	3.2	--	--	A
VIN_VCC1 to VCC1_SW P-MOSFET Leakage Current	$I_{LK\_VCC1\_SW}$	V_{VCC1_SW} = 0V	--	1	10	μA
Soft-Start Time	t_{SS_VCC1}	01h[7]=0	--	1	--	ms
		01h[7]=1	--	3	--	ms
Fault Trip Level		V_{CC1} falling	--	VCC1 x 65%	--	V
Short Circuit Level	V_{SC_VCC1}	V_{CC1} falling	--	VCC1 x 20%	--	V
OVP Level		V_{CC1} rising, hysteresis=0.11V	--	VCC1 x 120%	--	V
Line Regulation		8.6V ≤ V_{IN} ≤ 15.9V, I_{out_VCC1} = 1mA	--	0.1	--	%/V
Load Regulation		50mA ≤ I_{out_VCC1} ≤ 500mA	--	0.2	--	%
Power Off Discharge Resistance	R_{DISCHG_VCC1}		--	0.3	--	kΩ

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Sync./Async. Buck Converter (VCC2)						
Output Voltage Range	V_{CC2}	Register address: “02h” 5bits, V_{CC2} = (0.8V to 3.7V) [00h to 0Fh], Resolution: 0.1V	0.8	--	3.7	V
Output Accuracy		No load, default output	-2	--	2	%
Operating Frequency	f_{SW_VCC2}	27h[3]=0h	675 (−10%)	750	825 (+10%)	kHz
		27h[3]=1h	450 (−10%)	500	550 (+10%)	
Maximum Duty Cycle	D_{MAX_VCC2}		--	90	--	%
VIN_VCC2 to VCC2_SW P-MOSFET On-Resistance	$R_{DSON\_HS\_VCC2}$	I_{VCC2_SW} = 200mA	--	300	--	mΩ
VCC2_SW to GND N-MOSFET On-Resistance	$R_{DSON\_LS\_VCC2}$	I_{VCC2_SW} = 200mA	--	400	--	mΩ
VCC2_SW Positive Current Limit	I_{LIM_VCC2}		1.2	--	--	A
VIN_VCC2 to VCC2_SW P-MOSFET Leakage Current	$I_{LK\_VCC2\_SW}$	V_{VCC2_SW} = 0V	--	1	10	μA
Soft-Start Time	t_{SS_VCC2}	02h[7]=0	--	1	--	ms
		02h[7]=1	--	3	--	ms
Fault Trip Level		V_{CC2} falling	--	VCC2 x 65%	--	V
Short Circuit Level	V_{SC_VCC2}	V_{CC2} falling	--	VCC2 x 20%	--	V
OVP Level		V_{CC2} rising, hysteresis=0.11V	--	VCC2 x 120%	--	V
Line Regulation		8.6V ≤ V_{IN} ≤ 15.9V, I_{out_VCC2} = 1mA	--	0.1	--	%/V
Load Regulation		50mA ≤ I_{out_VCC2} ≤ 500mA	--	0.2	--	%
Power Off Discharge Resistance	R_{DISCHG_VCC2}		--	0.3	--	kΩ
Sync. Buck Converter (HAVDD)						
Adjustable Output Voltage Range	V_{HAVDD}		GLDO[4:0]* ((HAVDD[9:0]+1)/1024)			V
Recommended Output Voltage Range	V_{HAVDD_RANGE}	Note 8	4	--	12	V
Output Accuracy		No load, default output, tracking with AVDD	−1.5%	1/2 x AVDD	1.5%	V
Operating Frequency	f_{SW_HAVDD}	0x2A[4]=0h, 0x2A[3]=0h	675 (−10%)	750	825 (+10%)	kHz
		0x2A[4]=0h, 0x2A[3]=1h	1350 (−10%)	1500	1650 (+10%)	kHz
		0x2A[4]=1h, 0x2A[3]=0h	450 (−10%)	500	550 (+10%)	kHz

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
		0x2A[4]=1h, 0x2A[3]=1h	900 (−10%)	1000	1100 (+10%)	kHz
HAVDD_VIN to HAVDD_SW P-MOSFET On-Resistance	$R_{DSON\_HS\_HAVDD}$	I_{HAVDD_SW} = 100mA	--	270	--	mΩ
HAVDD_SW Positive Current Limit	$I_{LIM\_P\_HAVDD}$		2.0	--	--	A
HVADD_VIN to HAVDD_SW P-MOSFET Switch Leakage Current	$I_{LEAK\_P\_HAVDD\_SW}$	V_{SW} = 0V	--	1	--	μA
HAVDD_SW to HAVDD_PGND N-MOSFET On-Resistance	$R_{DSON\_LS\_HAVDD}$		--	250	--	mΩ
SW Negative Current Limit	$I_{LIM\_N\_HAVDD}$		2.0	--	--	A
HAVDD_SW to HAVDD_PGND N-MOSFET Switch Leakage Current	$I_{LEAK\_N\_HAVDD\_SW}$	V_{SW} = 0V	--	1	--	μA
Soft-Start Time	t_{SS_HAVDD}	Tracking with AVDD	--	1.5	--	ms
Fault Trip Level		HAVDD falling	--	V_{HAVDD} x 65%	--	V
Short Circuit Level	V_{SC1_HAVDD}	HAVDD_SW switching frequency reduced to f_{OSC_HAVDD} / 2	--	4.8	--	V
	V_{SC2_HAVDD}	HAVDD_SW stop switching	--	2.4	--	
Over-Voltage Level		HAVDD rising	--	V_{HVDD} x 120%	--	V
Power Off Discharge Resistance	R_{DISCHG_HVDD}		--	0.5	--	kΩ
Line Regulation		8.6V ≤ V_{IN} ≤ 15.9V, I_{OUT_HAVDD} = 1mA	--	0.1	--	%/V
Load Regulation		1mA ≤ I_{OUT_HVDD} ≤ 500mA	--	0.2	--	%
Power Off Discharge Resistance	R_{DISCHG_HAVDD}		--	0.5	--	kΩ
Negative OP Regulator (VGL1)						
Adjustable Room Temperature Output Voltage Range	V_{GL1}	Register address = ”05h”, 7 bits/128 steps, V_{GL} = (−1.8V to −15.0V) [00h to 42h] , Resolution = 0.2V	-15	--	−1.8	V
Output Accuracy		Default code	−3		3	%
Output short source current	$I_{O\_SC\_HS}$		0.21	0.28	0.35	A
Output short sink current	$I_{O\_SC\_LS}$		0.21	0.28	0.35	A
Soft-Start Time	t_{SS_VGL1}		--	1.5	--	ms

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VGL1 Fault Trip Level		V_{GL1} rising	--	V_{GL1} + 1.8	--	V
VGL1 Short Circuit Level	V_{SC_VGL1}	V_{GL1} rising	--	–1.3	--	V
Power Off Discharge Resistance	R_{DISCHG_VGL1}		--	0.2	--	kΩ
Load Regulation		10mA< I_{LOAD} < 30mA	--	0.2	--	%
Power Off Discharge Resistance	R_{DISCHG_VGL1}		--	0.2	--	kΩ
Async. Buck-Boost Converter (VGL2)						
Adjustable Room Temperature Output Voltage Range (VGL2_LT)	V_{GL2_LT}	Register address = ”06h”, 7 bits/128 steps, [00h to 4Dh] Resolution = 0.2V [4Dh to 4Eh] Resolution = 0.1V	–20	--	–4.5	V
Adjustable High Temperature Output Voltage Range (VGL2_HT)	V_{GL2_HT}	Register address = ”07h”, 7 bits/128 steps, [00h to 4Dh] Resolution = 0.2V [4Dh to 4Eh] Resolution = 0.1V	–20	--	–4.5	V
Output Accuracy		Default code	–2%	--	2%	V
Operating Frequency	f_{SW_VGL2}	0x2A[1]=0h	675 (–10%)	750	825 (+10%)	kHz
		0x2A[1]=1h	450 (–10%)	500	550 (+10%)	kHz
High-side On-Resistance			--	500	--	mΩ
Maximum Duty Cycle			80	90	--	%
Minimum On-time			--	100	--	ns
VGL2_SW Positive Current Limit	I_{LIM_VGL2}		1.6	--	--	A
Switch Leakage Current	I_{leak_VGL2}	V_{GL2_SW} = V_{IN} or V_{GL2}	--	5	--	μA
Soft Start Time	t_{SS_VGL2}		--	3	--	ms
VGL2 Fault Trip Level		V_{GL2} rising	--	VGL2 x 75%	--	%
VGL2 Short Circuit Level	V_{SC_VGL2}	V_{GL2} rising	--	–2.5	--	V
VGL2 OVP level		V_{GL2} falling, hysteresis=0.5V	--	–22.5	--	V
Line Regulation		8.6V ≤ V_{IN} ≤ 15.9V, I_{OUT_VGL2} = 0.1A	--	0.1	--	%/V
Load Regulation		0mA ≤ I_{OUT_VGL2} ≤ 150mA	--	0.2	--	%
Power Off Discharge Resistance	R_{DISCHG_VGL2}		--	0.2	--	kΩ
Async. Boost Converter (VGH)						
Adjustable Low Temperature Output Voltage Range (VGH_LT)	V_{GH_LT}	Register Address = ”03h”, 7 bits, V_{GH_LT} = (21V to 45V) [00h to 78h], Resolution = 0.2V	21	--	45	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Adjustable Room Temperature Output Voltage Range (VGH_HT)	V_{GH_HT}	Register Address = ”04h”, 7bits, V_{GH_HT} = (20V to 44V) [00h to 78h], Resolution = 0.2V	20	--	44	V
Output Accuracy			–3	--	3	%
Operating Frequency	f_{SW_VGH}	0x2A[4]=0h, 0x2A[3]=0h	675 (–10%)	750	825 (+10%)	kHz
		0x2A[4]=0h, 0x2A[3]=1h	1350 (–10%)	1500	1650 (+10%)	kHz
		0x2A[4]=1h, 0x2A[3]=0h	450 (–10%)	500	550 (+10%)	kHz
		0x2A[4]=1h, 0x2A[3]=1h	900 (–10%)	1000	1100 (+10%)	kHz
VGH_SW to GND N-MOSFET On-Resistance	$R_{DSON\_LS\_VGH}$		--	350	--	mΩ
Soft-Start Time	t_{SS_VGH}	Programmable Soft-Start Time, t_{SS_VGH} 2Ah[7], 3m/6ms, Default=0h	3	--	6	ms
VGH Fault Trip Level		V_{GH} falling	--	VGH x 70%	--	V
VGH Short Circuit Level		V_{GH} falling	--	VGH x 20%	--	V
VGH Over Voltage Level	V_{GH_OVP}	V_{GH} Rising, hysteresis=1V	--	47.5	--	V
VGH_SW Leakage Current		V_{GH_SW} = 44V	--	1	--	μA
VGH_SW Current Limit	I_{LIM}		1.6	--	--	A
Power Off Discharge Resistance	R_{DISCHG_VGH}		--	1.5	--	kΩ
Line Regulation		V_{AVDD} = 14V to 18V, (I_{OUT_VGH} =100mA)	--	0.1	--	%/V
Load Regulation		10mA < I_{OUT_VGH} < 100mA	--	0.2	--	%
Power Off Discharge Resistance	R_{DISCHG_VGH}		--	1.5	--	kΩ
External N-MOSFET Gate Driver (VGH_Gate)						
Gate High Voltage	DGate_OH		4.5	5	5.5	V
Gate Low Voltage	DGate_OL		--	--	0.3	V
External NMOS Switch Current Limit	$V_{GH\_CS\_OCP}$	R_{CS}=100mΩ	0.2	0.25	0.3	V
GAMMA Outputs (GMA1 to GMA14)						
Output Voltage Range	V_{GMA}		GLDO[4:0]* ((GMA[9:0]+1)/1024)			V
VCOM Resolution	Res		--	10	--	bits
Soft-Start Time	t_{SS_GMA}		--	3	--	ms
Integral Nonlinearity	INL_{GMA}		–1	--	1	LSB

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Integral Nonlinearity Margin	INL_{margin_GMA}		–4	--	4	LSB
Differential Nonlinearity	DNL_{GMA}		–1	--	1	LSB
Continuous Current	I_{CON_GMA}	VOUT drop 0.5V	--	30	--	mA
Short-Circuit Current	I_{SC_GMA}	Outputs to V_{AVDD} or GND	--	±200	--	mA
Output Impedance	Z_{O_GMA}	Output resistance when output is disabled	--	300	--	kΩ
Program to Output Delay	t_{D_GMA}	From ACK falling edge to start-up point of programming gamma voltage	--	0.5	--	μs
Load Regulation	LR_{GMA}	12mA & 12mA, Code = 256	--	±0.5	--	mV/ mA
VCOM (VCOM1, VCOM2 and VCOM3)						
VCOM Output Range	VCOM1~3		GLDO[4:0]* ((VCOM[9:0]+1)/1024)			V
VCOM Resolution	Res		--	10	--	bits
Soft-Start Time	t_{SS_VCOM}		--	3	--	ms
Integral Nonlinearity	INL_{VCOM}		–1	--	1	LSB
Integral Nonlinearity Margin	INL_{margin_VCOM}		–4	--	4	LSB
Differential Nonlinearity	DNL_{VCOM}		–1	--	1	LSB
Program to Output Delay	t_{D_VCOM}	From ACK falling edge to start-up point of programming VCOM voltage	--	0.5	--	μs
Input Offset Voltage	V_{OS}	OP-Amp Outx = V_{AVDD} / 2	--	2	25	mV
Input Bias Current	I_B	OP-Amp Outx = V_{AVDD} / 2	--	2	100	nA
Load Regulation	ΔV_{LOAD}	Sink current, I_{LOAD} = 0 to -80mA	--	0.1	--	mV/ mA
		Source current, I_{LOAD} = 0 to +80mA	--	0.1	--	mV/ mA
Common Mode Input Range	CMIR	OP-Amp Outx = V_{AVDD} / 2	0.5	--	V_{AVDD} –0.5	V
Common Mode Rejection Ratio	CMRR	0.5V ≤ OP-Amp Outx ≤V_{AVDD}-0.5V	--	95	--	dB
Open Loop Gain	AV_{OL}	0.5V ≤ OP-Amp Outx ≤ V_{AVDD}-0.5V	--	80	--	dB

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply Rejection Ratio		PSRR	OP-Amp Outx = V_{AVDD} / 2	--	96	--	dB
Output Swing Low		V_{OL}	I_{LOAD} = -50mA	--	0.6	1.5	V
Output Swing High		V_{OH}	I_{LOAD} = +50mA	V_{AVDD} –1.5	V_{AVDD} –0.6	--	V
Short-Circuit Current		I_{SC_VCOM}	Outputs to V_{AVDD} or PGND	--	±400	--	mA
Slew Rate		SR	OP-Amp Outx = 4V step, 20% to 80%, AV = 1, R_L = 10kΩ, C_L = 100pF	--	35	--	V/μs
Gain-Bandwidth Product		GBWP	R_L = 10kΩ, C_L = 10pF	--	12	--	MHz
Phase Margin		PM	R_L = 10kΩ, C_L = 10pF	--	50	--	degree
Level Shifter							
Power Supplies		$V_{GH, GH2}$		20	--	45	V
		V_{GL2}		–20	--	–4.5	
		V_{GL1}		–15		–1.8	
		$V_{GH, GH2 - VGL}$		--	--	57	
Positive (VGH) Power Supply Current		I_{VGH}		--	TBD	--	mA
Positive (VGH2) Power Supply Current		I_{VGH2}		--	TBD	--	mA
Negative (VGL1) Power Supply Current		I_{VGL1}		--	0.05	--	mA
Negative (VGL2) Power Supply Current		I_{VGL2}		--	0.2	--	mA
VGH UVLO Threshold		V_{UVLO_VGH}	VGH rising	--	19	--	V
			VGH falling	--	3.8	--	
Input Voltage	Logic-High	V_{IH_LVSFT}	Input rising for STV1, STV2, STV3, CPV1, CPV2, LCIN1, LCIN2/CPV3, BLANK/CPV4	1.3	--	--	V
	Logic-Low	V_{IL_LVSFT}	Input falling for STV1, STV2, STV3, CPV1, CPV2, LCIN1, LCIN2/CPV3, BLANK/CPV4	--	--	0.8	
Input Current		I_{IN_LVSFT}	STV1, STV2, STV3, CPV1, CPV2, LCIN1, LCIN2/CPV3, BLANK/CPV4 = 0V	–100	--	100	nA
			STV1, STV2, STV3, CPV1, CPV2, LCIN1, LCIN2/CPV3, BLANK/CPV4 = 3.3V	4	--	10	μA
CLKOUT1 to CLKOUT12 P-MOSFET Resistance		R_{dson_P1}	I_{OUT} = 10mA, sourcing	--	5	--	Ω

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
CLKOUT1 to CLKOUT12 N-MOSFET Resistance	R_{dson_N1}	I_{OUT} = 10mA, sinking	--	4	--	Ω
High side resistance of STVOUT1, STVOUT2, STVOUT3 LCOUT1, LCOUT2 DISCH1, DISCH2	R_{dson_P3}	I_{OUT} = 10mA, sourcing	12	20	50	Ω
Low side resistance of STVOUT1, STVOUT2, STVOUT3 LCOUT1, LCOUT2 DISCH1, DISCH2	R_{dson_N3}	I_{OUT} = 10mA, sinking	7	10	30	Ω
CLKOUT1 to CLKOUT12 Rising / Falling Slew Rate (Note 6)	t_R	VGH = 28V, VGL1 = -5V, VGL2 = -15.1V, R_L = 51Ω, C_L = 4.7nF, 20% to 80%	--	1000	--	V/us
			--	700	--	
			--	400	--	
			--	100	--	
	t_F	VGH = 28V, VGL1 = -5V, VGL2 = -15.1V, R_L = 51Ω, C_L = 4.7nF, 80% to 20%	--	1000	--	
			--	700	--	
			--	400	--	
			--	100	--	
Rising Propagation Delay (Note 7)	t_{PHG1}	No Load	--	50	70	ns
Falling Propagation Delay2 (Note 7)	t_{PHG2}	No Load	--	50	70	ns
High side current limit of CLKOUT1~CLKOUT12	I_{GOCP_P}	Tolerance : ±10%	20	--	270	mA
Low side current limit of CLKOUT1~CLKOUT12	I_{GOCP_N}	Tolerance : ±10%	20	--	270	mA
High side current limit of STVOUT1, STVOUT2, STVOUT3	I_{SOCP_P}	Tolerance : 50mA@±10%, others ±30%	20	--	135	mA
Low side current limit of STVOUT1, STVOUT2, STVOUT3	I_{SOCP_N}	Tolerance : 50mA@±10%, others ±30%	20	--	135	mA
High side current limit of LCOUT1, LCOUT2	I_{EOCP_P}	Tolerance : 30mA@±10%, others ±30%	10	--	135	mA
Low side current limit of LCOUT1, LCOUT2	I_{EOCP_N}	Tolerance : 30mA@±10%, others ±30%	10	--	135	mA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Low side current limit of DISCH1, DISCH2	I_{EOCP_N}	Tolerance : 50mA@±10%, others ±30%	40	--	135	mA
High side OCP sensing time of CLKOUT1~CLKOUT12	GOCP_P	Tolerance : ±10%	1	--	8.5	µs
Low side OCP sensing time of CLKOUT1~CLKOUT12	GOCP_N	Tolerance : ±10%	1	--	8.5	µs
High side OCP sensing time of STVOUT1, STVOUT2, STVOUT3	GOCP_P	Tolerance : 2µs@±20%, others ±30%	1	--	8.5	µs
Low side OCP sensing time of STVOUT1, STVOUT2, STVOUT3	GOCP_N	Tolerance : 2µs@±20%, others ±30%	1	--	8.5	µs
High side OCP sensing time of LCOUT1, LCOUT2	EOCP_P	Tolerance : 80µs@±20%, others ±30%	10	--	160	µs
Low side OCP sensing time of LCOUT1, LCOUT2, DISCH1, DISCH2	EOCP_N	Tolerance : 80µs@±20%, others ±30%	10	--	160	µs

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” September cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions September affect device reliability.

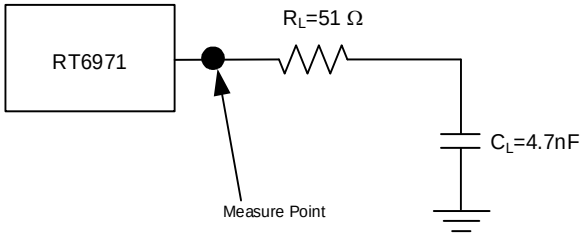
Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. Case temperature is measured on the high effective thermal conductivity four layers thermal test board of JEDEC 51-7 thermal measurement standard. The case temperature point is on the expose pad.

Note 6. Rising/Falling time measure point is before RC.



Note 7. Pulse less than 10ns will be filter.

Note 8. The minimum duty of the converter needs to be considered.

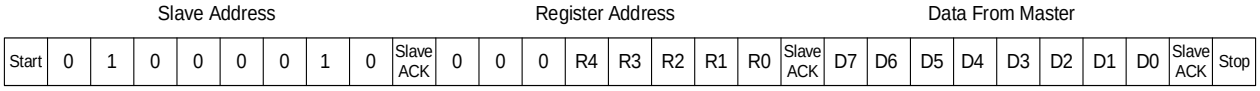
I2C Command

Slave Address

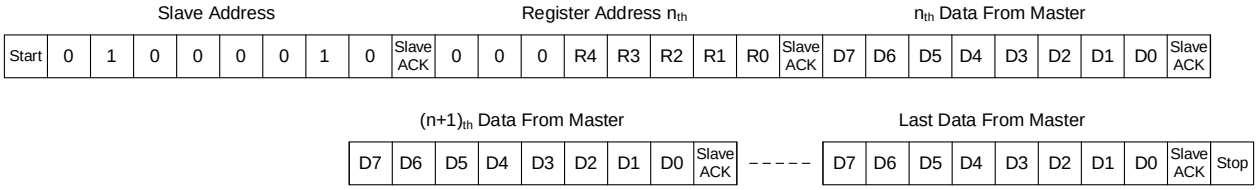
Bit7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 = LSB
0	1	0	0	0	0	1	R/$\overline{W}$

Write Command

(a) Write single byte of data to Register



(b) Write multiple bytes of data to Registers

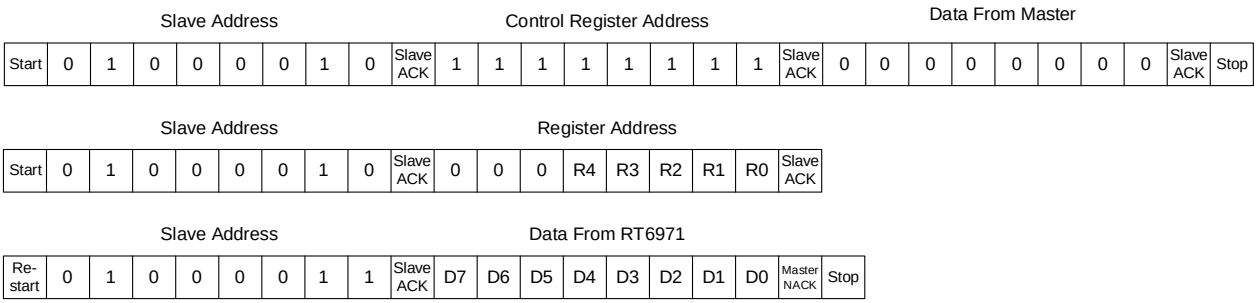


(c) Write All Registers into EEPROM

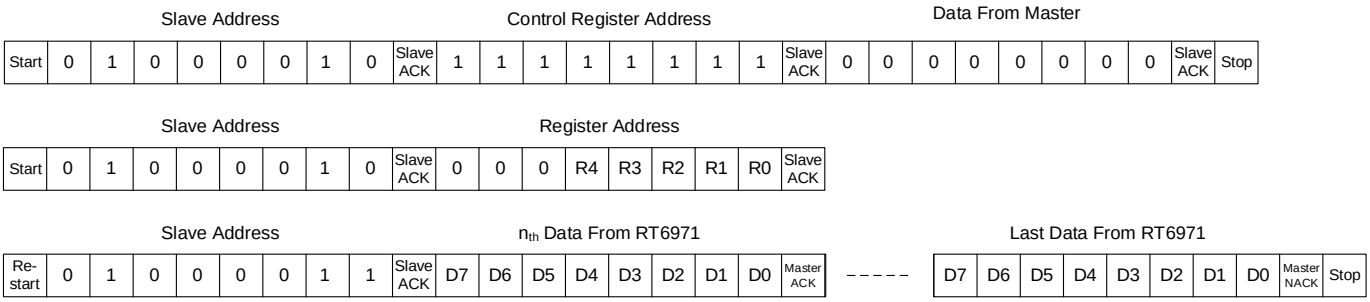
(d) Write VCOM data Registers into EEPROM

Read Command

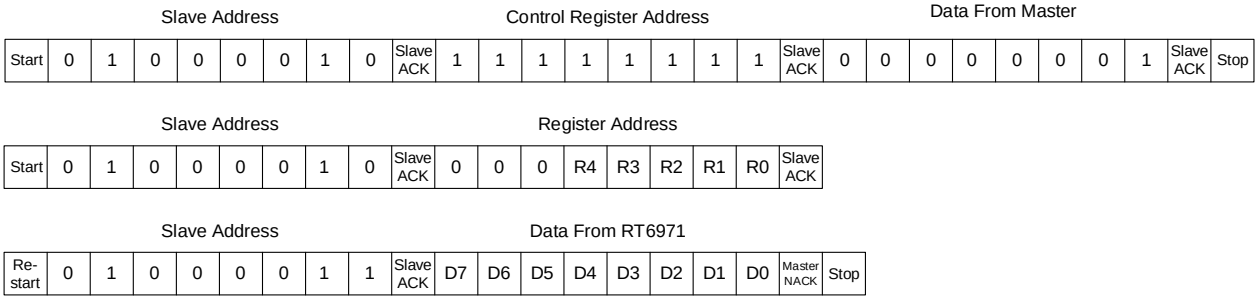
(a) Read single byte of data from Register



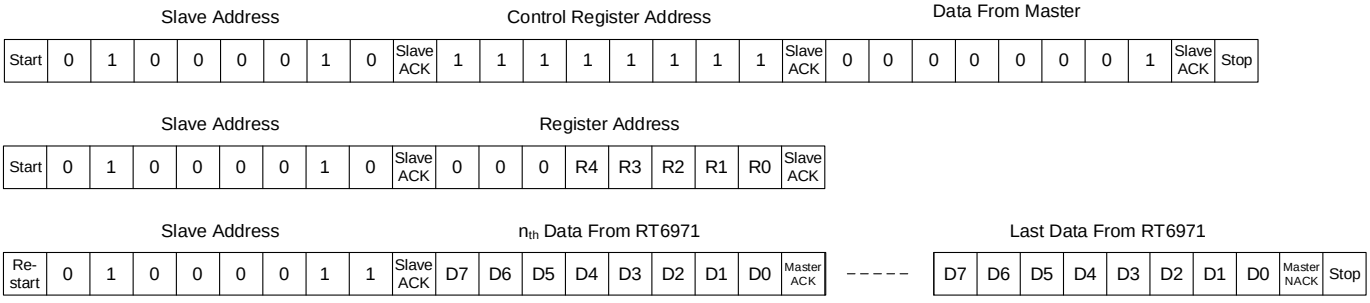
(b) Read multiple bytes of data from Registers



(c) Read data from EEPROM



(d) Read multiple bytes of data from EEPROM



Register Map

Block	ADDR	DEC	HEX	DEC	7	6	5	4	3	2	1	0
AVDD	**0x00**	**0**	0x17h		AVDD<5:0>							
VCC1	**0x01**	**1**	0x32h		VCC1_SS	VCC1<6:0>						
VCC2	**0x02**	**2**	0x19h		VCC2_SS		VCC2<4:0>					
VGH	**0x03**	**3**	0x2Dh			VGH_LT<6:0>						
VGH	**0x04**	**4**	0x28h			VGH_HT<6:0>						
VGL1	**0x05**	**5**	0x10h			VGL1<6:0>						
VGL2	**0x06**	**6**	0x35h			VGL2_LT<6:0>						
VGL2	**0x07**	**7**	0x1Ch			VGL2_HT<6:0>						
DLY	**0x08**	**8**	0x15h		DLY0<1:0>		DLY1<1:0>		DLY2<1:0>		DLY3<1:0>	
OP	**0x09**	**9**	0x52		GLDO<4:0>						HAVDD<9:8>	
OP	**0x0A**	**10**	0x21		HAVDD<7:0>							
OP	**0x0B**	**11**	0x03								GMA1<9:8>	
OP	**0x0C**	**12**	0x99		GMA1<7:0>							
OP	**0x0D**	**13**	0x03								GMA2<9:8>	
OP	**0x0E**	**14**	0x88		GMA2<7:0>							
OP	**0x0F**	**15**	0x03								GMA3<9:8>	
OP	**0x10**	**16**	0x0D		GMA3<7:0>							
OP	**0x11**	**17**	0x02								GMA4<9:8>	
OP	**0x12**	**18**	0xCA		GMA4<7:0>							
OP	**0x13**	**19**	0x02								GMA5<9:8>	
OP	**0x14**	**20**	0xA1		GMA5<7:0>							
OP	**0x15**	**21**	0x02								GMA6<9:8>	
OP	**0x16**	**22**	0x30		GMA6<7:0>							
OP	**0x17**	**23**	0x02								GMA7<9:8>	
OP	**0x18**	**24**	0x17		GMA7<7:0>							
OP	**0x19**	**25**	0x01								GMA8<9:8>	
OP	**0x1A**	**26**	0xC3		GMA8<7:0>							
OP	**0x1B**	**27**	0x01								GMA9<9:8>	
OP	**0x1C**	**28**	0xAA		GMA9<7:0>							
TCOM	**0x1D**	**29**	0x00h		VGH_ TC_EN	VCOM_ TC_EN	VGH_TC_ Type					
MISC	**0x1E**	**30**	0x07h		VGH_TCOM_MODE <1:0>		VGX_ PRT_ OFF		VCOM_TC<3:0>			
LS	**0x1F**	**31**	0xFFh		EOCP_TIME<3:0>				GOCP_TIME<3:0>			
LS	**0x20**	**32**	0x7Fh			EOCP_LEVEL<2:0>			GOCP_LEVEL<3:0>			
LS	**0x21**	**33**	0xFFh		SOCP_TIME<3:0>				SOCP_LEVEL<3:0>			
LS	**0x22**	**34**	0x20h				SCLK_ PSK_RST					

Block	ADDR	DEC	HEX	DEC	7	6	5	4	3	2	1	0
LS	**0x23**	**35**	0x00h				Dummy CLK	EN_120Hz	REVERSE	DOUBLE		
MISC	**0x24**	**36**	0x00h		AVDD_ DIS	HAVDD_ DIS	VGH_DIS	VGL1_DIS	VCC1_DIS	VCOM3_ DIS	VCOM2_ DIS	VCOM1_DIS
MISC	**0x25**	**37**	0x00h				VCC2_DIS	VGL2_DIS		AVDD_EXT_DRV <1:0>		VGH_EXT_ INT
MISC	**0x26**	**38**	0x00h		VCOM1_ EN	VCOM2_EN	VCOM3_ EN					
OP	**0x27**	**39**	0x10h			VCC1 Syn./Asyn.	VCC2 Syn./Asyn.	VCC2_EN	FRE_ VCC1/2	FT_VCC2		
OP	**0x28**	**40**	0x01h								GMA10<9:8>	
MISC	**0x29**	**41**	0xC0h		Protection _EN	VCC_EN	VGL1_EN	VGL2_EN	AVDD_EN	VGH_EN	HAVDD_ EN	GMA_EN
MISC	**0x2A**	**42**	0x01h		VGH_SS	AVDD_SS		FRE_ AVDD	FRE_ HAVDD	FRE_ VGH	FRE_ VGL2	PMIC_EN
MISC	**0x2B**	**43**	0xA3h		DISCH1/2_OCP_Level					DISCH1/2_OCP_Time		
MISC	**0x2C**	**44**	0x00h				AVDD Protection	VCC1 Protection	HAVDD Protection	VGH Protection	VGL2 Protection	VGL1 Protection
OP	**0x2D**	**45**	0x00h		L/S 7 Protection	L/S 6 Protection	L/S 5 Protection	OTP Protection	L/S 4 Protection	L/S 3 Protection	L/S 2 Protection	L/S 1 Protection
MISC	**0x2E**	**46**	0x0Bh		Read Only (Chip ID : 0x0B)							
OP	**0x2F**	**47**	0x2Fh		GMA10<7:0>							
OP	**0x30**	**48**	0x41h								GMA11<9:8>	
OP	**0x31**	**49**	0x04h		GMA11<7:0>							
OP	**0x32**	**50**	0x00h								GMA12<9:8>	
OP	**0x33**	**51**	0xB6h		GMA12<7:0>							
OP	**0x34**	**52**	0x00h								GMA13<9:8>	
OP	**0x35**	**53**	0x23h		GMA13<7:0>							
OP	**0x36**	**54**	0x00h								GMA14<9:8>	
OP	**0x37**	**55**	0x0Ch		GMA14<7:0>							
OP	**0x38**	**56**	0x01h								VCOM1<9:8>	
OP	**0x39**	**57**	0x8Dh		VCOM1<7:0>							
OP	**0x3A**	**58**	0x01h								VCOM2<9:8>	
OP	**0x3B**	**59**	0x8Dh		VCOM2<7:0>							
OP	**0x3C**	**60**	0x01h								VCOM3<9:8>	
OP	**0x3D**	**61**	0x8Dh		VCOM3<7:0>							
LS	**0x40**	**64**	0x00h		LS_EN	HSR<2:0>			CLK Rising Slew Rate		CLK Falling Slew Rate	
LS	**0x41**	**65**	0x00h		STV1_DIS <1:0>		STV2_DIS <1:0>		STV3_DIS <1:0>		DISCH_DIS<1:0>	
LS	**0x42**	**66**	0x06h		CLK_DIS <1:0>		LC_DIS<1:0>		LC_Initial State<2:0>			Auto Pulse
MISC	**0x43**	**67**	0x00h		VCOM_Delay<1:0>			XON On Delay <1:0>		XON Off Delay <1:0>		
LS	**0x44**	**68**	0x00h		ILMT_1		ILMT_A	VIN_UVLO_F			EN_Type	
MISC	**0x45**	**69**	0x58h		VGH1_UV LO_F_ State	STV1_Reset	CH_MODE			Power Off Discharge Threshold <2:0>		

Block	ADDR	DEC	HEX	DEC	7	6	5	4	3	2	1	0
MISC	**0xFF**	**255**	0x00h		CR (Note 8)							

Note 9. CR DATA :

0xFF=80h : Write all DAC register into EEPROM.

0xFF=40h : “Write” only VCOM1/2/3 data to EEPROM.

0xFF=01h : Read data from EEPROM.

0xFF=00h : Read data from DAC register.

The Suggested writing all DAC register into EEPROM time is 300ms

The Suggested writing only VCOM data to EEPROM time is 100ms

Channels Output Table(Unit : V)

Register Code	AVDD	VCC1	VCC2	VGH_ LT	VGH_ HT	VGL1	VGL2_ LT	VGL2_ HT	GLDO
00h	NA	0.80	0.8	21	20	-1.8	-4.5	-4.5	13.0
01h	13.8	0.82	0.9	21.2	20.2	-2.0	-4.7	-4.7	13.2
02h	13.9	0.84	1.0	21.4	20.4	-2.2	-4.9	-4.9	13.4
03h	14.0	0.86	1.1	21.6	20.6	-2.4	-5.1	-5.1	13.6
04h	14.1	0.88	1.2	21.8	20.8	-2.6	-5.3	-5.3	13.8
05h	14.2	0.90	1.3	22	21	-2.8	-5.5	-5.5	14.0
06h	14.3	0.92	1.4	22.2	21.2	-3.0	-5.7	-5.7	14.2
07h	14.4	0.94	1.5	22.4	21.4	-3.2	-5.9	-5.9	14.4
08h	14.5	0.96	1.6	22.6	21.6	-3.4	-6.1	-6.1	14.6
09h	14.6	0.98	1.7	22.8	21.8	-3.6	-6.3	-6.3	14.8
0Ah	14.7	1.00	1.8	23	22	-3.8	-6.5	-6.5	15.0
0Bh	14.8	1.02	1.9	23.2	22.2	-4.0	-6.7	-6.7	15.2
0Ch	14.9	1.04	2.0	23.4	22.4	-4.2	-6.9	-6.9	15.4
0Dh	15.0	1.06	2.1	23.6	22.6	-4.4	-7.1	-7.1	15.6
0Eh	15.1	1.08	2.2	23.8	22.8	-4.6	-7.3	-7.3	15.8
0Fh	15.2	1.10	2.3	24	23	-4.8	-7.5	-7.5	16.0
10h	15.3	1.12	2.4	24.2	23.2	-5.0	-7.7	-7.7	16.2
11h	15.4	1.14	2.5	24.4	23.4	-5.2	-7.9	-7.9	16.4
12h	15.5	1.16	2.6	24.6	23.6	-5.4	-8.1	-8.1	16.6
13h	15.6	1.18	2.7	24.8	23.8	-5.6	-8.3	-8.3	16.8
14h	15.7	1.20	2.8	25	24	-5.8	-8.5	-8.5	17.0
15h	15.8	1.22	2.9	25.2	24.2	-6.0	-8.7	-8.7	17.2
16h	15.9	1.24	3.0	25.4	24.4	-6.2	-8.9	-8.9	17.4
17h	16.0	1.26	3.1	25.6	24.6	-6.4	-9.1	-9.1	17.6
18h	16.1	1.28	3.2	25.8	24.8	-6.6	-9.3	-9.3	17.8
19h	16.2	1.30	3.3	26	25	-6.8	-9.5	-9.5	18.0
1Ah	16.3	1.32	3.4	26.2	25.2	-7.0	-9.7	-9.7	18.0
1Bh	16.4	1.34	3.5	26.4	25.4	-7.2	-9.9	-9.9	18.0
1Ch	16.5	1.36	3.6	26.6	25.6	-7.4	-10.1	-10.1	18.0
1Dh	16.6	1.38	3.7	26.8	25.8	-7.6	-10.3	-10.3	18.0
1Eh	16.7	1.40	3.7	27	26	-7.8	-10.5	-10.5	18.0
1Fh	16.8	1.42	3.7	27.2	26.2	-8.0	-10.7	-10.7	18.0
20h	16.9	1.44		27.4	26.4	-8.2	-10.9	-10.9	
21h	17.0	1.46		27.6	26.6	-8.4	-11.1	-11.1	
22h	17.1	1.48		27.8	26.8	-8.6	-11.3	-11.3	

Register Code	AVDD	VCC1	VCC2	VGH_LT	VGH_HT	VGL1	VGL2_LT	VGL2_HT	GLDO
23h	17.2	1.50		28	27	-8.8	-11.5	-11.5	
24h	17.3	1.52		28.2	27.2	-9.0	-11.7	-11.7	
25h	17.4	1.54		28.4	27.4	-9.2	-11.9	-11.9	
26h	17.5	1.56		28.6	27.6	-9.4	-12.1	-12.1	
27h	17.6	1.58		28.8	27.8	-9.6	-12.3	-12.3	
28h	17.7	1.60		29	28	-9.8	-12.5	-12.5	
29h	17.8	1.62		29.2	28.2	-10.0	-12.7	-12.7	
2Ah	17.9	1.64		29.4	28.4	-10.2	-12.9	-12.9	
2Bh	18.0	1.66		29.6	28.6	-10.4	-13.1	-13.1	
2Ch	18.1	1.68		29.8	28.8	-10.6	-13.3	-13.3	
2Dh	18.2	1.70		30	29	-10.8	-13.5	-13.5	
2Eh	18.3	1.72		30.2	29.2	-11.0	-13.7	-13.7	
2Fh	18.4	1.74		30.4	29.4	-11.2	-13.9	-13.9	
30h	18.5	1.76		30.6	29.6	-11.4	-14.1	-14.1	
31h	18.6	1.78		30.8	29.8	-11.6	-14.3	-14.3	
32h	18.7	1.80		31	30	-11.8	-14.5	-14.5	
33h	18.8	1.82		31.2	30.2	-12.0	-14.7	-14.7	
34h	18.9	1.84		31.4	30.4	-12.2	-14.9	-14.9	
35h	19.0	1.86		31.6	30.6	-12.4	-15.1	-15.1	
36h	19.1	1.88		31.8	30.8	-12.6	-15.3	-15.3	
37h	19.2	1.90		32	31	-12.8	-15.5	-15.5	
38h	19.3	1.92		32.2	31.2	-13.0	-15.7	-15.7	
39h	19.4	1.94		32.4	31.4	-13.2	-15.9	-15.9	
3Ah	19.5	1.96		32.6	31.6	-13.4	-16.1	-16.1	
3Bh	19.6	1.98		32.8	31.8	-13.6	-16.3	-16.3	
3Ch	19.7	2.00		33	32	-13.8	-16.5	-16.5	
3Dh	19.8	2.02		33.2	32.2	-14.0	-16.7	-16.7	
3Eh	19.9	2.04		33.4	32.4	-14.2	-16.9	-16.9	
3Fh	20.0	2.06		33.6	32.6	-14.4	-17.1	-17.1	
40h		2.08		33.8	32.8	-14.6	-17.3	-17.3	
41h		2.10		34	33	-14.8	-17.5	-17.5	
42h		2.12		34.2	33.2	-15.0	-17.7	-17.7	
43h		2.14		34.4	33.4		-17.9	-17.9	
44h		2.16		34.6	33.6		-18.1	-18.1	
45h		2.18		34.8	33.8		-18.3	-18.3	
46h		2.20		35	34		-18.5	-18.5	
47h		2.22		35.2	34.2		-18.7	-18.7	
48h		2.24		35.4	34.4		-18.9	-18.9	

Register Code	AVDD	VCC1	VCC2	VGH_ LT	VGH_ HT	VGL1	VGL2_ LT	VGL2_ HT	GLDO
49h		2.26		35.6	34.6		-19.1	-19.1	
4Ah		2.28		35.8	34.8		-19.3	-19.3	
4Bh		2.30		36	35		-19.5	-19.5	
4Ch		2.32		36.2	35.2		-19.7	-19.7	
4Dh		2.34		36.4	35.4		-19.9	-19.9	
4Eh		2.36		36.6	35.6		-20	-20	
4Fh				36.8	35.8				
50h				37	36				
51h				37.2	36.2				
52h				37.4	36.4				
53h				37.6	36.6				
54h				37.8	36.8				
55h				38	37				
56h				38.2	37.2				
57h				38.4	37.4				
58h				38.6	37.6				
59h				38.8	37.8				
5Ah				39	38				
5Bh				39.2	38.2				
5Ch				39.4	38.4				
5Dh				39.6	38.6				
5Eh				39.8	38.8				
5Fh				40	39				
60h				40.2	39.2				
61h				40.4	39.4				
62h				40.6	39.6				
63h				40.8	39.8				
64h				41	40				
65h				41.2	40.2				
66h				41.4	40.4				
67h				41.6	40.6				
68h				41.8	40.8				
69h				42	41				
6Ah				42.2	41.2				
6Bh				42.4	41.4				
6Ch				42.6	41.6				
6Dh				42.8	41.8				
6Eh				43	42				

Register Code	AVDD	VCC1	VCC2	VGH_ LT	VGH_ HT	VGL1	VGL2_ LT	VGL2_ HT	GLDO
6Fh				43.2	42.2				
70h				43.4	42.4				
71h				43.6	42.6				
72h				43.8	42.8				
73h				44	43				
74h				44.2	43.2				
75h				44.4	43.4				
76h				44.6	43.6				
77h				44.8	43.8				
78h				45	44				

GAMMA Output Table, RES = GLDO / 1024 (unit: V)

Register Code	Gamma 1~14
0000h	RES
0001h	RES+RES*1
0002h	RES+RES*2
0003h	RES+RES*3
0004h	RES+RES*4
0005h	RES+RES*5
0006h	RES+RES*6
0007h	RES+RES*7
0008h	RES+RES*8
0009h	RES+RES*9
000Ah	RES+RES*10
000Bh	RES+RES*11
000Ch	RES+RES*12
000Dh	RES+RES*13
000Eh	RES+RES*14
000Fh	RES+RES*15
.....	
0037h	RES+RES*55
0038h	RES+RES*56
0039h	RES+RES*57
003Ah	RES+RES*58
003Bh	RES+RES*59
003Ch	RES+RES*60
003Dh	RES+RES*61
003Eh	RES+RES*62
003Fh	RES+RES*63
0040h	RES+RES*64
0041h	RES+RES*65
0042h	RES+RES*66
.....	
0109h	RES+RES*265
010Ah	RES+RES*266
010Bh	RES+RES*267
010Ch	RES+RES*268
010Dh	RES+RES*269
010Eh	RES+RES*270
010Fh	RES+RES*271
0110h	RES+RES*272
0111h	RES+RES*273
0112h	RES+RES*274
0113h	RES+RES*275
0114h	RES+RES*276
.....	
0180h	RES+RES*384
0181h	RES+RES*385
0182h	RES+RES*386
0183h	RES+RES*387
0184h	RES+RES*388
0185h	RES+RES*389
0186h	RES+RES*390
0187h	RES+RES*391
0188h	RES+RES*392
0189h	RES+RES*393
018Ah	RES+RES*394
018Bh	RES+RES*395
.....	
01F1h	RES+RES*497
01F2h	RES+RES*498
01F3h	RES+RES*499
01F4h	RES+RES*500
01F5h	RES+RES*501
01F6h	RES+RES*502
01F7h	RES+RES*503
01F8h	RES+RES*504
01F9h	RES+RES*505
01FAh	RES+RES*506
01FBh	RES+RES*507
01FCh	RES+RES*508
01FDh	RES+RES*509
01FEh	RES+RES*510
01FFh	RES+RES*511
.....	
0258h	RES+RES*600
0259h	RES+RES*601
025Ah	RES+RES*602
025Bh	RES+RES*603
025Ch	RES+RES*604
025Dh	RES+RES*605
025Eh	RES+RES*606
025Fh	RES+RES*607
0260h	RES+RES*608
0261h	RES+RES*609
0262h	RES+RES*610
0263h	RES+RES*611
0264h	RES+RES*612
0265h	RES+RES*613
0266h	RES+RES*614
.....	
03F1h	RES+RES*1009
03F2h	RES+RES*1010
03F3h	RES+RES*1011
03F4h	RES+RES*1012
03F5h	RES+RES*1013
03F6h	RES+RES*1014
03F7h	RES+RES*1015
03F8h	RES+RES*1016
03F9h	RES+RES*1017
03FAh	RES+RES*1018
03FBh	RES+RES*1019
03FCh	RES+RES*1020
03FDh	RES+RES*1021
03FEh	RES+RES*1022
03FFh	RES+RES*1023

VCOM, HAVDD Output Table, RES = GLDO/ 1024 (unit: V)

Register Code	HAVDD/VCOM1/2
0000h	RES
0001h	RES+RES*1
0002h	RES+RES*2
0003h	RES+RES*3
0004h	RES+RES*4
0005h	RES+RES*5
0006h	RES+RES*6
0007h	RES+RES*7
0008h	RES+RES*8
0009h	RES+RES*9
000Ah	RES+RES*10
000Bh	RES+RES*11
000Ch	RES+RES*12
000Dh	RES+RES*13
000Eh	RES+RES*14
000Fh	RES+RES*15
……	
0037h	RES+RES*55
0038h	RES+RES*56
0039h	RES+RES*57
003Ah	RES+RES*58
003Bh	RES+RES*59
003Ch	RES+RES*60
003Dh	RES+RES*61
003Eh	RES+RES*62
003Fh	RES+RES*63
0040h	RES+RES*64
0041h	RES+RES*65
0042h	RES+RES*66
……	
0109h	RES+RES*265
010Ah	RES+RES*266
010Bh	RES+RES*267
010Ch	RES+RES*268
010Dh	RES+RES*269
010Eh	RES+RES*270
010Fh	RES+RES*271
0110h	RES+RES*272
0111h	RES+RES*273
0112h	RES+RES*274
0113h	RES+RES*275
0114h	RES+RES*276
……	
0180h	RES+RES*384
0181h	RES+RES*385
0182h	RES+RES*386
0183h	RES+RES*387
0184h	RES+RES*388
0185h	RES+RES*389
0186h	RES+RES*390
0187h	RES+RES*391
0188h	RES+RES*392
0189h	RES+RES*393
018Ah	RES+RES*394
018Bh	RES+RES*395
……	
01F1h	RES+RES*497
01F2h	RES+RES*498
01F3h	RES+RES*499
01F4h	RES+RES*500
01F5h	RES+RES*501
01F6h	RES+RES*502
01F7h	RES+RES*503
01F8h	RES+RES*504
01F9h	RES+RES*505
01FAh	RES+RES*506
01FBh	RES+RES*507
01FCh	RES+RES*508
01FDh	RES+RES*509
01FEh	RES+RES*510
01FFh	RES+RES*511
……	
0258h	RES+RES*600
0259h	RES+RES*601
025Ah	RES+RES*602
025Bh	RES+RES*603
025Ch	RES+RES*604
025Dh	RES+RES*605
025Eh	RES+RES*606
025Fh	RES+RES*607
0260h	RES+RES*608
0261h	RES+RES*609
0262h	RES+RES*610
0263h	RES+RES*611
0264h	RES+RES*612
0265h	RES+RES*613
0266h	RES+RES*614
……	
03F1h	RES+RES*1009
03F2h	RES+RES*1010
03F3h	RES+RES*1011
03F4h	RES+RES*1012
03F5h	RES+RES*1013
03F6h	RES+RES*1014
03F7h	RES+RES*1015
03F8h	RES+RES*1016
03F9h	RES+RES*1017
03FAh	RES+RES*1018
03FBh	RES+RES*1019
03FCh	RES+RES*1020
03FDh	RES+RES*1021
03FEh	RES+RES*1022
03FFh	RES+RES*1023

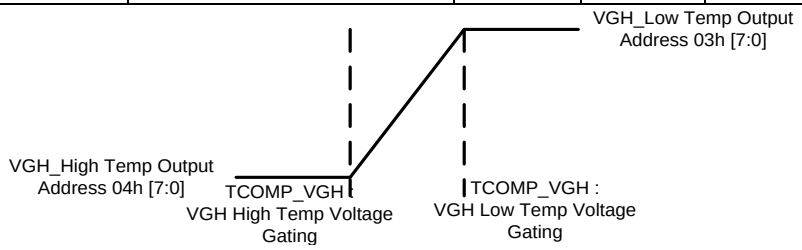
Register Detail Description

Address : 0x01h/0x02h

Step[0]	VCC1/2 SS
0	1ms
1	3ms

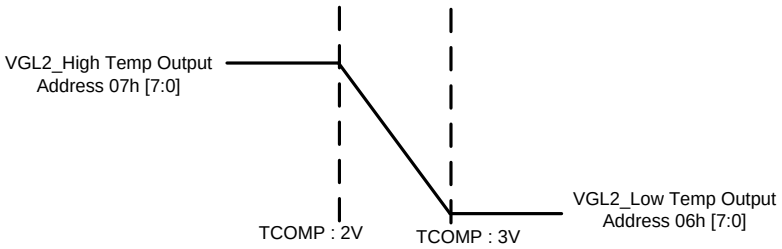
Address : 0x03h/0x04h

Name	Function	Address	Bits	Factor (Power-Up Default)	MSB						LSB
VGH_LT	VGH Boost (Low Temp)	0x03h	7bit	2Dh	X	0	1	0	1	1	0	1
VGH_HT	VGH Boost (Room Temp)	0x04h	7bit	28h	X	0	1	0	1	0	0	0



Address : 0x06h/0x07h

Name	Function	Address	Bits	Factor (Power-Up Default)	MSB						LSB
VGL2_LT	VGL2 (Low Temp)	0x06h	7bit	35h	X	0	1	1	0	1	0	1
VGL2_HT	VGL2 (High Temp)	0x07h	7bit	1Ch	X	0	0	1	1	1	0	0



Address : 0x08h

Name	Function	Address	Bits	Factor (Power-Up Default)	MSB							LSB
DLY0	Delay 0	0x08h	2bit	15h	0	0	X	X	X	X	X	X
DLY1	Delay 1		2bit		X	X	0	1	X	X	X	X
DLY2	Delay 2		2bit		X	X	X	X	0	1	X	X
DLY3	Delay 3		2bit		X	X	X	X	X	X	0	1

	Start to Finish
DLY0	VIN_UVLO & EN to VCC1
DLY1	VIN_UVLO & EN to VCC2
DLY2	VCC1/2 to VGL2
DLY3	VGL2 to AVDD

	DLY0	DLY1	DLY2	DLY3
00	3ms	3ms	0ms	0ms
01	8ms	8ms	5ms	10ms
10	16ms	16ms	10ms	20ms
11	0ms	0ms	15ms	30ms

Address : 0x1Dh

	VGH_TC_EN/VCOM_TC_EN
0	Disable
1	Enable

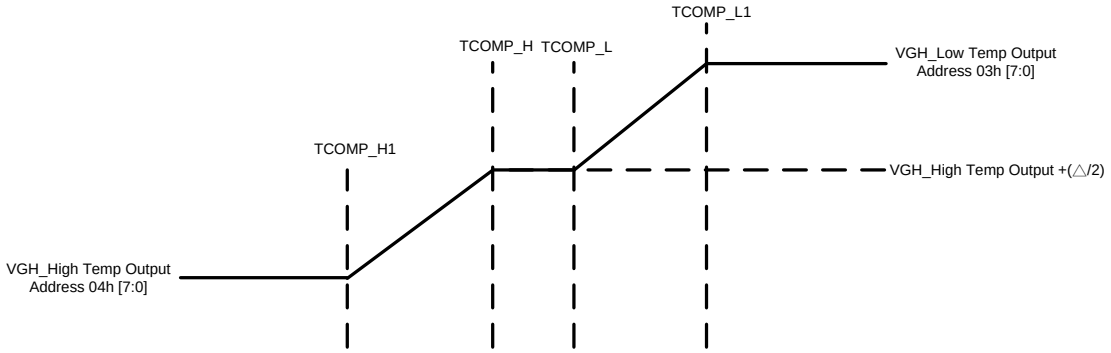
	VGH_TC_Type
0	Two stage
1	Three stage

Address : 0x1Eh

Name	Function	Address	Bits	Factor (Power-Up Default)	MSB							LSB
VGH_TC_MODE	VGH Temp. Compensation Range Selection	0x1Eh	2bit	07h	0	0	X	X	X	X	X	X
VGx_PRT_OFF	VGH/VGL Protection Enable		1bit		X	X	0	X	X	X	X	X
VCOM_TC	VCOM Compensation		4bit		X	X	X	X	0	1	1	1

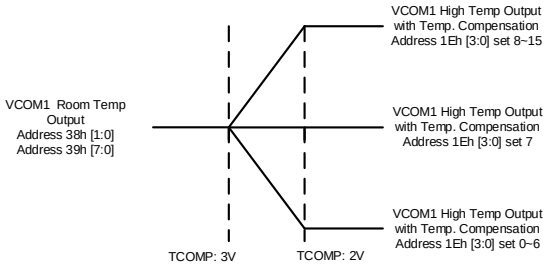
Step[7:6] VGH_TC_MODE and VGH_TC_Type=0				
Item	**00h**	**01h**	**02h**	**03h**
TCOMP_L	2.94 V	3.35 V	2.94 V	2.94 V
TCOMP_H	2.09 V	2.95 V	2.44 V	2.64 V
Temp	0℃~25℃	-20℃~0℃	0℃~15℃	0℃~10℃
Panel	LGD/HKC	INX	SDP	SDP

Step[7:6] VGH_TC_MODE and VGH_TC_Type=1				
Item	**00h**	**01h**	**02h**	**03h**
TCOMP_L1	3.79 V	3.75 V	3.44 V	3.24 V
TCOMP_L	2.94 V	3.35 V	2.94 V	2.94 V
TCOMP_H	2.09 V	2.95 V	2.44 V	2.64 V
TCOMP_H1	1.24 V	2.55 V	1.94 V	2.34 V
Temp	0℃~25℃	-20℃~0℃	0℃~15℃	0℃~10℃
Panel	LGD/HKC	INX	SDP	SDP



Step[5]	VGx_PRT_Enable
0	VGH, VGL1, VGL2 Protection Enable
1	VGH, VGL1, VGL2 Protection Disable

Step[3:0]	VCOM Compensation
0000	VCOM-GLDO/1024*14
0001	VCOM-GLDO1024*12
0010	VCOM-GLDO/1024*10
0011	VCOM-GLDO/1024*8
0100	VCOM- GLDO /1024*6
0101	VCOM- GLDO /1024*4
0110	VCOM- GLDO /1024*2
0111	VCOM
1000	VCOM+ GLDO /1024*2
1001	VCOM+ GLDO /1024*4
1010	VCOM+ GLDO /1024*6
1011	VCOM+ GLDO /1024*8
1100	VCOM+ GLDO /1024*10
1101	VCOM+ GLDO /1024*12
1110	VCOM+ GLDO /1024*14
1111	VCOM+ GLDO /1024*16



LS_EG_OCP_TIME Register								
0x1Fh	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
Register	**EOCP_TIME**				**GOCP_TIME**			
Initial(HEX)	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Description

GOCP_TIME 0x1F[3:0]	us CLKOUT1 ~ CLKOUT12
0000	1
0001	1.5
0010	2
0011	2.5
0100	3
0101	3.5
0110	4
0111	4.5
1000	5
1001	5.5
1010	6
1011	6.5
1100	7
1101	7.5
1110	8
1111	8.5

EOCP_TIME 0x1F[7:4]	us LCOUT1/LCOUT2
0000	10
0001	20
0010	30
0011	40
0100	50
0101	60
0110	70
0111	80
1000	90
1001	100
1010	110
1011	120
1100	130
1101	140
1110	150
1111	160

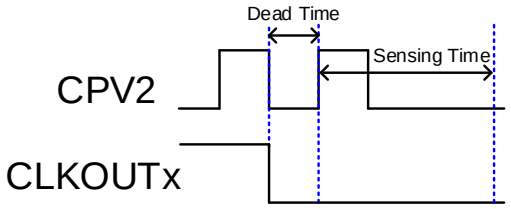
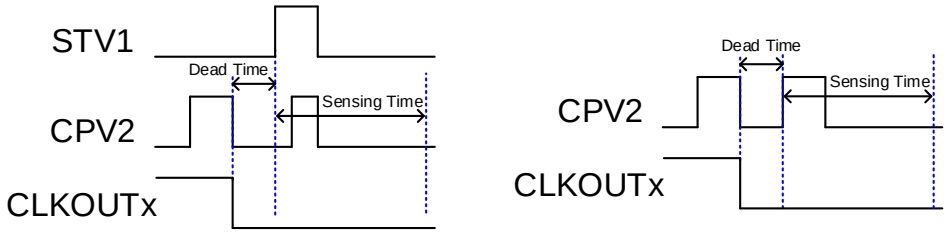
LS_EG_OCP_LEVEL Register								
0x20h	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
Register	**Reserved**	**EOCP_LEVEL**			**GOCP_LEVEL**			
Initial(HEX)	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Description

GOCP_LEVEL 0x20[3:0]	mA CLKOUT1 ~ CLKOUT12
0000	20
0001	30
0010	40
0011	50
0100	60
0101	70
0110	80
0111	90
1000	100
1001	110
1010	120
1011	130
1100	140
1101	150
1110	160
1111	270

EOCP_LEVEL 0x20[6:4]	mA LCOUT1/LCOUT2
000	10
001	20
010	30
011	40
100	50
101	60
110	70
111	135

<table>
<tr><th colspan="9">LS_STV_OCP_TIME_LEVEL Register</th></tr>
<tr><th>0x21h</th><th>Bit7</th><th>Bit6</th><th>Bit5</th><th>Bit4</th><th>Bit3</th><th>Bit2</th><th>Bit1</th><th>Bit0</th></tr>
<tr><td>Register</td><td colspan="4">SOCP_TIME</td><td colspan="4">SOCP_LEVEL</td></tr>
<tr><td>Initial(HEX)</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>Description</td><td colspan="8">
<table>
<tr><td>SOCP_LEVEL
0x21[3:0]</td><td>mA
STVOUT1/2/3</td></tr>
<tr><td>0000</td><td>20</td></tr>
<tr><td>0001</td><td>30</td></tr>
<tr><td>0010</td><td>40</td></tr>
<tr><td>0011</td><td>50</td></tr>
<tr><td>0100</td><td>60</td></tr>
<tr><td>0101</td><td>70</td></tr>
<tr><td>0110</td><td>80</td></tr>
<tr><td>0111</td><td>90</td></tr>
<tr><td>1000</td><td>100</td></tr>
<tr><td>1001</td><td>110</td></tr>
<tr><td>1010</td><td>120</td></tr>
<tr><td>1011</td><td>130</td></tr>
<tr><td>1100 to 1111</td><td>135</td></tr>
</table>
<table>
<tr><td>SOCP_TIME
0x21[7:4]</td><td>us
STVOUT1/2/3</td></tr>
<tr><td>0000</td><td>1</td></tr>
<tr><td>0001</td><td>1.5</td></tr>
<tr><td>0010</td><td>2</td></tr>
<tr><td>0011</td><td>2.5</td></tr>
<tr><td>0100</td><td>3</td></tr>
<tr><td>0101</td><td>3.5</td></tr>
<tr><td>0110</td><td>4</td></tr>
<tr><td>0111</td><td>4.5</td></tr>
<tr><td>1000</td><td>5</td></tr>
<tr><td>1001</td><td>5.5</td></tr>
<tr><td>1010</td><td>6</td></tr>
<tr><td>1011</td><td>6.5</td></tr>
<tr><td>1100</td><td>7</td></tr>
<tr><td>1101</td><td>7.5</td></tr>
<tr><td>1110</td><td>8</td></tr>
<tr><td>1111</td><td>8.5</td></tr>
</table>
</td></tr>
</table>

Timing setting of LS								
0x22h	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
Register			**SCLK_PSK_RST**					
Initial(HEX)			**1**					
Description	**SCLK_PSK_RST:** 0x22[5] = 0 : Duration between falling edge of OFF_CLK to rising edge of OFF_CLK as dead time during low side OCP detecting(INX, HKC,SDP)  0x22[5] = 1 : Duration between falling edge of OFF_CLK to rising edge of OFF_CLK or rising edge of SCLK as dead time during low side OCP detecting(LGD, BOE)  								

Timing setting of LS								
0x23h	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
Register			DUM_CLK	EN_120Hz	REVERSE	DOUBLE		
Initial(HEX)			0	0	0	0		

Description

Single 0x23[2]=0				
	0x23[3] =0, 0x23[5]=0	0x23[3] =0, 0x23[5]=1	0x23[3] =1, 0x23[5]=0	0x23[3] =1, 0x23[5]=1
4-CH CLKOUT	CLK1-2-3-4-1	CLK3-4-1-2-3	CLK4-3-2-1-4	CLK2-1-4-3-2
6-CH CLKOUT	CLK1-2-3-4-5-6-1	CLK4-5-6-1-2-3-4	CLK6-5-4-3-2-1-6	CLK3-2-1-6-5-4
8-CH CLKOUT	CLK1-2-3-4-5-6-7-8-1	CLK4-5-6-7-8-1-2-3-4	CLK8-7-6-5-4-3-2-1-8	CLK4-3-2-1-8-7-6-5-4
10-CH CLKOUT	CLK1-2-3-4-5-6-7-8-9-10-1	CLK6-7-8-9-10-1-2-3-4-5-6	CLK10-9-8-7-6-5-4-3-2-1-10	CLK5-4-3-2-1-10-9-8-7-6-5
12-CH CLKOUT	CLK1-2-3-4-5-6-7-8-9-10-11-12-1	CLK6-7-8-9-10-11-12-1-2-3-4-5	CLK12-11-10-9-8-7-6-5-4-3-2-1-12	CLK6-5-4-3-2-1-12-11-10-9-8-7-6
Double 0x23[2]=1				
	0x23[3] =0, 0x23[5]=0	0x23[3] =0, 0x23[5]=1	0x23[3] =1, 0x23[5]=0	0x23[3] =1, 0x23[5]=1
4-CH CLKOUT	CLK1/2-3/4/-1/2	CLK3/4/-1/2-3/4	CLK4/3-2/1-4/3	CLK2/1-4/3-2/1
6-CH CLKOUT	CLK1/2-3/4/-5/6-1/2	CLK3/4-5/6-1/2-3/4	CLK6/5-4/3-2/1-6/5	CLK4/3-2/1-6/5
8-CH CLKOUT	CLK1/2-3/4/-5/6-7/8-1/2	CLK5/6-7/8-1/2-3/4	CLK8/7-6/5-4/3-2/1-8/7	CLK4/3-2/1-8/7-6/5-4/3
10-CH CLKOUT	CLK1/2-3/4/-5/6-7/8-9/10-1/2	CLK5/6-7/8-9/10-1/2-3/4-5/6	CLK10/9-8/7-6/5-4/3-2/1-10/9	CLK4/3-2/1-10/9-8/7-6/5-4/3
12-CH CLKOUT	CLK1/2-3/4/-5/6-7/8-9/10-11/12-1/2	CLK5/6-7/8-9/10-11/12-1/2-3/4-5/6	CLK12/11-10/9-8/7-6/5-4/3-2/1-12/11	CLK6/5-4/3-2/1-12/11-10/9-8/7-6/5
EN_120Hz 0x23[4]=1				
	0x23[3] =0, 0x23[5]=0	0x23[3] =0, 0x23[5]=1	0x23[3] =1, 0x23[5]=0	0x23[3] =1, 0x23[5]=1
4-CH CLKOUT	CLK1/3-2/4-1/3	CLK2/4-1/3-2/4	CLK4/2-3/1-4/2	CLK3/1-4/2-3/1
8-CH CLKOUT	CLK1/3-2/4-5/7-6/8-1/3	CLK5/7-6/8-1/3-2/4-5/7	CLK8/6-7/5-4/2-3/1-8/6	CLK4/2-3/1-8/6-7/5
12-CH CLKOUT	CLK1/3-2/4-5/7-6/8-9/11-10/12-1/3	CLK5/7-6/8-9/11-10/12-1/3-2/4-5/7	CLK12/10-11/9-8/6-7/5-4/2-3/1-12/10	CLK6/5-4/3-2/1-12/11-10/9-8/7-6/5

0x24h	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
Register	AVDD_DIS	HAVDD_DIS	VGH_DIS	VGL1_DIS	VCC1_DIS	VCOM3_DIS	VCOM2_DIS	VCOM1_DIS
Initial(HEX)	0	0	0	0	0	0	0	0

Description

	Discharging
0	Discharge Operation Disable
1	Discharge Operation Enable

	Discharging Resistor
AVDD	800 Ω
HAVDD	500 Ω
VCC	300 Ω
VGH	1500 Ω
VGL1	200 Ω
VCOM1/2/3	1k Ω

0x25h	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Register			VCC2_DIS	VGL2_DIS		AVDD_EXT_DRV		VGH_EXT_INT
Initial(HEX)			0	0		00		0

Description

	VGH_EXT_INT
0	Internal
1	External

	AVDD_EXT_DRV
00	EXT_DRV1_FF : 2ohm
01	EXT_DRV2_F : 10ohm
10	EXT_DRV3_S : 50ohm
11	EXT_DRV4_SS : 200ohm

	Discharging
0	Discharge Operation Disable
1	Discharge Operation Enable

	Discharging Resistor
VCC2	300 Ω
VGL2	200 Ω

0x26h	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Register	VCOM1_EN	VCOM2_EN	VCOM3_EN					

Initial(HEX)	0	0	0	

Description

	VCOM1/2/3_EN
0	Disable
1	Enable

0x27h	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Register		VCC1 Syn./Asyn.	VCC2 Syn./Asyn	VCC2_ EN	FRE_ VCC 1/2	FT_VCC2		
Initial(HEX)		0	0	1	0	0		

Description

0x27[2]:
FT_VCC2 : the UVP, SCP flag of VCC2

	FRE_VCC1/2
0	750kHz
1	500kHz

	VCC2_EN
0	Disable
1	Enable

	VCC1/2 Sync./Async.
0	Sync.
1	Async.

Address : 0x29h

	Enable
0	Disable
1	Enable

	CH_Enable
0	Disable
1	Enable

	Protection_EN
0	Disable all protection
1	Enable all protection

0x2Ah	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Register	VGH_SS	AVDD_SS		FRE_ AVDD	FRE_ HAVDD	FRE_ VGH	FRE_ VGL2	PMIC_EN
Initial(HEX)	0	0	0	0	0	0	0	1

Description

	PMIC_EN
0	Disable
1	Enable

	FRE_VGL2
0	750kHz
1	500kHz

	FRE_VGH
0	AVDD x 1
1	AVDD x 2

	FRE_HAVDD
0	AVDD x 1
1	AVDD x 2

	FRE_AVDD
0	750kHz
1	500kHz

	AVDD_SS
00	5ms
01	10ms
10	15ms
11	20ms

	VGH_SS
0	3ms
1	6ms

0x2Bh	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Register	DISCH1/2_OCP_Level					DISCH1/2_OCP_Time		
Initial(HEX)	101					011		

Description

DSICH1/2_OCP_Time 0x2B[2:0]	us
	DISCH1/2
000	10
001	20
010	30
011	50
100	80
101	100
110	120
111	160

DISCH1/2_OCP_Time 0x2B[7:5]	mA
	DISCH1/2
000	40
001	50
010	60
011	70
100	80
101	120
110	135
111	Disable

0x2Ch	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Register			FT_AVDD	FT_ VCC1	FT_ HAVDD	FT_VGH	FT_VGL2	FT _VGL1
Initial(HEX) (Read Only)			0	0	0	0	0	0
Description	0x2C[0]: FT_VGL1: the UVP, SCP flag of VGL1 0x2C[1]: FT_VGL2: the UVP, SCP flag of VGL2 0x2C[2]: FT_VGH: the UVP, SCP flag of VGH 0x2C[3]: FT_HAVDD: the UVP, SCP flag of HAVDD 0x2C[4]: FT_VCC: the UVP, SCP flag of VCC1 0x2C[5]: FT_AVDD: the UVP, SCP flag of AVDD							

0x2Dh	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Register	FT _L/S 7	FT _L/S 6	FT _L/S 5	FT_OTP	FT _ L/S 4	FT _ L/S 3	FT _ L/S 2	FT _ L/S 1
Initial(HEX) (Read Only)	0	0	0	0	0	0	0	0

<table>
<tr><td>Description</td><td>0x2D[0:3]:
FT_L/S 1 ~ 3: the OCP flag of CLKOUT1 ~ CLKOUT12
<table>
<tr><td>0001</td><td>CLKOUT1</td></tr>
<tr><td>0010</td><td>CLKOUT2</td></tr>
<tr><td>0011</td><td>CLKOUT3</td></tr>
<tr><td>0100</td><td>CLKOUT4</td></tr>
<tr><td>0101</td><td>CLKOUT5</td></tr>
<tr><td>0110</td><td>CLKOUT6</td></tr>
<tr><td>0111</td><td>CLKOUT7</td></tr>
<tr><td>1000</td><td>CLKOUT8</td></tr>
<tr><td>1001</td><td>CLKOUT9</td></tr>
<tr><td>1010</td><td>CLKOUT10</td></tr>
<tr><td>1011</td><td>CLKOUT11</td></tr>
<tr><td>1100</td><td>CLKOUT12</td></tr>
<tr><td>1101 ~ 1111</td><td>NC</td></tr>
</table>
0x2D[4]:
FT_OTP: the OTP flag
0x2D[5]:
FT_L/S 5: the OCP flag of DISCH1, DISCH2
0x2D[6]:
FT_L/S 6: the OCP flag of LCOUT1, LCOUT2
0x2D[7]:
FT_L/S 7: the OCP flag of STVOUT1, STVOUT2, STVOUT3</td></tr>
</table>

0x40h	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Register	LS_EN	HSR			CLK Rising Slew Rate		CLK Falling Slew Rate	
Initial(HEX)	0	000			00		00	

Description

	LS_EN
0	All L/S outputs Hi-Z
1	All L/S outputs normally operate

	HSR
000	Normal Mode – LC 1-In, 2-Out
001	Normal Mode – LC 2-In, 2-Out
010	HSR 120Hz If is used 6,10, follow Normal Mode
011 to 111	Only enable at forward, wo Dummy, single. Otherwise = 000

	CLK1 to 12 Rising Slew Rate
00	1000V/us
01	700V/us
10	400V/us
11	100V/us

	CLK1 to 12 Falling Slew Rate
00	1000V/us
01	700V/us
10	400V/us
11	100V/us

0x41h	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Register	STV1_DIS		STV2_DIS		STV3_DIS		DISCH1/2_DIS	
Initial(HEX)	00		00		00		00	

Description

	STVOUT1,2,3/DISCH1,2_DIS
00	Pull to VGH
01	Pull to VGL2
10	Hi-Z
11	Hi-Z

0x42h	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Register	CLK_DIS		LC_DIS		LC_Initial State			Auto Pulse
Initial(HEX)	00		00		011			0

Description

	Auto Pulse
0	Disable
1	Enable

	LC_Initial State
000	Follow VGH until LC_IN rising edge
001	Follow VGH until VGH_UVLO_R
010	Follow VGL2 until LC_IN rising edge
011	Follow VGL2 until VGH_UVLO_R
100	LC1 follow VGL2 and LC2 follow VGH until LC_IN rising edge
101	LC1 follow VGH and LC2 follow VGL2 until LC_IN rising edge
110, 111	LC1 follow VGH and LC2 follow VGL2 until VGH_UVLO_R

	CLK/LC_DIS
00	Pull to VGH
01	Pull to VGL2
10	Hi-Z
11	Hi-Z

0x43h	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Register	VCOM_Delay			XON On Delay		XON Off Delay		
Initial(HEX)	000			00		00		

Description

	XON Off Delay
00	0ms
01	5ms
10	10ms
11	20ms

	XON On Delay
00	0ms
01	5ms
10	10ms
11	20ms

	VCOM_Delay
000	0ms
001	30ms
010	60ms
011	90ms
100	120ms
101	150ms
110	180ms
111	210ms

0x44h	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Register	ILMT_1		ILM_A	VIN_UVLO_F			EN_Type	
Initial(HEX)	0		0	00			00	

Description

	EN_Type
00	EN control AVDD, HAVDD, VGH, VCOM, GMA
01	EN control all channels
10	EN don’t control any channels
11	EN don’t control any channels

	VIN_UVLO_F
00	6.5V
01	7.0V
10	7.5V
11	8.0V

	ILMT_A
0	5A (0.25V)
1	8A (0.4V)

	ILMT_1
0	1.5A
1	3.2A

0x45h	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Register	VGH1_ UVLO_State	STV1_ Reset	CH_MODE			Power Off Discharge Threshold		
Initial(HEX)	0	1	011			000		

Description

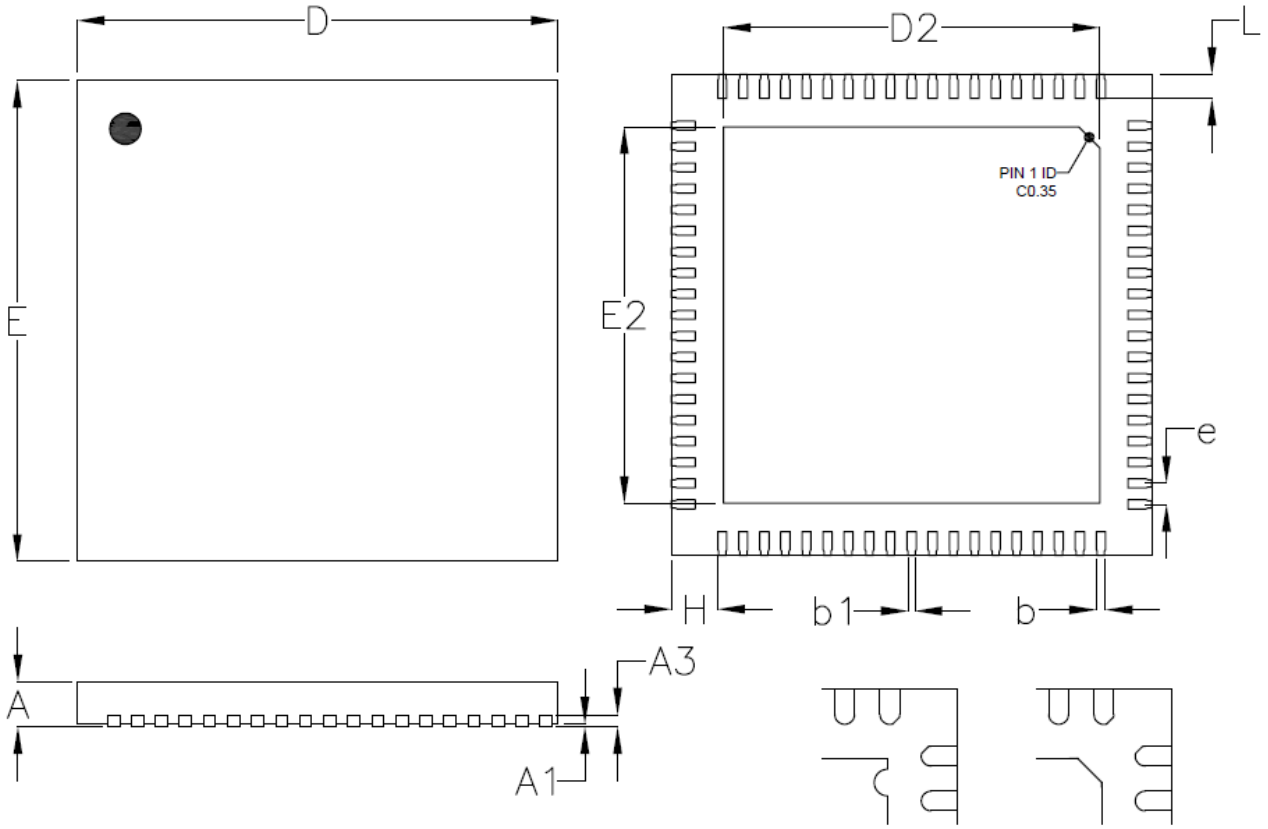
	Power Off Discharge Threshold
000	VIN_UVLO_F
001	7.0V
010	7.5V
011	8.0V
100	8.5V
101	9.0V
110	9.5V
111	10.0V

CH_MODE:
0x41[2:0] = 000 : 4 phase of L/S operation
0x41[2:0] = 001 : 6 phase of L/S operation
0x41[2:0] = 010 : 8 phase of L/S operation
0x41[2:0] = 011 : 10 phase of L/S operation
0x41[2:0] = 100 : 12 phase of L/S operation
0x41[2:0] = 101 : 12 phase of L/S operation
0x41[2:0] = 110 : 12 phase of L/S operation
0x41[2:0] = 111 : 12 phase of L/S operation

	STV1_Reset
0	Don’t reset anything
1	STV1 rising reset all CLKx to VGL2

	VGH1_UVLO_State
0	Disable
1	Enable

Outline Dimension



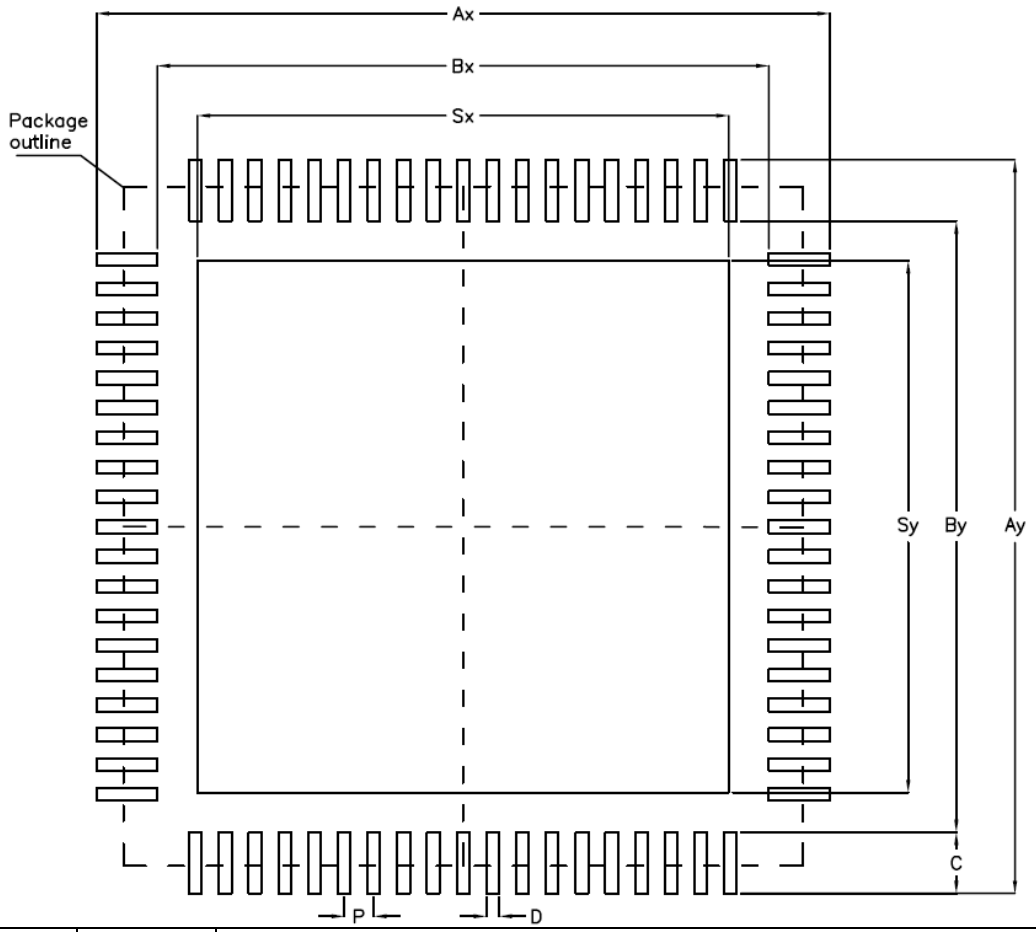
DETAILA
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.000	0.031	0.039
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.100	0.200	0.004	0.008
b1	0.120		0.005	
D	7.950	8.050	0.313	0.317
D2	6.210	6.310	0.244	0.248
E	7.950	8.050	0.313	0.317
E2	6.210	6.310	0.244	0.248
E	0.350		0.014	
L	0.350	0.450	0.014	0.018
H	0.775		0.031	

V-Type 76E QFN 8x8 Package

Footprint Information



Package	Number of Pin	Footprint Dimension (mm)									Tolerance
		P	Ax	Ay	Bx	By	C	D	Sx	Sy	
V/W/U/XQFN8*8-76E	76	0.35	8.64	8.64	7.20	7.20	0.72	0.15	6.26	6.26	±0.05

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