PMIC for TFT-LCD TV Panels

General Description

The CS601C is a programmable multi-functional power solution with integrated 12 channels of level shifter for TFT-LCD panels. It contains an asynchronous step-up converter for main power and a step-down converter to provide the driver and logic voltages for the system. Moreover, a positive charge pump regulator provides the adjustable gate-high voltage, VGH; a negative charge pump regulator provides the gate-low voltage, VGL. The 14-CH gamma buffers and 2-CH VCOM control are also integrated. Output level and sequence of all channels is programmable by the I2C interface.

The AVDD Boost and VDD Buck converter incorporate current mode, fixed-frequency, pulse width modulation (PWM) circuitry and FCCM Mode in light load to gain better transient response and output ripple.

With high current capabilities, the CS601C is ideal for large screen monitor panels and LCD TV applications with 5V/12V supply voltage, and it also integrates complete protection functions including, OVP, UVP, OCP, and OTP. The CS601C is available in a VQFN-72L 8x8 package.

Ordering and Marking Information

|  |  |  |
| --- | --- | --- |
| **Part No.** | **Marking Information** | Package Type |
| CS601C | NA | VQFN-72L 8x8 (V-Type) |

Features

* 4.3V to 15.5V Input Supply Voltage
* 2A Async. Boost Regulator for AVDD with 13V to 19.2V Programmable Output and Current Limit 2A/2.5A/3A/3.5A
* 1A Sync. Buck Regulator for VDD with 2.2V to 3.7V Programmable Output
* Negative Charge Pump Regulator for VGL with 20V to 4.5V Programmable Output
* Negative Operational Amplifier for VSS with 16V to 4.5V
* Positive Charge Pump Regulator for VGH with 20V to 40V Programmable Output
* 1-CH HAVDD Operational Amplifier
* 14-CH Gamma Buffers with Programmable Output
* 2-CH VCOM Buffers with Programmable Output
* Programmable Sequencing
* 12 Channels of Level Shifters Support 8-CH CLKOUT, STVOUT, 2-CH LC and DCHG.
* Suitable for 4/6/8 Phase and 1/2/4 Line Level Shifter Applications
* Over-temperature Protection
* Overvoltage Protection
* I2C-Compatible Interface for Register Control
* Thin 72-Lead VQFN Package

Applications

TFT-LCD TV Panels

TFT-LCD Monitor Panels

Simplified Application Circuit



Pin Configuration

(TOP VIEW)



VQFN-72L 8x8

Typical Application Circuit



Figure 1. Application Circuit (VGH change pump x1 and VGL change pump x2)



Figure 2. Application Circuit (VGH change pump x2 and VGL change pump x2)

Functional Pin Description

| **Pin No.** | **Pin Name** | I/O | Pin Function |
| --- | --- | --- | --- |
| 1 | CLK\_ON | I | Level shifter logic signal input for clock out on |
| 2 | CLK\_OFF | I | Level shifter logic signal input for clock out off |
| 3 | STV | I | Level shifter logic signal input for STVOUT |
| 4 | NC | -- | Internal not connected. |
| 5 | LC | I | Level shifter logic signal input for LC1/2 |
| 6 | AGND | -- | Analog ground. |
| 7 | VSS | I | Operational amplifier output for VSS |
| 8 | NC | -- | Internal not connected. |
| 9 | VGL | I | Feedback voltage input for VGL. |
| 10 | DRVN | O | Negative charge pump (VGL) base drive signal pin. |
| 11 | NC | -- | Internal not connected. |
| 12 | NC | -- | Internal not connected. |
| 13 | NC | -- | Internal not connected. |
| 14 | VIN | I | Power input pin for VDD |
| 15 | PGND | -- | Power ground. |
| 16 | VDD\_SW | I/O | Switch node of the buck converter. |
| 17 | VDD | I | Feedback voltage input for VDD. |
| 18 | EN | I | Enable control pin. The EN pin and EN bit control the ON/OFF status of AVDD, HAVDD, VGH, VCOM and GMA buffer. EN pin = 1, EN bit = 1 and DLY0 finish = 1 turn on these channels. 1M pull down resistor is connected from this pin to ground. |
| 19 | INVL | I | Supply voltage input of internal regulator. |
| 20 | COMPA | O | Boost converter (AVDD) compensation pin. |
| 21 | NC | -- | Internal not connected. |
| 22 | VL | O | Internal regulator output pin. |
| 23 | BANK\_SEL | I | Registers bank selection. Select Bank A when this pin is pulled low; Select Bank B when this pin is pulled high. The main chip should make sure that value in the registers are correct before switching to another bank. |
| 24 | NC | -- | Internal not connected. |
| 25 | SDA | I/O | I2C-compatible serial bidirectional data line. |
| 26 | SCL | I | I2C-compatible clock input. |
| 27 | PGND | -- | Power ground. |
| 28 | LXA | I/O | Switch node of the boost converter. |
| 29 | SWI | I | Input of the Isolation MOSFET. |
| 30 | NC | -- | Internal not connected. |
| 31 | SWO | O | Output of the Isolation MOSFET. |
| 32 | OPO | O | HAVDD operational amplifier output. |
| 33 | NC | -- | Internal not connected. |
| 34 | NC | -- | Internal not connected. |
| 35 | VCOM2 | O | VCOM2 operational amplifier output. |
| 36 | NC | -- | Internal not connected. |
| 37 | NC | -- | Internal not connected. |
| 38 | VCOM1 | O | VCOM1 operational amplifier output. |
| 39 | G14 | O | CH14 output of gamma reference buffer. |
| 40 | G13 | O | CH13 output of gamma reference buffer. |
| 41 | G12 | O | CH12 output of gamma reference buffer. |
| 42 | G11 | O | CH11 output of gamma reference buffer. |
| 43 | G10 | O | CH10 output of gamma reference buffer. |
| 44 | G9 | O | CH9 output of gamma reference buffer. |
| 45 | G8 | O | CH8 output of gamma reference buffer. |
| 46 | G7 | O | CH7 output of gamma reference buffer. |
| 47 | G6 | O | CH6 output of gamma reference buffer. |
| 48 | G5 | O | CH5 output of gamma reference buffer. |
| 49 | G4 | O | CH4 output of gamma reference buffer. |
| 50 | G3 | O | CH3 output of gamma reference buffer. |
| 51 | G2 | O | CH2 output of gamma reference buffer. |
| 52 | G1 | O | CH1 output of gamma reference buffer. |
| 53 | AGND | -- | Analog ground. |
| 54 | PGND | -- | Power ground. |
| 55 | NC | -- | Internal not connected. |
| 56 | NC | -- | Internal not connected. |
| 57 | DRVP | I/O | Driver output for positive linear-regulator. |
| 58 | VGH | I | Feedback voltage input for VGH and level shifter supply. |
| 59 | NC | -- | Internal not connected. |
| 60 | LC2 | O | Level shifter output signal (Low frequency clock) out-of-phase with LC. |
| 61 | LC1 | O | Level shifter output signal (Low frequency clock) in-phase with LC. |
| 62 | NC | -- | Internal not connected. |
| 63 | STVOUT | O | Level shifter STVOUT output signal. |
| 64 | CLKOUT1 | O | Level shifter CLK output 1 |
| 65 | CLKOUT2 | O | Level shifter CLK output 2. |
| 66 | CLKOUT3 | O | Level shifter CLK output 3. |
| 67 | CLKOUT4 | O | Level shifter CLK output 4. |
| 68 | CLKOUT5 | O | Level shifter CLK output 5. |
| 69 | CLKOUT6 | O | Level shifter CLK output 6. |
| 70 | CLKOUT7 | O | Level shifter CLK output 7. |
| 71 | CLKOUT8 | O | Level shifter CLK output 8. |
| 72 | DCHG | O | Level shifter output for discharge function. |
| 73  (Exposed Pad) | PGND | -- | The exposed pad must be soldered to a large PCB and connected to PGND for maximum power dissipation. |

Function Block Diagram

**For PMIC**



**For LSIC**



Operation

The CS601C is a 3-in-1 power management IC. There are 34 output channels, and the outputs are included: VDD, AVDD, HAVDD, VGH, VGL, VSS, VCOM1-2, G1-14, DCHG, STVOUT, CLKOUT1-8, LC1-2. In TFT-LCD panel application, the CS601C can be used by the I2C interface to program these functions. For example, to enable or disable each output, to set each output voltage, to control the power-on sequence and the switching frequency, etc. Refer to the register table for detailed control descriptions, and the I2C protocol is described in the Application Information section.

Timing Diagram

**PMIC Power Selection**



Figure 3. Power Selection Sequence\_PMIC

PMIC Timing



Figure 4. Timing Sequence\_PMIC

| **Address** | **Name** | **Description** | | **Default Value** | | **Resolution** | **Range** | |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 01h/31h | Timing Control | [6] | AVDD\_SS | 10ms | 0 | 10ms | 10ms to 20m | (0h to 1h) |
| [5:4] | DLY2 | 3ms | 01 | 3ms | 0ms to 9ms | (0h to 3h) |
| [3:2] | DLY1 | 10ms | 00 | 5ms | 10ms to 25ms | (0h to 3h) |
| [1:0] | DLY0 | 9ms | 01 | 3ms | 6ms to 15ms | (0h to 3h) |

**Table 1. EN Control and Channel Output Behavior**

| **Case** | **EN\_PIN** | **EN\_VDD 00h[0]** | **EN\_CTRL 00h[3]** | **EN\_VGL 00h[1]** | **EN\_VSS 00h[2]** | **EN\_AVDD 00h[4]** | **EN\_VGH 00h[5]** | **VDD\_O** | **VGL\_O** | **VSS\_O** | **SWO\_O** | **VGH\_O** | **VCOM\_O** | **GMA\_O** | **OPO (HAVDD)** | **Description** |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1.1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | All channel are normal power on |
| 1.2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | All channel are turn-off |
| 2.1 | **1 → 0** | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | EN\_PIN = 1 to 0, VDD/VGL/VSS are always keep 1. SWO/VGH/VCOM/GMA/OPO are turn-off |
| 2.2 | **0 → 1** | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | EN\_PIN = 0 to 1, VDD/VGL/VSS are always keep 1. SWO/VGH/VCOM/GMA/OPO repeat soft- start power on without DLY0 |
| 3.1 | 1 | **1 → 0** | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | **EN \_VDD = 1 to 0**, VDD is turn-off **and VGL OLP causes IC fault shutdown** |
| 3.2 | 1 | **0 → 1** | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | **EN \_VDD = 0 to 1,** VDD is repeat soft-start **and VGL OLP causes IC fault shutdown,** |
| 3.3 | 1 | **1 → 0** | 1 | **1 → 0** | **1 → 0** | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | EN \_VDD/VGL/VSS = 1 to 0, VDD/VGL/VSS are off and other channels are normal. |
| 3.4 | 1 | **0 → 1** | 1 | **0 → 1** | **0 → 1** | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | EN \_VDD/VGL/VSS = 0 to 1, VDD/VGL/VSS soft-start at the same time and other channel are normal. |
| 4.1 | 1 | 1 | **1 → 0** | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | EN CTRL = 1 to 0, VDD are always keep 1. Other channels are turn-off |
| 4.2 | 1 | 1 | **0 → 1** | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | EN CTRL = 1 to 0, VDD are always keep 1. Other channels are repeat soft- start with DLY1/2. |
| 5.1 | 1 | 1 | 1 | **1 → 0** | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | **EN \_VGL = 1 to 0**, VDD is always keep 1 **and VSS OLP causes IC fault shutdown** |
| 5.2 | 1 | 1 | 1 | **0 → 1** | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | **EN \_VGL = 1 to 0,** VDD is always keep 1 **and VSS OLP causes IC fault shutdown** |
| 5.3 | 1 | 1 | 1 | **1 → 0** | **1 → 0** | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | EN \_VGL/VSS = 1 to 0, VGL/VSS are off and other channels are normal. |
| 5.4 | 1 | 1 | 1 | **0 → 1** | **0 → 1** | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | EN \_VGL/VSS = 0 to 1, VGL/VSS are repeat soft- start with delay and other channels are normal. |
| 6.1 | 1 | 1 | 1 | 1 | **1 → 0** | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | EN \_VSS = 1 to 0, VSS is turn-off and other channel are normal. |
| 6.2 | 1 | 1 | 1 | 1 | **0 → 1** | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | EN \_VSS = 0 to 1, VSS are repeat soft- start and other channels are normal. |
| 7.1 | 1 | 1 | 1 | 1 | 1 | **1 → 0** | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | **EN \_AVDD = 1 to 0,** VDD/VGL/VSS are always keep 1 **and VGH OLP causes IC fault shutdown** |
| 7.2 | 1 | 1 | 1 | 1 | 1 | **0 → 1** | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | **EN \_AVDD = 0 to 1,** VDD/VGL/VSS are always keep 1 **and VGH OLP causes IC fault shutdown** |
| 7.3 | 1 | 1 | 1 | 1 | 1 | **1 → 0** | **1 → 0** | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | EN \_AVDD/VGH = 1 to 0, VDD/VGL/VSS are always keep 1 and Other channels are turn-off |
| 7.4 | 1 | 1 | 1 | 1 | 1 | **0 → 1** | **0 → 1** | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | EN \_AVDD/VGH = 0 to 1, VDD/VGL/VSS are always keep 1 and Other channels are repeat soft- start with DLY1/2. |
| 8.1 | 1 | 1 | 1 | 1 | 1 | 1 | **1 → 0** | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | EN \_VGH = 1 to 0, VGH is off and other channels are normal. |
| 8.2 | 1 | 1 | 1 | 1 | 1 | 1 | **0 → 1** | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | EN \_VGH = 0 to 1, VGH are repeat soft- start after I2C STOP CMD |

**Level Shift Timing**



Figure 5. Timing Sequence\_Level Shifter

Table 2.1 LS Power On Condition

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Case | Analog Input Power Condition | | | | | Level Shifter Input | | | Level Shifter Output | | | |
| Dis\_charge | VDD | VGH | Blanking  130ms | 1st STV rising edge after 130ms blanking | STV | CLK\_ON CLK\_OFF | LC | STVOUT | CLKOUTx | LC1/2 | DCHG |
| 1 | <UVLO | <UVLO | <UVLO | 0 | 0 | w/i or w/o signal | w/i or w/o signal | w/i or w/o signal | VGL | VGL | VGL | VSS |
| 2 | >UVLO | <UVLO | <UVLO | 0 | 0 | w/i or w/o signal | w/i or w/o signal | w/i or w/o signal | VGL | VGL | VGL | VSS |
| 3 | >UVLO | >UVLO | <UVLO | 0 | 0 | w/i or w/o signal | w/i or w/o signal | w/i or w/o signal | VGL | VGL | VGL | VSS |
| 4 | >UVLO | >UVLO | >UVLO | 0 | 0 | w/i or w/o signal | w/i or w/o signal | w/i  signal | VGL | VGL | Normal  Operation | VSS |
| 5 | >UVLO | >UVLO | >UVLO | 1 | 0 | w/i  signal | w/i or w/o signal | w/i  signal | Normal  Operation | VGL | Normal  Operation | VSS |
| 6 | >UVLO | >UVLO | >UVLO | 1 | 1 | w/i  signal | w/i  signal | w/i  signal | Normal  Operation | Normal  Operation | Normal  Operation | VSS |

Table 2.2 LS Power Off Condition

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Normal Power Off (Dis\_charge >> VDD\_UVLO >> VGH UVLO >> VGH\_DCD | | | | | | | | | | | | | |
| Case | Analog Input Power Condition | | | | | | Level Shifter Input | | | Level Shifter Output | | | |
| Dis\_charge | VDD | VGH | VGH\_ DCD | Blanking  130ms | 1st STV rising edge after 130ms blanking | STV | CLK\_ON CLK\_OFF | LC | STVOUT | CLKOUTx | LC1/2 | DCHG |
| 1 | >UVLO | >UVLO | >UVLO | >3V | 1 | 1 | w/i signal | w/i signal | w/i signal | Normal  Operation | Normal  Operation | Normal  Operation | VSS |
| 2 | <UVLO | >UVLO | >UVLO | >3V | 0 | 0 | w/i or w/o signal | w/i or w/o signal | w/i or w/o signal | \*VGH/HiZ | \*VGH/HiZ | \*VGH/HiZ | \*VGH/HiZ |
| 3 | <UVLO | <UVLO | >UVLO | >3V | 0 | 0 | w/i or w/o signal | w/i or w/o signal | w/i or w/o signal | \*VGH/HiZ | \*VGH/HiZ | \*VGH/HiZ | \*VGH/HiZ |
| 4 | <UVLO | <UVLO | <UVLO | >3V | 0 | 0 | w/i or w/o signal | w/i or w/o signal | w/i or w/o signal | \*VGH/HiZ | \*VGH/HiZ | \*VGH/HiZ | \*VGH/HiZ |
| 5 | <UVLO | <UVLO | <UVLO | <3V | 0 | 0 | w/i or w/o signal | w/i or w/o signal | w/i or w/o signal | VGL | VGL | VGL | VSS |

Table 3.1 LS Power Off Condition (Abnormal ─ I)

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Abormal Power Off (VDD\_UVLO >> Dis\_charge >> VGH UVLO >> VGH\_DCD | | | | | | | | | | | | | | | | |
| Case | Analog Input Power Condition | | | | | | | Level Shifter Input | | | | Level Shifter Output | | | | |
| VDD | Dis\_charge | VGH | VGH\_ DCD | Blanking  130ms | 1st STV rising edge after 130ms blanking | STV | | CLK\_ON CLK\_OFF | LC | STVOUT | | CLKOUTx | LC1/2 | DCHG |
| 1 | >UVLO | >UVLO | >UVLO | >3V | 1 | 1 | w/i signal | | w/i signal | w/i signal | Normal  Operation | | Normal  Operation | Normal  Operation | VSS |
| 2 | <UVLO | >UVLO | >UVLO | >3V | 0 | 0 | w/i or w/o signal | | w/i or w/o signal | w/i or w/o signal | VGL | | VGL | VGL | VSS |
| 3 | <UVLO | <UVLO | >UVLO | >3V | 0 | 0 | w/i or w/o signal | | w/i or w/o signal | w/i or w/o signal | \*VGH/HiZ | | \*VGH/HiZ | \*VGH/HiZ | \*VGH/HiZ |
| 4 | <UVLO | <UVLO | <UVLO | >3V | 0 | 0 | w/i or w/o signal | | w/i or w/o signal | w/i or w/o signal | \*VGH/HiZ | | \*VGH/HiZ | \*VGH/HiZ | \*VGH/HiZ |
| 5 | <UVLO | <UVLO | <UVLO | <3V | 0 | 0 | w/i or w/o signal | | w/i or w/o signal | w/i or w/o signal | VGL | | VGL | VGL | VSS |

Table 3.2 LS Power Off Condition (Abnormal ─ II)

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Abormal Power Off (VDD\_UVLO >> VGH UVLO>> Dis\_charge >> VGH\_DCD | | | | | | | | | | | | | |
| Case | Analog Input Power Condition | | | | | | Level Shifter Input | | | Level Shifter Output | | | |
| VDD | VGH | Dis\_charge | VGH\_ DCD | Blanking  130ms | 1st STV rising edge after 130ms blanking | STV | CLK\_ON CLK\_OFF | LC | STVOUT | CLKOUTx | LC1/2 | DCHG |
| 1 | >UVLO | >UVLO | >UVLO | >3V | 1 | 1 | w/i signal | w/i signal | w/i signal | Normal  Operation | Normal  Operation | Normal  Operation | VSS |
| 2 | <UVLO | >UVLO | >UVLO | >3V | 0 | 0 | w/i or w/o signal | w/i or w/o signal | w/i or w/o signal | VGL | VGL | VGL | VSS |
| 3 | <UVLO | <UVLO | >UVLO | >3V | 0 | 0 | w/i or w/o signal | w/i or w/o signal | w/i or w/o signal | VGL | VGL | VGL | VSS |
| 4 | <UVLO | <UVLO | <UVLO | >3V | 0 | 0 | w/i or w/o signal | w/i or w/o signal | w/i or w/o signal | \*VGH/HiZ | \*VGH/HiZ | \*VGH/HiZ | \*VGH/HiZ |
| 5 | <UVLO | <UVLO | <UVLO | <3V | 0 | 0 | w/i or w/o signal | w/i or w/o signal | w/i or w/o signal | VGL | VGL | VGL | VSS |

**Note. \*: LS output discharge can be controlled by I2C 02/32h[7]**

Absolute Maximum Ratings (Note 1)

* VIN, INVL, LXA, SWI, SWO to PGND 0.3V to 23V
* LXA to SWI 0.3V to 23V
* SWI to SWO 0.3V to 23V
* OPO to PGND 0.3V to (SWI+0.3V)
* EN, VL, SDA, SCL, BANK\_SEL to GND 0.3V to 6V
* VDD, COMPA to GND 0.3V to 23V
* LXB to GND 0.3V to (VIN+0.3V)
* VSS, VGL, DRVN to GND 24V to 0.7V
* VGH, DRVP to GND 0.3V to 58V
* VCOM1, VCOM2 to GND 0.3V to 23V
* VSS to VGL 0.3V
* PGND to AGND 0.3V
* (G1~G14) to AGND 0.3V to (SWO+0.3V)
* LC, STV, CLK\_ON, CLK\_OFF to AGND −0.3V to 6V
* CLKOUT1~8, STVOUT, LC1, LC2 to GND (−0.3V+VGL) to VGH+0.3V
* DCHG to GND (−0.3V+VSS) to VGH+0.3V
* Power Dissipation, PD @ TA = 25°C

VQFN-72L 8x8 4.01W

* Package Thermal Resistance (Note 2)

VQFN-72L 8x8, JA 24.9°C/W

VQFN-72L 8x8, JC 3.3°C/W

* Lead Temperature (Soldering, 10 sec.) 260°C
* Junction Temperature 150°C
* Storage Temperature Range 65°C to 150°C
* ESD Susceptibility (Note 3)

HBM (Human Body Model) 2kV

Recommended Operating Conditions (Note 4)

* Ambient Temperature Range 40°C to 85°C
* Junction Temperature Range 40°C to 125°C

Electrical Characteristics

(VIN = 5/12V, VAVDD = 16V, VDD = 3.3V, VHAVDD = 8V, VGH = 30V, VGL = 10V, VSS = 6V, TA = 25°C, unless otherwise specified)

| **Parameter** | **Symbol** | **Test Conditions** | **Min** | **Typ** | **Max** | **Unit** |
| --- | --- | --- | --- | --- | --- | --- |
| Supply Current | | | | | | |
| Input Voltage Range | VIN\_SEL1 | SEL\_5V/12V 00h[7] = 1 | 4.3 | 5 | 6 | V |
| VIN\_SEL0 | SEL\_5V/12V 00h[7] = 0 | 9.5 | 12 | 15.5 | V |
| VIN Quiescent Current | IQVIN | SW not switching, EN = 0, SEL\_5V/12V 00h[7] = 1 or 0 | -- | TBD | -- | mA |
| INVL Quiescent Current | IQINVL | SW not switching, EN = 0, SEL\_5V/12V 00h[7] = 1 or 0 | -- | TBD | -- | mA |
| VIN Undervoltage Lockout Threshold | VIN,UVLO\_SEL1 | VIN rising, SEL\_5V/12V 00h[7] = 1 | -- | 4 | -- | V |
| Hysteresis, SEL\_5V/12V 00h[7] = 1 | -- | 0.3 | -- | V |
| VIN Undervoltage Lockout Threshold | VIN,UVLO\_SEL0 | VIN rising, SEL\_5V/12V 00h[7] = 0 | -- | 7.2 | -- | V |
| Hysteresis, SEL\_5V/12V 00h[7] = 0 | -- | 0.5 | -- | V |
| VL Output Voltage | VL | VIN > 5.5V | -- | 5 | -- | V |
| VL Undervoltage Lockout Threshold | VL,UVLO\_SEL | VIN rising | -- | 3 | -- | V |
| Hysteresis | -- | 0.3 | -- | V |
| Fault Delay Time Duration to IC Shutdown | UVPDLY | UVP trigger delay time | -- | 3 | -- | ms |
| SCPDLY | SCP trigger delay time | -- | 10 | -- | s |
| Switching Frequency | FSW500k | 02h/32h[6] = 0h | 400 | 500 | 600 | kHz |
| FSW750k | 02h/32h[6] = 1h | 600 | 750 | 900 | kHz |
| EN/BANK\_SEL/CLK\_O  N/CLK\_OFF/STV/LC  Logic High Level | VIH |  | 1.7 | -- | -- | V |
| EN/BANK\_SEL/CLK\_O  N/CLK\_OFF/STV/LC  Logic Low Level | VIL |  | -- | -- | 0.6 | V |
| EN Pull Down Resistance | RLOW1 |  | -- | 1 | -- | M |
| CLK\_ON/CLK\_OFF/STV  /LC Pull Down Resistance | RLOW2 |  | -- | 400 | -- | k |
| Thermal Shutdown Threshold | OTP | Temperature rising | -- | 150 | -- | °C |
| **Delay Time (DLYVDD and DLY0/1/2)** | | | | | | |
| VDD Delay Time | DLYVDD | VIN UVLO\_R to VDD Start | -- | 3 | -- | ms |
| DLY0 Delay Time | DLY0 | VSS soft-start done to GD MOSFET turn-on, 2Bits, 3ms/step, 01h/31h[1:0] | 6 | -- | 15 | ms |
| DLY1 Delay Time | DLY1 | GD MOSFET turn-on to SWO soft-start start, 2Bits, 5ms/step, 01h/31h[3:2] | 10 | -- | 25 | ms |
| DLY2 Delay Time | DLY2 | SWO soft-start Done to VGH soft-start start , 2Bits, 3ms/step, 01h/31h[5:4] | 0 | -- | 9 | ms |
| Logic Inputs (SDA SCL) | | | | | | |
| Input High Voltage | VIH |  | 1.7 | -- | -- | V |
| Input Low Voltage | VIL |  | -- | -- | 0.6 | V |
| Input Leakage Current | IIH, IIL | VIN = 0 or 3.3V | 1 | 0.01 | 1 | A |
| Input Capacitance |  |  | -- | 5 | -- | pF |
| SDA/SCL Output Low Voltage | VOL | ISINK = 3mA | -- | -- | 0.4 | V |
| I2C Timing Characteristics | | | | | | |
| Serial-Clock Frequency | fSCL |  | 1 | -- | 400 | kHz |
| Bus Free Time Between STOP and START Conditions | tBUF |  | 1.3 | -- | -- | s |
| Hold Time (Repeated) START Condition | tHD,STA |  | 0.6 | -- | -- | s |
| SCL Pulse-Width Low | tLOW |  | 1.3 | -- | -- | s |
| SCL Pulse-Width High | tHIGH |  | 0.6 | -- | -- | s |
| Setup Time for a Repeated START Condition | tSU,STA |  | 0.6 | -- | -- | s |
| Data Hold Time | tHD,DAT |  | 0 | -- | 900 | ns |
| Data Setup Time | tSU,DAT |  | 100 | -- | -- | ns |
| SDA and SCL Receiving Rise Time | tR | Depend on load | 20  + 0.1CB | -- | 300 | ns |
| SDA and SCL Receiving Fall Time | tF | Depend on load | 20  + 0.1CB | -- | 300 | ns |
| SDA Transmitting Fall Time | tF |  | 20  + 0.1CB | -- | 250 | ns |
| Setup Time for STOP Condition | tSU\_STO |  | 0.6 | -- | -- | s |
| Bus Capacitance | CB |  | -- | -- | 400 | pF |
| Pulse Width of Suppressed Spike | tSP |  | -- | 85 | -- | ns |
| BOOST Converter (AVDD/SWO) | | | | | | |
| Output Voltage Range | SWO | 6Bits, 0.1V/step, 02h/32h[5:0], VSWO>1.14×VIN | 13 | -- | 19.2 | V |
| Output Voltage Accuracy (Default) | ACCSWO,DEFAULT | 02h/32h[5:0] = 1Fh | 15.84 | 16 | 16.16 | V |
| Output Voltage Accuracy | ACCSWO | VIN = 9.5 to 15.5V and 4.3 to 6V, SWO = 13V to 19.2V, No load | 1 | -- | 1 | % |
| Maximum Duty | DMAXSWO |  | 80 | -- | -- | % |
| Minimum On Time | MOTSWO |  | -- | 75 | -- | ns |
| Line Regulation | LIRSWO | 9.5V ≤ VIN ≤15.5V, IOUT = 1mA | -- | 0.08 | -- | %/V |
| Load Regulation | LORSWO | 1mA ≤ IOUT ≤1A | -- | 0.5 | -- | %/A |
| N-MOSFET On-Resistance | RDS\_ON | ILXA = 500mA | -- | 200 | -- | m |
| N-MOSFET Switch Current Limit before AVDD Soft-start Done | ILIM,SWO\_SS |  | 1 | 1.5 | 2 | A |
| N-MOSFET Switch Current Limit | ILIM,SWO\_2A | 2Bits, 0.5A/step,  0Ah/3Ah[7:6] = 0h | 2 | 2.5 | 3 | A |
| ILIM,SWO\_3.5A | 2Bits, 0.5A/step,  0Ah/3Ah[7:6] = 3h | 3.5 | 4.25 | 5 |
| Soft-Start Time | Tss\_SWO | Programmable soft-start time, 1Bits, 10ms/step, 01h/31h[6] | 10 | -- | 20 | ms |
| Switch Leakage Current | ILEAK | VLXA = 16.5V | -- | -- | 5 | A |
| SWI Overvoltage Protection | OVPSWI | SWI rising | 20.5 | 21.5 | 22.5 | V |
| SWI Overvoltage Protection Hysteresis | OVPSWI,HYS |  | -- | 1.5 | -- | V |
| OVP Times before Latch  Off | TOVPSWI | AVDD\_OVP 03h/33h[5] = 1 | -- | 10 | -- | Times |
| Undervoltage Protection Threshold | UVPSWO | SWO falling | -- | 80 | -- | % |
| Undervoltage Protection Delay Time | UVPDLY,SWO | UVP trigger delay time | -- | 3 | -- | ms |
| Short Circuit Protection Threshold | SCPSWO | SWO falling | -- | 60 | -- | % |
| Short Circuit Protection Delay Time | SCPDLY | SCP trigger delay time | -- | 10 | -- | s |
| Isolation Switch (GD) | | | | | | |
| P-MOSFET On-Resistance | RDS(ON) | ISWI =0.2A | -- | 200 | 250 | m |
| Switch Current | ILIMGD |  | -- | -- | 3 | A |
| Short Circuit Trigger Duration | SCPDLY | ISWI ≥ 3.1A | -- | 100 | -- | s |
| SYNC. Buck Converter (VDD) | | | | | | |
| Output Voltage Range | VDD | 5Bits,0.05V/step,03h/33h[4:0] | 2.2 | -- | 3.7 | V |
| Output Voltage Accuracy (Default) | ACCVDD,DEFAULT | 03h/33h[4:0] = 16h | 3.234 | 3.3 | 3.366 | V |
| Output Voltage Accuracy | ACCVDD | VIN = 9.5 to 15.5V and 4.3 to 6V, VDD = 2.2V to 3.7V, No load | 2 | -- | 2 | % |
| Maximum Duty | DMAXVDD |  | 84 | 90 | 96 | % |
| Minimum On Time | MOTVDD |  | -- | 65 | -- | ns |
| Line Regulation | LIRVDD | VIN = 9.5 to 15.5V, ILoad = 200mA, VDD = 3.3V | -- | 0.05 | -- | %/V |
| Load Regulation | LORVDD | 1mA ≤ IOUT ≤1A, VDD = 3.3V | -- | 0.25 | -- | %/A |
| High Side P-MOSFET On-Resistance | RDS\_HS | ILXB = 100mA | -- | 400 | -- | m |
| Low Side N-MOSFET On-Resistance | RDS\_LS | ILXB = 100mA | -- | 200 | -- | m |
| Switch Current Limit | ILIM,VDD |  | 1 | -- | -- | A |
| VIN to VDD\_SW  P-MOSFET Leakage Current | Ileak\_P\_VDD | VVDD1\_SW = 0V | -- | -- | 5 | A |
| VDD\_SW to PGND  N-MOSFET Leakage Current | Ileak\_N\_VDD | VVDD1\_SW = 15.5V | -- | -- | 5 | A |
| Overvoltage Protection | OVPVDD | VDD rising | -- | 120 | -- | % |
| Overvoltage Protection Hysteresis | OVPVDD,HYS |  | -- | 10 | -- | % |
| Undervoltage Protection Threshold | UVPVDD | VDD falling | -- | 80 | -- | % |
| Undervoltage Protection Delay Time | UVPDLY,VDD | UVP trigger delay time | -- | 3 | -- | ms |
| Short Circuit Protection Threshold | SCPVDD | VDD falling | -- | 60 | -- | % |
| Short Circuit Protection Delay Time | SCPDLY | SCP trigger delay time | -- | 10 | -- | s |
| Soft-Start Time | tSS\_vDD1 |  | -- | 3 | -- | ms |
| Operating Amplifier (HAVDD/OPO) | | | | | | |
| Output Voltage Range | OPO |  | (G7+G8)/2 | | | V |
| Input Offset Voltage | OSOPO |  | 50 | -- | 50 | mV |
| Input Common Mode Range | CMVIN |  | 2 | -- | SWI 2 | V |
| Input Common-Mode Rejection Ratio | CMRROPO |  | -- | 80 | -- | db |
| Output Voltage High | VOH\_OPO | IO = 100mA | -- | SWI  2 | -- | V |
| Output Voltage Low | VOL\_OPO | IO = 100mA | -- | 2 | -- | V |
| Continuous Output Current | IOUT\_OPO |  | -- | ±100 | -- | mA |
| Short-Circuit Current | ISC\_OPO |  | -- | ±300 | -- | mA |
| VGL Negative Charge Pump Regulator | | | | | | |
| Output Voltage Range | VGL | 5 Bits, 0.5V/step, 06h/36h[4:0] | 20 | 10 | 4.5 | V |
| Output Voltage Accuracy | ACCVGL\_DEFAULT | 06h/36h[4:0] = Bh | 10.3 | 10 | 9.7 | V |
| Output Voltage Accuracy | ACCVGL | VGL<-7V, No Load | 300 | -- | 300 | mV |
| VGL>-7V, No Load | 200 | -- | 200 | mV |
| DRVN Sink Current | IDRVN | Programmable DRVN current 3Bits, 1mA/step, 0Ah/3A[5:3] | 1 | 4 | 8 | mA |
| DRVN Off-leakage Current | ILEAKN | VGL< 10V, VDRVN = 10V | -- | 0.1 | 10 | A |
| Load Regulation | LORVGL | ILOAD = 0 to 150mA | -- | 5 | -- | %/A |
| Undervoltage Protection Threshold | UVPVGL | VGL rising | -- | 80 | -- | % |
| Undervoltage Protection Delay Time | UVPDLY,VGL | UVP trigger delay time | -- | 3 | -- | ms |
| Short Circuit Protection Threshold | SCPVGL | VGL rising | -- | 60 | -- | % |
| Short Circuit Protection Delay Time | SCPDLY | SCP trigger delay time | -- | 10 | -- | s |
| Soft-Start Time | tSS\_VGL |  | -- | 3 | -- | ms |
| **VSS Negative Regulator** | | | | | | |
| Output Voltage Range | VSS | 5Bits, 0.5V/step, 04h/34h[4:0] | 16 | 6 | 4.5 | V |
| Output Voltage Accuracy (Default) | ACCVSS,DEFAULT | 04h/34h[4:0] = 3h | 6.12 | 6 | 5.88 | V |
| Output Voltage Accuracy | ACCVSS | VSS = 16V to 4.5V, No load | 2 | -- | 2 | % |
| Undervoltage Protection Threshold | UVPVSS | VSS rising | -- | 80 | -- | % |
| Undervoltage Protection Delay Time | UVPDLY,VSS | UVP trigger delay time | -- | 3 | -- | ms |
| Short Circuit Protection Threshold | SCPVSS | VSS rising | -- | 60 | -- | % |
| Short Circuit Protection Delay Time | SCPDLY | SCP trigger delay time | -- | 10 | -- | s |
| Soft-Start Duration | tSS\_VSS |  | -- | 3 | -- | ms |
| **VGH Positive Charge Pump Regulator** | | | | | | |
| Output Voltage Range | VGH | 5Bits, 1V/step, 08h/38h[4:0] | 20 | 30 | 40 | V |
| Output Voltage Accuracy (Default) | ACCVGH,DEFAULT | 08h/38h[4:0] = Ah | 29.4 | 30 | 30.6 | V |
| Output Voltage Accuracy | ACCVGH | VGH = 20V to 40V, No load | 2 | -- | 2 | % |
| DRVP Sink Current | IDRVP | Programmable DRVP current  3Bits, 1mA/step, 0Ah/3Ah[2:0] | 1 | 4 | 8 | mA |
| DRVP Off-leakage Current | ILEAKP | VGH >30V, VDRVP = 34V | -- | 0.1 | 10 | A |
| Load Regulation | LORVGH | ILOAD = 0 to 150mA | -- | 5 | -- | %/A |
| Undervoltage Protection Threshold | UVPVGH | VGH falling | -- | 80 | -- | % |
| Undervoltage Protection Delay Time | UVPDLY,VGH | UVP trigger delay time | -- | 3 | -- | ms |
| Short Circuit Protection Threshold | SCPVGH | VGH falling | -- | 60 | -- | % |
| Short Circuit Protection Delay Time | SCPDLY | SCP trigger delay time | -- | 10 | -- | s |
| Soft-Start Duration | tSS\_VGH |  | -- | 3 | -- | ms |
| **GMAx Buffer (G1 to G14)** | | | | | | |
| Full Scale Output Voltage  Range | GMAx | OPLDO, 09h/39h[4:0] = 13 to 18V | 13 | -- | 18 | V |
| Resolution | Res | 10bits/1024 steps | -- | VOPLDO / 1024 | -- | V |
| Output Low | VOL | No load DAC = 0 | **--** | 1 | -- | LSB |
| Output High | VOH | No load DAC = 1023 | -- | VOPLDO | -- | V |
| Integral Non-linearity | INL\_GMA |  | 4 | -- | 4 | LSB |
| Differential Non-linearity | DNL\_GMA |  | 1 | -- | 1 | LSB |
| Continuous Current | Icon\_GMA |  | -- | ±30 | -- | mA |
| Short-Circuit Current | Isc\_GMA |  | -- | ±75 | -- | mA |
| Program to Output Delay | td\_GMA | From ACK falling edge to programming gamma change 50% voltage at output | -- | 1 | -- | s |
| Load Regulation | LR\_GMA | 12mA & 12mA, Code = 1FFh | -- | ±0.5 | -- | mV/mA |
| **VCOMx Buffer (VCOM1/2)** | | | | | | |
| VCOMx Output Range | VCOMx | 391 steps, IVCOM = 20mA | VOPLDO x 250 / 1024 | -- | VOPLDO  x 640 / 1024 | V |
| VCOMx Resolution | RESVCOMx |  | -- | VOPLDO / 1024 | -- | V |
| Integral Non-linearity | INL |  | 4 | -- | 4 | LSB |
| Differential Non-linearity | DNL |  | 1 | -- | 1 | LSB |
| Load Regulation | LORVCOM | 100mA & +100mA, code = Default | 1 | ±0.5 | 1 | mV/mA |
| Output Current | IOUT | Outputs to VAVDD/2 or PGND | -- | ±300 | -- | mA |
| Short-Circuit Current | ISC | Outputs to VAVDD/2 or PGND | -- | ±400 | -- | mA |
| Slew Rate | VSLEW | To SWO (rising) or to PGND (falling) | -- | 30 | -- | V/s |
| 3dB Bandwidth | f3dB | RL = 10k, CL = 10pF, Buffer Configuration | -- | 30 | -- | MHz |
| Level Shifter | | | | | | |
| Power Supplies | VGH |  | 20 | -- | 40 | V |
| VGL |  | 20 | -- | 4.5 |
| VSS |  | 16 | -- | 4.5 |
| VGH - VGL |  | -- | -- | 60 |
| VGH - VSS |  | -- | -- | 56 |
| Positive Power Supply Current1 | IVGH\_LS |  | -- | 0.25 | -- | mA |
| Negative Power Supply Current | IVGL |  | -- | 0.45 | -- | mA |
| VGH UVLO Threshold | VGHUVLO | VGH rising | -- | 15 | -- | V |
| Hysteresis | -- | 8 | -- |
| VDD UVLO Threshold | VDDUVLO | VDD rising | -- | 2 | -- | V |
| Hysteresis | -- | 0.2 | -- |
| Discharge Threshold | DIS­TR\_3 | SEL\_5V/12V,00h/30h[7] = 1, 0Bh/3Bh[7:4] = 0h, Trigger Level, VIN Falling | -- | 3 | -- | V |
| DISRE\_3.5 | SEL\_5V/12V,00h/30h[7] = 1, 0Bh/3Bh[7:4] = 0h, Recover Level VIN Rising | -- | 3.5 | -- |
| Discharge Threshold | DIS­TR\_6 | SEL\_5V/12V,00h/30h[7] = 0, 0Bh/3Bh[7:4] = 0h,Trigger Level, VIN Falling | -- | 6 | -- | V |
| DISRE\_6.5 | SEL\_5V/12V,00h/30h[7] = 0, 0Bh/3Bh[7:4] = 0h, Recover Level VIN Rising | -- | 6.5 | -- |
| Discharge Function Relieve Condition After VIN< Discharge Threshold Voltage | VGH,DCD | VGH Falling | -- | 3 | -- | V |
| CLK\_ON/OFF Frequency | fCLK |  | -- | 500 | -- | kHz |
| Input Pull Low Resistance | RIN |  | -- | 400 | -- | k |
| CLK1~ 8, STVOUT LC1~2 High Side Resistance | RDSON\_HS | IOUT =10mA, sourcing | -- | 10 | -- |  |
| CLK1~ 8 ,STVOUT LC1~2 Low Side Resistance | RDSON\_LS | IOUT =10mA, sinking | -- | 10 | -- |  |
| Propagation Delay1 | tPHG1 | VGH = 30V, VGL = 10V,  CLOAD = 4.7nF, CLK\_ON rising to CLKX output rising | -- | 100 | 200 | ns |
| Propagation Delay2 | tPHG2 | VGH = 30V, VGL = 10V,  CLOAD = 4.7nF, CLK\_OFF falling to CLKX output falling | -- | 100 | 200 | ns |
| Blanking Time | TBLANKING | VGH UVLO Rising to STVx, CLKx output Active | 100 | 130 | 160 | ms |
| Output Voltage Swing  Low | VSL | IOUT = 10mA | VGL | VGL +  0.2V | VGL +  0.5V | V |
| Output Voltage Swing  High | VSH | IOUT = 10mA | VGH   0.5 | VGH   0.2V | VGH | V |
| CLKOUT 1~8, STVOUT,LC1, LC2, , DCHG (PMOS) | IOCP\_P | OCP setting,4Bits, 10mA/step, 0Ch/3Ch[7:4] | 10 | -- | 160 | mA |
| CLKOUT 1~8, STVOUT,LC1, LC2, , DCHG (NMOS) | IOCP\_N | OCP setting,4Bits, 10mA/step, 0Ch/3Ch[7:4] | 10 | -- | 160 | mA |
| Overcurrent Accuracy | IOCP\_ACC<100m | ISET < 100mA | 10 | -- | 10 | mA |
| IOCP\_ACC≥100m | ISET ≥ 100mA | 10 | -- | 10 | % |
| Overcurrent Delay  Time Rang | tOCP,DLY | 3Bits, 2s/step, 0Ch/3Ch[3:1] | 2 | -- | 16 | s |
| Overcurrent Detect  Time | tDET |  | 1.4 | 1.8 | 2.2 | s |
| Rising Time (CLKOUT1 to 8, STVOUT, LC1, LC2) | tR1 | VGH = 30V, VGL = 10V,  CLOAD = 4.7nF, 20% to 80% | -- | 350 | 700 | ns |
| Falling Time (CLKOUT1 to 8, STVOUT, LC1, LC2) | tF1 | VGH = 30V, VGL = 10V,  CLOAD = 4.7nF, 80% to 20% | -- | 350 | 700 | ns |
| Rising Time (DCHG) | tR2 | VGH = 30V, VGL = 10V,  CLOAD = 4.7nF, 20% to 80% | -- | -- | 1500 | ns |
| Falling Time (DCHG) | tF2 | VGH = 30V, VGL = 10V,  CLOAD = 4.7nF, 80% to 20% | -- | -- | 1500 | ns |

1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.
2. JA is measured under natural convection (still air) at TA = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. JC is measured at the exposed pad of the package.
3. Devices are ESD sensitive. Handling precautions are recommended.
4. The device is not guaranteed to function outside its operating conditions.

Application Information

|  |
| --- |
| ***Richtek’s component specification does not include the following information in the Application Information section. Thereby no warranty is given regarding its validity and accuracy. Customers should take responsibility to verify their own designs and reserve suitable design margin to ensure the functional suitability of their components and systems.*** |

The CS601C is a programmable multi-functional power solution with integrated 14 channels of level shifter for TFT-LCD panels. It contains 14-CH gamma buffers, and 2-CH VCOM controls are also integrated; the device also contains an asynchronous Boost converter for main power and one synchronous Buck converter to provide the driver and logic voltages for the system. Moreover, a VGH Charge pump regulator provides the adjustable gate-high voltage, VGH; a negative charge pump regulator provides the gate-low voltage, VGL. All channel output level and sequence is programmable by the I2C interface.

Soft-Start

Soft-start of the Boost/Buck converter and positive/negative charge-pump regulator are set by the internal counter. The typical soft-start duration of positive/negative charge pump regulators are 3ms, and Buck converter is 3ms.The typical delay time of isolation GD\_MOS (internal and external) is controlled by internal digital control.

Overvoltage Protection

The Boost converter has an overvoltage protection to prevent the internal MOSFET being damaged. In such an event, the output voltage rises and is monitored by the overvoltage protection comparator over the SWI pin. As soon as the comparator trips at typically 21.5V, the Boost converter turns off the N-MOSFET. The output voltage falls below the overvoltage threshold and the converter continues to operate. AVDD OVP behavior is controlled by register 03h/33h[5]

1). 03h/33h[5] = 0h: AVDD boost will stop switching when AVDD OVP triggered.

2). 03h/33h[5] = 1h: AVDD boost will stop switching when AVDD OVP triggered and IC latch off when 10times OVP are triggered in 20ms

**AVDD Isolation MOSFET Overcurrent**

When the current of internal isolated MOSFET is larger than 3.1A and lasts longer than 100s, IC will trigger AVDD short protection (IC latch off except VDD/VGL/VSS). The current limit of isolated MOSFET is 4A.

Over-Temperature Protection

The CS601C equips an Over-temperature Protection (OTP) circuitry to prevent overheating due to excessive power dissipation. The OTP will shut down all of functions when junction temperature exceeds 150°C, and it can be released form shut down state when re-power on again.

AVDD Boost Overcurrent Protection

The CS601C senses the inductor current that is flowing into the SW pin. The internal N-MOSFET will be turned off if the peak inductor current reaches 2A (typ.). The current limit level can programmable by AVDD OCP register. Thus, the output current at the current limit boundary, denoted as IOUT(LIM), can be calculated according to the following equation:

where η is the efficiency of the boost converter, ILIM is the value of the current limit, and tS is the switching period.

AVDD Boost Fault Protection

The Boost converter has a fault protection. This function disables the boost converter if SWO is detected to be below 80%. The IC will shut down if SWO remains below 80% after 3ms.

AVDD Boost Short Circuit Protection

To limit the short circuit current, the device (SW MOSFET) has a cycle-by- cycle current limit. The IC will shut down if SWO remains below 60% after 10s.

AVDD Boost Inductor Selection

The inductor value depends on the maximum input current. As a general rule the inductor ripple current is 20% to 40% of maximum input current. If 40% is selected as an example, the inductor ripple current can be calculated according to the following equation:



where η is the efficiency of the boost converter, IIN(MAX) is the maximum input current, and IRIPPLE is the inductor ripple current. The input peak current can be obtained by adding the maximum input current with half of the inductor ripple current as shown in the following equation:

IRIPPLE = 0.2 x IIN(MAX)

Note that the saturated current of inductor must be greater than IPEAK. The inductance can eventually be determined according to the following equation:



where fOSC is the switching frequency. For better system performance, a shielded inductor is preferred to avoid EMI problems.

AVDD Boost Diode Selection

The Schottky diode is a good choice for any asynchronous boost converter due to the small forward voltage. However, when selecting a Schottky diode, important parameters such as power dissipation, reverse voltage rating, and pulsating peak current must all be taken into consideration. A suitable Schottky diode's reverse voltage rating must be greater than the maximum output voltage, and its average current rating must exceed the average output current.

AVDD Boost Output Capacitor Selection

Output ripple voltage is an important index for estimating the performance. This portion consists of two parts, one is the product of IIN and ESR of output capacitor, another part is formed by charging and discharging process of output capacitor. As shown in Figure 5, VOUT1 can be evaluated based on the ideal energy equalization. According to the definition of Q, the Q value can be calculated as following equation:



where fOSC is the switching frequency and IL is the inductor ripple current. Move COUT to left side to estimate the value of VOUT1 as following equation:



Where D is the duty cycle and η is the boost converter efficiency. Finally, taking ESR into account, the overall output ripple voltage can be determined by the following equation:





Figure 6. The Output Ripple Voltage without the Contribution of ESR.

AVDD Loop Compensation

The voltage feedback loop can be compensated with an external compensation network consisting of RCOMP and CCOMP. Choose RCOMP to set high frequency integrator gain for fast transient response and CCOMP to set the integrator zero to maintain stability.

VDD Buck Converter

The synchronous Buck converter is a high efficiency PWM architecture with 500kHz to 750kHz operation frequency and fast transient response. The converter needs external high-side and low-side N-MOSFET as synchronous rectifier and does not require Schottky diode on the LXB pin. The high-side MOSFET is connected between the VIN and LXB pins, while the low-side MOSFET is connected between the LXB pin and PGND.

VDD Buck Overcurrent Protection

The CS601C senses the inductor current that flows out of the LXB pin. The internal MOSFET will be turned off if the peak inductor current reaches 1A (min.).

VDD Buck Short-Circuit Protection

To limit the short-circuit current, the device has a cycle- by-cycle current limit function. When the short-circuit occurs, the output current will be limited, and the output voltage decreases. The MOSFET will be turned off when the output voltage is below 60% of nominal voltage. If the short is removed, the Buck converter will resume operation. If the output voltage remains below 60% nominal voltage for 10s, the IC will shut down.

Buck Inductor Selection

The inductor value and operating frequency determine the ripple current according to a specific input and output voltage. The ripple current, ΔIL, will increase with higher VIN and decrease with higher inductance, as shown in the following equation:



Having a lower ripple current reduces not only the ESR losses in the output capacitors but also the output voltage ripple. High frequency with small ripple current can achieve the highest efficiency operation. However, it requires a large inductor to achieve this goal. For the ripple current selection, IL(MAX) = 0.4A is a reasonable starting point. The largest ripple current occurs at the highest VIN. To guarantee that the ripple current stays below the specified maximum, the inductor value should be chosen according to the following equation :



Buck Input Capacitor Selection

The input capacitance, CIN, is needed to filter the trapezoidal current at the Source of the high-side MOSFET. To prevent large ripple current, a low ESR input capacitor sized for the maximum RMS current should be used. The RMS current is given by:



This formula has a maximum at VIN = 2VOUT, where IRMS = IOUT/2. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. For the input capacitor, a 10F low ESR ceramic capacitor is recommended.

Buck Output Capacitor Selection

The selection of COUT is determined by the required ESR to minimize voltage ripple. Moreover, the amount of bulk capacitance is also a key for COUT selection to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response as described in a later section. The output ripple, VOUT, is determined by:



The output ripple will be highest at the maximum input voltage since IL increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirement. Suitable candidates such as dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Special polymer capacitors offer very low ESR value. However, it provides lower capacitance density than other types. Although tantalum capacitors have the highest capacitance density, it is important to only use types that pass the surge test for switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR. However, it can be used in cost-sensitive applications requiring high ripple current rating and long term reliability. Ceramic capacitors have excellent low ESR characteristics but have a high voltage coefficient and audible piezoelectric effects. The high Q of ceramic capacitors with trace inductance can also lead to significant ringing. Nevertheless, higher value, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at input and output. When a ceramic capacitor is used at the input, VIN, and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at VIN large enough to damage the part.

VGL Negative Charge Pump Regulator

The VGL negative charge pump regulator provides low level voltage to the level shifter. The linear regulator can provide a programmable output voltage. During normal operation, the CS601C is able to provide up to 4mA (typ.) of the base current and is designed to work best with transistors of which DC gain (hfe) is between 100 and 300.

VGL Charge Pump Regulator Fault Protection

The VGL negative charge pump regulator has a fault protection. This function can disable the VGL negative charge pump controller if the VGL voltage is below 80%. If the VGL voltage remains below 80% for 3ms, the IC will shut down.

VSS Negative OP Amplifier Fault Protection

The VSS negative OP amplifier has a fault protection. This function can disable the VSS negative regulator if the VSS voltage is below 80%. If the VSS voltage remains below 80% for 3ms, the IC will shut down.

VGH Charge Pump Regulator Fault Protection

The VGH positive charge pump controller has a fault protection. This function can disable the VGH positive charge pump controller if the VGH voltage is below 80%. If the VGH voltage remains below 80% for 3ms, the IC will shut down.

During normal operation, the CS601-C0Y is able to provide up to 4mA (typ.) of the base current and is designed to work best with transistors of which DC gain (hfe) is between 100 and 300.

Undervoltage Lockout (UVLO)

The UVLO circuit compares the input voltage at VIN with the UVLO threshold to ensure the input voltage is high enough for reliable operation. Once the VIN exceeds the UVLO rising threshold, the device then starts to download, the start-up begins when programming finished. When VIN falls below the UVLO falling threshold, the IC turns off all IC internal functions, and the UVLO signal will be latched at low level after VIN falls below the UVLO falling threshold.

Level Shifter

The CS601C provides 12-Channel level shifter designed to drive panel. This IC converts the logic-level signals generated by Timing Controller (T- CON) to high-level signals required by panel. At the output of level shifter, VGH is the high voltage level for STVOUT, CLKOUTx, LC1/LC2 and DCHG. VGL is the low voltage level for STVOUT, CLKOUTx and LC1/LC2. VSS is the low voltage level for DCHG. VIN is seemed as the Dis\_charge signal. Table 2.1 is the Power On condition list and Table 2.2 is the Power Off condition. The level shifter input signal CLK\_ON and CLK\_OFF can create different patterns which can be selected by I2C setting. The Level shifter employs an OCP protection function and detailed operation is shown in the protection table.

L/S OCP Blanking Frame

L/S OCP blanking frame can be set with register 0Dh/3Dh[7:4]:

1. Only CLKOUTx OCP will be affected by blanking frame.
2. STVOUT OCP will be effective after 130ms blanking time.
3. LC1/2 OCP will be effective after VGH>VGH\_UVLO.
4. If OCP blanking frame was set to 0 frame, after 130ms of L/S output blanking time, the OCP detecting process will start at the rising edge of the 1st STV pulse.



Figure 7-(a). OCP blanking frame = 0 frame

1. If OCP blanking frame was set to 4 frame, after 130ms of L/S output blanking time, the OCP detecting process will start at the rising edge of the 4th STV pulse.



Figure 7-(b). OCP blanking frame = 4 frame

Level Shift OCP Function

1. STV and CLKOUT output OCP:

OCP fault will be high when L/S CLKOUT OCP cycle is counting to set value continuously. And both high-side and low-side in 1 channel OC are added up together to count cycle times in one frame.

1. LC1/2 and DCHG OCP:

C x VREF / I1 = 160s

DCHG, LC1 and LC2 OCP function are enabledin 130ms blanking time.



Figure 8-(a) STVOUT High-side OCP Occurred.



Figure 8-(b) STVOUT Low-side OCP Occurred.



Figure 9-(a) LC1/2 High-side OCP Occurred.



Figure 9-(b) LC1/2 Low-side OCP Occurred.



Figure 10 DCHG Low-side OCP Occurred.



Figure 11-(a) CLKOUT OCP Occurred for High-side



Figure 11-(b) CLKOUT OCP Occurred for Low-side



Figure 11-(c) CLKOUT Abnormal OCP Occurred for High-side.

Table 3.1 LS OCP Setting

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Level Shifter  Output Channel | MOS Type | OCP Start Point | OCP Frame Blanking  (frame) 0Dh/3Dh[7:4]  (1step = 2 frames) | OCP DELAY (s)  0Ch/3Ch[3:1]  (1step = 2s) | Detect Time (us) Fixed | OCP\_CLK\_Cycle  (frame) 0Dh/3Dh[3:0]  (1step = 4 times) |
| CLKOUT 1 to 8 | UG | After 130ms  Blanking Time | 0 to 30 | 2 to 16 | 1.8 | 4 to 64 |
| LG |
| STVOUT | UG | After 130ms  Blanking Time |  | 2 to 16 | 1.8 | 1 (Fixed) |
| LG | 160 |
| LC1/LC2 | UG | In the 130ms  Blanking Time |  | 2 to 16 | 160 | 1 (Fixed) |
| LG |
| DCHG | UG | After the 130ms  Blanking Time |  | 2 to 16 | 160 | 1 (Fixed) |
| LG |

Table 3.2 LS OCP Detection Behavior

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Channel** | **OCP Start** | **OCP Stop** | **OCP Disable** | **OCP Status Released** |
| CLKOUT 1 to 8 | UVLO\_VDD\_R &  UVLO\_VGH\_R &  DIS,TH\_R &  After 130ms Blanking Time | UVLO\_VDD\_F or  UVLO\_VGH\_F or  DIS,TH\_F | 0Ch/3Ch[0] = 0 | UVLO\_VIN\_F |
| STVOUT | UVLO\_VDD\_R &  UVLO\_VGH\_R &  DIS,TH\_R &  After 130ms Blanking Time | UVLO\_VDD\_F or  UVLO\_VGH\_F or  DIS,TH\_F | 0Ch/3Ch[0] = 0 | UVLO\_VIN\_F |
| LC1/LC2 | UVLO\_VDD\_R &  UVLO\_VGH\_R &  DIS,TH\_R | UVLO\_VDD\_F or  UVLO\_VGH\_F or  DIS,TH\_F | 0Ch/3Ch[0] = 0 | UVLO\_VIN\_F |
| DCHG | UVLO\_VDD\_R &  UVLO\_VGH\_R &  DIS,TH\_R &  After 130ms Blanking Time | UVLO\_VDD\_F or  UVLO\_VGH\_F or  DIS,TH\_F | 0Ch/3Ch[0] = 0 | UVLO\_VIN\_F |

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature TJ(MAX), listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

PD(MAX) = (TJ(MAX)  TA)/JA

where TJ(MAX) is the maximum junction temperature, TA is the ambient temperature, and JA is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-  
ambient thermal resistance, JA, is highly package dependent. For a VQFN-72L 8x8 package, the thermal resistance, JA, is 24.9°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at TA = 25°C can be calculated as below:

PD(MAX) = (125°C  25°C)/(24.9°C/W) = 4.01W for a VQFN-72L 8x8 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed TJ(MAX) and the thermal resistance, JA. The derating curves in Figure 11 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.



Figure 12. Derating Curve of Maximum Power Dissipation

Layout Consideration

PCB layout is very important for designing power switching converter circuits. For best performance of the CS601C, the following layout guidelines must be followed:

* For good regulation, place the power components as close as possible. The traces should be wider and shorter especially for the high current output loop.
* The output sense voltage must be near the sense pin. The sense voltage pin trace must be short and avoid the trace near any switching nodes.
* Minimize the size of the LX node and keep it wide and shorter. Keep the LX node away from the analog ground.
* The power ground (PGND) consists of input and output capacitor grounds.
* Separate power ground (PGND) and analog ground (AGND). Connect the AGND and the PGND islands at a single end. Make sure that there are no other connections between these separate ground planes. Connect the exposed pad to a strong ground plane for maximum thermal dissipation.

Layout Considerations



Figure 13. PCB Layout Guide for VGH Charge Pump + VGL Charge Pump x 2

|  |  |  |
| --- | --- | --- |
|  |  |  |
|  |  |  |
|  |  |  |

Figure 14. LS Output Timing for Phase and Line

Protection Table

| **Channel** | **Protection** | **Criteria** | **Behavior** | **Recovery** |
| --- | --- | --- | --- | --- |
| IC | OTP | IC Case Temp .> 150°C | IC Shutdown | Release < VIN\_UVLO |
| VDD | OCP | ILXB > 1A (min) | Normal operating:  Cycle by cycle Current limit | Inductor Current Peak<OCP |
| UVP | VDD < 80% | Count 3ms, IC shutdown and latch VDD, VGL, VSS, AVDD, GMA, VCOM, VGH, LS | Release < VIN\_UVLO |
| SCP | VDD < 60% | Count 10s, VDD LXB Stop Switching immediately, and then IC shutdown and latch VDD, VGL, VSS, AVDD, GMA, VCOM, VGH, LS | Release < VIN\_UVLO |
| OVP | VDD > 120% | VDD UG Stop Switching | VDD < OVP\_HYS |
| AVDD | OCP | ILXA > 2A (min), I2C Setting:2~3.5A | Normal operating:  Cycle by cycle Current limit | Inductor Current Peak < OCP |
| UVP | SWO < 80% | Count 3ms, IC shutdown and latch  AVDD,GMA,VCOM,VGH,LS | Release < VIN\_UVLO |
| SCP | SWO < 60% | Count 10s, SW Stop Switching immediately, and then IC shutdown and latch AVDD, GMA, VCOM, VGH,LS | Release < VIN\_UVLO |
| OVP | SWI > 21.5V | 1. SW Stop Switching  2. OVP number of times is detected to be exceed 10 times for longer than 20ms then shut down an latch AVDD, GMA, VCOM, VGH, LS. The function can be disable by 03h/33h[5] | < OVP\_HYS  Release<VIN\_UVLO |
| VSS | UVP | VSS < 80% | Count 3ms then shut down and latch VGL, VSS, AVDD, GMA, VCOM, VGH, LS. | Release < VIN\_UVLO |
| SCP | VSS < 60% | Count 10s then shut down and latch VGL, VSS, AVDD, GMA, VCOM, VGH, LS. | Release < VIN\_UVLO |
| VGL | UVP | VGL < 80% | Count 3ms, IC shutdown and latch  VGL, VSS, AVDD, GMA, VCOM, VGH, LS | Release<VIN\_UVLO |
| SCP | VGL < 60% | Count 10s then IC shutdown and latch.  VGL, VSS, AVDD, GMA, VCOM, VGH, LS | Release<VIN\_UVLO |
| VGH | UVP | VGH < 80% | Count 3ms, IC shutdown and latch  AVDD, GMA, VCOM, VGH, LS | Release < VIN\_UVLO |
| SCP | VGH < 60% | Count 10s then IC shutdown and latch  AVDD, GMA, VCOM, VGH, LS | Release < VIN\_UVLO |
| VCOM  1/2 | OCP | I\_VCOM overcurrent limit (source and sink) | Normal operating:  Current limit. | I\_VCOM<Current limit |
| G1~G14 | OCP | I\_Gamma overcurrent limit (source and sink) | Normal operating:  Current limit. | I\_Gamma<Current limit |
| L/S | OCP | I2C Setting  10~160mA | 1. CLKOUT1~8 High side or Low side MOS is triggered four times continuously and independently, all Channels will be Hi-Z. (Cycle times can be setting by I2C from 4~64cycle) 2. STVOUT/ DCHG/ LC1/ LC2 High side or Low side MOS is triggered one times continuously and independently, all Channels will be Hi-Z and then FLT go high.  Shutdown and latch AVDD, GMA, VCOM, VGH, LS | Release < VIN\_UVLO |

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Channel** | **Protections** | **VDD** | **VGL** | **VSS** | **GD** | **AVDD** | **VCOM 1/2** | **GMA** | **VGH** | **Level Shifter** |
| **VDD** | OCP | Duty Limit | N | N | N | N | N | N | N | N |
| SCP | X | X | X | X | X | X | X | X | X |
| UVP | X | X | X | X | X | X | X | X | X |
| OVP | SB | N | N | N | N | N | N | N | N |
| **VGL** | SCP | N | X | X | X | X | X | X | X | X |
| UVP | N | X | X | X | X | X | X | X | X |
| **VSS** | SCP | N | X | X | X | X | X | X | X | X |
| UVP | N | X | X | X | X | X | X | X | X |
| **AVDD** | OVP (Not switching) | N | N | N | N | SB | N | N | N | N |
| OVP (Latch) | N | N | N | X | X | X | X | X | X |
| OCP | N | N | N | N | Duty Limit | N | N | N | N |
| SCP | N | N | N | X | X | X | X | X | X |
| UVP | N | N | N | X | X | X | X | X | X |
| **VCOM**  **1/2** | OCP | N | N | N | N | N | Current Limit | N | N | N |
| SCP | N | N | N | N | N | Current Limit | N | N | N |
| **G1~G14** | OCP | N | N | N | N | N | N | Current Limit | N | N |
| **VGH** | UVP | N | N | N | X | X | X | X | X | X |
| SCP | N | N | N | X | X | X | X | X | X |
| **Level Shift** | OCP | N | N | N | X | X | X | X | X | X |
| **IC** | Thermal Shutdown | X | X | X | X | X | X | X | X | X |

**Note.** N: Normal work, X: Channel shut down, SB: Channel off and stand by.

I2C Command

Slave Address

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Bit 7** | **Bit 6** | **Bit 5** | **Bit 4** | **Bit 3** | **Bit 2** | **Bit 1** | **Bit 0 = LSB** |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | **R/** |

Write Command

(a) Write single byte of data to Register



(b) Write multiple bytes of data to Registers



Read Command

(a) Read single byte of data from Register



(b) Read multiple bytes of data from Registers

Register Map

| **Address** | **Name** | **Bit 7** | **Bit 6** | **Bit 5** | **Bit 4** | **Bit 3** | **Bit 2** | **Bit 1** | **Bit 0** |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| BankA | | | | | | | | | |
| 00h | Control Register | SEL\_5V/12V | X | EN\_VGH | EN\_AVDD | EN\_Control | EN\_VSS | EN\_VGL | EN\_VDD |
| 01h | Timing Control | X | AVDD\_SS | DLY2[5:4] | | DLY1[3:2] | | DLY0[1:0] | |
| 02h | AVDD&LS  discharge function | EN\_LS\_DIS | SW\_Freq | AVDD[5:0] | | | | | |
| 03h | VDD | X | X | AVDD OVP | VDD[4:0] | | | | |
| 04h | VSS | X | X | X | VSS[4:0] | | | | |
| 05h | X | X | X | X | X | | | | |
| 06h | VGL | X | X | X | VGL[4:0] | | | | |
| 07h | X | X | X | X | X | | | | |
| 08h | VGH | X | X | X | VGH[4:0] | | | | |
| 09h | OPLDO | X | X | X | OPLDO[4:0] | | | | |
| 0Ah | PMIC OCP | AVDD\_OC[7:6] | | DRVN[5:3] | | | DRVP[2:0] | | |
| 0Bh | LS Function | LS\_DIS[7:4] | | | | PHASE[3:2] | | LINE[1:0] | |
| 0Ch | LS OCP | OCP\_Level[7:4] | | | | OCP\_DELAY[3:1] | | | LS OCP Enable |
| 0Dh | LS OCP | OCP Frame Blanking[7:4] | | | | OCP CLK Cycle Number[3:0] | | | |
| 0Eh | G1 | X | X | X | X | X | X | G1[9:8] | |
| 0Fh | G1[7:0] | | | | | | | |
| 10h | G2 | X | X | X | X | X | X | G2[9:8] | |
| 11h | G2[7:0] | | | | | | | |
| 12h | G3 | X | X | X | X | X | X | G3[9:8] | |
| 13h | G3[7:0] | | | | | | | |
| 14h | G4 | X | X | X | X | X | X | G4[9:8] | |
| 15h | G4[7:0] | | | | | | | |
| 16h | G5 | X | X | X | X | X | X | G5[9:8] | |
| 17h | G5[7:0] | | | | | | | |
| 18h | G6 | X | X | X | X | X | X | G6[9:8] | |
| 19h | G6[7:0] | | | | | | | |
| 1Ah | G7 | X | X | X | X | X | X | G7[9:8] | |
| 1Bh | G7[7:0] | | | | | | | |
| 1Ch | G8 | X | X | X | X | X | X | G8[9:8] | |
| 1Dh | G8[7:0] | | | | | | | |
| 1Eh | G9 | X | X | X | X | X | X | G9[9:8] | |
| 1Fh | G9[7:0] | | | | | | | |
| 20h | G10 | X | X | X | X | X | X | G10[9:8] | |
| 21h | G10[7:0] | | | | | | | |
| 22h | G11 | X | X | X | X | X | X | G11[9:8] | |
| 23h | G11[7:0] | | | | | | | |
| 24h | G12 | X | X | X | X | X | X | G12[9:8] | |
| 25h | G12[7:0] | | | | | | | |
| 26h | G13 | X | X | X | X | X | X | G13[9:8] | |
| 27h | G13[7:0] | | | | | | | |
| 28h | G14 | X | X | X | X | X | X | G14[9:8] | |
| 29h | G14[7:0] | | | | | | | |
| 2Ah | VCOM1 | X | X | X | X | X | X | X | VCOM1[8] |
| 2Bh | VCOM1[7:0] | | | | | | | |
| 2Ch | VCOM2 | X | X | X | X | X | X | X | VCOM2[8] |
| 2Dh | VCOM2[7:0] | | | | | | | |
| 2Eh | CRC | Received CRC[17:10] | | | | | | | |
| 2Fh | CRC | Received CRC[7:0] | | | | | | | |
| BankB | | | | | | | | | |
| 30h | Control Register | SEL\_5V/12V | X | EN\_VGH | EN\_AVDD | EN\_Control | EN\_VSS | EN\_VGL | EN\_VDD |
| 31h | Timing Control | X | AVDD\_SS | DLY2[5:4] | | DLY1[3:2] | | DLY0[1:0] | |
| 32h | AVDD&LS  discharge function | EN\_LS\_DIS | SW\_Freq | AVDD[5:0] | | | | | |
| 33h | VDD | X | X | AVDD OVP | VDD[4:0] | | | | |
| 34h | VSS | X | X | X | VSS[4:0] | | | | |
| 35h | X | X | X | X | X | | | | |
| 36h | VGL | X | X | X | VGL[4:0] | | | | |
| 37h | X | X | X | X | X | | | | |
| 38h | VGH | X | X | X | VGH[4:0] | | | | |
| 39h | OPLDO | X | X | X | OPLDO[4:0] | | | | |
| 3Ah | PMIC OCP | AVDD\_OC[7:6] | | DRVN[5:3] | | | DRVP[2:0] | | |
| 3Bh | LS Function | LS\_DIS[7:4] | | | | PHASE[3:2] | | LINE[1:0] | |
| 3Ch | LS OCP | OCP\_Level[7:4] | | | | OCP\_DELAY[3:1] | | | LS OCP Enable |
| 3Dh | LS OCP | OCP Frame Blanking[7:4] | | | | OCP CLK Cycle Number[3:0] | | | |
| 3Eh | G1 | X | X | X | X | X | X | G1[9:8] | |
| 3Fh | G1[7:0] | | | | | | | |
| 40h | G2 | X | X | X | X | X | X | G2[9:8] | |
| 41h | G2[7:0] | | | | | | | |
| 42h | G3 | X | X | X | X | X | X | G3[9:8] | |
| 43h | G3[7:0] | | | | | | | |
| 44h | G4 | X | X | X | X | X | X | G4[9:8] | |
| 45h | G4[7:0] | | | | | | | |
| 46h | G5 | X | X | X | X | X | X | G5[9:8] | |
| 47h | G5[7:0] | | | | | | | |
| 48h | G6 | X | X | X | X | X | X | G6[9:8] | |
| 49h | G6[7:0] | | | | | | | |
| 4Ah | G7 | X | X | X | X | X | X | G7[9:8] | |
| 4Bh | G7[7:0] | | | | | | | |
| 4Ch | G8 | X | X | X | X | X | X | G8[9:8] | |
| 4Dh | G8[7:0] | | | | | | | |
| 4Eh | G9 | X | X | X | X | X | X | G9[9:8] | |
| 4Fh | G9[7:0] | | | | | | | |
| 50h | G10 | X | X | X | X | X | X | G10[9:8] | |
| 51h | G10[7:0] | | | | | | | |
| 52h | G11 | X | X | X | X | X | X | G11[9:8] | |
| 53h | G11[7:0] | | | | | | | |
| 54h | G12 | X | X | X | X | X | X | G12[9:8] | |
| 55h | G12[7:0] | | | | | | | |
| 56h | G13 | X | X | X | X | X | X | G13[9:8] | |
| 57h | G13[7:0] | | | | | | | |
| 58h | G14 | X | X | X | X | X | X | G14[9:8] | |
| 59h | G14[7:0] | | | | | | | |
| 5Ah | VCOM1 | X | X | X | X | X | X | X | VCOM1[8] |
| 5Bh | VCOM1[7:0] | | | | | | | |
| 5Ch | VCOM2 | X | X | X | X | X | X | X | VCOM2[8] |
| 5Dh | VCOM2[7:0] | | | | | | | |
| 5Eh | CRC | Received CRC[17:10] | | | | | | | |
| 5Fh | CRC | Received CRC[7:0] | | | | | | | |
| 60h | Status Register1 | CRC00 | VALID\_A | CRC12 | KEY5 | CRC05 | KEY1 | CRC14 | VALID\_B |
| 61h | Status Register2 | KEY4 | BANK | CRC06 | KEY2 | CRC02 | X | CRC10 | CRC16 |
| 62h | Status Register3 | CRC13 | VGL\_PG | CRC01 | KEY0 | CRC07 | KEY7 | VGH\_PG | CRC03 |
| 63h | Status Register4 | AVDD\_PG | X | CRC11 | CRC17 | KEY3 | CRC04 | CRC15 | KEY6 |
| 64h | Status Register5 | MODE | X | X | X | X | X | X | X |

**Note 7.** Writing 0 when writing X bit

Register Define

| **Address** | **Name** | **Description** | | **Default Value** | | **Resolution** | **Range** | |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 00h/30h | Control Register | [7] | SEL\_5V/12V | 0 | 01h | N/A | 0: VIN = 12V | 1: VIN = 5V |
| [5] | EN\_VGH | 0 | N/A | 0: VGH disable | 1: VGH enable |
| [4] | EN\_AVDD | 0 | N/A | 0: AVDD disable | 1: AVDD enable |
| [3] | EN\_Control | 0 | N/A | 0:VDD, still works, VGL,VSS, AVDD, HAVDD, VGH, all OP are off 1: VGL,VSS, AVDD, OP, VGH start power on by sequence after (EN pin& En\_Control register & DLY0 = 1) goes from low to high | |
| [2] | EN\_VSS | 0 | N/A | 0: VSS disable | 1: VSS enable |
| [1] | EN\_VGL | 0 | N/A | 0: VGL disable | 1: VGL enable |
| [0] | EN\_VDD | 1 | N/A | 0: VDD disable | 1: VDD enable |
| 01h/31h | Timing Control | [6] | AVDD SS | 10ms | 11h | 10ms | 0:10ms | 1:20ms |
| [5:4] | DLY2 | 3ms | 3ms | 0ms to 9ms | (00h to 03h) |
| [3:2] | DLY1 | 10ms | 5ms | 10ms to 25ms | (00h to 03h) |
| [1:0] | DLY0 | 9ms | 3ms | 6ms to 15ms | (00h to 03h) |
| 02h/32h | AVDD& LS discharge function | [7] | EN\_LS\_DIS | 1 | DFh | NA | 0: Hi-Z | 1: Discharge |
| [6] | SW\_Freq | 1 | N/A | 0: 500kHz | 1: 750Khz |
| [5:0] | AVDD | 16V | 0.1V | 13V to 19.2V | (00h to 3Fh) |
| 03h/33h | VDD | [5] | AVDD\_OVP | 1 | 36h | N/A | 0: Disable AVDD OVP 10T in 20ms | 1: Enable AVDD OVP 10T in 20ms |
| [4:0] | VDD | 3.3V | 0.05V | 2.2V to 3.7V | (00h to 1Eh) |
| 04h/34h | VSS | [4:0] | VSS | -8V | 07h | 0.5V | -4.5V to -16V | (00h to 17h) |
| 06h/36h | VGL | [4:0] | VGL | -10V | 0Bh | 0.5V | -4.5V to -20V | (00h to 1Fh) |
| 08h/38h | VGH | [4:0] | VGH | 30V | 0Ah | 1V | 20V to 40V | (00h to 14h) |
| 09h/39h | OPLDO | [4:0] | OPLDO | 15.4V | 0Ch | 0.2V | 13V to 18V | (00h to 19h) |
| 0Ah/3Ah | PMIC OCP | [7:6] | AVDD\_OC | 2A | 1Bh | 0.5A | 2A to 3.5A | (00h to 03h) |
| [5:3] | DRVN | 4mA | 1mA | 1mA to 8mA | (00h to 07h) |
| [2:0] | DRVP | 4mA | 1mA | 1mA to 8mA | (00h to 07h) |
| 0Bh/3Bh | LS Function | [7:4] | LS\_DIS | 8V (4V) | 44h | 0.5V (0.25V) | SEL\_5V/12V = 0, 6V to 10V  (SEL\_5V/12V = 1, 3V to 5V) | (00h to 0Fh) |
| [3:2] | PHASE | 6Phase | N/A | 4Phase to 8Phase | (00h to 02h) |
| [1:0] | LINE | 1 line | N/A | 1 line to 4 line | (00h to 02h) |
| 0Ch/3Ch | LS OCP | [7:4] | OCP\_Level | 100mA | 91h | 10mA | 10mA to 160mA | (00h to 0Fh) |
| [3:1] | OCP\_DELAY | 2s | 2s | 2s to 16s | (00h to 07h) |
| [0] | LS OCP Enable | 1 | N/A | 0: LS OCP Disable | 1: LS OCP Enable |
| 0Dh/3Dh | LS OCP | [7:4] | OCP Delay frame | 2 Frame | 10h | 2 Frame | OCP detection function can set by frame. 0 to 30 Frame | (00h to 0Fh) |
| [3:0] | OCP CLK Cycle | 4 Cycle | 4 Cycle | OCP trigger times can set by Cycle. 4 to 64 Cycle | (00h to 0Fh) |
| 0Eh/3Eh | GAMMA1 | [9:0] | G1 | 14.14V | 03h | Res:OPLDO/1024 | 0 to 1023\*Res | (000h to 3FFh) |
| 0Fh/3Fh | ACh |
| 10h/40h | GAMMA2 | [9:0] | G2 | 13.66V | 03h | Res:OPLDO/1024 | 0 to 1023\*Res | (000h to 3FFh) |
| 11h/41h | 8Ch |
| 12h/42h | GAMMA3 | [9:0] | G3 | 11.05V | 02h | Res:OPLDO/1024 | 0 to 1023\*Res | (000h to 3FFh) |
| 13h/43h | DFh |
| 14h/44h | GAMMA4 | [9:0] | G4 | 9.98V | 02h | Res:OPLDO/1024 | 0 to 1023\*Res | (000h to 3FFh) |
| 15h/45h | 98h |
| 16h/46h | GAMMA5 | [9:0] | G5 | 9.45V | 02h | Res:OPLDO/1024 | 0 to 1023\*Res | (000h to 3FFh) |
| 17h/47h | 74h |
| 18h/48h | GAMMA6 | [9:0] | G6 | 7.77V | 02h | Res:OPLDO/1024 | 0 to 1023\*Res | (000h to 3FFh) |
| 19h/49h | 05h |
| 1Ah/4Ah | GAMMA7 | [9:0] | G7 | 7.77V | 02h | Res:OPLDO/1024 | 0 to 1023\*Res | (000h to 3FFh) |
| 1Bh/4Bh | 05h |
| 1Ch/4Ch | GAMMA8 | [9:0] | G8 | 7.36V | 01h | Res:OPLDO/1024 | 0 to 1023\*Res | (000h to 3FFh) |
| 1Dh/4Dh | E9h |
| 1Eh/4Eh | GAMMA9 | [9:0] | G9 | 7.34V | 01h | Res:OPLDO/1024 | 0 to 1023\*Res | (000h to 3FFh) |
| 1Fh/4Fh | E8h |
| 20h/50h | GAMMA10 | [9:0] | G10 | 4.25V | 01h | Res:OPLDO/1024 | 0 to 1023\*Res | (000h to 3FFh) |
| 21h/51h | 1Bh |
| 22h/52h | GAMMA11 | [9:0] | G11 | 3.44V | 00h | Res:OPLDO/1024 | 0 to 1023\*Res | (000h to 3FFh) |
| 23h/53h | E5h |
| 24h/54h | GAMMA12 | [9:0] | G12 | 2.15V | 00h | Res:OPLDO/1024 | 0 to 1023\*Res | (000h to 3FFh) |
| 25h/55h | 8Fh |
| 26h/56h | GAMMA13 | [9:0] | G13 | 0.34V | 00h | Res:OPLDO/1024 | 0 to 1023\*Res | (000h to 3FFh) |
| 27h/57h | 17h |
| 28h/58h | GAMMA14 | [9:0] | G14 | 0.2V | 00h | Res:OPLDO/1024 | 0 to 1023\*Res | (000h to 3FFh) |
| 29h/59h | 0Dh |
| 2Ah/5Ah | VCOM1 | [8:0] | VCOM1 | 7V | 00h | Res:OPLDO/1024 | 250\*Res to 640\*Res | (000h to 186h) |
| 2Bh/5Bh | D8h |
| 2Ch/5Ch | VCOM2 | [8:0] | VCOM2 | 7V | 00h | Res:OPLDO/1024 | 250\*Res to 640\*Res | (000h to 186h) |
| 2Dh/5Dh | D8h |
| 2Eh/5Eh | CRC | [17:10] | CRC |  |  |  |  |  |
| 2Fh/5Fh | CRC | [7:0] | CRC |  |  |  |  |  |
| 60h | Status Register1 | [7] | CRC00 | 0 | 00h | N/A | PMIC calculated CRC code bit 0 | |
| [6] | VALID\_A | 0 | BANK A data Validate 0: BANK A data is invalidate 1: BANK A data is validate | |
| [5] | CRC12 | 0 | PMIC calculated CRC code bit 12 | |
| [4] | KEY5 | 0 | KEY\_ID bit 5, KEY5 is always “0” | |
| [3] | CRC05 | 0 | PMIC calculated CRC code bit 5 | |
| [2] | KEY1 | 0 | KEY\_ID bit 1, KEY 1 is always “0” | |
| [1] | CRC14 | 0 | PMIC calculated CRC code bit 14 | |
| [0] | VALID\_B | 0 | BANK B data Validate 0: BANK B data is invalidate 1: BANK B data is validate | |
| 61h | Status Register2 | [7] | KEY4 | 1 | 90h | N/A | KEY\_ID bit 4. KEY4 is always “1” | |
| [6] | BANK | 0 | BANK bit follow Bank\_Sel pin state | |
| [5] | CRC06 | 0 | PMIC calculated CRC code bit 6 | |
| [4] | KEY2 | 1 | KEY\_ID bit 2. KEY2 is always “1” | |
| [3] | CRC02 | 0 | PMIC calculated CRC code bit 2 | |
| [2] | Reserved | 0 | Reserved | |
| [1] | CRC10 | 0 | PMIC calculated CRC code bit 10 | |
| [0] | CRC16 | 0 | PMIC calculated CRC code bit 16 | |
| 62h | Status Register3 | [7] | CRC13 | 0 | 10h | N/A | PMIC calculated CRC code bit 13 | |
| [6] | VGL\_PG | 0 | 1:VGL<80% VGL setting | |
| [5] | CRC01 | 0 | PMIC calculated CRC code bit 1 | |
| [4] | KEY0 | 1 | KEY\_ID bit 0. KEY0 is always“1” | |
| [3] | CRC07 | 0 | PMIC calculated CRC code bit 7 | |
| [2] | KEY7 | 0 | KEY\_ID bit 7. KEY7 is always “0” | |
| [1] | VGH\_PG | 0 | 1:VGH>80% VGH setting | |
| [0] | CRC03 | 0 | PMIC calculated CRC code bit 3 | |
| 63h | Status Register4 | [7] | AVDD\_PG | 0 | 09h | N/A | 1:AVDD>80% AVDD setting | |
| [6] | Reserved | 0 | Reserved | |
| [5] | CRC11 | 0 | PMIC calculated CRC code bit 11 | |
| [4] | CRC17 | 0 | PMIC calculated CRC code bit 17 | |
| [3] | KEY3 | 1 | KEY\_ID bit 3. KEY3 is always “1” | |
| [2] | CRC04 | 0 | PMIC calculated CRC code bit 4 | |
| [1] | CRC15 | 0 | PMIC calculated CRC code bit 15 | |
| [0] | KEY6 | 1 | KEY\_ID bit 6. KEY6 is always “1” | |
| 64h | Status Register5 | [7] | Mode | 0 | 00h | N/A | VSA data transmission mode control 0: Normal mode. CRC is enabled 1: Test mode. CRC is disabled | |
| [6] | Reserved | 0 | Reserved | |
| [5] | Reserved | 0 | Reserved | |
| [4] | Reserved | 0 | Reserved | |
| [3] | Reserved | 0 | Reserved | |
| [2] | Reserved | 0 | Reserved | |
| [1] | Reserved | 0 | Reserved | |
| [0] | Reserved | 0 | Reserved | |

Output Table (unit: V)

| **Register Code** | **AVDD(V)** | **VDD**  **(V)** | **VGH**  **(V)** | **VSS**  **(V)** | **VGL**  **(V)** | **AVDD**  **OCP**  **(A)** | **DLY0**  **(ms)** | **DLY1**  **(ms)** | **DLY2**  **(ms)** | **AVDD\_**  **SS**  **(ms)** | **OPLDO**  **(V)** |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 00h | 13 | 2.2 | 20 | -4.5 | -4.5 | 2 | 6 | 10 | 0 | 10 | 13 |
| 01h | 13 | 2.25 | 21 | -5 | -5 | 2.5 | 9 | 15 | 3 | 20 | 13.2 |
| 02h | 13.1 | 2.3 | 22 | -5.5 | -5.5 | 3 | 12 | 20 | 6 |  | 13.4 |
| 03h | 13.2 | 2.35 | 23 | -6 | -6 | 3.5 | 15 | 25 | 9 |  | 13.6 |
| 04h | 13.3 | 2.4 | 24 | -6.5 | -6.5 |  |  |  |  |  | 13.8 |
| 05h | 13.4 | 2.45 | 25 | -7 | -7 |  |  |  |  |  | 14.0 |
| 06h | 13.5 | 2.5 | 26 | -7.5 | -7.5 |  |  |  |  |  | 14.2 |
| 07h | 13.6 | 2.55 | 27 | -8 | -8 |  |  |  |  |  | 14.4 |
| 08h | 13.7 | 2.6 | 28 | -8.5 | -8.5 |  |  |  |  |  | 14.6 |
| 09h | 13.8 | 2.65 | 29 | -9 | -9 |  |  |  |  |  | 14.8 |
| 0Ah | 13.9 | 2.7 | 30 | -9.5 | -9.5 |  |  |  |  |  | 15.0 |
| 0Bh | 14.0 | 2.75 | 31 | -10 | -10 |  |  |  |  |  | 15.2 |
| 0Ch | 14.1 | 2.8 | 32 | -10.5 | -10.5 |  |  |  |  |  | 15.4 |
| 0Dh | 14.2 | 2.85 | 33 | -11 | -11 |  |  |  |  |  | 15.6 |
| 0Eh | 14.3 | 2.9 | 34 | -11.5 | -11.5 |  |  |  |  |  | 15.8 |
| 0Fh | 14.4 | 2.95 | 35 | -12 | -12 |  |  |  |  |  | 16.0 |
| 10h | 14.5 | 3 | 36 | -12.5 | -12.5 |  |  |  |  |  | 16.2 |
| 11h | 14.6 | 3.05 | 37 | -13 | -13 |  |  |  |  |  | 16.4 |
| 12h | 14.7 | 3.1 | 38 | -13.5 | -13.5 |  |  |  |  |  | 16.6 |
| 13h | 14.8 | 3.15 | 39 | -14 | -14 |  |  |  |  |  | 16.8 |
| 14h | 14.9 | 3.2 | 40 | -14.5 | -14.5 |  |  |  |  |  | 17.0 |
| 15h | 15.0 | 3.25 |  | -15 | -15 |  |  |  |  |  | 17.2 |
| 16h | 15.1 | 3.3 |  | -15.5 | -15.5 |  |  |  |  |  | 17.4 |
| 17h | 15.2 | 3.35 |  | -16 | -16 |  |  |  |  |  | 17.6 |
| 18h | 15.3 | 3.4 |  |  | -16.5 |  |  |  |  |  | 17.8 |
| 19h | 15.4 | 3.45 |  |  | -17 |  |  |  |  |  | 18.0 |
| 1Ah | 15.5 | 3.5 |  |  | -17.5 |  |  |  |  |  |  |
| 1Bh | 15.6 | 3.55 |  |  | -18 |  |  |  |  |  |  |
| 1Ch | 15.7 | 3.6 |  |  | -18.5 |  |  |  |  |  |  |
| 1Dh | 15.8 | 3.65 |  |  | -19 |  |  |  |  |  |  |
| 1Eh | 15.9 | 3.7 |  |  | -19.5 |  |  |  |  |  |  |
| 1Fh | 16.0 |  |  |  | -20 |  |  |  |  |  |  |
| 20h | 16.1 |  |  |  |  |  |  |  |  |  |  |
| 21h | 16.2 |  |  |  |  |  |  |  |  |  |  |
| 22h | 16.3 |  |  |  |  |  |  |  |  |  |  |
| 23h | 16.4 |  |  |  |  |  |  |  |  |  |  |
| 24h | 16.5 |  |  |  |  |  |  |  |  |  |  |
| 25h | 16.6 |  |  |  |  |  |  |  |  |  |  |
| 26h | 16.7 |  |  |  |  |  |  |  |  |  |  |
| 27h | 16.8 |  |  |  |  |  |  |  |  |  |  |
| 28h | 16.9 |  |  |  |  |  |  |  |  |  |  |
| 29h | 17.0 |  |  |  |  |  |  |  |  |  |  |
| 2Ah | 17.1 |  |  |  |  |  |  |  |  |  |  |
| 2Bh | 17.2 |  |  |  |  |  |  |  |  |  |  |
| 2Ch | 17.3 |  |  |  |  |  |  |  |  |  |  |
| 2Dh | 17.4 |  |  |  |  |  |  |  |  |  |  |
| 2Eh | 17.5 |  |  |  |  |  |  |  |  |  |  |
| 2Fh | 17.6 |  |  |  |  |  |  |  |  |  |  |
| 30h | 17.7 |  |  |  |  |  |  |  |  |  |  |
| 31h | 17.8 |  |  |  |  |  |  |  |  |  |  |
| 32h | 17.9 |  |  |  |  |  |  |  |  |  |  |
| 33h | 18.0 |  |  |  |  |  |  |  |  |  |  |
| 34h | 18.1 |  |  |  |  |  |  |  |  |  |  |
| 35h | 18.2 |  |  |  |  |  |  |  |  |  |  |
| 36h | 18.3 |  |  |  |  |  |  |  |  |  |  |
| 37h | 18.4 |  |  |  |  |  |  |  |  |  |  |
| 38h | 18.5 |  |  |  |  |  |  |  |  |  |  |
| 39h | 18.6 |  |  |  |  |  |  |  |  |  |  |
| 3Ah | 18.7 |  |  |  |  |  |  |  |  |  |  |
| 3Bh | 18.8 |  |  |  |  |  |  |  |  |  |  |
| 3Ch | 18.9 |  |  |  |  |  |  |  |  |  |  |
| 3Dh | 19.0 |  |  |  |  |  |  |  |  |  |  |
| 3Eh | 19.1 |  |  |  |  |  |  |  |  |  |  |
| 3Fh | 19.2 |  |  |  |  |  |  |  |  |  |  |

| **Register Code** | **DRVN**  **(mA)** | **DRVP**  **(mA)** | **LS\_DIS (V)** | | **CLKOUT**  **Phase** | **LS OCP\_Level**  **(mA)** | **LS OCP\_Delay**  **(us)** | **LS OCP Frame Blanking** | **CLK OCP Cycle** | **CLK**  **Line** |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **SEL\_**  **5V/12V = 0** | **SEL\_**  **5V/12V = 1** |
| 00h | 1 | 1 | 6 | 3 | 4 | 10 | 2 | 0 | 4 | 1 |
| 01h | 2 | 2 | 6.5 | 3.25 | 6 | 20 | 4 | 2 | 8 | 2 |
| 02h | 3 | 3 | 7 | 3.5 | 8 | 30 | 6 | 4 | 12 | 4 |
| 03h | 4 | 4 | 7.5 | 3.75 | 8 | 40 | 8 | 6 | 16 | 4 |
| 04h | 5 | 5 | 8 | 4 |  | 50 | 10 | 8 | 20 |  |
| 05h | 6 | 6 | 8.5 | 4.25 |  | 60 | 12 | 10 | 24 |  |
| 06h | 7 | 7 | 9 | 4.5 |  | 70 | 14 | 12 | 28 |  |
| 07h | 8 | 8 | 9.5 | 4.75 |  | 80 | 16 | 14 | 32 |  |
| 08h |  |  | 10 | 5 |  | 90 |  | 16 | 36 |  |
| 09h |  |  | 10 | 5 |  | 100 |  | 18 | 40 |  |
| 0Ah |  |  | 10 | 5 |  | 110 |  | 20 | 44 |  |
| 0Bh |  |  | 10 | 5 |  | 120 |  | 22 | 48 |  |
| 0Ch |  |  | 10 | 5 |  | 130 |  | 24 | 52 |  |
| 0Dh |  |  | 10 | 5 |  | 140 |  | 26 | 56 |  |
| 0Eh |  |  | 10 | 5 |  | 150 |  | 28 | 60 |  |
| 0Fh |  |  | 10 | 5 |  | 160 |  | 30 | 64 |  |

VCOM Output Table, RES = OPLDO/1024 (unit: V)

|  |  |
| --- | --- |
| **Register Code** | **VCOM**  **Register** |
| 000h | RES\*250 |
| 001h | RES\*251 |
| 002h | RES\*252 |
| 003h | RES\*253 |
| 004h | RES\*254 |
| 005h | RES\*255 |
| 006h | RES\*256 |
| 007h | RES\*257 |
| 008h | RES\*258 |
| 009h | RES\*259 |
| 00Ah | RES\*260 |
| 00Bh | RES\*261 |
| 00Ch | RES\*262 |
| 00Dh | RES\*263 |
| 00Eh | RES\*264 |
| 00Fh | RES\*265 |

……

|  |  |
| --- | --- |
| 037h | RES\*305 |
| 038h | RES\*306 |
| 039h | RES\*307 |
| 03Ah | RES\*308 |
| 03Bh | RES\*309 |
| 03Ch | RES\*310 |
| 03Dh | RES\*311 |
| 03Eh | RES\*312 |
| 03Fh | RES\*313 |
| 040h | RES\*314 |
| 041h | RES\*315 |
| 042h | RES\*316 |

……

|  |  |
| --- | --- |
| 109h | RES\*515 |
| 10Ah | RES\*516 |
| 10Bh | RES\*517 |
| 10Ch | RES\*518 |
| 10Dh | RES\*519 |
| 10Eh | RES\*520 |
| 10Fh | RES\*521 |
| 110h | RES\*522 |
| 111h | RES\*523 |
| 112h | RES\*524 |
| 113h | RES\*525 |
| 114h | RES\*526 |

……

|  |  |
| --- | --- |
| 180h | RES\*634 |
| 181h | RES\*635 |
| 182h | RES\*636 |
| 183h | RES\*637 |
| 184h | RES\*638 |
| 185h | RES\*639 |
| 186h | RES\*640 |
| 187h | x |
| 188h | x |
| 189h | x |
| 18Ah | x |
| 18Bh | x |

……

|  |  |
| --- | --- |
| 1F1h | x |
| 1F2h | x |
| 1F3h | x |
| 1F4h | x |
| 1F5h | x |
| 1F6h | x |
| 1F7h | x |
| 1F8h | x |
| 1F9h | x |
| 1FAh | x |
| 1FBh | x |
| 1FCh | x |
| 1FDh | x |
| 1FEh | x |
| 1FFh | x |

GAMMA Output Table, RES = OPLDO/1024 (unit: V)

|  |  |
| --- | --- |
| **Register Code** | **G1~G14** |
| 0000h | 0 |
| 0001h | RES\*1 |
| 0002h | RES\*2 |
| 0003h | RES\*3 |
| 0004h | RES\*4 |
| 0005h | RES\*5 |
| 0006h | RES\*6 |
| 0007h | RES\*7 |
| 0008h | RES\*8 |
| 0009h | RES\*9 |
| 000Ah | RES\*10 |
| 000Bh | RES\*11 |
| 000Ch | RES\*12 |
| 000Dh | RES\*13 |
| 000Eh | RES\*14 |
| 000Fh | RES\*15 |

**……**

|  |  |
| --- | --- |
| 0037h | RES\*55 |
| 0038h | RES\*56 |
| 0039h | RES\*57 |
| 003Ah | RES\*58 |
| 003Bh | RES\*59 |
| 003Ch | RES\*60 |
| 003Dh | RES\*61 |
| 003Eh | RES\*62 |
| 003Fh | RES\*63 |
| 0040h | RES\*64 |
| 0041h | RES\*65 |
| 0042h | RES\*66 |

**……**

|  |  |
| --- | --- |
| 0109h | RES\*265 |
| 010Ah | RES\*266 |
| 010Bh | RES\*267 |
| 010Ch | RES\*268 |
| 010Dh | RES\*269 |
| 010Eh | RES\*270 |
| 010Fh | RES\*271 |
| 0110h | RES\*272 |
| 0111h | RES\*273 |
| 0112h | RES\*274 |
| 0113h | RES\*275 |
| 0114h | RES\*276 |

**……**

|  |  |
| --- | --- |
| 0180h | RES\*384 |
| 0181h | RES\*385 |
| 0182h | RES\*386 |
| 0183h | RES\*387 |
| 0184h | RES\*388 |
| 0185h | RES\*389 |
| 0186h | RES\*390 |
| 0187h | RES\*391 |
| 0188h | RES\*392 |
| 0189h | RES\*393 |
| 018Ah | RES\*394 |
| 018Bh | RES\*395 |

……

|  |  |
| --- | --- |
| 01F1h | RES\*497 |
| 01F2h | RES\*498 |
| 01F3h | RES\*499 |
| 01F4h | RES\*500 |
| 01F5h | RES\*501 |
| 01F6h | RES\*502 |
| 01F7h | RES\*503 |
| 01F8h | RES\*504 |
| 01F9h | RES\*505 |
| 01FAh | RES\*506 |
| 01FBh | RES\*507 |
| 01FCh | RES\*508 |
| 01FDh | RES\*509 |
| 01FEh | RES\*510 |
| 01FFh | RES\*511 |

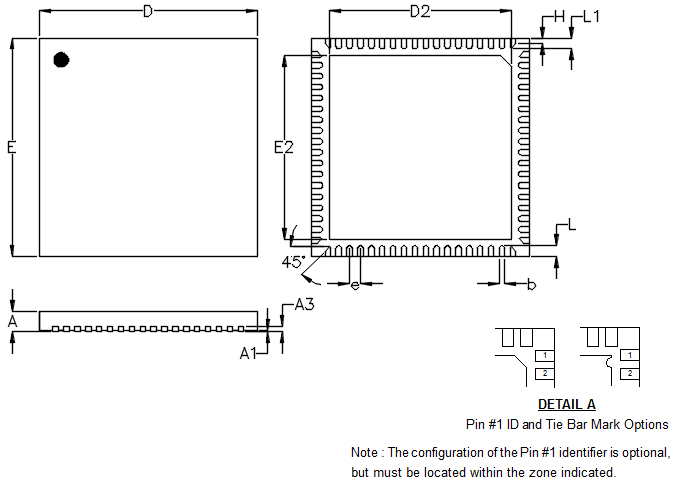
……

|  |  |
| --- | --- |
| 0258h | RES\*600 |
| 0259h | RES\*601 |
| 025Ah | RES\*602 |
| 025Bh | RES\*603 |
| 025Ch | RES\*604 |
| 025Dh | RES\*605 |
| 025Eh | RES\*606 |
| 025Fh | RES\*607 |
| 0260h | RES\*608 |
| 0261h | RES\*609 |
| 0262h | RES\*610 |
| 0263h | RES\*611 |
| 0264h | RES\*612 |
| 0265h | RES\*613 |
| 0266h | RES\*614 |

……

|  |  |
| --- | --- |
| 03F1h | RES\*1009 |
| 03F2h | RES\*1010 |
| 03F3h | RES\*1011 |
| 03F4h | RES\*1012 |
| 03F5h | RES\*1013 |
| 03F6h | RES\*1014 |
| 03F7h | RES\*1015 |
| 03F8h | RES\*1016 |
| 03F9h | RES\*1017 |
| 03FAh | RES\*1018 |
| 03FBh | RES\*1019 |
| 03FCh | RES\*1020 |
| 03FDh | RES\*1021 |
| 03FEh | RES\*1022 |
| 03FFh | RES\*1023 |

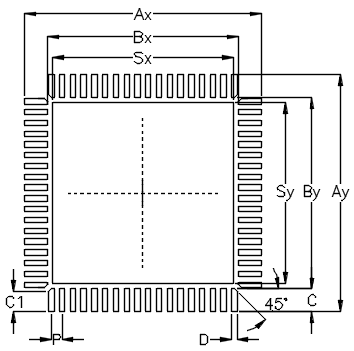
Outline Dimension



|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Symbol** | **Dimensions In Millimeters** | | **Dimensions In Inches** | |
| **Min** | **Max** | **Min** | **Max** |
| A | 0.800 | 1.000 | 0.031 | 0.039 |
| A1 | 0.000 | 0.050 | 0.000 | 0.002 |
| A3 | 0.175 | 0.250 | 0.007 | 0.010 |
| b | 0.150 | 0.250 | 0.006 | 0.010 |
| D | 7.900 | 8.100 | 0.311 | 0.319 |
| D2 | 6.650 | 6.750 | 0.262 | 0.266 |
| E | 7.900 | 8.100 | 0.311 | 0.319 |
| E2 | 6.650 | 6.750 | 0.262 | 0.266 |
| e | 0.400 | | 0.016 | |
| L | 0.350 | 0.450 | 0.014 | 0.018 |
| L1 | 0.320 | 0.420 | 0.013 | 0.017 |
| H | 0.150 | 0.250 | 0.006 | 0.010 |

**V-Type 72L QFN 8x8 Package**

Footprint Information



|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Package | Number of Pin | Footprint Dimension (mm) | | | | | | | | | | Tolerance |
| P | Ax | Ay | Bx | By | C\*72 | C1\*8 | D | Sx | Sy |
| V/W/U/XQFN8\*8-72 | 72 | 0.40 | 8.80 | 8.80 | 7.10 | 7.10 | 0.85 | 0.75 | 0.20 | 6.70 | 6.70 | ±0.05 |

Packing Information

Tape and Reel Data

**一張含有 寫生, 圖表, 工程製圖, 圖畫 的圖片

自動產生的描述 一張含有 圓形, 圖表, 寫生, 行 的圖片

自動產生的描述**

**一張含有 文字, 圖表, 行, 字型 的圖片

自動產生的描述**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Package Type | Tape Size (W1) (mm) | Pocket Pitch (P) (mm) | Reel Size (A) | | Units per Reel | Trailer (mm) | Leader(mm) | Reel Width (W2)  Min./Max. (mm) |
| (mm) | (in) |
| QFN/DFN 8x8 | 16 | 12 | 330 | 13 | 2,500 | 160 | 600 | 16.4/18.4 |

**一張含有 圖表, 行, 文字, 方案 的圖片

自動產生的描述**

**C, D and K are determined by component size. The clearance between the components and the cavity is as follows:**

**- For 16mm carrier tape: 1.0mm max.**

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Tape Size | W1 | P | | B | | F | | ØJ | | H |
| Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Max. |
| 16mm | 16.3mm | 11.9mm | 12.1mm | 1.65mm | 1.85mm | 3.9mm | 4.1mm | 1.5mm | 1.6mm | 0.6mm |

Tape and Reel Packing

|  |  |  |  |
| --- | --- | --- | --- |
| **Step** | **Photo/Description** | **Step** | **Photo/Description** |
| **1** | 一張含有 圓形, 扇子 的圖片  自動產生的描述 | **4** | 一張含有 文字, 包裝與標籤, 硬紙盒, 紙板 的圖片  自動產生的描述 |
| Reel 13” | 1 reel per inner box **Box G** |
| **2** | 一張含有 圓形, 符號, 文字, 標誌 的圖片  自動產生的描述 | **5** | 一張含有 Rectangle, 視窗, 容器, 箱子 的圖片  自動產生的描述 |
| HIC & Desiccant (2 Unit) inside | 6 inner boxes per outer box |
| **3** | 一張含有 文字, 扇子 的圖片  自動產生的描述  Caution label is on backside of Al bag | **6** | D:\Alice\DS\Packing\Pack-outerbox.jpg  Outer box **Carton A** |
| Caution label is on backside of Al bag | Outer box **Carton A** |

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Container  Package | Reel | | Box | | | | Carton | | |
| Size | Units | Item | Weight(kg) | Reels | Units | Item | Boxes | Units |
| QFN and DFN 8x8 | 13” | 2,500 | Box G | 1.11 | 1 | 2,500 | Carton A | 6 | 15,000 |

Packing Material Anti-ESD Property

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Surface Resistance | Aluminum Bag | Reel | Cover tape | Carrier tape | Tube | Protection Band |
| Ω/cm2 | **104 to 1011** | **104 to 1011** | **104 to 1011** | **104 to 1011** | **104 to 1011** | **104 to 1011** |

Richtek Technology Corporation

14F, No. 8, Tai Yuen 1st Street, Chupei City

Hsinchu, Taiwan, R.O.C.

Tel: (8863)5526789

Richtek products are sold by description only. Richtek reserves the right to change the circuitry and/or specifications without notice at any time. Customers should obtain the latest relevant information and data sheets before placing orders and should verify that such information is current and complete. Richtek cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Richtek product. Information furnished by Richtek is believed to be accurate and reliable. However, no responsibility is assumed by Richtek or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Richtek or its subsidiaries.

**Datasheet R**evisio**n History**

|  |  |  |  |
| --- | --- | --- | --- |
| **Version** | **Date** | **Description** | **Item** |
| P00 | 2023/7/11 | First Edition |  |