Oliver Cassidy

ollyj.cassidy@gmail.com | P: +44 7484 232315 | https://github.com/ollycassidy13 | https://olly-cassidy.vercel.app/ |
www.linkedin.com/in/oliver-cassidy-286ba3235

EDUCATION

Imperial College London London, UK
MEng in Electronic and Information Engineering Expected May 2027
Predicted First-Class Honours; Dean's List 2024; Ranked 2nd in the year
Relevant coursework: RISC-V CPU in SystemVerilog, C90 compiler, FPGA/AWS based duel game system, WiFi controlled rover

The Manchester Grammar School Manchester, UK
A Levels – Mathematics A*, Further Mathematics A*, Physics A*, Electronics A*; Winner of the Paton Electronics Prize Jun 2023

CONFERENCE PUBLICATIONS

ReducedLUT: Table Decomposition with "Don't Care" Conditions London, UK
Paper published in the ACM/SIGDA International Symposium on Field-Programmable Gate Arrays 2025 Aug 2024 – Present
- Lead-author of a paper focused on reducing the physical lookup table (P-LUT) utilisation of L-LUT based neural network (NN) models for ultra-low latency applications by introducing extra similarities within the data to allow for more effective decomposition
- Reduced the P-LUT utilisation by over 38% with a maximum test accuracy drop of 0.01%: https://doi.org/10.1145/3706628.3708823
- Presented the paper to leading academics at both FPGA 2025 and to the CAS research group at Imperial College London

PROFESSIONAL EXPERIENCE

Imperial College London Undergraduate Research Opportunity London, UK
Ultra-low Latency ML FPGA Research Jun 2024 – Sep 2024
- Investigated research papers such as NeuraLUT, LogicNets, CompressedLUT and Yukio Miyasaka's paper on BDD's gaining a concrete understanding of deep neural networks on FPGA devices, LUTs and how don't care conditions can be leveraged
- Modified CompressedLUT's code to be lossless in the context of NNs' train and test accuracy
- Adapted the toolflow of NeuraLUT to integrate CUDA for LUT based testing, Verilator testing of the Verilog model and synthesis of the model using Vivado by modifying oh-my-xilinx to perform a suitable synthesis allowing for multiple models to be evaluated in parallel
- Implemented a new toolflow to integrate the use of the lossless CompressedLUT, and then ReducedLUT to NeuraLUT models

Private 1:1 Tutoring Jan 2021-Sep 2024
- Used social media to market my own tutoring business and attract clients, leading to a full client roster and a waitlist
- Tutored over fifteen students at GCSE and A level in preparation for their examinations, leading to an increase in grades

RESEARCH EXPERIENCE

FPGA-Based Brain Simulation Mar 2025-Present
- Worked with a team from TU Delft to map gate activation and timestep functions to L-LUTs
- Applied multiple LUT decomposition techniques to reduce the LUT utilisation while still meeting strict timing requirements

ACADEMIC PROJECTS

CMATMUL – Cache Based Matrix Multiplication Kernel Feb 2025-Mar 2025
- Developed an effective C++ based matrix multiplication kernel leading to over a 100x increase in throughput from a naïve solution
- Optimised the throughput by implementing cache-aware tiling, register blocking, an AVX2 microkernel and OpenMP parallelism

Network Intrusion detection System Jul 2024
- Created FNN in PyTorch trained on the CIC-IDS2017 dataset, implemented on Pi Zero to deliver real-time alerts of network threats.

Collabify Mar 2024-Aug 2024
- Designed and created a website which introduced more collaboration to Spotify
- Used a release date weighted cosine similarity model in Python and the Spotify API to suggest new music personalised to the user
- Initialised and maintained a database using SQL to store account details and the users' liked songs to allow for a shared liked songs playlist

Remote Control Car from Logic Dec 2022-Mar 2023
- Designed and built a remote control car using a RF transmitter/receiver pair, logic gates, counters and motor drivers
- Built the RF unit using a crystal oscillator and filter to obtain the carrier wave, and ASK modulation to transmit the information

ADDITIONAL

Programming Proficiencies: Advanced in C++, Python, PyTorch, HTML/CSS, CUDA, Verilator, Git; Proficient in C, JavaScript, SQL, Java, Verilog, SystemVerilog, React, Electron, Basic, Assembly languages, Flask, Tcl
Awards: Dean's List (2024), Paton Electronics Prize (2023), Gold Crest Award, Gold Kangaroo in the Senior Maths Challenge, Silver in the Physics Olympiad and Silver Industrial Cadets Award (2022)
Interests: 5K competitive track running for The Thames Valley Harriers (2023-Present), Raced nationally for junior cycling development teams and trained weekly with British Cycling (2020-2023)