Oliver Cassidy

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EDUCATION

Imperial College London — London, UK
MEng in Electronic and Information Engineering — Expected May 2027
Predicted First-Class Honours; Dean's List 2024; Ranked 2nd in the year
Relevant coursework: RISC-V CPU in SystemVerilog, C compiler, FPGA/AWS based duel game system, WiFi controlled rover

The Manchester Grammar School — Manchester, UK
A Levels – Mathematics A*, Further Mathematics A*, Physics A*, Electronics A*; Winner of the Paton Electronics Prize — Jun 2023

CONFERENCE PUBLICATIONS

ReducedLUT: Table Decomposition with "Don't Care" Conditions — London, UK
Paper published to the ACM/SIGDA International Symposium on Field-Programmable Gate Arrays 2025 — Aug 2024 – Present

- Lead-author of a paper focused on reducing the physical lookup table (P-LUT) utilisation of L-LUT based neural network (NN) models for ultra-low latency applications by introducing extra similarities within the data to allow for more effective decomposition
- Reduced the P-LUT utilisation by over 38% with a maximum test accuracy drop of 0.01%: https://arxiv.org/abs/2412.18579
- Presented the paper to leading academics at both FPGA 2025 and to the CAS research group at Imperial College London

PROFESSIONAL EXPERIENCE

Imperial College London Undergraduate Research Opportunity — London, UK
Ultra-low Latency ML FPGA Research — Jun 2024 – Sep 2024

- Investigated research papers such as NeuraLUT, LogicNets, CompressedLUT and Yukio Miyasaka's paper on BDD's gaining a concrete understanding of deep neural networks on FPGA devices, LUTs and how don't care conditions can be leveraged
- Modified CompressedLUT's code to be lossless in the context of NNs' train and test accuracy
- Adapted the toolflow of NeuraLUT to integrate CUDA for LUT based testing, Verilator testing of the Verilog model and synthesis of the model using Vivado by modifying oh-my-xilinx to perform a suitable synthesis allowing for multiple models to be tested in parallel
- Implemented a new toolflow to integrate the use of the lossless CompressedLUT, and then ReducedLUT to NeuraLUT models

Private 1:1 Tutoring — Jan 2021-Sep 2024

- Used social media to market my own tutoring business and attract clients, leading to a full client roster and a waitlist
- Tutored over fifteen students at GCSE and A level in preparation for their examinations, leading to an increase in grades

Adelphi Automation — Stockport, UK
Robotics Placement — Jun 2022

- Obtained a 15x increase in rate of transfer of materials by programming a KUKA robotic arm
- Designed adapters to attach a suction cup and pump to the robotic arm using Solidworks before machining the parts by hand

ACADEMIC PROJECTS

CANNL – Cache Accelerated Neural Network Library — Feb 2025-Present

- Developing a C based library for neural networks which aims to reduce training time by 2.5x through effective matrix multiplication
- Optimized throughput by implementing cache-aware tiling, an AVX-512 microkernel and OpenMP parallelism
- I added support for dropout, multiple loss, activation and normalization functions, as well as example data augmentation techniques, learning rate scheduling and memory management from scratch to allow users to more effectively make use of the multiplication algorithm

Collabify — Mar 2024-Aug 2024

- Designed and created a website which introduced more collaboration to Spotify
- Used a release date weighted cosine similarity model in Python and the Spotify API to suggest new music personalised to the user
- Initialised and maintained a database using SQL to store account details and the users' liked songs to allow for a shared liked songs playlist

Remote Control Car from Logic — Dec 2022-Mar 2023

- Designed and built a remote control car using a RF transmitter/receiver pair, logic gates, counters and motor drivers
- Built the RF unit using a crystal oscillator and filter to obtain the carrier wave, and ASK modulation to transmit the information

ADDITIONAL

Programming Proficiencies: Advanced in C++, Python, PyTorch, HTML/CSS, CUDA, Verilator, Git; Proficient in C, JavaScript, SQL, Java, Verilog, SystemVerilog, React, Electron, Basic, Assembly languages, Flask, Tcl
Awards: Dean's List (2024), Paton Electronics Prize (2023), Gold Crest Award, Gold Kangaroo in the Senior Maths Challenge, Silver in the Physics Olympiad and Silver Industrial Cadets Award (2022)
Interests: 5K competitive track running for The Thames Valley Harriers (2023-Present), Raced nationally for junior cycling development teams and trained weekly with British Cycling (2020-2023)