Oliver Cassidy

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EDUCATION

Imperial College London — London, UK
MEng in Electronic and Information Engineering — Expected May 2027
Predicted First-Class Honours; Dean's List 2024; Ranked in the top 10 (5%) of the year

The Manchester Grammar School — Manchester, UK
A Levels – Mathematics A*, Further Mathematics A*, Physics A*, Electronics A*; Winner of the Paton Electronics Prize — Jun 2023

WORK EXPERIENCE

ReducedLUT: Table Decomposition with "don't care" conditions — London, UK
Submission for the ACM/SIGDA International Symposium on Field-Programmable Gate Arrays 2025 — Aug 2024 – Present

- First authored my paper on reducing the lookup table (LUT) utilisation of LUT based neural network (NN) models for ultra-low latency applications by introducing extra similarities within the data to allow for more effective decomposition
- Reduced the LUT count by over 38% with a maximum test accuracy drop of 0.01%
- Wrote code to implement 'don't care' conditions strategically within a LUT decomposition framework in C++
- Researched, developed a deep understanding of and later implemented code from Yukio Miyasaka's paper on binary decision diagrams (BDD) in synthesis using ABC to take comparable results for my paper
- Clearly conveyed my methodology and my results in a concise form to submit to FPGA 2025 Conference
- Currently investigating the generalisation of NN functions post training when introducing randomised values where 'don't cares' lie to form a mathematical basis for the use of exiguity and search for further applications of ReducedLUT's methodology

Imperial College London Undergraduate Research Opportunity — London, UK
Ultra-low Latency ML FPGA Research — Jun 2024 – Sep 2024

- Investigated research papers such as NeuraLUT, LogicNets, CompressedLUT and Yukio Miyasaka's paper on BDD's gaining a deep understanding of deep neural networks on FPGA devices, LUTs and how don't care conditions can be leveraged
- Modified CompressedLUT's code to be lossless in the context of NNs' train and test accuracy
- Adapted the toolflow of NeuraLUT to integrate CUDA for LUT based testing, Verilator testing of the Verilog model and synthesis of the model using Vivado by modifying oh-my-xilinx to perform a suitable synthesis allowing for multiple models to be tested in parallel
- Integrated neuron logging by performing inference on the model using the train dataset to record the used activations per neuron
- Implemented a new toolflow to integrate the use of the lossless CompressedLUT, and then ReducedLUT to the NeuraLUT models

Private 1:1 Tutoring — Jan 2021-Present

- Used social media to market my own tutoring business and attract clients, leading to a full client roster and a waitlist
- Tutored over fifteen students at GCSE and A level in preparation for their examinations, leading to an increase in grades

Adelphi Automation — Stockport, UK
Robotics Placement — Jun 2022

- Designed adapters to attach a suction cup and pump to a robotic arm using Solidworks
- Machined the parts by hand to match the designs, and fitted them to the robotic arm
- Programmed the a KUKA arm to automate the transfer of materials, leading to a 15x increase in the speed of the transfer

ACADEMIC PROJECTS

Collabify — Mar 2024 – Present

- Designed and created a website which helped bring people together over music by introducing more collaboration to Spotify
- Used a release date weighted cosine similarity model in Python and the Spotify API to suggest new music personalised to the user
- Initialised a database using SQL to store account details and the users' liked songs to allow for a shared liked songs playlist
- Implemented a frontend web design with animations using HTML, CSS and JavaScript (user-friendly, ergonomic)

Remote Control Car from Logic — Dec 2022-Mar 2023

- Designed and built a remote control car using a RF transmitter/receiver pair, logic gates, counters and motor drivers
- Built the RF unit using a crystal oscillator to generate the desired carrier frequency, and ASK modulation to transmit the information

ADDITIONAL

Programming Proficiencies: Advanced in C++, Python, PyTorch, JavaScript, HTML/CSS, CUDA, Verilator, Tcl; Proficient in C, SQL, Java, Verilog, React, Electron, Basic, Assembly languages, Flask
Awards: Dean's List (2024), Paton Electronics Prize (2023), Gold Crest Award, Gold Kangaroo in the Senior Maths Challenge, Silver in the Physics Olympiad and Silver Industrial Cadets Award (2022)