ECE 271

Digital Logic Design
Final Project

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Contents

List of Figures

1 Project Description

Intro to Project paragraph. The inputs and outputs of the overall design immediately follow. An overall description diagram is then shown in **Figure 1** and a hardware diagram is shown in **Figure 2**.

- **Inputs:** inputs
- **Outputs:** outputs

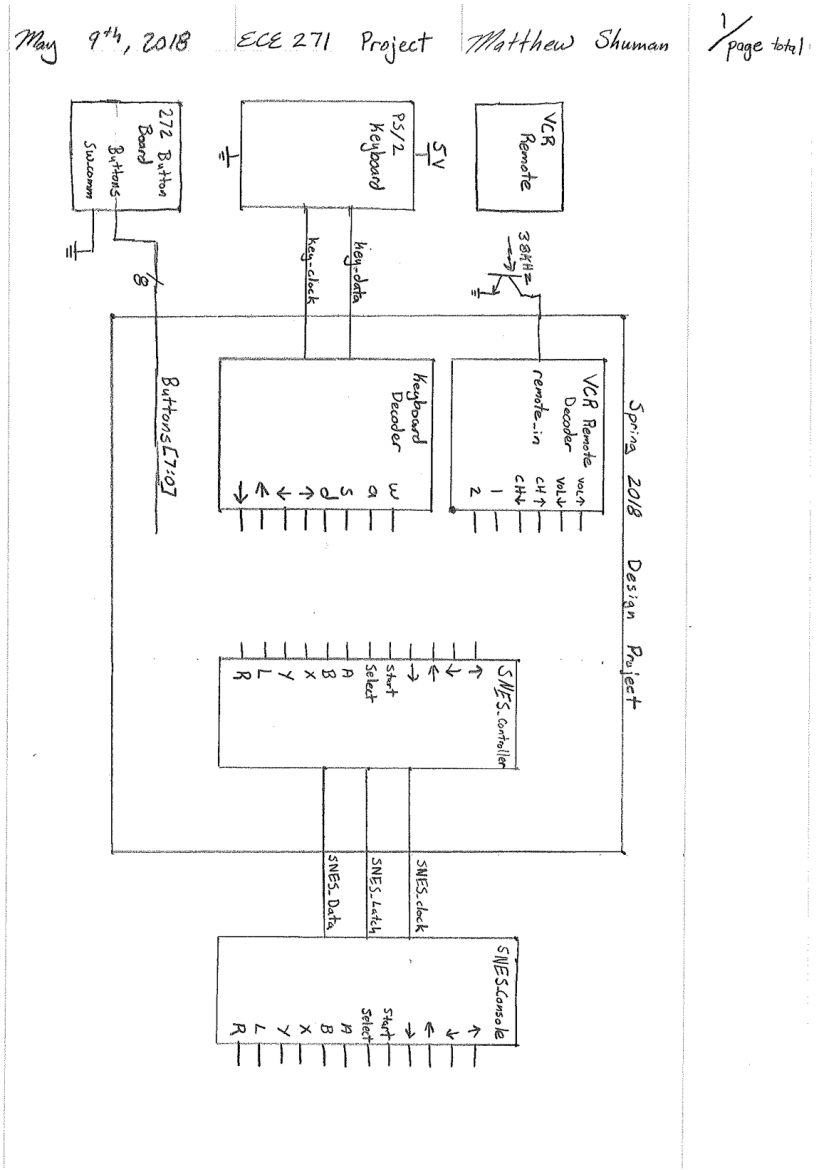


Figure 1: This image is legible, and conveys the point of the design. Your image can be hand drawn, but it must have straight lines, use your OSU ID. I don't recommend drafting this on the computer, because there aren't any decent tools to draw these block diagrams quickly.

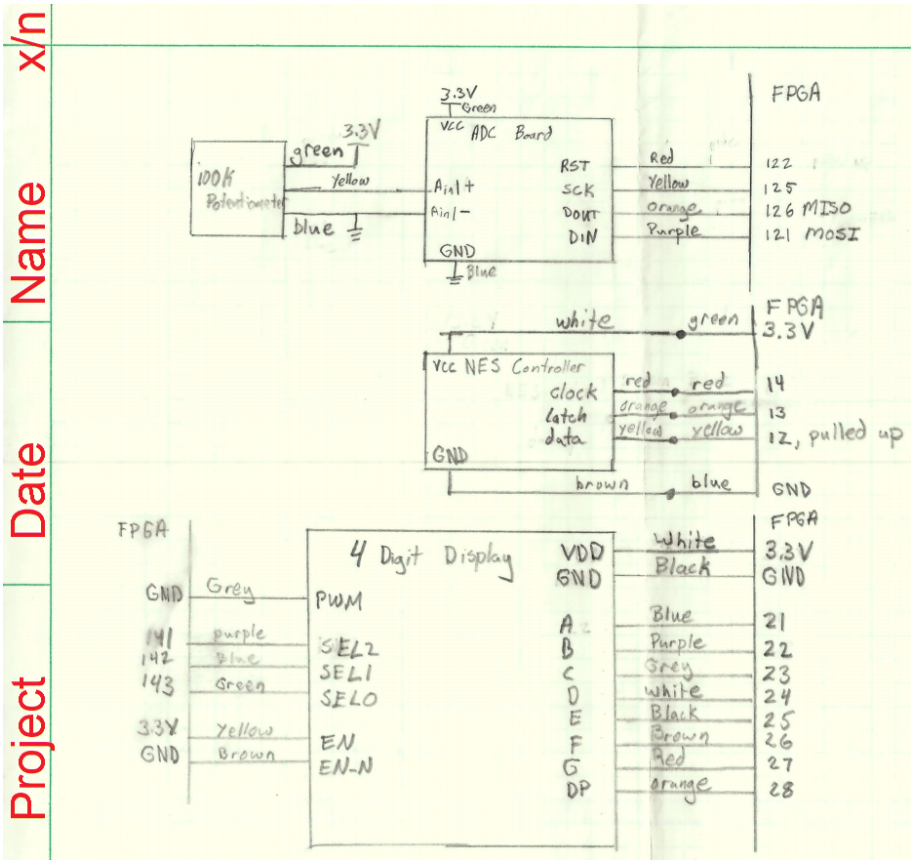


Figure 2: The hardware diagram shows which pins are used on the FPGA, module boards, and relevant supply voltages for the different pieces of hardware used in the system.

2 High Level Description

Top level introduction. The input and output specifications follow, a toplevel diagram follows in **Figure 3**, and the simulation results follow in **Figure 4**.

- **Inputs:** inputs
- **Outputs:** outputs

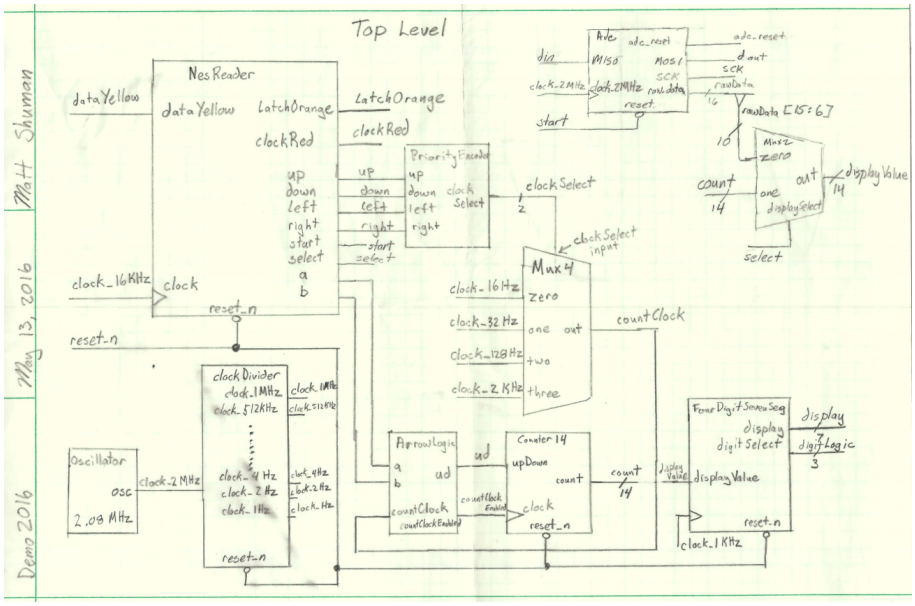


Figure 3: The top level design for the project. This would be improved by combining the priority encoder and Mux4 into a single clock select block. Combining the ArrowLogic and Counter14 would also make this diagram better. Use chapter 1 concepts wisely on this diagram, specifically hierarchy, modularity, regularity, and discipline.

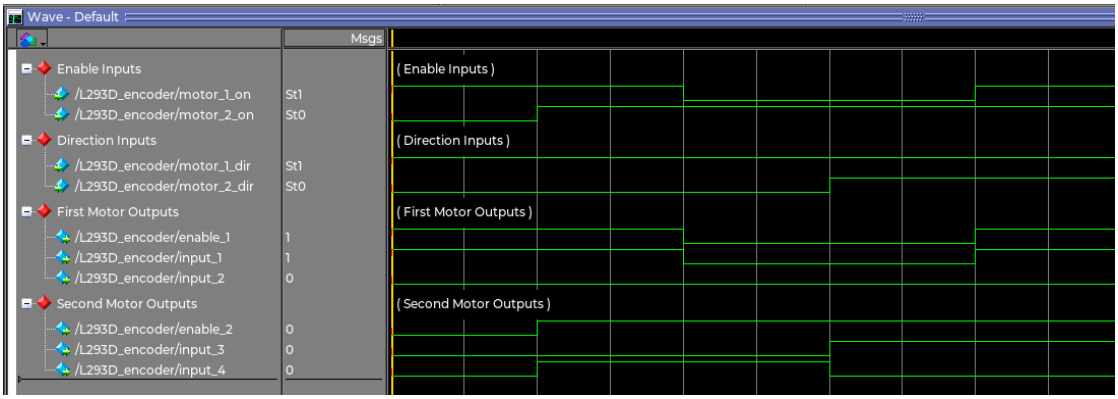


Figure 4: The simulation results of the top level design for the project.

The following subsections will discuss the inputs, outputs, designs, and simulation results of all elements of the design at two levels of scrutiny: functional units and individual blocks of digital logic.

2.1 Functional Unit 1 Name

Introduction to functional unit. The input and output specifications follow, a block diagram of the unit follows in **Figure A**, the simulation results for the unit follows in **Figure B**, and the details for each individual block comprising the unit follow after.

- **Inputs:** inputs
- **Outputs:** outputs

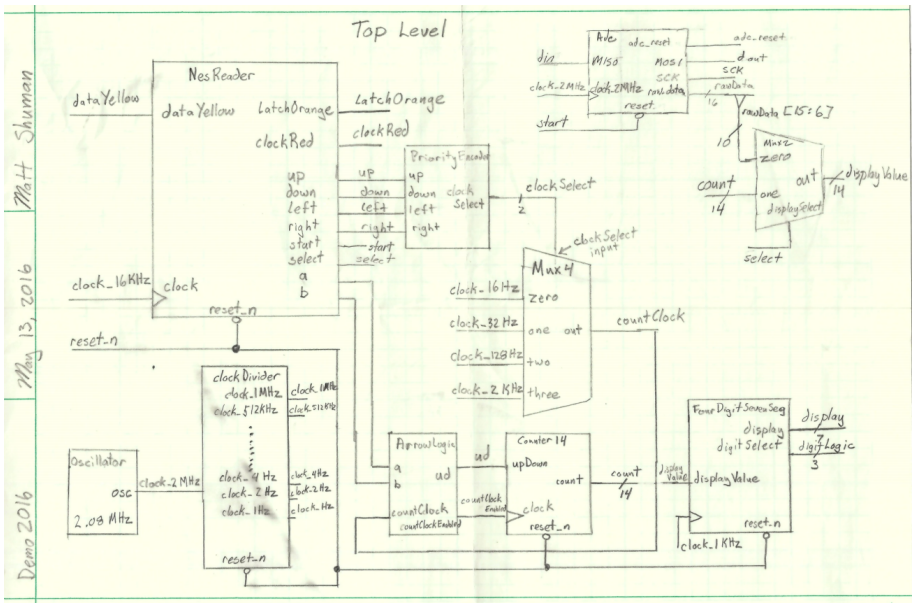


Figure 5: The logic design of the (NAME) functional unit used in the final design.

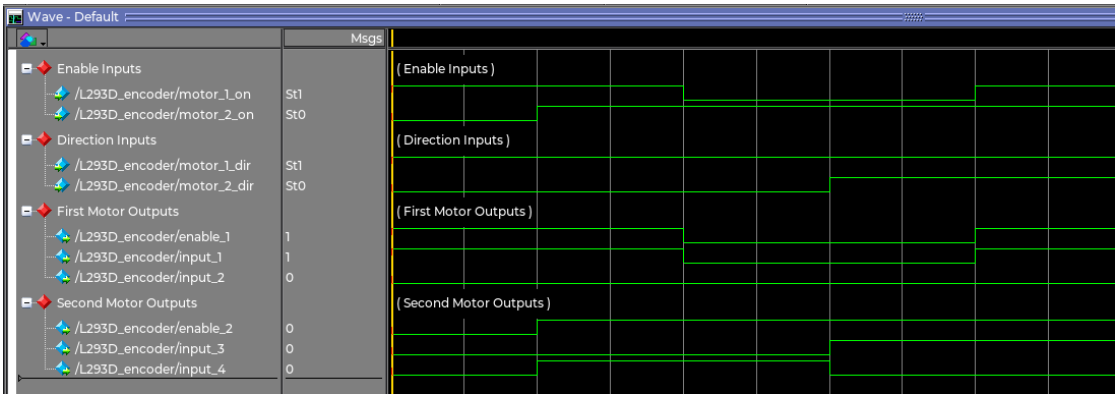
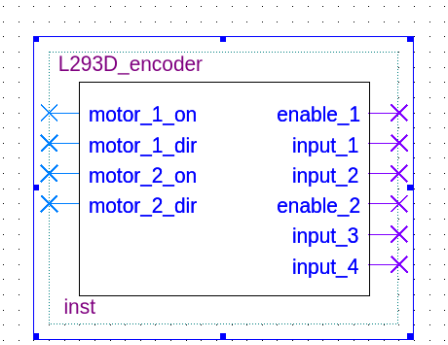


Figure 6: The simulation results of the top level design for the project.

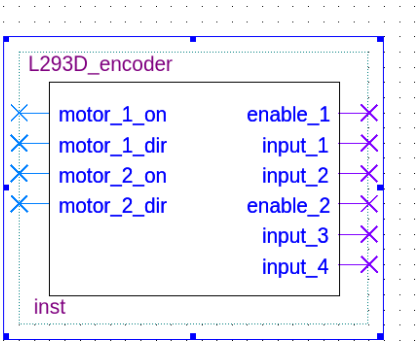
2.1.1 Individual Block 1 Name (with testbench)

Introduction to individual block. The input and output specifications follow, as well as the block diagram (**Figure C**), and simulation results **Figure D** for the individual block.

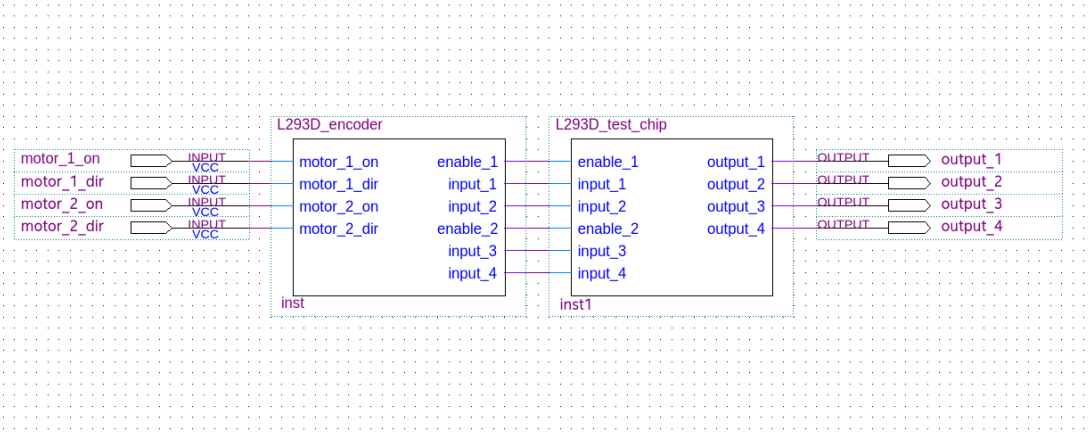
- **Inputs:** inputs
- **Outputs:** outputs



(a) The block symbol of the (NAME) individual block used in the (NAME) functional unit.

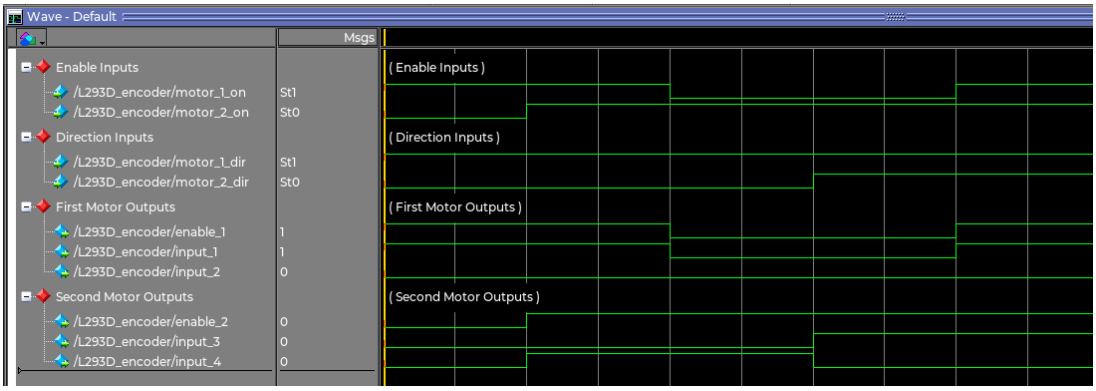


(b) The block symbol of the test block used in the testbench made to further simulate the (NAME) individual block.

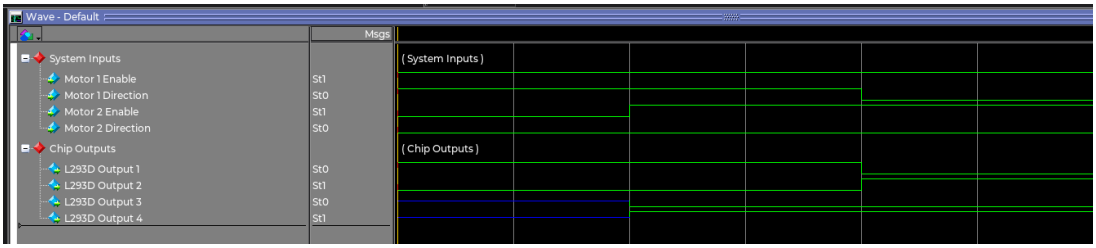


(c) The testbench used to further simulate the (NAME) individual block.

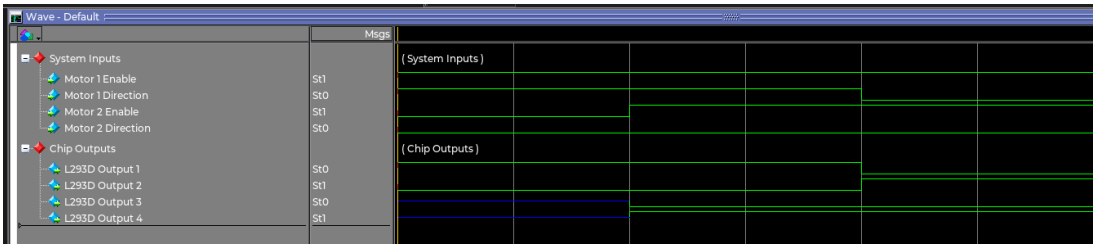
Figure 7: The block symbol of the (NAME) individual block used in the (NAME) functional unit, the block diagram of the logic of the testbench used to further simulate the block, and the block symbol of the test chip used in the testbench of the block.



(a) The simulation results for the (NAME) individual block alone.



(b) The simulation results of the test block used in the testbench.



(c) The simulation results of the testbench used.

Figure 8: The simulation results of the block alone, the testbench used to further simulate the block, and the simulation results for the testbebch of the (NAME) individual block used in the (NAME) functional unit.

2.1.2 Individual Block 2 Name (without testbench)

Introduction to individual block. The input and output specifications follow, as well as the block diagram (**Figure C**), and simulation results **Figure D** for the individual block.

- **Inputs:** inputs
- **Outputs:** outputs

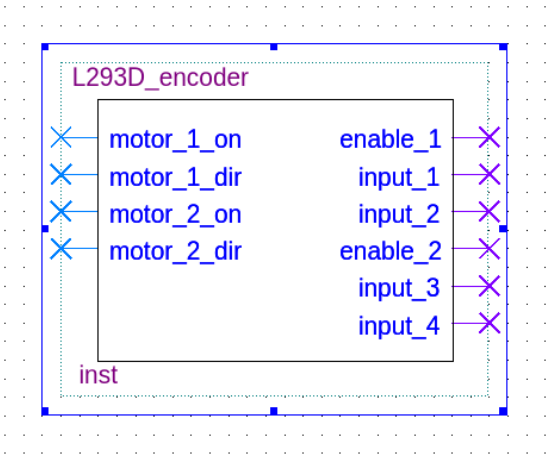


Figure 9: The block symbol of the (NAME) individual block used in the (NAME) functional unit.

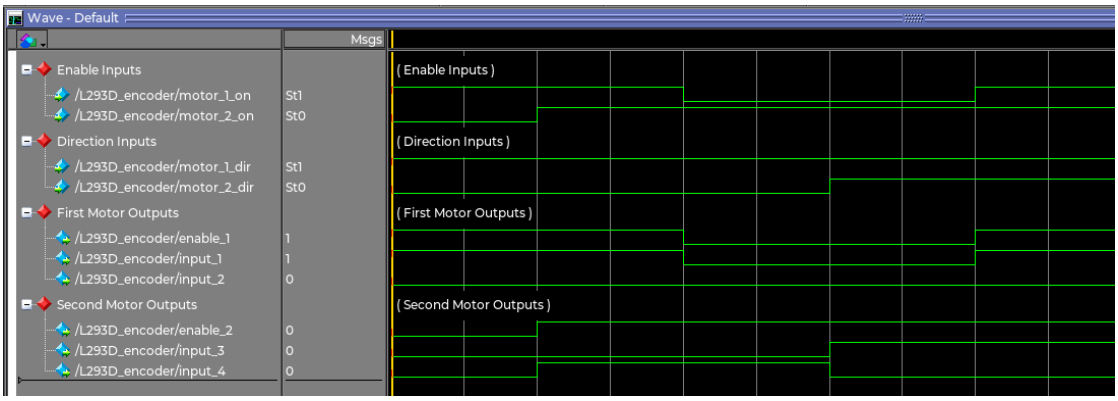


Figure 10: The simulation results of the (NAME) individual block used in the (NAME) functional unit.

A SystemVerilog Files

This appendix will list the SystemVerilog code used for each block used in the design project.

A.1 Functional Unit Name

```
1
2  // https://www.st.com/content/ccc/resource/technical/document/datasheet/04/ac/22/f9/20/5d/4
3
4  // Delay will have scale of 1ns per #n listed (resolution 100ps)
5  `timescale 1ns/100ps
6
7  module L293D_test_chip (
8     input logic     enable_1,    // pin 1     -  enable for inputs 1 and 2
9                     input_1,     // pin 2     -  input 1 (forward for motor 1)
10                    input_2,     // pin 7     -  input 2 (backward for motor 1)
11
12                    enable_2,    // pin 9     -  enable for inputs 3 and 4
13                    input_3,     // pin 10    -  input 3 (forward for motor 2)
14                    input_4,     // pin 15    -  input 4 (backward for motor 2)
15
16    output logic    output_1,    // pin 3     -  output 1 (forward for motor 1)
17                    output_2,    // pin 6     -  output 2 (backward for motor 2)
18
19                    output_3,    // pin 11    -  output 3 (forward for motor 3)
20                    output_4 // pin 14    -  output 4 (backward for motor 4)
21    );
22
23    always_comb begin
24
25       output_1 <= (enable_1) ? (input_1) : (1'bz);
26       output_2 <= (enable_1) ? (input_2) : (1'bz);
27
28       output_3 <= (enable_2) ? (input_3) : (1'bz);
29       output_4 <= (enable_2) ? (input_4) : (1'bz);
30    end
31
32 endmodule
```

(a) SystemVerilog code for the (NAME) block used in the design.

```
1
2  // https://www.st.com/content/ccc/resource/technical/document/datasheet/04/ac/22/f9/20/5d/4
3
4  // Delay will have scale of 1ns per #n listed (resolution 100ps)
5  `timescale 1ns/100ps
6
7  module L293D_test_chip (
8     input logic     enable_1,    // pin 1     -  enable for inputs 1 and 2
9                     input_1,     // pin 2     -  input 1 (forward for motor 1)
10                    input_2,     // pin 7     -  input 2 (backward for motor 1)
11
12                    enable_2,    // pin 9     -  enable for inputs 3 and 4
13                    input_3,     // pin 10    -  input 3 (forward for motor 2)
14                    input_4,     // pin 15    -  input 4 (backward for motor 2)
15
16    output logic    output_1,    // pin 3     -  output 1 (forward for motor 1)
17                    output_2,    // pin 6     -  output 2 (backward for motor 2)
18
19                    output_3,    // pin 11    -  output 3 (forward for motor 3)
20                    output_4 // pin 14    -  output 4 (backward for motor 4)
21    );
22
23    always_comb begin
24
25       output_1 <= (enable_1) ? (input_1) : (1'bz);
26       output_2 <= (enable_1) ? (input_2) : (1'bz);
27
28       output_3 <= (enable_2) ? (input_3) : (1'bz);
29       output_4 <= (enable_2) ? (input_4) : (1'bz);
30    end
31
32 endmodule
```

(a) SystemVerilog code for the (NAME) block used in the design.

```
1
2  // https://www.st.com/content/ccc/resource/technical/document/datasheet/04/ac/22/f9/20/5d/4
3
4  // Delay will have scale of 1ns per #n listed (resolution 100ps)
5  `timescale 1ns/100ps
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7  module L293D_test_chip (
8     input logic     enable_1,    // pin 1     -  enable for inputs 1 and 2
9                     input_1,     // pin 2     -  input 1 (forward for motor 1)
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11
12                    enable_2,    // pin 9     -  enable for inputs 3 and 4
13                    input_3,     // pin 10    -  input 3 (forward for motor 2)
14                    input_4,     // pin 15    -  input 4 (backward for motor 2)
15
16    output logic    output_1,    // pin 3     -  output 1 (forward for motor 1)
17                    output_2,    // pin 6     -  output 2 (backward for motor 2)
18
19                    output_3,    // pin 11    -  output 3 (forward for motor 3)
20                    output_4 // pin 14    -  output 4 (backward for motor 4)
21    );
22
23    always_comb begin
24
25       output_1 <= (enable_1) ? (input_1) : (1'bz);
26       output_2 <= (enable_1) ? (input_2) : (1'bz);
27
28       output_3 <= (enable_2) ? (input_3) : (1'bz);
29       output_4 <= (enable_2) ? (input_4) : (1'bz);
30    end
31
32 endmodule
```

(a) SystemVerilog code for the (NAME) block used in the design.

A.2 Functional Unit Name

```
1
2  // https://www.st.com/content/ccc/resource/technical/document/datasheet/04/ac/22/f9/20/5d/4
3
4  // Delay will have scale of 1ns per #n listed (resolution 100ps)
5  `timescale 1ns/100ps
6
7  module L293D_test_chip (
8     input logic     enable_1,    // pin 1     -  enable for inputs 1 and 2
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10                    input_2,     // pin 7     -  input 2 (backward for motor 1)
11
12                    enable_2,    // pin 9     -  enable for inputs 3 and 4
13                    input_3,     // pin 10    -  input 3 (forward for motor 2)
14                    input_4,     // pin 15    -  input 4 (backward for motor 2)
15
16    output logic    output_1,    // pin 3     -  output 1 (forward for motor 1)
17                    output_2,    // pin 6     -  output 2 (backward for motor 2)
18
19                    output_3,    // pin 11    -  output 3 (forward for motor 3)
20                    output_4 // pin 14    -  output 4 (backward for motor 4)
21    );
22
23    always_comb begin
24
25       output_1 <= (enable_1) ? (input_1) : (1'bz);
26       output_2 <= (enable_1) ? (input_2) : (1'bz);
27
28       output_3 <= (enable_2) ? (input_3) : (1'bz);
29       output_4 <= (enable_2) ? (input_4) : (1'bz);
30    end
31
32 endmodule
```

(a) SystemVerilog code for the (NAME) block used in the design.

```
1
2  // https://www.st.com/content/ccc/resource/technical/document/datasheet/04/ac/22/f9/20/5d/4
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4  // Delay will have scale of 1ns per #n listed (resolution 100ps)
5  `timescale 1ns/100ps
6
7  module L293D_test_chip (
8     input logic     enable_1,    // pin 1    -  enable for inputs 1 and 2
9                     input_1,     // pin 2    -  input 1 (forward for motor 1)
10                    input_2,     // pin 7    -  input 2 (backward for motor 1)
11
12                    enable_2,    // pin 9    -  enable for inputs 3 and 4
13                    input_3,     // pin 10   -  input 3 (forward for motor 2)
14                    input_4,     // pin 15   -  input 4 (backward for motor 2)
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16    output logic    output_1,    // pin 3    -  output 1 (forward for motor 1)
17                    output_2,    // pin 6    -  output 2 (backward for motor 2)
18
19                    output_3,    // pin 11   -  output 3 (forward for motor 3)
20                    output_4 // pin 14    -  output 4 (backward for motor 4)
21    );
22
23    always_comb begin
24
25       output_1 <= (enable_1) ? (input_1) : (1'bz);
26       output_2 <= (enable_1) ? (input_2) : (1'bz);
27
28       output_3 <= (enable_2) ? (input_3) : (1'bz);
29       output_4 <= (enable_2) ? (input_4) : (1'bz);
30    end
31
32 endmodule
```

(a) SystemVerilog code for the (NAME) block used in the design.

```
1
2  // https://www.st.com/content/ccc/resource/technical/document/datasheet/04/ac/22/f9/20/5d/4
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4  // Delay will have scale of 1ns per #n listed (resolution 100ps)
5  `timescale 1ns/100ps
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7  module L293D_test_chip (
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10                    input_2,     // pin 7    -  input 2 (backward for motor 1)
11
12                    enable_2,    // pin 9    -  enable for inputs 3 and 4
13                    input_3,     // pin 10   -  input 3 (forward for motor 2)
14                    input_4,     // pin 15   -  input 4 (backward for motor 2)
15
16    output logic    output_1,    // pin 3    -  output 1 (forward for motor 1)
17                    output_2,    // pin 6    -  output 2 (backward for motor 2)
18
19                    output_3,    // pin 11   -  output 3 (forward for motor 3)
20                    output_4 // pin 14    -  output 4 (backward for motor 4)
21    );
22
23    always_comb begin
24
25       output_1 <= (enable_1) ? (input_1) : (1'bz);
26       output_2 <= (enable_1) ? (input_2) : (1'bz);
27
28       output_3 <= (enable_2) ? (input_3) : (1'bz);
29       output_4 <= (enable_2) ? (input_4) : (1'bz);
30    end
31
32 endmodule
```

(a) SystemVerilog code for the (NAME) block used in the design.

B Simulation Files (Do Scripts)

This appendix will list the Do Scripts used to simulate each block used in the design project.

B.1 Functional Unit Name

```
1
2  // https://www.st.com/content/ccc/resource/technical/document/datasheet/04/ac/22/f9/20/5d/4
3
4  // Delay will have scale of 1ns per #n listed (resolution 100ps)
5  `timescale 1ns/100ps
6
7  module L293D_test_chip (
8     input logic     enable_1,    // pin 1     -  enable for inputs 1 and 2
9                     input_1,     // pin 2     -  input 1 (forward for motor 1)
10                    input_2,     // pin 7     -  input 2 (backward for motor 1)
11
12                    enable_2,    // pin 9     -  enable for inputs 3 and 4
13                    input_3,     // pin 10    -  input 3 (forward for motor 2)
14                    input_4,     // pin 15    -  input 4 (backward for motor 2)
15
16    output logic    output_1,    // pin 3     -  output 1 (forward for motor 1)
17                    output_2,    // pin 6     -  output 2 (backward for motor 2)
18
19                    output_3,    // pin 11    -  output 3 (forward for motor 3)
20                    output_4 // pin 14    -  output 4 (backward for motor 4)
21    );
22
23    always_comb begin
24
25       output_1 <= (enable_1) ? (input_1) : (1'bz);
26       output_2 <= (enable_1) ? (input_2) : (1'bz);
27
28       output_3 <= (enable_2) ? (input_3) : (1'bz);
29       output_4 <= (enable_2) ? (input_4) : (1'bz);
30    end
31
32 endmodule
```

(a) Do Script for the (NAME) block used in the design.

```
1
2  // https://www.st.com/content/ccc/resource/technical/document/datasheet/04/ac/22/f9/20/5d/4
3
4  // Delay will have scale of 1ns per #n listed (resolution 100ps)
5  `timescale 1ns/100ps
6
7  module L293D_test_chip (
8     input logic     enable_1,    // pin 1     -  enable for inputs 1 and 2
9                     input_1,     // pin 2     -  input 1 (forward for motor 1)
10                    input_2,     // pin 7     -  input 2 (backward for motor 1)
11
12                    enable_2,    // pin 9     -  enable for inputs 3 and 4
13                    input_3,     // pin 10    -  input 3 (forward for motor 2)
14                    input_4,     // pin 15    -  input 4 (backward for motor 2)
15
16    output logic    output_1,    // pin 3     -  output 1 (forward for motor 1)
17                    output_2,    // pin 6     -  output 2 (backward for motor 2)
18
19                    output_3,    // pin 11    -  output 3 (forward for motor 3)
20                    output_4 // pin 14    -  output 4 (backward for motor 4)
21    );
22
23    always_comb begin
24
25       output_1 <= (enable_1) ? (input_1) : (1'bz);
26       output_2 <= (enable_1) ? (input_2) : (1'bz);
27
28       output_3 <= (enable_2) ? (input_3) : (1'bz);
29       output_4 <= (enable_2) ? (input_4) : (1'bz);
30    end
31
32 endmodule
```

(a) Do Script code for the (NAME) block used in the design.

```
1
2  // https://www.st.com/content/ccc/resource/technical/document/datasheet/04/ac/22/f9/20/5d/4
3
4  // Delay will have scale of 1ns per #n listed (resolution 100ps)
5  `timescale 1ns/100ps
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8     input logic     enable_1,    // pin 1    -  enable for inputs 1 and 2
9                     input_1,     // pin 2    -  input 1 (forward for motor 1)
10                    input_2,     // pin 7    -  input 2 (backward for motor 1)
11
12                    enable_2,    // pin 9    -  enable for inputs 3 and 4
13                    input_3,     // pin 10   -  input 3 (forward for motor 2)
14                    input_4,     // pin 15   -  input 4 (backward for motor 2)
15
16    output logic    output_1,    // pin 3    -  output 1 (forward for motor 1)
17                    output_2,    // pin 6    -  output 2 (backward for motor 2)
18
19                    output_3,    // pin 11   -  output 3 (forward for motor 3)
20                    output_4 // pin 14    -  output 4 (backward for motor 4)
21    );
22
23    always_comb begin
24
25       output_1 <= (enable_1) ? (input_1) : (1'bz);
26       output_2 <= (enable_1) ? (input_2) : (1'bz);
27
28       output_3 <= (enable_2) ? (input_3) : (1'bz);
29       output_4 <= (enable_2) ? (input_4) : (1'bz);
30    end
31
32 endmodule
```

(a) Do Script code for the (NAME) block used in the design.

B.2 Functional Unit Name

```
1
2  // https://www.st.com/content/ccc/resource/technical/document/datasheet/04/ac/22/f9/20/5d/4
3
4  // Delay will have scale of 1ns per #n listed (resolution 100ps)
5  `timescale 1ns/100ps
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7  module L293D_test_chip (
8     input logic     enable_1,    // pin 1     -  enable for inputs 1 and 2
9                     input_1,     // pin 2     -  input 1 (forward for motor 1)
10                    input_2,     // pin 7     -  input 2 (backward for motor 1)
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12                    enable_2,    // pin 9     -  enable for inputs 3 and 4
13                    input_3,     // pin 10    -  input 3 (forward for motor 2)
14                    input_4,     // pin 15    -  input 4 (backward for motor 2)
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16    output logic    output_1,    // pin 3     -  output 1 (forward for motor 1)
17                    output_2,    // pin 6     -  output 2 (backward for motor 2)
18
19                    output_3,    // pin 11    -  output 3 (forward for motor 3)
20                    output_4 // pin 14    -  output 4 (backward for motor 4)
21    );
22
23    always_comb begin
24
25       output_1 <= (enable_1) ? (input_1) : (1'bz);
26       output_2 <= (enable_1) ? (input_2) : (1'bz);
27
28       output_3 <= (enable_2) ? (input_3) : (1'bz);
29       output_4 <= (enable_2) ? (input_4) : (1'bz);
30    end
31
32 endmodule
```

(a) Do Script for the (NAME) block used in the design.

```
1
2  // https://www.st.com/content/ccc/resource/technical/document/datasheet/04/ac/22/f9/20/5d/4
3
4  // Delay will have scale of 1ns per #n listed (resolution 100ps)
5  `timescale 1ns/100ps
6
7  module L293D_test_chip (
8     input logic     enable_1,    // pin 1    -  enable for inputs 1 and 2
9                     input_1,     // pin 2    -  input 1 (forward for motor 1)
10                    input_2,     // pin 7    -  input 2 (backward for motor 1)
11
12                    enable_2,    // pin 9    -  enable for inputs 3 and 4
13                    input_3,     // pin 10   -  input 3 (forward for motor 2)
14                    input_4,     // pin 15   -  input 4 (backward for motor 2)
15
16    output logic    output_1,    // pin 3    -  output 1 (forward for motor 1)
17                    output_2,    // pin 6    -  output 2 (backward for motor 2)
18
19                    output_3,    // pin 11   -  output 3 (forward for motor 3)
20                    output_4 // pin 14    -  output 4 (backward for motor 4)
21    );
22
23    always_comb begin
24
25       output_1 <= (enable_1) ? (input_1) : (1'bz);
26       output_2 <= (enable_1) ? (input_2) : (1'bz);
27
28       output_3 <= (enable_2) ? (input_3) : (1'bz);
29       output_4 <= (enable_2) ? (input_4) : (1'bz);
30    end
31
32 endmodule
```

(a) Do Script code for the (NAME) block used in the design.

```
1
2  // https://www.st.com/content/ccc/resource/technical/document/datasheet/04/ac/22/f9/20/5d/4
3
4  // Delay will have scale of 1ns per #n listed (resolution 100ps)
5  `timescale 1ns/100ps
6
7  module L293D_test_chip (
8     input logic     enable_1,    // pin 1    -  enable for inputs 1 and 2
9                     input_1,     // pin 2    -  input 1 (forward for motor 1)
10                    input_2,     // pin 7    -  input 2 (backward for motor 1)
11
12                    enable_2,    // pin 9    -  enable for inputs 3 and 4
13                    input_3,     // pin 10   -  input 3 (forward for motor 2)
14                    input_4,     // pin 15   -  input 4 (backward for motor 2)
15
16    output logic    output_1,    // pin 3    -  output 1 (forward for motor 1)
17                    output_2,    // pin 6    -  output 2 (backward for motor 2)
18
19                    output_3,    // pin 11   -  output 3 (forward for motor 3)
20                    output_4 // pin 14    -  output 4 (backward for motor 4)
21    );
22
23    always_comb begin
24
25       output_1 <= (enable_1) ? (input_1) : (1'bz);
26       output_2 <= (enable_1) ? (input_2) : (1'bz);
27
28       output_3 <= (enable_2) ? (input_3) : (1'bz);
29       output_4 <= (enable_2) ? (input_4) : (1'bz);
30    end
31
32 endmodule
```

(a) Do Script code for the (NAME) block used in the design.