Intel® Open Source HD Graphics Programmers' Reference Manual (PRM)

Volume 2c: Command Reference: Register Addresses

For the 2014-2015 Intel Atom™ Processors, Celeron™ Processors and Pentium™ Processors based on the "Cherry Trail/Braswell" Platform (Cherryview/Braswell graphics)

June 2015, Revision 1.0

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Advanced Features Length and Capabilities

AFLC - Advanced Features Length and Capabilities		
Register Space:	PCI: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x03060013	
Size (in bits):	32	
Address:	000A4h	
FLR capability advertisement		

DWord	Bit	Description	
0	31:26	**RESERVED**	
		Default Value:	00h
		Access:	RO
		Reserved	
	25	**FLR_CAP**	
		Default Value:	1b
		Access:	RO
		Function Level Reset Capability (FLR_CAP): 0: Function Level Reset is not supported 1: Function Level Reset is supported	
	24	**TP_CAP**	
		Default Value:	1b
		Access:	RO
		Transactions Pending Capability (TP_CAP): 0: Transactions Pending bit is not supported 1: Transactions Pending bit is supported	
	23:16	**LENGTH**	
		Default Value:	06h
		Access:	RO
		Advanced Features Structure Length(LENGTH): The Advanced Features capability structure is 6bytes long.	
	15:8	**NXT_PTR**	
		Default Value:	00h
		Access:	R/W Once
		Next Pointer (NXT_PTR):	

AFLC - Advanced Features Length and Capabilities

		Points to the next item in the list (B0=Vendor Capabilities ID). This register should be programmed by BIOS during boot-up. Once written, this register becomes Read_Only. This register can only be cleared by a Reset. Write once so capabilities list can be changed if needed.
	7:0	**CAP_ID**

Default Value:	13h
Access:	RO

Capability Identifier (CAP_ID):
A value of 13h identifies that this PCI Function is capable of Advanced Features.

Advanced Scheduler Reset Request Messages

ASSRREQ - Advanced Scheduler Reset Request Messages		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0810Ch	
Hardware (CS, VCS) initiated Advanced Scheduler reset request messages.		

DWord	Bit	Description
0	31:16	**Message Mask**
		Access: RO
		Message Mask In order to write to bits 15:0, the corresponding message mask bits must be written. For example, for bit 14 to be set, bit 30 needs to be 1 : 40004000
	15:4	**Reserved**
		Access: RO
		Reserved
	3	**VINunit cmfxrst reset request message (2nd Vbox)**
		Access: R/W Set
		CMFX Reset Request Message from the VINunit in 2nd Vbox: '1' : CMFX Reset Requested - This bit is cleared by the CP upon completion of the reset request '0' : CMFX Reset Not Requested
	2	**VINunit cmfxrst Reset Request message**
		Access: R/W Set
		CMFX Reset Request Message from the VINunit: '1' : CMFX Reset Requested - This bit is cleared by the CP upon completion of the reset request '0' : CMFX Reset Not Requested
	1	**Render AS Reset Request Message**
		Access: R/W Set
		Render AS Reset Request Message from the CSunit: '1' : Render AS Reset Requested - This bit is cleared by the CP upon completion of the reset request '0' : Render AS Reset Not Requested

ASSRREQ - Advanced Scheduler Reset Request Messages

	0	**Media AS Reset Request Message**

Access:	R/W Set

Media AS Reset Request Message from the VCSunit:
'1' : Media AS Reset Requested
- This bit is cleared by the CP upon completion of the reset request
'0' : Media AS Reset Not Requested

Aggregate_Perf_Counter_A31

OAPERF_A31 - Aggregate_Perf_Counter_A31	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	028F8h
Valid Projects:	[CHV, BSW]

This register reflects the count value of the OA Performance counter A31

DWord	Bit	Description
0	31:0	**Considerations**
		Format: U32
		This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate_Perf_Counter_A32

OAPERF_A32 - Aggregate_Perf_Counter_A32	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02900h
Valid Projects:	[CHV, BSW]

This register reflects the count value of the OA Performance counter A32

DWord	Bit	Description
0	31:0	**Considerations**
		<table><tr><td>Format:</td><td>U32</td></tr></table> This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate_Perf_Counter_A33

OAPERF_A33 - Aggregate_Perf_Counter_A33	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02904h
Valid Projects:	[CHV, BSW]

This register reflects the count value of the OA Performance counter A33

DWord	Bit	Description
0	31:0	**Considerations**
		Format: U32
		This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate_Perf_Counter_A34

OAPERF_A34 - Aggregate_Perf_Counter_A34

Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32

Address:	02908h
Valid Projects:	[CHV, BSW]

This register reflects the count value of the OA Performance counter A34

DWord	Bit	Description
0	31:0	**Considerations**

Format:	U32

This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate_Perf_Counter_A35

OAPERF_A35 - Aggregate_Perf_Counter_A35	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	0290Ch
Valid Projects:	[CHV, BSW]

This register reflects the count value of the OA Performance counter A35

DWord	Bit	Description
0	31:0	**Considerations**
		Format: U32
		This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A1

<table>
<tr><td colspan="2">**OAPERF_A1 - Aggregate Perf Counter A1**</td></tr>
<tr><td>Register Space:</td><td>MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td>CHV, BSW</td></tr>
<tr><td>Source:</td><td>BSpec</td></tr>
<tr><td>Default Value:</td><td>0x00000000</td></tr>
<tr><td>Access:</td><td>R/W</td></tr>
<tr><td>Size (in bits):</td><td>32</td></tr>
<tr><td>Address:</td><td>02808h</td></tr>
<tr><td>Valid Projects:</td><td>[CHV, BSW]</td></tr>
</table>

This register reflects the count value of the OA Performance counter A1. DefaultValue="00000000h"

DWord	Bit	Description
0	31:0	Considerations: This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A5

OAPERF_A5 - Aggregate Perf Counter A5	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02828h
Valid Projects:	[CHV, BSW]

This register reflects the count value of the OA Performance counter A5. DefaultValue="00000000h"

DWord	Bit	Description
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A7

OAPERF_A7 - Aggregate Perf Counter A7	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02838h
Valid Projects:	[CHV, BSW]

This register reflects the count value of the OA Performance counter A7. DefaultValue="00000000h"

DWord	Bit	Description
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A8

OAPERF_A8 - Aggregate Perf Counter A8	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02840h
Valid Projects:	[CHV, BSW]

This register reflects the count value of the OA Performance counter A8. DefaultValue="00000000h"

DWord	Bit	Description
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A9

OAPERF_A9 - Aggregate Perf Counter A9	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02848h
Valid Projects:	[CHV, BSW]

This register reflects the count value of the OA Performance counter A9. DefaultValue="00000000h"

DWord	Bit	Description
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A10

OAPERF_A10 - Aggregate Perf Counter A10	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02850h
Valid Projects:	[CHV, BSW]

This register reflects the count value of the OA Performance counter A10. DefaultValue="00000000h"

DWord	Bit	Description
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A11

OAPERF_A11 - Aggregate Perf Counter A11	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02858h
Valid Projects:	[CHV, BSW]

This register reflects the count value of the OA Performance counter A11. DefaultValue="00000000h"

DWord	Bit	Description
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A12

OAPERF_A12 - Aggregate Perf Counter A12	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02860h
Valid Projects:	[CHV, BSW]

This register reflects the count value of the OA Performance counter A12. DefaultValue="00000000h"

DWord	Bit	Description
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A14

OAPERF_A14 - Aggregate Perf Counter A14	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02870h
Valid Projects:	[CHV, BSW]

This register reflects the count value of the OA Performance counter A14. DefaultValue="00000000h"

DWord	Bit	Description
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A15

OAPERF_A15 - Aggregate Perf Counter A15	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02878h
Valid Projects:	[CHV, BSW]

This register reflects the count value of the OA Performance counter A15. DefaultValue="00000000h"

DWord	Bit	Description
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A16

OAPERF_A16 - Aggregate Perf Counter A16	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02880h
Valid Projects:	[CHV, BSW]

This register reflects the count value of the OA Performance counter A16. DefaultValue="00000000h"

DWord	Bit	Description
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A17

OAPERF_A17 - Aggregate Perf Counter A17	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02888h
Valid Projects:	[CHV, BSW]

This register reflects the count value of the OA Performance counter A17. DefaultValue="00000000h"

DWord	Bit	Description
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A18

OAPERF_A18 - Aggregate Perf Counter A18	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02890h
Valid Projects:	[CHV, BSW]

This register reflects the count value of the OA Performance counter A9. DefaultValue="00000000h"

DWord	Bit	Description
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A21

OAPERF_A21 - Aggregate Perf Counter A21	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	028A8h
Valid Projects:	[CHV, BSW]

This register reflects the count value of the OA Performance counter A21. DefaultValue="00000000h"

DWord	Bit	Description
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A22

OAPERF_A22 - Aggregate Perf Counter A22	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	028B0h
Valid Projects:	[CHV, BSW]

This register reflects the count value of the OA Performance counter A22. DefaultValue="00000000h"

DWord	Bit	Description
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A23

OAPERF_A23 - Aggregate Perf Counter A23	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	028B8h
Valid Projects:	[CHV, BSW]

This register reflects the count value of the OA Performance counter A23. DefaultValue="00000000h"

DWord	Bit	Description
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A24

OAPERF_A24 - Aggregate Perf Counter A24	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	028C0h
Valid Projects:	[CHV, BSW]

This register reflects the count value of the OA Performance counter A24. DefaultValue="00000000h"

DWord	Bit	Description
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A25

<table>
<tr><td colspan="2" align="center">**OAPERF_A25 - Aggregate Perf Counter A25**</td></tr>
<tr><td>Register Space:</td><td>MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td>CHV, BSW</td></tr>
<tr><td>Source:</td><td>BSpec</td></tr>
<tr><td>Default Value:</td><td>0x00000000</td></tr>
<tr><td>Access:</td><td>R/W</td></tr>
<tr><td>Size (in bits):</td><td>32</td></tr>
<tr><td>Address:</td><td>028C8h</td></tr>
<tr><td>Valid Projects:</td><td>[CHV, BSW]</td></tr>
</table>

This register reflects the count value of the OA Performance counter A25. DefaultValue="00000000h"

DWord	Bit	Description
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A26

OAPERF_A26 - Aggregate Perf Counter A26	

Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32

Address:	028D0h
Valid Projects:	[CHV, BSW]

This register reflects the count value of the OA Performance counter A26. DefaultValue="00000000h"

DWord	Bit	Description
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A27

OAPERF_A27 - Aggregate Perf Counter A27	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	028D8h
Valid Projects:	[CHV, BSW]

This register reflects the count value of the OA Performance counter A27. DefaultValue="00000000h"

DWord	Bit	Description
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A28

OAPERF_A28 - Aggregate Perf Counter A28	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	028E0h
Valid Projects:	[CHV, BSW]

This register reflects the count value of the OA Performance counter A28. DefaultValue="00000000h"

DWord	Bit	Description
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A29

OAPERF_A29 - Aggregate Perf Counter A29	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	028E8h
Valid Projects:	[CHV, BSW]

This register reflects the count value of the OA Performance counter A29. DefaultValue="00000000h"

DWord	Bit	Description
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A30

OAPERF_A30 - Aggregate Perf Counter A30	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	028F0h
Valid Projects:	[CHV, BSW]

This register reflects the count value of the OA Performance counter A30. DefaultValue="00000000h"

DWord	Bit	Description
0	31:0	**Considerations** This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

AFCTLSTS

<table>
<tr><td colspan="3" align="center">**AFCTLSTS - AFCTLSTS**</td></tr>
<tr><td colspan="3">Register Space: PCI: 0/2/0</td></tr>
<tr><td colspan="3">Project: CHV, BSW</td></tr>
<tr><td colspan="3">Source: PRM</td></tr>
<tr><td colspan="3">Default Value: 0x00000000</td></tr>
<tr><td colspan="3">Size (in bits):   16</td></tr>
<tr><td colspan="3">Address: 000A8h</td></tr>
<tr><td colspan="3">FLR control
Advanced Feature Status</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td>**Description**</td></tr>
<tr><td>0</td><td>15:9</td><td>**Reserved**
Default Value: 00h
Access: RO
Reserved (RSVD)</td></tr>
<tr><td></td><td>8</td><td>**TP**
Default Value: 0b
Access: RO
Transaction Pending (TP):
1: The Function has issued one or more non-posted transactions which have not been completed, including non-posted transactions that a target has terminated with Retry.
0: All non-posted transactions have been completed.</td></tr>
<tr><td></td><td>7:1</td><td>**Reserved**
Default Value: 00h
Access: RO
Reserved (RSVD)</td></tr>
<tr><td></td><td>0</td><td>**INIT_FLR**
Default Value: 0b
Access: R/W Set
Initiate Function Level Reset (INIT_FLR):
A write of 1b initiates Function Level Reset (FLR).
FLR requirements are defined in the PCI Express Base Specification. Registers and state information that do not apply to conventional PCI are exempt from the FLR requirements given there.
Once written 1, FLR will be initiated. During FLR, a read will return 1's since device 2 reads abort. Once FLR completes, hardware will clear the bit to 0.</td></tr>
</table>

All Engine Fault Register

FAULT_REG - All Engine Fault Register		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04094h	

DWord	Bit	Description
0	31:1	**All Engine Fault Register**
		<table><tr><td>Default Value:</td><td>00000000000000000000000000000000b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table>
		Bit[31:15]: Reserved. Bit[14:12]: Engine ID: 000b - GFX. 001b - MFX0. 010b - MFX1. 011b - VEBX. 100b - BLT.
		110b - WIDI. Bit[11]: Reserved. Bit[10:3]: SRCID of Fault. This is the Source ID of the unit that requested the cycle that generated the First Page fault for this engine. This value is locked and not updated on subsequent faults, until the valid bit of this register is cleared by SW. Bit[2:1]: Fault Type (GFX_FT): Type of Fault recorded: 00b - Invalid PTE Fault. 01b - Invalid PDE Fault. 10b - Invalid PDPE Fault. 11b - Invalid PML4E Fault. This value is locked and not updated on subsequent faults, until the valid bit of this register is cleared by SW. All bits are only valid with bit[0]=1.
	0	**Valid Bit**
		<table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table>
		This bit indicates that the first fault for this engine has been recorded. It can only be cleared by SW, which also clears the other fields.

ARAT CUTRIG HI

ARAT_CUTRIG_HI - ARAT CUTRIG HI	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0A1B4h

DWord	Bit	Description
0	31:0	**ARAT TRIG HI** Access: RO [31:0]: 63:32 of (ARAT_TDELTA + TSC)[63:32] when A174[0] transitions to a one, or when A174[1:0]=11 and TSC crosses over ARAT_TRIG

ARAT CUTRIG LO

ARAT_CUTRIG_LO - ARAT CUTRIG LO		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A1B0h	

DWord	Bit	Description
0	31:3	**ARAT TRIG LO**
		Access: RO
		31:3 of (ARAT_TDELTA + TSC)[31:3] when A174[0] transitions to a one, or when A174[1:0]=11 and TSC crosses over ARAT_TRIG
	2	**Reserved**
		Access: RO
	1:0	**ARAT TRIG Mode**
		Access: RO
		0xA174[1:0] when A174[0] transitions to a one, or when A174[1:0]=11 and TSC crosses over ARAT_TRIG

ARAT Delta (LSB)

ARAT_TDELTA_LOW - ARAT Delta (LSB)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A174h	

DWord	Bit	Description
0	31:3	**Lower Bits of Delta Time for ARAT** Access: R/W Low Bits [31:3] of Delta Time, in 80ns increments(LSB would be in 10ns increments, if it went down to zero)
	2	**Reserved** Access: RO
	1	**ARAT Mode** Access: R/W 0b : One-Shot Mode (default) 1b : Periodic Mode
	0	**ARAT Enable** Access: R/W 0b : ARAT Disabled (default) 1b : ARAT Enabled

ARAT Delta (MSB)

ARAT_TDELTA_HIGH - ARAT Delta (MSB)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A170h	

DWord	Bit	Description
0	31:24	**Reserved**
		Access: RO
	23:0	**Upper Bits of Delta Time for ARAT**
		Access: R/W
		High Bits [55:32] of Delta Time, in 80ns increments

ARAT POST CU BUSY

ARAT_POSTCUBUSY - ARAT POST CU BUSY		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A17Ch	

DWord	Bit	Description
0	31:3	**ARAT PostThreshold**
		Access: R/W
		PostThreshold, in 80ns increments to prevent short gfx_clockstartreq. If current_TSC - ARAT_CUTRIG > PostThreshold, show GFX as busy.
	2:0	**Reserved**
		Access: RO

ARAT PRE CU BUSY

<table>
<tr><td colspan="4" align="center">**ARAT_PRECUBUSY - ARAT PRE CU BUSY**</td></tr>
<tr><td colspan="2">Register Space:</td><td colspan="2">MMIO: 0/2/0</td></tr>
<tr><td colspan="2">Project:</td><td colspan="2">CHV, BSW</td></tr>
<tr><td colspan="2">Source:</td><td colspan="2">PRM</td></tr>
<tr><td colspan="2">Default Value:</td><td colspan="2">0x00000000</td></tr>
<tr><td colspan="2">Size (in bits):</td><td colspan="2">32</td></tr>
<tr><td colspan="2">Address:</td><td colspan="2">0A178h</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td colspan="2" align="center">**Description**</td></tr>
<tr><td rowspan="4">0</td><td rowspan="3">31:3</td><td colspan="2">**ARAT PreThreshold**</td></tr>
<tr><td>Access:</td><td>R/W</td></tr>
<tr><td colspan="2">PreThreshold, in 80ns increments to prevent short gfx_clockstartreq. If ARAT_CUTRIG minus current_TSC < PreThreshold, show GFX as busy.</td></tr>
<tr><td>2:0</td><td colspan="2">**Reserved**</td></tr>
<tr><td></td><td></td><td>Access:</td><td>RO</td></tr>
</table>

Arbiter Control Register

GARBCNTLREG - Arbiter Control Register		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x29124100 CHV, BSW	
Size (in bits):	32	
Address:	0B004h	

DWord	Bit	Description
0	31	**Reserved**
	30	**Disables hashing function**
		Access: R/W
		Disables hashing function to generate bank_id[1:0] for L3$ bank accessing, and forces the use of address[7:6] for bank_id[1:0].0: (default) Hash function enabled to generate L3$ bank IDs. 1: L3$ address[7:6] used as L3$ bank IDs. lncf_csr_l3bankidhashdis. (This bit needs to set corresponding bit lpfcon_csr_l3bankidhashdis in LPFC.)
	29:28	**Arbitration priority order between RCC and MSC**
		Default Value: 10b
		Access: R/W
		Arbitration priority order between RCC and MSC. 00b/11b: Invalid; default setting used. 10b: Default setting; RCC MSC (i.e., MSC has higher priority). 01b: RCC MSC (i.e., RCC has higher priority). lncf_csr_rcc_msc_pri[1:0].
	27:22	**Arbitration priority order between RCZ, STC, and HIZ**
		Default Value: 100100b
		Access: R/W
		Arbitration priority order between RCZ, STC, and HIZ. 100100b: Default setting; RCZ STC HIZ. (i.e., RCZ has lowest priority; HIZ has highest priority). 100001b: RCZ ; HIZ ; STC. 011000b: STC ; RCZ ; HIZ. 010010b: STC ; HIZ ; RCZ. 001001b: HIZ ; RCZ ; STC. 000110b: HIZ ; STC ; RCZ. Note: Others settings are invalid, and result in use of default. lncf_csr_rcz_stc_hiz_pri[5:0].

GARBCNTLREG - Arbiter Control Register

21:19	**Write data port arbitration priority between Z client writes and L3$ evictions**	
	Default Value:	010b
	Access:	R/W
	Z Max Write Request Limit Count (GFXC_MRLC). This is the MAX number of Allowed Requests Count - These counters keep track of the accepted requests from each engine. Requests are counted, regardless of kind of cycle (both Slice 0 and 1). Minimum count value must be = 1. lncf_csr_wdpagapz[2:0].	
18:16	**Write data port arbitration priority between C client writes and Z/L3$ writes/evictions**	
	Default Value:	010b
	Access:	R/W
	C Max Request Limit Count (GFXZ_MRLC). This is the MAX number of Allowed Requests Count - These counters keep track of the accepted requests from each engine. Requests are counted, regardless of kind of cycle (both Slice 0 and 1). Minimum count value must be = 1. lncf_csr_wdpagapc[2:0].	
15	**Reserved**	
	Access:	RO
14:12	**L3 Max Write Request Limit Count**	
	Default Value:	100b
	Access:	R/W
	L3 Max Write Request Limit Count (GFXL3_MRLC). This is the MAX number of Allowed Requests Count - These counters keep track of the accepted requests from each engine. Requests are counted, regardless of kind of cycle (Miss/Hit/Present). Minimum count value must be = 1. lncf_csr_wdpagapl3[2:0].	
11:9	**Reserved**	
	Access:	RO
8	**GAPs_fixarb_en**	
	Default Value:	1b
	Access:	R/W
	lncf_csr_gaps_fixarb_en.	
6:0	**Reserved**	
	Project:	CHV, BSW
	Access:	RO

Arbiter Mode Control Register

		ARB_MODE - Arbiter Mode Control Register

Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32

Address:	04030h

DWord	Bit	Description
0	31:16	**Mask Bits**
		Default Value: 0000000000000000b
		Access: RO
		Mask Bits act as Write Enables for the bits[15:0] of this register.
	15	**Extra Register Bit 15**
		Default Value: 0b
		Access: R/W
		Bit 15 toggles (XOR) the meaning of Per Client Write Drop Enables (Register 40b4); If 0, drop per client happens as stated in register 40b4 definition; If 1, the meaning changes, and a 1 on a bit in register 40b4 means dont drop while 0 means drop. In this case, the default (for clients not included in 40b4) will be drop enabled.
	14	**Extra Register Bit 14**
		Default Value: 0b
		Project: CHV, BSW
		Access: R/W
		PD load disable - When this bit is set, the PD load is disabled for GFX/MFX0/MFX1. A-step: Default Value: 0 B-step: Default Value: 0 - Bug ID: 1905990 Future steppings can have value 1.
	13	**DC GDR**
		Default Value: 0b
		Access: R/W
	12	**HIZ GDR**
		Default Value: 0b
		Access: R/W
	11	**STC GDR**
		Default Value: 0b
		Access: R/W

ARB_MODE - Arbiter Mode Control Register

	10	**BLB GDR**	
		Default Value:	0b
		Access:	R/W

	9	**GAM PD GDR**	
		Default Value:	0b
		Access:	R/W

	8	**Extra Register Bit 8**	
		Default Value:	0b
		Access:	R/W

Description
Snoop Override [CHV, BSW Only] 0 - No override (default) 1 - Snoop is set for all accesses to memory

	7:6	**Cacheability Attribute Override**	
		Default Value:	00b
		Access:	R/W

00b No override.
01b UC (LLC/eLLC) - Allocation age is don't care.
10b WT in LLC/eLLC - Aged is 3.
11b WB in LLC/eLLC - Aged is 3.
The above conditions apply for the following conditions only:
1. Register overwrite except for GTT, CFG and L3 coherent wcil cycles
2. Read- GTTRD, CFGRD
3. Write- GTTWR, CFGWR, DMWR (with gam_ci_wcoherenttype[2:0]="001" WCIL* w/self snoop)

	5	**Extra Register Bit 5**	
		Default Value:	0b
		Access:	R/W

Reserved.

	4	**VMC GDR Enable**	
		Default Value:	0b
		Access:	R/W

When this bit is set, data requested from the VMC client is generated by the GDR Algorithm.

	3	**Texture Cache (MT) GDR Enable Bit**	
		Default Value:	0b
		Access:	R/W

When this bit is set, data requested from the Texture Cache (MT) client is generated by the GDR algorithm.

ARB_MODE - Arbiter Mode Control Register

	2	**Depth (RCZ) Cache GDR Enable bit**	
		Default Value:	0b
		Access:	R/W
		Depth Cache GDR enable bit. Project: All. Format: U1. When this bit is set, data requested from the Depth Cache client is generated by the GDR algorithm (See GDR algorithm in xxx section).	
	1	**Color Cache (RCC) GDR Enable Bit**	
		Default Value:	0b
		Access:	R/W
		When this bit is set, data requested from the Color Cache (RCC) client is generated by the GDR algorithm.	
	0	**GTT Accesses GDR**	
		Default Value:	0b
		Access:	R/W
		When this bit is enabled along with the Client's GDR bit, PPGTT and GGTT requests for this memory access are also tagged as GDR to SQ.	

ASLS

<table>
<tr><td colspan="4" align="center">**ASLS - ASLS**</td></tr>
<tr><td colspan="4">Register Space: PCI: 0/2/0

Project: CHV, BSW

Source: PRM

Default Value: 0x00000000

Size (in bits):   32</td></tr>
<tr><td colspan="4">Address: 000FCh</td></tr>
<tr><td colspan="4">ASL Storage.

This software scratch register only needs to be read/write accessible. The exact bit register usage must be worked out in common between System BIOS and driver software, but storage for switching/indicating up to 6 devices is possible with this amount.
For each device, the ASL control method with require two bits for _DOD (BIOS detectable yes or no, VGA/NonVGA), one bit for _DGS (enable/disable requested), and two bits for _DCS (enabled now/disabled now, connected or not).</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td colspan="2" align="center">**Description**</td></tr>
<tr><td>0</td><td>31:0</td><td colspan="2">**SCRATCH**
<table><tr><td>Default Value:</td><td>00000000h</td></tr><tr><td>Access:</td><td>R/W</td></tr></table>This register provides a means for the BIOS to communicate with the driver. This definition of this scratch register is worked out in common between System BIOS and driver software. Storage for up to 6 devices is possible. For each device, the ASL control method requires two bits for _DOD (BIOS detectable yes or no, VGA/NonVGA), one bit for _DGS (enable/disable requested), and two bits for DCS (enabled now/disabled now, connected or not).</td></tr>
</table>

ASYNC_SLICE_COUNT

ASYNC_SLICE_COUNT - ASYNC_SLICE_COUNT	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000280
Size (in bits):	32
Address:	0A204h

Async Slice Count Select Register

DWord	Bit	Description
0	31:11	**Reserved** Default Value: 00000h Access: RO Reserved
	10:8	**Async_SS** Default Value: 010b Access: R/W Number of subslices to power (Async Mode): 001 : 1 subslice 010 : 2 subslices (GT1-based CHV, BSW only) Actual SSs used = Async_SS if SScountEn=0 Actual SSs used = SScount if SScountEn=1
	7:4	**Async_EU** Default Value: 1000b Access: R/W Maximum number of EUs to power per subslice if multiple subslices enabled Async Mode Actual EUs used = Async_EU if EUmin < Async_EU < EUmax Actual EUs used = EUmax if Async_EU >= EUmax Actual EUs used = EUmin if EUmin >= Async_EU
	3	**Reserved** Default Value: 0b Access: RO Reserved
	2:0	**temp_slicecount** Default Value: 000b Access: R/W Slice Count Request in Asynchronous Mode.

Auto Draw End Offset

3DPRIM_END_OFFSET - Auto Draw End Offset		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	02420h-02423h	
Valid Projects:		
DWord	**Bit**	**Description**
0	31:0	**End Offset**
		Format: U32
		This register is used to store the end offset value used by the Vertex Fetch to determine when to stop processing the 3D_PRIMITIVE command. This register is valid when the End Offset Enable is set in the 3D_PRIMITIVE command.

Base of Data Stolen Memory

BDSM - Base of Data Stolen Memory	
Register Space:	PCI: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0005Ch

This register contains the base address of Graphics Data Stolen DRAM memory.
Graphics Stolen Memory is within DRAM space. The base of stolen memory will always be below 4G.

DWord	Bit	Description
0	31:20	**BDSM**
		<table><tr><td>Default Value:</td><td>000h</td></tr><tr><td>Access:</td><td>R/W Lock</td></tr></table> BDSM: BASE_OF_Data_STOLEN_MEMORY. This register contains bits 31 to 20 of the base address of Data stolen DRAM memory. For certain GTLC generated accesses, this base register will be added to GTLC-provided offset address, forming the full physical address for the PFI fabric. This is also used as a base for VGA paged accesses.
	19:1	**RESERVED**
		<table><tr><td>Default Value:</td><td>00000h</td></tr><tr><td>Access:</td><td>RO</td></tr></table> Reserved
	0	**BDSM_LOCK**
		<table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W Lock</td></tr></table> This bit will lock all writable settings in this register, including itself.

Base of GTT Stolen Memory

<table>
<tr><td colspan="3" align="center">**BGSM - Base of GTT Stolen Memory**</td></tr>
<tr><td colspan="3">Register Space: PCI: 0/2/0
Project: CHV, BSW
Source: PRM
Default Value: 0x00000000
Size (in bits):   32</td></tr>
<tr><td colspan="3">Address: 00070h</td></tr>
<tr><td colspan="3">Base of GTT table in Gfx Stolen Memory
The GTT table is located within Graphics Stolen Memory in DRAM space. The base of stolen memory will always be below 4G.</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td>**Description**</td></tr>
<tr><td>0</td><td>31:20</td><td>**BGSM**

<table><tr><td>Default Value:</td><td>000h</td></tr><tr><td>Access:</td><td>R/W Lock</td></tr></table>
BGSM: Gfx Base of GTT Stolen Memory. This register contains bits 31 to 20 of the base address of GTT Table in stolen DRAM memory.
BIOS determines base of GTT stolen memory by subtracting the GTT graphics stolen memory size (PCI offset 50 bits 9:8) from the
Graphics Base of Data stolen(PCI offset 5C bits 31:20).</td></tr>
<tr><td></td><td>19:1</td><td>**RESERVED**

<table><tr><td>Default Value:</td><td>00000h</td></tr><tr><td>Access:</td><td>RO</td></tr></table>
Reserved</td></tr>
<tr><td></td><td>0</td><td>**BGSM_LOCK**

<table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W Lock</td></tr></table>
This bit will lock all writeable settings in this register including itself</td></tr>
</table>

Batch Address Difference Register

<table>
<tr><td colspan="2" align="center">**BB_ADDR_DIFF - Batch Address Difference Register**</td></tr>
<tr><td>Register Space:</td><td>MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td>CHV, BSW</td></tr>
<tr><td>Source:</td><td>PRM</td></tr>
<tr><td>Default Value:</td><td>0x00000000</td></tr>
<tr><td>Access:</td><td>R/W</td></tr>
<tr><td>Size (in bits):</td><td>32</td></tr>
<tr><td>Address:
Name:
ShortName:</td><td>02154h-02157h
Batch Address Difference Register
BB_ADDR_DIFF_RCSUNIT</td></tr>
<tr><td>Address:
Name:
ShortName:</td><td>12154h-12157h
Batch Address Difference Register
BB_ADDR_DIFF_VCSUNIT0</td></tr>
<tr><td>Address:
Name:
ShortName:</td><td>1A154h-1A157h
Batch Address Difference Register
BB_ADDR_DIFF_VECSUNIT</td></tr>
<tr><td>Address:
Name:
ShortName:</td><td>1C154h-1C157h
Batch Address Difference Register
BB_ADDR_DIFF_VCSUNIT1</td></tr>
<tr><td>Address:
Name:
ShortName:</td><td>22154h-22157h
Batch Address Difference Register
BB_ADDR_DIFF_BCSUNIT</td></tr>
<tr><td colspan="2">This register contains the difference between the start of the last batch and where the last initiated Batch Buffer is currently fetching commands.</td></tr>
</table>

Programming Notes
Programming Restriction: This register should NEVER be programmed by driver, this is for HW internal use only.

DWord	Bit	Description
0	31:2	**Batch Buffer Address Difference**
		<table><tr><td>Format:</td><td>GraphicsAddress[31:2]</td></tr></table> This field specifies the DWord-aligned difference between the starting address of the batch buffer and where the last initiated Batch Buffer is currently fetching commands.
	1:0	**Reserved**
		<table><tr><td>Format:</td><td>MBZ</td></tr></table>

Batch Buffer Head Pointer Preemption Register

BB_PREEMPT_ADDR - Batch Buffer Head Pointer Preemption Register	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02148h-0214Bh
Name:	Batch Buffer Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_RCSUNIT
Address:	12148h-1214Bh
Name:	Batch Buffer Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_VCSUNIT0
Address:	1A148h-1A14Bh
Name:	Batch Buffer Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_VECSUNIT
Address:	1C148h-1C14Bh
Name:	Batch Buffer Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_VCSUNIT1
Address:	22148h-2214Bh
Name:	Batch Buffer Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_BCSUNIT

Description
This register gets updated with the DWord-aligned graphics memory address of the PREEMPTABLE command in the batch buffer on which preemption has occurred.
This register gets updated with the DWord-aligned graphics memory address of the command following the MI_BATCH_START corresponding to the second level batch buffer, when the preemption has occurred in the second level batch buffer.
This register value should be looked at only when the preemption has occurred in the batch buffer. This is indicated by "Ring/Batch Indicator" in "RING_BUFFER_HEAD_PREEMPT_REG". This register value retains its previous value and doesn't change when the preemption occurs on a preemptable command in ring buffer. Preemption is triggered by valid UHPTR in ring buffer mode of scheduling and by a pending execlist in Exec-List mode of scheduling. Note that this register is only for debug mode in ExecList mode of scheduling. This is a global register and context save/restored as part of power context image.

BB_PREEMPT_ADDR - Batch Buffer Head Pointer Preemption Register

Preemptable Commands	Source
MI_ARB_CHECK 3D_PRIMITIVE GPGPU_WALKER MEDIA_STATE_FLUSH PIPE_CONTROL (Only in GPGPU mode of pipeline selection) MI_ATOMIC (Post Sync Operation set in GPGPU mode of pipeline selection) MI_SEMAPHORE_SIGNAL (Post Sync Operation set in GPGPU mode of pipeline selection)	RenderCS

Programming Notes
Programming Restriction: This register should NEVER be programmed by driver, this is for HW internal use only.

DWord	Bit	Description
0	31:2	**Batch Buffer Head Pointer**
		Format: GraphicsAddress[31:2]
		This field specifies the DWord-aligned Graphics Memory Address of the PREEMPTABLE command in a batch buffer where the Preemption has occurred.
	1:0	**Reserved**
		Format: MBZ

Batch Buffer Head Pointer Register

BB_ADDR - Batch Buffer Head Pointer Register	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	02140h-02143h
Name:	Batch Buffer Head Pointer Register
ShortName:	BB_ADDR_RCSUNIT
Address:	12140h-12143h
Name:	Batch Buffer Head Pointer Register
ShortName:	BB_ADDR_VCSUNIT0
Address:	1A140h-1A143h
Name:	Batch Buffer Head Pointer Register
ShortName:	BB_ADDR_VECSUNIT
Address:	1C140h-1C143h
Name:	Batch Buffer Head Pointer Register
ShortName:	BB_ADDR_VCSUNIT1
Address:	22140h-22143h
Name:	Batch Buffer Head Pointer Register
ShortName:	BB_ADDR_BCSUNIT

This register contains the current DWord Graphics Memory Address of the last-initiated batch buffer.

Programming Notes
Programming Restriction: This register should NEVER be programmed by driver. This is for HW internal use only.

DWord	Bit	Description
0	31:2	**Batch Buffer Head Pointer** <table><tr><td>Project:</td><td>CHV, BSW</td></tr><tr><td>Format:</td><td>GraphicsAddress[31:2]</td></tr></table> This field specifies the DWord-aligned Graphics Memory Address where the last initiated Batch Buffer is currently fetching commands. If no batch buffer is currently active, the Valid bit will be 0 and this field will be meaningless.
	1	**Reserved** <table><tr><td>Format:</td><td>MBZ</td></tr></table>

BB_ADDR - Batch Buffer Head Pointer Register

	0	**Valid**

Format:	U1

Value	Name	Description
0h	Invalid **[Default]**	Batch buffer Invalid
1h	Valid	Batch buffer Valid

Batch Buffer Per Context Pointer

BB_PER_CTX_PTR - Batch Buffer Per Context Pointer	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	021C0h-021C3h
Name:	Batch Buffer Per Context Pointer
ShortName:	BB_PER_CTX_PTR_RCSUNIT
Address:	121C0h-121C3h
Name:	Batch Buffer Per Context Pointer
ShortName:	BB_PER_CTX_PTR_VCSUNIT0
Address:	1A1C0h-1A1C3h
Name:	Batch Buffer Per Context Pointer
ShortName:	BB_PER_CTX_PTR_VECSUNIT
Address:	1C1C0h-1C1C3h
Name:	Batch Buffer Per Context Pointer
ShortName:	BB_PER_CTX_PTR_VCSUNIT1
Address:	221C0h-221C3h
Name:	Batch Buffer Per Context Pointer
ShortName:	BB_PER_CTX_PTR_BCSUNIT

This register is used to program the batch buffer address to be executed between context restore and execution of ring/execution list if enabled. This will only get executed due to regular context save/restore and not during power restore. This register is part of the execution list context and will be executed per context. Only supported if execution list is enabled. There is no preempting workloads within the Per Context Batch Buffer.

Source
BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS
RenderCS
RenderCS
RenderCS

BB_PER_CTX_PTR - Batch Buffer Per Context Pointer

Workaround

Workaround: [Render CS Only][Execlist Mode of Scheduling]: SW must ensure arbitration is switched off while context restore is in progress for any given context. This is achieved by disabling arbitration by programming MI_ARB_ON_OFF to "Arbitration Disable" in RCS_INDIRECT_CTX buffer and by enabling back the arbitration by programming MI_ARB_ON_OFF to "Arbitration Enable" as the last command prior to MI_BATCH_END in the BB_PER_CTX_PTR buffer of every context submitted. Note that RCS_INDIRECT_CTX_OFFSET could be set to default value or any other legitimate value as per the programming notes of the register definition. Arbitration disable by programming MI_ARB_ON_OFF (Arbitration Disabled) in RCS_INDIRECT_CTX buffer. Arbitration enabled by programming MI_ARB_ON_OFF (Arbitration Enabled) as the last command prior to MI_BATCH_BUFFER_END in BB_PER_CTX_PTR buffer. Additional Note: This WA need not be applied when it is guaranteed for no preemption to occur during execution of GPGPU workload. Preemption of GPGPU workload can be avoided by Bracketing the GPGPU workload with MI_ARB_ON_OFF (Arbitration Disable) and MI_ARB_ON_OFF (Arbitration Enable) command. MI_ARB_ON_OFF is a privileged command and can only be programmed in ring buffer or in privileged batch buffer (batch buffer in GGTT memory). Pending execlist submitted must not trigger preemption of the ongoing GPGPU workload due to following reasons First context of the pending execlist submitted is not the same as the ongoing GPGPU context. Force restore bit set for the submitted pending execlist.

Workaround:
To work around a known HW issue, SW must do the below Programming Sequence prior to programming MI_BATCH_BUFFER_END command in BB_PER_CTX_PTR. SW must ensure both MI_LOAD_REGISTER_REG and MI_BATCH_BUFFER_END commands mentioned in the below sequence are placed in the same cacheline of memory.

1. MI_LOAD_REGISTER_IMM: 0x00800000 à 0x20C0

2. MI_ATOMIC

    a. Set "CS STALL" (Dword0[17])
    b. "Return Data Control" enabled (Dword0[16])
    c. "ATOMIC OPCODE" set to LOAD operation (Dword0[15:8]= 0x4)
    d. "Memory Address" set to scratch space in GFX memory.
    e. "Operand1 Data Dword 0" must be programmed to 0x0080_0080

3. MI_LOAD_REGISTER_MEM

    a. Set "Async Mode Enable" (Dword0[21])
    b. "Memory Address" set to same as in MI_ATOMIC command above.
    c. "Register Address" set to 0x20C0

4. MI_LOAD_REGISTER_REG: 0x215C à 0x215C

5. MI_BATCH_BUFFER_END   // Note that there shouldn't be any commands programmed between step4 & step5 and also these commands must be placed in the same cacheline of memory.

Additional Note:

BB_PER_CTX_PTR - Batch Buffer Per Context Pointer

This workaround need not be applied when Resource Streamer (RS) is not enabled or when a Resource Streamer enabled context is guaranteed not to be preempted.
• Preemption of RS enabled workload can be avoided by
• Bracketing the RS enabled workload with MI_ARB_ON_OFF (Arbitration Disable) and MI_ARB_ON_OFF (Arbitration Enable) command. MI_ARB_ON_OFF is a privileged command and can only be programmed in ring buffer or in privileged batch buffer (batch buffer in GGTT memory).
• Pending execlist submitted must not trigger preemption of the ongoing RS enabled workload due to following reasons
• First context of the pending execlist submitted is not the same as the ongoing RS enabled context.
• Force restore bit set for the submitted pending execlist.

DWord	Bit	Description
0	31:12	**Batch Buffer Per Context Address**
		Format: U20
		Pointer to the Context in memory to be executed as a batch.
	11:2	**Reserved**
		Format: MBZ
	1	**RS Enabled Batch Buffer Per Context**
		Format: U1
		If set, the command stream will enable the RS to parse commands.
		Programming Notes
		This must be set when programming the resource streamer pool commands (3DSTATE_BINDING_TABLE_POOL_ALLOC, 3DSTATE_GATHER_POOL_ALLOC, and 3DSTATE_DX9_CONSTANT_BUFFER_POOL_ALLOC) in order for the pool alloc fields to be valid in both the render engine and resource streamer.
	0	**Batch Buffer Per Context Valid**
		Format: U1
		If set, the command stream will execute the context from the **Batch Buffer Per Context Address** prior to the execution of actual submitted workloads.

		BB_START_ADDR - Batch Buffer Start Head Pointer Register	
		This bit is set by: • Ctx restore of this bit • MI_RS_CONTROL_STOP (except for the ctx restore command) This bit is cleared by: • MI_RS_CONTROL_START • Any Batch start except resubmitted RS batch • A batch end that doesn't include preemption • Ctx save Writing 0 to bit[0] of the RS STATUS register	
	0	**Reserved**	
		Format:	MBZ

Batch Buffer Start Head Pointer Register for Upper DWord

BB_START_ADDR_UDW - Batch Buffer Start Head Pointer Register for Upper DWord	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02170h
Address:	12170h-12173h
Name:	Batch Buffer Start Upper Head Pointer Register
ShortName:	BB_START_ADDR_UDW_VCSUNIT0
Address:	1A170h-1A173h
Name:	Batch Buffer Start Upper Head Pointer Register
ShortName:	BB_START_ADDR_UDW_VECSUNIT
Address:	1C170h-1C173h
Name:	Batch Buffer Start Upper Head Pointer Register
ShortName:	BB_START_ADDR_UDW_VCSUNIT1
Address:	22170h-22173h
Name:	Batch Buffer Start Upper Head Pointer Register
ShortName:	BB_START_ADDR_UDW_BCSUNIT

This register contains the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space specified in the last MI_START_BATCH_BUFFER command.

Programming Notes
Programming Restriction: This register should NEVER be programmed by driver, this is for HW internal use only.

DWord	Bit	Description	
0	31:16	**Reserved**	
		Format:	MBZ
	15:0	**Batch Buffer Start Head Pointer Upper DWORD**	
		Format:	GraphicsAddress[47:32]
		This field specifies the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space for the last initiated Batch Buffer starting address.	

Batch Buffer State Register

BB_STATE - Batch Buffer State Register	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000 CHV, BSW
Access:	RO
Size (in bits):	32

Address:	02110h-02113h
Name:	Batch Buffer State Register
ShortName:	BB_STATE_RCSUNIT

Address:	12110h-12113h
Name:	Batch Buffer State Register
ShortName:	BB_STATE_VCSUNIT0

Address:	1A110h-1A113h
Name:	Batch Buffer State Register
ShortName:	BB_STATE_VECSUNIT

Address:	1C110h-1C113h
Name:	Batch Buffer State Register
ShortName:	BB_STATE_VCSUNIT1

Address:	22110h-22113h
Name:	Batch Buffer State Register
ShortName:	BB_STATE_BCSUNIT

This register contains the attributes of the current batch buffer initiated from the Ring Buffer.

This register should not be written by software. These fields should only get written by a context restore. Software should always set these fields via the MI_BATCH_BUFFER_START command when initiating a batch buffer. This register is saved and restored with context.

DWord	Bit	Description	
0	31:8	**Reserved**	
		Project:	All
		Format:	MBZ
	7	**Reserved**	
		Project:	All
		Source:	BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS
		Format:	MBZ

BB_STATE - Batch Buffer State Register

	7	**Resource Streamer Enable**	
		Project:	CHV, BSW
		Source:	RenderCS
		Format:	U1

When this bit is set, the Resource Streamer will execute the batch buffer. When this bit is clear the Resource Streamer will not execute the batch buffer.

	6	**Reserved**	

	6	**2nd Level Buffer Security Indicator**	
		Project:	CHV, BSW
		Source:	VideoCS, VideoCS2
		Exists If:	//VCS, VCS2

If set, VCS is fetching 2nd level batch commands from a PPGTT address space. If clear, GGTT. If execlists are enabled and this is set, the batch buffer is non-secure and cannot execute privileged commands nor access privileged (GGTT) memory. It will be accessed via the PPGTT. If clear, this batch buffer is secure and will be accessed via the GGTT. Note: When execlists are enabled this field reflects the effective security level and may not be the same as the Buffer Security Indicator written using MI_BATCH_BUFFER_START.

Value	Name	Description
0h	MIBUFFER_SECURE **[Default]**	Located in GGTT memory
1h	MIBUFFER_NONSECURE	Located in PPGTT memory

	6	**2nd Level Buffer Security Indicator**	
		Project:	CHV, BSW
		Source:	BlitterCS, VideoEnhancementCS
		Exists If:	//BCS, VECS
		Format:	MI_2ndBufferSecurityType

If set, VECS is fetching 2nd level batch commands from a PPGTT address space. If clear, GGTT. If execlists are enabled and this is set, the batch buffer is non-secure and cannot execute privileged commands nor access privileged (GGTT) memory. It will be accessed via the PPGTT. If clear, this batch buffer is secure and will be accessed via the GGTT.

Value	Name	Description
0h	MIBUFFER_SECURE **[Default]**	Located in GGTT memory
1h	MIBUFFER_NONSECURE	Located in PPGTT memory

Programming Notes
When execlists are enabled, this field reflects the effective security level and may not be the same as the Buffer Security Indicator written using MI_BATCH_BUFFER_START.

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BB_STATE - Batch Buffer State Register

	5	**Address Space Indicator**		
		Project:		CHV, BSW
		Note: This field reflects the effective address space indicator security level and may not be the same as the Address Space Indicator written using MI_BATCH_BUFFER_START.		
		Value	**Name**	**Description**
		0h	GGTT **[Default]**	This Batch buffer is located in GGTT memory and is privileged
		1h	PPGTT	This Batch buffer is located in PPGTT memory and is non-privileged.
	4	**Reserved**		
	4	**Reserved**		
		Project:		All
		Source:		BlitterCS
		Exists If:		//BCS
		Format:		MBZ
	3:0	**Reserved**		
		Project:		All
		Format:		MBZ

Batch Buffer Upper Head Pointer Preemption Register

BB_PREEMPT_ADDR_UDW - Batch Buffer Upper Head Pointer Preemption Register	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	0216Ch-0216Fh
Name:	Batch Buffer Upper Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_UDW_RCSUNIT
Address:	1216Ch-1216Fh
Name:	Batch Buffer Upper Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_UDW_VCSUNIT0
Address:	1A16Ch-1A16Fh
Name:	Batch Buffer Upper Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_UDW_VECSUNIT
Address:	1C16Ch-1C16Fh
Name:	Batch Buffer Upper Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_UDW_VCSUNIT1
Address:	2216Ch-2216Fh
Name:	Batch Buffer Upper Head Pointer Preemption Register
ShortName:	BB_PREEMPT_ADDR_UDW_BCSUNIT

This register contains the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space of the last preempted batch buffer. This register follows the same rules as the BB_PREEMPT_ADDR register.

Programming Notes
Programming Restriction: This register should NEVER be programmed by driver, this is for HW internal use only.

DWord	Bit	Description
0	31:16	**Reserved**
		Format: MBZ
	15:0	**Batch Buffer Head Pointer Upper DWORD**
		Format: GraphicsAddress[47:32]
		This field specifies the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space of the last preempted batch buffer.

Batch Buffer Upper Head Pointer Register

BB_ADDR_UDW - Batch Buffer Upper Head Pointer Register	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	02168h-0216Bh
Name:	Batch Buffer Upper Head Pointer Register
ShortName:	BB_ADDR_UDW_RCSUNIT
Address:	12168h-1216Bh
Name:	Batch Buffer Upper Head Pointer Register
ShortName:	BB_ADDR_UDW_VCSUNIT0
Address:	1A168h-1A16Bh
Name:	Batch Buffer Upper Head Pointer Register
ShortName:	BB_ADDR_UDW_VECSUNIT
Address:	1C168h-1C16Bh
Name:	Batch Buffer Upper Head Pointer Register
ShortName:	BB_ADDR_UDW_VCSUNIT1
Address:	22168h-2216Bh
Name:	Batch Buffer Upper Head Pointer Register
ShortName:	BB_ADDR_UDW_BCSUNIT

This register contains the current Upper DWord of Graphics Memory Address of the last-initiated batch buffer.
Programming Restriction:
This register should NEVER be programmed by driver. This is for HW internal use only.

DWord	Bit	Description
0	31:16	**Reserved**
		Format: MBZ
	15:0	**Batch Buffer Head Pointer Upper DWORD**
		Format: GraphicsAddress[47:32]
		This field specifies the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space where the last initiated Batch Buffer is currently fetching commands. If no batch buffer is currently active, the Valid bit in BB_ADDR will be 0 and this field is meaningless.

Batch Offset Register

BB_OFFSET - Batch Offset Register	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000001
Access:	R/W
Size (in bits):	32

Address:	02158h-0215Bh
Name:	Batch Offset Register
ShortName:	BB_OFFSET_RCSUNIT

Address:	12158h-1215Bh
Name:	Batch Offset Register
ShortName:	BB_OFFSET_VCSUNIT0

Address:	1A158h-1A15Bh
Name:	Batch Offset Register
ShortName:	BB_OFFSET_VECSUNIT

Address:	1C158h-1C15Bh
Name:	Batch Offset Register
ShortName:	BB_OFFSET_VCSUNIT1

Address:	22158h-2215Bh
Name:	Batch Offset Register
ShortName:	BB_OFFSET_BCSUNIT

Description	Source
This register contains the offset value to be added to the Batch Buffer Start Address in the MI_BATCH_BUFFER_START command when the Enable Offset bit in MI_BATCH_BUFFER_START command is set.	
Preemptable Commands • MI_ARB_CHECK • 3D_PRIMITIVE • GPGPU_WALKER • MEDIA_STATE_FLUSH • PIPE_CONTROL (Only in GPGPU mode of pipeline selection) • MI_ATOMIC (Post Sync Operation set in GPGPU mode of pipeline selection) • MI_SEMAPHORE_SIGNAL (Post Sync Operation set in GPGPU mode of pipeline selection)	RenderCS

BB_OFFSET - Batch Offset Register

Programming Notes
On preemption occurring whith in a primary/chain batch buffer this register is loaded with the offset value of the preempted command header from the batch start address when the Enable Load is set. Preemption of 3D or GP_GPU workloads can only occur on preemptable commands. Batch buffer offset always points to the preemptable command if preempted on preemption or the immediate command following it if not preempted on preemption. Note that this register is only for debug mode in ExecList mode of scheduling. EX: Preemption occurs on 3D_PRIMITVE command • If the 3D_PRIMTIVE command is completely processed by render pipe then the BB_OFFSET points to the command following 3D_PRIMITIVE • If the 3D_PRIMTIVE command is not completely processed by render pipe then the BB_OFFSET points to the 3D_PRIMITIVE command.

DWord	Bit	Description
0	31:2	**Batch Buffer Offset**
		<table><tr><td>Format:</td><td>GraphicsAddress[31:2]</td></tr></table> This field specifies the DWord-aligned offset between the starting address of the batch buffer and where the last initiated Batch Buffer is currently fetching commands.
	1	**Reserved**
		<table><tr><td>Format:</td><td>MBZ</td></tr></table>
	0	**Enable Load**
		<table><tr><td>Default Value:</td><td>1</td></tr><tr><td>Format:</td><td>Enable</td></tr></table> <table><tr><td>Description</td></tr><tr><td>If this bit is set then the Batch Buffer Offset is loaded with the preempted command offset or the following command whenever a batch buffer is ended due to a Preemptable command.</td></tr></table>

BCS_PREEMPTION_HINT

BCS_PREEMPTION_HINT - BCS_PREEMPTION_HINT
Register Space: MMIO: 0/2/0
Project: CHV, BSW
Source: BlitterCS
Default Value: 0x00000000
Access: R/W
Size (in bits): 32
Address: 224BCh

This register contains the Head pointer offset in to the Ring Buffer or the Dword aligned Graphics address in to the Batch Buffer corresponding to either MI_ARB_CHECK called Preemption Hint Address. When Preemption Hint Address is enabled, BCS will honor UHPTR only on parsing MI_ARB_CHK at Preemption Hint Address.

This register contains the Head pointer offset into the Ring Buffer or the Dword aligned Graphics address into the Batch Buffer corresponding to the below listed commands in execlist mode of operation

- MI_ARB_CHECK
- MI_WAIT_FOR_EVENT
- MI_SEMAPHORE_WAIT

Programming Notes

Programming Restriction: This register should NEVER be programmed in functional mode, this should be used only in validation mode to achieve deterministic behavior of UHPTR being sampled by a given MI_ARB_CHECK in command stream. Programmer has to ensure that BCS Preemption Hint register gets programmed before UHPTR is programmed and well before BCS crosses the corresponding execution point. Preemption hint for both RingBuffer and Batch Buffer can't be enabled simultaneously.

DWord	Bit	Description
0	31:2	**Preempted Hint Address**
		Format: U30
		Format: GraphicsAddress[31:2]
		This field contains the Head offset in to the Ring Buffer when Preemption Hint is set to Ring Buffer and Dword aligned Graphics Address in to the batch buffer when Preemption Hint is set to Batch Buffer.
	1	**Batch Buffer Preemption Hint**
		Format: Enable

Value	Name	Description
0h	Disabled	Preemption hint is disabled in batch buffer.
1h	Enabled	Preemption hint is enabled in ring buffer and preemption hint address corresponds to the instruction in Batch Buffer.

BCS_PREEMPTION_HINT - BCS_PREEMPTION_HINT

0	**Ring Preemption Hint**		

Format:	Enable

Value	Name	Description
0h	Disable	Preemption hint is disabled in ring buffer.
1h	Enabled	Preemption hint is enabled in ring buffer and preemption hint address corresponds to the instruction in Ring Buffer.

BCS_PREEMPTION_HINT_UDW

BCS_PREEMPTION_HINT_UDW - BCS_PREEMPTION_HINT_UDW

Register Space: MMIO: 0/2/0

Project: CHV, BSW

Source: BlitterCS

Default Value: 0x00000000

Access: R/W

Size (in bits):   32

Address: 224C8h

This register contains the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space of the Batch Buffer corresponding to MI_ARB_CHECK command called Preemption Hint Address.

Programming Notes

Programming Restriction: This register should NEVER be programmed in functional mode, this should be used only in validation mode to achieve deterministic behavior of UHPTR being sampled by a given MI_ARB_CHK in command stream.

DWord	Bit	Description
0	31:16	**Reserved** Format: MBZ
	15:0	**Preempted Hint Address Upper DWORD** Format: GraphicsAddress[47:32] This field contains the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space of the batch buffer when Preemption Hint is set to Batch Buffer. This field is not valid when Preemption Hint is set to Ring Buffer.

BCS Active Upper Head Pointer Register

BCS_ACTHD_UDW - BCS Active Upper Head Pointer Register	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	BlitterCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	2205Ch

This register contains the Head "Pointer" (4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space) of the currently-active batch buffer.

DWord	Bit	Description	
0	31:16	**Reserved**	
		Format:	MBZ
	15:0	**Head Pointer Upper DWORD**	
		Default Value:	0h
		Format:	GraphicsAddress[47:32]
		4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space corresponding to the Head Pointer of the currently-active batch buffer.	

BCS Context ID Preemption Hint

BCS_CTXID_PREEMPTION_HINT - BCS Context ID Preemption Hint	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	BlitterCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	224CCh

This register contains the Context ID of a context in execlist mode of operation. In execlist mode of operation BCS_PREEMPTION_HINT registers are looked at by Blitter Command Streamer on executing a context having Context ID that matches with the contents of this register. This register contents are valid and looked at only in execlist mode of operation.

Programming Notes
This register should NEVER be programmed in functional mode, this must be used only in validation mode to achieve deterministic preemption behavior in execlist mode of operation.

DWord	Bit	Description
0	31:0	**Context ID Preemption Hint**
		Format: U32
		If 0 this field has no effect. If nonzero it indicates the only context ID that can be preempted when execlists are enabled. A preemption attempt when the context ID of the currently executing ring context does not match this field will be ignored.

BCS Context Sizes

<table>
<tr><td colspan="3" align="center">**BCS_CXT_SIZE - BCS Context Sizes**</td></tr>
<tr><td colspan="3">Register Space: MMIO: 0/2/0</td></tr>
<tr><td colspan="3">Project: CHV, BSW</td></tr>
<tr><td colspan="3">Source: BlitterCS</td></tr>
<tr><td colspan="3">Default Value: 0x00000A05 CHV, BSW</td></tr>
<tr><td colspan="3">Access: Read/32 bit Write Only</td></tr>
<tr><td colspan="3">Size (in bits):   32</td></tr>
<tr><td colspan="3">Address: 221A8h</td></tr>
</table>

DWord	Bit	Description
0	31:13	**Reserved** Project: All Format: MBZ
	12:8	**BCS Context Size** Project: All Format: U5 Value: Ah, Name: [Default], Project: CHV, BSW
	7:5	**Reserved** Project: All Format: MBZ
	4:0	**Execlist Context Size** Project: CHV, BSW Format: U5 Value: 5h, Name: [Default], Project: CHV, BSW

BCS Context Timestamp Count

BCS_CTX_TIMESTAMP - BCS Context Timestamp Count	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	BlitterCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	223A8h

This register provides a mechanism to obtain cumulative run time of a GPU context on HW. This register gets context save/restored on a context switch. SW must reset this register on very first submission of a context to HW, then afterwards gets context save/restored maintaining the cumulative run time of the corresponding context. Note that the value of this register can be obtained in a 3D pipeline-synchronous fashion without a pipeline flush by using the PIPE_CONTROL command. See 3D Geometry Pipeline in the "3D and Media" volume. This register (effectively) counts at a constant frequency by adjusting the increment amount according to the actual reference clock frequency. SW therefore does not need to know the reference clock frequency. This register gets reset on an engine reset.

This register is context save restore on a context switch.

DWord	Bit	Description
0	31:0	**Timestamp Value**
		Format: U32
		This register increments for every 80 ns of time.

BCS Counter for the Blitter Engine

BCS_CNTR - BCS Counter for the Blitter Engine		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	BlitterCS	
Default Value:	0xFFFFFFFF	
Access:	R/W	
Size (in bits):	32	
Address:	22178h	

DWord	Bit	Description	
0	31:0	**Count Value**	
		Default Value:	ffffffffh
		Writing a Zero value to this register starts the counting. Writing a Value of FFFF FFFF to this counter stops the counter.	

BCS Error Identity Register

BCS_EIR - BCS Error Identity Register	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	BlitterCS
Default Value:	0x00000000
Access:	R/WC
Size (in bits):	32
Address:	220B0h

The EIR register contains the persistent values of Hardware-Detected Error Condition bits. Any bit set in this register will cause the Master Error bit in the ISR to be set. The EIR register is also used by software to clear detected errors (by writing a '1' to the appropriate bit(s) except for the unrecoverable bits described).).

DWord	Bit	Description
0	31:16	**Reserved**
		Project: All
		Format: MBZ
	15:0	**Error Identity Bits**

Project: All

Format: Array of Error condition bits See Table 1 5. Hardware-Detected Error Bits

This register contains the persistent values of ESR error status bits that are unmasked via the EMR register. The logical OR of all (defined) bits in this register is reported in the Master Error bit of the Interrupt Status Register. To clear an error condition, software must first clear the error by writing a '1' to the appropriate bit(s) in this field. If required, software should then proceed to clear the Master Error bit of the IIR.

Value	Name	Description
0h	**[Default]**	
1h	Error occurred	Error occurred

Programming Notes
Writing a '1' to a set bit will cause that error condition to be cleared. However, the Instruction Error bit (Bit 0) cannot be cleared except by reset (i.e., it is a fatal error).

BCS Error Mask Register

BCS_EMR - BCS Error Mask Register	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	BlitterCS
Default Value:	0xFFFFFFFF CHV, BSW
Access:	R/W
Size (in bits):	32
Address:	220B4h

The EMR register is used by software to control which Error Status Register bits are "masked" or "unmasked". "Unmasked" bits will be reported in the EIR, thus setting the Master Error ISR bit and possibly triggering a CPU interrupt, and will persist in the EIR until cleared by software. "Masked" bits will not be reported in the EIR and therefore cannot generate Master Error conditions or CPU interrupts.

Undefined or reserved bits in the Hardware Detected Error Bit Table will always return a read value of '1'

DWord	Bit	Description
0	31:16	**Reserved**
			Default Value:	FFFFh	
			Project:	CHV, BSW	
			Format:	Must Be One	
	15:0	**Error Mask Bits**
			Project:	All	
			Format:	Array of error condition mask bits See Table 1 5. Hardware-Detected Error Bits	
		This register contains a bit mask that selects which error condition bits (from the ESR) are reported in the EIR.

Value	Name	Description
0000h	Not Masked	Will be reported in the EIR
FFFFh	Masked **[Default]**	Will not be reported in the EIR

BCS Error Status Register

<table>
<tr><th colspan="3">BCS_ESR - BCS Error Status Register</th></tr>
<tr><td colspan="3">Register Space: MMIO: 0/2/0</td></tr>
<tr><td colspan="3">Project: CHV, BSW</td></tr>
<tr><td colspan="3">Source: BlitterCS</td></tr>
<tr><td colspan="3">Default Value: 0x00000000</td></tr>
<tr><td colspan="3">Access: RO</td></tr>
<tr><td colspan="3">Size (in bits):   32</td></tr>
<tr><td colspan="3">Address: 220B8h</td></tr>
<tr><td colspan="3">The ESR register contains the current values of all Hardware-Detected Error condition bits (these are all by definition "persistent"). The EMR register selects which of these error conditions are reported in the persistent EIR (i.e., set bits must be cleared by software) and thereby causing a Master Error interrupt condition to be reported in the ISR.</td></tr>
<tr><th>DWord</th><th>Bit</th><th>Description</th></tr>
<tr><td>0</td><td>31:16</td><td>**Reserved**
Project: All
Format: MBZ</td></tr>
<tr><td></td><td>15:0</td><td>**Error Status Bits**
Project: All
Format: Array of error condition bits See Table 1 5. Hardware-Detected Error Bits
This register contains the non-persistent values of all hardware-detected error condition bits.

Value / Name / Description
0h / [Default] /
1h / Error Condition Detected / Error Condition detected</td></tr>
</table>

BCS Execute Condition Code Register

BCS_EXCC - BCS Execute Condition Code Register	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	BlitterCS
Default Value:	0x00000000
Access:	R/W, RO
Size (in bits):	32
Trusted Type:	1
Address:	22028h

This register contains user defined and hardware generated conditions that are used by MI_WAIT_FOR_EVENT commands. An MI_WAIT_FOR_EVENT instruction excludes the executing ring from arbitration if the selected event evaluates to a 1, while instruction is discarded if the condition evaluates to a 0. Once excluded, a ring is enabled into arbitration when the selected condition evaluates to a 0. This register also contains control for the invalidation of indirect state pointers on context restore.

DWord	Bit	Description
0	31:16	**Mask Bits** Format: Mask[15:0] These bits serves as a write enable for bits 15:0. If this register is written with any of these bits clear the corresponding bit in the field 15:0 will not be modified. Reading these bits always returns 0s.
	15	**Reserved** Format: MBZ
	14	**Context Wait for V-blank on Pipe-C** Project: CHV, BSW This field when set indicates the corresponding context has executed MI_WAIT_FOR_EVENT with "Display Pipe C Vertical Blank Wait Enable" set. This is an internal HW flag and should not be accessed by SW.
	13	**Context Wait for V-blank on Pipe-B** Project: CHV, BSW This field when set indicates the corresponding context has executed MI_WAIT_FOR_EVENT with "Display Pipe B Vertical Blank Wait Enable" set. This is an internal HW flag and should not be accessed by SW.
	12	**Context Wait for V-blank on Pipe-A** Project: CHV, BSW This field when set indicates the corresponding context has executed MI_WAIT_FOR_EVENT with "Display Pipe A Vertical Blank Wait Enable" set. This is an internal HW flag and should not be accessed by SW.

BCS_EXCC - BCS Execute Condition Code Register

11:5	**Reserved**	
	Format:	MBZ
4:0	**Reserved**	
	Project:	CHV, BSW
	Format:	MBZ

BCS General Purpose Register

BCS_GPR - BCS General Purpose Register	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	BlitterCS
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Address:	22600h-2267Fh

This is a general purpose register bank of sixteen 64-bit registers, used as temporary storage by the MI_MATH command to do ALU operations.

Programming Notes
Any operation that initiates a read to register 0x2266C will return the value of 0x2260c register. This does not include context save or MI_MATH command operation.

DWord	Bit	Description	
0	63:0	**Reserved**	
		Format:	MBZ

BCS Hardware Status Mask Register

BCS_HWSTAM - BCS Hardware Status Mask Register	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	BlitterCS
Default Value:	0xFFFFFFFF
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	22098h

Access: RO for Reserved Control bits

The HWSTAM register has the same format as the Interrupt Control Registers. The bits in this register are "mask" bits that prevent the corresponding bits in the Interrupt Status Register from generating a "Hardware Status Write" (PCI write cycle). Any unmasked interrupt bit (HWSTAM bit set to 0) will allow the Interrupt Status Register to be written to the ISR location (within the memory page specified by the Hardware Status Page Address Register) when that Interrupt Status Register bit changes state.

Programming Notes

To write the interrupt to the HWSP, the corresponding IMR bit must also be clear (enabled). At most 1 bit can be unmasked at any given time.

DWord	Bit	Description	
0	31:0	**Hardware Status Mask Register**	
		Default Value:	FFFFFFFFh
		Project:	All
		Format:	Array of Masks
		refer to Table 5-1 in Interrupt Control Register section for bit definitions	

BCS IDLE Max Count

BCS_PWRCTX_MAXCNT - BCS IDLE Max Count	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	BlitterCS
Default Value:	0x00000040 CHV, BSW
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	22054h

This register contains the time in 0.64us to wait before telling power management hardware the render pipe is IDLE

DWord	Bit	Description
0	31:20	**Reserved**

Project:	All
Format:	MBZ

	19:0	**Blitter IDLE Wait Time**

Project:	All
Format:	Max Count

Specifies how long the command stream should wait before ensuring the pipe is IDLE and to let power management hardware know

Value	Name	Description
00040h	**[Default]**	0x00040 * 0.64us ~ 41us wait time

Programming Notes
• This is only useable if bit 0 of the PC_PSMI_CTRL is clear.
• The value in this field must be greater than 1.

BCS Idle Switch Delay

BCS_IDLEDLY - BCS Idle Switch Delay	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	BlitterCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	2223Ch

The IDLEDLY register contains an Idle Delay field which specifies the minimum number of microseconds allowed for command streamer to wait before a context is switched out leading to IDLE state in Execlist mode, i.e following this context switch there is no active element available in HW to execute.
A default value of 0, means that by default, there is no restriction to wait on a context switch leading to IDLE. This register has no significance when execlists are not enabled.

DWord	Bit	Description	
0	31:21	**Reserved**	
		Project:	All
		Format:	MBZ
	20:0	**IDLE Delay**	
		Project:	All
		Format:	U21
		Minimum number of micro-seconds allowed	

BCS Instruction Parser Mode Register

BCS_INSTPM - BCS Instruction Parser Mode Register		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	BlitterCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	220C0h	

Desc

DWord	Bit	Description
0	31:16	**Mask Bits**
		Format: Mask[15:0]
		Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)
	15:11	**Reserved**
		Project: All
		Format: MBZ
	10	**Implied Atomic Fences To Write Fences**
		Project: CHV, BSW
		Format: U1
		If set, all implied atomic fences generated by HW during various operations (Flushes, Context Switch) are converted to regular write fences. Setting this bit will affect data ordering functionality and must be only used in debug mode. When reset HW behaves as expected.
		Programming Notes
		This bit is not context save and restored. SW must set this bit through the Workaround Batch buffer in order to retain through standby and set this bit on each context submission.
	9	**Reserved**
		Project: CHV, BSW
		Format: MBZ
	8:7	**Reserved**
		Project: All
		Format: MBZ
	6:5	**Reserved**
		Project: CHV, BSW
		Format: MBZ

BCS_INSTPM - BCS Instruction Parser Mode Register

	4:0	**Reserved**	
		Project:	All
		Format:	MBZ

BCS Interrupt Mask Register

BCS_IMR - BCS Interrupt Mask Register	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	BlitterCS
Default Value:	0xFFFFFFFF
Access:	R/W
Size (in bits):	32
Address:	220A8h

The IMR register is used by software to control which Interrupt Status Register bits are "masked" or "unmasked". "Unmasked" bits will be reported in the IIR, possibly triggering a CPU interrupt, and will persist in the IIR until cleared by software. "Masked" bits will not be reported in the IIR and therefore cannot generate CPU interrupts.

DWord	Bit	Description
0	31:0	**Interrupt Mask Bits**

		Project:	All
		Format:	Array of interrupt mask bits Refer to Table 5-1 in Interrupt Control Register section for bit definitions

This field contains a bit mask which selects which interrupt bits (from the ISR) are reported in the IIR.

Value	Name	Description
FFFF FFFFh	**[Default]**	
0h	Not Masked	Will be reported in the IIR
1h	Masked	Will not be reported in the IIR

BCS Mode Register for Software Interface

BCS_MI_MODE - BCS Mode Register for Software Interface

Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	BlitterCS
Default Value:	0x00000200 CHV, BSW
Access:	R/W
Size (in bits):	32

Address:	2209Ch-2209Fh

The MI_MODE register contains information that controls software interface aspects of the command parser.

DWord	Bit	Description
0	31:16	**Masks** A 1 in a bit in this field allows the modification of the corresponding bit in Bits 15:0
	15	**Suspend Flush** <table><tr><td>Project:</td><td>All</td></tr></table>Mask: MMIO(0x209c)#31 <table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>0h</td><td>No Delay</td><td>HW will not delay flush, this bit will get cleared by MI_SUSPEND_FLUSH as well</td></tr><tr><td>1h</td><td>Delay Flush</td><td>Suspend flush is active</td></tr></table>
	14:12	**Reserved** Read/Write
	11	**Invalidate UHPTR enable** If bit set H/W clears the valid bit of BCS_UHPTR (4134h, bit 0) when current active head pointer is equal to UHPTR.
	10	**Atomic Read Return for MI_COPY_MEM_MEM** <table><tr><td>Project:</td><td>CHV, BSW</td></tr></table><table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>0h</td><td>Disable [Default]</td><td>Hardware does a regular memory fence write to complete the write to the destination address before moving to the next instruction.</td></tr><tr><td>1h</td><td>Enable</td><td>Hardware does Atomic Move with Read Return to complete the write to the destination address before moving to the next instruction.</td></tr></table>

BCS_MI_MODE - BCS Mode Register for Software Interface

	9	**Ring Idle (Read Only Status Bit)** *Writes to this bit are not allowed.*

Value	Name
0	Parser not idle
1	Parser idle **[Default]**

	8	**Stop Ring** Software must set this bit to force the Ring and Command Parser to Idle. Software must read a 1 in Ring Idle bit after setting this bit to ensure that the hardware is idle. *Software must clear this bit for Ring to resume normal operation.*

Value	Name
0	Normal Operation **[Default]**
1	Parser is turned off

	7:2	**Reserved** Read/Write

	1	**Bypass Fence Write** If set, this bit will bypass all writes during flushes, independent of programming. This includes post-sync op bits, the implicit TLB invalidate write (set in GFX_MODE[13]), and sync flush fences. *Note this is only intended for work-arounds*

Value	Name
0	Normal Operation
1	Bypass

	0	**Reserved** Read/Write

BCS PPGTT Directory Cacheline Valid Register

BCS_PP_DCLV - BCS PPGTT Directory Cacheline Valid Register	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	BlitterCS
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Address:	22220h

Default Value = 0h

This register controls update of the on-chip PPGTT Directory Cache during a context restore. Bits that are set will trigger the load of the corresponding 16 directory entry group. This register is restored with context (prior to restoring the on-chip directory cache itself). This register is also restored when switching to a context whose LRCA matches the current CCID if the Force PD Restore bit is set in the context descriptor.

The context image of this register must be updated and maintained by SW; SW should not normally need to read this register.

This register can also effectively be used to limit the size of a processes' virtual address space. Any access by a process that requires a PD entry in a set that is not enabled in this register will cause a fatal error, and no fetch of the PD entry will be attempted.

DWord	Bit	Description
0	63:32	**Reserved**
		Format: MBZ
	31:0	**PPGTT Directory Cache Restore**
		Format: Enable[32]
		[1..32] 16 entries If set, the [1st..32nd] 16 entries of the directory cache are considered valid and will be brought in on context restore. If clear, these entries are considered invalid and fetch of these entries will not be attempted.

BCS Primary DMA Engine Fetch Upper Address

BCS_DMA_FADD_P_UDW - BCS Primary DMA Engine Fetch Upper Address	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	BlitterCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	22060h

This register contains the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space of the instruction being fetched by the Primary DMA engine. This register contents are valid only when Batch Buffer is active.

DWord	Bit	Description	
0	31:16	**Reserved**	
		Format:	MBZ
	15:0	**Current DMA Address Upper DWORD**	
		Format:	GraphicsAddress[47:32]
		This field contains 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space of the batch buffer that the "Primary" instruction parser DMA engine is currently accessing (fetching). Note that this address will typically lead the Head offset (as instructions must be fetched before execution).	

BCS Reported Timestamp Count

<table>
<tr><td colspan="2" align="center">**BCS_TIMESTAMP - BCS Reported Timestamp Count**</td></tr>
<tr><td>Register Space:</td><td>MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td>CHV, BSW</td></tr>
<tr><td>Source:</td><td>BlitterCS</td></tr>
<tr><td>Default Value:</td><td>0x00000000, 0x00000000</td></tr>
<tr><td>Access:</td><td>RO. This register is not set by the context restore.</td></tr>
<tr><td>Size (in bits):</td><td>64</td></tr>
<tr><td>Address:</td><td>22358h</td></tr>
</table>

This register provides an elapsed real-time value that can be used as a timestamp. This register is not reset by a graphics reset. It will maintain its value unless a full chipset reset is performed. Note: This timestamp register reflects the value of the PCU TSC. The PCU TSC counts 10ns increments; this timestamp reflects bits 38:3 of the TSC (i.e. 80ns granularity, rolling over every 1.5 hours).

DWord	Bit	Description
0	63:36	**Reserved**
		Project: All
		Format: MBZ
	35:0	**Timestamp Value**
		Project: All
		Format: U36
		This register toggles every 80 ns. The upper 28 bits are zero.

BCS Reset Control Register

<table>
<tr><td colspan="3" align="center">**BCS_RESET_CTRL - BCS Reset Control Register**</td></tr>
<tr><td colspan="3">Register Space: MMIO: 0/2/0</td></tr>
<tr><td colspan="3">Project: CHV, BSW</td></tr>
<tr><td colspan="3">Source: BlitterCS</td></tr>
<tr><td colspan="3">Default Value: 0x00000000</td></tr>
<tr><td colspan="3">Access: R/W</td></tr>
<tr><td colspan="3">Size (in bits):   32</td></tr>
<tr><td colspan="3">Address: 220D0h</td></tr>
<tr><td colspan="3">This register is to be used to control soft reset.</td></tr>
</table>

DWord	Bit	Description
0	31:16	**Mask Bits** <table><tr><td>Format:</td><td>Mask[15:0]</td></tr></table> Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)
	15:2	**Reserved** <table><tr><td>Format:</td><td>MBZ</td></tr></table>
	1	**Ready for Reset** <table><tr><td>Format:</td><td>U1</td></tr></table> When set indicates blitter engine is ready for reset. This bit gets cleared on engine reset or when Soft Reset In progress is cleared.
	0	**Request Reset** <table><tr><td>Format:</td><td>U1</td></tr></table> When set indicates SW wishes to reset the blitter engine. On seeing this bit set Command Streamer will take appropriate action and set Ready For Reset status bit. This bit gets cleared on engine reset. This bit can also be cleared by writing "0" to this bit, this mode of clearing must be only used in debug and validation mode.

BCS Ring Buffer Next Context ID Register

BCS_RNCID - BCS Ring Buffer Next Context ID Register		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	BlitterCS	
Default Value:	0x00000000, 0x00000000	
Access:	R/W	
Size (in bits):	64	
Address:	22198h-2219Fh	
This register contains the *next* ring context ID associated with the ring buffer.		
Programming Notes		
The current context (RCCID) register can be updated indirectly from this register on a context switch event. Note that the only time a context switch can occur is when MI_ARB_CHECK enables preemption or the current context runs dry (head pointer becomes equal to tail pointer).		
DWord	**Bit**	**Description**
0	63:0	**Unnamed** See Context Descriptor for BCS

BCS Semaphore Polling Interval on Wait

BCS_SEMA_WAIT_POLL - BCS Semaphore Polling Interval on Wait	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	BlitterCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	2224Ch

The SEMA_WAIT_POLL register contains Poll Interval field which specifies the minimum number of microseconds allowed for command streamer to wait before re-fetching the data from the address mentioned in the MI_SEMAPHORE_WAIT command on WAIT Mode set to POLL until the condition is satisfied while the context is not switched out.

When value of 0 is written the poll interval will be equal to the memory latency of the read completion.

DWord	Bit	Description	
0	31:21	**Reserved**	
		Project:	All
		Format:	MBZ
	20:0	**Poll Interval**	
		Project:	All
		Format:	U21
		Minimum number of micro-seconds allowed	

BCS Sleep State and PSMI Control

BCS_PSMI_CTRL - BCS Sleep State and PSMI Control	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	BlitterCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	22050h

This register is to be used to control all aspects of PSMI and power saving functions

DWord	Bit	Description
0	31:16	**Mask Bits**
		Format: Mask[15:0]
		Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)
	15	**Reserved**
		Project: CHV, BSW
		Format: MBZ
	14:13	**Reserved**
		Project: All
		Format: MBZ
	12	**Reserved**
		Project: CHV, BSW
		Format: MBZ
	11:8	**Reserved**
		Format: MBZ
	7	**Reserved**
		Project: CHV, BSW
		Format: MBZ
	6:5	**Reserved**
		Format: MBZ

BCS_PSMI_CTRL - BCS Sleep State and PSMI Control

4	**GO Indicator**	
	Project:	All
	Access:	RO
	Format:	GO

This is a read only field. Writing to this bit is undefined. To simplify power saving and soft reset flows, the power management hardware has the ability to block all pending memory cycles of the render pipe. When GO=0, all cycles are blocked. All CPD enter/exit and RC6 enter/exit has this bit set to 0.

Value	Name	Description
0h	Disable **[Default]**	No cycles allowed coming out of IDLE. All pending memory read cycles are complete. No new cycles permitted except for power context or PSMI cycles.
1h	Enable	Normal execution

3	**IDLE Indicator**	
	Default Value:	0h Render is assumed NOT IDLE coming out of reset
	Project:	All
	Access:	RO
	Format:	IDLE

This is a read only field. Writing to this bit is undefined. This indicates what power management thinks what state the render pipe is in. That is, if set, the full handshake between render and power management has occured and most likely the render clocks are currently turned off.

2	**Reserved**	
	Project:	All

1	**Reserved**	
	Project:	All
	Format:	MBZ

0	**RC* IDLE Message Disable**	
	Project:	All
	Format:	Disable FormatDesc

For GT to get in any power saving RC* states, the render pipe must let the power management hardware know when it is IDLE. If this bit is set, power management will always assume the blitter pipe is not IDLE.

Value	Name	Description
0h	Enable **[Default]**	IDLE message is enabled
1h	Disable	IDLE message is disabled

BCS SW Control

BCS_SWCTRL - BCS SW Control		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	BlitterCS	
Default Value:	0x00000000	
Access:	r/w	
Size (in bits):	32	
Trusted Type:	1	
Address:	22200h	

DWord	Bit	Description
0	31:16	**Mask**
		Access: WO
		Format: Mask
	15:4	**Reserved**
		Project: CHV, BSW
		Format: MBZ
	3:2	**Reserved**
		Project: CHV, BSW
		Format: MBZ
	1	**Tile Y Destination**
		Project: CHV, BSW
		Format: U1
		Programming this bit makes the HW treat all destination surfaces as Tile Y. This bit over-rides the setting of the destination format in the packet provided to the blitter command streamer. SW is required to flush the HW before changing the polarity of this bit. This bit is part of the context save/restore.
	0	**Tile Y Source**
		Project: CHV, BSW
		Format: U1
		Programming this bit makes the HW treat all source surfaces as Tile Y. This bit over-rides the setting of the source format in the packet provided to the blitter command streamer. SW is required to flush the HW before changing the polarity of this bit. This bit is part of the context save/restore.

BCS Watchdog Counter Threshold

BCS_CTR_THRSH - BCS Watchdog Counter Threshold	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	BlitterCS
Default Value:	0x00150000
Access:	R/W
Size (in bits):	32
Address:	2217Ch

DWord	Bit	Description
0	31:0	**Counter logic Threshold**

Default Value:	00150000h
Format:	U32

 This field specifies the threshold that the hardware checks against for the value of the blitter clock counter before generating an interrupt. The counter in hardware generates an interrupt when the threshold is reached, rolls over and starts counting again. The interrupt generated is the "Media Hang Notify" interrupt since this watchdog timer is intended primarily to remedy VLD hangs on the main pipeline.

Bitstream Output Bit Count for the last Syntax Element Report Register

MFC_BITSTREAM_SE_BITCOUNT_SLICE - Bitstream Output Bit Count for the last Syntax Element Report Register	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	128D4h
Name:	VDBOX1
Valid Projects:	CHV, BSW

This register stores the count of number of bits in the bitstream for the last syntax element before padding. The bit count is before the byte-aligned alignment padding insertion, but includes the stop-one-bit. This register is part of the context save and restore.

DWord	Bit	Description
0	31:0	**MFC Bitstream Syntax Element Bit Count** Total number of bits in the bitstream output before padding. This count is updated each time the internal counter is incremented.

Bitstream Output Byte Count Per Slice Report Register

MFC_BITSTREAM_BYTECOUNT_SLICE - Bitstream Output Byte Count Per Slice Report Register	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	128D0h
Valid Projects:	CHV, BSW

This register stores the count of bytes of the bitstream output. This register is part of the context save and restore.

DWord	Bit	Description
0	31:0	**MFC Bitstream Byte Count** Total number of bytes in the bitstream output from the encoder. This count is updated for every time the internal bitstream counter is incremented.

Bitstream Output Minimal Size Padding Count Report Register

MFC_AVC_MINSIZE_PADDING_COUNT - Bitstream Output Minimal Size Padding Count Report Register	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	12814h
Name:	VDBOX1
Valid Projects:	CHV, BSW

 This register stores the count in bytes of **minimal size padding insertion. It is primarily provided for statistical data gathering.** This register is part of the context save and restore.

DWord	Bit	Description
0	31:0	**MFC AVC MinSize Padding Count** Total number of bytes in the bitstream output contributing to minimal size padding operation. This count is updated each time when the padding count is incremented.

Blitter Mode Register

<table>
<tr><td colspan="3" align="center">**BLT_MODE - Blitter Mode Register**</td></tr>
<tr><td colspan="3">Register Space: MMIO: 0/2/0</td></tr>
<tr><td colspan="3">Project: CHV, BSW</td></tr>
<tr><td colspan="3">Source: BlitterCS</td></tr>
<tr><td colspan="3">Default Value: 0x00000000</td></tr>
<tr><td colspan="3">Access: R/W</td></tr>
<tr><td colspan="3">Size (in bits):   32</td></tr>
<tr><td colspan="3">Trusted Type: 1</td></tr>
<tr><td colspan="3">Address: 2229Ch</td></tr>
</table>

DWord	Bit	Description
0	31:16	**Mask Bits** Format: Mask[15:0] Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)
	15	**Execlist Enable** Default Value: 0h Project: CHV, BSW Mask: MMIO#31 When set, software can utilize the execlist registers to load a context into hardware. When this bit is clear the Execlist mechanism cannot be used. The ring must be loaded via MMIO access. **Programming Notes** This bit is not intended to be changed dynamically. Changing the value of this bit while rendering is in progress will have UNDEFINED results. This bit should be changed only after a full reset and before submitting any commands to the device
	14	**Interrupt Steering Bit** Project: CHV, BSW Format: U1 When set, Command Streamer sends interrupt messages to the SHIM of the ON CHIP Micro Controller through message channel.When reset, Command Streamer sends the interrupt messages to Display Engine as config writes on GAM interface.
	13:10	**Reserved** Project: All Format: MBZ

BLT_MODE - Blitter Mode Register

9	**Per-Process GTT Enable**	

Project:	All
Format:	Enable Per-Process GTT BS Mode Enable

Value	Name	Description
0h	PPGTT Disable **[Default]**	When clear, the Global GTT will be used to translate memory access from designated commands and for commands that select the PPGTT as their translation space.
1h	PPGTT Enable	When set, the PPGTT will be used to translate memory access from designated commands and for commands that select the PPGTT as their translation space.

Programming Notes
This bit is used for enabling PPGTT access in Ring Buffer mode of scheduling. Privilege field in context descriptor states the same in Execlist Mode of scheduling. This field should be set before programming PDP0/1/2/3 registers in order to set the PPGTT translation of memory access.

8	**Reserved**	

Project:		All

7	**64Bit Virtual Addressing Enable**	

Project:	CHV, BSW
Format:	Enable

Per-Process GTT Enable

Value	Name	Description
0h	64Bit Virtual Addressing Disable **[Default]**	When clear indicates GFX operating in 32bit Virtual Addressing for PPGTT based memory access.

Programming Notes
This bit is only valid when PPGTT is enabled in ring buffer mode of scheduling. Context Descriptor has a similar bit to control 64bit virtual addressing in execlist mode of scheduling. Irrespective of this field set or clear virtual addresses translated through GGTT are always 32Bit. This field should be programmed before enabling PPGTT access. When this field is not set or for GGTT virtual addresses, Graphics Address [47:32] field of any commands or register exercised by SW should be programmed to 0x0.
64 Bit Virtual Addressing is not supported on CHV, BSW and must not be set.

6:5	**Reserved**	

Project:	CHV, BSW

4	**Reserved**	

Project:	CHV, BSW

BLT_MODE - Blitter Mode Register		
3:1	**Reserved**	
	Project:	All
	Format:	MBZ
0	**Privilege Check Disable**	
	Project:	CHV, BSW
	Format:	Enable
	This field when set, disables Privilege Violation checks on non-privileged batch buffers. When set Privileged commands are allowed to be executed from non-privileged batch buffers.	

Blitter TLB Control Register

BTCR - Blitter TLB Control Register		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0426Ch	

DWord	Bit	Description
0	31:1	**Reserved**
		Default Value: 00000000000000000000000000000000b
		Access: RO
	0	**Invalidate TLBs on the corresponding Engine**
		Default Value: 0b
		Access: R/W
		SW writes 1 to invalidate the TLBs for the associated engine and HW clears the bit when invalidation is complete. To ensure proper invalidation of the TLBs, SW has to ensure the corresponding engine's HW pipeline is flushed and cleared from all its memory accesses. Otherwise HW cannot guarantee the proper invalidation for TLBs.
		This bit is self clear.

BLT Context Element Descriptor (High Part)

BLT_CTX_EDR_H - BLT Context Element Descriptor (High Part)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04504h	

DWord	Bit	Description	
0	31:0	**BLT Context Element Descriptor (High Part)**	
		Default Value:	00000000h
		Access:	R/W

BLT Context Element Descriptor (Low Part)

BLT_CTX_EDR_L - BLT Context Element Descriptor (Low Part)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000009	
Size (in bits):	32	
Address:	04500h	

DWord	Bit	Description
0	31:0	**BLT Context Element Descriptor (Low Part)**
		Default Value: 00000009h
		Access: R/W

BLT Context Element Descriptor (Low Part)

BLT_CTX_EDR_L - BLT Context Element Descriptor (Low Part)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000009	
Size (in bits):	32	
Address:	04500h	

DWord	Bit	Description
0	31:0	**BLT Context Element Descriptor**
		Default Value: 00000009h
		Access: R/W

BLT Fault Counter

BLT_FAULT_CNTR - BLT Fault Counter	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	045B8h

DWord	Bit	Description
0	31:0	**BLT Fault Counter**
		Default Value: 00000000h
		Access: RO
		This counter only applies to advance context when fault and stream mode is selected.

BLT Fixed Counter

BLT_FIXED_CNTR - BLT Fixed Counter		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	045BCh	
DWord	**Bit**	**Description**
0	31:0	**BLT Fixed Counter**
		Default Value: · · · · 00000000h
		Access: · · · · RO
		This counter only applies to advance context when fault and stream mode is selected.

BLT PDP0/PML4/PASID Descriptor (High Part)

BLT_CTX_PDP0_H - BLT PDP0/PML4/PASID Descriptor (High Part)	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0450Ch

DWord	Bit	Description	
0	31:0	**BLT PDP0/PML4/PASID Descriptor (High Part)**	
		Default Value:	00000000h
		Access:	R/W

BLT PDP0/PML4/PASID Descriptor (Low Part)

BLT_CTX_PDP0_L - BLT PDP0/PML4/PASID Descriptor (Low Part)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04508h	

DWord	Bit	Description	
0	31:0	**BLT PDP0/PML4/PASID Descriptor (Low Part)**	
		Default Value:	00000000h
		Access:	R/W

BLT PDP1 Descriptor Register (High Part)

BLT_CTX_PDP1_H - BLT PDP1 Descriptor Register (High Part)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04514h	

DWord	Bit	Description
0	31:0	**BLT PDP1 Descriptor Register (High Part)**
		Default Value: 00000000h
		Access: R/W

BLT PDP1 Descriptor Register (Low Part)

BLT_CTX_PDP1_L - BLT PDP1 Descriptor Register (Low Part)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04510h	

DWord	Bit	Description
0	31:0	**BLT PDP1 Descriptor Register (Low Part)**
		Default Value: 00000000h
		Access: R/W

BLT PDP2 Descriptor Register (High Part)

BLT_CTX_PDP2_H - BLT PDP2 Descriptor Register (High Part)	

Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0451Ch

DWord	Bit	Description	
0	31:0	**BLT PDP2 Descriptor Register (High Part)**	
		Default Value:	00000000h
		Access:	R/W

BLT PDP2 Descriptor Register (Low Part)

BLT_CTX_PDP2_L - BLT PDP2 Descriptor Register (Low Part)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04518h	

DWord	Bit	Description	
0	31:0	**BLT PDP2 Descriptor Register (Low Part)**	
		Default Value:	00000000h
		Access:	R/W

BLT PDP3 Descriptor Register (High Part)

BLT_CTX_PDP3_H - BLT PDP3 Descriptor Register (High Part)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04524h	

DWord	Bit	Description
0	31:0	**BLT PDP3 Descriptor Register (High Part)**
		Default Value: 00000000h
		Access: R/W

BLT PDP3 Descriptor Register (Low Part)

BLT_CTX_PDP3_L - BLT PDP3 Descriptor Register (Low Part)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04520h	

DWord	Bit	Description
0	31:0	**BLT PDP3 Descriptor Register (Low Part)**

Default Value:	00000000h
Access:	R/W

Boolean_Counter_B0

<table>
<tr><th colspan="2">OAPERF_B0 - Boolean_Counter_B0</th></tr>
<tr><td>Register Space:</td><td>MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td>CHV, BSW</td></tr>
<tr><td>Source:</td><td>BSpec</td></tr>
<tr><td>Default Value:</td><td>0x00000000</td></tr>
<tr><td>Access:</td><td>R/W</td></tr>
<tr><td>Size (in bits):</td><td>32</td></tr>
<tr><td>Address:</td><td>02920h</td></tr>
<tr><td>Valid Projects:</td><td>[CHV, BSW]</td></tr>
</table>

This register enables the current live value of performance counter B0 to be read. Since what conditions cause B0 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.

DWord	Bit	Description
0	31:0	**Considerations**

Format:	U32

This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Boolean_Counter_B1

OAPERF_B1 - Boolean_Counter_B1	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02924h
Valid Projects:	[CHV, BSW]

This register enables the current live value of performance counter B1 to be read. Since what conditions cause B1 to increment are defined by the programming of CEC1-0/CEC1-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.

DWord	Bit	Description
0	31:0	**Considerations**
		<table><tr><td>Format:</td><td>U32</td></tr></table> This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Boolean_Counter_B2

OAPERF_B2 - Boolean_Counter_B2	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02928h
Valid Projects:	[CHV, BSW]

This register enables the current live value of performance counter B2 to be read. Since what conditions cause B2 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.

DWord	Bit	Description
0	31:0	**Considerations**
		Format: U32
		This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Boolean_Counter_B3

OAPERF_B3 - Boolean_Counter_B3	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	0292Ch
Valid Projects:	[CHV, BSW]

This register enables the current live value of performance counter B3 to be read. Since what conditions cause B3 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.

DWord	Bit	Description
0	31:0	**Considerations**
		Format: U32
		This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Boolean_Counter_B4

OAPERF_B4 - Boolean_Counter_B4	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02930h
Valid Projects:	[CHV, BSW]

This register enables the current live value of performance counter B4 to be read. Since what conditions cause B4 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.

DWord	Bit	Description
0	31:0	**Considerations**
		Format: U32
		This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Boolean_Counter_B5

OAPERF_B5 - Boolean_Counter_B5	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02934h
Valid Projects:	[CHV, BSW]

This register enables the current live value of performance counter B5 to be read. Since what conditions cause B5 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.

DWord	Bit	Description
0	31:0	**Considerations**

Format:	U32

This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Boolean_Counter_B6

OAPERF_B6 - Boolean_Counter_B6	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02938h
Valid Projects:	[CHV, BSW]

This register enables the current live value of performance counter B6 to be read. Since what conditions cause B6 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.

DWord	Bit	Description
0	31:0	**Considerations**
		Format: U32
		This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Boolean_Counter_B7

OAPERF_B7 - Boolean_Counter_B7	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	0293Ch
Valid Projects:	[CHV, BSW]

This register enables the current live value of performance counter B7 to be read. Since what conditions cause B7 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.

DWord	Bit	Description
0	31:0	**Considerations**
		Format: U32
		This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

BTB Not Consumed By RCS

BTP_PRODUCE_COUNT - BTB Not Consumed By RCS	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	02480h

This register keeps track of the outstanding BTP produced by RS which are not yet consumed by Render Command Streamer. This register is part of the render context save and restore.

Programming Notes
This register should not be programmed by SW.

DWord	Bit	Description
0	31:0	**BTP Produce Count** This register keeps track of the outstanding BTP produced by RS which are not yet consumed by Render Command Streamer. This register is part of the render context save and restore.

BTP Commands Parsed By RCS

BTP_PARSE_COUNT - BTP Commands Parsed By RCS	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	02490h

This register keeps track of the BTP commands parsed by RCS prior to encountering the Draw Call in an RS enabled Batch Buffer which has BTP Pool Alloc Valid. BTP parse count should be less then equal to the BTP produce count for Command Streamer to make progress on a 3D_PRIMITIVE command. BTP Parse count is subtracted from the BTP Produce Count upon parsing 3D_PRIMITIVE command. This register is part of the render context save and restore. This register should not be programmed by SW.

DWord	Bit	Description
0	31:0	**BTP Parse Count** This register keeps track of the BTP commands parsed by RCS prior to encountering the Draw Call in an RS enabled Batch Buffer which has BTP Pool Alloc Valid. BTP parse count should be less then equal to the BTP produce count for Command Streamer to make progress on a 3D_PRIMITIVE command. BTP Parse count is subtracted from the BTP Produce Count upon parsing 3D_PRIMITIVE command.

Cache Mode Register 0

CACHE_MODE_0 - Cache Mode Register 0	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00000004 CHV, BSW
Access:	R/W
Size (in bits):	32
Address:	07000h
Valid Projects:	CHV, BSW

Description
This register is used to control the operation of the Render and Sampler L2 Caches. All reserved bits are implemented as read/write. Before changing the value of this register, GFX pipeline must be idle i.e. full flush is required. This Register is saved and restored as part of Context.
RegisterType = MMIO_SVL

DWord	Bit	Description
0	31:16	**Mask**
		Access: WO
		Format: Mask[15:0]
		A 1 in a bit in this field allows the modification of the corresponding bit in Bits 15:0.
	15	**Sampler L2 Disable**
		Project: CHV, BSW
		Access: r/w
		Format: Disable
		Value — Name — Description 0h — [Default] — Sampler L2 Cache Enabled. 1h — Sampler L2 Cache Disabled. All accesses are treated as misses.
	14:12	**MSAA Compression Plane Number Threshold for eLLC**
		Project: CHV, BSW
		Security: IP.eLLC
		Access: r/w
		Value — Name — Description 0h — threshold0 [Default] — Cache only planeID = 0 in eLLC. 1h — threshold1 — Cache only planeID = 0, 1 in eLLC.

			CACHE_MODE_0 - Cache Mode Register 0		
		2h	threshold2	Cache only planeID = 0..2 in eLLC.	
		3h	threshold3	Cache only planeID = 0..3 in eLLC.	
		4h	threshold4	Cache only planeID = 0..4 in eLLC.	
		5h	threshold5	Cache only planeID = 0..5 in eLLC.	
		6h	threshold6	Cache only planeID = 0..6 in eLLC.	
		7h	threshold7	Cache only planeID = 0..7 in eLLC.	

Programming Notes
This bit-field is programmed based on MSAA. When MSAA compression is enabled, these settings affect HW, else it is ignored. For 16X MSAA only lower 8 planes can be cached in eLLC.

11	**Sampler Set Remmapping for 3D Disable**

Project:	CHV, BSW
Access:	r/w

Value	Name	Description
0h	Enable Set Remap **[Default]**	Set remapping for 3d enabled
1h	Disable Set Remap	Set remapping for 3d disabled

10	**RCZ PMA Chicken Bit**

Project:	CHV, BSW
Format:	Disable

This bit controls the bug-fix in the allocation pipe for expansions when the PMA-optimization mode is enabled.

Value	Name	Description
0h	Enable **[Default]**	Allocation pipe is not stalled if there are pending expansions
1h	Disable	Allocation pipe is stalled if there are pending expansions

9	**Sampler L2 TLB Prefetch Enable**

Access:	r/w

Value	Name	Description
0h	**[Default]**	TLB Prefetch Disabled
1h		TLB Prefetch Enabled

8	**Reserved**

CACHE_MODE_0 - Cache Mode Register 0

7:6	**Sampler L2 Request Arbitration**	
	Project:	CHV, BSW
	Access:	r/w
	Format:	U2

Value	Name	Description
00b		Round Robin
01b		Fetch are Highest Priority
10b		Constants are Highest Priority
11b		Reserved

5	**STC Eviction Policy**	
	Project:	CHV, BSW
	Access:	r/w
	Format:	Disable

If this bit is set, STCunit will have LRA as replacement policy. The default value i.e. (when this bit is reset) indicates that non-LRA eviction policy. This bit must be reset. LRA replacement policy is not supported.

Programming Notes	Project
If this bit is set to "1", bit 4 of 0x7010h must also be set to "1".	CHV, BSW

4	**RCC Eviction Policy**	
	Project:	CHV, BSW
	Access:	r/w
	Format:	Disable

If this bit is set, RCCunit will have LRA as replacement policy. The default value i.e. (when this bit is reset) indicates that non-LRA eviction policy. This bit must be reset. LRA replacement policy is not supported.

Programming Notes	Project
If this bit is set to "1", bit 7 of 0x7010h must also be set to "1".	CHV, BSW

3	**Reserved**

CACHE_MODE_0 - Cache Mode Register 0		

Hierarchical Z RAW Stall Optimization Disable — bit 2

Project:	CHV, BSW
Access:	r/w
Format:	U1

The Hierarchical Z RAW Stall Optimization allows non-overlapping polygons in the same 8x4 pixel/sample area to be processed without stalling waiting for the earlier ones to write to Hierarchical Z buffer.

Value	Name	Description
0h	Enable	Enables the hierarchical Z RAW Stall Optimization.
1h	Disable **[Default]**	Disables the hierarchical Z RAW Stall Optimization.

Programming Notes	Project
This bit must be set to 0 to enable the Hierarchical Z RAW stall optimization.	CHV, BSW

Disable clock gating in the pixel backend — bit 1

Access:	r/w
Format:	Disable

MCL related clock gating is disabled in the pixel backend. Before setting this bit to 1, the instruction/state caches must be invalidated. [DevGT:{WKA}]

RW optimization (portal2) fix disable — bit 0

Project:	CHV, BSW
Access:	r/w

Portal 2 fix :
a) In MSAA mode, RCC source clear cacheline will be allocated as RW, only if its a true read (ie blend enabled, etc) and will be allocated as WO otherwise.
b) In any mode, RCC should not allocate a cacheline as RW, if its not a true read, evenif MSC sends RW = 11 to RCC. MSC sends an additional "True read' indicator to help RCC override the RW bit.

Value	Name	Description
0	**[Default]**	Portal 2 fix enabled.
1		Portal 2 fix disabled. a) RCC will always allocate source clear as RW in MSAA mode. b) RCC will always allocate on the basic of MSC RW indicator to RCC, in non source clear mode.

Cache Mode Register 1

CACHE_MODE_1 - Cache Mode Register 1	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00000180 CHV, BSW
Access:	R/W
Size (in bits):	32
Address:	07004h
Valid Projects:	CHV, BSW

Description
RegisterType: MMIO_SVL
Before changing the value of this register, GFX pipeline must be idle; i.e., full flush is required. This Register is saved and restored as part of Context.

DWord	Bit	Description	
0	31:16	**Mask**	
		Access:	WO
		Mask:	MASK
		Format:	Mask[15:0]
		Must be set to modify corresponding data bit. Reads to this field returns zero.	
	15	**MSC Smart Bank Arbitration Disable**	
		Project:	CHV, BSW
		Access:	r/w
		Format:	Disable
		Setting this bit causes MSC Bank Arbitration to be disabled. Default value, i.e. resetting this bit, will Enable MSC Smart Bank Arbitration.	

Value	Name
0h	Enable **[Default]**
1h	Disable

CACHE_MODE_1 - Cache Mode Register 1

<table>
<tr><td>14</td><td colspan="2">**MSC Resolve Optimization Disable**</td></tr>
<tr><td></td><td>Project:</td><td>CHV, BSW</td></tr>
<tr><td></td><td>Access:</td><td>r/w</td></tr>
<tr><td></td><td>Format:</td><td>U1</td></tr>
</table>

Setting this bit causes MSC to mark cachelines dirty and appropriately update MSC during the classic clear resolve pass. Default value, i.e. resetting this bit, suppresses MSC buffer modification during the classic clear resolve pass.

Value	Name
1h	Disable
0h	Enable **[Default]**

<table>
<tr><td>13</td><td colspan="2">**NP EARLY Z FAILS DISABLE**</td></tr>
<tr><td></td><td>Project:</td><td>CHV, BSW</td></tr>
<tr><td></td><td>Access:</td><td>r/w</td></tr>
</table>

Value	Name	Description
0h	Disable **[Default]**	When NP PMA FIX ENABLE = 1, clearing this bit disables IZ to conservatively fail pixels.
1h	Enable	When NP PMA FIX ENABLE = 1, IZ does conservatively fail any NP pixels.

Programming Notes
This bit must be set when NP PMA FIX ENABLE = 1
This bit must not be set when NP PMA FIX ENABLE = 0

<table>
<tr><td>12</td><td colspan="2">**HIZ Eviction Policy**</td></tr>
<tr><td></td><td>Project:</td><td>CHV, BSW</td></tr>
<tr><td></td><td>Access:</td><td>r/w</td></tr>
<tr><td></td><td>Format:</td><td>U1</td></tr>
</table>

If this bit is set, Hizunit will have LRA as replacement policy. The default value i.e. (when this bit is reset) indicates the non-LRA eviction policy. For performance reasons, this bit must be reset.

Value	Name	Description
0h	**[Default]**	Non-LRA eviction Policy
1h		LRA eviction Policy

Programming Notes
If this bit is set to "1", bit 3 of 0x7010h must also be set to "1"

CACHE_MODE_1 - Cache Mode Register 1

	11	**NP PMA FIX ENABLE**		
		Project:		CHV, BSW
		Access:		r/w

Value	Name	Description
0h	Disable **[Default]**	Enables stalling PMA behavior for NP depth pixels in the early depth pipeline. (Legacy behavior)
1h	Enable	Enables non-stalling PMA behavior for NP depth pixels in the early depth pipeline.

Programming Notes
SW must set this bit in order to enable this fix when following expression is TRUE. 3DSTATE_WM::ForceThreadDispatch != 1 && !(3DSTATE_RASTER::ForceSampleCount != NUMRASTSAMPLES_0) && (3DSTATE_DEPTH_BUFFER::SURFACE_TYPE != NULL) && (3DSTATE_DEPTH_BUFFER:: HIZ Enable) && !(3DSTATE_WM::EDSC_Mode == 2) && (3DSTATE_PS_EXTRA::PixelShaderValid) && !(3DSTATE_WM_HZ_OP::DepthBufferClear || 3DSTATE_WM_HZ_OP::DepthBufferResolve || 3DSTATE_WM_HZ_OP::Hierarchical Depth Buffer Resolve Enable || 3DSTATE_WM_HZ_OP::StencilBufferClear) && (3DSTATE_WM_DEPTH_STENCIL::DepthTestEnable) && (((3DSTATE_PS_EXTRA::PixelShaderKillsPixels || 3DSTATE_PS_EXTRA:: oMask Present to RenderTarget || 3DSTATE_PS_BLEND::AlphaToCoverageEnable || 3DSTATE_PS_BLEND::AlphaTestEnable || 3DSTATE_WM_CHROMAKEY::ChromaKeyKillEnable) && (3DSTATE_WM::ForceKillPix != ForceOff && ((3DSTATE_WM_DEPTH_STENCIL::DepthWriteEnable && 3DSTATE_DEPTH_BUFFER::DEPTH_WRITE_ENABLE) || (3DSTATE_WM_DEPTH_STENCIL::Stencil Buffer Write Enable && 3DSTATE_DEPTH_BUFFER::STENCIL_WRITE_ENABLE && 3DSTATE_STENCIL_BUFFER::STENCIL_BUFFER_ENABLE)))) || (3DSTATE_PS_EXTRA:: Pixel Shader Computed Depth mode != PSCDEPTH_OFF))

	10	**Reserved**	
		Project:	CHV, BSW

	9	**Reserved**	
		Project:	CHV, BSW
		Access:	r/w

CACHE_MODE_1 - Cache Mode Register 1			
	8:7	**Sampler Cache Set XOR selection**	
		Project:	CHV, BSW
		Access:	r/w
		Format:	U2

These bits have an impact only when the Sampler cache is configured in 16 way set associative mode. If the cache is being used for immediate data or for blitter data these bits have no effect.

Value	Name	Description
00b	None	No XOR.
01b	Scheme 1	New_set_mask[3:0] = Tiled_address[16:13]. New_set[3:0] less than or = New_set_mask[3:0] ^Old_set[3:0]. Rationale: These bits can distinguish among 16 different equivalent classes of virtual pages. These bits also represent the lsb for tile rows ranging from a pitch of 1 tile to 16 tiles.
10b	Scheme 2	New_set_mask[3] = Tiled_address[17] ^ Tiled_address[16].New_set_mask[2] = Tiled_address[16] ^ Tiled_address[15].New_set_mask[1] = Tiled_address[15] ^ Tiled_address[14].New_set_mask[0] = Tiled_address[14] ^ Tiled_address[13].New_set[3:0] less than or = New_set_mask[3:0] ^ Old_set[3:0].Rationale: More bits on each XOR can give better statistical uniformity on sets and since two lsbs are taken for each tile row size, it reduces the chance of aliasing on sets.
11b	Scheme 3 **[Default]**	New_set_mask[3] = Tiled_address[22] ^ Tiled_address[21] ^ Tiled_address[20] ^ Tiled_address[19].New_set_mask[2] = Tiled_address[18] ^ Tiled_address[17] ^ Tiled_address[16].New_set_mask[1] = Tiled_address[15] ^ Tiled_address[14].New_set_mask[0] = Tiled_address[13].New_set[3:0] less than or = New_set_mask[3:0] ^ Old_set[3:0].Rationale: More bits on each XOR can give better statistical uniformity on sets and since each XOR has different bits, it reduces the chance of aliasing on sets even more.

Programming Notes
This field should be programmed as "00b" corresponding to NO XOR option when the 3D map performance fix in MT is enabled using the field "**Sampler Set Remmapping for 3D Disable**" in **CACHE_MODE_0 - Cache Mode Register 0.**

CACHE_MODE_1 - Cache Mode Register 1

	6	**4X4 RCPFE-STC Optimization Disable**	
		Project:	CHV, BSW
		Access:	r/w
		Format:	Disable

Value	Name	Description
0h	**[Default]**	Enables two contiguous 4x2s to be collected as 4X4 access for STC interface. This allows for less bank collision and less RAM power on STC.
1h		Disables this optimization and therefore only one valid 4x2 is sent to STC on the 4X4 interface.

Restriction
Restriction Gen9-LP bug# 1715730 : This bit must be set.

	5	**MCS Cache Disable**	
		Project:	CHV, BSW
		Access:	r/w
		Format:	Disable

For Programming restrictions please refer to the 3D Pipeline.

Value	Name	Description
0h	**[Default]**	MCS cache enabled. It allows RTs with MCS buffer enabled to be rendered using either MSAA compression for MSRT OR with color clear feature for non MSRT.
1h		MCS cache is disabled. Hence no MSAA compression for MSRT and no color clear for non-MSRT.

	4	**Float Blend Optimization Enable**	
		Project:	CHV, BSW
		Access:	r/w
		Format:	Enable

Value	Name	Description
0h	**[Default]**	Disables blend optimization for floating point RTs.
1h		Enables blend optimization for floating point RTs.

CACHE_MODE_1 - Cache Mode Register 1

	3	**Depth Read Hit Write-Only Optimization Disable**	
		Project:	CHV, BSW
		Access:	r/w
		Format:	Disable

Value	Name	Description
0h	**[Default]**	Read Hit Write-only optimization is enabled in the Depth cache (RCZ).
1h		Read Hit Write-only optimization is disabled in the Depth cache (RCZ).

	2	**RCZ Read after expansion control fix 2**	
		Access:	r/w
		Format:	Enable

Value	Name	Description
0h	**[Default]**	RCZ will suppress the read request to memory if it was allocated as a expansion Cacheline RCZ will always issue a read request to memory, even if it was previously allocated as expansion Cacheline
1h		RCZ will always issue a read request to memory, even if it was previously allocated as expansion Cacheline RCZ will suppress the read request to memory if it was allocated as a expansion Cacheline

	1	**Blend Optimization Fix Disable**	
		Project:	CHV, BSW
		Access:	r/w

Description
This bit when reset, enables blend optimization fix. If this bit is set, it disables the blend optimization fix and may exhibit corruption on alpha components in the render target under some conditions.

Value	Name
0	**[Default]**
1	

	0	**Reserved**	
		Project:	CHV, BSW

CAPPOINT

<table>
<tr><td colspan="4" align="center">**CAPPOINT - CAPPOINT**</td></tr>
<tr><td colspan="4">Register Space: PCI: 0/2/0</td></tr>
<tr><td colspan="4">Project: CHV, BSW</td></tr>
<tr><td colspan="4">Source: PRM</td></tr>
<tr><td colspan="4">Default Value: 0x000000D0</td></tr>
<tr><td colspan="4">Size (in bits):   32</td></tr>
<tr><td colspan="4">Address: 00034h</td></tr>
<tr><td colspan="4">This register points to a linked list of capabilities implemented by this device.</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td colspan="2">**Description**</td></tr>
<tr><td>0</td><td>31:8</td><td colspan="2">**RESERVED**</td></tr>
<tr><td></td><td></td><td>Default Value:</td><td>000000h</td></tr>
<tr><td></td><td></td><td>Access:</td><td>RO</td></tr>
<tr><td></td><td></td><td colspan="2">Reserved</td></tr>
<tr><td></td><td>7:0</td><td colspan="2">**CAPABILITIES_POINTER**</td></tr>
<tr><td></td><td></td><td>Default Value:</td><td>D0h</td></tr>
<tr><td></td><td></td><td>Access:</td><td>R/W Once</td></tr>
<tr><td></td><td></td><td colspan="2">The first item in the capabilities list is at address D0h (PMCS).
This register is programmed by BIOS during boot-up.Once written, this register becomes Read_Only. This register can only be cleared by a Reset.</td></tr>
</table>

CCK_CTL1

<table>
<tr><td colspan="4" align="center">**CCK_CTL1 - CCK_CTL1**</td></tr>
<tr><td colspan="4">Register Space: MMIO: 0/2/0</td></tr>
<tr><td colspan="4">Project: CHV, BSW</td></tr>
<tr><td colspan="4">Source: PRM</td></tr>
<tr><td colspan="4">Default Value: 0x00200000</td></tr>
<tr><td colspan="4">Size (in bits):   32</td></tr>
<tr><td colspan="4">Address: 101100h</td></tr>
</table>

BGF related programming.Note: This register should be the last one written between 10_1100, 10_1104, 10_1108. To be more specific, 10_1100[0] is the last one to be programmed between 10_1100h, 10_1104h and 10_1108h registers. The reason is that CZ clock does not stop on a frequency change and hence the fused values for the CZ clock domain must be the same and not intermittently transition to an invalid value, like all zeros.Changed for CHV, BSW.

DWord	Bit	Description
0	31:28	**czcount_30ns**

Default Value:	0h
Access:	R/W

Description

This register contains the number of cz clock cycles that it takes to make up 30ns.

Frequency (MHz)	czcount_30ns
400	4'b1011
333.333	4'b1001
320	4'b0001
266.667	4'b0111
200	4'b0101

Frequency (MHz)	czcount_30ns
533.333	4'b1111
466.667	4'b1101
373.333	4'b1011
360	4'b1010
355.556	4'b1010
350	4'b1010

	27	**Reserved**

Default Value:	0b
Access:	RO

Reserved

CCK_CTL1 - CCK_CTL1

26:24	**WellPUfreq**		
	Default Value:		000b
	Access:		R/W
	While Render or Media is being waking up from standby, clocks are allowed to be run for some time for x-contention removal. For CHV, BSW, there is a perceived di/dt risk by running this x-contention removal at full CU2X/CU frequency. This potential issue is amplified for CHV, BSW supports a 1:1 primary gear ratio and having a CU2X clock frequency of upto 2G. * 0xx: x-contention removal time will use: CU2X/1 for 2x clock, CU/1 for 1X clock. * 100: x-contention removal time will use a CU/4. * 101: x-contention removal time will use a CU/8. * 110: x-contention removal time will use a CU/16. * 111: x-contention removal time will use a CU/32.		
	Programming Notes		
	Punit should never program this bitfield to 3'b000 and it should program this to 3'b110.		
23	**CFG1Fuse0**		
	Default Value:		0b
	Access:		R/W
	bgfsource_config1fuse0. By default, there is no frequency change. The set of BGF and SS registers are provided by fuses. When frequency change is required, this bit must be set to '1' and Punit/driver must program the remainder of the clock crossing registers. This bit must be last bit written between register 10_1100, 10_1104 and 10_1108. The following registers are affected by this configuration bit: selecting between fuse values and configuration register: 0x10_1100[26:24] 0x10_1100[22:16] 0x10_1104[31:0] 0x10_1108[31:0]		
22:20	**CZ2CU_PTRSEP**		
	Default Value:		010b
	Access:		R/W
	bgf_cz2cu_ptrsep. Pointer separation for cz2cu BGF 000 = Pointer separation of 0 001 = Pointer separation of 1 010 = Pointer separation of 2 (Primary) 011 = Pointer separation of 3 (Secondary) 100 = Pointer separation of 4 101 = Pointer separation of 5 110 = Pointer separation of 6 111 = Pointer separation of 7		

CCK_CTL1 - CCK_CTL1		
19	**Reserved**	
	Default Value:	0b
	Access:	RO
	Reserved	
18:16	**CU2CZ_PTRSEP**	
	Default Value:	0h
	Access:	R/W
	bgf_cu2cz_ptrsep. Pointer separation for cu2cz BGF 000 = Pointer separation of 0 001 = Pointer separation of 1 010 = Pointer separation of 2 (Primary) 011 = Pointer separation of 3 (Secondary) 100 = Pointer separation of 4 101 = Pointer separation of 5 110 = Pointer separation of 6 111 = Pointer separation of 7	
15:9	**Reserved**	
	Default Value:	00h
	Access:	RO
	Reserved	
8	**ClkSquashEn**	
	Default Value:	0b
	Access:	R/W
	Clock Squash Enable. 0 = disabled. 1 = enabled. When this bit is enabled the GFX clock squashing feature is enabled. Clock squashing is only allowed when VNN is set to Vmin.	
	Programming Notes	
	This field must be zero at all times when in HPLLmode.	
7:1	**Reserved**	
	Default Value:	0h
	Access:	RO
	Reserved	
0	**DblBufPulse**	
	Default Value:	0h
	Access:	WO
	Reading from this register will always return a zero. Punit will write a one into this bit in order to push the BGF parameters into the double buffer during CPD/clock squah being enabled. A write to this register bit creates a one clock wide pulse (doublebufferpulse)to the CPunit.	

CCK_CTL2

CCK_CTL2 - CCK_CTL2	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	101104h

CZ and CU ratios for BGFs and for common clock calculations.Changed for CHV, BSW.

DWord	Bit	Description
0	31:16	**CZ2CU_CUratio**

Default Value:	0000h
Access:	R/W

These 16 bits shows the CU part of the BGF ratio between CZ and CU clock domain.
CU_SquashAllow (=CZ2CU_CUratio) must always be less than or equal to CU_SquashWindow.
When ClkSquashEn=0, CU_SquashAllow = CZ2CU_CUratio = CU_SquashWindow.
10_1108h will be dont care when ClkSquashEn=0. The effective/average squashed frequency will be determined by:(CU_SquashAllow/CU_SquashWindow)
When ClkSquashEn=1 and in GPLLmode, 12 <= CZ2CU_CUratio(10_1104[31:16]) <= CU_Squashwindow(10_1108[31:16]) and multiples of 4. Effective CUfrequency = CUratio/(CU Squash Window)
Actual CUfrequency = UnsquashedFrequency*CUratio/(CU Squash Window)
If in GPLLmode, CU2x frequency =
(400/10)*N, where N inside {2,50}
(333/8)*N, where N inside {2,48}
(320/8)*N, where N inside {2,50}
(267/6)*N, where N inside {2,45}
(200/5)*N, where N inside {2,50}
The value programmed into this bitfield will be N*4.
In HPLLmode: CZ2CU_CUratio=720/(INTEGER*2). The HPLLvco (as determined by CCK_FUSE_REG0[1:0]) is divided by an INTEGER=(1,2,3,4,5,6,8,9,10) to create the CU2x frequency. CUclk=CU2xclk/2.

CCK_CTL2 - CCK_CTL2

	15:0	**CZ2CU_CZratio**		
		Default Value:		0000h
		Access:		R/W
		These 16 bits shows the CU part of the BGF ratio between CZ and CU clock domain.		
		CZ2CU_CZratio = UsyncPeriod/CZperiod		
		In GPLLmode, UsyncPeriod is expected to be (8*GPLLref_in_ns). GPLLref_in_ns is expected to be		
		CZperiod*5 for CZ200		
		CZperiod*6 for CZ266		
		CZperiod*8 for CZ320		
		CZperiod*8 for CZ333		
		CZperiod*10 for CZ400.		
		That makes		
		CZ2CU_CZratio = 8*5 for CZ200 and GPLL mode.		
		CZ2CU_CZratio = 8*6 for CZ266 and GPLL mode.		
		CZ2CU_CZratio = 8*8 for CZ320 and GPLL mode.		
		CZ2CU_CZratio = 8*8 for CZ333 and GPLL mode.		
		CZ2CU_CZratio = 8*10 for CZ400 and GPLL mode.		
		The above only applies for GPLL mode and when UsyncPeriod = 8*GPLLref, CPunit will internally		
		generate the following signal:		
		CZ_Com_limit = CZ2CU_CZratio - 1		
		In HPLLmode: CZ2CU_CZratio=720/(INTEGER*1). The HPLLvco (as determined by		
		CCK_FUSE_REG0[1:0]) is divided by an INTEGER=(1,2,3,4,5,6,8,9,10) to create the CZ frequency.		

CCK_CTL3

<table>
<tr><td colspan="3" align="center">**CCK_CTL3 - CCK_CTL3**</td></tr>
<tr><td>Register Space:</td><td colspan="2">MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td colspan="2">CHV, BSW</td></tr>
<tr><td>Source:</td><td colspan="2">PRM</td></tr>
<tr><td>Default Value:</td><td colspan="2">0x00008000</td></tr>
<tr><td>Size (in bits):</td><td colspan="2">32</td></tr>
<tr><td>Address:</td><td colspan="2">101108h</td></tr>
<tr><td colspan="3">Graphics clock squash control.Changed for CHV, BSW.</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td>**Description**</td></tr>
<tr><td>0</td><td>31:16</td><td>**CU SQUASH WINDOW**

Default Value: 0000h
Access: R/W

This register will always show the number of unsquashed clock cycles in a usync window.
CU_SquashWindow = UsyncPeriod/Unsquashed_CUperiod.
In GPLLmode, UsyncPeriod is expected to be (8*GPLLref_in_ns). CUperiod will be GPLLref_in_ns/Ratio.
That makes, CU_SquashWindow = (8*GPLLref_in_ns)/(GPLLref_in_ns/Ratio) = 8*Ratio.
Ratio is the multiplier from GPLLref to provide the CU clock frequency.
Note: CU_SquashWindow = 8*Ratio only applies for GPLL mode when the usync period is 8*GPLL.
In HPLLmode, clock squashing is not supported and 10_1100[8] must be zero at all times in HPLLmode.</td></tr>
<tr><td></td><td>15:0</td><td>**CU SQUASH INIT**

Default Value: 8000h
Access: R/W

This register is used to move around the location of where the clocks are squashed. For initial design, this is always set to 8000h.</td></tr>
</table>

CCK_CTL4

CCK_CTL4 - CCK_CTL4		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	10110Ch	

CZclk 30ns TSV Generation

DCN requires support for more CZclk frequencies

DWord	Bit	Description
0	31:17	**SPARE**
		Default Value: 00000000h
		Access: R/W
		Reserved
	16	**CZCLK 30ns Mechanism**
		Access: R/W
		This bit defines whether we use the old counter mechanism for generating the 30ns pulse or use this new TSV scheme 0 - Use the old counter mechanism to determine the 30ns pulse (default) 1 - Use the new TSV scheme with the Allow and Window values from this register
	15:8	**CZclk HPLL VCOS IN 30ns**
		Access: R/W
		These bits determine the window in terms of the number of HPLL VCO clock cycles in 30ns
	7:0	**CZclk HPLL DIV**
		Access: R/W
		These bits define the integer used to divide HPLLvco to get CZclk

CLAIM_ER

CLAIM_ER - CLAIM_ER	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	182028h

Claim Error Counter - counts the RM claim error (no RM claim) reported at CLAIM_ERROR field of EIR

DWord	Bit	Description	
0	31	**CLAIM_ER_CLR**	
		Default Value:	0b
		Access:	WO
		writing a '1' to this bit clears the CLAIM_ER_CTR, CTR_OVERFLOW and CLAIM_ERROR bit (EIR[0]). A read of this bit always returns 0	
	30:17	**RESERVED**	
		Default Value:	0000h
		Access:	RO
		Reserved	
	16	**CTR_OVERFLOW**	
		Default Value:	0b
		Access:	RO
		When set, indicates that the CLAIM_ER_CTR field of this register has overflowed (i.e., claim-error count has reached the value of 65536) The overflow is supplied by the RMbus master.	
	15:0	**CLAIM_ER_CTR**	
		Default Value:	0000h
		Access:	RO

Clipper Invocation Counter

CL_INVOCATION_COUNT - Clipper Invocation Counter	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Trusted Type:	1
Address:	02338h
Valid Projects:	

This register stores the count of objects entering the Clipper stage. This register is part of the context save and restore.

DWord	Bit	Description
0	63:32	**CL Invocation Count Report UDW** Number of objects entering the clipper stage. Updated only when Statistics Enable is set in CLIP_STATE (see the Clipper Chapter in the 3D Volume.)
	31:0	**CL Invocation Count Report LDW** Number of objects entering the clipper stage. Updated only when Statistics Enable is set in CLIP_STATE (see the Clipper Chapter in the 3D Volume.)

Clipper Primitives Counter

CL_PRIMITIVES_COUNT - Clipper Primitives Counter	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Trusted Type:	1
Address:	02340h
Valid Projects:	

This register reflects the total number of primitives that have been output by the clipper. This register is part of the context save and restore.

DWord	Bit	Description
0	63:32	**Clipped Primitives Output Count UDW** Total number of primitives output by the clipper stage. This count is updated for every primitive output by the clipper stage, as long as Statistics Enable is set in SF_STATE (see the Clipper and SF Chapters in the 3D Volume.)
	31:0	**Clipped Primitives Output Count LDW** Total number of primitives output by the clipper stage. This count is updated for every primitive output by the clipper stage, as long as Statistics Enable is set in SF_STATE (see the Clipper and SF Chapters in the 3D Volume.)

CLKGATE Messaging Register for Clocking Unit

MSG_CLKGATE_GCP - CLKGATE Messaging Register for Clocking Unit	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	16
Address:	0802Ch

Message registers have bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16]. In order to set bit0, for example, the data would be 0x0001_0001. In order to clear bit0, for example, the data would be 0x0001_0000. Note that mask bit is the data bit offset + 16. Message registers are protected from non-GT writes via the Message Channel.

DWord	Bit	Description	
0	15:7	**Reserved**	
		Access:	RO
	6	**Gate cmclk Acknowledgement (VCS1)**	
		Access:	R/W
		Gate cmclk Acknowledgement (VCS1) 1'b0 : Clocks are ungated <default> 1'b1 : Clocks are gated	
	5	**Gate cwclk Acknowledgement (WIN)**	
		Access:	R/W
		Gate cwclk Acknowledgement (WIN) 1'b0 : Clocks are ungated <default> 1'b1 : Clocks are gated	
	4	**Reserved**	
	3	**Gate cfclk Acknowledgement (CS)**	
		Access:	R/W
		Gate cfclk Acknowledgement (CS) 1'b0 : Clocks are ungated <default> 1'b1 : Clocks are gated	
	2	**Gate cvclk Acknowledgement (VECS)**	
		Access:	R/W
		Gate cvclk Acknowledgement (VECS) 1'b0 : Clocks are ungated <default> 1'b1 : Clocks are gated	

MSG_CLKGATE_GCP - CLKGATE Messaging Register for Clocking Unit

	1	**Gate cmclk Acknowledgement (VCS0)**
		Access: R/W
		Gate cmclk Acknowledgement (VCS0) 1'b0 : Clocks are ungated <default> 1'b1 : Clocks are gated
	0	**Gate crclk Acknowledgement (CS)**
		Access: R/W
		Gate crclk Acknowledgement (CS) 1'b0 : Clocks are ungated <default> 1'b1 : Clocks are gated

CLOCK_GATE_DIS1

CLOCK_GATE_DIS1 - CLOCK_GATE_DIS1		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	182060h	
Gunit Clock Gating Disable		
DWord	**Bit**	**Description**
0	31	**GIOSF_DIS**
		Default Value: 0b
		Access: R/W
		0 = Enable clock gating 1 = Disable clock gating
	30	**GPFI_DIS**
		Default Value: 0b
		Access: R/W
		0 = Enable clock gating 1 = Disable clock gating
	29	**GRMW_DIS**
		Default Value: 0b
		Access: R/W
		0 = Enable clock gating 1 = Disable clock gating
	28	**GSA_OUTBOUND_DIS**
		Default Value: 0b
		Access: R/W
		0 = Enable clock gating 1 = Disable clock gating
	27	**GSA_RTN_DIS**
		Default Value: 0b
		Access: R/W
		0 = Enable clock gating 1 = Disable clock gating

CLOCK_GATE_DIS1 - CLOCK_GATE_DIS1

26	**GUP_DIS**	
	Default Value:	0b
	Access:	R/W
	0 = Enable clock gating 1 = Disable clock gating	

25	**GWAKE_DIS**	
	Default Value:	0b
	Access:	R/W
	0 = Enable clock gating 1 = Disable clock gating	

24	**GCR_DIS**	
	Default Value:	0b
	Access:	R/W
	0 = Enable clock gating 1 = Disable clock gating	

23	**GBC_DIS**	
	Default Value:	0b
	Access:	R/W
	0 = Enable clock gating 1 = Disable clock gating	

22	**GINT_DIS**	
	Default Value:	0b
	Access:	R/W
	0 = Enable clock gating 1 = Disable clock gating	

21	**GRMBUS_DIS**	
	Default Value:	0b
	Access:	R/W
	0 = Enable clock gating 1 = Disable clock gating	

20	**GCCBCZ_KEYCMP_DIS**	
	Default Value:	0b
	Access:	R/W
	0 = Enable clock gating 1 = Disable clock gating	

CLOCK_GATE_DIS1 - CLOCK_GATE_DIS1

19:16	**SPARE1**	
	Default Value:	0h
	Access:	R/W
	Spare	

15	**Reserved**

14	**Reserved**

13	**Reserved**

12	**GSECDISP_DIS**	
	Default Value:	0b
	Access:	R/W
	0 = Enable clock gating 1 = Disable clock gating	

11	**GREGDISP_DIS**	
	Default Value:	0b
	Access:	R/W
	0 = Enable clock gating 1 = Disable clock gating	

10	**GCTLQ_DIS**	
	Default Value:	0b
	Access:	R/W
	0 = Enable clock gating 1 = Disable clock gating	

9	**GMMIO_DIS**	
	Default Value:	0b
	Access:	R/W
	0 = Enable clock gating 1 = Disable clock gating	

8	**GCFG_DIS**	
	Default Value:	0b
	Access:	R/W
	0 = Enable clock gating 1 = Disable clock gating	

7:4	**SPARE2**	
	Default Value:	0h
	Access:	R/W
	Spare	

CLOCK_GATE_DIS1 - CLOCK_GATE_DIS1

	3:0	**CZ_IDLE_TIMER**	
		Default Value:	0h
		Access:	R/W
		Gunit CZ domain idle timer count value. Individual Gunit CZ fubs use this as a counter pre-load value. 0 = Idle timer disabled 1 - 15 = After a unit indicates idle, wait this many clocks before gating.	

CLOCK_GATE_DIS2

<table>
<tr><td colspan="3" align="center">**CLOCK_GATE_DIS2 - CLOCK_GATE_DIS2**</td></tr>
<tr><td colspan="3">Register Space: MMIO: 0/2/0</td></tr>
<tr><td colspan="3">Project: CHV, BSW</td></tr>
<tr><td colspan="3">Source: PRM</td></tr>
<tr><td colspan="3">Default Value: 0x00000000</td></tr>
<tr><td colspan="3">Size (in bits):   32</td></tr>
<tr><td colspan="3">Address: 182064h</td></tr>
<tr><td colspan="3">Gunit Clock Gating Disable register2.</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td>**Description**</td></tr>
<tr><td>0</td><td>31:9</td><td>**CLKGATE_SPARE**
Default Value: 000000h
Access: R/W
Spare to be assigned to clock gate disables.</td></tr>
<tr><td></td><td>8</td><td>**GPMH_DIS**
Default Value: 0b
Access: R/W
New for CHV, BSW
0 = Enable clock gating
1 = Disable clock gating</td></tr>
<tr><td></td><td>7</td><td>**ATOMICS_DIS**
Default Value: 0b
Access: R/W
New for CHV, BSW
0 = Enable clock gating
1 = Disable clock gating</td></tr>
<tr><td></td><td>6</td><td>**IOSFSB_P_DIS**
Default Value: 0b
Access: R/W
New for CHV, BSW
0 = Enable clock gating
1 = Disable clock gating</td></tr>
<tr><td></td><td>5</td><td>**IOSFSB_DIS**
Default Value: 0b
Access: R/W
New for CHV, BSW
0 = Enable clock gating
1 = Disable clock gating</td></tr>
</table>

CLOCK_GATE_DIS2 - CLOCK_GATE_DIS2

	4	**GARB_DIS**	
		Default Value:	0b
		Access:	R/W
		0 = Enable clock gating 1 = Disable clock gating	
	3	**GMAP_DIS**	
		Default Value:	0b
		Access:	R/W
		0 = Enable clock gating 1 = Disable clock gating	
	2	**Reserved**	
	1	**GRDDATBUF_DIS**	
		Default Value:	0b
		Access:	R/W
		0 = Enable clock gating 1 = Disable clock gating	
	0	**GWRDATQ_DIS**	
		Default Value:	0b
		Access:	R/W
		0 = Enable clock gating 1 = Disable clock gating	

Clock gate and clear EU metrics

EUMETRICSCLEAR - Clock gate and clear EU metrics	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	138198h

EU Metrics Clear

DWord	Bit	Description		
0	31:1	**Reserved**		
		Default Value:		00000000h
		Access:		RO
		Reserved		
	0	**Clear EU Metrics**		
		Default Value:		0b
		Access:		R/W
		For Cdyn optimization, when this bit is set to one, all of the 13 counters are clock gated. Then, after setting it to '0(zero), On the falling edge of EUMetricsClr, all of the 13 counters are reset to zero and counting resumes.		

Event Name	Units	Maximum per cycle (average)	Metric	Comments
event0: ss0_gpm_sampler_active_igpa	1 = 1 sampler busy in this sub-slice.	1 sampler busy in this sub-slice.	Sampler busy per sub-slice	Measures sampler utilization (i.e, sampler not idle)
event1: ss1_gpm_sampler_active_igpa	1 = 1 sampler busy in this sub-slice.	1 sampler busy in this sub-slice.	Sampler busy per sub-slice	Measures sampler utilization (i.e, sampler not idle)
event2: tdl0_gpm_eu_stall	1 = 32 EUs stalled on this sub-slice.	8 EUs stalled on this sub-slice.	EU stall per sub-slice	Measures EU stalls
event3: tdl1_gpm_eu_stall	1 = 32 EUs stalled on this sub-slice.	8 EUs stalled on this sub-slice.	EU stall per sub-slice	Measures EU stalls

EUMETRICSCLEAR - Clock gate and clear EU metrics

		event4: tdl0_gpm_ipc_count	1 = 32 instructions executed on this sub-slice.	16 instructions executed on this sub-slice.	IPC per sub-slice	Measures EU utilization: 0, 1, or 2 counts per clock per EU
		event5: tdl1_gpm_ipc_count	1 = 32 instructions executed on this sub-slice.	16 instructions executed on this sub-slice.	IPC per sub-slice	Measures EU utilization: 0, 1, or 2 counts per clock per EU
		event6: tdl0_gpm_threads_allocated	1 = 64 threads allocated in this sub-slice.	56 threads allocated in this sub-slice.	Thread allocated per sub-slice	Measures the threads allocated
		event7: tdl1_gpm_threads_allocated	1 = 64 threads allocated in this sub-slice.	56 threads allocated in this sub-slice.	Thread allocated per sub-slice	Measures the threads allocated
		event8: tdl0_gpm_eu_stall_sampler	1 = 64 EUs stalled by sampler in this sub-slice.	56 threads stalled by sampler in this sub-slice.	Placeholder for EUstallTime by sampler per sub-slice	Measures how much of eu stalls are due to sampler
		event9: tdl1_gpm_eu_stall_sampler	1 = 64 EUs stalled by sampler in this sub-slice.	56 threads stalled by sampler in this sub-slice.	Placeholder for EUstallTime by sampler per sub-slice	Measures how much of eu stalls are due to sampler
		event10: tdl0_gpm_eu_not_idle	1 = 32 EUs not idle in this sub-slice.	8 EUs not idle in this sub-slice.	Clocks any EU is not idle per sub-slice	Measures EU utilization (i.e, EU not idle)
		event11: tdl1_gpm_eu_not_idle	1 = 32 EUs not idle in this sub-slice.	8 EUs not idle in this sub-slice.	Clocks any EU is not idle per sub-slice	Measures EU utilization (i.e, EU not idle)
		event12: constant_one	1			one clock cycle toggles.

Clock Gating Messages

<table>
<tr><th colspan="3">CGMSG - Clock Gating Messages</th></tr>
<tr><td>Register Space:</td><td colspan="2">MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td colspan="2">CHV, BSW</td></tr>
<tr><td>Source:</td><td colspan="2">PRM</td></tr>
<tr><td>Default Value:</td><td colspan="2">0x00000000</td></tr>
<tr><td>Size (in bits):</td><td colspan="2">32</td></tr>
<tr><td>Address:</td><td colspan="2">08104h</td></tr>
<tr><td colspan="3">Clock Gating Messages Register</td></tr>
<tr><th>DWord</th><th>Bit</th><th>Description</th></tr>
<tr><td>0</td><td>31:16</td><td>

Message Mask

Access:	RO

Message Mask
In order to write to bits 15:0, the corresponding message mask bits must be written.
For example, for bit 14 to be set, bit 30 needs to be 1 : 40004000

</td></tr>
<tr><td></td><td>15:7</td><td>

Reserved

Access:	RO

Reserved

</td></tr>
<tr><td></td><td>6</td><td>

Media 1 Clock gating control message

Access:	R/W

Gate Media 1 (2nd Vbox) Clock Message :
'0' : Media 1 Clock Un-gate Request (un-gates the cmclk clock in the 2n Media block)
'1' : Media 1 Clock Gate Request (gates the cmclk clockin the 2nd Media block)

</td></tr>
<tr><td></td><td>5</td><td>

WIDI CLock Gating control Message

Access:	R/W

Gate WIDI Clock Message :
'0' : WIDI Clock Un-gate Request (un-gates the cwclk clock)
'1' : WIDI Clock Gate Request (gates the cwclk clock)

</td></tr>
<tr><td></td><td>4</td><td>

Reserved

</td></tr>
<tr><td></td><td>3</td><td>

Fix Function Clock gating Control Message

Access:	R/W

Gate Fix Clock Message :
'0' : Fix Clock Un-gate Request (un-gates the cfclk/cf2xclk clock)
'1' : Fix Clock Gate Request (gates the cfclk/cf2xclk clock)

</td></tr>
<tr><td></td><td>2</td><td>

VEbox Clock gating Control message

Access:	R/W

Gate VE-box Clock Message :
'0' : VEbox Clock Un-gate Request (un-gates the cvclk clock)
'1' : VEbox Clock Gate Request (gates the cvclk clock)

</td></tr>
</table>

		CGMSG - Clock Gating Messages	
	1	**Media 0 Clock Gating Control Message**	
		Access:	R/W
		Gate Media Clock Message : '0' : Media 0 Clock Un-gate Request (un-gates the cmclk clock) '1' : Media 0 Clock Gate Request (gates the cmclk clock)	
	0	**Row Clock Gating Control Message**	
		Access:	R/W
		Gate Row Clocks Message : '0' : Row Clock Un-gate Request (un-gates the crclk and cr2xclk clocks) '1' : Row Clock Gate Request (gates the crclk and cr2xclk clocks)	

Color/Depth Write FIFO Watermarks

CZWMRK - Color/Depth Write FIFO Watermarks	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	04060h

This register is directly mapped to the current Virtual Addresses in the MTTLB (Texture and constant cache TLB).

DWord	Bit	Description
0	31:24	**Reserved** Format: MBZ
	23:18	**Color Wr Burst Size** This is the maximum size of the requests burst, from the last High Watermark trip, before reevaluating the High Watermark again.
	17:16	**Reserved** Format: MBZ
	15:12	**Color Wr FIFO High Watermark** This is the number of accumulated Color writes that will trigger a Burst of Z Writes.
	11:6	**Z Wr Burst Size** This is the maximum size of the requests burst, from the last High Watermark trip, before reevaluating the High Watermark again.
	5:4	**Reserved** Format: MBZ
	3:0	**Z Wr FIFO High Watermark** This is the number of accumulated Depth writes that will trigger a Burst of Z Writes.

Configuration Register0 for RPMunit

CONFIG0 - Configuration Register0 for RPMunit	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Default Value:	0x00000000
Size (in bits):	32
Address:	00D00h

Lock bit LOCK applies to all RW/L fields in this register. Lock is overridden during context restore.

DWord	Bit	Description
0	31	**Lock for RW/L Fields in this Register** <table><tr><td>Access:</td><td>R/W Lock</td></tr></table>0 = Bits of CONFIG0 register are R/W. 1 = All bits of CONFIG0 register are RO (including this lock bit). Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). Lock is reset on a restore after context is captured.
	30:0	**Placeholder Bits** <table><tr><td>Project:</td><td>CHV, BSW</td></tr><tr><td>Access:</td><td>R/W Lock</td></tr></table>Placeholder bits for implementation or ECO loops.

Configuration Register1 for RPMunit

<table>
<tr><td colspan="3" align="center">**CONFIG1 - Configuration Register1 for RPMunit**</td></tr>
<tr><td>Register Space:</td><td colspan="2">MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td colspan="2">CHV, BSW</td></tr>
<tr><td>Default Value:</td><td colspan="2">0x00000000</td></tr>
<tr><td>Size (in bits):</td><td colspan="2">32</td></tr>
<tr><td>Address:</td><td colspan="2">00D04h</td></tr>
<tr><td colspan="3">Lock bit LOCK applies to all RW/L fields in this register. Lock is overridden during context restore.</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td>**Description**</td></tr>
<tr><td>0</td><td>31</td><td>**Lock for RW/L Fields in this Register**

Access: R/W Lock

0 = Bits of CONFIG0 register are R/W.
1 = All bits of CONFIG0 register are RO (including this lock bit).
Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock).
Lock is reset on a restore after context is captured.</td></tr>
<tr><td></td><td>30:0</td><td>**Placeholder Bits**

Project: CHV, BSW
Access: R/W Lock

Placeholder bits for implementation or ECO loops.</td></tr>
</table>

Configuration Register for RCPunit

RCPCONFIG - Configuration Register for RCPunit			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Default Value:	0x0000000F		
Size (in bits):	32		

Address:	00D08h

Unit Level Clock Gating Control Registers			

DWord	Bit	Description	
0	31:5	**Placeholder Bits**	
		Access:	R/W Lock
		Placeholder bits for implementation or ECO loops.	
	4	**Reserved**	
	3	**RPMunit Clock Gating Disable in Uncore Well**	
		Default Value:	1b
		Access:	R/W
		Clock Gating Disable Control: '0': Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality). '1': Clock Gating Disabled. (i.e., clocks are toggling, always) (DEFAULT).	
	2	**MGSRunit Clock Gating Disable in Uncore Well**	
		Default Value:	1b
		Access:	R/W
		Clock Gating Disable Control: '0': Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality). '1': Clock Gating Disabled. (i.e., clocks are toggling, always) (DEFAULT).	
	1	**MDRBunit Clock Gating Disable in Uncore Well**	
		Default Value:	1b
		Access:	R/W
		Clock Gating Disable Control: '0': Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality). '1': Clock Gating Disabled. (i.e., clocks are toggling, always) (DEFAULT).	

RCPCONFIG - Configuration Register for RCPunit

	0	**MCRunit Clock Gating Disable in Uncore Well**	
		Default Value:	1b
		Access:	R/W
		Clock Gating Disable Control: '0': Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality). '1': Clock Gating Disabled. (i.e., clocks are toggling, always) (DEFAULT).	

Context Load Protocol Register BLT

BLT_CTX_LD_PRTCL - Context Load Protocol Register BLT		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000 CHV, BSW	
Size (in bits):	32	
Address:	04014h	

DWord	Bit	Description	
0	31:16	**Mask Bits**	
		Default Value:	0000h
		Access:	RO
	15	**Context Load Protocol Register - BCS 15**	
		Default Value:	0b
		Access:	R/W
		For Future Use. This bit is self clear.	
	14	**Context Load Protocol Register - BCS 14**	
		Default Value:	0b
		Access:	R/W
		For Future Use. This bit is self clear.	
	13	**Context Load Protocol Register - BCS 13**	
		Default Value:	0b
		Access:	R/W
		For Future Use. This bit is self clear.	
	12	**Context Load Protocol Register - BCS 12**	
		Default Value:	0b
		Access:	R/W
		For Future Use. This bit is self clear.	
	11	**Context Load Protocol Register - BCS 11**	
		Default Value:	0b
		Access:	R/W
		For Future Use. This bit is self clear.	

BLT_CTX_LD_PRTCL - Context Load Protocol Register BLT

10	**Context Load Protocol Register - BCS 10**		
	Default Value:		0b
	Access:		R/W
	For Future Use. This bit is self clear.		
9	**Context Load Protocol Register - BCS 9**		
	Default Value:		0b
	Access:		R/W
	For Future Use. This bit is self clear.		
8	**Context Load Protocol Register - BCS 8**		
	Default Value:		0b
	Access:		R/W
	For Future Use. This bit is self clear.		
7	**Context Load Protocol Register - BCS 7**		
	Default Value:		0b
	Access:		R/W
	For Future Use. This bit is self clear.		
6	**Context Load Protocol Register - BCS 6**		
	Default Value:		0b
	Access:		R/W
	For Future Use. This bit is self clear.		
5	**Context Load Protocol Register - BCS 5**		
	Default Value:		0b
	Access:		R/W
	For Future Use. This bit is self clear.		
4	**Context Load Protocol Register - BCS 4**		
	Default Value:		0b
	Access:		R/W
	For Future Use. This bit is self clear.		
3	**Context Load Protocol Register - BCS 3**		
	Default Value:	0b	
	Project:	CHV, BSW	
	Access:	R/W	

BLT_CTX_LD_PRTCL - Context Load Protocol Register BLT

		Bit 3 = Context Complete. Only valid with Bit 2 asserted and indicates whether the context switching out as complete vs. incomplete. This bit is self clear.

2	**Context Load Protocol Register - BCS 2**	
	Default Value:	0b
	Access:	R/W

Context Load Protocol Register
(Written by BCS)
Bit 2 = Request from BCS to GAM for context save readiness. GAM will acknowledge appropriated steps taken.
This bit is self clear.

1	**Context Load Protocol Register - BCS 1**	
	Default Value:	0b
	Access:	R/W

Context Load Protocol Register
(Written by BCS)
Bit 1 = Context Launched.
This bit is self clear.

0	**Context Load Protocol Register - BCS 0**	
	Default Value:	0b
	Access:	R/W

Context Load Protocol Register
(Written by BCS)
Bit 0 = Context Available.
This bit is self clear.

Context Load Protocol Register CS

GFX_CTX_LD_PRTCL - Context Load Protocol Register CS	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000 CHV, BSW
Size (in bits):	32
Address:	04004h

DWord	Bit	Description
0	31:16	**Mask Bits** Default Value: 0000h Access: RO
	15	**Context Load Protocol Register - CS 15** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	14	**Context Load Protocol Register - CS 14** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	13	**Context Load Protocol Register - CS 13** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	12	**Context Load Protocol Register - CS 12** Default Value: 0b Access: R/W For Future Use. This bit is self clear.
	11	**Context Load Protocol Register - CS 11** Default Value: 0b Access: R/W For Future Use. This bit is self clear.

GFX_CTX_LD_PRTCL - Context Load Protocol Register CS

10	**Context Load Protocol Register - CS 10**	
	Default Value:	0b
	Access:	R/W
	For Future Use. This bit is self clear.	

9	**Context Load Protocol Register - CS 9**	
	Default Value:	0b
	Access:	R/W
	For Future Use. This bit is self clear.	

8	**Context Load Protocol Register - CS 8**	
	Default Value:	0b
	Access:	R/W
	For Future Use. This bit is self clear.	

7	**Context Load Protocol Register - CS 7**	
	Default Value:	0b
	Access:	R/W
	For Future Use. This bit is self clear.	

6	**Context Load Protocol Register - CS 6**	
	Default Value:	0b
	Access:	R/W
	For Future Use. This bit is self clear.	

5	**Context Load Protocol Register - CS 5**	
	Default Value:	0b
	Access:	R/W
	For Future Use. This bit is self clear.	

4	**Context Load Protocol Register - CS 4**	
	Default Value:	0b
	Access:	R/W
	For Future Use. This bit is self clear.	

3	**Context Load Protocol Register - CS 3**	
	Default Value:	0b
	Project:	CHV, BSW
	Access:	R/W

		GFX_CTX_LD_PRTCL - Context Load Protocol Register CS	
		Bit 3 = Context Complete. Only valid with Bit 2 asserted and indicates whether the context switching out as complete vs. incomplete. This bit is self clear.	
	2	**Context Load Protocol Register - CS 2**	
		Default Value:	0b
		Access:	R/W
		Context Load Protocol Register (Written by CS) Bit 2 = Request from CS to GAM for context save readiness. GAM will acknowledge appropriated steps taken. This bit is self clear.	
	1	**Context Load Protocol Register - CS 1**	
		Default Value:	0b
		Access:	R/W
		Context Load Protocol Register (Written by CS) Bit 1 = Context Launched. This bit is self clear.	
	0	**Context Load Protocol Register - CS 0**	
		Default Value:	0b
		Access:	R/W
		Context Load Protocol Register (Written by CS) Bit 0 = Context Available. This bit is self clear.	

Context Load Protocol Register VCS0

MFX0_CTX_LD_PRTCL - Context Load Protocol Register VCS0		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000 CHV, BSW	
Size (in bits):	32	
Address:	04008h	

DWord	Bit	Description
0	31:16	**Mask Bits**
		<table><tr><td>Default Value:</td><td>0000h</td></tr><tr><td>Access:</td><td>RO</td></tr></table>
	15	**Context Load Protocol Register - VCS0 15**
		<table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> For Future Use. This bit is self clear.
	14	**Context Load Protocol Register - VCS0 14**
		<table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> For Future Use. This bit is self clear.
	13	**Context Load Protocol Register - VCS0 13**
		<table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> For Future Use. This bit is self clear.
	12	**Context Load Protocol Register - VCS0 12**
		<table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> For Future Use. This bit is self clear.
	11	**Context Load Protocol Register - VCS0 11**
		<table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> For Future Use. This bit is self clear.

MFX0_CTX_LD_PRTCL - Context Load Protocol Register VCS0

	10	**Context Load Protocol Register - VCS0 10**	
		Default Value:	0b
		Access:	R/W
		For Future Use. This bit is self clear.	
	9	**Context Load Protocol Register - VCS0 9**	
		Default Value:	0b
		Access:	R/W
		For Future Use. This bit is self clear.	
	8	**Context Load Protocol Register - VCS0 8**	
		Default Value:	0b
		Access:	R/W
		For Future Use. This bit is self clear.	
	7	**Context Load Protocol Register - VCS0 7**	
		Default Value:	0b
		Access:	R/W
		For Future Use. This bit is self clear.	
	6	**Context Load Protocol Register - VCS0 6**	
		Default Value:	0b
		Access:	R/W
		For Future Use. This bit is self clear.	
	5	**Context Load Protocol Register - VCS0 5**	
		Default Value:	0b
		Access:	R/W
		For Future Use. This bit is self clear.	
	4	**Context Load Protocol Register - VCS0 4**	
		Default Value:	0b
		Access:	R/W
		For Future Use. This bit is self clear.	

MFX0_CTX_LD_PRTCL - Context Load Protocol Register VCS0

3	**Context Load Protocol Register - VCS0 3**	
	Default Value:	0b
	Project:	CHV, BSW
	Access:	R/W
	Bit 3 = Context Complete. Only valid with Bit 2 asserted and indicates whether the context switching out as complete vs. incomplete. This bit is self clear.	

2	**Context Load Protocol Register - VCS0 2**	
	Default Value:	0b
	Access:	R/W
	Context Load Protocol Register (Written by VCS0) Bit 2 = Request from VCS0 to GAM for context save readiness. GAM will acknowledge appropriated steps taken. This bit is self clear.	

1	**Context Load Protocol Register - VCS0 1**	
	Default Value:	0b
	Access:	R/W
	Context Load Protocol Register (Written by VCS0) Bit 1 = Context Launched. This bit is self clear.	

0	**Context Load Protocol Register - VCS0 0**	
	Default Value:	0b
	Access:	R/W
	Context Load Protocol Register (Written by VCS0) Bit 0 = Context Available. This bit is self clear.	

Context Load Protocol Register VCS1

MFX1_CTX_LD_PRTCL - Context Load Protocol Register VCS1		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000 CHV, BSW	
Size (in bits):	32	
Address:	0400Ch	

DWord	Bit	Description
0	31:16	**Mask Bits**
		Default Value: 0000h
		Access: RO
	15	**Context Load Protocol Register - VCS1 15**
		Default Value: 0b
		Access: R/W
		For Future Use. This bit is self clear.
	14	**Context Load Protocol Register - VCS1 14**
		Default Value: 0b
		Access: R/W
		For Future Use. This bit is self clear.
	13	**Context Load Protocol Register - VCS1 13**
		Default Value: 0b
		Access: R/W
		For Future Use. This bit is self clear.
	12	**Context Load Protocol Register - VCS1 12**
		Default Value: 0b
		Access: R/W
		For Future Use. This bit is self clear.
	11	**Context Load Protocol Register - VCS1 11**
		Default Value: 0b
		Access: R/W
		For Future Use. This bit is self clear.

MFX1_CTX_LD_PRTCL - Context Load Protocol Register VCS1

	10	**Context Load Protocol Register - VCS1 10**	
		Default Value:	0b
		Access:	R/W
		For Future Use. This bit is self clear.	
	9	**Context Load Protocol Register - VCS1 9**	
		Default Value:	0b
		Access:	R/W
		For Future Use. This bit is self clear.	
	8	**Context Load Protocol Register - VCS1 8**	
		Default Value:	0b
		Access:	R/W
		For Future Use. This bit is self clear.	
	7	**Context Load Protocol Register - VCS1 7**	
		Default Value:	0b
		Access:	R/W
		For Future Use. This bit is self clear.	
	6	**Context Load Protocol Register - VCS1 6**	
		Default Value:	0b
		Access:	R/W
		For Future Use. This bit is self clear.	
	5	**Context Load Protocol Register - VCS1 5**	
		Default Value:	0b
		Access:	R/W
		For Future Use. This bit is self clear.	
	4	**Context Load Protocol Register - VCS1 4**	
		Default Value:	0b
		Access:	R/W
		For Future Use. This bit is self clear.	

MFX1_CTX_LD_PRTCL - Context Load Protocol Register VCS1

<table>
<tr><td rowspan="5">3</td><td colspan="2">Context Load Protocol Register - VCS1 3</td></tr>
<tr><td>Default Value:</td><td>0b</td></tr>
<tr><td>Project:</td><td>CHV, BSW</td></tr>
<tr><td>Access:</td><td>R/W</td></tr>
<tr><td colspan="2">Bit 3 = Context Complete. Only valid with Bit 2 asserted and indicates whether the context switching out as complete vs. incomplete.
This bit is self clear.</td></tr>

<tr><td rowspan="4">2</td><td colspan="2">Context Load Protocol Register - VCS1 2</td></tr>
<tr><td>Default Value:</td><td>0b</td></tr>
<tr><td>Access:</td><td>R/W</td></tr>
<tr><td colspan="2">Context Load Protocol Register
(Written by VCS1)
Bit 2 = Request from VCS1 to GAM for context save readiness. GAM will acknowledge appropriated steps taken.
This bit is self clear.</td></tr>

<tr><td rowspan="4">1</td><td colspan="2">Context Load Protocol Register - VCS1 1</td></tr>
<tr><td>Default Value:</td><td>0b</td></tr>
<tr><td>Access:</td><td>R/W</td></tr>
<tr><td colspan="2">Context Load Protocol Register
(Written by VCS1)
Bit 1 = Context Launched
This bit is self clear.</td></tr>

<tr><td rowspan="4">0</td><td colspan="2">Context Load Protocol Register - VCS1 0</td></tr>
<tr><td>Default Value:</td><td>0b</td></tr>
<tr><td>Access:</td><td>R/W</td></tr>
<tr><td colspan="2">Context Load Protocol Register
(Written by VCS1)
Bit 0 = Context Available.
This bit is self clear.</td></tr>
</table>

Context Load Protocol Register VEBX

VEBX_CTX_LD_PRTCL - Context Load Protocol Register VEBX		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000 CHV, BSW	
Size (in bits):	32	
Address:	04010h	

DWord	Bit	Description
0	31:16	**Mask Bits**
		Default Value: 0000h
		Access: RO
	15	**Context Load Protocol Register - VEBX 15**
		Default Value: 0b
		Access: R/W
		For Future Use. This bit is self clear.
	14	**Context Load Protocol Register - VEBX 14**
		Default Value: 0b
		Access: R/W
		For Future Use. This bit is self clear.
	13	**Context Load Protocol Register - VEBX 13**
		Default Value: 0b
		Access: R/W
		For Future Use. This bit is self clear.
	12	**Context Load Protocol Register - VEBX 12**
		Default Value: 0b
		Access: R/W
		For Future Use. This bit is self clear.
	11	**Context Load Protocol Register - VEBX 11**
		Default Value: 0b
		Access: R/W
		For Future Use. This bit is self clear.

VEBX_CTX_LD_PRTCL - Context Load Protocol Register VEBX

10	**Context Load Protocol Register - VEBX 10**	
	Default Value:	0b
	Access:	R/W
	For Future Use. This bit is self clear.	

9	**Context Load Protocol Register - VEBX 9**	
	Default Value:	0b
	Access:	R/W
	For Future Use. This bit is self clear.	

8	**Context Load Protocol Register - VEBX 8**	
	Default Value:	0b
	Access:	R/W
	For Future Use. This bit is self clear.	

7	**Context Load Protocol Register - VEBX 7**	
	Default Value:	0b
	Access:	R/W
	For Future Use. This bit is self clear.	

6	**Context Load Protocol Register - VEBX 6**	
	Default Value:	0b
	Access:	R/W
	For Future Use. This bit is self clear.	

5	**Context Load Protocol Register - VEBX 5**	
	Default Value:	0b
	Access:	R/W
	For Future Use. This bit is self clear.	

4	**Context Load Protocol Register - VEBX 4**	
	Default Value:	0b
	Access:	R/W
	For Future Use. This bit is self clear.	

VEBX_CTX_LD_PRTCL - Context Load Protocol Register VEBX

3	**Context Load Protocol Register - VEBX 3**	
	Default Value:	0b
	Project:	CHV, BSW
	Access:	R/W
	Bit 3 = Context Complete. Only valid with Bit 2 asserted and indicates whether the context switching out as complete vs. incomplete. This bit is self clear.	

2	**Context Load Protocol Register - VEBX 2**	
	Default Value:	0b
	Access:	R/W
	Context Load Protocol Register (Written by VEBX) Bit 2 = Request from VEBX to GAM for context save readiness. GAM will acknowledge appropriated steps taken. This bit is self clear.	

1	**Context Load Protocol Register - VEBX 1**	
	Default Value:	0b
	Access:	R/W
	Context Load Protocol Register (Written by VEBX) Bit 1 = Context Launched. This bit is self clear.	

0	**Context Load Protocol Register - VEBX 0**	
	Default Value:	0b
	Access:	R/W
	Context Load Protocol Register (Written by VEBX) Bit 0 = Context Available. This bit is self clear.	

Context Restore Request To TDL

TDL_CONTEXT_RESTORE - Context Restore Request To TDL	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Access:	WO
Size (in bits):	32
Address:	0E440h
Valid Projects:	CHV, BSW

DWord	Bit	Description
0	31:17	**Reserved** Format: MBZ
	16	**Context Restore Mask** Value: 1 Name: Description: Bit 0 and bit 16 both need to be 1 for Context restore request
	15:1	**Reserved** Format: MBZ
	0	**Context Restore** Value: 1 Name: Description: Bit 0 and bit 16 both need to be 1 for Context restore request

Context Save Request To TDL

TDL_CONTEXT_SAVE - Context Save Request To TDL	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Access:	WO
Size (in bits):	32
Address:	0E4FCh
Valid Projects:	CHV, BSW

DWord	Bit	Description
0	31:17	**Reserved** Format: MBZ
	16	**Context Save Mask** <table><tr><td>Value</td><td>Name</td><td>Description</td></tr><tr><td>1</td><td></td><td>Bit 0 and Bit 16 both need to be '1' for Context Save Request</td></tr></table>
	15:1	**Reserved** Format: MBZ
	0	**Context Save** <table><tr><td>Value</td><td>Name</td><td>Description</td></tr><tr><td>1</td><td></td><td>Bit 0 and Bit 16 both need to be '1' for Context Save Request</td></tr></table>

Context Sizes

CXT_SIZE - Context Sizes	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x05655582
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	021A8h

The actual size of a logical rendering context is the amount of data stored/restored during a context switch and is measured in 64B cache lines.

This register will be power context save/restored. Note that this register will default to the correct value, so software should not have to modify it.

DWord	Bit	Description
0	31:27	**Reserved**
		Format: MBZ
	26:24	**Ring Context Size**
		Default Value: 5h
		This field indicates the Ring context data that needs to be save/restored.
	23:16	**Render Context Size**
		Default Value: 65h
		This field indicates the size of the render context data that needs to be save/restored when extended mode is not enabled for a context; this also excludes VF, VFE, and URB context size.
	15:8	**SOL Context Offset**
		Default Value: 55h
		This field indicates the cacheline aligned offset of the SOL context in the render context image starting from Ring Context. Note that in execlist of scheduling Ring context itself is at 4KB offset from LRCA.
	7:0	**VF and VFE State Context Size**
		Default Value: 82h
		This field indicates the amount of VF and VFE unit data context save/restored in cachelines.

Context Status Buffer Contents

<table>
<tr><td colspan="2" align="center">**CTXT_ST_BUF - Context Status Buffer Contents**</td></tr>
<tr><td>Register Space:</td><td>MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td>CHV, BSW</td></tr>
<tr><td>Source:</td><td>PRM</td></tr>
<tr><td>Default Value:</td><td>0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000</td></tr>
<tr><td>Access:</td><td>R/W</td></tr>
<tr><td>Size (in bits):</td><td>384</td></tr>
<tr><td>Trusted Type:</td><td>1</td></tr>
<tr><td>Address:</td><td>02370h-0239Fh</td></tr>
<tr><td>Name:</td><td>Context Status Buffer Contents</td></tr>
<tr><td>ShortName:</td><td>CTXT_ST_BUF_RCSUNIT</td></tr>
<tr><td>Address:</td><td>12370h-1239Fh</td></tr>
<tr><td>Name:</td><td>Context Status Buffer Contents</td></tr>
<tr><td>ShortName:</td><td>CTXT_ST_BUF_VCSUNIT0</td></tr>
<tr><td>Address:</td><td>1A370h-1A39Fh</td></tr>
<tr><td>Name:</td><td>Context Status Buffer Contents</td></tr>
<tr><td>ShortName:</td><td>CTXT_ST_BUF_VECSUNIT</td></tr>
<tr><td>Address:</td><td>1C370h-1C39Fh</td></tr>
<tr><td>Name:</td><td>Context Status Buffer Contents</td></tr>
<tr><td>ShortName:</td><td>CTXT_ST_BUF_VCSUNIT1</td></tr>
<tr><td>Address:</td><td>22370h-2239Fh</td></tr>
<tr><td>Name:</td><td>Context Status Buffer Contents</td></tr>
<tr><td>ShortName:</td><td>CTXT_ST_BUF_BCSUNIT</td></tr>
<tr><td colspan="2">Contents of the Execlist 0 in HW.</td></tr>
</table>

Programming Notes
This structure contains the Context Switch status locations Context Status 0 to Context Status 5.

DWord	Bit	Description	
0	63:32	**Context Status 0 UDW**	
		Format:	Context Status CHV, BSW
	31:0	**Context Status 0 LDW**	
		Format:	Context Status CHV, BSW
1	63:32	**Context Status 1 UDW**	
		Format:	Context Status CHV, BSW

CTXT_ST_BUF - Context Status Buffer Contents

	31:0	**Context Status 1 LDW**	
		Format:	Context Status CHV, BSW
2	63:32	**Context Status 2 UDW**	
		Format:	Context Status CHV, BSW
	31:0	**Context Status 2 LDW**	
		Format:	Context Status CHV, BSW
3	63:32	**Context Status 3 UDW**	
		Format:	Context Status CHV, BSW
	31:0	**Context Status 3 LDW**	
		Format:	Context Status CHV, BSW
4	63:32	**Context Status 4 UDW**	
		Format:	Context Status CHV, BSW
	31:0	**Context Status 4 LDW**	
		Format:	Context Status CHV, BSW
5	63:32	**Context Status 5 UDW**	
		Format:	Context Status CHV, BSW
	31:0	**Context Status 5 LDW**	
		Format:	Context Status CHV, BSW

Control Register for Power Management

WAIT_FOR_RC6_EXIT - Control Register for Power Management		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	020CCh	
Address:	120CCh-120CFh	
Name:	Control Register for Power Management	
ShortName:	WAIT_FOR_RC6_EXIT_VCSUNIT0	
Address:	1A0CCh-1A0CFh	
Name:	Control Register for Power Management	
ShortName:	WAIT_FOR_RC6_EXIT_VECSUNIT	
Address:	1C0CCh-1C0CFh	
Name:	Control Register for Power Management	
ShortName:	WAIT_FOR_RC6_EXIT_VCSUNIT1	
Address:	220CCh-220CFh	
Name:	Control Register for Power Management	
ShortName:	WAIT_FOR_RC6_EXIT_BCSUNIT	

DWord	Bit	Description
	31:16	**Mask Bits** <table><tr><td>Format:</td><td>Mask[15:0]</td></tr></table> Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)
	15:14	**Reserved** <table><tr><td>Format:</td><td>MBZ</td></tr></table>

WAIT_FOR_RC6_EXIT - Control Register for Power Management

0	13	**Selective Read Addressing Enable**		
This register gets power context save/restored. Bit[0] contents of this register doesn't get save/restored.		Project:		CHV, BSW
		This field controls the outbound read request originating from Render Command Streamer. This field enables to read the MMIO register from selected unit in a given slice and sub-slice instead of multicasting the read cycle to all slices/sub-slices.		
		Value	**Name**	**Description**
		0h	**[Default]**	Lowest Slice and Lowest Sub-Slice Enabled. Ex: Slice-0, Sub-Slice-0 are the lowest in GT.
		1h	Selective Unit Enabled	Unit selected based on **Selective Read Slice Select** and **Selective Read Sub-Slice Select**.
	12:11	**Selective Read Slice Select**		
		Project:		CHV, BSW
		This field selects the slice from which the read return data value has to be considered when **Selective Read Addressing Enable** is set. Below value must be programmed with a legal value supported by the GT configuration, one must not program this to a slice that is disabled or not supported by GT.		
		Value		**Name**
		00b		Slice-0
		01b		Slice-1
		10b		Slice-2
		11b		Reserved
	10:9	**Selective Read Sub-Slice Select**		
		Project:		CHV, BSW
		This field selects the sub-slice from which the read return data value has to be considered when **Selective Read Addressing Enable** is set. Below value must be programmed with a legal value supported by the GT configuration, one must not program this to a sub-slice that is disabled or not supported by GT.		
		Value		**Name**
		00b		Sub Slice-0
		01b		Sub Slice-1
		10b		Sub Slice-2
		11b		Reserved

WAIT_FOR_RC6_EXIT - Control Register for Power Management

	8	**Render Inhibit**		

Format: | Disable

Value	Name	Description
0h	Disabled **[Default]**	When not Set CS doesn't take any special action.
1h	Enabled	When Set CS will not save/restore render context as part of power context save/restore. Render context includes RS context as well if enabled.

Programming Notes
If this bit is set S/W should set Resource Streamer Context Enable (Bit[7] of this register)as well.

	7	**Resource Streamer Context Enable**

Format: | Enable

Value	Name	Description
1h	Disable	The current context does not include the resource streamer context
0h	Enable **[Default]**	The current context does include the resource streamer context.

	6	**Selective Write Addressing Enable**

Project: | CHV, BSW

This field controls the outbound write request on message channel originating from Render Command Streamer on executing MI_LOAD_REGISTER_IMM, MI_LOAD_REGISTER_REG and MI_LOAD_REGISTER_MEM commands. Setting this field doesn't affect the execution of MI_LOAD_REGISTER_IMM command from context image during context restore. This field enables to direct the message channel write cycle to the unit in the selected slice and sub-slice instead of multicasting it to all the instances of the unit in all the slices and sub-slices.

Value	Name	Description
0h	Multi Cast **[Default]**	
1h	Selective Unit Enabled	Unit selected based on **Selective Write Slice Select** and **Selective Write Sub-Slice Select**.

WAIT_FOR_RC6_EXIT - Control Register for Power Management

<table>
<tr>
<td>5:4</td>
<td colspan="2">Selective Write Slice Select</td>
</tr>
<tr>
<td></td>
<td>Project:</td>
<td>CHV, BSW</td>
</tr>
<tr>
<td></td>
<td colspan="2">This field selects the slice to which the write has to be done when Selective Write Addressing Enable is set. Below value must be programmed with a legal value supported by the GT configuration, one must not program this to a slice that is disabled or not supported by GT.</td>
</tr>
</table>

Value	Name
00b	Slice-0
01b	Slice-1
10b	Slice-2
11b	Reserved

<table>
<tr>
<td>3:2</td>
<td colspan="2">Selective Write Sub-Slice Select</td>
</tr>
<tr>
<td></td>
<td>Project:</td>
<td>CHV, BSW</td>
</tr>
<tr>
<td></td>
<td colspan="2">This field selects the Sub-Slice to which the write has to be done when Selective Write Addressing Enable is set. Below value must be programmed with a legal value supported by the GT configuration, one must not program this to a sub-slice that is disabled or not supported by GT.</td>
</tr>
</table>

Value	Name
00b	Sub Slice-0
01b	Sub Slice-1
10b	Sub Slice-2
11b	Reserved

<table>
<tr>
<td>1</td>
<td colspan="2">Reserved</td>
</tr>
<tr>
<td></td>
<td>Format:</td>
<td>MBZ</td>
</tr>
<tr>
<td>0</td>
<td colspan="2">WAIT FOR RC6 EXIT</td>
</tr>
<tr>
<td></td>
<td>Format:</td>
<td>Disable</td>
</tr>
</table>

Value	Name	Description
0h	Disabled **[Default]**	When not Set CS doesn't take any action.
1h	Enabled	When Set CS will stop on the next appropriate command boundary and will initiate IDLE sequence with PM.

Programming Notes
WAIT_FOR_RC6_EXIT functionality is only supported in ring buffer mode of scheduling and not supported in execlist mode of scheduling.

Count Active Channels Dispatched

TS_GPGPU_THREADS_DISPATCHED - Count Active Channels Dispatched	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Trusted Type:	1
Address:	02290h

This register is used to count the number of active channels that TS sends for dispatch. For each dispatch the active bits in the execution mask are summed and added to this register. This register is reset when a write occurs to 2290h

DWord	Bit	Description
0	63:32	**GPGPU_THREADS_DISPATCHED UDW**
		Format: U32
		This count is increased by the number of active bits in the execution mask each time the TS sends a GPGPU dispatch.
	31:0	**GPGPU_THREADS_DISPATCHED LDW**
		Format: U32
		This count is increased by the number of active bits in the execution mask each time the TS sends a GPGPU dispatch.

CS Context Timestamp Count

CS_CTX_TIMESTAMP - CS Context Timestamp Count	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	023A8h

This register provides a mechanism to obtain cumulative run time of a GPU context on HW. This register gets context save/restored on a context switch. SW must reset this register on very first submission of a context to HW, then afterwards gets context save/restored maintaining the cumulative run time of the corresponding context. This register (effectively) counts at a constant frequency by adjusting the increment amount according to the actual reference clock frequency. SW therefore does not need to know the reference clock frequency. This register gets reset on an engine reset.

This register is context save restore on a context switch. The time to execute the context switch is included in the CS_CTX_TIMESTAMP register.

DWord	Bit	Description
0	31:0	**Timestamp Value**

		Format:	U32

This register increments for every 80 ns of time.

CS General Purpose Register

CS_GPR - CS General Purpose Register	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Address:	02600h
Name:	CS General Purpose Register 0
ShortName:	CS_GPR_R_0
Address:	02608h
Name:	CS General Purpose Register 1
ShortName:	CS_GPR_R_1
Address:	02610h
Name:	CS General Purpose Register 2
ShortName:	CS_GPR_R_2
Address:	02618h
Name:	CS General Purpose Register 3
ShortName:	CS_GPR_R_3
Address:	02620h
Name:	CS General Purpose Register 4
ShortName:	CS_GPR_R_4
Address:	02628h
Name:	CS General Purpose Register 5
ShortName:	CS_GPR_R_5
Address:	02630h
Name:	CS General Purpose Register 6
ShortName:	CS_GPR_R_6
Address:	02638h
Name:	CS General Purpose Register 7
ShortName:	CS_GPR_R_7
Address:	02640h
Name:	CS General Purpose Register 8
ShortName:	CS_GPR_R_8

CS_GPR - CS General Purpose Register

Address:	02648h
Name:	CS General Purpose Register 9
ShortName:	CS_GPR_R_9

Address:	02650h
Name:	CS General Purpose Register 10
ShortName:	CS_GPR_R_10

Address:	02658h
Name:	CS General Purpose Register 11
ShortName:	CS_GPR_R_11

Address:	02660h
Name:	CS General Purpose Register 12
ShortName:	CS_GPR_R_12

Address:	02668h
Name:	CS General Purpose Register 13
ShortName:	CS_GPR_R_13

Address:	02670h
Name:	CS General Purpose Register 14
ShortName:	CS_GPR_R_14

Address:	02678h
Name:	CS General Purpose Register 15
ShortName:	CS_GPR_R_15

Address:	12600h-12607h
Name:	General Purpose Register
ShortName:	CS_GPR_VCSUNIT0

Address:	1A600h-1A607h
Name:	General Purpose Register
ShortName:	CS_GPR_VECSUNIT

Address:	1C600h-1C607h
Name:	General Purpose Register
ShortName:	CS_GPR_VCSUNIT1

Address:	22600h-22607h
Name:	General Purpose Register
ShortName:	CS_GPR_BCSUNIT

This is a General Purpose Register bank of sixteen 64bit registers, which will be used as temporary storage by MI_MATH command to do ALU operations.

CS_GPR - CS General Purpose Register

GPR Index	MMIO Offset
R_0	0x2600
R_1	0x2608
R_2	0x2610
R_3	0x2618
R_4	0x2620
R_5	0x2628
R_6	0x2630
R_7	0x2638
R_8	0x2640
R_9	0x2648
R_10	0x2650
R_11	0x2658
R_12	0x2660
R_13	0x2668
R_14	0x2670
R_15	0x2678

DWord	Bit	Description
0	63:0	**CS_GPR_DATA**

Project:	CHV, BSW

This register is a temporary register for ALU operations. See MI_MATH command for more details.

CS Power Management FSM

CSPWRFSM - CS Power Management FSM	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	022ACh

This register contains the state code of the Power Management FSM, FBC Forward FSM, CSSTDT FSM, CSARB FSM, CSBUPDATE FSM. Decoding the contents of this register will indicate what the state of the corresponding state machine.

DWord	Bit	Description
0	31:30	**Reserved** Format: MBZ
	29:28	**CSFBCSLICE0** Format: U2 FBC message forward FSM state <table><tr><th>Value</th><th>Name</th></tr><tr><td>0h</td><td>CSFBCIDLE_0</td></tr><tr><td>1h</td><td>CSFBCMODIFY_0</td></tr><tr><td>2h</td><td>CSFBCCLEAN_0</td></tr><tr><td>3h</td><td>CSFBCDONE_0</td></tr></table>
	27:24	**Reserved** Format: MBZ
	23:21	**CS ARB** Format: U3 Overall state of the command streamer. Describes what state CS is in <table><tr><th>Value</th><th>Name</th><th>Project</th></tr><tr><td>0h</td><td>ARBIDLE_s</td><td></td></tr><tr><td>1h</td><td>P0RNG_s CS</td><td></td></tr><tr><td>2h</td><td>P0BATCH_s</td><td></td></tr><tr><td>3h</td><td>ARBCHK</td><td></td></tr><tr><td>4h</td><td>ARBCHK1</td><td></td></tr><tr><td>5h</td><td>CTXOP_s</td><td></td></tr><tr><td>6h</td><td>WABATCH_s</td><td>CHV, BSW</td></tr><tr><td>7h</td><td>PSLBATCH</td><td>CHV, BSW</td></tr></table>

CSPWRFSM - CS Power Management FSM

	20	**Reserved**
		Format: MBZ

19:17 **CSSWITCH**

Format: U3

Arbiters CSSWITCH FSM state decoding.

Value	Name
0h	SWIDLE_s
1h	SWITCH_s
2h	ASREQ_s
3h	DMACHK_s
4h	ARBWAIT_s
5h	FIFORECFG_s
6h-7h	Reserved

16:13 **CSCSBUPDATE**

Format: U4

CS Power Management CSBLOCK FSM state

Value	Name
0h	CSBIDLE
1h	CSQ
2h	WRPTR
3h	SEMA1
4h	SEMA2
5h	TS1
6h	TS2
7h	TS3
8h	TS4
9h	DUMMYREQ
Ah	DUMMYWT
Bh	INTWT
Ch-Fh	Reserved

CSPWRFSM - CS Power Management FSM

12:11	**R2MWRREQ**		
	Format:		U2

CSSTDT memory request FSM state

Value	Name
0h	WRIDLE
1h	WRREQ_HW1
2h	WRREQ_HW2
3h	WRRD

10	**Reserved**	
	Format:	MBZ

9:7	**LOADARB**		
	Format:		U3

CSSTDT arbiter FSM state

Value	Name
0h	LDIDLE
1h	LDAUTO
2h	LDPRSR
3h	LDCTX
4h	LDFLSH
5h	LDREG
6h	LDSHR1

Programming Notes
LOADARB FSM states needs 4 bits for encoding, however only 3bits have been mapped on MMIO. 8h -> LDLRM is the state which is missed out, due to less bits mapped, LDLRM/LDIDLE cant be resolved with certain.

6:4	**CSBLOCK**		
	Format:		U3

CS Power Management CSBLOCK FSM state

Value	Name
0h	CSBLOCK
1h	CSCTXARB
2h	CSUNBLOCKRESTORE
3h	CSUNBLOCK
4h	CSPREP4BLOCK
5h-7h	Reserved

CSPWRFSM - CS Power Management FSM

	3:0	**CSIDLE**	

Format:	U4

CS Power Management CSBLOCK FSM state

Value	Name
0h	CSBUSY
1h	CNTWT
2h	FLSHREQ
3h	FLSHWT
4h	CTXSAVE
5h	CSREQBLOCK
6h	PMTURNOFF
7h	PMIDLEWT
8h	IDLE
9h	PMTURNON
Ah	PMBUSYWT
Bh	DOPFFCGREQ
Ch	DOPFFCGWAIT
Dh	DOPFFCG
Eh	DOPFFCUGREQ
Fh	DOPFFCUGWAIT

CSPREEMPT

<table>
<tr><td colspan="3" align="center">**CSPREEMPT - CSPREEMPT**</td></tr>
<tr><td>Register Space:</td><td colspan="2">MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td colspan="2">CHV, BSW</td></tr>
<tr><td>Source:</td><td colspan="2">RenderCS</td></tr>
<tr><td>Default Value:</td><td colspan="2">0x00000000</td></tr>
<tr><td>Access:</td><td colspan="2">R/W</td></tr>
<tr><td>Size (in bits):</td><td colspan="2">32</td></tr>
<tr><td>Trusted Type:</td><td colspan="2">1</td></tr>
<tr><td>Address:</td><td colspan="2">024B0h</td></tr>
<tr><td colspan="3"></td></tr>
</table>

Programming Notes
This is for HW internal usage and must not be written by SW.

DWord	Bit	Description
0	31:16	**Mask Bits** <table><tr><td>Project:</td><td>CHV, BSW</td></tr><tr><td>Format:</td><td>Mask[15:0]</td></tr></table> Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)
	15:1	**Reserved** <table><tr><td>Project:</td><td>CHV, BSW</td></tr><tr><td>Format:</td><td>MBZ</td></tr></table>
	0	**Unnamed** <table><tr><td>Project:</td><td>CHV, BSW</td></tr><tr><td>Format:</td><td>Disable</td></tr></table> This is a message bit written by the cross CS in case of GT4-CBR/SFR mode of operation. To set this bit both bit[0] and bit[16] (mask) needs to be set. This bit set indicates CS in other GT has reached a preemption point. This bit gets reset by CS when preemption takes place.

CS Reset Control Register

CS_RESET_CTRL - CS Reset Control Register		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	020D0h	
This register is to be used to control soft reset.		

DWord	Bit	Description
0	31:16	**Mask Bits** Format: Mask[15:0] Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)
	15:2	**Reserved** Format: MBZ
	1	**Ready for Reset** Format: U1 When set indicates render engine is ready for reset. This bit gets cleared on engine reset or when Soft Reset In progress is cleared.
	0	**Request Reset** Format: U1 When set indicates SW wishes to reset the render engine. On seeing this bit set Command Streamer will take appropriate action and set Ready For Reset status bit. This bit gets cleared on engine reset. This bit can also be cleared by writing "0" to this bit, this mode of clearing must be only used in debug and validation mode.

Current Context Register

CCID - Current Context Register	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02180h
Address:	12180h-12183h
Name:	Current Context Register
ShortName:	CCID_VCSUNIT0
Address:	1A180h-1A183h
Name:	Current Context Register
ShortName:	CCID_VECSUNIT
Address:	1C180h-1C183h
Name:	Current Context Register
ShortName:	CCID_VCSUNIT1
Address:	22180h-22183h
Name:	Current Context Register
ShortName:	CCID_BCSUNIT

This register contains the current logical rendering context address associated with the ring buffer in ring buffer mode of scheduling. This register contents are not valid in Exec-List mode of scheduling.

Programming Notes
The CCID register must not be written directly (via MMIO) unless the Command Streamer is completely idle (i.e., the Ring Buffer is empty and the pipeline is idle). Note that, under normal conditions, the CCID register should only be updated from the command stream using the MI_SET_CONTEXT command.

DWord	Bit	Description
0	31:12	**Logical Render Context Address (LRCA)**
		Default Value: 0h
		Format: GraphicsAddress[31:12]
		This field contains the 4 KB-aligned Graphics Memory Address of the current Logical Rendering Context. Bit 11 MBZ.
	11:10	**Reserved**
		Format: MBZ

CCID - Current Context Register

<table>
<tr><td>9</td><td colspan="3">HD DVD Context</td></tr>
<tr><td></td><td>Value</td><td>Name</td><td>Description</td></tr>
<tr><td></td><td>0h</td><td>Regular Context</td><td></td></tr>
<tr><td></td><td>1h</td><td>HD DVD Context</td><td>Special considerations for TDP allow for higher voltage and frequency.</td></tr>
<tr><td>8</td><td colspan="3">Reserved</td></tr>
<tr><td></td><td colspan="2">Format:</td><td>Must Be One</td></tr>
<tr><td>7:4</td><td colspan="3">Reserved</td></tr>
<tr><td></td><td colspan="2">Format:</td><td>MBZ</td></tr>
<tr><td>3</td><td colspan="3">Extended State Save Enable</td></tr>
<tr><td></td><td colspan="2">Format:</td><td>Enable</td></tr>
<tr><td></td><td colspan="3">If set, the extended state identified in the Logical Context Data section of the Memory Data Formats chapter, is saved as part of switching away from this logical context.</td></tr>
<tr><td>2</td><td colspan="3">Extended State Restore Enable</td></tr>
<tr><td></td><td colspan="2">Format:</td><td>Enable</td></tr>
<tr><td></td><td colspan="3">If set, the extended state identified in the Logical Context Data section of the Memory Data Formats chapter, was loaded (or restored) as part of switching to this logical context.</td></tr>
<tr><td>1</td><td colspan="3">Reserved</td></tr>
<tr><td></td><td colspan="2">Format:</td><td>MBZ</td></tr>
<tr><td>0</td><td colspan="3">Valid</td></tr>
<tr><td></td><td colspan="2">Format:</td><td>U1</td></tr>
<tr><td></td><td>Value</td><td>Name</td><td>Description</td></tr>
<tr><td></td><td>0h</td><td>Invalid [Default]</td><td>The other fields of this register are invalid. A switch away from the context will not invoke a context save operation.</td></tr>
<tr><td></td><td>1h</td><td>Valid</td><td>The other fields of this register are valid, and a switch from the context will invoke the normal context save/restore operations.</td></tr>
</table>

Current Idle/Busy/Avg Count for Freq Down Recommendation

RPCURDN - Current Idle/Busy/Avg Count for Freq Down Recommendation		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A060h-0A063h	

DWord	Bit	Description
0	31:24	**Reserved**
		Access: RO
	23:0	**Current Busy in Down EI**
		Access: RO
		Reports the current busyness in the down evaluation interval 0 = 0 usec 1 = 1.28 usec 2 = 2.56 usec 3 = 3.84 usec FF FFFF = 21.474 sec pmcr_current_ei_down_busy[23:0]

Current Idle/Busy/Avg Count for Freq Up Recommendation

RPCURUP - Current Idle/Busy/Avg Count for Freq Up Recommendation

Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0A054h-0A057h

DWord	Bit	Description
0	31:24	**Reserved**
		Access: RO
	23:0	**Current Busy in UP EI**
		Access: RO
		Reports the current busyness in the UP evaluation interval 0 = 0 usec 1 = 1.28 usec 2 = 2.56 usec 3 = 3.84 usec FF FFFF = 21.474 sec pmcr_current_ei_up_busy[23:0]

Current Time in DOWN EI

RPCURDNEI - Current Time in DOWN EI		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A05Ch-0A05Fh	

DWord	Bit	Description
0	31:24	**Reserved**
		Access: RO
	23:0	**Current_Time_in_Down_EI**
		Access: RO
		Reports the current Time in the down evaluation interval 0 = 0 usec 1 = 1.28 usec 2 = 2.56 usec 3 = 3.84 usec FF FFFF = 21.474 sec pmcr_current_ei_down_time[23:0]

Current Time in UP EI

RPCURUPEI - Current Time in UP EI		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A050h-0A053h	
DWord	**Bit**	**Description**
0	31:24	**Reserved**
		Access: RO
	23:0	**Current Time**
		Access: RO
		Reports the current time in UP EI
		0 = 0 usec
		1 = 1.28 usec
		2 = 2.56 usec
		3 = 3.84 usec
		FF FFFF = 21.474 sec
		pmcr_current_ei_up_time[23:0]

Customizable Event Creation 0-0

CEC0-0 - Customizable Event Creation 0-0	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02770h
Valid Projects:	CHV, BSW

This register is used to define custom counter event 0, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.

DWord	Bit	Description
0	31:21	**Negate**
			Project:	CHV, BSW	
			Format:	U11	
		The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B | !C)). Note that LSB of this field affects bit 0 of the selected input bus.
			Value	Name	Description	
			0b	Pass-through	Input bit is passed through to comparator as is	
			1b	Negated	Input bit is negated before passing to comparator	
	20:19	**Source Select**
			Format:	U2	
		Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section).
			Value	Name	Description	
			01b	Prev Event	Selects the conditioned/flopped input from the last CEC block as the input bus to CEC0 block	
			11b	Reserved		
	18:3	**Compare Value**
			Format:	U16	
		The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator (see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.

CEC0-0 - Customizable Event Creation 0-0

	2:0	**Compare Function**		
		Format:		U3

This field selects the function used by the CEC0 comparator when comparing the compare value to the value active on the CEC0 conditioned input bus (see block diagram in the Custom Event Counters section).

Value	Name	Description
000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
001b	Greater Than	Compare and assert output if greater than
010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
011b	Greater Than or Equal	Compare and assert output if greater than or equal
100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal
110b	Less Than or Equal	Compare and assert output if less than or equal
111b	Reserved	

Customizable Event Creation 1-0

CEC1-0 - Customizable Event Creation 1-0	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02778h
Valid Projects:	CHV, BSW

 This register is used to define custom counter event 1, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.

DWord	Bit	Description
0	31:21	**Negate**

Project:	CHV, BSW
Format:	U11

 The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B | !C)). Note that LSB of this field affects bit 0 of the selected input bus.

Value	Name	Description
0b	Pass-through	Input bit is passed through to comparator as is
1b	Negated	Input bit is negated before passing to comparator

20:19 Source Select

Format:	U2

 Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section).

Value	Name	Description
01b	Prev Event	Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block
11b	Reserved	

18:3 Compare Value

Format:	U16

The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator (see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.

CEC1-0 - Customizable Event Creation 1-0

2:0	**Compare Function**		
	Format:		U3

This field selects the function used by the CEC comparator when comparing the compare value to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section).

Value	Name	Description
000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
001b	Greater Than	Compare and assert output if greater than
010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
011b	Greater Than or Equal	Compare and assert output if greater than or equal
100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal
110b	Less Than or Equal	Compare and assert output if less than or equal
111b	Reserved	

Customizable Event Creation 2-0

CEC2-0 - Customizable Event Creation 2-0	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02780h
Valid Projects:	CHV, BSW

This register is used to define custom counter event 2, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.

DWord	Bit	Description
0	31:21	**Negate**

Project:	CHV, BSW
Format:	U11

The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B | !C)). Note that LSB of this field affects bit 0 of the selected input bus.

Value	Name	Description
0b	Pass-through	Input bit is passed through to comparator as is
1b	Negated	Input bit is negated before passing to comparator

	20:19	**Source Select**

Format:	U2

Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section).

Value	Name	Description
01b	Prev Event	Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block
11b	Reserved	

	18:3	**Compare Value**

Format:	U16

The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator (see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.

CEC2-0 - Customizable Event Creation 2-0

	2:0	**Compare Function**	

Format:	U3

This field selects the function used by the CEC comparator when comparing the compare value to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section).

Value	Name	Description
000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
001b	Greater Than	Compare and assert output if greater than
010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
011b	Greater Than or Equal	Compare and assert output if greater than or equal
100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal
110b	Less Than or Equal	Compare and assert output if less than or equal
111b	Reserved	

Customizable Event Creation 3-0

CEC3-0 - Customizable Event Creation 3-0	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02788h
Valid Projects:	CHV, BSW

This register is used to define custom counter event 3, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.

DWord	Bit	Description
0	31:21	**Negate**

Project:	CHV, BSW
Format:	U11

The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B | !C)). Note that LSB of this field affects bit 0 of the selected input bus.

Value	Name	Description
0b	Pass-through	Input bit is passed through to comparator as is
1b	Negated	Input bit is negated before passing to comparator

20:19 Source Select

Format:	U2

Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section).

Value	Name	Description
01b	Prev Event	Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block
11b	Reserved	

18:3 Compare Value

Format:	U16

The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator (see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.

Customizable Event Creation 4-0

<table>
<tr><td colspan="3" align="center">**CEC4-0 - Customizable Event Creation 4-0**</td></tr>
<tr><td colspan="3">Register Space: MMIO: 0/2/0</td></tr>
<tr><td colspan="3">Project: CHV, BSW</td></tr>
<tr><td colspan="3">Source: PRM</td></tr>
<tr><td colspan="3">Default Value: 0x00000000</td></tr>
<tr><td colspan="3">Access: R/W</td></tr>
<tr><td colspan="3">Size (in bits):   32</td></tr>
<tr><td colspan="3">Address: 02790h</td></tr>
<tr><td colspan="3">This register is used to define custom counter event 4, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td>**Description**</td></tr>
<tr><td>0</td><td>31:21</td><td>**Negate**

Project: CHV, BSW
Format: U11

The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B | !C)). Note that LSB of this field affects bit 0 of the selected input bus.

Value / Name / Description
0b / Pass-through / Input bit is passed through to comparator as is
1b / Negated / Input bit is negated before passing to comparator</td></tr>
<tr><td></td><td>20:19</td><td>**Source Select**
Format: U2

Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section).

Value / Name / Description
01b / Prev Event / Selects the conditioned/flopped input from the last CEC block as the input bus to CEC0 block
11b / Reserved</td></tr>
<tr><td></td><td>18:3</td><td>**Compare Value**
Format: U16

The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator (see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.</td></tr>
</table>

CEC4-0 - Customizable Event Creation 4-0

	2:0	**Compare Function**	

Format:	U3

This field selects the function used by the CEC comparator when comparing the compare value to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section).

Value	Name	Description
000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
001b	Greater Than	Compare and assert output if greater than
010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
011b	Greater Than or Equal	Compare and assert output if greater than or equal
100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal
110b	Less Than or Equal	Compare and assert output if less than or equal
111b	Reserved	

Customizable Event Creation 5-0

<table>
<tr><td colspan="3" align="center">**CEC5-0 - Customizable Event Creation 5-0**</td></tr>
<tr><td>Register Space:</td><td colspan="2">MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td colspan="2">CHV, BSW</td></tr>
<tr><td>Source:</td><td colspan="2">PRM</td></tr>
<tr><td>Default Value:</td><td colspan="2">0x00000000</td></tr>
<tr><td>Access:</td><td colspan="2">R/W</td></tr>
<tr><td>Size (in bits):</td><td colspan="2">32</td></tr>
<tr><td>Address:</td><td colspan="2">02798h</td></tr>
<tr><td colspan="3">This register is used to define custom counter event 5, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.</td></tr>
</table>

DWord	Bit	Description
0	31:21	**Negate**

Project:	CHV, BSW
Format:	U11

The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B | !C)). Note that LSB of this field affects bit 0 of the selected input bus.

Value	Name	Description	Project
0b	Pass-through	Input bit is passed through to comparator as is	All
1b	Negated	Input bit is negated before passing to comparator	All

20:19 Source Select

Format:		U2

Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section).

Value	Name	Description	Project
01b	Prev Event	Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block	All
11b	Reserved		

18:3 Compare Value

Format:		U16

The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator (see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.

CEC5-0 - Customizable Event Creation 5-0

	2:0	**Compare Function**	

Format:	U3

This field selects the function used by the CEC comparator when comparing the compare value to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section).

Value	Name	Description
000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
001b	Greater Than	Compare and assert output if greater than
010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
011b	Greater Than or Equal	Compare and assert output if greater than or equal
100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal
110b	Less Than or Equal	Compare and assert output if less than or equal
111b	Reserved	

Customizable Event Creation 6-0

<table>
<tr><td colspan="3" align="center">**CEC6-0 - Customizable Event Creation 6-0**</td></tr>
<tr><td colspan="3">Register Space: MMIO: 0/2/0</td></tr>
<tr><td colspan="3">Project: CHV, BSW</td></tr>
<tr><td colspan="3">Source: PRM</td></tr>
<tr><td colspan="3">Default Value: 0x00000000</td></tr>
<tr><td colspan="3">Access: R/W</td></tr>
<tr><td colspan="3">Size (in bits):   32</td></tr>
<tr><td colspan="3">Address: 027A0h</td></tr>
<tr><td colspan="3">This register is used to define custom counter event 6, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.</td></tr>
</table>

DWord	Bit	Description
0	31:21	**Negate**
		Project: CHV, BSW
		Format: U11
		The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B | !C)). Note that LSB of this field affects bit 0 of the selected input bus.

Value	Name	Description	Project
0b	Pass-through	Input bit is passed through to comparator as is	All
1b	Negated	Input bit is negated before passing to comparator	All

DWord	Bit	Description
	20:19	**Source Select**
		Format: U2
		Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section).

Value	Name	Description	Project
01b	Prev Event	Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block	All
11b	Reserved		

DWord	Bit	Description
	18:3	**Compare Value**
		Format: U16
		The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator (see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.

CEC6-0 - Customizable Event Creation 6-0

	2:0	**Compare Function**		
		Format:		U3

This field selects the function used by the CEC comparator when comparing the compare value to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section).

Value	Name	Description
000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
001b	Greater Than	Compare and assert output if greater than
010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
011b	Greater Than or Equal	Compare and assert output if greater than or equal
100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal
110b	Less Than or Equal	Compare and assert output if less than or equal
111b	Reserved	

Customizable Event Creation 7-0

<table>
<tr><td colspan="2" align="center">**CEC7-0 - Customizable Event Creation 7-0**</td></tr>
<tr><td>Register Space:</td><td>MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td>CHV, BSW</td></tr>
<tr><td>Source:</td><td>PRM</td></tr>
<tr><td>Default Value:</td><td>0x00000000</td></tr>
<tr><td>Access:</td><td>R/W</td></tr>
<tr><td>Size (in bits):</td><td>32</td></tr>
</table>

Address:	027A8h

This register is used to define custom counter event 7, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.

DWord	Bit	Description
0	31:21	**Negate** 	Project:	CHV, BSW
Format:	U11	 The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B | !C)). Note that LSB of this field affects bit 0 of the selected input bus. 	Value	Name	Description
0b	Pass-through	Input bit is passed through to comparator as is
1b	Negated	Input bit is negated before passing to comparator	
	20:19	**Source Select** | Format:		U2 | Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section). | Value	Name	Description
01b	Prev Event	Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block
11b	Reserved		
	18:3	**Compare Value** 	Format:		U16	 The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator (see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.

CEC7-0 - Customizable Event Creation 7-0

	2:0	**Compare Function**

Format:	U3

This field selects the function used by the CEC comparator when comparing the compare value to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section).

Value	Name	Description
000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
001b	Greater Than	Compare and assert output if greater than
010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
011b	Greater Than or Equal	Compare and assert output if greater than or equal
100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal
110b	Less Than or Equal	Compare and assert output if less than or equal
111b	Reserved	

CVS TLB LRA 0

CVS_TLB_LRA_0 - CVS TLB LRA 0		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x5F201F00 CHV, BSW	
Size (in bits):	32	
Address:	04A20h	

DWord	Bit	Description
0	31	**Reserved**
		Default Value: — 0b
		Access: — RO
	30:24	**CVS LRA1 Max**
		Default Value: — 1011111b
		Project: — CHV, BSW, :GT2:B
		Access: — R/W
		Maximum value of programmable LRA1.
	23	**Reserved**
		Default Value: — 0b
		Access: — RO
	22:16	**CVS LRA1 Min**
		Default Value: — 0100000b
		Access: — R/W
		Minimum value of programmable LRA1.
	15	**Reserved**
		Default Value: — 0b
		Access: — RO
	14:8	**CVS LRA0 Max**
		Default Value: — 0011111b
		Access: — R/W
		Maximum value of programmable LRA0.
	7	**Reserved**
		Default Value: — 0b
		Access: — RO

CVS_TLB_LRA_0 - CVS TLB LRA 0

	6:0	**CVS LRA0 Min**	
		Default Value:	0000000b
		Access:	R/W
		Minimum value of programmable LRA0.	

CVS TLB LRA 1

<table>
<tr><td colspan="3" align="center">**CVS_TLB_LRA_1 - CVS TLB LRA 1**</td></tr>
<tr><td>Register Space:</td><td colspan="2">MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td colspan="2">CHV, BSW, :GT2:B</td></tr>
<tr><td>Source:</td><td colspan="2">PRM</td></tr>
<tr><td>Default Value:</td><td colspan="2">0x7F007F60</td></tr>
<tr><td>Size (in bits):</td><td colspan="2">32</td></tr>
<tr><td>Address:</td><td colspan="2">04A24h</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td>**Description**</td></tr>
<tr><td>0</td><td>31</td><td>**Reserved**

Default Value: 0b
Access: RO</td></tr>
<tr><td></td><td>30:24</td><td>**CVS LRA3 Max**

Default Value: 1111111b
Access: R/W
For Future Use.</td></tr>
<tr><td></td><td>23</td><td>**Reserved**

Default Value: 0b
Access: RO</td></tr>
<tr><td></td><td>22:16</td><td>**CVS LRA3 Min**

Default Value: 0000000b
Access: R/W
For Future Use.</td></tr>
<tr><td></td><td>15</td><td>**Reserved**

Default Value: 0b
Access: RO</td></tr>
<tr><td></td><td>14:8</td><td>**CVS LRA2 Max**

Default Value: 1111111b
Access: R/W
Maximum value of programmable LRA2.</td></tr>
<tr><td></td><td>7</td><td>**Reserved**

Default Value: 0b
Access: RO</td></tr>
</table>

CVS_TLB_LRA_1 - CVS TLB LRA 1

	6:0	**CVS LRA2 Min**	
		Default Value:	1100000b
		Access:	R/W
		Minimum value of programmable LRA2.	

CVS TLB LRA 2

CVS_TLB_LRA_2 - CVS TLB LRA 2		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW, :GT2:B	
Source:	PRM	
Default Value:	0x0000001A	
Size (in bits):	32	
Address:	04A28h	

DWord	Bit	Description		
0	31:8	**Reserved**		
		Default Value:		000000h
		Access:		RO
	7:6	**RS LRA**		
		Default Value:		00b
		Access:		R/W
		Which LRA should RS use		
	5:4	**CS LRA**		
		Default Value:		01b
		Access:		R/W
		Which LRA should CS use.		
	3:2	**SOL LRA**		
		Default Value:		10b
		Access:		R/W
		Which LRA should SOL use.		
	1:0	**VF LRA**		
		Default Value:		10b
		Access:		R/W
		Which LRA should VF use.		

Depth/Early Depth TLB Partitioning Register

ZSHR - Depth/Early Depth TLB Partitioning Register	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00000020
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	04050h

This register is used to determine the number of TLB entries from the total of 64 available to be used by the Depth partition of the TLB. The rest of the entries are used for the Early Depth/Stencil TLB.

DWord	Bit	Description	
0	31:6	**Reserved**	
		Format:	MBZ
	5:0	**Number of TLB Entries Out of 64 used for Depth TLB**	
		Default Value:	32
		The rest are be used for Early Depth/Stencil TLB. Default value is 32.	

DID

DID - DID		
Register Space:	PCI: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x22B08086 CHV, BSW	
Size (in bits):	32	
Address:	00000h	
D2: PCI Device ID and Vendor ID Register		

DWord	Bit	Description	
0	31:24	**DEVICEID_UB**	
		Default Value:	22h
		Access:	R/W
		DID_MSB: Identifier assigned to the dev2 PCI. Punit will update this bitfield before handing control to BIOS.	
	23:16	**DEVICEID_LB**	
		Default Value:	B0h
		Project:	CHV, BSW
		Access:	RO
		DID_LSB: Identifier assigned to the dev2 PCI. This bitfield is updated from metal straps. CHV, BSW allocated values : 0xB0 0xB1 0xB2 0xB3.	
	23:16	**DEVICEID_LB**	
		Default Value:	B0h
		Project:	CHV, BSW
		Access:	RO
		DID_LSB: Identifier assigned to the dev2 PCI. Bits[7:2] is updated from metal straps. Bits[1:0] will be based on market segment SKU (ie via. fusing) CHV, BSW allocated values : 0xB0 0xB1 0xB2 0xB3.	

DID - DID

	15:0	**VENDORID**	
		Default Value:	8086h
		Access:	RO
		VID: PCI standard identification for Intel	

Display Message Forward Status Register

<table>
<tr>
<td colspan="2" align="center">DISPLAY_MESSAGE_FORWARD_STATUS - Display Message Forward Status Register</td>
</tr>
<tr>
<td>Register Space:</td>
<td>MMIO: 0/2/0</td>
</tr>
<tr>
<td>Project:</td>
<td>CHV, BSW</td>
</tr>
<tr>
<td>Source:</td>
<td>PRM</td>
</tr>
<tr>
<td>Default Value:</td>
<td>0x00000000</td>
</tr>
<tr>
<td>Access:</td>
<td>R/W</td>
</tr>
<tr>
<td>Size (in bits):</td>
<td>32</td>
</tr>
<tr>
<td>Address:
Name:
ShortName:</td>
<td>022E8h
RCS Display Message Forward Status Register
RCS_DISPLAY_MESSAGE_FORWARD_STATUS</td>
</tr>
<tr>
<td>Address:
Name:
ShortName:</td>
<td>122E8h-122EBh
Display Message Forward Status Register
DISPLAY_MESSAGE_FORWARD_STATUS_VCSUNIT0</td>
</tr>
<tr>
<td>Address:
Name:
ShortName:</td>
<td>1A2E8h-1A2EBh
Display Message Forward Status Register
DISPLAY_MESSAGE_FORWARD_STATUS_VECSUNIT</td>
</tr>
<tr>
<td>Address:
Name:
ShortName:</td>
<td>1C2E8h-1C2EBh
Display Message Forward Status Register
DISPLAY_MESSAGE_FORWARD_STATUS_VCSUNIT1</td>
</tr>
<tr>
<td>Address:
Name:
ShortName:</td>
<td>222E8h
BCS Display Message Forward Status Register
BCS_DISPLAY_MESSAGE_FORWARD_STATUS</td>
</tr>
<tr>
<td colspan="2">This register stores the internal HW status flags related to display message forward logic. This register should not be accessed by SW. This register is part of power context image. Note: Even though this register exists in VideoCS and VideoEnhancementCS, individual bit driven functionality is not supported.</td>
</tr>
</table>

DWord	Bit	Description	
0	31:30	**Reserved**	
		Source:	RenderCS, BlitterCS
		Format:	MBZ

DISPLAY_MESSAGE_FORWARD_STATUS - Display Message Forward Status Register

29:28	**Display Pipe Sprite-C3 Flip Done Message Forward**	
	Project:	CHV, BSW
	Source:	RenderCS, BlitterCS

This field has the HW flag for forwarding the Flip Done message to GUC by CS when execlists are enabled.

Value	Name	Description
0h	Never Forward	Never forward the message to GUC.
1h	Always Forward	Always forward the message to GUC unconditionally.
2h	Conditionally Forward	Forward the message to GUC only when the corresponding context is switched out.
3h	Reserved	

27:26	**Display Pipe Sprite-B3 Flip Done Message Forward**	
	Project:	CHV, BSW
	Source:	RenderCS, BlitterCS

This field has the HW flag for forwarding the Flip Done message to GUC by CS when execlists are enabled.

Value	Name	Description
0h	Never Forward	Never forward the message to GUC.
1h	Always Forward	Always forward the message to GUC unconditionally.
2h	Conditionally Forward	Forward the message to GUC only when the corresponding context is switched out.
3h	Reserved	

25:24	**Display Pipe Sprite-A3 Flip Done Message Forward**	
	Project:	CHV, BSW
	Source:	RenderCS, BlitterCS

This field has the HW flag for forwarding the Flip Done message to GUC by CS when execlists are enabled.

Value	Name	Description
0h	Never Forward	Never forward the message to GUC.
1h	Always Forward	Always forward the message to GUC unconditionally.
2h	Conditionally Forward	Forward the message to GUC only when the corresponding context is switched out.
3h	Reserved	

DISPLAY_MESSAGE_FORWARD_STATUS - Display Message Forward Status Register

<table>
<tr><td>23:22</td><td colspan="3">Display Pipe Sprite-C2 Flip Done Message Forward</td></tr>
<tr><td></td><td colspan="2">Project:</td><td>CHV, BSW</td></tr>
<tr><td></td><td colspan="2">Source:</td><td>RenderCS, BlitterCS</td></tr>
<tr><td></td><td colspan="3">This field has the HW flag for forwarding the Flip Done message to GUC by CS when execlists are enabled.</td></tr>
<tr><td></td><td>Value</td><td>Name</td><td>Description</td></tr>
<tr><td></td><td>0h</td><td>Never Forward</td><td>Never forward the message to GUC.</td></tr>
<tr><td></td><td>1h</td><td>Always Forward</td><td>Always forward the message to GUC unconditionally.</td></tr>
<tr><td></td><td>2h</td><td>Conditionally Forward</td><td>Forward the message to GUC only when the corresponding context is switched out.</td></tr>
<tr><td></td><td>3h</td><td>Reserved</td><td></td></tr>
<tr><td>21:20</td><td colspan="3">Display Pipe Sprite-B2 Flip Done Message Forward</td></tr>
<tr><td></td><td colspan="2">Project:</td><td>CHV, BSW</td></tr>
<tr><td></td><td colspan="2">Source:</td><td>RenderCS, BlitterCS</td></tr>
<tr><td></td><td colspan="3">This field has the HW flag for forwarding the Flip Done message to GUC by CS when execlists are enabled.</td></tr>
<tr><td></td><td>Value</td><td>Name</td><td>Description</td></tr>
<tr><td></td><td>0h</td><td>Never Forward</td><td>Never forward the message to GUC.</td></tr>
<tr><td></td><td>1h</td><td>Always Forward</td><td>Always forward the message to GUC unconditionally.</td></tr>
<tr><td></td><td>2h</td><td>Conditionally Forward</td><td>Forward the message to GUC only when the corresponding context is switched out.</td></tr>
<tr><td></td><td>3h</td><td>Reserved</td><td></td></tr>
<tr><td>19:18</td><td colspan="3">Display Pipe Sprite-A2 Flip Done Message Forward</td></tr>
<tr><td></td><td colspan="2">Project:</td><td>CHV, BSW</td></tr>
<tr><td></td><td colspan="2">Source:</td><td>RenderCS, BlitterCS</td></tr>
<tr><td></td><td colspan="3">This field has the HW flag for forwarding the Flip Done message to GUC by CS when execlists are enabled.</td></tr>
<tr><td></td><td>Value</td><td>Name</td><td>Description</td></tr>
<tr><td></td><td>0h</td><td>Never Forward</td><td>Never forward the message to GUC.</td></tr>
<tr><td></td><td>1h</td><td>Always Forward</td><td>Always forward the message to GUC unconditionally.</td></tr>
<tr><td></td><td>2h</td><td>Conditionally Forward</td><td>Forward the message to GUC only when the corresponding context is switched out.</td></tr>
<tr><td></td><td>3h</td><td>Reserved</td><td></td></tr>
</table>

DISPLAY_MESSAGE_FORWARD_STATUS - Display Message Forward Status Register

	17:16	**Display Pipe C Scanline Event Done Message Forward**		
		Source:	RenderCS, BlitterCS	
		This field has the HW flag for forwarding the Scanline Event Done message to GUC by CS when execlists are enabled.		
		Value	**Name**	**Description**
		0h	Never Forward	Never forward the message to GUC.
		1h	Always Forward	Always forward the message to GUC unconditionally.
		2h	Conditionally Forward	Forward the message to GUC only when the corresponding context is switched out.
		3h	Reserved	
	15:14	**Display Pipe B Scanline Event Done Message Forward**		
		Source:	RenderCS, BlitterCS	
		This field has the HW flag for forwarding the Scanline Event Done message to GUC by CS when execlists are enabled.		
		Value	**Name**	**Description**
		0h	Never Forward	Never forward the message to GUC.
		1h	Always Forward	Always forward the message to GUC unconditionally.
		2h	Conditionally Forward	Forward the message to GUC only when the corresponding context is switched out.
		3h	Reserved	
	13:12	**Display Pipe A Scanline Event Done Message Forward**		
		Source:	RenderCS, BlitterCS	
		This field has the HW flag for forwarding the Scanline Event Done message to GUC by CS when execlists are enabled.		
		Value	**Name**	**Description**
		0h	Never Forward	Never forward the message to GUC.
		1h	Always Forward	Always forward the message to GUC unconditionally.
		2h	Conditionally Forward	Forward the message to GUC only when the corresponding context is switched out.
		3h	Reserved	

DISPLAY_MESSAGE_FORWARD_STATUS - Display Message Forward Status Register

	11:10	**Display Pipe Sprite-C Flip Done Message Forward**		
		Source:		RenderCS, BlitterCS
		This field has the HW flag for forwarding the Flip Done message to GUC by CS when execlists are enabled.		
		Value	**Name**	**Description**
		0h	Never Forward	Never forward the message to GUC.
		1h	Always Forward	Always forward the message to GUC unconditionally.
		2h	Conditionally Forward	Forward the message to GUC only when the corresponding context is switched out.
		3h	Reserved	
	9:8	**Display Pipe Sprite-B Flip Done Message Forward**		
		Source:		RenderCS, BlitterCS
		This field has the HW flag for forwarding the Flip Done message to GUC by CS when execlists are enabled.		
		Value	**Name**	**Description**
		0h	Never Forward	Never forward the message to GUC.
		1h	Always Forward	Always forward the message to GUC unconditionally.
		2h	Conditionally Forward	Forward the message to GUC only when the corresponding context is switched out.
		3h	Reserved	
	7:6	**Display Pipe Sprite-A Flip Done Message Forward**		
		Source:		RenderCS, BlitterCS
		This field has the HW flag for forwarding the Flip Done message to GUC by CS when execlists are enabled.		
		Value	**Name**	**Description**
		0h	Never Forward	Never forward the message to GUC.
		1h	Always Forward	Always forward the message to GUC unconditionally.
		2h	Conditionally Forward	Forward the message to GUC only when the corresponding context is switched out.
		3h	Reserved	

		DISPLAY_MESSAGE_FORWARD_STATUS - Display Message Forward Status Register

	5:4	**Display Plane C Flip Done Message Forward**

Source:	RenderCS, BlitterCS

This field has the HW flag for forwarding the Flip Done message to GUC by CS when execlists are enabled.

Value	Name	Description
0h	Never Forward	Never forward the message to GUC.
1h	Always Forward	Always forward the message to GUC unconditionally.
2h	Conditionally Forward	Forward the message to GUC only when the corresponding context is switched out.
3h	Reserved	

	3:2	**Display Plane B Flip Done Message Forward**

Source:	RenderCS, BlitterCS

This field has the HW flag for forwarding the Flip Done message to GUC by CS when execlists are enabled.

Value	Name	Description
0h	Never Forward	Never forward the message to GUC.
1h	Always Forward	Always forward the message to GUC unconditionally.
2h	Conditionally Forward	Forward the message to GUC only when the corresponding context is switched out.
3h	Reserved	

	1:0	**Display Plane A Flip Done Message Forward**

Source:	RenderCS, BlitterCS

This field has the HW flag for forwarding the Flip Done message to GUC by CS when execlists are enabled.

Value	Name	Description
0h	Never Forward	Never forward the message to GUC.
1h	Always Forward	Always forward the message to GUC unconditionally.
2h	Conditionally Forward	Forward the message to GUC only when the corresponding context is switched out.
3h	Reserved	

DS Invocation Counter

<table>
<tr><td colspan="2" align="center">**DS_INVOCATION_COUNT - DS Invocation Counter**</td></tr>
<tr><td>Register Space:</td><td>MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td>CHV, BSW</td></tr>
<tr><td>Source:</td><td>RenderCS</td></tr>
<tr><td>Default Value:</td><td>0x00000000, 0x00000000</td></tr>
<tr><td>Access:</td><td>R/W</td></tr>
<tr><td>Size (in bits):</td><td>64</td></tr>
<tr><td>Trusted Type:</td><td>1</td></tr>
<tr><td>Address:</td><td>02308h</td></tr>
</table>

This register stores the number of domain points shaded by the DS threads. Domain points which hit in the DS cache will not cause this register to increment. Note that the spawning of a DS thread which shades two domain points will cause this counter to increment by two.This register is part of the context save and restore.

DWord	Bit	Description
0	63:32	**DS Invocation Count UDW** Number of domain points shaded by the DS threads. Updated only when DS Function Enable and Statistics Enable are set in 3DSTATE_DS
	31:0	**DS Invocation Count LDW** Number of domain points shaded by the DS threads. Updated only when DS Function Enable and Statistics Enable are set in 3DSTATE_DS

DX9 Constants Not Consumed By RCS

DX9CONST_PRODUCE_COUNT - DX9 Constants Not Consumed By RCS	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	02484h

This register keeps track of the outstanding DX9 Constants produced by RS which are not yet consumed by Render Command Streamer. This register is part of the render context save and restore. This register should not be programmed by SW.

DWord	Bit	Description
0	31:0	**DX9 Constants Produce Count** This register keeps track of the outstanding DX9 Constants produced by RS which are not yet consumed by Render Command Streamer. This register is part of the render context save and restore.

DX9 Constants Prsed By RCS

DX9CONST_PARSE_COUNT - DX9 Constants Prsed By RCS	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	02494h

This register keeps track of the DX9 Constant commands parsed by RCS prior to encountering the Draw Call in an RS enabled Batch Buffer which has DX9 Pool Alloc Valid. DX9 parse count should be less then equal to the DX9 produce count for Command Streamer to make progress on a 3D_PRIMITIVE command. DX9 Parse count is subtracted from the DX9 Produce Count upon parsing 3D_PRIMITIVE command. This register is part of the render context save and restore. This register should not be programmed by SW.

DWord	Bit	Description
0	31:0	**DX9 Constants Produce Count** This register keeps track of the DX9 Constant commands parsed by RCS prior to encountering the Draw Call in an RS enabled Batch Buffer which has DX9 Pool Alloc Valid. DX9 parse count should be less then equal to the DX9 produce count for Command Streamer to make progress on a 3D_PRIMITIVE command. DX9 Parse count is subtracted from the DX9 Produce Count upon parsing 3D_PRIMITIVE command.

ECO Bits - Bus Reset Domain with lock bit

ECOBUS - ECO Bits - Bus Reset Domain with lock bit		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A180h-0A183h	

DWord	Bit	Description
0	31	**ECO Bits - Bus Reset Domain - LOCK BIT**
		Access: R/W Lock
	30	**Reserved**
		Access: RO
	29	**Flush and block gfx pipes during cpd enter**
		Access: R/W Lock
		0 = GFX Pipes will not blocked during CPD enter 1 = GFX Pipes will be blocked and flushed during CPD enter. They will be unblocked again during CPD exit. This bit must not be set to 1
	28	**Block gfx from accessing memory during cpd enter**
		Access: R/W Lock
		0 = GFX will not be blocked from accessing memory during CPD enter 1 = GFX will be blocked from accessing memory (go=0) during CPD enter. They will be unblocked again during CPD exit (go=1).
	27:26	**ECO Bits - Bus Reset Domain1**
		Access: R/W Lock
		Register bits that have no connection to design. Used to enable/disable changes to the design that were put in during the ECO process. pmcr_eco_busrst[26:25]
	25	**CPD GAM GO Messaging Enable**
		Access: R/W Lock
		0 = No GO Messages to GAM during during CPD enter/exit flows (including slice shutdown) (default) 1 = GO Messages to GAM will occur during CPD enter/exit flows (including slice shutdown)

ECOBUS - ECO Bits - Bus Reset Domain with lock bit

24:0	ECO Bits - Bus Reset Domain0	
	Access:	R/W Lock

Description
Register bits that have no connection to design. Used to enable/disable changes to the design that were put in during the ECO process. pmcr_eco_busrst[24:0] ---- [21] = 1 VCS/CS/BCS Idleness, as well as CP/MBC/DT Idleness required for RC6 entry [21] = 0 VCS/CS/BCS Idleness required for RC6 entry ---- [20] - Chicken bit to disable Compensation of RC counters during CPD [19] - Chicken bit to disable Compensation of RP UPEI counter during CPD [18] - Chicken bit to disable Compensation of RP DOWNEI counter during CPD 1 - Disable compensation 0 - Enable compensation of respective counters ---- [17] - Chicken bit to disable Context Save/Restore for WIDI (Win unit) 1 -- Disable WIDI Context Save/Restore 0 -- Enable WIDI Context Save/Restore (Default) ----
[16:15] -- Bits to indicate how many EU's, in each SubSlice, to bring up as part of Render Standby exit 00 -- Bring up 8 EU's (Default) 01 -- Bring up only 6 EU's 10 -- Bring up only 4 EU's 11 -- Bring up just 2 EU's ---- [14:0] are spare bits for ECO process. ----

ECO Bits - Device Reset Domain

ECODEV - ECO Bits - Device Reset Domain	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0A184h-0A187h

DWord	Bit	Description
0	31:0	**ECODEV**

Access:	R/W

Register bits that have no connection to design. Used to enable/disable changes to the design that were put in during the ECO process.
pmcr_eco_bits[31:0]

ECO Message Register

ECO_MSG - ECO Message Register

Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	16

Address:	08040h

Message registers have bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16]. In order to set bit0, for example, the data would be 0x0001_0001. In order to clear bit0, for example, the data would be 0x0001_0000. Note that mask bit is the data bit offset + 16. Message registers are protected from non-GT writes via the Message Channel.

DWord	Bit	Description
0	15	**Placeholder for ECO Bit 15**
		Access: R/W
		ECO Bits 1'b0 : <default> Register definition will be modified if ECOs are required.
	14	**Placeholder for ECO Bit 14**
		Access: R/W
		ECO Bits 1'b0 : <default> Register definition will be modified if ECOs are required.
	13	**Placeholder for ECO Bit 13**
		Access: R/W
		ECO Bits 1'b0 : <default> Register definition will be modified if ECOs are required.
	12	**Placeholder for ECO Bit 12**
		Access: R/W
		ECO Bits 1'b0 : <default> Register definition will be modified if ECOs are required.
	11	**Placeholder for ECO Bit 11**
		Access: R/W
		ECO Bits 1'b0 : <default> Register definition will be modified if ECOs are required.
	10	**Placeholder for ECO Bit 10**
		Access: R/W
		ECO Bits 1'b0 : <default> Register definition will be modified if ECOs are required.

ECO_MSG - ECO Message Register

	9	**Placeholder for ECO Bit 9**	
		Access:	R/W
		ECO Bits 1'b0 : <default> Register definition will be modified if ECOs are required.	
	8	**Placeholder for ECO Bit 8**	
		Access:	R/W
		ECO Bits 1'b0 : <default> Register definition will be modified if ECOs are required.	
	7	**Placeholder for ECO Bit 7**	
		Access:	R/W
		ECO Bits 1'b0 : <default> Register definition will be modified if ECOs are required.	
	6	**Placeholder for ECO Bit 6**	
		Access:	R/W
		ECO Bits 1'b0 : <default> Register definition will be modified if ECOs are required.	
	5	**Placeholder for ECO Bit 5**	
		Access:	R/W
		ECO Bits 1'b0 : <default> Register definition will be modified if ECOs are required.	
	4	**Placeholder for ECO Bit 4**	
		Access:	R/W
		ECO Bits 1'b0 : <default> Register definition will be modified if ECOs are required.	
	3	**Placeholder for ECO Bit 3**	
		Access:	R/W
		ECO Bits 1'b0 : <default> Register definition will be modified if ECOs are required.	
	2	**Placeholder for ECO Bit 2**	
		Access:	R/W
		ECO Bits 1'b0 : <default> Register definition will be modified if ECOs are required.	
	1	**Placeholder for ECO Bit 1**	
		Access:	R/W
		ECO Bits 1'b0 : <default> Register definition will be modified if ECOs are required.	
	0	**Placeholder for ECO Bit 0**	
		Access:	R/W
		ECO Bits 1'b0 : <default> Register definition will be modified if ECOs are required.	

ECO Reserved

<table>
<tr><td colspan="3" align="center">**ECOResrv - ECO Reserved**</td></tr>
<tr><td>Register Space:</td><td colspan="2">MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td colspan="2">CHV, BSW</td></tr>
<tr><td>Source:</td><td colspan="2">PRM</td></tr>
<tr><td>Default Value:</td><td colspan="2">0x00000000</td></tr>
<tr><td>Size (in bits):</td><td colspan="2">32</td></tr>
<tr><td>Address:</td><td colspan="2">09898h</td></tr>
<tr><td colspan="3">ECO Reserved bits</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td>**Description**</td></tr>
<tr><td>0</td><td>31:0</td><td>**ECO Reserved Bits**
<table><tr><td>Access:</td><td>R/WC</td></tr></table></td></tr>
</table>

ECREQ

<table>
<tr><td colspan="2" align="center">**ECREQ - ECREQ**</td></tr>
<tr><td>Register Space:</td><td>MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td>CHV, BSW</td></tr>
<tr><td>Source:</td><td>PRM</td></tr>
<tr><td>Default Value:</td><td>0x00000000</td></tr>
<tr><td>Size (in bits):</td><td>32</td></tr>
<tr><td>Address:</td><td>1300A0h</td></tr>
</table>

This register contains the energy counter request bit.

DWord	Bit	Description
0	31:1	**SPARE**
		Default Value: 00000000h
		Access: R/W
		Spare bits for Duty cycle control feature.
	0	**Energy Count Request**
		Default Value: 0b
		Access: WO
		WO access type of this register means that it will always return a zero when read. A write will generate a one CZ clock wide pulse to indicate that Punit requests for Gunit to push the energy counters. This pulse will only be created when both the data attempted to be written is one and when the byte enables allow the write.

Element Descriptor Register

ELEM_DESCRIPTOR - Element Descriptor Register	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000, 0x00000000
Access:	RO
Size (in bits):	64

Address:	04500h
Name:	BCS Element Descriptor Register
ShortName:	BCS_ELEM_DESCRIPTOR

Address:	04400h
Name:	RCS Element Descriptor Register
ShortName:	RCS_ELEM_DESCRIPTOR

Address:	04440h
Name:	VCS Element Descriptor Register
ShortName:	VCS_ELEM_DESCRIPTOR

Address:	044C0h
Name:	VECS Element Descriptor Register
ShortName:	VECS_ELEM_DESCRIPTOR

Element Information: The register is populated by command streamer and consumed by GAM

DWord	Bit	Description
0	63:32	**Context ID** Context identification number assigned to separate this context from others. Context IDs needs to be recycled in such a way that there could not be two active context with the same ID. This is a unique identification number by which a context is identified and referenced
	31:12	**LRCA** Command Streamer Only
	11:9	**Function Number** GFX device is considered to be on Bus0 with device number of 2. Function number is normally assigned as "0" however for gfx virtualization; there would be different function numbers which needs to be attached to context. Not used in Gen8.

ELEM_DESCRIPTOR - Element Descriptor Register

<table>
<tr><td>8</td><td colspan="3">Privileged Context / GGTT vs PPGTT mode
In Legacy Context: Defines the page tables to be used. This is how page walker come to know PPGTT vs GGTT selection for the entire context. In Advanced Context: Defines the privilege level for the context</td></tr>
<tr><td></td><td>Value</td><td>Name</td><td>Description</td></tr>
<tr><td></td><td>0h</td><td>[Default]</td><td>Use Global GTT (In Legacy Context) User Mode Context (In Advanced Context)</td></tr>
<tr><td></td><td>1h</td><td></td><td>Use Per-Process GTT (In Legacy Context) Supervisor Mode Context (In Advanced Context)</td></tr>
<tr><td>7:6</td><td colspan="3">Fault Model</td></tr>
<tr><td></td><td>Value</td><td>Name</td><td>Description</td></tr>
<tr><td></td><td>00h</td><td>[Default]</td><td>Fault and Hang (chicken bit to survive). Same mode as gen7.5</td></tr>
<tr><td></td><td>01h</td><td></td><td>Fault and Halt/Wait. Same mode as gen7.5</td></tr>
<tr><td></td><td>10h</td><td></td><td>Fault and Stream and Switch</td></tr>
<tr><td></td><td>11h</td><td></td><td>Fault and Continue (reserved for gen8) - does not generate a page request to IOMMU.</td></tr>
<tr><td>5</td><td colspan="3">Deeper IA coherency Support
In Advanced Context: Defines the level of IA coherency</td></tr>
<tr><td></td><td>Value</td><td>Name</td><td>Description</td></tr>
<tr><td></td><td>0h</td><td>[Default]</td><td>IA coherency is provided at LLC level for all streams of GPU (i.e. gen7.5 like mode)</td></tr>
<tr><td></td><td>1h</td><td></td><td>IA coherency is provided at L3 level for EU data accesses of GPU</td></tr>
<tr><td>4</td><td colspan="3">A and D Support / 32 and 64b Address Support
In Legacy Context: Defines 32b vs 64b (48b canonical) addressing format In Advanced Context: Defines A/D bit support</td></tr>
<tr><td></td><td>Value</td><td>Name</td><td>Description</td></tr>
<tr><td></td><td>0h</td><td>[Default]</td><td>32b addressing format (In Legacy Context) A/D bit management in page tables is NOT supported (In Advanced Context)</td></tr>
<tr><td></td><td>1h</td><td></td><td>64b (48b canonical) addressing format (In Legacy Context) A/D bit management in page tables is supported (In Advanced Context)</td></tr>
<tr><td>3</td><td colspan="3">Context Type: Legacy vs Advanced
Defines the context type. Note that: Bits [8:4] differs in functions when legacy vs advanced context modes are selected.</td></tr>
<tr><td></td><td>Value</td><td>Name</td><td>Description</td></tr>
<tr><td></td><td>0h</td><td>[Default]</td><td>Advanced Context: Defines the rest of the advanced capabilities (i.e. OS page table support, fault models...). Note that advanced context is not bounded to GPGPU.</td></tr>
<tr><td></td><td>1h</td><td></td><td>Legacy Context: Defines the context as legacy mode which is similar to prior generations of gen8.</td></tr>
</table>

ELEM_DESCRIPTOR - Element Descriptor Register

	2	**FR** Command Streamer Specific
	1	**Scheduling Mode**

Project:	

Value	Name	Description
0h	**[Default]**	Indicates execlist mode of scheduling.
1h		Indicates Ring Buffer mode of scheduling.

	0	**Valid** Indicates that element descriptor is valid. If GAM is programmed with an invalid descriptor, it will continue but flag an error.

Error_Identity_Reg

EIR - Error_Identity_Reg	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	020B0h-020B3h
Name:	Error Identity Register
ShortName:	EIR_RCSUNIT
Address:	120B0h-120B3h
Name:	Error Identity Register
ShortName:	EIR_VCSUNIT0
Address:	1A0B0h-1A0B3h
Name:	Error Identity Register
ShortName:	EIR_VECSUNIT
Address:	1C0B0h-1C0B3h
Name:	Error Identity Register
ShortName:	EIR_VCSUNIT1
Address:	220B0h-220B3h
Name:	Error Identity Register
ShortName:	EIR_BCSUNIT
Address:	1820B0h

Error Identity. This register contains the persistent values of ESR error status bits that are unmasked via the EMR register.

The logical OR of all (defined) bits in this register is reported in the Master Error bit of the Interrupt Status Register (ISR).

In order to clear an error condition, software must first clear the error by writing a 1 to the appropriate bit(s) in this field.

If required, software should then proceed to clear the Master Error bit of the IIR

DWord	Bit	Description	
0	31:7	**RESERVED**	
		Default Value:	0000000h
		Access:	RO
		Reserved	
	6	**Gunit_TLB_DataE**	
		Default Value:	0b

EIR - Error_Identity_Reg

		Access:		R/W One Clear
		Set if Gunit TLB has a data valid error		
	5	**Gunit_TLB_PTE**		
		Default Value:		0b
		Access:		R/W One Clear
		Set if Gunit TLB has a PTE translation error.		
	4	**PAGE_TABLE_ERROR**		
		Default Value:		0b
		Access:		R/W One Clear
		PTE: This bit is set when a Graphics Memory Mapping Error is detected and it's not EMR masked. The cause of the error is indicated (to some extent) in the PGTBL_ER register. This error condition cannot be cleared except by reset (i.e., it is a fatalerror) mir_EIR[4] = (((dsp_gvd_invldgttpte_int_dczfwoh and ~mir_EMR[4])	mir_EIR[4]) and ~(sys_wdata[4] and mir_write and mirb0_decode and ~sys_data_mask[0]));		
	3:1	**RESERVED**		
		Default Value:		0h
		Access:		RO
		Reserved		
	0	**CLAIM_ERROR**		
		Default Value:		0b
		Access:		R/W One Clear
		If EMR[0]=1, this bit is set when an address within Gunit address space is accessed, but no memory mapped register exists in this address. This error condition can be cleared by writing 1b to this bit. Mir_EIR[0] = (((noRMclaim_err and ~mir_EMR[0]) |mir_EIR[0]) and ~(sys_wdata[0] and mir_write and mirb0_decode and ~sys_data_mask[0]));		

Error_Mask_Reg

<table>
<tr><td colspan="4" align="center">EMR - Error_Mask_Reg</td></tr>
<tr><td colspan="2">Register Space:</td><td colspan="2">MMIO: 0/2/0</td></tr>
<tr><td colspan="2">Project:</td><td colspan="2">CHV, BSW</td></tr>
<tr><td colspan="2">Source:</td><td colspan="2">PRM</td></tr>
<tr><td colspan="2">Default Value:</td><td colspan="2">0x00000071</td></tr>
<tr><td colspan="2">Size (in bits):</td><td colspan="2">32</td></tr>
<tr><td colspan="2">Address:</td><td colspan="2">020B4h-020B7h</td></tr>
<tr><td colspan="2">Name:</td><td colspan="2">Error Mask Register</td></tr>
<tr><td colspan="2">ShortName:</td><td colspan="2">EMR_RCSUNIT</td></tr>
<tr><td colspan="2">Address:</td><td colspan="2">120B4h-120B7h</td></tr>
<tr><td colspan="2">Name:</td><td colspan="2">Error Mask Register</td></tr>
<tr><td colspan="2">ShortName:</td><td colspan="2">EMR_VCSUNIT0</td></tr>
<tr><td colspan="2">Address:</td><td colspan="2">1A0B4h-1A0B7h</td></tr>
<tr><td colspan="2">Name:</td><td colspan="2">Error Mask Register</td></tr>
<tr><td colspan="2">ShortName:</td><td colspan="2">EMR_VECSUNIT</td></tr>
<tr><td colspan="2">Address:</td><td colspan="2">1C0B4h-1C0B7h</td></tr>
<tr><td colspan="2">Name:</td><td colspan="2">Error Mask Register</td></tr>
<tr><td colspan="2">ShortName:</td><td colspan="2">EMR_VCSUNIT1</td></tr>
<tr><td colspan="2">Address:</td><td colspan="2">220B4h-220B7h</td></tr>
<tr><td colspan="2">Name:</td><td colspan="2">Error Mask Register</td></tr>
<tr><td colspan="2">ShortName:</td><td colspan="2">EMR_BCSUNIT</td></tr>
<tr><td colspan="2">Address:</td><td colspan="2">1820B4h</td></tr>
<tr><td colspan="4">Error Mask. This register contains a bit mask that selects which error condition bits (from the ESR) are reported in the EIR</td></tr>
<tr><td>DWord</td><td>Bit</td><td colspan="2">Description</td></tr>
<tr><td rowspan="2">0</td><td>31:7</td><td colspan="2">RESERVED
Default Value: 0000000h
Access: RO
Reserved</td></tr>
<tr><td>6</td><td colspan="2">Gunit_TLB_DataE
Default Value: 1b
Access: R/W
1 = Masked. This error will neither be reported in the EIR, nor set the master error condition in the IIR.
0 = Unmasked. This interrupt will be reported in the EIR and will set the master error condition in the IIR.</td></tr>
</table>

		EMR - Error_Mask_Reg		
	5	**Gunit_TLB_PTE**		
		Default Value:		1b
		Access:		R/W
		1 = Masked. This error will neither be reported in the EIR, nor set the master error condition in the IIR. 0 = Unmasked. This interrupt will be reported in the EIR and will set the master error condition in the IIR.		
	4	**PAGE_TABLE_ERROR**		
		Default Value:		1b
		Access:		R/W
		1 = Masked. This error will neither be reported in the EIR, nor set the master error condition in the IIR. 0 = Unmasked. This interrupt will be reported in the EIR and will set the master error condition in the IIR.		
	3:1	**RESERVED**		
		Default Value:		0h
		Access:		RO
		Reserved		
	0	**CLAIM_ERROR**		
		Default Value:		1b
		Access:		R/W
		1 = Masked. This error will neither be reported in the EIR, nor set the master error condition in the IIR. 0 = Unmasked. This interrupt will be reported in the EIR and will set the master error condition in the IIR.		

Error_Status_Reg

<table>
<tr><td colspan="4" align="center">**ESR - Error_Status_Reg**</td></tr>
<tr><td>Register Space:</td><td colspan="3">MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td colspan="3">CHV, BSW</td></tr>
<tr><td>Source:</td><td colspan="3">PRM</td></tr>
<tr><td>Default Value:</td><td colspan="3">0x00000000</td></tr>
<tr><td>Size (in bits):</td><td colspan="3">32</td></tr>
<tr><td>Address:</td><td colspan="3">020B8h-020BBh</td></tr>
<tr><td>Name:</td><td colspan="3">Error Status Register</td></tr>
<tr><td>ShortName:</td><td colspan="3">ESR_RCSUNIT</td></tr>
<tr><td>Address:</td><td colspan="3">120B8h-120BBh</td></tr>
<tr><td>Name:</td><td colspan="3">Error Status Register</td></tr>
<tr><td>ShortName:</td><td colspan="3">ESR_VCSUNIT0</td></tr>
<tr><td>Address:</td><td colspan="3">1A0B8h-1A0BBh</td></tr>
<tr><td>Name:</td><td colspan="3">Error Status Register</td></tr>
<tr><td>ShortName:</td><td colspan="3">ESR_VECSUNIT</td></tr>
<tr><td>Address:</td><td colspan="3">1C0B8h-1C0BBh</td></tr>
<tr><td>Name:</td><td colspan="3">Error Status Register</td></tr>
<tr><td>ShortName:</td><td colspan="3">ESR_VCSUNIT1</td></tr>
<tr><td>Address:</td><td colspan="3">220B8h-220BBh</td></tr>
<tr><td>Name:</td><td colspan="3">Error Status Register</td></tr>
<tr><td>ShortName:</td><td colspan="3">ESR_BCSUNIT</td></tr>
<tr><td>Address:</td><td colspan="3">1820B8h</td></tr>
<tr><td colspan="4">Error Status. This register contains the non-persistent values of all hardware-detected error condition bits.</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td colspan="2">**Description**</td></tr>
<tr><td rowspan="7">0</td><td rowspan="4">31:7</td><td colspan="2">**RESERVED**</td></tr>
<tr><td>Default Value:</td><td>0000000h</td></tr>
<tr><td>Access:</td><td>RO</td></tr>
<tr><td colspan="2">Reserved</td></tr>
<tr><td rowspan="3">6</td><td colspan="2">**Gunit_TLB_DataE**</td></tr>
<tr><td>Default Value:</td><td>0b</td></tr>
<tr><td>Access:</td><td>RO</td></tr>
<tr><td></td><td></td><td colspan="2">1 = This error condition currently exists.
0 = This error condition currently does not exist</td></tr>
</table>

ESR - Error_Status_Reg

	5	**Gunit_TLB_PTE**	
		Default Value:	0b
		Access:	RO
		1 = This error condition currently exists. 0 = This error condition currently does not exist	
	4	**PAGE_TABLE_ERROR**	
		Default Value:	0b
		Access:	RO
		1 = This error condition currently exists. 0 = This error condition currently does not exist(Was reported based on 0x18_2024h "OR".	
	3:1	**RESERVED**	
		Default Value:	0h
		Access:	RO
		Reserved	
	0	**CLAIM_ERROR**	
		Default Value:	0b
		Access:	RO
		No RMbus claim occurred. Logging the error. 1 = This error condition currently exists. 0 = This error condition currently does not exist. Internal Gunit 'noRMclaim_err' wire from RMbus master.	

Error Identity Register

<table>
<tr><td colspan="2" align="center">**EIR - Error Identity Register**</td></tr>
<tr><td>Register Space:</td><td>MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td>CHV, BSW</td></tr>
<tr><td>Source:</td><td>RenderCS</td></tr>
<tr><td>Default Value:</td><td>0x00000000</td></tr>
<tr><td>Access:</td><td>R/W, RO</td></tr>
<tr><td>Size (in bits):</td><td>32</td></tr>
<tr><td>Address:</td><td>020B0h</td></tr>
</table>

The EIR register contains the persistent values of Hardware-Detected Error Condition bits. Any bit set in this register will cause the Master Error bit in the ISR to be set. The EIR register is also used by software to clear detected errors (by writing a 1 to the appropriate bit(s)), except for the unrecoverable bits described.)

Restriction
Restriction https://vthsd.iind.intel.com/hsd/gen9lp/bug_de/default.aspx?bug_de_id=2131892 : EIR register contents are not power or render context save/restored. EIR register contents of an engine will get lost when the corresponding graphics engine (Render, Video, Vidoe Enhancement, Blitter) is power down.

DWord	Bit	Description
0	31:16	**Reserved**
		Format: MBZ
	15:0	**Error Identity Bits**
		Format: Array of Error condition bits See the table titled Hardware-Detected Error Bits.
		This register contains the persistent values of ESR error status bits that are unmasked via the EMR register. (See Table Table 3-3. Hardware-Detected Error Bits). The logical OR of all (defined) bits in this register is reported in the Master Error bit of the Interrupt Status Register. In order to clear an error condition, software must first clear the error by writing a 1 to the appropriate bit(s) in this field. If required, software should then proceed to clear the Master Error bit of the IIR. Reserved bits are RO.

Value	Name
1h	Error occurred

Programming Notes
Writing a 1 to a set bit will cause that error condition to be cleared. However, neither the Page Table Error bit (Bit 4) nor the Instruction Error bit (Bit 0) can be cleared except by reset (i.e., it is a fatal error).

Error Mask Register

<table>
<tr><td colspan="2" align="center">**EMR - Error Mask Register**</td></tr>
<tr><td>Register Space:</td><td>MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td>CHV, BSW</td></tr>
<tr><td>Source:</td><td>RenderCS</td></tr>
<tr><td>Default Value:</td><td>0xFFFFFFFF</td></tr>
<tr><td>Access:</td><td>R/W, RO</td></tr>
<tr><td>Size (in bits):</td><td>32</td></tr>
<tr><td>Address:</td><td>020B4h</td></tr>
</table>

The EMR register is used by software to control which Error Status Register bits are masked or unmasked. Unmasked bits will be reported in the EIR, thus setting the Master Error ISR bit and possibly triggering a CPU interrupt, and will persist in the EIR until cleared by software. Masked bits will not be reported in the EIR and therefore cannot generate Master Error conditions or CPU interrupts. Reserved bits are RO.

DWord	Bit	Description
0	31:8	**Reserved**

Default Value:	FFFFFFh
Format:	Must Be One

Programming Notes
These bits are not implemented in HW and must be set to '1'

	7:0	**Error Mask Bits**

Format:	Array of error condition mask bits See the table titled Hardware-Detected Error Bits.

This register contains a bit mask that selects which error condition bits (from the ESR) are reported in the EIR.

Value	Name	Description
FFh	**[Default]**	
0h	Not Masked	Will be reported in the EIR
1h	Masked	Will not be reported in the EIR

Error Reporting Register

<table>
<tr><td colspan="2" align="center">**ERR - Error Reporting Register**</td></tr>
<tr><td>Register Space:</td><td>MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td>CHV, BSW</td></tr>
<tr><td>Source:</td><td>PRM</td></tr>
<tr><td>Default Value:</td><td>0x00000000</td></tr>
<tr><td>Size (in bits):</td><td>32</td></tr>
<tr><td>Address:</td><td>0B42Ch</td></tr>
</table>

DWord	Bit	Description
0	31:5	**Reserved** Access: RO Reserved.
	4	**First Content Buffer Ready 0** Access: R/W First Content Buffer Ready 0 (FRSNTBFR0). First Content Buffer Ready: This bit gets set by the HW when the buffer is completely filled up and cleared by the driver when the contents of this buffer are copied out of memory. Is set by lpfc_lpconf_buffer0_ready (pulse). lpconf_lpfc_buffer0_ready (static signal to lpfc).
	3	**Second Buffer ready slice 0** Access: R/W Second Content Buffer Ready slice 0 (SCNBFR0). Second Content Buffer Ready: This bit gets set by the HW when the buffer is completely filled up and cleared by the driver when the contents of this buffer are copied out of memory. Is set by lpfc_lpconf_buffer1_ready (pulse). lpconf_lpfc_buffer1_ready (static signal to lpfc).
	2	**Write Expire Error Slice 0** Access: R/W Write Expired Error slice 0 (WEERR0). Write Expired Error: If DMA controller could not get a chance to push the write of 64Bytes to LTISEQ and data gets clobbered with the new expiration of the save timer, this error bit is set to indicate something went wrong. Signal -lpfc_lpconf_wrexp_error.
	1	**Buffer full Error Slice 0** Access: R/W Buffer full Error Slice 0 (BFFLERR0). Set by lpfc_lpconf_error_buffer_full. When all buffers are full lpfc sets this bit or if only 1 buffer is enabled then lpfc sets this bit when the buffer is full.

ERR - Error Reporting Register

	0	**Reserved**	
		Access:	RO
		Reserved.	

Error Status Register

<table>
<tr><td colspan="2" align="center">**ESR - Error Status Register**</td></tr>
<tr><td>Register Space:</td><td>MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td>CHV, BSW</td></tr>
<tr><td>Source:</td><td>RenderCS</td></tr>
<tr><td>Default Value:</td><td>0x00000000</td></tr>
<tr><td>Access:</td><td>RO</td></tr>
<tr><td>Size (in bits):</td><td>32</td></tr>
<tr><td>Address:</td><td>020B8h</td></tr>
</table>

The ESR register contains the current values of all Hardware-Detected Error condition bits (these are all by definition persistent). The EMR register selects which of these error conditions are reported in the persistent EIR (i.e., set bits must be cleared by software) and thereby causing a Master Error interrupt condition to be reported in the ISR.

DWord	Bit	Description
0	31:16	**Reserved**
		Format: MBZ
	15:0	**Error Status Bits**
		Format: Array of error condition bits See the table titled Hardware-Detected Error Bits.
		This register contains the non-persistent values of all hardware-detected error condition bits.

Value	Name
1h	Error Condition Detected

EU Mask Programming

TD_PM_MODE_EUCOUNT - EU Mask Programming	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Access:	WO
Size (in bits):	32
Address:	0E4F8h
Name:	EU Mask Programming Slice 0
ShortName:	TD_PM_MODE_EUCOUNT_S0
Valid Projects:	CHV, BSW
Address:	0E5F8h
Name:	EU Mask Programming Slice 1
ShortName:	TD_PM_MODE_EUCOUNT_S1
Valid Projects:	CHV, BSW
Address:	0E6F8h
Name:	EU Mask Programming Slice 2
ShortName:	TD_PM_MODE_EUCOUNT_S2
Valid Projects:	CHV, BSW

DWord	Bit	Description	
0	31:24	**Reserved**	
		Project:	CHV, BSW
		Format:	MBZ
	23	**SubSlice 2 EU 7 Enable**	
		Format:	Enable
	22	**SubSlice 2 EU 6 Enable**	
		Format:	Enable
	21	**SubSlice 2 EU 5 Enable**	
		Format:	Enable
	20	**SubSlice 2 EU 4 Enable**	
		Format:	Enable
	19	**SubSlice 2 EU 3 Enable**	
		Format:	Enable
	18	**SubSlice 2 EU 2 Enable**	

TD_PM_MODE_EUCOUNT - EU Mask Programming

		Format:	Enable
	17	**SubSlice 2 EU 1 Enable**	
		Format:	Enable
	16	**SubSlice 2 EU 0 Enable**	
		Format:	Enable
	15	**SubSlice 1 EU 7 Enable**	
		Format:	Enable
	14	**SubSlice 1 EU 6 Enable**	
		Format:	Enable
	13	**SubSlice 1 EU 5 Enable**	
		Format:	Enable
	12	**SubSlice 1 EU 4 Enable**	
		Format:	Enable
	11	**SubSlice 1 EU 3 Enable**	
		Format:	Enable
	10	**SubSlice 1 EU 2 Enable**	
		Format:	Enable
	9	**SubSlice 1 EU 1 Enable**	
		Format:	Enable
	8	**SubSlice 1 EU 0 Enable**	
		Format:	Enable
	7	**SubSlice 0 EU 7 Enable**	
		Format:	Enable
	6	**SubSlice 0 EU 6 Enable**	
		Format:	Enable
	5	**SubSlice 0 EU 5 Enable**	
		Format:	Enable
	4	**SubSlice 0 EU 4 Enable**	
		Format:	Enable
	3	**SubSlice 0 EU 3 Enable**	
		Format:	Enable
	2	**SubSlice 0 EU 2 Enable**	
		Format:	Enable
	1	**SubSlice 0 EU 1 Enable**	
		Format:	Enable

TD_PM_MODE_EUCOUNT - EU Mask Programming

	0	SubSlice 0 EU 0 Enable	
		Format:	Enable

EU Metrics for Event0 High

EUMETRICSEVENT0H - EU Metrics for Event0 High		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	138134h	
Upper 32 bits of the EU Metrics Event0		

DWord	**Bit**	**Description**	
0	31:0	**EUMetrics, Event0 High**	
		Default Value:	00000000h
		Access:	RO
		Contains Upper 32 bits of EU Metrics, Event0	

EU Metrics for Event0 Low

<table>
<tr><td colspan="3" align="center">**EUMETRICSEVENT0L - EU Metrics for Event0 Low**</td></tr>
<tr><td>Register Space:</td><td colspan="2">MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td colspan="2">CHV, BSW</td></tr>
<tr><td>Source:</td><td colspan="2">PRM</td></tr>
<tr><td>Default Value:</td><td colspan="2">0x00000000</td></tr>
<tr><td>Size (in bits):</td><td colspan="2">32</td></tr>
<tr><td>Address:</td><td colspan="2">138130h</td></tr>
<tr><td colspan="3">Lower 14 bits of the EU Metrics Event0</td></tr>
</table>

DWord	Bit	Description
0	31:18	**EUMetrics, Event0 Low**
		Default Value: 0000h
		Access: RO
		Contains lower 14 bits of EU Metrics, Event0
	17:0	**Reserved**
		Default Value: 00000h
		Access: RO
		Reserved

EU Metrics for Event1 High

EUMETRICSEVENT1H - EU Metrics for Event1 High		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	13813Ch	
Upper 32 bits of the EU Metrics Event1		
DWord	**Bit**	**Description**
0	31:0	**EUMetrics, Event1 High**
		Default Value: 00000000h
		Access: RO
		Contains Upper 32 bits of EU Metrics, Event1

EU Metrics for Event1 Low

EUMETRICSEVENT1L - EU Metrics for Event1 Low		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	138138h	
Lower 14 bits of the EU Metrics Event1		

DWord	Bit	Description	
0	31:18	**EUMetrics, Event1 Low**	
		Default Value:	0000h
		Access:	RO
		Contains lower 14 bits of EU Metrics, Event1	
	17:0	**Reserved**	
		Default Value:	00000h
		Access:	RO
		Reserved	

EU Metrics for Event2 High

EUMETRICSEVENT2H - EU Metrics for Event2 High	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	138144h

Upper 32 bits of the EU Metrics Event2

DWord	Bit	Description	
0	31:0	**EUMetrics, Event2 High**	
		Default Value:	00000000h
		Access:	RO
		Contains Upper 32 bits of EU Metrics, Event2	

EU Metrics for Event2 Low

EUMETRICSEVENT2L - EU Metrics for Event2 Low			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	138140h		
Lower 14 bits of the EU Metrics Event2			
DWord	**Bit**	**Description**	
0	31:18	**EUMetrics, Event2 Low**	
		Default Value:	0000h
		Access:	RO
		Contains lower 14 bits of EU Metrics, Event2	
	17:0	**Reserved**	
		Default Value:	00000h
		Access:	RO
		Reserved	

EU Metrics for Event3 High

EUMETRICSEVENT3H - EU Metrics for Event3 High	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	13814Ch

Upper 32 bits of the EU Metrics Event3

DWord	Bit	Description	
0	31:0	**EUMetrics, Event3 High**	
		Default Value:	00000000h
		Access:	RO
		Contains Upper 32 bits of EU Metrics, Event3	

EU Metrics for Event3 Low

EUMETRICSEVENT3L - EU Metrics for Event3 Low		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	138148h	
Lower 14 bits of the EU Metrics Event3		

DWord	Bit	Description
0	31:18	**EUMetrics, Event3 Low**
		Default Value: 0000h
		Access: RO
		Contains lower 14 bits of EU Metrics, Event3
	17:0	**Reserved**
		Default Value: 00000h
		Access: RO
		Reserved

EU Metrics for Event4 High

EUMETRICSEVENT4H - EU Metrics for Event4 High		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	138154h	
Upper 32 bits of the EU Metrics Event4		

DWord	Bit	Description
0	31:0	**EUMetrics, Event4 High**
		Default Value: 00000000h
		Access: RO
		Contains Upper 32 bits of EU Metrics, Event4

EU Metrics for Event4 Low

EUMETRICSEVENT4L - EU Metrics for Event4 Low		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	138150h	
Lower 14 bits of the EU Metrics Event4		

DWord	Bit	Description
0	31:18	**EUMetrics, Event4 Low**
		Default Value: 0000h
		Access: RO
		Contains lower 14 bits of EU Metrics, Event4
	17:0	**Reserved**
		Default Value: 00000h
		Access: RO
		Reserved

EU Metrics for Event5 High

<table>
<tr><td colspan="4" align="center">**EUMETRICSEVENT5H - EU Metrics for Event5 High**</td></tr>
<tr><td colspan="4">Register Space: MMIO: 0/2/0</td></tr>
<tr><td colspan="4">Project: CHV, BSW</td></tr>
<tr><td colspan="4">Source: PRM</td></tr>
<tr><td colspan="4">Default Value: 0x00000000</td></tr>
<tr><td colspan="4">Size (in bits):   32</td></tr>
<tr><td colspan="4">Address: 13815Ch</td></tr>
<tr><td colspan="4">Upper 32 bits of the EU Metrics Event5</td></tr>
</table>

DWord	Bit	Description	
0	31:0	**EUMetrics, Event5 High**	
		Default Value:	00000000h
		Access:	RO
		Contains Upper 32 bits of EU Metrics, Event5	

EU Metrics for Event5 Low

EUMETRICSEVENT5L - EU Metrics for Event5 Low		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	138158h	
Lower 14 bits of the EU Metrics Event5		

DWord	Bit	Description
0	31:18	**EUMetrics, Event5 Low**
		Default Value: 0000h
		Access: RO
		Contains lower 14 bits of EU Metrics, Event5
	17:0	**Reserved**
		Default Value: 00000h
		Access: RO
		Reserved

EU Metrics for Event6 High

EUMETRICSEVENT6H - EU Metrics for Event6 High		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	138164h	
Upper 32 bits of the EU Metrics Event6		

DWord	Bit	Description
0	31:0	**EUMetrics, Event6 High**
		Default Value: · 00000000h
		Access: · RO
		Contains Upper 32 bits of EU Metrics, Event6

EU Metrics for Event6 Low

EUMETRICSEVENT6L - EU Metrics for Event6 Low		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	138160h	
Lower 14 bits of the EU Metrics Event6		

DWord	Bit	Description	
0	31:18	**EUMetrics, Event6 Low**	
		Default Value:	0000h
		Access:	RO
		Contains lower 14 bits of EU Metrics, Event6	
	17:0	**Reserved**	
		Default Value:	00000h
		Access:	RO
		Reserved	

EU Metrics for Event7 High

EUMETRICSEVENT7H - EU Metrics for Event7 High	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	13816Ch

Upper 32 bits of the EU Metrics Event7

DWord	Bit	Description	
0	31:0	**EUMetrics, Event7 High**	
		Default Value:	00000000h
		Access:	RO
		Contains Upper 32 bits of EU Metrics, Event7	

EU Metrics for Event7 Low

EUMETRICSEVENT7L - EU Metrics for Event7 Low		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	138168h	

Lower 14 bits of the EU Metrics Event7		
DWord	**Bit**	**Description**
0	31:18	**EUMetrics, Event7 Low**
		Default Value: 0000h
		Access: RO
		Contains lower 14 bits of EU Metrics, Event7
	17:0	**Reserved**
		Default Value: 00000h
		Access: RO
		Reserved

EU Metrics for Event8 High

<table>
<tr><td colspan="4" align="center">**EUMETRICSEVENT8H - EU Metrics for Event8 High**</td></tr>
<tr><td colspan="4">Register Space: MMIO: 0/2/0</td></tr>
<tr><td colspan="4">Project: CHV, BSW</td></tr>
<tr><td colspan="4">Source: PRM</td></tr>
<tr><td colspan="4">Default Value: 0x00000000</td></tr>
<tr><td colspan="4">Size (in bits):   32</td></tr>
<tr><td colspan="4">Address: 138174h</td></tr>
<tr><td colspan="4">Upper 32 bits of the EU Metrics Event8</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td colspan="2">**Description**</td></tr>
<tr><td>0</td><td>31:0</td><td colspan="2">**EUMetrics, Event8 High**</td></tr>
<tr><td></td><td></td><td>Default Value:</td><td>00000000h</td></tr>
<tr><td></td><td></td><td>Access:</td><td>RO</td></tr>
<tr><td></td><td></td><td colspan="2">Contains Upper 32 bits of EU Metrics, Event8</td></tr>
</table>

EU Metrics for Event8 Low

EUMETRICSEVENT8L - EU Metrics for Event8 Low		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	138170h	
Lower 14 bits of the EU Metrics Event8		

DWord	Bit	Description
0	31:18	**EUMetrics, Event8 Low**
		Default Value: 0000h
		Access: RO
		Contains lower 14 bits of EU Metrics, Event8
	17:0	**Reserved**
		Default Value: 00000h
		Access: RO
		Reserved

EU Metrics for Event9 High

<table>
<tr><td colspan="3" align="center">**EUMETRICSEVENT9H - EU Metrics for Event9 High**</td></tr>
<tr><td>Register Space:</td><td colspan="2">MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td colspan="2">CHV, BSW</td></tr>
<tr><td>Source:</td><td colspan="2">PRM</td></tr>
<tr><td>Default Value:</td><td colspan="2">0x00000000</td></tr>
<tr><td>Size (in bits):</td><td colspan="2">32</td></tr>
<tr><td>Address:</td><td colspan="2">13817Ch</td></tr>
<tr><td colspan="3">Upper 32 bits of the EU Metrics Event9</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td>**Description**</td></tr>
<tr><td>0</td><td>31:0</td><td>**EUMetrics, Event9 High**

Default Value:	00000000h
Access:	RO

Contains Upper 32 bits of EU Metrics, Event9</td></tr>
</table>

EU Metrics for Event9 Low

<table>
<tr><td colspan="4" align="center">**EUMETRICSEVENT9L - EU Metrics for Event9 Low**</td></tr>
<tr><td colspan="4">Register Space: MMIO: 0/2/0</td></tr>
<tr><td colspan="4">Project: CHV, BSW</td></tr>
<tr><td colspan="4">Source: PRM</td></tr>
<tr><td colspan="4">Default Value: 0x00000000</td></tr>
<tr><td colspan="4">Size (in bits):   32</td></tr>
<tr><td colspan="4">Address: 138178h</td></tr>
<tr><td colspan="4">Lower 14 bits of the EU Metrics Event9</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td colspan="2">**Description**</td></tr>
<tr><td>0</td><td>31:18</td><td colspan="2">**EUMetrics, Event9 Low**
Default Value: 0000h
Access: RO
Contains lower 14 bits of EU Metrics, Event9</td></tr>
<tr><td></td><td>17:0</td><td colspan="2">**Reserved**
Default Value: 00000h
Access: RO
Reserved</td></tr>
</table>

EU Metrics for Event10 High

<table>
<tr><td colspan="2" align="center">**EUMETRICSEVENT10H - EU Metrics for Event10 High**</td></tr>
<tr><td>Register Space:</td><td>MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td>CHV, BSW</td></tr>
<tr><td>Source:</td><td>PRM</td></tr>
<tr><td>Default Value:</td><td>0x00000000</td></tr>
<tr><td>Size (in bits):</td><td>32</td></tr>
<tr><td>Address:</td><td>138184h</td></tr>
</table>

Upper 32 bits of the EU Metrics Event10

DWord	Bit	Description
0	31:0	**EUMetrics, Event10 High**
		Default Value: 00000000h
		Access: RO
		Contains Upper 32 bits of EU Metrics, Event10

EU Metrics for Event10 Low

EUMETRICSEVENT10L - EU Metrics for Event10 Low		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	138180h	
Lower 14 bits of the EU Metrics Event10		

DWord	Bit	Description	
0	31:18	**EUMetrics, Event10 Low**	
		Default Value:	0000h
		Access:	RO
		Contains lower 14 bits of EU Metrics, Event10	
	17:0	**Reserved**	
		Default Value:	00000h
		Access:	RO
		Reserved	

EU Metrics for Event11 High

<table>
<tr><th colspan="3">EUMETRICSEVENT11H - EU Metrics for Event11 High</th></tr>
<tr><td>Register Space:</td><td colspan="2">MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td colspan="2">CHV, BSW</td></tr>
<tr><td>Source:</td><td colspan="2">PRM</td></tr>
<tr><td>Default Value:</td><td colspan="2">0x00000000</td></tr>
<tr><td>Size (in bits):</td><td colspan="2">32</td></tr>
<tr><td>Address:</td><td colspan="2">13818Ch</td></tr>
<tr><td colspan="3">Upper 32 bits of the EU Metrics Event11</td></tr>
<tr><th>DWord</th><th>Bit</th><th>Description</th></tr>
<tr><td>0</td><td>31:0</td><td>**EUMetrics, Event11 High**

Default Value: 00000000h
Access: RO
Contains Upper 32 bits of EU Metrics, Event11</td></tr>
</table>

EU Metrics for Event11 Low

EUMETRICSEVENT11L - EU Metrics for Event11 Low		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	138188h	
Lower 14 bits of the EU Metrics Event11		

DWord	Bit	Description
0	31:18	**EUMetrics, Event11 Low**
		Default Value: 0000h
		Access: RO
		Contains lower 14 bits of EU Metrics, Event11
	17:0	**Reserved**
		Default Value: 00000h
		Access: RO
		Reserved

EU Metrics for Event12 High

EUMETRICSEVENT12H - EU Metrics for Event12 High		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	138194h	
Upper 32 bits of the EU Metrics Event12		
DWord	**Bit**	**Description**
0	31:0	**EUMetrics, Event12 High**
		Default Value: 00000000h
		Access: RO
		Contains Upper 32 bits of EU Metrics, Event12

EU Metrics for Event12 Low

<table>
<tr>
<td colspan="3" align="center">EUMETRICSEVENT12L - EU Metrics for Event12 Low</td>
</tr>
<tr>
<td colspan="3">
Register Space: MMIO: 0/2/0
Project: CHV, BSW
Source: PRM
Default Value: 0x00000000
Size (in bits):   32
</td>
</tr>
<tr>
<td colspan="3">Address: 138190h</td>
</tr>
<tr>
<td colspan="3">Lower 14 bits of the EU Metrics Event12</td>
</tr>
<tr>
<td>DWord</td>
<td>Bit</td>
<td>Description</td>
</tr>
<tr>
<td>0</td>
<td>31:18</td>
<td>

EUMetrics, Event12 Low

Default Value:	0000h
Access:	RO

Contains lower 14 bits of EU Metrics, Event12
</td>
</tr>
<tr>
<td></td>
<td>17:0</td>
<td>

Reserved

Default Value:	00000h
Access:	RO

Reserved
</td>
</tr>
</table>

Event selection and base counters

LPFCREG2 - Event selection and base counters		

Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0B00Ch

DWord	Bit	Description
0	31:24	**Counter 7 client**

Access:	R/W

lncf_lpfc_cnt7_client[7:0].Client Encoding (hex):
GAFS Rd 00
GAFS Wr 01
HDC0 Data Rd 02
HDC0 Const Rd 03
HDC0 URB Rd 04
HDC0 Data Wr 05
HDC0 URB Wr 06
HDC1 Data Rd 07
HDC1 Const Rd 08
HDC1 URB Rd 09
HDC1 Data Wr 0A
HDC1 URB Wr 0B
TDL0 Rd 0C
TDL1 Rd 0D
Tex0 Rd 0E
Tex1 Rd 0F
Tex2 Rd (reserved) 10
Tex3 Rd (reserved) 11
SBE Rd 12
IC0 Rd 13
IC1 Rd 14
SARB Rd 15
Aggregated Tex 16
SLM0 Rd 17
SLM1 Rd 18
SLM0 Wr 19
SLM1 Wr 1A
SLM0 Atomics 1B
SLM1 Atomics 1C
Reserved 1D
Reserved 1E

LPFCREG2 - Event selection and base counters
Reserved 1F FF Stalls 20 HDC Stalls 21 TDL Stalls 22 Texture Stalls 23 IC Stalls 24 SBE Stalls 25 SLM Stalls 26 Bank0 Total Hits 40 Bank0 Total Cycles 41 Bank0 Total Rds 42 Bank0 Total Wrs 43 Bank0 FF Rds 44 Bank0 FF Wrs 45 Bank0 DC Rds 46 Bank0 DC Wrs 47 Bank0 DC Hits 48 rsvd 49 Bank0 Tex Rds 4A Bank0 Tex Hits 4B Bank0 IC Rds 4C Bank0 IC Hits 4D Reserved 4E Reserved 4F Bank1 Events 50-5F (except 59-reserved) Bank2 Events 60-6F(except 69-reserved) Bank3 Events 70-7F(except 79-reserved) MSC Rd 80 MSC Wr 81 STC Rd 82 STC Wr 83 Hiz Rd 84 Hiz Wr 85 RCZ Rd 86 RCZ Wr 87 RCC Rd 88 RCC Wr 89 LTCD0 Err Corr EE LTCD1 Err Corr EF LTCD2 Err Corr F0 LTCD3 Err Corr F1 LTCD0 Err UnCorr F2 LTCD1 Err UnCorr F3 LTCD2 Err UnCorr F4 LTCD3 Err UnCorr F5

LPFCREG2 - Event selection and base counters

		Counter#7 Client Selection: This field controls which client's request stream is observed in counter#7.
	23:16	**Counter 6 client**
		Access: R/W
		lncf_lpfc_cnt6_client[7:0].Counter#6 Client Selection: This field controls which client's request stream is observed in counter#6.
	15:8	**Counter 5 client**
		Access: R/W
		lncf_lpfc_cnt5_client[7:0].Counter#5 Client Selection: This field controls which client's request stream is observed in counter#5.
	7:0	**Counter 4 client**
		Access: R/W
		lncf_lpfc_cnt4_client[7:0].Counter#4 Client Selection: This field controls which client's request stream is observed in counter#4.

Event Selection and Base Counters1

LPFCREG1 - Event Selection and Base Counters1		

Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32

Address:	0B010h

DWord	Bit	Description
0	31:24	**Counter 3 client**
		Access: .... R/W
		lncf_lpfc_cnt3_client[7:0].Counter#3 Client Selection: This field controls which client's request stream is observed in counter#3.
	23:16	**Counter 2 client**
		Access: .... R/W
		lncf_lpfc_cnt2_client[7:0].Counter#2 Client Selection: This field controls which client's request stream is observed in counter#2.
	15:8	**Counter 1 Client**
		Access: .... R/W
		lncf_lpfc_cnt1_client[7:0].Counter#1 Client Selection: This field controls which client's request stream is observed in counter#1.
	7:0	**Counter0 Client**
		Access: .... R/W
		lncf_lpfc_cnt0_client[7:0].Counter#0 Client Selection: This field controls which client's request stream is observed in counter#0.

Exec-List Context Offset

CXT_EL_OFFSET - Exec-List Context Offset	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00010000
Access:	Read/32 bit Write Only
Size (in bits):	32
Address:	021ACh
Address:	121ACh-121AFh
Name:	Exec-List Context Offset
ShortName:	CXT_EL_OFFSET_VCSUNIT0
Address:	1A1ACh-1A1AFh
Name:	Exec-List Context Offset
ShortName:	CXT_EL_OFFSET_VECSUNIT
Address:	1C1ACh-1C1AFh
Name:	Exec-List Context Offset
ShortName:	CXT_EL_OFFSET_VCSUNIT1
Address:	221ACh-221AFh
Name:	Exec-List Context Offset
ShortName:	CXT_EL_OFFSET_BCSUNIT

This register provides the layout format of LRCA in Exec-List mode of scheduling. Each field represents its location in 4KB offset from LRCA base address. Register gets initialized to default value coming out of reset. This register is for debug mode usage and SW must not program this register.

DWord	Bit	Description	
0	31:20	**Reserved**	
		Format:	MBZ
	19:16	**Ring Context Offset**	
		Default Value:	1h
		Project:	CHV, BSW
	15:4	**Reserved**	
		Project:	CHV, BSW
		Format:	MBZ
	3:0	**PerProcess HW Status Page Offset**	
		Default Value:	0h
		Project:	CHV, BSW

Execlist Status

<table>
<tr><td colspan="4" align="center">**EXECLIST_STATUS - Execlist Status**</td></tr>
<tr><td colspan="4">Register Space: MMIO: 0/2/0</td></tr>
<tr><td colspan="4">Project: CHV, BSW</td></tr>
<tr><td colspan="4">Source: PRM</td></tr>
<tr><td colspan="4">Default Value: 0x00000001, 0x00000000</td></tr>
<tr><td colspan="4">Access: RO</td></tr>
<tr><td colspan="4">Size (in bits):   64</td></tr>
</table>

Address:	02234h-0223Bh
Name:	RCS Execlist Status
ShortName:	EXECLIST_STATUS_RCSUNIT

Address:	12234h-1223Bh
Name:	RCS Execlist Status
ShortName:	EXECLIST_STATUS_VCSUNIT0

Address:	1A234h-1A23Bh
Name:	RCS Execlist Status
ShortName:	EXECLIST_STATUS_VECSUNIT

Address:	1C234h-1C23Bh
Name:	RCS Execlist Status
ShortName:	EXECLIST_STATUS_VCSUNIT1

Address:	22234h-2223Bh
Name:	RCS Execlist Status
ShortName:	EXECLIST_STATUS_BCSUNIT

This register contains the pointers and full indicator for the Execlist Queue and the context ID of the currently running context. DefaultValue = UUUU UUU1h (4:0 default to 00001b, others UNDEFINED).

DWord	Bit	Description
0	63:32	**Current Context ID** Format: U32 Contains the context ID of the currently running context.
	31:30	**Reserved** Project: CHV, BSW Format: MBZ
	29:27	**Reserved** Format: MBZ

EXECLIST_STATUS - Execlist Status

<table>
<tr><td>26:19</td><td colspan="2">Reserved</td></tr>
<tr><td></td><td>Project:</td><td>CHV, BSW</td></tr>
<tr><td></td><td>Format:</td><td>MBZ</td></tr>
<tr><td>18</td><td colspan="2">Execlist 0 Active</td></tr>
<tr><td></td><td>Format:</td><td>U1</td></tr>
<tr><td></td><td colspan="2">RL0 valid and actively being processed by HW. This bit is for additional debug purpose.</td></tr>
<tr><td>17</td><td colspan="2">Execlist 1 Active</td></tr>
<tr><td></td><td>Project:</td><td>CHV, BSW</td></tr>
<tr><td></td><td>Format:</td><td>U1</td></tr>
<tr><td></td><td colspan="2">RL1 valid and actively being processed by HW. This bit is for additional debug purpose.</td></tr>
<tr><td>16</td><td colspan="2">Arbitration Enable</td></tr>
<tr><td></td><td>Project:</td><td>CHV, BSW</td></tr>
<tr><td></td><td>Format:</td><td>U1</td></tr>
<tr><td></td><td colspan="2">This field reflects the Arbitration Flag set by the MI_ARB_ON_OFF command in Command Streamer.</td></tr>
<tr><td>15:14</td><td colspan="2">Current Active Element Status</td></tr>
<tr><td></td><td>Project:</td><td>CHV, BSW</td></tr>
<tr><td></td><td>Format:</td><td>U2</td></tr>
<tr><td></td><td colspan="2">Points at the element being executed in current Execlist (if there is one).</td></tr>
</table>

Value	Name
00b	No Active Element being executed
01b	Element0 of current execlist being executed
10b	Element1 of current execlist being executed
11b	Reserved

<table>
<tr><td>13:5</td><td colspan="2">Last Context Switch Reason</td></tr>
<tr><td></td><td>Project:</td><td>CHV, BSW</td></tr>
<tr><td></td><td>Access:</td><td>R/W</td></tr>
<tr><td></td><td>Format:</td><td>U9</td></tr>
<tr><td></td><td colspan="2">This field contains the switch reason for the last context to switch away, as captured in the Context Status Dword, bits 8:0.</td></tr>
</table>

Programming Notes
This field should not written by SW.

EXECLIST_STATUS - Execlist Status

	4	**Execlist 0 Valid**	
		Project:	CHV, BSW
		Format:	Flag

This bit is set when the first DW for this Execlist port 0 is written through the submission port, and will not be cleared till the CSB is updated and the command stream is switching to the next execution list. If no execution list is pending, the transition of this bit from one to zero guarentees there will be no preemption on the next submission.

Value	Name
0	Invalid **[Default]**
1	Valid

	3	**Execlist 1 Valid**	
		Project:	CHV, BSW
		Format:	Flag

This bit is set when the first DW for this Execlist port 1 is written through the submission port, and will not be cleared till the CSB is updated and the command stream is switching to the next execution list. If no execution list is pending, the transition of this bit from one to zero guarentees there will be no preemption on the next submission.

Value	Name
0	Invalid **[Default]**
1	Valid

	2	**Execlist Queue Full**	
		Project:	CHV, BSW

When [Execlist Write Pointer] and [Current Execlist Pointer] are equal, this bit differentiates between Queue Full and Queue Empty.

Value	Name	Description
0	Execlist Queue Empty **[Default]**	
1	Execlist Queue Full	There is a current and a pending execlist.

	1	**Execlist Write Pointer**	
		Project:	CHV, BSW
		Format:	ExeclistContentsIndex

Determines which Execlist will be the next submitted to. When a new execlist is submitted, this pointer increments to point to the next execlist slot.

	0	**Current Execlist Pointer**	
		Default Value:	1h
		Project:	CHV, BSW
		Format:	ExeclistContentsIndex

Points at the currently executing Execlist (if there is one). This pointer advances when the first context of new execlist is restored.

Execlist Submit Port Register

EXECLIST_SUBMITPORT - Execlist Submit Port Register	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Access:	WO
Size (in bits):	32
Address:	02230h-02233h
Name:	Execlist Submit Port Register
ShortName:	EXECLIST_SUBMITPORT_RCSUNIT
Address:	12230h-12233h
Name:	Execlist Submit Port Register
ShortName:	EXECLIST_SUBMITPORT_VCSUNIT0
Address:	1A230h-1A233h
Name:	Execlist Submit Port Register
ShortName:	EXECLIST_SUBMITPORT_VECSUNIT
Address:	1C230h-1C233h
Name:	Execlist Submit Port Register
ShortName:	EXECLIST_SUBMITPORT_VCSUNIT1
Address:	22230h-22233h
Name:	Execlist Submit Port Register
ShortName:	EXECLIST_SUBMITPORT_BCSUNIT

SW should submit a new pending execlist to this register. The DWs of the context descriptors must be written in a specific order: Element 1 must be written first and then Element 0. For each Element, DW1 must be written first followed by DW0. Context descriptors for both the elements must be written even if only one context are being submitted. The valid bits of the unused context descriptors should be set to 0.

Order of DW Submission to the Execlist Port
Element 1, High Dword
Element 1, Low Dword
Element 0, High Dword
Element 0, Low Dword

If a execlist of only one element is being submitted, it must be submitted in Element 0. It is UNDEFINED to submit a execlist with the valid bit of Element 0 clear (an "empty" execlist). It is possible that one or all of the contexts submitted in a execlists are "empty"; that is, have head and tail pointers equal to each other indicating no commands to be run. All of the valid bits in the Execlist Element Status Registers for the "about to be submitted" execlist will be cleared when the first DW (DW1 of Element 1) is written to the submit port.

EXECLIST_SUBMITPORT - Execlist Submit Port Register

Submission of the Element 0 Context Descriptor low Dword with the valid bit set is interpreted as a request to switch (as soon as possible) to the new execlist, i.e., a pre-emption request.

If a submitted Execlist's Element 0 Context Descriptor LRCA matches the LRCA of the currently executing context, then the newly submitted execlist will become the currently executing execlist without any context switch and without any impact to the executing context except that it will re-sample the tail pointer from the context image. This is done in case more commands have been inserted into its ring buffer between the first execlist submission and the 2nd.

Programming Notes	Source
SW must ensure the contexts submitted to the both the context descriptors in the execlist are different, i.e SW must not submit the same context descriptor to both the elements of the execlist.	
SW must follow below programming sequence for ELSP submission in host mode of scheduling and not required for GUC based scheduling. SW must set Force Wakeup bit to prevent GT from entering C6 while ELSP writes are in progress. Ex: Set Force Wakeup Program ELSP writes Reset Force Wakeup	

Render CS Only: Command Streamer triggers IDLE sequence flows for RDOP_CG on un-successful Semaphore Waits and Wait for Display Events when "Inhibit Synchronous Context Switch" is set in CTXT_SR_CTL register. As part of IDLE flows CS flushes the Write Caches (Z, Color, HDC). While IDLE flush in progress context switch can happen due to pending execlist submitted and when this condition occurs CS might not issue context switch flush resulting in RO caches not invalidated (State, Texture, Instruction, Constant).
 	
To WA above issue, SW must always program a valid BB_PER_CTX_PTR for every context submitted with a PIPE_CONTROL command to invalidate all RO caches.
 	
PIPE_CONTROL with below bits set in it:
 	
    Instruction Cache Invalidate Enable
    Texture Cache Invalidate Enable
    Constant Cache Invalidate Enable
    State Cache Invalidate Enable
	RenderCS

[All Command Streamers]: When SW intends to use semaphore signaling between Command streamers, SW must avoid lite restores in HW by programming Force Restore bit to '1' in context descriptor during context submission, this is required to avoid known HW issue.	

Workaround	Source
Workaround: SW must always ensure there are valid commands to be executed by HW on a context submission, i.e ring buffer head pointer must not be equal to the ring buffer head pointer on context submission to HW for execution.	RenderCS

EXECLIST_SUBMITPORT - Execlist Submit Port Register

Additional Note: This WA need not be applied when the arbitration is not disabled prior to executing "Batch Buffer Per Context Pointer" as part of context restore. Arbitration can be disabled prior to executing "Batch Buffer Per Context Pointer" by programming MI_ARB_ON_OFF (arbitration disable) in indirect context pointer.	
Workaround: SW must always ensure a preempted context submitted to HW doesn't undergo lite restore due to the same context getting submitted on the next Execlist submission. This can be achieved by setting "Force Restore Bit" in the context descriptor of the context getting submitted and if the same context is known to be submitted to HW for execution on the earlier Execlist submission Or SW on submitting a **preempted** context must wait for the context to switch out before submitting the same context to the Execlist Submit Port. **Note:** This WA need not be applied when "Force Sync Command Ordering" bit of INSTPM register is not disabled (programmed to value '0') during execution of "Batch Buffer Per Context Pointer" during context restore. "Force Sync Command Ordering" can be disabled prior to or during execution of "Batch Buffer Per Context Pointer" by programming INSTPM register using MI_LOAD_REGISTER_IMM command in Indirect Context Pointer or in "Batch Buffer Per Context Pointer". Disabling of "Force Sync Command Ordering" during "Batch Buffer Per Context Pointer" execution was required to address Resource Streamer related preemption issue on HSD 1912487, this WA is not applied when Resource Streamer (RS) is not enabled or when a Resource Streamer enabled context is not preemptable.	

DWord	Bit	Description
0	31:0	**Context Descriptor DW**

Format:	Context Descriptor

See "Context Descriptor Format" for format. The element that this DW is submitted as and whether it is the high DW or the low DW is determined by order. This register must be written to 4 times in order to submit a execlist.

Execute Condition Code Register

EXCC - Execute Condition Code Register	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W, RO
Size (in bits):	32
Trusted Type:	1
Address:	02028h
Address:	12028h-1202Bh
Name:	Execute Condition Code Register
ShortName:	EXCC_VCSUNIT0
Address:	1A028h-1A02Bh
Name:	Execute Condition Code Register
ShortName:	EXCC_VECSUNIT
Address:	1C028h-1C02Bh
Name:	Execute Condition Code Register
ShortName:	EXCC_VCSUNIT1
Address:	22028h-2202Bh
Name:	Execute Condition Code Register
ShortName:	EXCC_BCSUNIT

This register contains user defined and hardware generated conditions that are used by MI_WAIT_FOR_EVENT commands. An MI_WAIT_FOR_EVENT instruction excludes the executing ring from arbitration if the selected event evaluates to a 1, while instruction is discarded if the condition evaluates to a 0. Once excluded a ring is enabled into arbitration when the selected condition evaluates to a 0.
This register also contains control for the invalidation of indirect state pointers on context restore.

DWord	Bit	Description
0	31:16	**Mask Bits**
		Format: Mask[15:0]
		These bits serves as a write enable for bits 15:0. If this register is written with any of these bits clear the corresponding bit in the field 15:0 will not be modified. Reading these bits always returns 0s.
	15	**Reserved**
		Project: CHV, BSW
		Format: MBZ

EXCC - Execute Condition Code Register

	14	**Context Wait for V-blank on Pipe-C**
		Project: CHV, BSW
		This field when set indicates the corresponding context has executed MI_WAIT_FOR_EVENT with "Display Pipe C Vertical Blank Wait Enable" set. This is an internal HW flag and should not be accessed by SW.
	13	**Context Wait for V-blank on Pipe-B**
		Project: CHV, BSW
		This field when set indicates the corresponding context has executed MI_WAIT_FOR_EVENT with "Display Pipe B Vertical Blank Wait Enable" set. This is an internal HW flag and should not be accessed by SW.
	12	**Context Wait for V-blank on Pipe-A**
		Project: CHV, BSW
		This field when set indicates the corresponding context has executed MI_WAIT_FOR_EVENT with "Display Pipe A Vertical Blank Wait Enable" set. This is an internal HW flag and should not be accessed by SW.
	11	**Pending Indirect State Dirty Bit**
		Project: CHV, BSW
		Access: RO
		This field keeps track of whether or not an indirect state pointer command has been parsed in the current context. Clears either on a context save or explicitly through a flush command. This bit is Read Only.
	10:7	**Pending Indirect State Counter**
		Project: CHV, BSW
		This field keeps track of the maximum number of indirect state pointers pending in the system. When the register is saved/restored, it saves either a value of 1 or 0. This field is Read-Only.
	6:5	**Reserved**
		Format: MBZ
	4:0	**User Defined Condition Codes**
		The software may signal a Stream Semaphore by setting the Mask bit and Signal Bit together to match the bit field specified in a WAIT_FOR_EVENT (Semaphore).

FAULT_TLB_RD_DATA0 Register

FAULT_TLB_RD_DATA0 - FAULT_TLB_RD_DATA0 Register		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04B10h	

DWord	Bit	Description
0	31:0	**FAULT_TLB_READ_DATA0 Register**

		Default Value:	00000000h
		Access:	RO

Fault cycle Virtual address [43:12]

FAULT_TLB_RD_DATA1 Register

<table>
<tr><td colspan="3" align="center">**FAULT_TLB_RD_DATA1 - FAULT_TLB_RD_DATA1 Register**</td></tr>
<tr><td>Register Space:</td><td colspan="2">MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td colspan="2">CHV, BSW</td></tr>
<tr><td>Source:</td><td colspan="2">PRM</td></tr>
<tr><td>Default Value:</td><td colspan="2">0x00000000</td></tr>
<tr><td>Size (in bits):</td><td colspan="2">32</td></tr>
<tr><td>Address:</td><td colspan="2">04B14h</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td>**Description**</td></tr>
<tr><td>0</td><td>31:0</td><td>

FAULT_TLB_READ_DATA1 Register

Default Value:	00000000h
Access:	RO

Bit[31:5] Reserved
Bit[4] Cycle GTT SEL (1-GGTT Cycle, 0-PPGTT Cycle)
Bit[3:0] Fault cycle Virtual address [47:44]
</td></tr>
</table>

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Fault Switch Out

FAULT_SO - Fault Switch Out		
Register Space:	MMIO: 0/2/0	
Project:	CHV	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04590h	
DWord	**Bit**	**Description**
0	31:0	**Fault Switch Out**
		Default Value: 00000000h
		Access: R/W

FBC_RT_BASE_ADDR_REGISTER

FBC_RT_BASE_ADDR_REGISTER - FBC_RT_BASE_ADDR_REGISTER	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	07020h
Valid Projects:	CHV, BSW

This Register is saved and restored as part of Context.

DWord	Bit	Description
0	31:12	**FBC RT Base Address**
		Access: R/W
		Format: PPGraphicsAddress[31:12]
		4KB aligned Base Address as mapped in the PPGTT or in the GGTT for the render target. This base address must be the one that is either front buffer or the back-buffer (a flip target). It must be programmed before any draw call binding that render target base address.
	11:2	**Reserved**
		Access: R/W
		Format: PBC
	1	**FBC Front Buffer Target**
		Project: CHV, BSW
		Access: R/W
		Format: Enable

Value	Name	Description
0h	[Default]	FBC is targeting the Back Buffer for compression. This buffer can be cached in the MLC/LLC, so a GFDT flush is required before FBC can begin compression.
1h		FBC is targeting the Font Buffer for compression. This buffer cannot be cached in the MLC/LLC. FBC compression can begin after any RC flush.

FBC_RT_BASE_ADDR_REGISTER - FBC_RT_BASE_ADDR_REGISTER

	0	**PPGTT Render Target Base Address Valid for FBC**	
		Project:	CHV, BSW
		Access:	R/W
		Format:	Enable

Value	Name	Description
0h	**[Default]**	Base address in this register [31:12] is not valid and therefore FBC will not get any modifications from rendering.
1h		Base address in this register [31:12] is valid and HW needs to compare the current render target base address with this base address to provide modifications to FBC.

FBC_RT_BASE_ADDR_REGISTER_UPPER

<table>
<tr>
<td colspan="3" align="center">**FBC_RT_BASE_ADDR_REGISTER_UPPER -
FBC_RT_BASE_ADDR_REGISTER_UPPER**</td>
</tr>
<tr>
<td>Register Space:</td>
<td colspan="2">MMIO: 0/2/0</td>
</tr>
<tr>
<td>Project:</td>
<td colspan="2">CHV, BSW</td>
</tr>
<tr>
<td>Source:</td>
<td colspan="2">RenderCS</td>
</tr>
<tr>
<td>Default Value:</td>
<td colspan="2">0x00000000</td>
</tr>
<tr>
<td>Access:</td>
<td colspan="2">R/W</td>
</tr>
<tr>
<td>Size (in bits):</td>
<td colspan="2">32</td>
</tr>
<tr>
<td>Address:</td>
<td colspan="2">07024h</td>
</tr>
<tr>
<td colspan="3">This Register is saved and restored as part of Context.</td>
</tr>
</table>

DWord	Bit	Description
0	31:16	**Reserved**

	Access:		R/W
	Format:		PBC

	15:0	**FBC RT Base Address High**

	Access:	R/W
	Format:	BaseAddress[47:32]

Must be set to modify corresponding data bit. Reads to this field returns zero. Upper 4KB aligned Base Address as mapped in the PPGTT or in the GGTT for the render target. This base address must be the one that is either front buffer or the back-buffer (a flip target). It can be only programmed once per context.

Programming Notes
It must be programmed before any draw call binding that render target base address.

FD

<table>
<tr><td colspan="3" align="center">**FD - FD**</td></tr>
<tr><td colspan="3">Register Space: PCI: 0/2/0</td></tr>
<tr><td colspan="3">Project: CHV, BSW</td></tr>
<tr><td colspan="3">Source: PRM</td></tr>
<tr><td colspan="3">Default Value: 0x00000000</td></tr>
<tr><td colspan="3">Size (in bits):   32</td></tr>
<tr><td colspan="3">Address: 000C4h</td></tr>
<tr><td colspan="3">Functional Disable. This register is used by SBIOS, not by driver.</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td>**Description**</td></tr>
<tr><td>0</td><td>31:1</td><td>

RESERVED

Default Value:	00000000h
Access:	RO

Reserved
</td></tr>
<tr><td></td><td>0</td><td>

FUNCTION_DISABLE

Default Value:	0b
Access:	R/W

Description
FD: 0 : Default - normal operation. 1 : When set, the function is disabled (configuration space is disabled). All new requests on the IOSF Primary bus, including any new configuration cycle requests are not claimed on IOSF Primary. This bit as no effect register accessibility via IOSF SB. Once programmed to '1', the only way to re-enable device 2 is via an IOSF SB write of '0' to this register.
CHV, BSW: Wire is sent to PSF for decode purposes gvd_psf_dev2disable_nczfwoh.

</td></tr>
</table>

FF Performance

FF_PERF - FF Performance		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	06B1Ch	
Valid Projects:	CHV, BSW	

DWord	Bit	Description
0	31:16	**Mask**
		Project: All
		Access: WO
		Format: Mask[15:0]
		Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)
	15:11	**Reserved**
		Project: All
		Access: r/w
		Format: PBC
	10:8	**Throttle counter value**
		Project: CHV, BSW
		Access: r/w
		Format: Disable
		Counter value defining how many clocks the interface needs to be slowed down.

Value	Name	Description
0h	**[Default]**	Masked by default.

DWord	Bit	Description
	7:3	**Reserved**
		Project: CHV, BSW
		Access: r/w
		Format: PBC

			FF_PERF - FF Performance

FF_PERF - FF Performance

	2	**Enable throttling for SF-WM interface**

Access:	r/w
Format:	Disable

Value	Name	Description
0h	Disable	No throttling
1h	Enable	Enable throttling in all SF-WM interfaces

	1	**Enable throttling for SF-SBE interface**

Access:	r/w
Format:	Disable

Value	Name	Description
0h	Disable	No throttling
1h	Enable	Enable throttling in all SF-SBE interfaces

	0	**Enable throttling for CL-SF interface**

Access:	r/w
Format:	Disable

Value	Name	Description
0h	Disable	No throttling
1h	Enable	Enable throttling in all CL-SF interfaces

First Buffer Size and Start

<table>
<tr><td colspan="3" align="center">**FBSS - First Buffer Size and Start**</td></tr>
<tr><td>Register Space:</td><td colspan="2">MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td colspan="2">CHV, BSW</td></tr>
<tr><td>Source:</td><td colspan="2">PRM</td></tr>
<tr><td>Default Value:</td><td colspan="2">0x00000000</td></tr>
<tr><td>Size (in bits):</td><td colspan="2">32</td></tr>
<tr><td>Address:</td><td colspan="2">0B420h</td></tr>
<tr><td colspan="3">LPFCREG02 - First Buffer Size and Start</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td>**Description**</td></tr>
<tr><td>0</td><td>31:16</td><td>**First Virtual Buffer Base**

Access: R/W

First Virtual Buffer Base: Programmed by driver to allocate a memory space for performance data storage. The buffer size should be aligned to the size of the memory allocated so it naturally aligns to the base (i.e. for 128KB bit[16]=0, 256KB bit[17:16]=0, 512KB bit[18:16]=0).
Signal - lpconf_lpfc_virtual_base0 [31:16].</td></tr>
<tr><td></td><td>15:12</td><td>**First Buffer Size**

Access: R/W

First Buffer Size: Determines the allowed buffer size for performance data storage.
0000b: 64KB.
0001b: 128KB.
0010b: 256KB.
0011b: 512KB.
...
1111b: 2GB.
Signal - lpconf_lpfc_buffer_size0 [3:0].</td></tr>
<tr><td></td><td>11:3</td><td>**Reserved**

Project: CHV, BSW
Access: RO

Reserved.</td></tr>
</table>

		FBSS - First Buffer Size and Start	
	2	**Frame count and Draw call enable**	
		Access:	R/W
		Enables the replacement of a specific L3 performance counter value in the reported data with a 16-bit tag created from the concatenation of the "Frame Count" and "Draw Call Number" programmable bitfields in the "Frame Count and Draw Call Number" register. The exact counter replaced is dependent on the programmed value of the "Counter Enabling Selection" bitfield. The replaced counter is always the last one, except in the case only a single performance counter is enabled for reporting (in which no replacement occurs):	

CNTRENSEL Value	Replaced Event Counter
00	No Replacement
01	Counter 1
10	Counter 3
11	Counter 7

	1	**CTX Save Chicken**	
		Access:	R/W
		Disable the context save and FLush Done sequencing fix athika. 0: (default) context save and FLush Done is sequenced. 1: set this bit if the context save and FLush Done sequencing needs to be disabled. This bit was initially used for LPFC dual buffer mode. Using this bit for ECO purpose.	
	0	**Master Counter Enable**	
		Access:	R/W
		Master Counter Enable: This is the global enable for performance tracking. Once set, it kicks off all performance tracking mechanism. Signal - lpconf_lpfc_master_cnt_en. This bit is used by all slices.	

Flexible EU Event Control 0

EU_PERF_CNT_CTL0 - Flexible EU Event Control 0		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	0E458h	
This register configures flexible EU event 0/1. Please refer to the description of the flexible EU events for more details on supported events. Please note that this register is render context saved/restored.		
DWord	**Bit**	**Description**
0	31:24	**Reserved**
			Project:	All	
			Format:	MBZ	
	23:20	**Fine Event Filter Select EU event 1**
			Project:	CHV, BSW	
			Format:	U4	
		This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 1. Note that the fine event filter is logically applied after the coarse event filter.
	19:16	**Coarse Event Filter Select EU event 1**
			Project:	CHV, BSW	
			Format:	U4	
		This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 1. Note that the coarse event filter is logically applied before the fine event filter.
	15:12	**Increment Event for EU event 1**
			Project:	CHV, BSW	
			Format:	U4	
		This field controls which increment event provides the basis for flexible EU event 1.
	11:8	**Fine Event Filter Select EU event 0**
			Project:	CHV, BSW	
			Format:	U4	
		This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 0. Note that the fine event filter is logically applied after the coarse event filter.
	7:4	**Coarse Event Filter Select EU event 0**

EU_PERF_CNT_CTL0 - Flexible EU Event Control 0

		Project:	CHV, BSW
		Format:	U4
		This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 0. Note that the coarse event filter is logically applied before the fine event filter.	
	3:0	**Increment Event for EU event 0**	
		Project:	CHV, BSW
		Format:	U4
		This field controls which increment event provides the basis for flexible EU event 0.	

Flexible EU Event Control 1

	EU_PERF_CNT_CTL1 - Flexible EU Event Control 1

Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	0E558h

This register configures flexible EU event 2/3. Please refer to the description of the flexible EU events for more details on supported events. Please note that this register is render context saved/restored.

DWord	Bit	Description
0	31:24	**Reserved**
		Project: All
		Format: MBZ
	23:20	**Fine Event Filter Select EU event 3**
		Project: CHV, BSW
		Format: U4
		This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 3. Note that the fine event filter is logically applied after the coarse event filter.
	19:16	**Coarse Event Filter Select EU event 3**
		Project: CHV, BSW
		Format: U4
		This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 3. Note that the coarse event filter is logically applied before the fine event filter.
	15:12	**Increment Event for EU event 3**
		Project: CHV, BSW
		Format: U4
		This field controls which increment event provides the basis for flexible EU event 3.
	11:8	**Fine Event Filter Select EU event 2**
		Project: CHV, BSW
		Format: U4
		This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 2. Note that the fine event filter is logically applied after the coarse event filter.

EU_PERF_CNT_CTL1 - Flexible EU Event Control 1

	7:4	**Coarse Event Filter Select EU event 2**	
		Project:	CHV, BSW
		Format:	U4
		This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 2. Note that the coarse event filter is logically applied before the fine event filter.	
	3:0	**Increment Event for EU event 2**	
		Project:	CHV, BSW
		Format:	U4
		This field controls which increment event provides the basis for flexible EU event 2.	

Flexible EU Event Control 2

EU_PERF_CNT_CTL2 - Flexible EU Event Control 2		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	0E658h	
This register configures flexible EU event 4/5. Please refer to the description of the flexible EU events for more details on supported events. Please note that this register is render context saved/restored.		
DWord	**Bit**	**Description**
0	31:24	**Reserved**
			Project:	All	
			Format:	MBZ	
	23:20	**Fine Event Filter Select EU event 5**
			Project:	CHV, BSW	
			Format:	U4	
		This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 5. Note that the fine event filter is logically applied after the coarse event filter.
	19:16	**Coarse Event Filter Select EU event 5**
			Project:	CHV, BSW	
			Format:	U4	
		This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 5. Note that the coarse event filter is logically applied before the fine event filter.
	15:12	**Increment Event for EU event 5**
			Project:	CHV, BSW	
			Format:	U4	
		This field controls which increment event provides the basis for flexible EU event 5.
	11:8	**Fine Event Filter Select EU event 4**
			Project:	CHV, BSW	
			Format:	U4	
		This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 4. Note that the fine event filter is logically applied after the coarse event filter.

EU_PERF_CNT_CTL2 - Flexible EU Event Control 2

	7:4	**Coarse Event Filter Select EU event 4**	
		Project:	CHV, BSW
		Format:	U4

This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 4. Note that the coarse event filter is logically applied before the fine event filter.

	3:0	**Increment Event for EU event 4**	
		Project:	CHV, BSW
		Format:	U4

This field controls which increment event provides the basis for flexible EU event 4.

Flexible EU Event Control 3

EU_PERF_CNT_CTL3 - Flexible EU Event Control 3	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	0E758h

This register configures flexible EU event 6/7. Please refer to the description of the flexible EU events for more details on supported events. Please note that this register is render context saved/restored.

DWord	Bit	Description
0	31:24	**Reserved** Project: All Format: MBZ
	23:20	**Fine Event Filter Select EU event 7** Project: CHV, BSW Format: U4 This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 7. Note that the fine event filter is logically applied after the coarse event filter.
	19:16	**Coarse Event Filter Select EU event 7** Project: CHV, BSW Format: U4 This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 7. Note that the coarse event filter is logically applied before the fine event filter.
	15:12	**Increment Event for EU event 7** Project: CHV, BSW Format: U4 This field controls which increment event provides the basis for flexible EU event 7.
	11:8	**Fine Event Filter Select EU event 6** Project: CHV, BSW Format: U4 This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 6. Note that the fine event filter is logically applied after the coarse event filter.

EU_PERF_CNT_CTL3 - Flexible EU Event Control 3

	7:4	**Coarse Event Filter Select EU event 6**	
		Project:	CHV, BSW
		Format:	U4
		This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 6. Note that the coarse event filter is logically applied before the fine event filter.	
	3:0	**Increment Event for EU event 6**	
		Project:	CHV, BSW
		Format:	U4
		This field controls which increment event provides the basis for flexible EU event 6.	

Flexible EU Event Control 4

EU_PERF_CNT_CTL4 - Flexible EU Event Control 4		

Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	

Address:	0E45Ch

This register configures flexible EU event 8/9. Please refer to the description of the flexible EU events for more details on supported events. Please note that this register is render context saved/restored.

DWord	Bit	Description
0	31:24	**Reserved**
		Project: / All
		Format: / MBZ
	23:20	**Fine Event Filter Select EU event 9**
		Project: / CHV, BSW
		Format: / U4
		This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 9. Note that the fine event filter is logically applied after the coarse event filter.
	19:16	**Coarse Event Filter Select EU event 9**
		Project: / CHV, BSW
		Format: / U4
		This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 9. Note that the coarse event filter is logically applied before the fine event filter.
	15:12	**Increment Event for EU event 9**
		Project: / CHV, BSW
		Format: / U4
		This field controls which increment event provides the basis for flexible EU event 9.
	11:8	**Fine Event Filter Select EU event 8**
		Project: / CHV, BSW
		Format: / U4
		This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 8. Note that the fine event filter is logically applied after the coarse event filter.
	7:4	**Coarse Event Filter Select EU event 8**

EU_PERF_CNT_CTL4 - Flexible EU Event Control 4

		Project:	CHV, BSW
		Format:	U4
		This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 8. Note that the coarse event filter is logically applied before the fine event filter.	
	3:0	**Increment Event for EU event 8**	
		Project:	CHV, BSW
		Format:	U4
		This field controls which increment event provides the basis for flexible EU event 8.	

Flexible EU Event Control 5

EU_PERF_CNT_CTL5 - Flexible EU Event Control 5	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	0E55Ch

This register configures flexible EU event 10/11. Please refer to the description of the flexible EU events for more details on supported events. Please note that this register is render context saved/restored.

DWord	Bit	Description
0	31:24	**Reserved**
		Project: All
		Format: MBZ
	23:20	**Fine Event Filter Select EU event 11**
		Project: CHV, BSW
		Format: U4
		This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 11. Note that the fine event filter is logically applied after the coarse event filter.
	19:16	**Coarse Event Filter Select EU event 11**
		Project: CHV, BSW
		Format: U4
		This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 11. Note that the coarse event filter is logically applied before the fine event filter.
	15:12	**Increment Event for EU event 11**
		Project: CHV, BSW
		Format: U4
		This field controls which increment event provides the basis for flexible EU event 11.
	11:8	**Fine Event Filter Select EU event 10**
		Project: CHV, BSW
		Format: U4
		This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 10. Note that the fine event filter is logically applied after the coarse event filter.

EU_PERF_CNT_CTL5 - Flexible EU Event Control 5

	7:4	**Coarse Event Filter Select EU event 10**	
		Project:	CHV, BSW
		Format:	U4
		This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 10. Note that the coarse event filter is logically applied before the fine event filter.	
	3:0	**Increment Event for EU event 10**	
		Project:	CHV, BSW
		Format:	U4
		This field controls which increment event provides the basis for flexible EU event 10.	

Flexible EU Event Control 6

EU_PERF_CNT_CTL6 - Flexible EU Event Control 6	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	0E65Ch

This register configures flexible EU event 12/13. Please refer to the description of the flexible EU events for more details on supported events. Please note that this register is render context saved/restored.

DWord	Bit	Description	
0	31:24	**Reserved**	
		Project:	All
		Format:	MBZ
	23:20	**Fine Event Filter Select EU event 13**	
		Project:	CHV, BSW
		Format:	U4
		This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 13. Note that the fine event filter is logically applied after the coarse event filter.	
	19:16	**Coarse Event Filter Select EU event 13**	
		Project:	CHV, BSW
		Format:	U4
		This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 13. Note that the coarse event filter is logically applied before the fine event filter.	
	15:12	**Increment Event for EU event 13**	
		Project:	CHV, BSW
		Format:	U4
		This field controls which increment event provides the basis for flexible EU event 13.	
	11:8	**Fine Event Filter Select EU event 12**	
		Project:	CHV, BSW
		Format:	U4
		This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 12. Note that the fine event filter is logically applied after the coarse event filter.	

		EU_PERF_CNT_CTL6 - Flexible EU Event Control 6	
	7:4	**Coarse Event Filter Select EU event 12**	
		Project:	CHV, BSW
		Format:	U4
		This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 12. Note that the coarse event filter is logically applied before the fine event filter.	
	3:0	**Increment Event for EU event 12**	
		Project:	CHV, BSW
		Format:	U4
		This field controls which increment event provides the basis for flexible EU event 12.	

FORCE_TO_NONPRIV

FORCE_TO_NONPRIV - FORCE_TO_NONPRIV	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00002094
Access:	R/W
Size (in bits):	32
Address:	024D0h-024D3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_0_RCSUNIT
Address:	024D4h-024D7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_1_RCSUNIT
Address:	024D8h-024DBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_2_RCSUNIT
Address:	024DCh-024DFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_3_RCSUNIT
Address:	024E0h-024E3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_4_RCSUNIT
Address:	024E4h-024E7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_5_RCSUNIT
Address:	024E8h-024EBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_6_RCSUNIT
Address:	024ECh-024EFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_7_RCSUNIT
Address:	024F0h-024F3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_8_RCSUNIT

FORCE_TO_NONPRIV - FORCE_TO_NONPRIV

Address:	024F4h-024F7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_9_RCSUNIT

Address:	024F8h-024FBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_10_RCSUNIT

Address:	024FCh-024FFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_11_RCSUNIT

Address:	124D0h-124D3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_0_VCSUNIT0

Address:	124D4h-124D7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_1_VCSUNIT0

Address:	124D8h-124DBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_2_VCSUNIT0

Address:	124DCh-124DFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_3_VCSUNIT0

Address:	124E0h-124E3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_4_VCSUNIT0

Address:	124E4h-124E7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_5_VCSUNIT0

Address:	124E8h-124EBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_6_VCSUNIT0

Address:	124ECh-124EFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_7_VCSUNIT0

Address:	124F0h-124F3h
Name:	FORCE_TO_NONPRIV

FORCE_TO_NONPRIV - FORCE_TO_NONPRIV	
ShortName:	FORCE_TO_NONPRIV_8_VCSUNIT0
Address:	124F4h-124F7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_9_VCSUNIT0
Address:	124F8h-124FBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_10_VCSUNIT0
Address:	124FCh-124FFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_11_VCSUNIT0
Address:	1A4D0h-1A4D3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_0_VECSUNIT
Address:	1A4D4h-1A4D7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_1_VECSUNIT
Address:	1A4D8h-1A4DBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_2_VECSUNIT
Address:	1A4DCh-1A4DFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_3_VECSUNIT
Address:	1A4E0h-1A4E3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_4_VECSUNIT
Address:	1A4E4h-1A4E7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_5_VECSUNIT
Address:	1A4E8h-1A4EBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_6_VECSUNIT
Address:	1A4ECh-1A4EFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_7_VECSUNIT
Address:	1A4F0h-1A4F3h

FORCE_TO_NONPRIV - FORCE_TO_NONPRIV

Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_8_VECSUNIT

Address:	1A4F4h-1A4F7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_9_VECSUNIT

Address:	1A4F8h-1A4FBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_10_VECSUNIT

Address:	1A4FCh-1A4FFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_11_VECSUNIT

Address:	1C4D0h-1C4D3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_0_VCSUNIT1

Address:	1C4D4h-1C4D7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_1_VCSUNIT1

Address:	1C4D8h-1C4DBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_2_VCSUNIT1

Address:	1C4DCh-1C4DFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_3_VCSUNIT1

Address:	1C4E0h-1C4E3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_4_VCSUNIT1

Address:	1C4E4h-1C4E7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_5_VCSUNIT1

Address:	1C4E8h-1C4EBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_6_VCSUNIT1

Address:	1C4ECh-1C4EFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_7_VCSUNIT1

FORCE_TO_NONPRIV - FORCE_TO_NONPRIV

Address:	1C4F0h-1C4F3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_8_VCSUNIT1

Address:	1C4F4h-1C4F7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_9_VCSUNIT1

Address:	1C4F8h-1C4FBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_10_VCSUNIT1

Address:	1C4FCh-1C4FFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_11_VCSUNIT1

Address:	224D0h-224D3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_0_BCSUNIT

Address:	224D4h-224D7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_1_BCSUNIT

Address:	224D8h-224DBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_2_BCSUNIT

Address:	224DCh-224DFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_3_BCSUNIT

Address:	224E0h-224E3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_4_BCSUNIT

Address:	224E4h-224E7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_5_BCSUNIT

Address:	224E8h-224EBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_6_BCSUNIT

Address:	224ECh-224EFh
Name:	FORCE_TO_NONPRIV

FORCE_TO_NONPRIV - FORCE_TO_NONPRIV

ShortName:	FORCE_TO_NONPRIV_7_BCSUNIT

Address:	224F0h-224F3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_8_BCSUNIT

Address:	224F4h-224F7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_9_BCSUNIT

Address:	224F8h-224FBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_10_BCSUNIT

Address:	224FCh-224FFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_11_BCSUNIT

These registers are privilege registers and are not allowed to be written from non-privilege batch buffer. These are global registers and power context save/restored.

Programming Notes
RCS_FORCE_TO_NONPRIV registers in render CS must be used to force the below registers to be treated as non-privileged by HW: • 0x7700 (GLOBAL_CLEAR_VALUE_0) • 0x7704 (GLOBAL_CLEAR_VALUE_1) • 0x7708 (GLOBAL_CLEAR_VALUE_2) • 0x770C (GLOBAL_CLEAR_VALUE_3)

DWord	Bit	Description
0	31:26	**Reserved** Format: MBZ
	25:2	**Non Privilege Register Address** Format: MmioAddress[25:2] This field contains the MMIO offset of a register. MMIO offset programmed in this field will be treated as a non-privilege register by render command streamer while processing register writes from a non-privilege batch buffer. This register provides programmability is to extend the non-privilege register table mentioned in MI_BATCH_BUFFER_START command in render command streamer. **Value** / **Name** 825h / **[Default]**
	1:0	**Reserved** Format: MBZ

Frame count and Draw call number

FCDCN - Frame count and Draw call number		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0B430h	

DWord	Bit	Description
0	31:16	**Reserved**
		Access: ⟶ RO
	15:8	**Frame Number**
		Access: ⟶ R/W
		Frame number is the first of two reporting tags that software (i.e. driver) may populate in order to provide reference points during L3 performance reporting modes. Should the "Frame Count and Draw Call Enable" bit (FCDCE) in the "First Buffer Size and Start" register be set, LPFC will selectively replace one of the reporting events with this programmable tag (in addition to the "Draw Call Number" field below).
		Software may use this to provide reference points for L3 performance counts when parsing the resulting data stream to align reported counts to higher-level operations.
		The original incarnation called for software to increment this value with each frame, however, the field is generic and may be used for any tagging purpose.
	7:0	**Draw call number**
		Access: ⟶ R/W
		The draw call number is the second programmable reporting tag provided by LPFC.
		With this second programmable tag, a more granular sampling boundary may be created by software, or it may be used to provide an alternative reference point for tracking L3 performance. The original incarnation called for software to increment this value with every draw call, but the field is generic and may be used for any similar purpose.

FUSEWORD0

FUSEWORD0 - FUSEWORD0		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	182130h	
Fuse readout information.		

DWord	Bit	Description	
0	31:0	**FUSEDW0**	
		Default Value:	00000000h
		Access:	RO
		Fuse Information DW0	

FUSEWORD1

<table>
<tr><td colspan="4" align="center">**FUSEWORD1 - FUSEWORD1**</td></tr>
<tr><td colspan="4">Register Space: MMIO: 0/2/0</td></tr>
<tr><td colspan="4">Project: CHV, BSW</td></tr>
<tr><td colspan="4">Source: PRM</td></tr>
<tr><td colspan="4">Default Value: 0x00000000</td></tr>
<tr><td colspan="4">Size (in bits):   32</td></tr>
<tr><td colspan="4">Address: 182134h</td></tr>
<tr><td colspan="4">Fuse readout information.</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td colspan="2">**Description**</td></tr>
<tr><td>0</td><td>31:0</td><td colspan="2">**FUSEDW1**</td></tr>
<tr><td></td><td></td><td>Default Value:</td><td>00000000h</td></tr>
<tr><td></td><td></td><td>Access:</td><td>RO</td></tr>
<tr><td></td><td></td><td colspan="2">Fuse Information DW1</td></tr>
</table>

FUSEWORD2

<table>
<tr><td colspan="4" align="center">**FUSEWORD2 - FUSEWORD2**</td></tr>
<tr><td>Register Space:</td><td colspan="3">MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td colspan="3">CHV, BSW</td></tr>
<tr><td>Source:</td><td colspan="3">PRM</td></tr>
<tr><td>Default Value:</td><td colspan="3">0x00000000</td></tr>
<tr><td>Size (in bits):</td><td colspan="3">32</td></tr>
<tr><td>Address:</td><td colspan="3">182138h</td></tr>
<tr><td colspan="4">Fuse readout information.</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td colspan="2">**Description**</td></tr>
<tr><td rowspan="4">0</td><td rowspan="4">31:0</td><td colspan="2">**FUSEDW2**</td></tr>
<tr><td>Default Value:</td><td>00000000h</td></tr>
<tr><td>Access:</td><td>RO</td></tr>
<tr><td colspan="2">Fuse Information DW2</td></tr>
</table>

FUSEWORD3

<table>
<tr><td colspan="4" align="center">**FUSEWORD3 - FUSEWORD3**</td></tr>
<tr><td>Register Space:</td><td colspan="3">MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td colspan="3">CHV, BSW</td></tr>
<tr><td>Source:</td><td colspan="3">PRM</td></tr>
<tr><td>Default Value:</td><td colspan="3">0x00000000</td></tr>
<tr><td>Size (in bits):</td><td colspan="3">32</td></tr>
<tr><td>Address:</td><td colspan="3">18213Ch</td></tr>
<tr><td colspan="4">Fuse readout information.</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td colspan="2">**Description**</td></tr>
<tr><td>0</td><td>31:0</td><td colspan="2">**FUSEDW3**
<table><tr><td>Default Value:</td><td>00000000h</td></tr><tr><td>Access:</td><td>RO</td></tr></table>Fuse Information DW3</td></tr>
</table>

FUSEWORD4

<table>
<tr><td colspan="3" align="center">**FUSEWORD4 - FUSEWORD4**</td></tr>
<tr><td>Register Space:</td><td colspan="2">MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td colspan="2">CHV, BSW</td></tr>
<tr><td>Source:</td><td colspan="2">PRM</td></tr>
<tr><td>Default Value:</td><td colspan="2">0x00000000</td></tr>
<tr><td>Size (in bits):</td><td colspan="2">32</td></tr>
<tr><td>Address:</td><td colspan="2">182140h</td></tr>
<tr><td colspan="3">Fuse readout information.</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td>**Description**</td></tr>
<tr><td>0</td><td>31:0</td><td>**FUSEDW4**

Default Value: 00000000h
Access: RO

Fuse Information DW4</td></tr>
</table>

FUSEWORD5

<table>
<tr><td colspan="3" align="center">**FUSEWORD5 - FUSEWORD5**</td></tr>
<tr><td>Register Space:</td><td colspan="2">MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td colspan="2">CHV, BSW</td></tr>
<tr><td>Source:</td><td colspan="2">PRM</td></tr>
<tr><td>Default Value:</td><td colspan="2">0x00000000</td></tr>
<tr><td>Size (in bits):</td><td colspan="2">32</td></tr>
<tr><td>Address:</td><td colspan="2">182144h</td></tr>
<tr><td colspan="3">Fuse readout information.</td></tr>
</table>

DWord	Bit	Description
0	31:0	**FUSEDW5**

		Default Value:	00000000h
		Access:	RO

Fuse Information DW5

FUSEWORD6

<table>
<tr><td colspan="4" align="center">**FUSEWORD6 - FUSEWORD6**</td></tr>
<tr><td colspan="4">Register Space: MMIO: 0/2/0</td></tr>
<tr><td colspan="4">Project: CHV, BSW</td></tr>
<tr><td colspan="4">Source: PRM</td></tr>
<tr><td colspan="4">Default Value: 0x00000000</td></tr>
<tr><td colspan="4">Size (in bits):   32</td></tr>
<tr><td colspan="4">Address: 182148h</td></tr>
<tr><td colspan="4">Fuse readout information.</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td colspan="2">**Description**</td></tr>
<tr><td>0</td><td>31:0</td><td colspan="2">**FUSEDW6**</td></tr>
<tr><td></td><td></td><td>Default Value:</td><td>00000000h</td></tr>
<tr><td></td><td></td><td>Access:</td><td>RO</td></tr>
<tr><td></td><td></td><td colspan="2">Fuse Information DW6</td></tr>
</table>

FUSEWORD7

FUSEWORD7 - FUSEWORD7		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	18214Ch	
Fuse readout information.		
DWord	**Bit**	**Description**
0	31:0	**FUSEDW7**
		Default Value: 00000000h
		Access: RO
		Fuse Information DW7

FUSEWORD8

<table>
<tr><td colspan="4" align="center">**FUSEWORD8 - FUSEWORD8**</td></tr>
<tr><td>Register Space:</td><td colspan="3">MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td colspan="3">CHV, BSW</td></tr>
<tr><td>Source:</td><td colspan="3">PRM</td></tr>
<tr><td>Default Value:</td><td colspan="3">0x00000000</td></tr>
<tr><td>Size (in bits):</td><td colspan="3">32</td></tr>
<tr><td>Address:</td><td colspan="3">182150h</td></tr>
<tr><td colspan="4">Fuse readout information.</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td colspan="2">**Description**</td></tr>
<tr><td rowspan="4">0</td><td rowspan="4">31:0</td><td colspan="2">**FUSEDW8**</td></tr>
<tr><td>Default Value:</td><td>00000000h</td></tr>
<tr><td>Access:</td><td>RO</td></tr>
<tr><td colspan="2">Fuse Information DW8</td></tr>
</table>

FUSEWORD9

<table>
<tr><td colspan="4" align="center">**FUSEWORD9 - FUSEWORD9**</td></tr>
<tr><td>Register Space:</td><td colspan="3">MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td colspan="3">CHV, BSW</td></tr>
<tr><td>Source:</td><td colspan="3">PRM</td></tr>
<tr><td>Default Value:</td><td colspan="3">0x00000000</td></tr>
<tr><td>Size (in bits):</td><td colspan="3">32</td></tr>
<tr><td>Address:</td><td colspan="3">182154h</td></tr>
<tr><td colspan="4">Fuse readout information.</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td colspan="2">**Description**</td></tr>
<tr><td rowspan="4" align="center">0</td><td rowspan="4" align="center">31:0</td><td colspan="2">**FUSEDW9**</td></tr>
<tr><td>Default Value:</td><td>00000000h</td></tr>
<tr><td>Access:</td><td>RO</td></tr>
<tr><td colspan="2">Fuse Information DW9</td></tr>
</table>

FUSEWORD10

<table>
<tr><td colspan="4" align="center">**FUSEWORD10 - FUSEWORD10**</td></tr>
<tr><td>Register Space:</td><td colspan="3">MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td colspan="3">CHV, BSW</td></tr>
<tr><td>Source:</td><td colspan="3">PRM</td></tr>
<tr><td>Default Value:</td><td colspan="3">0x00000000</td></tr>
<tr><td>Size (in bits):</td><td colspan="3">32</td></tr>
<tr><td>Address:</td><td colspan="3">182158h</td></tr>
<tr><td colspan="4">Fuse readout information.</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td colspan="2">**Description**</td></tr>
<tr><td rowspan="4">0</td><td rowspan="4">31:0</td><td colspan="2">**FUSEDW10**</td></tr>
<tr><td>Default Value:</td><td>00000000h</td></tr>
<tr><td>Access:</td><td>RO</td></tr>
<tr><td colspan="2">Fuse information DW10</td></tr>
</table>

FUSEWORD11

FUSEWORD11 - FUSEWORD11		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	18215Ch	
Fuse readout information.		

DWord	Bit	Description
0	31:0	**FUSEDW11**
		Default Value: 00000000h
		Access: RO
		Fuse information DW11

FUSEWORD12

<table>
<tr><td colspan="4" align="center">**FUSEWORD12 - FUSEWORD12**</td></tr>
<tr><td>Register Space:</td><td colspan="3">MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td colspan="3">CHV, BSW</td></tr>
<tr><td>Source:</td><td colspan="3">PRM</td></tr>
<tr><td>Default Value:</td><td colspan="3">0x00000000</td></tr>
<tr><td>Size (in bits):</td><td colspan="3">32</td></tr>
<tr><td>Address:</td><td colspan="3">182160h</td></tr>
<tr><td colspan="4">Fuse readout information. CHV, BSW: New for CHV, BSW.</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td colspan="2">**Description**</td></tr>
<tr><td rowspan="4">0</td><td rowspan="4">31:0</td><td colspan="2">**FUSEDW12**</td></tr>
<tr><td>Default Value:</td><td>00000000h</td></tr>
<tr><td>Access:</td><td>RO</td></tr>
<tr><td colspan="2">Fuse information DW12</td></tr>
</table>

FUSEWORD13

<table>
<tr><td colspan="3" align="center">**FUSEWORD13 - FUSEWORD13**</td></tr>
<tr><td>Register Space:</td><td colspan="2">MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td colspan="2">CHV, BSW</td></tr>
<tr><td>Source:</td><td colspan="2">PRM</td></tr>
<tr><td>Default Value:</td><td colspan="2">0x00000000</td></tr>
<tr><td>Size (in bits):</td><td colspan="2">32</td></tr>
<tr><td>Address:</td><td colspan="2">182164h</td></tr>
<tr><td colspan="3">Fuse readout information. CHV, BSW: New for CHV, BSW.</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td>**Description**</td></tr>
<tr><td>0</td><td>31:0</td><td>**FUSEDW13**

Default Value: 00000000h

Access: RO

Fuse information DW13</td></tr>
</table>

FUSEWORD14

FUSEWORD14 - FUSEWORD14		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	182168h	
Fuse readout information. CHV, BSW: New for CHV, BSW.		
DWord	**Bit**	**Description**
0	31:0	**FUSEDW14**
		Default Value: 00000000h
		Access: RO
		Fuse information DW14 [31:28] - FUSE_GT_EU_DISABLE: SS1, ROW1 - EU[3:0] [27:24] - FUSE_GT_EU_DISABLE: SS1, ROW0 - EU[3:0] [23:20] - FUSE_GT_EU_DISABLE: SS0, ROW1 - EU[3:0] [19:16] - FUSE_GT_EU_DISABLE: SS0, ROW0 - EU[3:0] [11] - FUSE_GT_SUBSLICE_DISABLE - SS1 [10] - FUSE_GT_SUBSLICE_DISABLE - SS0

FUSEWORD15

<table>
<tr><td colspan="4" align="center">**FUSEWORD15 - FUSEWORD15**</td></tr>
<tr><td colspan="4">Register Space: MMIO: 0/2/0</td></tr>
<tr><td colspan="4">Project: CHV, BSW</td></tr>
<tr><td colspan="4">Source: PRM</td></tr>
<tr><td colspan="4">Default Value: 0x00000000</td></tr>
<tr><td colspan="4">Size (in bits):   32</td></tr>
<tr><td colspan="4">Address: 18216Ch</td></tr>
<tr><td colspan="4">Fuse readout information. CHV, BSW: New for CHV, BSW.</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td colspan="2">**Description**</td></tr>
<tr>
<td>0</td>
<td>31:0</td>
<td colspan="2">

FUSEDW15

Default Value:	00000000h
Access:	RO

Fuse information DW15
</td>
</tr>
</table>

FUSEWORD16

<table>
<tr><td colspan="4" align="center">**FUSEWORD16 - FUSEWORD16**</td></tr>
<tr><td>Register Space:</td><td colspan="3">MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td colspan="3">CHV, BSW</td></tr>
<tr><td>Source:</td><td colspan="3">PRM</td></tr>
<tr><td>Default Value:</td><td colspan="3">0x00000000</td></tr>
<tr><td>Size (in bits):</td><td colspan="3">32</td></tr>
<tr><td>Address:</td><td colspan="3">182170h</td></tr>
<tr><td colspan="4">Fuse readout information. CHV, BSW: New for CHV, BSW.</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td colspan="2">**Description**</td></tr>
<tr><td>0</td><td>31:0</td><td colspan="2">**FUSEDW16**</td></tr>
<tr><td></td><td></td><td>Default Value:</td><td>00000000h</td></tr>
<tr><td></td><td></td><td>Access:</td><td>RO</td></tr>
<tr><td></td><td></td><td colspan="2">Fuse information DW16</td></tr>
</table>

FUSEWORD17

<table>
<tr><td colspan="4" align="center">**FUSEWORD17 - FUSEWORD17**</td></tr>
<tr><td>Register Space:</td><td colspan="3">MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td colspan="3">CHV, BSW</td></tr>
<tr><td>Source:</td><td colspan="3">PRM</td></tr>
<tr><td>Default Value:</td><td colspan="3">0x00000000</td></tr>
<tr><td>Size (in bits):</td><td colspan="3">32</td></tr>
<tr><td>Address:</td><td colspan="3">182174h</td></tr>
<tr><td colspan="4">Fuse readout information. CHV, BSW: New for CHV, BSW.</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td colspan="2">**Description**</td></tr>
<tr><td>0</td><td>31:0</td><td colspan="2">**FUSEDW17**</td></tr>
<tr><td></td><td></td><td>Default Value:</td><td>00000000h</td></tr>
<tr><td></td><td></td><td>Access:</td><td>RO</td></tr>
<tr><td></td><td></td><td colspan="2">Spare</td></tr>
</table>

FUSEWORD18

<table>
<tr><td colspan="3" align="center">**FUSEWORD18 - FUSEWORD18**</td></tr>
<tr><td>Register Space:</td><td colspan="2">MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td colspan="2">CHV, BSW</td></tr>
<tr><td>Source:</td><td colspan="2">PRM</td></tr>
<tr><td>Default Value:</td><td colspan="2">0x00000000</td></tr>
<tr><td>Size (in bits):</td><td colspan="2">32</td></tr>
<tr><td>Address:</td><td colspan="2">182178h</td></tr>
<tr><td colspan="3">Fuse readout information. CHV, BSW: New for CHV, BSW.</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td>**Description**</td></tr>
<tr><td>0</td><td>31:0</td><td>**FUSEDW18**

Default Value: 00000000h

Access: RO

Spare</td></tr>
</table>

FUSEWORD19

<table>
<tr><td colspan="4" align="center">**FUSEWORD19 - FUSEWORD19**</td></tr>
<tr><td>Register Space:</td><td colspan="3">MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td colspan="3">CHV, BSW</td></tr>
<tr><td>Source:</td><td colspan="3">PRM</td></tr>
<tr><td>Default Value:</td><td colspan="3">0x00000000</td></tr>
<tr><td>Size (in bits):</td><td colspan="3">32</td></tr>
<tr><td>Address:</td><td colspan="3">18217Ch</td></tr>
<tr><td colspan="4">Fuse readout information. CHV, BSW: New for CHV, BSW.</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td colspan="2">**Description**</td></tr>
<tr><td>0</td><td>31:0</td><td colspan="2">**FUSEDW19**</td></tr>
<tr><td></td><td></td><td>Default Value:</td><td>00000000h</td></tr>
<tr><td></td><td></td><td>Access:</td><td>RO</td></tr>
<tr><td></td><td></td><td colspan="2">Spare</td></tr>
</table>

G3D Control Register

G3DCTL - G3D Control Register		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	09024h	
G3D unit Control Register. Controls GUNIT's response to GAM Traffic.		

DWord	Bit	Description
0	31:27	**G3D Spare** <table><tr><td>Access:</td><td>R/W</td></tr></table> Spare config bits sent to G3D.
	26	**RTN Mode** <table><tr><td>Access:</td><td>R/W</td></tr></table> RTN mode. When set to one all GAM read returns are considered slow (no b2b to any source ID).
	25	**Return Ordering Queue Disable** <table><tr><td>Access:</td><td>R/W</td></tr></table> ROQ Disable. When set to a '1', the G3D Return Ordering queue will be mostly disabled by forcing the Data queue to be considered full when it has one entry occupied.
	24	**Command Bandwidth Arb Mode** <table><tr><td>Access:</td><td>R/W</td></tr></table> Command Bandwidth Arbitration mode. When programmed to a '1', reads will be allowed to go 1 cycle after writes as long as writes are not in write grant mode.
	23:0	**RSVD** <table><tr><td>Access:</td><td>RO</td></tr></table> Reserved.

GAB Arbitration Programmable

<table>
<tr><td colspan="3" align="center">**GAB_AP - GAB Arbitration Programmable**</td></tr>
<tr><td colspan="3">Register Space: MMIO: 0/2/0</td></tr>
<tr><td colspan="3">Project: CHV, BSW</td></tr>
<tr><td colspan="3">Source: PRM</td></tr>
<tr><td colspan="3">Default Value: 0x00000000</td></tr>
<tr><td colspan="3">Size (in bits):   32</td></tr>
<tr><td colspan="3">Address: 040F0h</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td>**Description**</td></tr>
<tr><td>0</td><td>31:0</td><td>**Reserved**</td></tr>
</table>

GAB GAC GAM Idle

GABGACGAMIDLE - GAB GAC GAM Idle		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A540h-0A543h	

DWord	Bit	Description
0	31:26	**Reserved** Access: RO
	25:16	**GAM Idle Timeout** Access: R/W **Programming Notes** This mode is not supported. It must be 0 at all times.
	15:10	**Reserved** Access: RO
	9:0	**Min GAB GAC Idle** Access: R/W **Programming Notes** This mode is not supported. It must be 0 at all times.

GAB LRA 0

		GAB_LRA_0 - GAB LRA 0		
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x1F100F00			
Size (in bits):	32			
Address:	04A70h			

DWord	Bit	Description		
0	31:29	**Reserved**		
		Default Value:		000b
		Access:		RO
	28:24	**GAB LRA1 Max**		
		Default Value:		11111b
		Access:		R/W
		Maximum value of programmable LRA1.		
	23:21	**Reserved**		
		Default Value:		000b
		Access:		RO
	20:16	**GAB LRA1 Min**		
		Default Value:		10000b
		Access:		R/W
		Minimum value of programmable LRA1.		
	15:13	**Reserved**		
		Default Value:		000b
		Access:		RO
	12:8	**GAB LRA0 Max**		
		Default Value:		01111b
		Access:		R/W
		Maximum value of programmable LRA0.		
	7:5	**Reserved**		
		Default Value:		000b
		Access:		RO

GAB_LRA_0 - GAB LRA 0		
4:0	**GABLRA0 Min**	
	Default Value:	00000b
	Access:	R/W
	Minimum value of programmable LRA0.	

GAB LRA 1

GAB_LRA_1 - GAB LRA 1		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000001	
Size (in bits):	32	
Address:	04A74h	

DWord	Bit	Description	
0	31:4	**Reserved**	
		Default Value:	0000000h
		Access:	RO
	3:2	**BLB**	
		Default Value:	00b
		Access:	R/W
		Which LRA should BLB use.	
	1:0	**BCS**	
		Default Value:	01b
		Access:	R/W
		Which LRA should BCS use.	

GAB unit Control Register

GAB_CTL_REG - GAB unit Control Register		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	BlitterCS	
Default Value:	0x000000BF	
Access:	R/W	
Size (in bits):	32	
Address:	24000h	
DefaultValue=FF0000BFh Trusted Type = 1		

DWord	Bit	Description
0	31:9	**Reserved**
	8	**Continue after Page Fault**

Value	Name	Description
1	GAB Set	Ipon receiving a page fault when requesting an address translation, GAB will set address bit 39 to 1 and continue.
0	GAB Hang	GAB will hang on a page fault. Default = b0.

| | 7:6 | **PPGTT BCS TLB LRA MIN** |

Default Value:	10b
TLB Depth Partitioning Register In PP GTT Mode.	

| | 5:4 | **GAB write request priority signal value used in GAC arbitration** |

Default Value:	11b

| | 3:2 | **GAB read only request priority signal value used in GAC arbitration** |

Default Value:	11b

| | 1:0 | **GAB read request priority signal value used in GAC arbitration** |

Default Value:	11b

GAC_GAM Arbitration Counters Register 0

ARB_GAC_GAM_REQCNTS0 - GAC_GAM Arbitration Counters Register 0		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	043A8h	

DWord	Bit	Description
0	31:22	**Reserved**
	21:16	**Number of GAC WR requests to be accumulated before applying the arbitration**
	15:14	**Reserved**
	13:8	**Number of GAC R requests to be accumulated before applying the arbitration**
	7:6	**Reserved**
	5:0	**Number of GAC RO requests to be accumulated before applying the arbitration**

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GAC_GAM Arbitration Counters Register 1

ARB_GAC_GAM_REQCNTS1 - GAC_GAM Arbitration Counters Register 1		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	043ACh	

DWord	Bit	Description
0	31:22	**Reserved**
	21:16	**Number of GAC WR requests to be accumulated before applying the arbitration**
	15:14	**Reserved**
	13:8	**Number of GAC R requests to be accumulated before applying the arbitration**
	7:6	**Reserved**
	5:0	**Number of GAC RO requests to be accumulated before applying the arbitration**

GAC_GAM R Arbitration Register 0

ARB_R_GAC_GAM0 - GAC_GAM R Arbitration Register 0		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	043E0h	

DWord	Bit	Description
0	31:28	**Reserved**
	27	**Priority for entry 1**
	26:24	**Goto field for entry 1 when request vector is 11b**
	23:21	**Goto field for entry 1 when request vector is 10b**
	20:18	**Goto field for entry 1 when request vector is 01b**
	17:15	**Goto field for entry 1 when request vector is 00b**
	14:13	**Reserved**
	12	**Priority for entry 0**
	11:9	**Goto field for entry 0 when request vector is 11b**
	8:6	**Goto field for entry 0 when request vector is 10b**
	5:3	**Goto field for entry 0 when request vector is 01b**
	2:0	**Goto field for entry 0 when request vector is 00b**

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GAC_GAM R Arbitration Register 1

ARB_R_GAC_GAM1 - GAC_GAM R Arbitration Register 1		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	043E4h	

DWord	Bit	Description
0	31:28	**Reserved**
	27	**Priority for entry 3**
	26:24	**Goto field for entry 3 when request vector is 11b**
	23:21	**Goto field for entry 3 when request vector is 10b**
	20:18	**Goto field for entry 3 when request vector is 01b**
	17:15	**Goto field for entry 3 when request vector is 00b**
	14:13	**Reserved**
	12	**Priority for entry 2**
	11:9	**Goto field for entry 2 when request vector is 11b**
	8:6	**Goto field for entry 2 when request vector is 10b**
	5:3	**Goto field for entry 2 when request vector is 01b**
	2:0	**Goto field for entry 2 when request vector is 00b**

GAC_GAM R Arbitration Register 2

ARB_R_GAC_GAM2 - GAC_GAM R Arbitration Register 2		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	043E8h	

DWord	Bit	Description
0	31:28	**Reserved**
	27	**Priority for entry 5**
	26:24	**Goto field for entry 5 when request vector is 11b**
	23:21	**Goto field for entry 5 when request vector is 10b**
	20:18	**Goto field for entry 5 when request vector is 01b**
	17:15	**Goto field for entry 5 when request vector is 00b**
	14:13	**Reserved**
	12	**Priority for entry 4**
	11:9	**Goto field for entry 4 when request vector is 11b**
	8:6	**Goto field for entry 4 when request vector is 10b**
	5:3	**Goto field for entry 4 when request vector is 01b**
	2:0	**Goto field for entry 4 when request vector is 00b**

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GAC_GAM R Arbitration Register 3

ARB_R_GAC_GAM3 - GAC_GAM R Arbitration Register 3		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	043ECh	

DWord	Bit	Description
0	31:28	**Reserved**
	27	**Priority for entry 7**
	26:24	**Goto field for entry 7 when request vector is 11b**
	23:21	**Goto field for entry 7 when request vector is 10b**
	20:18	**Goto field for entry 7 when request vector is 01b**
	17:15	**Goto field for entry 7 when request vector is 00b**
	14:13	**Reserved**
	12	**Priority for entry 6**
	11:9	**Goto field for entry 6 when request vector is 11b**
	8:6	**Goto field for entry 6 when request vector is 10b**
	5:3	**Goto field for entry 6 when request vector is 01b**
	2:0	**Goto field for entry 6 when request vector is 00b**

GAC_GAM RO Arbitration Register 0

ARB_RO_GAC_GAM0 - GAC_GAM RO Arbitration Register 0		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	043D0h	

DWord	Bit	Description
0	31:28	**Reserved**
	27	**Priority for entry 1**
	26:24	**Goto field for entry 1 when request vector is 11b**
	23:21	**Goto field for entry 1 when request vector is 10b**
	20:18	**Goto field for entry 1 when request vector is 01b**
	17:15	**Goto field for entry 1 when request vector is 00b**
	14:13	**Reserved**
	12	**Priority for entry 01**
	11:9	**Goto field for entry 01 when request vector is 11b**
	8:6	**Goto field for entry 01 when request vector is 10b**
	5:3	**Goto field for entry 01 when request vector is 01b**
	2:0	**Goto field for entry 01 when request vector is 00b**

GAC_GAM RO Arbitration Register 1

ARB_RO_GAC_GAM1 - GAC_GAM RO Arbitration Register 1		

Register Space: MMIO: 0/2/0
Project: CHV, BSW
Source: RenderCS
Default Value: 0x00000000
Access: R/W
Size (in bits): 32
Trusted Type: 1

Address: 043D4h

DWord	Bit	Description
0	31:28	**Reserved**
	27	**Priority for entry 3**
	26:24	**Goto field for entry 3 when request vector is 11b**
	23:21	**Goto field for entry 3 when request vector is 10b**
	20:18	**Goto field for entry 3 when request vector is 01b**
	17:15	**Goto field for entry 3 when request vector is 00b**
	14:13	**Reserved**
	12	**Priority for entry 2**
	11:9	**Goto field for entry 2 when request vector is 11b**
	8:6	**Goto field for entry 2 when request vector is 10b**
	5:3	**Goto field for entry 2 when request vector is 01b**
	2:0	**Goto field for entry 2 when request vector is 00b**

GAC_GAM RO Arbitration Register 2

ARB_RO_GAC_GAM2 - GAC_GAM RO Arbitration Register 2		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	043D8h	

DWord	Bit	Description
0	31:28	**Reserved**
	27	**Priority for entry 5**
	26:24	**Goto field for entry 5 when request vector is 11b**
	23:21	**Goto field for entry 5 when request vector is 10b**
	20:18	**Goto field for entry 5 when request vector is 01b**
	17:15	**Goto field for entry 5 when request vector is 00b**
	14:13	**Reserved**
	12	**Priority for entry 4**
	11:9	**Goto field for entry 4 when request vector is 11b**
	8:6	**Goto field for entry 4 when request vector is 10b**
	5:3	**Goto field for entry 4 when request vector is 01b**
	2:0	**Goto field for entry 4 when request vector is 00b**

GAC_GAM RO Arbitration Register 3

	ARB_RO_GAC_GAM3 - GAC_GAM RO Arbitration Register 3	
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	043DCh	

DWord	Bit	Description
0	31:28	**Reserved**
	27	**Priority for entry 7**
	26:24	**Goto field for entry 7 when request vector is 11b**
	23:21	**Goto field for entry 7 when request vector is 10b**
	20:18	**Goto field for entry 7 when request vector is 01b**
	17:15	**Goto field for entry 7 when request vector is 00b**
	14:13	**Reserved**
	12	**Priority for entry 6**
	11:9	**Goto field for entry 6 when request vector is 11b**
	8:6	**Goto field for entry 6 when request vector is 10b**
	5:3	**Goto field for entry 6 when request vector is 01b**
	2:0	**Goto field for entry 6 when request vector is 00b**

GAC_GAM WR Arbitration Register 0

ARB_WR_GAC_GAM0 - GAC_GAM WR Arbitration Register 0		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	043F0h	

DWord	Bit	Description
0	31:28	**Reserved**
	27	**Priority for entry 1**
	26:24	**Goto field for entry 1 when request vector is 11b**
	23:21	**Goto field for entry 1 when request vector is 10b**
	20:18	**Goto field for entry 1 when request vector is 01b**
	17:15	**Goto field for entry 1 when request vector is 00b**
	14:13	**Reserved**
	12	**Priority for entry 0**
	11:9	**Goto field for entry 0 when request vector is 11b**
	8:6	**Goto field for entry 0 when request vector is 10b**
	5:3	**Goto field for entry 0 when request vector is 01b**
	2:0	**Goto field for entry 0 when request vector is 00b**

GAC_GAM WR Arbitration Register 1

ARB_WR_GAC_GAM1 - GAC_GAM WR Arbitration Register 1		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	043F4h	

DWord	Bit	Description
0	31:28	**Reserved**
	27	**Priority for entry 3**
	26:24	**Goto field for entry 3 when request vector is 11b**
	23:21	**Goto field for entry 3 when request vector is 10b**
	20:18	**Goto field for entry 3 when request vector is 01b**
	17:15	**Goto field for entry 3 when request vector is 00b**
	14:13	**Reserved**
	12	**Priority for entry 2**
	11:9	**Goto field for entry 2 when request vector is 11b**
	8:6	**Goto field for entry 2 when request vector is 10b**
	5:3	**Goto field for entry 2 when request vector is 01b**
	2:0	**Goto field for entry 2 when request vector is 00b**

GAC_GAM WR Arbitration Register 2

ARB_WR_GAC_GAM2 - GAC_GAM WR Arbitration Register 2		

Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	

Address:	043F8h	

DWord	Bit	Description
0	31:28	**Reserved**
	27	**Priority for entry 5**
	26:24	**Goto field for entry 5 when request vector is 11b**
	23:21	**Goto field for entry 5 when request vector is 10b**
	20:18	**Goto field for entry 5 when request vector is 01b**
	17:15	**Goto field for entry 5 when request vector is 00b**
	14:13	**Reserved**
	12	**Priority for entry 4**
	11:9	**Goto field for entry 4 when request vector is 11b**
	8:6	**Goto field for entry 4 when request vector is 10b**
	5:3	**Goto field for entry 4 when request vector is 01b**
	2:0	**Goto field for entry 4 when request vector is 00b**

GAC_GAM WR Arbitration Register 3

ARB_WR_GAC_GAM3 - GAC_GAM WR Arbitration Register 3		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	043FCh	

DWord	Bit	Description
0	31:28	**Reserved**
	27	**Priority for entry 7**
	26:24	**Goto field for entry 7 when request vector is 11b**
	23:21	**Goto field for entry 7 when request vector is 10b**
	20:18	**Goto field for entry 7 when request vector is 01b**
	17:15	**Goto field for entry 7 when request vector is 00b**
	14:13	**Reserved**
	12	**Priority for entry 6**
	11:9	**Goto field for entry 6 when request vector is 11b**
	8:6	**Goto field for entry 6 when request vector is 10b**
	5:3	**Goto field for entry 6 when request vector is 01b**
	2:0	**Goto field for entry 6 when request vector is 00b**

GAM and SA Communication Register

GAMSACOMREG - GAM and SA Communication Register		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	042A0h	

DWord	Bit	Description
0	31:16	**Mask Bits** <table><tr><td>Default Value:</td><td>0000h</td></tr><tr><td>Access:</td><td>RO</td></tr></table> Mask Bits act as Write Enables for the bits[15:0] of this register.
	15	**GAM and SA Communication Register 15** <table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> For Future Use. This bit is self clear.
	14	**GAM and SA Communication Register 14** <table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> For Future Use. This bit is self clear.
	13	**GAM and SA Communication Register 13** <table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> For Future Use. This bit is self clear.
	12	**GAM and SA Communication Register 12** <table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> For Future Use. This bit is self clear.
	11	**GAM and SA Communication Register 11** <table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> For Future Use.

GAMSACOMREG - GAM and SA Communication Register

		This bit is self clear.	
	10	**GAM and SA Communication Register 10**	
		Default Value:	0b
		Access:	R/W
		For Future Use. This bit is self clear.	
	9	**GAM and SA Communication Register 9**	
		Default Value:	0b
		Access:	R/W
		For Future Use. This bit is self clear.	
	8	**GAM and SA Communication Register 8**	
		Default Value:	0b
		Access:	R/W
		For Future Use. This bit is self clear.	
	7	**GAM and SA Communication Register 7**	
		Default Value:	0b
		Access:	R/W
		For Future Use. This bit is self clear.	
	6	**GAM and SA Communication Register 6**	
		Default Value:	0b
		Access:	R/W
		For Future Use. This bit is self clear.	
	5	**GAM and SA Communication Register 5**	
		Default Value:	0b
		Access:	R/W
		For Future Use. This bit is self clear.	
	4	**GAM and SA Communication Register 4**	
		Default Value:	0b
		Access:	R/W
		For Future Use. This bit is self clear.	
	3	**GAM and SA Communication Register 3**	
		Default Value:	0b
		Access:	R/W

GAMSACOMREG - GAM and SA Communication Register

		For Future Use. This bit is self clear.	
	2	**GAM and SA Communication Register 2**	
		Default Value:	0b
		Access:	R/W
		Bit2 - Root Table Address Update Request. This bit is self clear.	
	1	**GAM and SA Communication Register 1**	
		Default Value:	0b
		Access:	R/W
		Bit1 - Queued Descriptor Request. This bit is self clear.	
	0	**GAM and SA Communication Register 0**	
		Default Value:	0b
		Access:	R/W
		Bit0 - Context Cache Invalidator Request. This bit is self clear.	

Gam Fub Done1 Lookup Register

DONE1_REG - Gam Fub Done1 Lookup Register		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0407Ch	
DWord	**Bit**	**Description**
0	31:0	**Gam Fub Done1 Lookup Reg**
		Default Value: / 00000000h
		Access: / RO
		GAM Done1 signals.

Gam Fub Done Lookup Register

DONE_REG - Gam Fub Done Lookup Register	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	040B0h

DWord	Bit	Description
0	31:0	**Gam Fub Done Lookup Reg**

Default Value:	00000000h
Access:	RO

31 CVS Credit Fifo is empty.
30 CVS TLB does not have any cycles.
29 Z Credit fifo is empty.
28 ZTLB does not have any cycles.
27 RCC Credit Fifo is empty.
26 RCC TLB does not have any cycles.
25 L3 Credit fifo is empty.
24 L3 TLB does not have any cycles.
23 VLF Credit fifo is empty.
22 VLF TLB does not have any cycles.
21 CASC Credit fifo empty.
20 CASC TLB does not have any cycles.
19 Miss Fub Done.
18 Read Stream Done.
17 Read Steam Fifo is empty.
16 Recycle Fifo in rstrm is empty.
15 TLB Pend Done.
14 TLB Pend PQ Array is done.
13 TLB pend PB Array is done.
12 Read route fub is done.
11 Gafm Data fifo is empty.
10 GAP data fifo is empty.
9 GAC data fifo is empty.
8 Wrdp is done with all the cycles.
7 Wrdp RID fifo is empty.
6 No hold from midarb to RTSTRM.
5 No hold from TLBPEND to MIDARB.

DONE_REG - Gam Fub Done Lookup Register		
		3 Tied to "1" - to be defined.
		2 Fence FSM are IDLE.
		1 Non PD Load Done.
		0 Tied to "1" - to be defined.

GAM Put Delay

GAM_PUT_DLY - GAM Put Delay		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0401Ch	
Number of clocks to wait between puts		

DWord	Bit	Description	
0	31:0	**GAM PUT DELAY**	
		Default Value:	00000000h
		Access:	R/W

GAMT_DONE Register

GAMT_DONE - GAMT_DONE Register		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04AC0h	

DWord	Bit	Description
0	31:0	**GAMT_DONE Register**

	Default Value:	00000000h
	Access:	RO

31: vebxtlb_all_done_f
30: cvstlb_all_done_f
29: ztlb_all_done_f
28: l3tlb_all_done_f
27: rcctlb_all_done_f
26: mfxtlb_all_done_f
25: vlftlb_all_done_f
24: bwgtlb_all_done_f
23: gamwrrb_all_done_f
22: mfxsl1tlb_all_done_f
21: vlfsl1tlb_all_done_f
20: bwgtlb_fifo_empty
19: l3tlb_fifo_empty
18: ztlb_fifo_empty
17: rcctlb_fifo_empty
16: cvstlb_fifo_empty
15: vebxtlb_fifo_empty
14: mfxtlb_fifo_empty
13: mfxsl1tlb_fifo_empty
12: vlfsl1tlb_fifo_empty
11: vlftlb_fifo_empty
10: wrdp_gafm_fifo_empty
9: wrdp_gap_fifo_empty
8: wrdp_gacfg_fifo_empty
7: wrdp_cs_fifo_empty
6: wrdp_vecs_fifo_empty
5: wrdp_oacs_fifo_empty
4: wrdp_gacv_fifo_empty

GAMT_DONE - GAMT_DONE Register		
		3: Tied to 1
		2: Tied to 1
		1: Tied to 1
		0: Tied to 1

GAMT_ECO_REG_RO_IA

GAMT_ECO_REG_RO_IA - GAMT_ECO_REG_RO_IA		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04AB4h	

DWord	Bit	Description	
0	31:0	**GAMTECO_REG_RO_IA**	
		Default Value:	00000000h
		Access:	RO
		This register is for ECO usage. RO register with IA Access Type on DEV reset.	

GAMT_ECO_REG_RW_IA

GAMT_ECO_REG_RW_IA - GAMT_ECO_REG_RW_IA	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW, :GT2:B
Source:	PRM
Default Value:	0x0000AB1B
Size (in bits):	32
Address:	04AB0h

Programmable Request Count - VEBX and BLT		
DWord	**Bit**	**Description**
0	31:0	**GAMTECO_REG_RW_IA** <table><tr><td>Default Value:</td><td>0000AB1Bh</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> Bit[31:16] = Reserved. Bit[15:8] = Number of max outstanding cycles (Misses and Hits not present) that can be allowed to potentially fault = 171. Bit[7:6] = Reserved. Bit[5:0] = Number of max outstanding misses that can be allowed to potentially fault = 27.

GAMT Arbiter Mode Control

GAMTARBMODE - GAMT Arbiter Mode Control		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000 CHV, BSW	
Size (in bits):	32	
Address:	04A08h	

DWord	Bit	Description
0	31:16	**Mask Bits**
		<table><tr><td>Default Value:</td><td>0000h</td></tr><tr><td>Access:</td><td>RO</td></tr></table>
	15	**GAMT Arbiter Mode Control 15**
		<table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> For Future Use
	14	**GAMT Arbiter Mode Control 14**
		<table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Project:</td><td>CHV, BSW</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> 0 - Cache the TLB even if there is a FAULT in GAMW read return. 1 - Don't Cache the TLB if there is a fault in GAMW return.
	13	**GAMT Arbiter Mode Control 13**
		<table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> 0 - VEBXTLB clock gate enabled. 1 - VEBXTLB clock gate disabled.
	12	**GAMT Arbiter Mode Control 12**
		<table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> 0 - MFXSL1TLB clock gate enabled. 1 - MFXSL1TLB clock gate disabled.
	11	**GAMT Arbiter Mode Control 11**
		<table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> 0 - VLFSL1TLB clock gate enabled. 1 - VLFSL1TLB clock gate disabled.

GAMTARBMODE - GAMT Arbiter Mode Control

	10	**GAMT Arbiter Mode Control 10**	
		Default Value:	0b
		Access:	R/W
		0 - gamwrrb clock gate enabled. 1 - gamwrrb clock gate disabled.	
	9	**GAMT Arbiter Mode Control 9**	
		Default Value:	0b
		Access:	R/W
		0 - BWGTLB clock gate enabled. 1 - BWGTLB clock gate disabled.	
	8	**GAMT Arbiter Mode Control 8**	
		Default Value:	0b
		Access:	R/W
		0 - VLFTLB clock gate enabled. 1 - VLFTLB clock gate disabled.	
	7	**GAMT Arbiter Mode Control 7**	
		Default Value:	0b
		Access:	R/W
		0 - MFXTLB clock gate enabled. 1 - MFXTLB clock gate disabled.	
	6	**GAMT Arbiter Mode Control 6**	
		Default Value:	0b
		Access:	R/W
		0 - RCCTLB clock gate enabled. 1 - RCCTLB clock gate disabled.	
	5	**GAMT Arbiter Mode Control 5**	
		Default Value:	0b
		Access:	R/W
		0 - L3TLB clock gate enabled. 1 - L3TLB clock gate disabled. bit[5] needs to be set as a work-around due to recent gacb bug. To update bit 5, a value of 0x00200020 needs to be written.	
	4	**GAMT Arbiter Mode Control 4**	
		Default Value:	0b
		Access:	R/W
		0 - ZTLB clock gate enabled. 1 - ZTLB clock gate disabled.	

GAMTARBMODE - GAMT Arbiter Mode Control

<table>
<tr><td rowspan="4">3</td><td colspan="2">GAMT Arbiter Mode Control 3</td></tr>
<tr><td>Default Value:</td><td>0b</td></tr>
<tr><td>Access:</td><td>R/W</td></tr>
<tr><td colspan="2">0 - CVS clock gate enabled.
1 - CVS clock gate disabled.</td></tr>

<tr><td rowspan="4">2</td><td colspan="2">GAMT Arbiter Mode Control 2</td></tr>
<tr><td>Default Value:</td><td>0b</td></tr>
<tr><td>Access:</td><td>R/W</td></tr>
<tr><td colspan="2">0 - No reg_hdc_inval_ack_force - take the value from client.
1 - reg_hdc_inval_ack_force - force value to 1 - disregard client value.</td></tr>

<tr><td rowspan="4">1</td><td colspan="2">GAMT Arbiter Mode Control 1</td></tr>
<tr><td>Default Value:</td><td>0b</td></tr>
<tr><td>Access:</td><td>R/W</td></tr>
<tr><td colspan="2">Bit [1]: Address Swizzling for Tiled Surfaces.
This register location is updated via GFX Driver prior to enabling DRAM accesses. Driver needs to obtain the need for memory address swizzling via DRAM configuration registers and set the following bits (in Display Engine and Render/Media access streams).
0: No address Swizzling.
1: Address bit[1] needs to be swizzled for tiled surfaces.</td></tr>

<tr><td rowspan="4">0</td><td colspan="2">GAMT Arbiter Mode Control 0</td></tr>
<tr><td>Default Value:</td><td>0b</td></tr>
<tr><td>Access:</td><td>R/W</td></tr>
<tr><td colspan="2">Bit[0]: GAM to Bypass GTT Translation.
GAM to Bypass GTT Translation and pass logical addresses through with 0's padded on the MSBs to form the Physical Address.</td></tr>
</table>

GAMW_ECO_BUS_RO_IA

GAMW_ECO_BUS_RO_IA - GAMW_ECO_BUS_RO_IA	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0408Ch

DWord	Bit	Description	
0	31:0	**GAMWECO_BUS_RO_IA**	
		Default Value:	00000000h
		Access:	RO
		This register is for ECO usage. RO register with IA Access Type on BUS reset.	

GAMW_ECO_BUS_RW_IA

GAMW_ECO_BUS_RW_IA - GAMW_ECO_BUS_RW_IA		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04084h	

DWord	Bit	Description	
0	31:0	**GAMWECO_BUS_RW_IA**	
		Default Value:	00000000h
		Access:	R/W
		This register is for ECO usage. RW register with IA Access Type on BUS reset.	

GAMW_ECO_DEV_RO_IA

GAMW_ECO_DEV_RO_IA - GAMW_ECO_DEV_RO_IA		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04088h	

DWord	Bit	Description
0	31:0	**GAMWECO_DEV_RO_IA**
			Default Value:	00000000h	
			Access:	RO	
		This register is for ECO usage. RO register with IA Access Type on DEV reset.

GAMW_ECO_DEV_RW_IA

GAMW_ECO_DEV_RW_IA - GAMW_ECO_DEV_RW_IA		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04080h	

DWord	Bit	Description	
0	31:0	**GAMWECO_DEV_RW_IA**	
		Default Value:	00000000h
		Access:	R/W

GAMW Power Context Save

PWRCTXSAVE - GAMW Power Context Save		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04000h	

DWord	Bit	Description		
0	31:16	**Mask Bits**		
		Default Value:		0000h
		Access:		RO
		Mask Bits act as Write Enables for the bits[15:0] of this register.		
	15	**Extra Bits15**		
		Default Value:		0b
		Access:		R/W
		Extra Bits for future use.		
	14	**Extra Bits14**		
		Default Value:		0b
		Access:		R/W
		Extra Bits for future use.		
	13	**Extra Bits13**		
		Default Value:		0b
		Access:		R/W
		Extra Bits for future use.		
	12	**Extra Bits12**		
		Default Value:		0b
		Access:		R/W
		Extra Bits for future use.		
	11	**Extra Bits11**		
		Default Value:		0b
		Access:		R/W
		Extra Bits for future use.		
	10	**Extra Bits10**		
		Default Value:		0b
		Access:		R/W
		Extra Bits for future use.		

PWRCTXSAVE - GAMW Power Context Save

	9	**Power Context Save Request**	
		Default Value:	0b
		Access:	R/W
		Power Context Save Bit[9] Power Context Save Request 1'b0: Power context save is not being requested (default). 1'b1: Power context save is being requested. Unit needs to self-clear this bit upon sampling. This bit is self clear.	
	8:0	**Power Context Save Quad Word Credits**	
		Default Value:	000000000b
		Access:	R/W
		Power Context Save Bits[8:0] QWord Credits for Power Context Save Request An initial length packet is required per power context save session, but that packet does not consume a credit. See protocol description for more details. Minimum Credits = 1: Unit may send 1 QWord pair. Maximum Credits = 511: Unit may send 511 QWord pairs. A QWord pair is defined as a 32-bit register address and the corresponding 32-bits of register data. Only valid with PWRCTX_SAVE_REQ (Bit9).	

GARB Messaging Register for Boot Controller

MSG_GARB_MBC - GARB Messaging Register for Boot Controller	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	16
Address:	0801Ch

Message registers have bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16]. In order to set bit0, for example, the data would be 0x0001_0001. In order to clear bit0, for example, the data would be 0x0001_0000. Note that mask bit is the data bit offset + 16. Message registers are protected from non-GT writes via the Message Channel.

DWord	Bit	Description	
0	15:7	**Reserved**	
		Access:	RO
	6	**Fuse Download Done Indication**	
		Access:	R/W
		Fuse Download Done Indication 1'b0 : Fuse download is not complete yet <default> 1'b1 : Fuse download is complete gpmunit self-clears this bit upon sampling.	
	5	**Boot Fetch Complete Indication**	
		Access:	R/W
		Boot Fetch Complete Indication 1'b0 : Boot Fetch is not complete yet <default> 1'b1 : Boot Fetch is complete gpmunit self-clears this bit upon sampling.	
	4	**IDI Block Status**	
		Access:	R/W
		IDI Block Status 1'b0 : IDI interface is not blocked <default> 1'b1 : IDI interface is blocked	
	3	**IDI Awake Status**	
		Access:	R/W
		IDI Awake Status 1'b0 : IDI interface is not ready <default> 1'b1 : IDI interface is ready	
	2	**Credit Active Status**	
		Access:	R/W
		Credit Active Status 1'b0 : Send credit active deassert Event Bus Message on transition from 1'b1 => 1'b0 <default> 1'b1 : Send credit active assert Event Bus Message on transition from 1'b0 => 1'b1	

MSG_GARB_MBC - GARB Messaging Register for Boot Controller

	1	**Global Arbitration Request**	
		Access:	R/W
		Global Arbitration Request 1'b0 : No request <default> 1'b1 : Request for arbitration Full handshake requiring ack	
	0	**Busy Indication**	
		Access:	R/W
		Busy Indication 1'b0 : Idle <default> 1'b1 : Busy Full handshake requiring ack	

GARB Messaging Register for Clocking Unit

MSG_GARB_GCP - GARB Messaging Register for Clocking Unit	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	16
Address:	08024h

Message registers have bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16]. In order to set bit0, for example, the data would be 0x0001_0001. In order to clear bit0, for example, the data would be 0x0001_0000. Note that mask bit is the data bit offset + 16. Message registers are protected from non-GT writes via the Message Channel.

DWord	Bit	Description
0	15:3	**Reserved** Access: RO
	2	**GCP Request to send FLR Complete Message to SA via GAM** Access: R/W GCP Request to send FLR Complete Message to SA via GAM 1'b0 : No request <default> 1'b1 : Send cycle on GA* Interface to address < address > with data < data > gpm will self-clear the request once it completes it. MBC needs to self-clear the acknowledgement once it sees it. GPM indicates a write cycle is complete once it puts it on the interface. GPM indicates a read cycle is complete once the read-return data comes back. gpmunit self-clears this bit upon sampling.
	1	**Global Arbitration Request** Access: R/W Global Arbitration Request 1'b0 : No request <default> 1'b1 : Request for arbitration Full handshake requiring ack
	0	**Busy Indication** Access: R/W Busy Indication 1'b0 : Idle <default> 1'b1 : Busy Full handshake requiring ack

Gather Constants Not Consumed By RCS

<table>
<tr><td colspan="2">**GATHER_CONST_PRODUCE_COUNT - Gather Constants Not Consumed By RCS**</td></tr>
<tr><td>Register Space:</td><td>MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td>CHV, BSW</td></tr>
<tr><td>Source:</td><td>RenderCS</td></tr>
<tr><td>Default Value:</td><td>0x00000000</td></tr>
<tr><td>Access:</td><td>R/W</td></tr>
<tr><td>Size (in bits):</td><td>32</td></tr>
<tr><td>Trusted Type:</td><td>1</td></tr>
<tr><td>Address:</td><td>0248Ch</td></tr>
</table>

This register keeps track of the outstanding Gather Constants produced by RS which are not yet consumed by Render Command Streamer. This register is part of the render context save and restore. This register should not be programmed by SW.

DWord	Bit	Description
0	31:0	**Gather Constants Produce Count** This register keeps track of the outstanding Gather Constants produced by RS which are not yet consumed by Render Command Streamer. This register is part of the render context save and restore.

GDR Per Client Write Drop Enables

WR_DROP_MODE - GDR Per Client Write Drop Enables		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	040B4h	

DWord	Bit	Description
0	31:0	**GDR Per Client Write Drop Enables**

Default Value:	00000000h
Access:	R/W

31 RSVD: Future use.
30 MBC write drop disable (0) or enable (1).
29 CS write drop disable (0) or enable (1).
28 SOL write drop disable (0) or enable (1).
27 RS write drop disable (0) or enable (1).
26 RCC write drop disable (0) or enable (1).
25 MSC write drop disable (0) or enable (1).
24 All L3 clients write drop disable (0) or enable (1).
23 STC write drop disable (0) or enable (1).
22 HIZ write drop disable (0) or enable (1).
21 RCZ write drop disable (0) or enable (1).
20 GAFS write drop disable (0) or enable (1).
19 GPM write drop disable (0) or enable (1).
18 GCP write drop disable (0) or enable (1).
17 VCS write drop disable (0) or enable (1).
16 BSP write drop disable (0) or enable (1).
15 VCR write drop disable (0) or enable (1).
14 VMX_RS write drop disable (0) or enable (1).
13 VMX_BS write drop disable (0) or enable (1).
12 VMX_RA write drop disable (0) or enable (1).
11 VMX_VDS write drop disable (0) or enable (1).
10 VLF_RS write drop disable (0) or enable (1).
9 VLF_FW write drop disable (0) or enable (1).
8 VECS write drop disable (0) or enable (1).
7 VEO write drop disable (0) or enable (1).

WR_DROP_MODE - GDR Per Client Write Drop Enables

		5 uC (DMA) write drop disable (0) or enable (1).
		4 BCS write drop disable (0) or enable (1).
		3 BLB write drop disable (0) or enable (1).
		2 W_BSP write drop disable (0) or enable (1).
		1 W_VMX_RS write drop disable (0) or enable (1).
		0 W_VMX_BS write drop disable (0) or enable (1).

GDR Write Drop

GDR_WR_DRP - GDR Write Drop		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04020h	

DWord	Bit	Description	
0	31:0	**GDR_WRITE_DROP**	
		Default Value:	00000000h
		Access:	R/W

General Purpose Power Management Performance Idle Hysteresis

GPMPIHYST - General Purpose Power Management Performance Idle Hysteresis		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A070h-0A073h	

DWord	Bit	Description
0	31:24	**Reserved**
		Access: RO
	23:0	**Performance Idle Hysteresis Direction**
		Access: R/W
		Idle intervals must be longer than this value to be considered idle. 0 = 0 usec 1 = 1.28 usec 2 = 2.56 usec 3 = 3.84 usec FF FFFF = 21.474 sec pmcr_idle_hyst[23:0] FYI: 0 means disabled.

GFX_FLSH_CNT

GFX_FLSH_CNT - GFX_FLSH_CNT		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	101008h	
Used to flush Gunit TLB		

DWord	Bit	Description
0	31:1	**RESERVED**
		Default Value: 00000000h
		Access: RO
		Reserved
	0	**GfxFlshCntl**
		Default Value: 0b
		Access: WO
		Access type of this register is WO. A write to this bit flushes the Gfx TLB in GUNIT. The data associated with the write is discarded and a read return all 0s.

GFX Arbiter Client Priority Control

GFX_PRIO_CTRL - GFX Arbiter Client Priority Control		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x880A2D10	
Size (in bits):	32	
Address:	04A00h	

DWord	Bit	Description	
0	31:27	**Read Rstrm Max Reject**	
		Default Value:	10001b
		Access:	R/W
	26:21	**Extra Bits**	
		Default Value:	000000b
		Access:	R/W
	20:18	**sol_gam_priority**	
		Default Value:	010b
		Access:	R/W
		Client Priority Control Bits - Lowest Bit [18] is NOT Used.	
	17:15	**veo_gam_priority**	
		Default Value:	100b
		Access:	R/W
		Client Priority Control Bits - Lowest Bit [15] is NOT Used.	
	14:12	**vfw_gam_priority**	
		Default Value:	010b
		Access:	R/W
		Client Priority Control Bits - Lowest Bit [12] is NOT Used.	
	11:9	**gapc_gam_c_priority**	
		Default Value:	110b
		Access:	R/W
		Client Priority Control Bits - Lowest Bit [9] is NOT Used.	
	8:6	**gapc_gam_z_priority**	
		Default Value:	100b
		Access:	R/W
		Client Priority Control Bits - Lowest Bit [6] is NOT Used.	

GFX_PRIO_CTRL - GFX Arbiter Client Priority Control

	5:3	**gapc_gam_l3_priority**	
		Default Value:	010b
		Access:	R/W
		Client Priority Control Bits - Lowest Bit [3] is NOT Used.	
	2:0	**csrsvf_gam_priority**	
		Default Value:	000b
		Access:	R/W
		Client Priority Control Bits - Lowest Bit [0] is NOT Used.	

GFX Context Element Descriptor (High Part)

GFX_CTX_EDR_H - GFX Context Element Descriptor (High Part)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04404h	

DWord	Bit	Description
0	31:0	**GFX Context Element Descriptor (High Part)**
		<table><tr><td>Default Value:</td><td>00000000h</td></tr><tr><td>Access:</td><td>R/W</td></tr></table>
		Bit[63:32] - Context ID: Context identification number assigned to separate this context from others. Context IDs need to be recycled in such a way that there cannot be two active contexts with the same ID. This is a unique identification number by which a context is identified and referenced.

GFX Context Element Descriptor (Low Part)

GFX_CTX_EDR_L - GFX Context Element Descriptor (Low Part)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000009	
Size (in bits):	32	
Address:	04400h	

DWord	Bit	Description
0	31:0	**GFX Context Element Descriptor (Low Part)** <table><tr><td>Default Value:</td><td>00000009h</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> Bit[31:12] - LRCA: Command Streamer Only. Bit[8] - Privileged Context / GGTT vs PPGTT mode: Differs in legacy vs advanced context modes: In Legacy Context: Defines the page tables to be used. This is how page walker comes to know PPGTT vs GGTT selection for the entire context. 0: Use Global GTT. 1: Use Per-Process GTT. In Advanced Context: Defines the privilege level for the context. 0: User mode context. 1: Supervisor mode context. Bit[5] - Deeper IA coherency Support: In Advanced Context: Defines the level of IA coherency. 0: IA coherency is provided at LLC level for all streams of GPU (i.e. Gen7.5 like mode). 1: IA coherency is provided at L3 level for EU data accesses of GPU. Bit[4] - A and D Support / 32 and 64b Address Support: Differs in legacy vs advanced context modes: In Legacy Context: Defines 32b vs 64b (48b canonical) addressing format: 0: 32b addressing format. 1: 64b (48b canonical) addressing format. In Advanced Context: Defines A and D bit support: 0: A and D bit management in page tables is NOT supported. 1: A and D bit management in page tables is supported. Bit[3] - Context Type: Legacy vs Advanced: Defines the context type 0: Advanced Context: Defines the rest of the advanced capabilities (i.e. OS page table support, fault models). Note that advanced context is not bounded to GPGPU. 1: Legacy Context: Defines the context as legacy mode which is similar to prior generations of Gen8. Note that: Bits [8:4] differs in functions when legacy vs advanced context modes are selected.

GFX_CTX_EDR_L - GFX Context Element Descriptor (Low Part)

		Bit[2] - FR: Command streamer specific.
		Bit[1] - Scheduling Mode: 1: Indicates execlist mode of scheduling. 0: Indicates Ring Buffer mode of scheduling. Bit[0] - Valid: Indicates that element descriptor is valid. If GAM is programmed with an invalid descriptor, it continues but flags an error.

GFX Context Element Descriptor (Low Part)

GFX_CTX_EDR_L - GFX Context Element Descriptor (Low Part)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000009	
Size (in bits):	32	
Address:	04400h	

DWord	Bit	Description
0	31:0	**GFX Context Element Descriptor**

Default Value:	00000009h
Access:	R/W

Bit[31:12] - LRCA:
Command Streamer Only.

Bit[8] - Privileged Context / GGTT vs PPGTT mode: Differs in legacy vs advanced context modes:
In Legacy Context: Defines the page tables to be used. This is how page walker comes to know PPGTT vs GGTT selection for the entire context.
0: Use Global GTT.
1: Use Per-Process GTT.
In Advanced Context: Defines the privilege level for the context.
0: User mode context.
1: Supervisor mode context.

Bit[5] - Deeper IA coherency Support:
In Advanced Context: Defines the level of IA coherency.
0: IA coherency is provided at LLC level for all streams of GPU (i.e. Gen7.5 like mode).
1: IA coherency is provided at L3 level for EU data accesses of GPU.
Bit[4] - A and D Support / 32 and 64b Address Support: Differs in legacy vs advanced context modes:
In Legacy Context: Defines 32b vs 64b (48b canonical) addressing format:
0: 32b addressing format.
1: 64b (48b canonical) addressing format.
In Advanced Context: Defines A and D bit support:
0: A and D bit management in page tables is NOT supported.
1: A and D bit management in page tables is supported.
Bit[3] - Context Type: Legacy vs Advanced:
Defines the context type
0: Advanced Context: Defines the rest of the advanced capabilities (i.e. OS page table support, fault models). Note that advanced context is not bounded to GPGPU.
1: Legacy Context: Defines the context as legacy mode which is similar to prior generations of Gen8.
Note that: Bits [8:4] differs in functions when legacy vs advanced context modes are selected.

GFX_CTX_EDR_L - GFX Context Element Descriptor (Low Part)

		Bit[2] - FR: Command streamer specific.
		Bit[1] - Scheduling Mode: 1: Indicates execlist mode of scheduling. 0: Indicates Ring Buffer mode of scheduling. Bit[0] - Valid: Indicates that element descriptor is valid. If GAM is programmed with an invalid descriptor, it continues but flags an error.

GFX Fault Counter

GFX_FAULT_CNTR - GFX Fault Counter		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	045A0h	
DWord	**Bit**	**Description**
0	31:0	**GFX Fault Counter**
		Default Value: 00000000h
		Access: RO
		This counter only applies to advance context when fault and stream mode is selected.

GFX Fixed Counter

GFX_FIXED_CNTR - GFX Fixed Counter		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	045A4h	

DWord	Bit	Description
0	31:0	**GFX Fixed Counter**
		Default Value: 00000000h
		Access: RO
		This counter only applies to advance context when fault and stream mode is selected.

GFX PDP0/PML4/PASID Descriptor (High Part)

GFX_CTX_PDP0_H - GFX PDP0/PML4/PASID Descriptor (High Part)	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0440Ch

DWord	Bit	Description
0	31:0	**GFX PDP0/PML4/PASID Descriptor (High Part)** <table><tr><td>Default Value:</td><td>00000000h</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> PDP0/PML4/PASID: This register can contain three values which depend on the element descriptor definition. PASID[19:0]: Populated in the first 20bits of the register and selected when Advanced Context flag is set. PML4[38:12]: Pointer to base address of PML4 and selected when Legacy Context flag is set and 64b address support is selected. PDP0[38:12]: Pointer to one of the four page directory pointer (lowest) and defines the first 0-1GB of memory mapping. Note: This is a guest physical address.

GFX PDP0/PML4/PASID Descriptor (Low Part)

GFX_CTX_PDP0_L - GFX PDP0/PML4/PASID Descriptor (Low Part)	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	04408h

DWord	Bit	Description
0	31:0	**GFX PDP0/PML4/PASID Descriptor (Low Part)** <table><tr><td>Default Value:</td><td>00000000h</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> PDP0/PML4/PASID: This register can contain three values which depend on the element descriptor definition. PASID[19:0]: Populated in the first 20 bits of the register and selected when Advanced Context flag is set. PML4[38:12]: Pointer to base address of PML4 and selected when Legacy Context flag is set and 64b address support is selected. PDP0[38:12]: Pointer to one of the four page directory pointer (lowest) and defines the first 0-1GB of memory mapping. Note: This is a guest physical address.

GFX PDP1 Descriptor Register (High Part)

GFX_CTX_PDP1_H - GFX PDP1 Descriptor Register (High Part)	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	04414h

DWord	Bit	Description
0	31:0	**GFX PDP1 Descriptor Register (High Part)** Default Value: 00000000h Access: R/W Pointer to one of the four page directory pointer (lowest+1) and defines the first 1-2GB of memory mapping. Note: This is a guest physical address.

GFX PDP1 Descriptor Register (Low Part)

GFX_CTX_PDP1_L - GFX PDP1 Descriptor Register (Low Part)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04410h	

DWord	Bit	Description
0	31:0	**GFX PDP1 Descriptor Register (Low Part)**
		Default Value:
		Access:
		Pointer to one of the four page directory pointer (lowest+1) and defines the first 1-2GB of memory mapping. Note: This is a guest physical address.

Default Value:	00000000h
Access:	R/W

GFX PDP2 Descriptor Register (High Part)

GFX_CTX_PDP2_H - GFX PDP2 Descriptor Register (High Part)	

Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0441Ch

DWord	Bit	Description
0	31:0	**GFX PDP2 Descriptor Register (High Part)** Default Value: 00000000h Access: R/W Pointer to one of the four page directory pointer (lowest+2) and defines the first 2-3GB of memory mapping. Note: This is a guest physical address.

GFX PDP2 Descriptor Register (Low Part)

	GFX_CTX_PDP2_L - GFX PDP2 Descriptor Register (Low Part)	
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04418h	

DWord	Bit	Description
0	31:0	**GFX PDP2 Descriptor Register (Low Part)** 	Default Value:	00000000h
Access:	R/W	 Pointer to one of the four page directory pointer (lowest+2) and defines the first 2-3GB of memory mapping. Note: This is a guest physical address.

GFX PDP3 Descriptor Register (Low Part)

GFX_CTX_PDP3_L - GFX PDP3 Descriptor Register (Low Part)	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	04420h

DWord	Bit	Description
0	31:0	**GFX PDP3 Descriptor Register (Low Part)**

Default Value:	00000000h
Access:	R/W

Pointer to one of the four page directory pointer (lowest+3) and defines the first 3-4GB of memory mapping.
Note: This is a guest physical address.

GGC

<table>
<tr><th colspan="3">GGC - GGC</th></tr>
<tr><td>Register Space:</td><td colspan="2">PCI: 0/2/0</td></tr>
<tr><td>Project:</td><td colspan="2">CHV, BSW</td></tr>
<tr><td>Source:</td><td colspan="2">PRM</td></tr>
<tr><td>Default Value:</td><td colspan="2">0x00000028</td></tr>
<tr><td>Size (in bits):</td><td colspan="2">32</td></tr>
<tr><td>Address:</td><td colspan="2">00050h</td></tr>
<tr><td colspan="3">GMCH Graphics Control Register.</td></tr>
<tr><th>DWord</th><th>Bit</th><th>Description</th></tr>
<tr><td>0</td><td>31:15</td><td>**RESERVED**
Default Value: 00000h
Access: RO
Reserved</td></tr>
<tr><td></td><td>14</td><td>**VAMEN**
Default Value: 0b
Access: R/W Lock
Enables the use of the iGFX engines for Versatile Acceleration.
1 - iGFX engines are in Versatile Acceleration Mode. Device 2 Class Code is 048000h.
0 - iGFX engines are in iGFX Mode. Device 2 Class Code is 030000h.</td></tr>
<tr><td></td><td>13:10</td><td>**RESERVED**
Default Value: 0h
Access: RO
Reserved</td></tr>
<tr><td></td><td>9:8</td><td>**GGMS**
Default Value: 00b
Access: R/W Lock
GTT Graphics Memory Size (GGMS):
This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics Translation Table. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled.
GSM is assumed to be a contiguous physical DRAM space with DSM, and BIOS needs to allocate a contiguous memory chunk. Hardware will derive the base of GSM from DSM only using the GSM size programmed in the register.
Hardware functionality in case of programming this value to Reserved is not guaranteed.
0h:No Preallocated Memory
1h: 2MB of Preallocated Memory
2h: 4MB of Preallocated Memory
3h: 8MB of Preallocated Memory</td></tr>
</table>

GGC - GGC		
7:3	**GMS**	
	Default Value:	00101b
	Access:	R/W Lock

Graphics Mode Select(GMS):
This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics device in VGA (non-linear) and Native (linear) modes. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled.
Hardware does not clear or set any of these bits automatically based on IGD being disabled/enabled. BIOS Requirement: BIOS must not set this field to 0h if IVD (bit 1 of this register) is 0.

0h = 0MB
1h = 32MB
2h = 64MB
3h = 96MB
4h = 128MB
5h = 160MB
6h = 192MB
7h = 224MB
8h = 256MB
9h = 288MB
Ah = 320MB
Bh = 352MB
Ch = 384MB
Dh = 416MB
Eh = 448MB
Fh = 480MB
10h = 512MB
11h = 8MB
12h = 12MB
13h = 16MB
14h = 20MB
15h = 24MB
16h = 28MB
17h = 36MB
18h = 40MB
19h = 44MB
1Ah = 48MB
1Bh = 52MB
1Ch = 56MB
1Dh = 60MB
1Eh = Reserved
1Fh = Reserved
.....
20h:1024MB (Not supported for CHV, BSW)

GGC - GGC

		..... 30h:1536MB (Not supported for CHV, BSW) ...... 40h:2048MB (Not supported for CHV, BSW) ...... 80h:4096MB (Not supported for CHV, BSW) 81h - FF:Reserved Other = Reserved When GMS != '0 (and VD=0): Address[31:0] is compared with VGA memory range. (The VGA memory range is A_0000h to B_FFFFh.). If there is a match and MSE = 1 and MEMRD or MEMWR, the access will route as a Rmdwvgamemen_cr cycle on the RMbus. If the RMbus returns a hit the GVD will select the command. As well, when 0 the GVD will check if scldown3_address[15:0] is one of the VGA IO register range. (The VGA IO range is 03B0h - 03BBh and 03C0h - 03DFh.) If there is a match and IOSE = 1 and the SCL command is either an IORD or IOWR, the GVD will intiate a (VGA) register cycle on the RMbus. If the RMbus returns a hit the GVD will select the command When GMS == '0 : No address compare will occur against VGA memory range or the VGA IO register range. Also, CC[15:8] is changed to 8'h80 from 8'h00

2	**RESERVED**

Default Value:	0b
Access:	RO

Reserved

1	**VGA_DISABLE**

Default Value:	0b
Access:	R/W Lock

VGA Disable (VD):
0: Enable. Device 2 (IGD) claims VGA memory and IO cycles, the Sub-Class Code within Device 2 Class Code register is 00.
1: Disable. Device 2 (IGD) does not claim VGA cycles (Mem and IO), and the Sub- Class Code field within Device 2 function 0 Class Code register is 80.
BIOS Requirement: BIOS must not set this bit to 0 if the GMS field pre-allocates no memory.
This bit MUST be set to 1 if Device 2 is disabled either via a fuse or fuse override (CAPID0[38] = 1) or via a register (DEVEN[3] = 0).

0	**GGCLCK**

Default Value:	0b
Access:	R/W Lock

When set to 1b, this will lock all the bits in this register.

Global Clear Value Register 0

GLOBAL_CLEAR_VALUE_0 - Global Clear Value Register 0	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	07700h

This register is to be used to program bits 31:0 of the Global clear value to be used for non MSRT render targets. This value will be used by pixel backend hardware in place of the 0/1 clear values, if the "Use Global Clear Value" bit is set.

DWord	Bit	Description
0	31:0	**Global Clear Value 0** Contains bits 31:0 of the global clear value. Clear value will be in native RT format. Clear Value for 8/16/32 bpp RTs will be contained in this format. For the rest it will contain bits 31:0.

Global Clear Value Register 1

GLOBAL_CLEAR_VALUE_1 - Global Clear Value Register 1	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	07704h

This register is to be used to program bits 63:32 of the Global clear value to be used for non MSRT render targets. This value will be used by pixel backend hardware in place of the 0/1 clear values, if the "Use Global Clear Value" bit is set.

DWord	Bit	Description
0	31:0	**Global Clear Value 1** Contains bits 63:32 of the global clear value. Clear value will be in native RT format. This field will contain bits 63:32 of the clear value of 64 bpp and 128 bpp RTs.

Global Clear Value Register 2

GLOBAL_CLEAR_VALUE_2 - Global Clear Value Register 2	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	07708h

This register is to be used to program bits 95:64 of the Global clear value to be used for non MSRT render targets. This value will be used by pixel backend hardware in place of the 0/1 clear values, if the "Use Global Clear Value" bit is set.

DWord	Bit	Description
0	31:0	**Global Clear Value 2** Contains bits 95:64 of the global clear value. Clear value will be in native RT format. Clear value will be in native RT format. This field will contain bits 95:64 of the clear value for 128 bpp RTs.

Global Clear Value Register 3

GLOBAL_CLEAR_VALUE_3 - Global Clear Value Register 3		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	0770Ch	
This register is to be used to program bits 127:96 of the Global clear value to be used for non MSRT render targets. This value will be used by pixel backend hardware in place of the 0/1 clear values, if the "Use Global Clear Value" bit is set.		
DWord	**Bit**	**Description**
0	31:0	**Global Clear Value 3** Contains bits 127:96 of the global clear value. Clear value will be in native RT format. This field will contain bits 127:96 of the clear value for 128 bpp RTs.

Global Invalidation Register

<table>
<tr><td colspan="3" align="center">**GLBLINVL - Global Invalidation Register**</td></tr>
<tr><td>Register Space:</td><td colspan="2">MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td colspan="2">CHV, BSW</td></tr>
<tr><td>Source:</td><td colspan="2">PRM</td></tr>
<tr><td>Default Value:</td><td colspan="2">0x00000000</td></tr>
<tr><td>Size (in bits):</td><td colspan="2">32</td></tr>
<tr><td>Address:</td><td colspan="2">0B404h</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td align="center">**Description**</td></tr>
<tr><td>0</td><td>31:3</td><td>**Reserved**

Access: RO

Reserved.</td></tr>
<tr><td></td><td>2</td><td>**Cross sync read disable**

Access: R/W

lpconf_crs_sync_dis: Cross Sync Read Disable (CSRD).
Cross Sync Read Disable (CSRD): Cross Sync Read Disable: upon a SYNC from HDC, follow with a write to cross SYNC Push and read to the same address.
When set read is disabled.</td></tr>
<tr><td></td><td>1</td><td>**Disables hashing function**

Access: R/W

Disables hashing function (DISHHF):
Disables hashing function to generate bank_id[1:0] for L3$ bank accessing, and forces the use of address[7:6] for bank_id[1:0].0: (default) Hash function enabled to generate L3$ bank IDs.
1: L3$ address[7:6] used as L3$ bank IDs.
lpconf_csr_l3bankidhashdis.
(This bit needs to set corresponding bit lncf_csr_l3bankidhashdis in LNCF.)</td></tr>
<tr><td></td><td>0</td><td>**Reserved**</td></tr>
</table>

Global Microcontroller Hardware Fatal Error Notification

HUC_HW_FATAL_ERROR - Global Microcontroller Hardware Fatal Error Notification

Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	0D598h
Valid Projects:	CHV, BSW

This register is used to HW to log the type of error encountered by HUC during operation. Bits in the register indicate the type of error and HW sets the corresponding bit when a certain type of error occurs. Graphics driver is expected to inspect, respond and clear. To clear a bit, SW must write 1 to the appropriate bit.

DWord	Bit	Description
0	31:18	**Reserved** Format: MBZ
	17	**Reserved** Format: U1
	16	**(INT)Local APIC Enable Error (?)** Format: U1
	15:0	**Reserved** Format: MBZ

Global System Interrupt Routine

EU_GLOBAL_SIP - Global System Interrupt Routine	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32

Address:	0E42Ch

DWord	Bit	Description
0	31:3	**Global SIP** <table><tr><td>Format:</td><td>GraphicsAddress[31:3]</td></tr></table> Specifies the base address for System Interrupt Routine that over-rides the SIP set by the state (STATE_SIP).
	2:1	**Reserved** <table><tr><td>Format:</td><td>MBZ</td></tr></table>
	0	**Global SIP Enable** The bit specifies if the System Routine starts from the Global SIP provided by the DW OR the SIP provided by the state (STATE_SIP) <table><tr><th>Value</th><th>Name</th></tr><tr><td>0</td><td>SIP used is from STATE_EIP</td></tr><tr><td>1</td><td>SIP used is from MMIO register</td></tr></table>

GMADR_LSB - GMADR_LSB

27	**ADMSK256**	
	Default Value:	0b
	Access:	R/W Lock
	256MB Address Mask (ADMSK256): Locked with MSAC.APSZ[0].See MSAC (Dev2, Func 0, offset 62h) for details.	

26:4	**Reserved**	
	Default Value:	000000h
	Access:	RO
	Address Mask (ADM): Hardwired to 0s to indicate at least 128MB address range.	

3	**PREFMEM**	
	Default Value:	1b
	Access:	RO
	Prefetchable Memory (PREFMEM): Hardwired to 1 to enable prefetching.	

2:1	**MEMTYP**	
	Default Value:	10b
	Access:	RO
	Memory Type (MEMTYP): 00: To indicate 32 bit base address 01: Reserved 10: To indicate 64 bit base address 11: Reserved	

0	**Reserved**	
	Default Value:	0b
	Access:	RO
	Memory/IO Space (MIOS): Hardwired to 0 to indicate memory space.	

GMADR_MSB

	GMADR_MSB - GMADR_MSB		
Register Space:	PCI: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0001Ch		

Gfx Aperture location.
GMADR is a Prefetchable range in order to apply USWC attribute (from the processor point of view) to that range. The USWC attribute is used by the processor for write combining.
Accesses to this range will be translated to DRAM Physical memory addresses. Fence registers may be used to sub-divide this range and allow tiled surfaces (determined by fence registers).
The supported sizes are determined by the MSAC register.

DWord	Bit	Description	
0	31:4	**MBA_MSB28**	
		Default Value:	0000000h
		Access:	R/W

Description	Project
Set by the OS, these bits correspond to address signals [63:39]	
Made them spare RW bits.	CHV, BSW

	3:0	**MBA**	
		Default Value:	0h
		Access:	R/W
		Memory Base Address (MBA)Set by the OS, these bits correspond to address signals [35:32]	

GMBC Message Register

<table>
<tr><td colspan="3" align="center">**GMBCMSG - GMBC Message Register**</td></tr>
<tr><td>Register Space:</td><td colspan="2">MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td colspan="2">CHV, BSW</td></tr>
<tr><td>Source:</td><td colspan="2">PRM</td></tr>
<tr><td>Default Value:</td><td colspan="2">0x00000000</td></tr>
<tr><td>Size (in bits):</td><td colspan="2">32</td></tr>
<tr><td>Address:</td><td colspan="2">08500h</td></tr>
<tr><td colspan="3">GMBC Message Register</td></tr>
</table>

DWord	Bit	Description
0	31:12	**RSVD**
		Access: RO
		Reserved
	11	**Context Restore Message**
		Access: R/W
		Context Restore Message 1 = Context Restore Message From CS 0 = Not a Message, GMBC clears when sending ACK to CS.
	10	**MBC BUSY ACK Message**
		Access: R/W
		1 = Busy Ack message from GPMG 0 = IDLE (non-busy) Ack message from GPMG
	9:7	**RSVD**
		Access: RO
		Reserved
	6	**Block Message**
		Access: R/W
		Block Message from GPMG 1 = Block Outbound GAM Traffic and wait for outstanding GAM write requests to be GO'd and reads to return 0 = Unblock Outbound GAM traffic
	5	**RSVD**
		Access: RO
		Reserved
	4	**Arbitration request/release ACK**
		Access: R/W

GMBCMSG - GMBC Message Register

		Global Arb request ACK message: 1 = GPMG ACK of GMBC Global Arb Update Request. 0 = GPMG ACK of GMBC Global Arb Release Request.

	3	**RSVD**
		Access: RO
		Reserved

	2	**Fuse Fetch Message**
		Access: R/W
		Fuse Fetch message: written to 1 by GPMG to indicate GMBC should perform a fuse fetch. Cleared by GMBC when done with the fuse fetch.

	1:0	**RSVD**
		Access: RO
		Reserved

GO Messaging Register for GAMunit

MSG_GO_GAM - GO Messaging Register for GAMunit	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	16
Address:	08028h

Message registers have bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16]. In order to set bit0, for example, the data would be 0x0001_0001. In order to clear bit0, for example, the data would be 0x0001_0000. Note that mask bit is the data bit offset + 16. Message registers are protected from non-GT writes via the Message Channel.
GA* Response to Allow Graphics Cycles to Read/Write from Memory
1'b0 : No gfx cycles allowed to memory <default>
1'b1 : Allow gfx cycles to memory
gpm currently only ever sends the same GO request for all agents; either all is go=0, or all is go=1.

DWord	Bit	Description	
0	15:7	**Reserved**	
		Access:	RO
	6	**GA* Response to Allow Wi-Di Graphics Cycles to Read/Write from Memory**	
		Access:	R/W
		[6] Controls Wi-Di Cycles (winunit)	
	5	**Reserved**	
	4	**GA* Response to Allow Blitter Graphics Cycles to Read/Write from Memory**	
		Access:	R/W
		[4] Controls Blitter Cycles (bcsunit)	
	3	**GA* Response to Allow VEBox Graphics Cycles to Read/Write from Memory**	
		Access:	R/W
		[3] Controls VEBox Cycles (vecsunit)	
	2	**GA* Response to Allow Media1 Graphics Cycles to Read/Write from Memory**	
		Access:	R/W
		[2] Controls Media1 Cycles (vcs1unit)	
	1	**GA* Response to Allow Media0 Graphics Cycles to Read/Write from Memory**	
		Access:	R/W
		[1] Controls Media0 Cycles (vcs0unit)	

MSG_GO_GAM - GO Messaging Register for GAMunit

	0	**GA* Response to Allow Render Graphics Cycles to Read/Write from Memory**	
		Access:	R/W
		[0] Controls Render Cycles (csunit)	

Go Protocol GAM Request

GO_GAM_REQ - Go Protocol GAM Request		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000 CHV, BSW	
Size (in bits):	32	
Address:	040D0h	

DWord	Bit	Description
0	31:16	**Mask Bits**
		Default Value: · 0000h
		Access: · RO
		Reserved.
	15	**GO_PROTOCOL_GAM_REQUEST15**
		Default Value: · 0b
		Project: · CHV, BSW
		Access: · R/W
		Go Protocol Request Reasons: 1'b0: Engine will NOT be resetting. 1'b1: Engine will be resetting (FLR/RC6 Enter or Soft Reset). Preparation for FLR (device) reset (cdevrst_b).
	14	**GO_PROTOCOL_GAM_REQUEST14**
		Default Value: · 0b
		Project: · CHV, BSW
		Access: · R/W
		Go Protocol Request Reasons: 1'b0: Engine will NOT be resetting. 1'b1: Engine will be resetting (FLR/RC6 Enter or Soft Reset). Preparation for Media1 reset (vcs1unit).
	13	**GO_PROTOCOL_GAM_REQUEST13**
		Default Value: · 0b
		Project: · CHV, BSW
		Access: · R/W
		Go Protocol Request Reasons: 1'b0: Engine will NOT be resetting. 1'b1: Engine will be resetting (FLR/RC6 Enter or Soft Reset). Preparation for Wi-Di reset (winunit).

GO_GAM_REQ - Go Protocol GAM Request

12 **GO_PROTOCOL_GAM_REQUEST12**

Default Value:	0b
Project:	CHV, BSW
Access:	R/W

Go Protocol Request Reasons:
1'b0: Engine will NOT be resetting.
1'b1: Engine will be resetting (FLR/RC6 Enter or Soft Reset).
Preparation for P24C reset (gucunit).

11 **GO_PROTOCOL_GAM_REQUEST11**

Default Value:	0b
Project:	CHV, BSW
Access:	R/W

Go Protocol Request Reasons:
1'b0: Engine will NOT be resetting.
1'b1: Engine will be resetting (FLR/RC6 Enter or Soft Reset).
Preparation for Blitter reset (bcsunit).

10 **GO_PROTOCOL_GAM_REQUEST10**

Default Value:	0b
Project:	CHV, BSW
Access:	R/W

Go Protocol Request Reasons:
1'b0: Engine will NOT be resetting.
1'b1: Engine will be resetting (FLR/RC6 Enter or Soft Reset).
Preparation for VEBox reset (vecsunit).

9 **GO_PROTOCOL_GAM_REQUEST9**

Default Value:	0b
Project:	CHV, BSW
Access:	R/W

Go Protocol Request Reasons:
1'b0: Engine will NOT be resetting.
1'b1: Engine will be resetting (FLR/RC6 Enter or Soft Reset).
Preparation for Media0 reset (vcs0unit).

8 **GO_PROTOCOL_GAM_REQUEST8**

Default Value:	0b
Project:	CHV, BSW

GO_GAM_REQ - Go Protocol GAM Request

		Access:	R/W

Go Protocol Request Reasons:
1'b0: Engine will NOT be resetting.
1'b1: Engine will be resetting (FLR/RC6 Enter or Soft Reset).
Preparation for Render reset (csunit).

| | 7 | **Reserved** |

| | 6 | **GO_PROTOCOL_GAM_REQUEST6** |

| | | Default Value: | 0b |
| | | Access: | R/W |

GPM to GAM Go Protocol Request.
0: No graphic cycles allowed to memory (default).
1: Allow graphic cycles to memory.
Controls Wi-Di Cycles (winunit).
GPM currently only ever sends the same GO request for all agents; either all is go=0, or all is go=1.

| | 5 | **Reserved** |

| | 4 | **GO_PROTOCOL_GAM_REQUEST4** |

| | | Default Value: | 0b |
| | | Access: | R/W |

GPM to GAM Go Protocol Request.
0: No graphic cycles allowed to memory (default).
1: Allow graphic cycles to memory.
Controls Blitter Cycles (bcsunit).
GPM currently only ever sends the same GO request for all agents; either all is go=0, or all is go=1.

| | 3 | **GO_PROTOCOL_GAM_REQUEST3** |

| | | Default Value: | 0b |
| | | Access: | R/W |

GPM to GAM Go Protocol Request.
0: No graphic cycles allowed to memory (default).
1: Allow graphic cycles to memory.
Controls VEBox Cycles (vecsunit).
GPM currently only ever sends the same GO request for all agents; either all is go=0, or all is go=1.

| | 2 | **GO_PROTOCOL_GAM_REQUEST2** |

| | | Default Value: | 0b |
| | | Access: | R/W |

GPM to GAM Go Protocol Request.

GO_GAM_REQ - Go Protocol GAM Request

		0: No graphic cycles allowed to memory (default). 1: Allow graphic cycles to memory. Controls Media1 Cycles (vcs1unit). GPM currently only ever sends the same GO request for all agents; either all is go=0, or all is go=1.	
	1	**GO_PROTOCOL_GAM_REQUEST1**	
		Default Value:	0b
		Access:	R/W
		GPM to GAM Go Protocol Request. 0: No graphic cycles allowed to memory (default). 1: Allow graphic cycles to memory. Controls Media0 Cycles (vcs0unit). GPM currently only ever sends the same GO request for all agents; either all is go=0, or all is go=1.	
	0	**GO_PROTOCOL_GAM_REQUEST0**	
		Default Value:	0b
		Access:	R/W
		GPM to GAM Go Protocol Request. 0: No graphic cycles allowed to memory (default). 1: Allow graphic cycles to memory. Controls Render Cycles (csunit). GPM currently only ever sends the same GO request for all agents; either all is go=0, or all is go=1.	

GPA to HPA Translation Request

GPA2HPAR - GPA to HPA Translation Request		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0420Ch	

DWord	Bit	Description
0	31:16	**Mask Bits**

Default Value:	0000h
Access:	RO

Mask Bits act as Write Enables for the bits[15:0] of this register.

	15	**GPA to HPA Translation Request 15**

Default Value:	0b
Access:	R/W

For Future Use.
This bit is self clear.

	14	**GPA to HPA Translation Request 14**

Default Value:	0b
Access:	R/W

For Future Use.
This bit is self clear.

	13	**GPA to HPA Translation Request 13**

Default Value:	0b
Access:	R/W

For Future Use.
This bit is self clear.

	12	**GPA to HPA Translation Request 12**

Default Value:	0b
Access:	R/W

For Future Use.
This bit is self clear.

	11	**GPA to HPA Translation Request 11**

Default Value:	0b
Access:	R/W

For Future Use.

GPA2HPAR - GPA to HPA Translation Request

		This bit is self clear.	
	10	**GPA to HPA Translation Request 10**	
		Default Value:	0b
		Access:	R/W
		For Future Use. This bit is self clear.	
	9	**GPA to HPA Translation Request 9**	
		Default Value:	0b
		Access:	R/W
		For Future Use. This bit is self clear.	
	8	**GPA to HPA Translation Request 8**	
		Default Value:	0b
		Access:	R/W
		For Future Use. This bit is self clear.	
	7	**GPA to HPA Translation Request 7**	
		Default Value:	0b
		Access:	R/W
		For Future Use. This bit is self clear.	
	6	**GPA to HPA Translation Request 6**	
		Default Value:	0b
		Access:	R/W
		For Future Use. This bit is self clear.	
	5	**GPA to HPA Translation Request 5**	
		Default Value:	0b
		Access:	R/W
		For Future Use. This bit is self clear.	
	4	**GPA to HPA Translation Request 4**	
		Default Value:	0b
		Access:	R/W
		For Future Use. This bit is self clear.	
	3	**GPA to HPA Translation Request 3**	
		Default Value:	0b
		Access:	R/W

GPA2HPAR - GPA to HPA Translation Request

		For Future Use. This bit is self clear.	
	2	**GPA to HPA Translation Request 2**	
		Default Value:	0b
		Access:	R/W
		Bit[2]: A request for GPA to HPA translation. Note that GPA register should have been written prior to sending the message for the translation. Mask bit[18] needs to be enabled to program the register. This bit is self clear.	
	1	**GPA to HPA Translation Request 1**	
		Default Value:	0b
		Access:	R/W
		For Future Use. This bit is self clear.	
	0	**GPA to HPA Translation Request 0**	
		Default Value:	0b
		Access:	R/W
		For Future Use. This bit is self clear.	

GPA value for GPA to HPA Translation

GPA2HPAV - GPA value for GPA to HPA Translation		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04210h	

DWord	Bit	Description
0	31:0	**GPA value for GPA to HPA Translation**
		Default Value: · 00000000h
		Access: · R/W
		The GPA value of the page that requires the GPA=>HPA translation bits[39:12] map to [28:1] of the register.

GPGPU Context Restore Request To TDL

GPGPU_CTX_RESTORE - GPGPU Context Restore Request To TDL	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Access:	WO
Size (in bits):	32
Address:	0E4CCh
Name:	GPGPU Context Restore Request To TDL Slice 0 SubSlice 0
ShortName:	GPGPU_CTX_RESTORE_S0_SS0
Valid Projects:	CHV, BSW
Address:	0E5CCh
Name:	GPGPU Context Restore Request To TDL Slice 0 SubSlice 1
ShortName:	GPGPU_CTX_RESTORE_S0_SS1
Valid Projects:	CHV, BSW
Address:	0E6CCh
Name:	GPGPU Context Restore Request To TDL Slice 0 SubSlice 2
ShortName:	GPGPU_CTX_RESTORE_S0_SS2
Valid Projects:	CHV, BSW
Address:	0E4DCh
Name:	GPGPU Context Restore Request To TDL Slice 1 SubSlice 0
ShortName:	GPGPU_CTX_RESTORE_S1_SS0
Valid Projects:	CHV, BSW
Address:	0E5DCh
Name:	GPGPU Context Restore Request To TDL Slice 1 SubSlice 1
ShortName:	GPGPU_CTX_RESTORE_S1_SS1
Valid Projects:	CHV, BSW
Address:	0E6DCh
Name:	GPGPU Context Restore Request To TDL Slice 1 SubSlice 2
ShortName:	GPGPU_CTX_RESTORE_S1_SS2
Valid Projects:	CHV, BSW
Address:	0E4ECh
Name:	GPGPU Context Restore Request To TDL Slice 2 SubSlice 0
ShortName:	GPGPU_CTX_RESTORE_S2_SS0
Valid Projects:	CHV, BSW

GPGPU_CTX_RESTORE - GPGPU Context Restore Request To TDL

Address:	0E5ECh
Name:	GPGPU Context Restore Request To TDL Slice 2 SubSlice 1
ShortName:	GPGPU_CTX_RESTORE_S2_SS1
Valid Projects:	CHV, BSW

Address:	0E6ECh
Name:	GPGPU Context Restore Request To TDL Slice 2 SubSlice 2
ShortName:	GPGPU_CTX_RESTORE_S2_SS2
Valid Projects:	CHV, BSW

DWord	Bit	Description	
0	31:0	**Reserved**	
		Format:	MBZ

GPGPU Context Save Request To TDL

GPGPU_CTX_SAVE - GPGPU Context Save Request To TDL		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Access:	WO	
Size (in bits):	32	
Address:	0E4D8h	
Valid Projects:	CHV, BSW	

DWord	Bit	Description	
0	31:0	**Reserved**	
		Format:	MBZ

GPGPU Dispatch Dimension X

GPGPU_DISPATCHDIMX - GPGPU Dispatch Dimension X	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02500h

DWord	Bit	Description
0	31:0	**Dispatch Dimension X**

Format:	U32

The number of thread groups to be dispatched in the X dimension (max x + 1).

Value	Name	Project
0, FFFFFFFFh		CHV, BSW

GPGPU Dispatch Dimension Y

<table>
<tr>
<td colspan="3" align="center">**GPGPU_DISPATCHDIMY - GPGPU Dispatch Dimension Y**</td>
</tr>
<tr>
<td colspan="3">Register Space: MMIO: 0/2/0</td>
</tr>
<tr>
<td colspan="3">Project: CHV, BSW</td>
</tr>
<tr>
<td colspan="3">Source: RenderCS</td>
</tr>
<tr>
<td colspan="3">Default Value: 0x00000000</td>
</tr>
<tr>
<td colspan="3">Access: R/W</td>
</tr>
<tr>
<td colspan="3">Size (in bits):   32</td>
</tr>
<tr>
<td colspan="3">Address: 02504h</td>
</tr>
</table>

DWord	Bit	Description
0	31:0	**Dispatch Dimension Y**

Format:	U32

The number of thread groups to be dispatched in the Y dimension (max y + 1

Value	Name	Project
0, FFFFFFFFh		CHV, BSW

GPGPU Dispatch Dimension Z

GPGPU_DISPATCHDIMZ - GPGPU Dispatch Dimension Z		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	02508h	

DWord	Bit	Description
0	31:0	**Dispatch Dimension Z**

<table>
<tr><td>Format:</td><td colspan="2">U32</td></tr>
<tr><td colspan="3">The number of thread groups to be dispatched in the Zdimension (max Z + 1)</td></tr>
<tr><th>Value</th><th>Name</th><th>Project</th></tr>
<tr><td>0, FFFFFFFFh</td><td></td><td>CHV, BSW</td></tr>
</table>

GPU_Ticks_Counter

GPU_TICKS - GPU_Ticks_Counter	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02910h
Valid Projects:	CHV, BSW

 Reading this register returns the live value of the GPU ticks counter that is sampled and included in the performance counter report header.

DWord	Bit	Description
0	31:0	**Considerations**

Format:	U32

 This 32-bit field returns bits 31:0 of the GPU tick counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Graphics Device Reset Control

GDRST - Graphics Device Reset Control		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0941Ch	
Graphics Device Reset Control Registers			
DWord	**Bit**	**Description**	
0	31:7	**Reserved**	
		Access:	RO
		Reserved	
	6	**Initiate Graphics WIDI soft reset**	
		Access:	R/W Set
		Graphics WIDI Soft-Reset Control (cwrst_b): '1' : Initiate a graphics WIDI domain reset. - Cleared by CP once the reset is complete '0' : N/A - Once set, clearing of this bit has no effect on CP. Only CP can reset this bit. Note: This is a non-posted register.	
		Programming Notes	**Project**
		WDBOX is defeatured for CHV, BSW, therefore, this bit should not be used and must be zero at all times.	CHV, BSW
	5	**Reserved**	
	4	**Initiate Graphics Vebox Soft Reset**	
		Access:	R/W Set
		Graphics VEbox Soft-Reset Control: '1' : Initiate a graphics Vebox domain reset. - Cleared by CP once the reset is complete '0' : N/A - Once set, clearing of this bit has no effect on CP. Only CP can reset this bit. Note: This is a non-posted register.	
	3	**Initiate Graphics Blitter Soft Reset**	
		Access:	R/W Set
		Graphics Blitter Soft-Reset Control: '1' : Initiate a graphics blitter domain reset. - Cleared by CP once the reset is complete '0' : N/A	

GDRST - Graphics Device Reset Control

		- Once set, clearing of this bit has no effect on CP. Only CP can reset this bit. Note: This is a non-posted register.
	2	**Initiate Graphics Media Soft Reset**
		Access: R/W Set
		Graphics Media Soft-Reset Control: '1' : Initiate a graphics media 0 domain reset. - Cleared by CP once the reset is complete '0' : N/A - Once set, clearing of this bit has no effect on CP. Only CP can reset this bit. Note: This is a non-posted register.
	1	**Initiate Graphics Render Soft Reset**
		Access: R/W Set
		Graphics Render Soft-Reset Control: '1' : Initiate a graphics render domain reset. - Cleared by CP once the reset is complete '0' : N/A - Once set, clearing of this bit has no effect on CP. Only CP can reset this bit. Note: This is a non-posted register.
	0	**Initiate Graphics Full Soft Reset**
		Access: R/W Set
		Graphics Full Soft-Reset Control: '1' : Initiate a full graphics reset (i.e., graphics render, media, and blitter reset). - Cleared by CP once the reset is complete '0' : N/A - Once set, clearing of this bit has no effect on CP. Only CP can reset this bit. Note: This is a non-posted register.

Graphics Mode Register

GFX_MODE - Graphics Mode Register	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00000000 [CHV:B, CHV:C, CHV:K]
	0x00000800 [CHV:A]
Size (in bits):	32
Trusted Type:	1
Address:	0229Ch
Valid Projects:	CHV, BSW
Address:	1229Ch-1229Fh
Name:	Graphics Mode Register
ShortName:	GFX_MODE_VCSUNIT0
Address:	1A29Ch-1A29Fh
Name:	Graphics Mode Register
ShortName:	GFX_MODE_VECSUNIT
Address:	1C29Ch-1C29Fh
Name:	Graphics Mode Register
ShortName:	GFX_MODE_VCSUNIT1
Address:	2229Ch-2229Fh
Name:	Graphics Mode Register
ShortName:	GFX_MODE_BCSUNIT

Description
This register contains a control bit for the new execlist and 2-level PPGTT functions.
DefaultValue = 00002800h

DWord	Bit	Description
0	31:16	**Mask Bits** Format: Mask[15:0] Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)
	15	**Execlist Enable** Mask: MMIO#31 When set, software can utilize the execlist registers to load a context into hardware. MI_SET_CONTEXT and MI_ARB_CHECK commands will be converted to NOOP if parsed. When this bit is clear, the Execlist mechanism cannot be used. The context must be loaded via MI_SET_CONTEXT and the ring must be loaded via MMIO access.

GFX_MODE - Graphics Mode Register

Programming Notes
This bit is *not* intended to be changed dynamically. Changing the value of this bit while rendering is in progress will have UNDEFINED results. This bit should be changed only <u>after a full reset</u> and <u>before</u> submitting *any* commands to the device.

14	**Reserved**	
	Project:	CHV, BSW

13	**Flush TLB invalidation Mode**	
	Project:	CHV, BSW
	Format:	U1

This field controls the invalidation if the TLB cache inside the hardware. When enabled this bit limits the invalidation of the TLB only to batch buffer boundaries, to pipe_control commands which have the TLB invalidation bit set and sync flushes. If disabled, the TLB caches are flushed for every full flush of the pipeline.

12	**Reserved**	
	Project:	All
	Format:	MBZ

11	**Reserved**	
	Project:	CHV, BSW
	Format:	MBZ

11	**Replay Mode**	
	Project:	CHV, BSW
	Format:	U1 Context Switch Granularity

This field controls the granularity of the replay mechanism when coming back into a previously preempted context.

Value	Name	Description
1h	Object Level Preemption **[Default]**	Object Level. Preemption is done on an Object Level Boundary in VF. Objects send down by VF are completely rendered. Pipeline is flushed before switching to the next context. On resubmission of the context VF starts parsing form the object where it got preempted last time.
0h	mid-cmdbuffer preemption	Drawcall Level. Pipeline is flushed before switching to the next context. Commands parsed are committed to completing before a context switch.

Programming Notes
A fixed function pipe flush is required before modifying this field.
The replay mode must be set to 0.

10	**Reserved**	
	Project:	All

GFX_MODE - Graphics Mode Register

		Format:		MBZ	

	9	**Per-Process GTT Enable**			
		Project:		CHV, BSW	
		Format:		Enabled	

Per-Process GTT Enable

Value	Name	Description
0h	PPGTT Disable **[Default]**	When clear, the Global GTT will be used to translate memory access from designated commands and for commands that select the PPGTT as their translation space.
1h	PPGTT Enable	When set, the PPGTT will be used to translate memory access from designated commands and for commands that select the PPGTT as their translation space.

Programming Notes
This bit is used for enabling PPGTT access in Ring Buffer mode of scheduling. Privilege field in context descriptor states the same in Execlist Mode of scheduling. This field should be set before programming PDP0/1/2/3 registers in order to set the PPGTT translation of memory access.
Programming this bit doesn't enable or disable the PPGTT translation of memory access immediately; the change comes in to affect only when the Page Directory registers are programmed. Programming this bit must be followed by programming Page Directory Registers in order to enable or disable the PPGTT translation of memory access.

	8	**Reserved**			
		Project:		CHV, BSW	

	7	**64Bit Virtual Addressing Enable**			
		Project:		CHV, BSW	
		Format:		Enabled	

Per-Process GTT Enable

Value	Name	Description
0h	64Bit Virtual Addressing Disable **[Default]**	When clear indicates GFX operating in 32bit Virtual Addressing for PPGTT based memory access.

Programming Notes
This bit is only valid when PPGTT is enabled in ring buffer mode of scheduling. Context Descriptor has a similar bit to control 64bit virtual addressing in execlist mode of scheduling. Whether this field is set or clear virtual addresses translated through GGTT are always 32Bit. This field should be programmed before enabling PPGTT access. When this field is not set or for GGTT virtual addresses, Graphics Address [47:32] field of any commands or register exercised by SW should be programmed to 0x0.
64 Bit Virtual Addressing is not supported on CHV, BSW and must not be set.

Command

GS Domain Clock Gate Control Register

GSCKGCTL - GS Domain Clock Gate Control Register	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	09028h
Gunit Graphics Slow Clock Domain Clock Gating Control Register	

DWord	Bit	Description
0	31:29	**RSVD** Access: RO RSVD
	28:24	**GMBC Clock Gate IDLE Count** Access: R/W GMBC IDLE Timer Count Value - bits[27:24] 0 = GMBC Idle timer disabled 1-15 = After GMBC indicates idle, wait this many clocks before gating. Bit [28] is additional Reserved R/W
	23:20	**GPMG Clock Gate IDLE Counter** Access: R/W GPMGi dle timer. GPMG uses this as a its idle counter pre-load value for clock gating 0 = Idle timer disabled 1 - 15 = After unit indicates its idle, wait this many clocks before gating
	19:16	**GSIDLECNT** Access: R/W Generic GUNIT GSCLK domain idle timer. GUNIT GS fubs (other than GMBC) use this as a counter pre-load value 0 = Idle timer disabled 1 - 15 = After a unit indicates idle, wait this many clocks before gating.
	15:13	**RSVD** Access: RO Reserved
	12	**GDTCKGEN** Access: R/W

GSCKGCTL - GS Domain Clock Gate Control Register

		GDT Clock Gating Enable. 0 = Disable clock gating. 1 = Enable clock gating.	
	11	**GMBCPCKDIS**	
		Access:	R/W
		GMBC Performance Monitor Clock Gating Disable 0 = Enable clock gating 1 = Disable clock gating	
	10	**GMBCCKGDIS**	
		Access:	R/W
		GMBC Clock Gating Disable: controls non-performance monitoring related clocks in the GMBC 0 = Enable clock gating 1 = Disable clock gating	
	9	**GPMGCKDIS**	
		Access:	R/W
		GPMG Clock Gating Disable 0 = Enable clock gating 1 = Disable clock gating	
	8	**G3DRDCKGDIS**	
		Access:	R/W
		G3D Read Return Clock Gating Disable 0 = Enable clock gating 1 = Disable clock gating	
	7	**G3DOUTCKGDIS**	
		Access:	R/W
		G3D Outbound Clock Gating Disable: controls clocks associated with outbound requests. 0 = Enable clock gating 1 = Disable clock gating	
	6	**GMCFGCKGDIS**	
		Access:	R/W
		GMCFG Clock Gating Disable 0 = Enable clock gating 1 = Disable clock gating	
	5	**GKEYSCKGDIS**	
		Access:	R/W

GSCKGCTL - GS Domain Clock Gate Control Register

		GKEYS Clock Gating Disable 0 = Enable clock gating 1 = Disable clock gating	
	4	**GCCBGSGDIS**	
		Access:	R/W
		GCCBGS Clock Gating Disable 0 = Enable clock gating 1 = Disable clock gating	
	3:0	**RSVD**	
		Access:	RO
		Reserved	

GS Invocation Counter

<table>
<tr><td colspan="2" align="center">**GS_INVOCATION_COUNT - GS Invocation Counter**</td></tr>
<tr><td>Register Space:</td><td>MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td>CHV, BSW</td></tr>
<tr><td>Source:</td><td>RenderCS</td></tr>
<tr><td>Default Value:</td><td>0x00000000, 0x00000000</td></tr>
<tr><td>Access:</td><td>R/W</td></tr>
<tr><td>Size (in bits):</td><td>64</td></tr>
<tr><td>Trusted Type:</td><td>1</td></tr>
<tr><td>Address:</td><td>02328h</td></tr>
<tr><td colspan="2">This register stores the number of objects that are part of geometry shader threads. This register is part of the context save and restore.</td></tr>
</table>

DWord	Bit	Description
0	63:32	**GS Invocation Count UDW** Number of objects that are dispatched as a geometry shader threads invoked by the GS stage. Updated only when **Statistics Enable** is set in GS_STATE (see the Geometry Shader Chapter in the 3D Volume.)
	31:0	**GS Invocation Count LDW** Number of objects that are dispatched as a geometry shader threads invoked by the GS stage. Updated only when **Statistics Enable** is set in GS_STATE (see the Geometry Shader Chapter in the 3D Volume.)

GS Primitives Counter

GS_PRIMITIVES_COUNT - GS Primitives Counter	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Trusted Type:	1
Address:	02330h

This register reflects the total number of primitives that have been output by the Geometry Shader stage. This register is part of the context save and restore.

DWord	Bit	Description
0	63:32	**GS Primitives Count UDW** Total number of primitives output by the geometry stage. Updated only when Statistics Enable is set in GS_STATE (see the Geometry Shader Chapter in the 3D Volume.)
	31:0	**GS Primitives Count LDW** Total number of primitives output by the geometry stage. Updated only when Statistics Enable is set in GS_STATE (see the Geometry Shader Chapter in the 3D Volume.)

GT_CR_POWER_METER_CTRL

PWRMTRLK - GT_CR_POWER_METER_CTRL		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A248h-0A24Bh	

DWord	Bit	Description
0	31	**Power Meter and Push Bus Control Lock** Access: R/W Lock Controls whether power meter weights and other push bus control registers are writeable. 0 : Power Meter weights and control registers are writeable. 1: Writes to Power Meter weights and control registers are blocked. Lock bit cannot be cleared without cold reset.
	30:7	**Reserved** Access: RO
	6	**GSclk Domain GTI Baseline Energy Count Enable** Access: R/W Lock Controls whether the energy counter for the GTI power well, counting in the GSclk domain, is running or not. 0: Accumulator in PM is disabled 1: Accumulator in PM is enabled
	5	**Reserved** Access: RO
	4	**Render Power Meter Counter Enable** Access: R/W Lock Render Power Meter Enable : Controls whether power meter is running or not. 0: All Power meter counters/accumulators in PM are disabled and held at zero. 1: All power meter counters/accumulators in PM are enabled. Note that this bit does not affect intermediate accumulation/overflow logic elsewhere in the Gfx engine.
	3	**Media Power Meter Counter Enable** Access: R/W Lock Media Power Meter Enable :

PWRMTRLK - GT_CR_POWER_METER_CTRL

		Controls whether power meter is running or not. 0: All Power meter counters/accumulators in PM are disabled and held at zero. 1: All power meter counters/accumulators in PM are enabled. Note that this bit does not affect intermediate accumulation/overflow logic elsewhere in the Gfx engine.	
	2:0	**Reserved**	
		Access:	RO

GTFIFOCTL

<table>
<tr><td colspan="3" align="center">**GTFIFOCTL - GTFIFOCTL**</td></tr>
<tr><td colspan="3">
Register Space: MMIO: 0/2/0

Project: CHV, BSW

Source: PRM

Default Value: 0x00000000

Size (in bits):   32
</td></tr>
<tr><td colspan="3">Address: 120008h</td></tr>
<tr><td colspan="3">GT FIFO Control.</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td>**Description**</td></tr>
<tr><td>0</td><td>31</td><td>

GT_IOSFSB_READ_POLICY

Default Value:	0b
Access:	R/W

The SEC must first write this register bit before attempting Gunit register context reads.
This is identified usage model requiring IOSF SB reads. Note : For CHV, BSW, Punit has it's own IOSF SB P interface.
0 (Default) : Abort IOSF SB reads. Only Kf1, Kf1 status, Punit Gkey debug, and Punit timestamp debug related IOSF SB reads are allowed.
1 : Allow IOSF SB reads.

</td></tr>
<tr><td></td><td>30:16</td><td>

SPARE15

Default Value:	0000h
Access:	RO

Reserved

</td></tr>
<tr><td></td><td>15</td><td>

GT_FIFO_SB_POLICY

Default Value:	0b
Access:	R/W

GT_WakeFIFO IOSF SB Policy register
0 (default) : If WakeFIFO threshold hit and dedicated IOSF SB buffering is full, stall IOSF SB accesses targeting WakeFIFO.
1 : If WakeFIFO threshold is hit AND dedicated IOSF SB buffering is full : a. Drop IOSF SB write requests to WakeFIFO b. IOSF SB reads targeting WakeFIFO return 1s.
Evaluated for the request at the head of the IA_WakeFIFO.

</td></tr>
<tr><td></td><td>14</td><td>

GT_FIFO_BLOB_POLICY

Default Value:	0b
Access:	R/W

</td></tr>
<tr><td></td><td>13</td><td>

GT_FIFO_PRI_POLICY

Default Value:	0b

</td></tr>
</table>

GTFIFOCTL - GTFIFOCTL

		Access:	R/W

GT_WakeFIFO IOSF Primary Policy register.
0 (Default) : If WakeFIFO threshold hit, stall IOSF Primary accesses targeting WakeFIFO.
1 : If WakeFIFO threshold is hit :
a. Drop IOSF Primary writes to WakeFIFO
b. IOSF Primary reads targeting WakeFIFO return 1s.
Don't hang the system, but device 2 may hang.

12	**Block all Policy**	
	Default Value:	0b
	Access:	R/W

BlockALL policy register applies to both HW FIFO and IA GT FIFO. This bit only applies when the GPM BlockALL indication is asserted.
GPM BlockALL indication can assert for : A) CPD and B) for a period of time during RC6 entry.
0 (default) : Allow register collapsing and stall request at the head if it is not collapse-able.
1 : Stall request at the head.

11	**RC6_POLICY**	
	Default Value:	0b
	Access:	R/W

RC6 policy register applies to both HW FIFO and IA GT FIFO. This bit only applies :
- when BlockALL is not asserted
- within RC6, and
- ONLY when AllowWake register (13_0090h[0]=1).
0 (default) : Allow register collapsing and drop request at the head if it is not collapsible.
1 : Stall request at the head if within RC6.
Note: All hardware initiated requests should be collapsible.
Note: Starting with Gen8 Gfx, the driver is required to ensure the targeted power well is alive before initiating an access outside shadow register space.

10:9	**SPARE2**	
	Default Value:	00b
	Access:	R/W

spare bit

8	**Reserved**	
	Default Value:	0b
	Access:	R/W

7:0	**SPARE8**	
	Default Value:	00h

GTFIFOCTL - GTFIFOCTL

		Access:	RO
		Reserved	

GT Function Level Reset Control Message

FLRCTLMSG - GT Function Level Reset Control Message		

Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	

Address:	08100h	

GT FLR Control Register

DWord	Bit	Description
0	31:16	**Message Mask**
		Access: RO
		Message Mask In order to write to bits 15:0, the corresponding message mask bits must be written. For example, for bit 14 to be set, bit 30 needs to be 1 : 40004000
	15:1	**Reserved**
		Access: RO
		Reserved
	0	**Reserved**
		Access: RO
		Reserved R/W: FLR is not supported on CHV, BSW.

GT INTERRUPT 0 ENABLE REGISTER

GT_INTERRUPT0_IER - GT INTERRUPT 0 ENABLE REGISTER	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	4430Ch-4430Fh

This table indicates which events are mapped to each bit of the GT Interrupt 0 registers. Bits 15:0 are used for Render CS. Bits 31:16 are used for Blitter CS.
The IER enabled Render Interrupt IIR (sticky) bits are ORed together to generate the Render Interrupts Pending bit in the Master Interrupt Control register.
The IER enabled Blitter Interrupt IIR (sticky) bits are ORed together to generate the Blitter Interrupts Pending bit in the Master Interrupt Control register.

DWord	Bit	Description	
0	31	**UNUSED0**	
		Access:	R/W
	30	**UNUSED1**	
		Access:	R/W
	29	**UNUSED2**	
		Access:	R/W
	28	**UNUSED3**	
		Access:	R/W
	27	**BCS_WAIT_ON_SEMAPHORE**	
		Access:	R/W
		BCS wait on semaphore	
	26	**UNUSED4**	
		Access:	R/W
	25	**UNUSED5**	
		Access:	R/W
	24	**BCS_CTX_SWITCH_INTERRUPT**	
		Access:	R/W
		BCS context switch interrupt	
	23	**UNUSED6**	
		Access:	R/W

GT_INTERRUPT0_IER - GT INTERRUPT 0 ENABLE REGISTER

22	**UNUSED7**		
	Access:		R/W
21	**UNUSED8**		
	Access:		R/W
20	**BCS_MI_FLUSH_DWNOTIFY**		
	Access:		R/W
	BCS MI flush DW notify		
19	**BCS_ERROR_INTERRUPT**		
	Access:		R/W
	BCS error interrupt		
18	**UNUSED9**		
	Access:		R/W
17	**UNUSED10**		
	Access:		R/W
16	**BCS_MI_USER_INTERRUPT**		
	Access:		R/W
	BCS MI user interrupt		
15	**UNUSED11**		
	Access:		R/W
14	**UNUSED12**		
	Access:		R/W
13	**UNUSED13**		
	Access:		R/W
12	**UNUSED14**		
	Access:		R/W
11	**CS_WAIT_ON_SEMAPHORE**		
	Access:		R/W
	CS wait on semaphore		
10	**CS_L3_COUNTER_SAVE**		
	Access:		R/W
	CS L3 counter save		
9	**UNUSED15**		
	Access:		R/W

GT_INTERRUPT0_IER - GT INTERRUPT 0 ENABLE REGISTER

	8	**CS_CTX_SWITCH_INTERRUPT**	
		Access:	R/W
		CS context switch interrupt	

	7	**PAGE_FAULT_ERROR**	
		Access:	R/W
		this interrupt is for handling legacy page fault interface for all command streamer (BCS, VCS, RCS, VECS). when fault repair mode is enabled, interrupt mask register value is not looked at to generate interrupt due to page fault. please refer to 'page fault support' section for more details.	

	6	**CS_WATCHDOG_COUNTER_EXPIRED**	
		Access:	R/W
		CS watchdog counter expired	

	5	**L3PARITYERROR**	
		Access:	R/W
		L3 parity error	

	4	**CS_PIPE_CONTROL_NOTIFY**	
		Access:	R/W
		CS pipe control notify	

	3	**CS_ERROR_INTERRUPT**	
		Access:	R/W
		CS error interrupt	

	2	**UNUSED17**	
		Access:	R/W

	1	**Reserved**	

	0	**CS_MI_USER_INTERRUPT**	
		Access:	R/W
		CS context switch interrupt	

GT INTERRUPT 0 IDENTITY REGISTER

GT_INTERRUPT0_IIR - GT INTERRUPT 0 IDENTITY REGISTER	

Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32

Address:	44308h-4430Bh

This table indicates which events are mapped to each bit of the GT Interrupt 0 registers. Bits 15:0 are used for Render CS. Bits 31:16 are used for Blitter CS.
The IER enabled Render Interrupt IIR (sticky) bits are ORed together to generate the Render Interrupts Pending bit in the Master Interrupt Control register.
The IER enabled Blitter Interrupt IIR (sticky) bits are ORed together to generate the Blitter Interrupts Pending bit in the Master Interrupt Control register.

DWord	Bit	Description	
0	31	**UNUSED0**	
		Access:	R/W One Clear
	30	**UNUSED1**	
		Access:	R/W One Clear
	29	**UNUSED2**	
		Access:	R/W One Clear
	28	**UNUSED3**	
		Access:	R/W One Clear
	27	**BCS_WAIT_ON_SEMAPHORE**	
		Access:	R/W One Clear
		BCS wait on semaphore	
	26	**UNUSED4**	
		Access:	R/W One Clear
	25	**UNUSED5**	
		Access:	R/W One Clear
	24	**BCS_CTX_SWITCH_INTERRUPT**	
		Access:	R/W One Clear
		BCS context switch interrupt	
	23	**UNUSED6**	
		Access:	R/W One Clear

GT_INTERRUPT0_IIR - GT INTERRUPT 0 IDENTITY REGISTER

	22	**UNUSED7**	
		Access:	R/W One Clear
	21	**UNUSED8**	
		Access:	R/W One Clear
	20	**BCS_MI_FLUSH_DWNOTIFY**	
		Access:	R/W One Clear
		BCS MI flush DW notify	
	19	**BCS_ERROR_INTERRUPT**	
		Access:	R/W One Clear
		BCS error interrupt	
	18	**UNUSED9**	
		Access:	R/W One Clear
	17	**UNUSED10**	
		Access:	R/W One Clear
	16	**BCS_MI_USER_INTERRUPT**	
		Access:	R/W One Clear
		BCS MI user interrupt	
	15	**UNUSED11**	
		Access:	R/W One Clear
	14	**UNUSED12**	
		Access:	R/W One Clear
	13	**UNUSED13**	
		Access:	R/W One Clear
	12	**UNUSED14**	
		Access:	R/W One Clear
	11	**CS_WAIT_ON_SEMAPHORE**	
		Access:	R/W One Clear
		CS wait on semaphore	
	10	**CS_L3_COUNTER_SAVE**	
		Access:	R/W One Clear
		CS L3 counter save	
	9	**UNUSED15**	
		Access:	R/W One Clear

GT_INTERRUPT0_IIR - GT INTERRUPT 0 IDENTITY REGISTER

8	**CS_CTX_SWITCH_INTERRUPT**	
	Access:	R/W One Clear
	CS context switch interrupt	

7	**PAGE_FAULT_ERROR**	
	Access:	R/W One Clear
	this interrupt is for handling legacy page fault interface for all command streamer (BCS, VCS, RCS, VECS). when fault repair mode is enabled, interrupt mask register value is not looked at to generate interrupt due to page fault. please refer to 'page fault support' section for more details.	

6	**CS_WATCHDOG_COUNTER_EXPIRED**	
	Access:	R/W One Clear
	CS watchdog counter expired	

5	**L3PARITYERROR**	
	Access:	R/W One Clear
	L3 parity error	

4	**CS_PIPE_CONTROL_NOTIFY**	
	Access:	R/W One Clear
	CS pipe control notify	

3	**CS_ERROR_INTERRUPT**	
	Access:	R/W One Clear
	CS error interrupt	

2	**UNUSED17**	
	Access:	R/W One Clear

1	**Reserved**

0	**CS_MI_USER_INTERRUPT**	
	Access:	R/W One Clear
	CS context switch interrupt	

GT INTERRUPT 0 MASK REGISTER

GT_INTERRUPT0_IMR - GT INTERRUPT 0 MASK REGISTER	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x09190DF9
Size (in bits):	32
Address:	44304h-44307h

This table indicates which events are mapped to each bit of the GT Interrupt 0 registers. Bits 15:0 are used for Render CS. Bits 31:16 are used for Blitter CS.
The IER enabled Render Interrupt IIR (sticky) bits are ORed together to generate the Render Interrupts Pending bit in the Master Interrupt Control register.
The IER enabled Blitter Interrupt IIR (sticky) bits are ORed together to generate the Blitter Interrupts Pending bit in the Master Interrupt Control register.

DWord	Bit	Description		
0	31	**UNUSED0**		
		Access:		R/W
	30	**UNUSED1**		
		Access:		R/W
	29	**UNUSED2**		
		Access:		R/W
	28	**UNUSED3**		
		Access:		R/W
	27	**BCS_WAIT_ON_SEMAPHORE**		
		Default Value:		1b
		Access:		R/W
		BCS wait on semaphore		
	26	**UNUSED4**		
		Access:		R/W
	25	**UNUSED5**		
		Access:		R/W
	24	**BCS_CTX_SWITCH_INTERRUPT**		
		Default Value:		1b
		Access:		R/W
		BCS context switch interrupt		
	23	**UNUSED6**		

GT_INTERRUPT0_IMR - GT INTERRUPT 0 MASK REGISTER

		Access:		R/W
	22	**UNUSED7**		
		Access:		R/W
	21	**UNUSED8**		
		Access:		R/W
	20	**BCS_MI_FLUSH_DWNOTIFY**		
		Default Value:		1b
		Access:		R/W
		BCS MI flush DW notify		
	19	**BCS_ERROR_INTERRUPT**		
		Default Value:		1b
		Access:		R/W
		BCS error interrupt		
	18	**UNUSED9**		
		Access:		R/W
	17	**UNUSED10**		
		Access:		R/W
	16	**BCS_MI_USER_INTERRUPT**		
		Default Value:		1b
		Access:		R/W
		BCS MI user interrupt		
	15	**UNUSED11**		
		Access:		R/W
	14	**UNUSED12**		
		Access:		R/W
	13	**UNUSED13**		
		Access:		R/W
	12	**UNUSED14**		
		Access:		R/W
	11	**CS_WAIT_ON_SEMAPHORE**		
		Default Value:		1b
		Access:		R/W
		CS wait on semaphore		

GT_INTERRUPT0_IMR - GT INTERRUPT 0 MASK REGISTER

10	**CS_L3_COUNTER_SAVE**	
	Default Value:	1b
	Access:	R/W
	CS L3 counter save	

9	**UNUSED15**	
	Access:	R/W

8	**CS_CTX_SWITCH_INTERRUPT**	
	Default Value:	1b
	Access:	R/W
	CS context switch interrupt	

7	**PAGE_FAULT_ERROR**	
	Default Value:	1b
	Access:	R/W
	this interrupt is for handling legacy page fault interface for all command streamer (BCS, VCS, RCS, VECS). when fault repair mode is enabled, interrupt mask register value is not looked at to generate interrupt due to page fault. please refer to 'page fault support' section for more details.	

6	**CS_WATCHDOG_COUNTER_EXPIRED**	
	Default Value:	1b
	Access:	R/W
	CS watchdog counter expired	

5	**L3PARITYERROR**	
	Default Value:	1b
	Access:	R/W
	L3 parity error	

4	**CS_PIPE_CONTROL_NOTIFY**	
	Default Value:	1b
	Access:	R/W
	CS pipe control notify	

3	**CS_ERROR_INTERRUPT**	
	Default Value:	1b
	Access:	R/W
	CS error interrupt	

GT_INTERRUPT0_IMR - GT INTERRUPT 0 MASK REGISTER

	2	**UNUSED17**		
		Access:		R/W
	1	**Reserved**		
	0	**CS_MI_USER_INTERRUPT**		
		Default Value:		1b
		Access:		R/W
		CS context switch interrupt		

GT INTERRUPT 0 STATUS REGISTER

GT_INTERRUPT0_ISR - GT INTERRUPT 0 STATUS REGISTER	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	44300h-44303h

This table indicates which events are mapped to each bit of the GT Interrupt 0 registers. Bits 15:0 are used for Render CS. Bits 31:16 are used for Blitter CS.
The IER enabled Render Interrupt IIR (sticky) bits are ORed together to generate the Render Interrupts Pending bit in the Master Interrupt Control register.
The IER enabled Blitter Interrupt IIR (sticky) bits are ORed together to generate the Blitter Interrupts Pending bit in the Master Interrupt Control register.

DWord	Bit	Description	
0	31	**UNUSED0**	
		Access:	RO
	30	**UNUSED1**	
		Access:	RO
	29	**UNUSED2**	
		Access:	RO
	28	**UNUSED3**	
		Access:	RO
	27	**BCS_WAIT_ON_SEMAPHORE**	
		Access:	RO
		BCS wait on semaphore	
	26	**UNUSED4**	
		Access:	RO
	25	**UNUSED5**	
		Access:	RO
	24	**BCS_CTX_SWITCH_INTERRUPT**	
		Access:	RO
		BCS context switch interrupt	
	23	**UNUSED6**	
		Access:	RO

GT_INTERRUPT0_ISR - GT INTERRUPT 0 STATUS REGISTER

22	**UNUSED7**	
	Access:	RO

21	**UNUSED8**	
	Access:	RO

20	**BCS_MI_FLUSH_DWNOTIFY**	
	Access:	RO
	BCS MI flush DW notify	

19	**BCS_ERROR_INTERRUPT**	
	Access:	RO
	BCS error interrupt	

18	**UNUSED9**	
	Access:	RO

17	**UNUSED10**	
	Access:	RO

16	**BCS_MI_USER_INTERRUPT**	
	Access:	RO
	BCS MI user interrupt	

15	**UNUSED11**	
	Access:	RO

14	**UNUSED12**	
	Access:	RO

13	**UNUSED13**	
	Access:	RO

12	**UNUSED14**	
	Access:	RO

11	**CS_WAIT_ON_SEMAPHORE**	
	Access:	RO
	CS wait on semaphore	

10	**CS_L3_COUNTER_SAVE**	
	Access:	RO
	CS L3 counter save	

9	**UNUSED15**	
	Access:	RO

GT_INTERRUPT0_ISR - GT INTERRUPT 0 STATUS REGISTER

8	**CS_CTX_SWITCH_INTERRUPT**	
	Access:	RO
	CS context switch interrupt	

7	**PAGE_FAULT_ERROR**	
	Access:	RO
	this interrupt is for handling legacy page fault interface for all command streamer (BCS, VCS, RCS, VECS). when fault repair mode is enabled, interrupt mask register value is not looked at to generate interrupt due to page fault. please refer to 'page fault support' section for more details.	

6	**CS_WATCHDOG_COUNTER_EXPIRED**	
	Access:	RO
	CS watchdog counter expired	

5	**L3PARITYERROR**	
	Access:	RO
	L3 parity error	

4	**CS_PIPE_CONTROL_NOTIFY**	
	Access:	RO
	CS pipe control notify	

3	**CS_ERROR_INTERRUPT**	
	Access:	RO
	CS error interrupt	

2	**UNUSED17**	
	Access:	RO

1	**Reserved**	

0	**CS_MI_USER_INTERRUPT**	
	Access:	RO
	CS context switch interrupt	

GT INTERRUPT1 ENABLE REGISTER

GT_INTERRUPT1_IER - GT INTERRUPT1 ENABLE REGISTER	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32

Address:	4431Ch-4431Fh

This table indicates which events are mapped to each bit of the GT Interrupt 0 registers. Bits 15:0 are used for VCS1. Bits 31:16 are used for VCS2.
The IER enabled VCS1 Interrupt IIR (sticky) bits are ORed together to generate the VCS1 Interrupts Pending bit in the Master Interrupt Control register.
The IER enabled VCS2 Interrupt IIR (sticky) bits are ORed together to generate the VCS2 Interrupt Pending bit in the Master Interrupt Control register.

DWord	Bit	Description	
0	31	**UNUSED0**	
		Access:	R/W
	30	**UNUSED1**	
		Access:	R/W
	29	**UNUSED2**	
		Access:	R/W
	28	**UNUSED3**	
		Access:	R/W
	27	**VCS2_WAIT_ON_SEMAPHORE**	
		Access:	R/W
		VCS2 wait on semaphore	
	26	**UNUSED4**	
		Access:	R/W
	25	**Reserved**	
	24	**VCS2_CTX_SWITCH_INTERRUPT**	
		Access:	R/W
		VCS2 context switch interrupt	
	23	**UNUSED5**	
		Access:	R/W
	22	**VCS2_WATCHDOG_COUNTER_EXPIRED**	

GT_INTERRUPT1_IER - GT INTERRUPT1 ENABLE REGISTER

		Access:	R/W
		VCS2 watchdog counter expired	
	21	**Reserved**	
	20	**VCS2_MI_FLUSH_DWNOTIFY**	
		Access:	R/W
		VCS2 MI flush DW notify	
	19	**VCS2_ERROR_INTERRUPT**	
		Access:	R/W
		VCS2 error interrupt	
	18	**UNUSED6**	
		Access:	R/W
	17	**UNUSED7**	
		Access:	R/W
	16	**VCS2_MI_USER_INTERRUPT**	
		Access:	R/W
		VCS2 MI user interrupt	
	15	**UNUSED8**	
		Access:	R/W
	14	**UNUSED9**	
		Access:	R/W
	13	**UNUSED10**	
		Access:	R/W
	12	**UNUSED11**	
		Access:	R/W
	11	**VCS1_WAIT_ON_SEMAPHORE**	
		Access:	R/W
		VCS1 wait on semaphore	
	10	**UNUSED12**	
		Access:	R/W
	9	**Reserved**	
	8	**VCS1_CTX_SWITCH_INTERRUPT**	
		Access:	R/W
		VCS1 context switch interrupt	

GT_INTERRUPT1_IER - GT INTERRUPT1 ENABLE REGISTER

7	**UNUSED13**	
	Access:	R/W
6	**VCS1_WATCHDOG_COUNTER_EXPIRED**	
	Access:	R/W
	VCS1 watchdog counter expired	
5	**Reserved**	
4	**VCS1_MI_FLUSH_DWNOTIFY**	
	Access:	R/W
	VCS1 MI flush DW notify	
3	**VCS1_ERROR_INTERRUPT**	
	Access:	R/W
	VCS1 error interrupt	
2	**UNUSED14**	
	Access:	R/W
1	**UNUSED15**	
	Access:	R/W
0	**VCS1_MI_USER_INTERRUPT**	
	Access:	R/W
	VCS1 MI user interrupt	

GT INTERRUPT1 IDENTITY REGISTER

	GT_INTERRUPT1_IIR - GT INTERRUPT1 IDENTITY REGISTER	
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	44318h-4431Bh	

This table indicates which events are mapped to each bit of the GT Interrupt 0 registers. Bits 15:0 are used for VCS1. Bits 31:16 are used for VCS2.
The IER enabled VCS1 Interrupt IIR (sticky) bits are ORed together to generate the VCS1 Interrupts Pending bit in the Master Interrupt Control register.
The IER enabled VCS2 Interrupt IIR (sticky) bits are ORed together to generate the VCS2 Interrupt Pending bit in the Master Interrupt Control register.

DWord	Bit	Description	
0	31	**UNUSED0**	
		Access:	R/W One Clear
	30	**UNUSED1**	
		Access:	R/W One Clear
	29	**UNUSED2**	
		Access:	R/W One Clear
	28	**UNUSED3**	
		Access:	R/W One Clear
	27	**VCS2_WAIT_ON_SEMAPHORE**	
		Access:	R/W One Clear
		VCS2 wait on semaphore	
	26	**UNUSED4**	
		Access:	R/W One Clear
	25	**Reserved**	
	24	**VCS2_CTX_SWITCH_INTERRUPT**	
		Access:	R/W One Clear
		VCS2 context switch interrupt	
	23	**UNUSED5**	
		Access:	R/W One Clear
	22	**VCS2_WATCHDOG_COUNTER_EXPIRED**	

GT_INTERRUPT1_IIR - GT INTERRUPT1 IDENTITY REGISTER

		Access:	R/W One Clear
		VCS2 watchdog counter expired	
	21	**Reserved**	
	20	**VCS2_MI_FLUSH_DWNOTIFY**	
		Access:	R/W One Clear
		VCS2 MI flush DW notify	
	19	**VCS2_ERROR_INTERRUPT**	
		Access:	R/W One Clear
		VCS2 error interrupt	
	18	**UNUSED6**	
		Access:	R/W One Clear
	17	**UNUSED7**	
		Access:	R/W One Clear
	16	**VCS2_MI_USER_INTERRUPT**	
		Access:	R/W One Clear
		VCS2 MI user interrupt	
	15	**UNUSED8**	
		Access:	R/W One Clear
	14	**UNUSED9**	
		Access:	R/W One Clear
	13	**UNUSED10**	
		Access:	R/W One Clear
	12	**UNUSED11**	
		Access:	R/W One Clear
	11	**VCS1_WAIT_ON_SEMAPHORE**	
		Access:	R/W One Clear
		VCS1 wait on semaphore	
	10	**UNUSED12**	
		Access:	R/W One Clear
	9	**Reserved**	
	8	**VCS1_CTX_SWITCH_INTERRUPT**	
		Access:	R/W One Clear
		VCS1 context switch interrupt	

GT_INTERRUPT1_IIR - GT INTERRUPT1 IDENTITY REGISTER

	7	**UNUSED13**
		Access:	R/W One Clear
	6	**VCS1_WATCHDOG_COUNTER_EXPIRED**
		Access:	R/W One Clear
		VCS1 watchdog counter expired
	5	**Reserved**
	4	**VCS1_MI_FLUSH_DWNOTIFY**
		Access:	R/W One Clear
		VCS1 MI flush DW notify
	3	**VCS1_ERROR_INTERRUPT**
		Access:	R/W One Clear
		VCS1 error interrupt
	2	**UNUSED14**
		Access:	R/W One Clear
	1	**UNUSED15**
		Access:	R/W One Clear
	0	**VCS1_MI_USER_INTERRUPT**
		Access:	R/W One Clear
		VCS1 MI user interrupt

GT INTERRUPT1 MASK REGISTER

GT_INTERRUPT1_IMR - GT INTERRUPT1 MASK REGISTER	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x09590959
Size (in bits):	32
Address:	44314h-44317h

This table indicates which events are mapped to each bit of the GT Interrupt 0 registers. Bits 15:0 are used for VCS1. Bits 31:16 are used for VCS2.
The IER enabled VCS1 Interrupt IIR (sticky) bits are ORed together to generate the VCS1 Interrupts Pending bit in the Master Interrupt Control register.
The IER enabled VCS2 Interrupt IIR (sticky) bits are ORed together to generate the VCS2 Interrupt Pending bit in the Master Interrupt Control register.

DWord	Bit	Description	
0	31	**UNUSED0**	
		Access:	R/W
	30	**UNUSED1**	
		Access:	R/W
	29	**UNUSED2**	
		Access:	R/W
	28	**UNUSED3**	
		Access:	R/W
	27	**VCS2_WAIT_ON_SEMAPHORE**	
		Default Value:	1b
		Access:	R/W
		VCS2 wait on semaphore	
	26	**UNUSED4**	
		Access:	R/W
	25	**Reserved**	
	24	**VCS2_CTX_SWITCH_INTERRUPT**	
		Default Value:	1b
		Access:	R/W
		VCS2 context switch interrupt	
	23	**UNUSED5**	
		Access:	R/W

GT_INTERRUPT1_IMR - GT INTERRUPT1 MASK REGISTER

22	**VCS2_WATCHDOG_COUNTER_EXPIRED**	
	Default Value:	1b
	Access:	R/W
	VCS2 watchdog counter expired	

21	**Reserved**	

20	**VCS2_MI_FLUSH_DWNOTIFY**	
	Default Value:	1b
	Access:	R/W
	VCS2 MI flush DW notify	

19	**VCS2_ERROR_INTERRUPT**	
	Default Value:	1b
	Access:	R/W
	VCS2 error interrupt	

18	**UNUSED6**	
	Access:	R/W

17	**UNUSED7**	
	Access:	R/W

16	**VCS2_MI_USER_INTERRUPT**	
	Default Value:	1b
	Access:	R/W
	VCS2 MI user interrupt	

15	**UNUSED8**	
	Access:	R/W

14	**UNUSED9**	
	Access:	R/W

13	**UNUSED10**	
	Access:	R/W

12	**UNUSED11**	
	Access:	R/W

11	**VCS1_WAIT_ON_SEMAPHORE**	
	Default Value:	1b
	Access:	R/W
	VCS1 wait on semaphore	

GT_INTERRUPT1_IMR - GT INTERRUPT1 MASK REGISTER

	10	**UNUSED12**	
		Access:	R/W

	9	**Reserved**	

	8	**VCS1_CTX_SWITCH_INTERRUPT**	
		Default Value:	1b
		Access:	R/W
		VCS1 context switch interrupt	

	7	**UNUSED13**	
		Access:	R/W

	6	**VCS1_WATCHDOG_COUNTER_EXPIRED**	
		Default Value:	1b
		Access:	R/W
		VCS1 watchdog counter expired	

	5	**Reserved**	

	4	**VCS1_MI_FLUSH_DWNOTIFY**	
		Default Value:	1b
		Access:	R/W
		VCS1 MI flush DW notify	

	3	**VCS1_ERROR_INTERRUPT**	
		Default Value:	1b
		Access:	R/W
		VCS1 error interrupt	

	2	**UNUSED14**	
		Access:	R/W

	1	**UNUSED15**	
		Access:	R/W

	0	**VCS1_MI_USER_INTERRUPT**	
		Default Value:	1b
		Access:	R/W
		VCS1 MI user interrupt	

GT INTERRUPT1 STATUS REGISTER

GT_INTERRUPT1_ISR - GT INTERRUPT1 STATUS REGISTER	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	44310h-44313h

This table indicates which events are mapped to each bit of the GT Interrupt 0 registers. Bits 15:0 are used for VCS1. Bits 31:16 are used for VCS2.
The IER enabled VCS1 Interrupt IIR (sticky) bits are ORed together to generate the VCS1 Interrupts Pending bit in the Master Interrupt Control register.
The IER enabled VCS2 Interrupt IIR (sticky) bits are ORed together to generate the VCS2 Interrupt Pending bit in the Master Interrupt Control register.

DWord	Bit	Description	
0	31	**UNUSED0**	
		Access:	RO
	30	**UNUSED1**	
		Access:	RO
	29	**UNUSED2**	
		Access:	RO
	28	**UNUSED3**	
		Access:	RO
	27	**VCS2_WAIT_ON_SEMAPHORE**	
		Access:	RO
		VCS2 wait on semaphore	
	26	**UNUSED4**	
		Access:	RO
	25	**Reserved**	
	24	**VCS2_CTX_SWITCH_INTERRUPT**	
		Access:	RO
		VCS2 context switch interrupt	
	23	**UNUSED5**	
		Access:	RO
	22	**VCS2_WATCHDOG_COUNTER_EXPIRED**	

GT_INTERRUPT1_ISR - GT INTERRUPT1 STATUS REGISTER

		Access:	RO
		VCS2 watchdog counter expired	
	21	**Reserved**	
	20	**VCS2_MI_FLUSH_DWNOTIFY**	
		Access:	RO
		VCS2 MI flush DW notify	
	19	**VCS2_ERROR_INTERRUPT**	
		Access:	RO
		VCS2 error interrupt	
	18	**UNUSED6**	
		Access:	RO
	17	**UNUSED7**	
		Access:	RO
	16	**VCS2_MI_USER_INTERRUPT**	
		Access:	RO
		VCS2 MI user interrupt	
	15	**UNUSED8**	
		Access:	RO
	14	**UNUSED9**	
		Access:	RO
	13	**UNUSED10**	
		Access:	RO
	12	**UNUSED11**	
		Access:	RO
	11	**VCS1_WAIT_ON_SEMAPHORE**	
		Access:	RO
		VCS1 wait on semaphore	
	10	**UNUSED12**	
		Access:	RO
	9	**Reserved**	
	8	**VCS1_CTX_SWITCH_INTERRUPT**	
		Access:	RO
		VCS1 context switch interrupt	

GT_INTERRUPT1_ISR - GT INTERRUPT1 STATUS REGISTER

	7	**UNUSED13**	
		Access:	RO
	6	**VCS1_WATCHDOG_COUNTER_EXPIRED**	
		Access:	RO
		VCS1 watchdog counter expired	
	5	**Reserved**	
	4	**VCS1_MI_FLUSH_DWNOTIFY**	
		Access:	RO
		VCS1 MI flush DW notify	
	3	**VCS1_ERROR_INTERRUPT**	
		Access:	RO
		VCS1 error interrupt	
	2	**UNUSED14**	
		Access:	RO
	1	**UNUSED15**	
		Access:	RO
	0	**VCS1_MI_USER_INTERRUPT**	
		Access:	RO
		VCS1 MI user interrupt	

GT INTERRUPT3 ENABLE REGISTER

GT_INTERRUPT3_IER - GT INTERRUPT3 ENABLE REGISTER	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	4433Ch-4433Fh

This table indicates which events are mapped to each bit of the GT interrupt 3 register.
Bits 15:0 are VEDBOX and Bit 27:16 are WDBOX AND 31:28 ARE OACS. the VEDBOX Interrupt IIR sticky bits are Ored together to generate VEDBOX interrupt pending bit in the master interrupt control register. WDBOX interrupt IIR and OACS interrupt IIR (sticky) bits are ORed together to generate the WDBOX interrupt pending bit in the master interrupt control register.

DWord	Bit	Description	
0	31:29	**UNUSED0**	
		Access:	R/W
	28	**Reserved**	
	27:17	**UNUSED1**	
		Access:	R/W
	16	**WDBOX_STAT_INT**	
		Access:	R/W
		WDBOX status interrupt	
	15:12	**UNUSED2**	
		Access:	R/W
	11	**VECS_WAIT_SEMAPHORE**	
		Access:	R/W
		VECS wait on semaphore	
	10:9	**UNUSED3**	
		Access:	R/W
	8	**VECS_CTX_SWITCH_INT**	
		Access:	R/W
		VECS context switch interrupt	
	7:5	**UNUSED4**	
		Access:	R/W
	4	**VECS_MI_FLUSH_DWNOTIFY**	

GT_INTERRUPT3_IER - GT INTERRUPT3 ENABLE REGISTER

		Access:	R/W
		VECS MI Flush DW Notify	
	3	**VECS_ERR_INT**	
		Access:	R/W
		VECS error interrupt	
	2:1	**UNUSED5**	
		Access:	R/W
	0	**VECS_MI_USER_INT**	
		Access:	R/W
		VECS MI user interrupt	

GT INTERRUPT3 IDENTITY REGISTER

GT_INTERRUPT3_IIR - GT INTERRUPT3 IDENTITY REGISTER	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	44338h-4433Bh

This table indicates which events are mapped to each bit of the GT interrupt 3 register.
Bits 15:0 are VEDBOX and Bit 27:16 are WDBOX AND 31:28 ARE OACS. the VEDBOX Interrupt IIR sticky bits are Ored together to generate VEDBOX interrupt pending bit in the master interrupt control register. WDBOX interrupt IIR and OACS interrupt IIR (sticky) bits are ORed together to generate the WDBOX interrupt pending bit in the master interrupt control register.

DWord	Bit	Description	
0	31:29	**UNUSED0**	
		Access:	R/W One Clear
	28	**Reserved**	
	27:17	**UNUSED1**	
		Access:	R/W One Clear
	16	**WDBOX_STAT_INT**	
		Access:	R/W One Clear
		WDBOX status interrupt	
	15:12	**UNUSED2**	
		Access:	R/W One Clear
	11	**VECS_WAIT_SEMAPHORE**	
		Access:	R/W One Clear
		VECS wait on semaphore	
	10:9	**UNUSED3**	
		Access:	R/W One Clear
	8	**VECS_CTX_SWITCH_INT**	
		Access:	R/W One Clear
		VECS context switch interrupt	
	7:5	**UNUSED4**	
		Access:	R/W One Clear
	4	**VECS_MI_FLUSH_DWNOTIFY**	

GT_INTERRUPT3_IIR - GT INTERRUPT3 IDENTITY REGISTER

		Access:	R/W One Clear
		VECS MI Flush DW Notify	
	3	**VECS_ERR_INT**	
		Access:	R/W One Clear
		VECS error interrupt	
	2:1	**UNUSED5**	
		Access:	R/W One Clear
	0	**VECS_MI_USER_INT**	
		Access:	R/W One Clear
		VECS MI user interrupt	

GT INTERRUPT3 MASK REGISTER

GT_INTERRUPT3_IMR - GT INTERRUPT3 MASK REGISTER	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00010919
Size (in bits):	32
Address:	44334h-44337h

This table indicates which events are mapped to each bit of the GT interrupt 3 register.
Bits 15:0 are VEDBOX and Bit 27:16 are WDBOX AND 31:28 ARE OACS. the VEDBOX Interrupt IIR sticky bits are Ored together to generate VEDBOX interrupt pending bit in the master interrupt control register. WDBOX interrupt IIR and OACS interrupt IIR (sticky) bits are ORed together to generate the WDBOX interrupt pending bit in the master interrupt control register.

DWord	Bit	Description		
0	31:29	**UNUSED0**		
		Access:		R/W
	28	**Reserved**		
	27:17	**UNUSED1**		
		Access:		R/W
	16	**WDBOX_STAT_INT**		
		Default Value:		1b
		Access:		R/W
		WDBOX status interrupt		
	15:12	**UNUSED2**		
		Access:		R/W
	11	**VECS_WAIT_SEMAPHORE**		
		Default Value:		1b
		Access:		R/W
		VECS wait on semaphore		
	10:9	**UNUSED3**		
		Access:		R/W
	8	**VECS_CTX_SWITCH_INT**		
		Default Value:		1b
		Access:		R/W
		VECS context switch interrupt		

GT_INTERRUPT3_IMR - GT INTERRUPT3 MASK REGISTER

	7:5	**UNUSED4**		
		Access:		R/W
	4	**VECS_MI_FLUSH_DWNOTIFY**		
		Default Value:		1b
		Access:		R/W
		VECS MI Flush DW Notify		
	3	**VECS_ERR_INT**		
		Default Value:		1b
		Access:		R/W
		VECS error interrupt		
	2:1	**UNUSED5**		
		Access:		R/W
	0	**VECS_MI_USER_INT**		
		Default Value:		1b
		Access:		R/W
		VECS MI user interrupt		

GT INTERRUPT3 STATUS REGISTER

GT_INTERRUPT3_ISR - GT INTERRUPT3 STATUS REGISTER	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	44330h-44333h

This table indicates which events are mapped to each bit of the GT interrupt 3 register.
Bits 15:0 are VEDBOX and Bit 27:16 are WDBOX AND 31:28 ARE OACS. the VEDBOX Interrupt IIR sticky bits are Ored together to generate VEDBOX interrupt pending bit in the master interrupt control register. WDBOX interrupt IIR and OACS interrupt IIR (sticky) bits are ORed together to generate the WDBOX interrupt pending bit in the master interrupt control register.

DWord	Bit	Description	
0	31:29	**UNUSED0**	
		Access:	RO
	28	**Reserved**	
	27:17	**UNUSED1**	
		Access:	RO
	16	**WDBOX_STAT_INT**	
		Access:	RO
		WDBOX status interrupt	
	15:12	**UNUSED2**	
		Access:	RO
	11	**VECS_WAIT_SEMAPHORE**	
		Access:	RO
		VECS wait on semaphore	
	10:9	**UNUSED3**	
		Access:	RO
	8	**VECS_CTX_SWITCH_INT**	
		Access:	RO
		VECS context switch interrupt	
	7:5	**UNUSED4**	
		Access:	RO
	4	**VECS_MI_FLUSH_DWNOTIFY**	

GT_INTERRUPT3_ISR - GT INTERRUPT3 STATUS REGISTER

		Access:	RO
		VECS MI Flush DW Notify	
	3	**VECS_ERR_INT**	
		Access:	RO
		VECS error interrupt	
	2:1	**UNUSED5**	
		Access:	RO
	0	**VECS_MI_USER_INT**	
		Access:	RO
		VECS MI user interrupt	

GTLC_PW_STAT

		GTLC_PW_STAT - GTLC_PW_STAT		
Register Space:		MMIO: 0/2/0		
Project:		CHV, BSW		
Source:		PRM		
Default Value:		0x00000000		
Size (in bits):		32		
Address:		130094h		
This register contains Ack and status information for power well requests.				
DWord	**Bit**	**Description**		
0	31:8	**RESERVED**		
		Default Value:		000000h
		Access:		RO
		Reserved		
	7	**Reserved**		
	6	**Reserved**		
		Default Value:		0b
		Access:		RO
		Reserved		
	5	**Reserved**		
	4	**Reserved**		
		Default Value:		0b
		Access:		RO
		Reserved		
	3:2	**Reserved**		
		Default Value:		00b
		Access:		RO
		Reserved		
	1	**ALLOWWAKEERR**		
		Default Value:		0b
		Access:		R/W One Clear
		HW set, SW cleared. When access to media or render is observed when ALLOWWAKE=0, the ALLOWWAKERR bit will be set. It will be up to SW or a power cycle to clear the ALLOWWAKEERR bit.		
	0	**ALLOWWAKEACK**		
		Default Value:		0b

GTLC_PW_STAT - GTLC_PW_STAT		
	Access:	RO
	Indicates that the allow wake request has been completed.	

GTLC_SURVIVE

GTLC_SURVIVE - GTLC_SURVIVE	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	130098h

This register contains configuration bits for modes that the PM unit should operate in.

DWord	Bit	Description	
0	31:12	**RESERVED**	
		Default Value:	00000h
		Access:	RO
		Reserved	
	11	**gvd_pmu_bonus1**	
		Default Value:	0b
		Access:	R/W
		gvd_pmu_bonus1_zczfwoh	
	10	**gvd_pmu_bonus0**	
		Default Value:	0b
		Access:	R/W
		gvd_pmu_bonus0_zczfwoh	
	9	**pmu_gvd_bonus1**	
		Default Value:	0b
		Access:	RO
		pmu_gvd_bonus1_zczfwoh	
	8	**pmu_gvd_bonus0**	
		Default Value:	0b
		Access:	RO
		pmu_gvd_bonus0_zczfwoh	
	7:4	**RESERVED**	
		Default Value:	0h
		Access:	RO
		Reserved	

GTLC_SURVIVE - GTLC_SURVIVE

	3	**GFXCLKSTATUS**	
		Default Value:	0b
		Access:	RO
		This bit is used as a way to confirm that the GFX clocks have been turned on with bit 2. SW would normally write a one to bit2 and then poll on this bit until.	
	2	**GFXCLKFORCEON**	
		Default Value:	0b
		Access:	R/W
		When this bit is set to a '1, the gvd_pmu_gfxclockstartreq_zczfwoh signal to the Punit will be forced to a one.	
	1	**SPAREBIT**	
		Default Value:	0b
		Access:	R/W

Description	Project
Spare bit for CHV, BSW.	CHV, BSW

	0	**GangMediaRender**	
		Default Value:	0b
		Access:	R/W
		0 : The media and render power wells are brought down and up independently. 1 : PM unit will treat both wells as a unit, taking well down together and up together.	

GTLC_WAKE

GTLC_WAKE - GTLC_WAKE		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	130090h	

GT Wake Control.
This register is used as a way for the Punit to control the GTLC Render and Media Power wells.
Writing bit 0 during normal operation may result in a hang.

DWord	Bit	Description		
0	31:26	**RESERVED**		
		Default Value:		00h
		Access:		RO
		Reserved			
	25	**RenderContextExists**		
		Default Value:		0b
		Access:		RO
		The usage is for support of s0ix, where Punit/Driver would restore the value in this bit no later than the time a '1 is written to ALLOWWAKEREQ (bit 0 of this register) during s0ix exit. SW should not write '1 to this bit during a cold boot exit or warm reset exit. CZ reset is the only thing that can clear this bit. This bit is set by HW after the first Render context save after cold boot or warm reset. SW can only write a one to this bit. If SW tries to write a zero, the previous value will be maintained.			
	24	**MediaContextExists**		
		Default Value:		0b
		Access:		RO
		The usage is for support of s0ix, where Punit/Driver would restore the value in this bit no later than the time a '1 is written to ALLOWWAKEREQ (bit 0 of this register) during s0ix exit. SW should not write '1 to this bit during a cold boot exit or warm reset exit. CZ reset is the only thing that can clear this bit. This bit is set by HW after the first Media context save after cold boot or warm reset. SW can only write a one to this bit. If SW tries to write a zero, the previous value will be maintained.			
	23:8	**Common No-wake Hysteresis timer for gfxstartclkreq**		
		Default Value:		0000h

GTLC_WAKE - GTLC_WAKE

		Access:		R/W
		New for CHV, BSW. Hysteresis timer would be used to deassert gfxclockstartreq in case of both wells being in standby and common no-wake request occurs. Counter will be incremented on 60ns interval.		
	7:1	**RESERVED**		
		Default Value:		00h
		Access:		RO
		Reserved		
	0	**ALLOWWAKEREQ**		
		Default Value:		0b
		Access:		R/W
		This bit is used as a way for the driver to make sure GTLC Render AND MEDIA engines do not wake while powered down. The usage is specifically with s0ix, where the driver wants to access the message channel common well (GSclk domain) and does not want the render/media wells to wake up. To remove ambiguity, this bit should be set to '1 and the ALLOWWAKEACK should be observed to the '1 before the FWAKEMEDIAREQ/FWAKERENDERREQ are set. Care must be taken to ONLY use this register prior to Gunit being powered down for S0ix or after registers have been initialized.		

GT Mode Register

GT_MODE - GT Mode Register		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000 CHV, BSW	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	07008h	
Valid Projects:	CHV, BSW	
This Register is used to control the 6EU and 12EU configuration for GT. Writing 0x01FF01FF to this register enables the 6EU mode.		

DWord	Bit	Description
0	31:16	**Mask**
		<table><tr><td>Access:</td><td>WO</td></tr><tr><td>Format:</td><td>Mask[15:0]</td></tr></table> Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)
	15	**EU Local Thread Checking Enable** <table><tr><td>Project:</td><td>CHV, BSW</td></tr><tr><td>Access:</td><td>r/w</td></tr></table> This field configures the EU local thread checking. If enable the stateless access will be checked against the local thread's scratch space size and start address. <table><tr><th>Value</th><th>Name</th><th>Description</th><th>Project</th></tr><tr><td>0h</td><td>Disable **[Default]**</td><td>EU local thread checking is disabled.</td><td>CHV, BSW</td></tr><tr><td>1h</td><td>Enable</td><td>EU local thread checking is enabled.</td><td>CHV, BSW</td></tr></table>
	14:13	**SFR mode** <table><tr><td>Project:</td><td>CHV, BSW</td></tr><tr><td>Access:</td><td>r/w</td></tr><tr><td>Format:</td><td>U2</td></tr></table> This field must be zero when not in GT4(SFR) configuration i.e GTB_rendermode fuse set to SFR.
	12	**Reserved** <table><tr><td>Project:</td><td>CHV, BSW</td></tr><tr><td>Access:</td><td>r/w</td></tr><tr><td>Format:</td><td>PBC</td></tr></table>
	11	**16X16 Cross Slice Hash Disable for SF**

GT_MODE - GT Mode Register

Project:	CHV, BSW
Access:	r/w
Format:	U1

Description
This field allows to control pixel block hashing across slices.
Supports 16X16 pixel block hashing in the checker-board pattern irrespective of MSAA. Setting this bit disables hashing and therefore HW will send all the Pixels to both the slices.

Value	Name	Description
0h	Enable **[Default]**	16X16 Checkerboard hashing enabled across slices
1h	Disable	16X16 Checkerboard hashing disabled across slices

Programming Notes
Normal mode of operation in GT3 mode will be to use either 16x16 Hashing or 32x32 Hashing.

10 **16X16 Cross Slice Hash Disable**

Project:	CHV, BSW
Access:	r/w
Format:	U1

This field allows to control pixel block hashing across slices.

Value	Name	Description
0h	Enable **[Default]**	16X16 Checkerboard hashing enabled across slices
1h	Disable	16X16 Checkerboard hashing disabled across slices

9 **WIZ Hashing Mode High Bit**

Project:	CHV, BSW
Access:	r/w
Format:	U1

This field adds additional hashing modes in combination with the WIZ Hashing Mode field. The Value column in the table below refers to this field (high bit) and the WIZ Hashing Mode field (low bit). This field is don't care if the Hashing Disable bit is set.

Value	Name	Description
0h	**[Default]**	8x8 Checkerboard hashing
1h		8x4 Checkerboard hashing
2h		16x4 Checkerboard hashing
3h		Reserved

Programming Notes
8x4 hashing preferred for when msaa enabled

GT_MODE - GT Mode Register

	8	**Reserved**	
		Project:	CHV, BSW
		Access:	r/w
		Format:	PBC
	7	**WIZ Hashing Mode**	
		Project:	CHV, BSW
		Access:	r/w
		Format:	U1

Description	Project
This field configures the Hashing mode in Windower. This field is don't care if the Hashing Disable bit is set.	
The WIZ Hashing Mode High Bit field is combined with this field to enable additional modes.	CHV, BSW

	6:3	**Reserved**	
		Access:	r/w
		Format:	PBC
	2	**Reserved**	
		Access:	r/w
		Format:	PBC
	1:0	**Reserved**	
		Access:	r/w
		Format:	PBC

GTSCRATCH1

GTSCRATCH1 - GTSCRATCH1	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	4F100h

These (8 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation.
The use of these register is defined by software architecture.

DWord	Bit	Description
0	31:0	**GT_Scratchpad**

Default Value:	00000000h
Access:	R/W

These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation.
The use of these register is defined by software architecture.

GTSCRATCH2

GTSCRATCH2 - GTSCRATCH2	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	4F104h

These (8 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation.
The use of these register is defined by software architecture.

DWord	Bit	Description	
0	31:0	**GT_Scratchpad**	
		Default Value:	00000000h
		Access:	R/W
		These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.	

GTSCRATCH3

GTSCRATCH3 - GTSCRATCH3	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	4F108h
These (8 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.	

DWord	Bit	Description	
0	31:0	**GT_Scratchpad**	
		Default Value:	00000000h
		Access:	R/W
		These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.	

GTSCRATCH4

GTSCRATCH4 - GTSCRATCH4	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	4F10Ch
These (8 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.	

DWord	Bit	Description
0	31:0	**GT_Scratchpad**
		Default Value: 00000000h
		Access: R/W
		These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.

GTSCRATCH5

<table>
<tr><td colspan="3" align="center">**GTSCRATCH5 - GTSCRATCH5**</td></tr>
<tr><td colspan="3">Register Space: MMIO: 0/2/0</td></tr>
<tr><td colspan="3">Project: CHV, BSW</td></tr>
<tr><td colspan="3">Source: PRM</td></tr>
<tr><td colspan="3">Default Value: 0x00000000</td></tr>
<tr><td colspan="3">Size (in bits):   32</td></tr>
<tr><td colspan="3">Address: 4F110h</td></tr>
<tr><td colspan="3">These (8 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation.
The use of these register is defined by software architecture.</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td>**Description**</td></tr>
<tr><td>0</td><td>31:0</td><td>**GT_Scratchpad**

<table><tr><td>Default Value:</td><td>00000000h</td></tr><tr><td>Access:</td><td>R/W</td></tr></table>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation.
The use of these register is defined by software architecture.</td></tr>
</table>

GTSCRATCH6

<table>
<tr><td colspan="3" align="center">**GTSCRATCH6 - GTSCRATCH6**</td></tr>
<tr><td colspan="3">Register Space: MMIO: 0/2/0</td></tr>
<tr><td colspan="3">Project: CHV, BSW</td></tr>
<tr><td colspan="3">Source: PRM</td></tr>
<tr><td colspan="3">Default Value: 0x00000000</td></tr>
<tr><td colspan="3">Size (in bits):   32</td></tr>
<tr><td colspan="3">Address: 4F114h</td></tr>
<tr><td colspan="3">These (8 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation.
The use of these register is defined by software architecture.</td></tr>
</table>

DWord	Bit	Description
0	31:0	**GT_Scratchpad**

Default Value:		00000000h
Access:		R/W

These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation.
The use of these register is defined by software architecture.

GTSCRATCH7

GTSCRATCH7 - GTSCRATCH7	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	4F118h

These (8 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation.
The use of these register is defined by software architecture.

DWord	Bit	Description
0	31:0	**GT_Scratchpad**

Default Value:	00000000h
Access:	R/W

These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation.
The use of these register is defined by software architecture.

GTSCRATCH8

GTSCRATCH8 - GTSCRATCH8		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	4F11Ch	
These (8 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.		
DWord	**Bit**	**Description**
0	31:0	**GT_Scratchpad**
		Default Value: 00000000h
		Access: R/W
		These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.

GTSCRATCHPAD0

GTSCRATCHPAD0 - GTSCRATCHPAD0		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	130040h	
GT scratchpad registers. Scratchpad register can be R/W by both driver and GT. One usage is that GT updates those registers before going to RC6 and reads them on RC6 exit. Write-able and read-able from GT. Reads do NOT rely on the register dispatch path, as dependencies could result. Read-able and write-able from IA. New for CHV, BSW.		

DWord	Bit	Description	
0	31:0	**GT_Scratch0**	
		Default Value:	00000000h
		Access:	R/W
		GT scratchpad register.	

GTSCRATCHPAD1

GTSCRATCHPAD1 - GTSCRATCHPAD1	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	130044h

GT scratchpad registers.
Scratchpad register can be R/W by both driver and GT.
One usage is that GT updates those registers before going to RC6 and reads them on RC6 exit.
Write-able and read-able from GT.
Reads do NOT rely on the register dispatch path, as dependencies could result.
Read-able and write-able from IA.
New for CHV, BSW.

DWord	Bit	Description	
0	31:0	**GT_Scratch1**	
		Default Value:	00000000h
		Access:	R/W
		GT scratchpad register.	

GTSCRATCHPAD2

GTSCRATCHPAD2 - GTSCRATCHPAD2	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	130048h
GT scratchpad registers. Scratchpad register can be R/W by both driver and GT. One usage is that GT updates those registers before going to RC6 and reads them on RC6 exit. Write-able and read-able from GT. Reads do NOT rely on the register dispatch path, as dependencies could result. Read-able and write-able from IA. New for CHV, BSW.	

DWord	Bit	Description	
0	31:0	**GT_Scratch2**	
		Default Value:	00000000h
		Access:	R/W
		GT scratchpad register.	

GTSCRATCHPAD3

GTSCRATCHPAD3 - GTSCRATCHPAD3	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	13004Ch

GT scratchpad registers.
Scratchpad register can be R/W by both driver and GT.
One usage is that GT updates those registers before going to RC6 and reads them on RC6 exit.
Write-able and read-able from GT.
Reads do NOT rely on the register dispatch path, as dependencies could result.
Read-able and write-able from IA.
New for CHV, BSW.

DWord	Bit	Description	
0	31:0	**GT_Scratch3**	
		Default Value:	00000000h
		Access:	R/W
		GT scratchpad register.	

GTSCRATCHPAD4

<table>
<tr><td colspan="4" align="center">**GTSCRATCHPAD4 - GTSCRATCHPAD4**</td></tr>
<tr><td colspan="4">Register Space: MMIO: 0/2/0</td></tr>
<tr><td colspan="4">Project: CHV, BSW</td></tr>
<tr><td colspan="4">Source: PRM</td></tr>
<tr><td colspan="4">Default Value: 0x00000000</td></tr>
<tr><td colspan="4">Size (in bits):   32</td></tr>
<tr><td colspan="4">Address: 130050h</td></tr>
<tr><td colspan="4">GT scratchpad registers.
Scratchpad register can be R/W by both driver and GT.
One usage is that GT updates those registers before going to RC6 and reads them on RC6 exit.
Write-able and read-able from GT.
Reads do NOT rely on the register dispatch path, as dependencies could result.
Read-able and write-able from IA.
New for CHV, BSW.</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td colspan="2">**Description**</td></tr>
<tr><td>0</td><td>31:0</td><td colspan="2">**GT_Scratch4**
<table><tr><td>Default Value:</td><td>00000000h</td></tr><tr><td>Access:</td><td>R/W</td></tr></table>GT scratchpad register.</td></tr>
</table>

GTSCRATCHPAD5

GTSCRATCHPAD5 - GTSCRATCHPAD5	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	130054h

GT scratchpad registers.
Scratchpad register can be R/W by both driver and GT.
One usage is that GT updates those registers before going to RC6 and reads them on RC6 exit.
Write-able and read-able from GT.
Reads do NOT rely on the register dispatch path, as dependencies could result.
Read-able and write-able from IA.
New for CHV, BSW.

DWord	Bit	Description	
0	31:0	**GT_Scratch5**	
		Default Value:	00000000h
		Access:	R/W
		GT scratchpad register.	

GTSCRATCHPAD6

GTSCRATCHPAD6 - GTSCRATCHPAD6		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	130058h	

GT scratchpad registers.
Scratchpad register can be R/W by both driver and GT.
One usage is that GT updates those registers before going to RC6 and reads them on RC6 exit.
Write-able and read-able from GT.
Reads do NOT rely on the register dispatch path, as dependencies could result.
Read-able and write-able from IA.
New for CHV, BSW.

DWord	Bit	Description	
0	31:0	**GT_Scratch6**	
		Default Value:	00000000h
		Access:	R/W
		GT scratchpad register.	

GTSCRATCHPAD7

GTSCRATCHPAD7 - GTSCRATCHPAD7	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	13005Ch

GT scratchpad registers.
Scratchpad register can be R/W by both driver and GT.
One usage is that GT updates those registers before going to RC6 and reads them on RC6 exit.
Write-able and read-able from GT.
Reads do NOT rely on the register dispatch path, as dependencies could result.
Read-able and write-able from IA.
New for CHV, BSW.

DWord	Bit	Description	
0	31:0	**GT_Scratch7**	
		Default Value:	00000000h
		Access:	R/W
		GT scratchpad register.	

GTT Cache Enable

GTT_CACHE_EN - GTT Cache Enable	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000 CHV, BSW
Size (in bits):	32
Address:	04024h
Enable GTT Cache for respective client(s), A0: Must program/observed this to all 0 due to Big Pages Bug 1898112	

DWord	Bit	Description
0	31:0	**GTT Cache Enable for CS**

Access:	R/W

Enable GTT Caching for all the client(s) below:
31: BLIT Engine (overrides individual enables of the units)
30: VEBX Engine (overrides individual enables of the units)
29: MFX Engine (overrides individual enables of the units)
28: GFX Engine (overrides individual enables of the units)
27-15: Reserved
14: VMCunit
13: VLFunit
12: BLBunit
11: VFWunit
10: VEOunit
9: HIZunit
8: RCZunit
7: RCCunit
6: ISCunit
5: DCunit
4: MTunit
3: SOLunit
2: VFunit
1: RSunit
0: CSunit

Value	Name	Project
00000000h	**[Default]**	CHV, BSW

GTTMMADR_LSB

<table>
<tr><td colspan="4" align="center">**GTTMMADR_LSB - GTTMMADR_LSB**</td></tr>
<tr><td colspan="4">Register Space: PCI: 0/2/0</td></tr>
<tr><td colspan="4">Project: CHV, BSW</td></tr>
<tr><td colspan="4">Source: PRM</td></tr>
<tr><td colspan="4">Default Value: 0x00000004</td></tr>
<tr><td colspan="4">Size (in bits):   32</td></tr>
<tr><td colspan="4">Address: 00010h</td></tr>
<tr><td colspan="4">Gfx Memory Mapped Address Range. This is the base
address for all memory mapped registers and GTT table.
This register requests allocation for the combined Graphics Translation Table Modification Range and Memory Mapped Range. For the Global GTT, this range is defined as a memory BAR in graphics device config space. It is an alias into which software is required to write Page Table Entry values (PTEs). Software may read PTE values from the global Graphics Translation Table (GTT). PTEs cannot be written directly into the global GTT memory area.
GTTMMADR comprises of 2 regions, GTT and MMADR. Prior to this feature it had a max size of 4M with 2M MMADR + {0,1M, 2M} GTT. Now GTTMMADR will have a max size of 16M.GTTMMADR = 2M MMADR + 6M rsvd + {0, 2M, 4M, 8M} GTT.GTTMMADR will be 16M aligned.</td></tr>
</table>

DWord	Bit	Description
0	31:24	**MBA_LSB**
		<table><tr><td>Default Value:</td><td>00h</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> Memory Base Address (MBA): Set by the OS, these bits correspond to address signals [35:24].16MB combined for MMIO and Global GTT table aperture (2MB for MMIO, 6MB reserved and 8 MB for GTT).
	23:4	**Reserved**
		<table><tr><td>Default Value:</td><td>00000h</td></tr><tr><td>Access:</td><td>RO</td></tr></table> RSVD:Hardwired to 0 to indicate at least 4MB address range.
	3	**Reserved**
		<table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>RO</td></tr></table> Prefetchable Memory (PREFMEM): Hardwired to 0to prevent prefetching.
	2:1	**MEMTYP**
		<table><tr><td>Default Value:</td><td>10b</td></tr><tr><td>Access:</td><td>RO</td></tr></table> Memory Type (MEMTYP):

		GTTMMADR_LSB - GTTMMADR_LSB
		00: To indicate 32 bit base address 01: Reserved 10: To indicate 64 bit base address 11: Reserved
	0	**Reserved**

GTTMMADR_MSB

GTTMMADR_MSB - GTTMMADR_MSB	
Register Space:	PCI: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	00014h

Gfx Memory Mapped Address Range. This is the base
address for all memory mapped registers and GTT table.
This register requests allocation for the combined Graphics Translation Table Modification Range and Memory Mapped Range. For the Global GTT, this range is defined as a memory BAR in graphics device config space. It is an alias into which software is required to write Page Table Entry values (PTEs). Software may read PTE values from the global Graphics Translation Table (GTT). PTEs cannot be written directly into the global GTT memory area.
GTTMMADR comprises of 2 regions, GTT and MMADR. Prior to this feature it had a max size of 4M with 2M MMADR + {0,1M, 2M} GTT. Now GTTMMADR will have a max size of 16M.GTTMMADR = 2M MMADR + 6M rsvd + {0, 2M, 4M, 8M} GTT.GTTMMADR will be 16M aligned.

DWord	Bit	Description
0	31:4	**MBA_MSB28**

Default Value:	0000000h
Access:	R/W

Description	Project
This field must be set to 0 since addressing above 64GB is not supported.	
Made them spare RW bits.	CHV, BSW

	3:0	**MBA_MSB**

Default Value:	0h
Access:	R/W

Memory Base Address (MBA): Set by the OS, these bits correspond to address signals [35:24].16MB combined for MMIO and Global GTT table aperture (2MB for MMIO, 6MB reserved and 8 MB for GTT).

GU_CTL0

<table>
<tr><td colspan="3" align="center">**GU_CTL0 - GU_CTL0**</td></tr>
<tr><td>Register Space:</td><td colspan="2">MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td colspan="2">CHV, BSW</td></tr>
<tr><td>Source:</td><td colspan="2">PRM</td></tr>
<tr><td>Default Value:</td><td colspan="2">0x00000070</td></tr>
<tr><td>Size (in bits):</td><td colspan="2">32</td></tr>
<tr><td>Address:</td><td colspan="2">182030h</td></tr>
<tr><td colspan="3">Gunit Configuration bits.</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td>**Description**</td></tr>
<tr><td>0</td><td>31</td><td>**GT_IOSFSB_P_READ_POLICY**

| Default Value: | 0b |
| Access: | R/W |

During an SOIx flow, the Punit must read Gunit registers.
0 (Default) : Allow IOSF SB P reads. Note : Punit knows when appropriate times are to issue IOSF SB P reads.
1 : Abort IOSF SB P reads.

Note : This default is the opposite of the IOSF SB polarity bit 12_0008h[31].
Note : For CHV, BSW, this policy register will applies to new PM endpoint (which includes the new PM endpoint).</td></tr>
<tr><td></td><td>30:16</td><td>**SPARE15**

| Default Value: | 0000h |
| Access: | R/W |

Spare register bits for future use</td></tr>
<tr><td></td><td>15</td><td>**SB_Doorbellprevention**

| Default Value: | 0b |
| Access: | R/W |

0 (default) : IOSF P to IOSF SB doorbell registers can be accesses by IOSF SB and IOSF SBp. Note : This should never occur during normal operation.
1 : IOSF SB and IOSF SBp accesses targeting the IOSF P to IOSF SB doorbell registers are aborted.</td></tr>
<tr><td></td><td>14</td><td>**SPARE1**

| Default Value: | 0b |
| Access: | R/W |

Spare register bits for future use</td></tr>
<tr><td></td><td>13</td><td>**Reserved**</td></tr>
</table>

GU_CTL0 - GU_CTL0

	12	**CMDperCLK_ECO**	
		Default Value:	0b
		Access:	R/W
		0(default): GSA command per clock supported. 1: A GAM write followed by a read command cannot dispatch in consecutive clocked.	
	11	**Clrlfsr**	
		Default Value:	0b
		Access:	R/W
		Resets the DFX LFSR's in GIOSFP (gcfg_giosfp_clrlfsr)Write 1, the DFX LFSR's in GIODFP are reset to their initial state. The bit must be written back to 0 before the reset can occur again.	
	10:9	**SPARE2**	
		Default Value:	00b
		Access:	R/W
		Spare bits for future use	
	8	**RESERVED**	
		Default Value:	0b
		Access:	RO
		Reserved	
	7	**IOSFP_DCR_Policy**	
		Default Value:	0b
		Access:	R/W
		IOSF Primary Data Credit Policy. 0 (default) : IOSF Primary data credits reflect data buffer depth. 1: IOSF Primary infinite data credits for both posted and non-posted data is advertised. Credit accounting (and flow control) will rely on cmd credits only.	
	6:4	**IOSFP_PCRD**	
		Default Value:	111b
		Access:	R/W
		IOSF Primary Credit AdvertisementNumber of posted command (and data credits/4) will advertize.	
	3	**SPARE3**	
		Default Value:	0b
		Access:	R/W
		Spare bits for future use	

GU_CTL0 - GU_CTL0	
2	**Reserved**
1	**Reserved**
0	**PFI_Snoop_Override**

Default Value:	0b
Access:	R/W

0 : Observe GAM snoop/non-snoop indications.
1 : Force all GAM requests to snoop.

Hardware Status Mask Register

<table>
<tr><th colspan="2">HWSTAM - Hardware Status Mask Register</th></tr>
<tr><td>Register Space:</td><td>MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td>CHV, BSW</td></tr>
<tr><td>Source:</td><td>RenderCS</td></tr>
<tr><td>Default Value:</td><td>0xFFFFFFFF</td></tr>
<tr><td>Access:</td><td>R/W, RO</td></tr>
<tr><td>Size (in bits):</td><td>32</td></tr>
<tr><td>Trusted Type:</td><td>1</td></tr>
<tr><td>Address:</td><td>02098h</td></tr>
<tr><td>Address:</td><td>12098h-1209Bh</td></tr>
<tr><td>Name:</td><td>Hardware Status Mask Register</td></tr>
<tr><td>ShortName:</td><td>HWSTAM_VCSUNIT0</td></tr>
<tr><td>Address:</td><td>1A098h-1A09Bh</td></tr>
<tr><td>Name:</td><td>Hardware Status Mask Register</td></tr>
<tr><td>ShortName:</td><td>HWSTAM_VECSUNIT</td></tr>
<tr><td>Address:</td><td>1C098h-1C09Bh</td></tr>
<tr><td>Name:</td><td>Hardware Status Mask Register</td></tr>
<tr><td>ShortName:</td><td>HWSTAM_VCSUNIT1</td></tr>
<tr><td>Address:</td><td>22098h-2209Bh</td></tr>
<tr><td>Name:</td><td>Hardware Status Mask Register</td></tr>
<tr><td>ShortName:</td><td>HWSTAM_BCSUNIT</td></tr>
<tr><td colspan="2">The HWSTAM register has the same format as the Interrupt Control Registers. The bits in this register are mask bits that prevent the corresponding bits in the Interrupt Status Register from generating a Hardware Status Write (PCI write cycle). Any unmasked interrupt bit (HWSTAM bit set to 0) will allow the Interrupt Status Register to be written to the ISR location (within the memory page specified by the Hardware Status Page Address Register) when that Interrupt Status Register bit changes state.</td></tr>
</table>

<table>
<tr><th colspan="2">Programming Notes</th></tr>
<tr><td colspan="2">• To write the interrupt to the HWSP, the corresponding IMR bit must also be clear (enabled).
• At most 1 bit can be unmasked at any given time.</td></tr>
</table>

DWord	Bit	Description
0	31:0	**Hardware Status Mask Register Value**

Default Value:	FFFFFFFFh
Format:	Array of Masks

Refer to the Interrupt Control Register section for bit definitions. Reserved bits are RO.

Hardware Status Page Address Register

HWS_PGA - Hardware Status Page Address Register	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1

Address:	02080h-02083h
Name:	Hardware Status Page Address Register
ShortName:	HWS_PGA_RCSUNIT

Address:	12080h-12083h
Name:	Hardware Status Page Address Register
ShortName:	HWS_PGA_VCSUNIT0

Address:	1A080h-1A083h
Name:	Hardware Status Page Address Register
ShortName:	HWS_PGA_VECSUNIT

Address:	1C080h-1C083h
Name:	Hardware Status Page Address Register
ShortName:	HWS_PGA_VCSUNIT1

Address:	22080h-22083h
Name:	Hardware Status Page Address Register
ShortName:	HWS_PGA_BCSUNIT

Description	Project
This register is used to program the 4 KB-aligned System Memory address of the Hardware Status Page used to report hardware status into (typically cacheable) System Memory.	
The address in this register is translated using the Global GTT in memory. The mapping type of the GTT entry determines the snoop nature of the transaction to memory.	CHV, BSW

DWord	Bit	Description
0	31:12	**Address**

Format:	GraphicsAddress[31:12]

This field is used by SW to specify Bits 31:12 of the 4 KB-aligned System Memory address of the 4 KB page known as the Hardware Status Page. The Global GTT is used to map this page from the graphics virtual address to physical address.

HWS_PGA - Hardware Status Page Address Register

		Programming Notes
		If the Per-Process Virtual Address Space and Exec List Enable bit is set, HW requires that the status page is programmed to allow for the context switch status to be reported.
	11:0	**Reserved**
		Format: MBZ

HCP CABAC Status

HCP_CABAC_STATUS - HCP CABAC Status	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoCS
Default Value:	0x00000000
Size (in bits):	32
Trusted Type:	1
Address:	1E904h

HCP CABAC status.

DWord	Bit	Description
0	31:12	**Reserved**
		<table><tr><td>Format:</td><td>MBZ</td></tr></table>
	11	**Temporal Direction Motion Vector Out-of-Bound Error**
		<table><tr><td>Default Value:</td><td>0</td></tr><tr><td>Access:</td><td>RO</td></tr><tr><td>Format:</td><td>U1</td></tr></table> This flag indicates motion vectors calculated from the Temporal Direct Motion vector is larger than the allowed range.
	10:7	**Reserved**
		<table><tr><td>Format:</td><td>MBZ</td></tr></table>
	6	**Motion Vector Delta SE**
		<table><tr><td>Default Value:</td><td>0</td></tr><tr><td>Access:</td><td>RO</td></tr><tr><td>Format:</td><td>U1</td></tr></table> This flag indicates out-of-bound motion vector delta SEs coded in the bit-stream.
	5	**Delta QP SE**
		<table><tr><td>Default Value:</td><td>0</td></tr><tr><td>Access:</td><td>RO</td></tr><tr><td>Format:</td><td>U1</td></tr></table> This flag indicates leading-one overflow during CABAC decode of cu_qp_delta_abs.
	4	**Residual Error**
		<table><tr><td>Default Value:</td><td>0</td></tr><tr><td>Access:</td><td>RO</td></tr></table>

HCP_CABAC_STATUS - HCP CABAC Status			
		Format:	U1
		This flag indicates out-of-bound absolute coefficient level SEs coded in the bit-stream.	
	3	**Slice and Error**	
		Default Value:	0
		Access:	RO
		Format:	U1
		This flag indicates a pre-mature end to the slice or an inconsistent end of slice on the last Ctb of a slice.	
	2:1	**Reserved**	
		Format:	MBZ
	0	**Ctb Concealment Flag**	
		Default Value:	0
		Access:	RO
		Format:	U1
		Each pulse from this flag indicates one Ctb is concealed by the HCP.	

HCP Decode Status

HCP_DEC_STATUS - HCP Decode Status	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	1E900h

HCP Decode status.

DWord	Bit	Description
0	31:18	**Number of Ctbs Concealed**
		<table><tr><td>Default Value:</td><td>0</td></tr><tr><td>Format:</td><td>U14</td></tr></table> This 16-bit field indicates the number of Ctbs concealed during the decoding of the current frame. This field is cleared with the HCP_PIPE_MODE_SELECT command.
	17	**Frame Dec Active**
		<table><tr><td>Default Value:</td><td>0</td></tr><tr><td>Format:</td><td>U1</td></tr></table> This flag indicates that the decoder hardware is actively decoding a picture.
	16	**Indirect Bitstream ObjectAccess Upper Bound Error**
		<table><tr><td>Default Value:</td><td>0</td></tr><tr><td>Format:</td><td>U1</td></tr></table> This flag indicates that the upper bound bit-stream address was reached.
	15:0	**Bit-stream Error Flags**
		<table><tr><td>Default Value:</td><td>0</td></tr><tr><td>Format:</td><td>U16</td></tr></table> This 16-bit field indicates the number of bit stream errors detected for each bit field indicated in the CABAC Status register.

HCP Picture Checksum cIdx0

HCP_PICTURE_CHECKSUM_CIDX0 - HCP Picture Checksum cIdx0	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	1E91Ch

- The HCP Picture Checksum cIdx0 register reports the 32-bit unsigned picture checksum for cIdx=0 calculated by the HCP hardware and whose algorithm is defined in Annex D of the HEVC standard specification.
- This calculated value is updated at the end of the frame.

DWord	Bit	Description	
0	31:0	**Picture checksum cIdx0**	
		Default Value:	0
		Format:	U32

HCP Picture Checksum cIdx1

HCP_PICTURE_CHECKSUM_CIDX1 - HCP Picture Checksum cIdx1	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	1E920h

- The HCP Picture Checksum cIdx1 register reports the 32-bit unsigned picture checksum for cIdx=1 calculated by the HCP hardware and whose algorithm is defined in Annex D of the HEVC standard specification.
- This calculated value is updated at the end of the frame.

DWord	Bit	Description	
0	31:0	**Picture checksum cIdx1**	
		Default Value:	0
		Format:	U32

HCP Picture Checksum cIdx2

HCP_PICTURE_CHECKSUM_CIDX2 - HCP Picture Checksum cIdx2	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	1E924h

- The HCP Picture Checksum cIdx2 register reports the 32-bit unsigned picture checksum for cIdx=2 calculated by the HCP hardware and whose algorithm is defined in Annex D of the HEVC standard specification.
- This calculated value is updated at the end of the frame.

DWord	Bit	Description	
0	31:0	**Picture checksum cIdx2**	
		Default Value:	0
		Format:	U32

HDR

<table>
<tr><td colspan="3" align="center">**HDR - HDR**</td></tr>
<tr><td>Register Space:</td><td colspan="2">PCI: 0/2/0</td></tr>
<tr><td>Project:</td><td colspan="2">CHV, BSW</td></tr>
<tr><td>Source:</td><td colspan="2">PRM</td></tr>
<tr><td>Default Value:</td><td colspan="2">0x00000000</td></tr>
<tr><td>Size (in bits):</td><td colspan="2">32</td></tr>
<tr><td>Address:</td><td colspan="2">0000Ch</td></tr>
<tr><td colspan="3">Header Type</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td>**Description**</td></tr>
<tr><td rowspan="4">0</td><td>31:24</td><td>**RESERVED**
Default Value: 00h
Access: RO
Reserved</td></tr>
<tr><td>23</td><td>**MULTI_FUNCTION_STATUS**
Default Value: 0b
Access: RO
MFUNC: Integrated graphics is a single function</td></tr>
<tr><td>22:16</td><td>**HEADER_CODE**
Default Value: 00h
Access: RO
HDR: Indicates a type 0 configuration space header format</td></tr>
<tr><td>15:0</td><td>**RESERVED**
Default Value: 0000h
Access: RO
Reserved</td></tr>
</table>

HEVC Local APIC Retry Vector

HEVC_LAPIC_RETRY_VECT - HEVC Local APIC Retry Vector	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	0D594h
Valid Projects:	CHV, BSW

Holds the 4 last retry interrupt vectors. The retry vector register holds the last 4 values P24C acknowledged as an interrupt retry. Retries are errors in hardware and are not expected. HUCINT handles retries by logging the interrupt vector in this register. No interrupt is actually retried, and the interrupt stimulus will be lost if a retry occurs. The system will hang eventually. A 2-bit counter (starting at reset value of 0) is used to point to the slot/byte location from which to load the next retry vector (into the 4 available slots) in sequence. This means if a 5th retry vector shows up, it will be loaded into slot 0 again (as the counter wraps around), over-writing the retry vector which existed there in slot_0.

DWord	Bit	Description	
0	31:24	**Vector Slot 3**	
		Format:	U8
	23:16	**Vector Slot 2**	
		Format:	U8
	15:8	**Vector Slot 1**	
		Format:	U8
	7:0	**Vector Slot 0**	
		Format:	U8

HEVC Microcontroller Header Info

HUC_UKERNEL_HDR_INFO - HEVC Microcontroller Header Info

Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoCS
Default Value:	0x00000000
Size (in bits):	32

Address:	0D014h
Valid Projects:	CHV, BSW
Access:	RO

Address:	FFE0D014h
Valid Projects:	CHV, BSW
Access:	R/W

The Address 0D014h is accessible in the MCI register space

DWord	Bit	Description
0	31:10	**Reserved** Format: MBZ
	9:2	**Kernel ID** Access: RO Format: U8 Kernel specified by the HUC_IMEM_STATE command.
	1	**Reserved** Format: MBZ
	0	**uKernel Header Valid** Access: RO Format: U1 A value of 1 indicates that the register contents are loaded successfully and Kernel ID field is valid.

HEVC Microcontroller Status

HUC_STATUS - HEVC Microcontroller Status	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoCS
Default Value:	0x00000000
Size (in bits):	32
Address:	0D000h
Name:	HUC0 MMIO Address
Valid Projects:	CHV, BSW

HUC Status

Programming Notes
The HUC front-side bus address is FFE0_D000h.

DWord	Bit	Description	
0	31:24	**Reserved**	
		Format:	MBZ
	23:16	**Reserved**	
		Access:	R/W
		Format:	U8
	15:8	**uKernel/uOS Status**	
		Access:	R/W
		Format:	U8
		This field is software-defined.	
	7:1	**Boot ROM Code Status**	
		Access:	R/W
		Format:	U7
		This field is software-defined.	
	0	**MinIA Is In Reset**	
		Access:	RO
		Format:	U1
		'1' indicates that MinIA is in reset.	

HS Invocation Counter

HS_INVOCATION_COUNT - HS Invocation Counter		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000, 0x00000000	
Access:	R/W	
Size (in bits):	64	
Trusted Type:	1	
Address:	02300h	

This register stores the number of patch objects processed by the HS unit. E.g., A PATCHLIST_2 topology with 6 vertices would cause this counter to increment by 3 (there are 3 2-vertex patch objects in that topology).This register is part of the context save and restore.

DWord	Bit	Description
0	63:32	**HS Invocation Count UDW** Number of patch objects processed by the HS stage. Updated only when HS Enable and HS Statistics Enable are set in 3DSTATE_HS
	31:0	**HS Invocation Count LDW** Number of patch objects processed by the HS stage. Updated only when HS Enable and HS Statistics Enable are set in 3DSTATE_HS

HUC BMEM SRAM Offset

HUC_BMEM_SRAM_OFFSET - HUC BMEM SRAM Offset		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	VideoCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Address:	FF100154h	
Valid Projects:	CHV, BSW	

DWord	Bit	Description
0	31:17	**Reserved**
		Format: MBZ
	16:6	**BMEM Offset**
		Format: U11
		96KB SRAM address of the start of the BMEM area
	5:0	**Reserved**
		Format: MBZ

HUC BMEM TOP

		HUC_BMEM_TOP - HUC BMEM TOP
Register Space:		MMIO: 0/2/0
Project:		CHV, BSW
Source:		VideoCS
Default Value:		0x00000000
Access:		RO
Size (in bits):		32
Address:		FF100150h
Valid Projects:		CHV, BSW

DWord	Bit	Description
0	31:17	**Reserved** Format: MBZ
	16:6	**BMEM Top** Format: U11 Size + BMEM offset in bytes of BMEM area in the SRAM minus size and bottom are in the kernel description.
	5:0	**Reserved** Format: MBZ

HUC DMA Address Register 0 High

HUC_DMA_ADDR_0_HIGH - HUC DMA Address Register 0 High	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	FFE0D304h
Valid Projects:	CHV, BSW
Address:	0D304h
Valid Projects:	CHV, BSW

The upper 32 bits of the Source DMA address register. The Address 0D304h is accessible in the MCI register space.

DWord	Bit	Description
0	31:16	**Reserved**
		Format: MBZ
	15:0	**Address Upper DWORD**
		Format: GraphicsAddress[47:32]
		This field contains an offset into the associated Graphics Address. Reserved for MinuteIA FSB Access

HUC DMA Address Register 0 Low

<center>**HEVC_DMA_ADDR_0_LOW - HUC DMA Address Register 0 Low**</center>

Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32

Address:	FFE0D300h
Valid Projects:	CHV, BSW

Address:	0D300h
Valid Projects:	CHV, BSW

The lower 32 bits of the Source DMA address register. The Address 0D300h is accessible in the MCI register space.

DWord	Bit	Description
0	31:6	**Address**
		<table><tr><td>Format:</td><td>U26</td></tr></table> This field contains an offset into the associated Graphics Address or MinuteIA FSB Address.
	5:0	**Reserved**
		<table><tr><td>Format:</td><td>MBZ</td></tr></table>

HUC DMA Address Register 1 Low

HUC_DMA_ADDR_DEST - HUC DMA Address Register 1 Low	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoCS
Default Value:	0x00000000
Size (in bits):	32
Address:	FFE0D308h
Valid Projects:	CHV, BSW
Access:	R/W
Address:	0D308h
Valid Projects:	CHV, BSW
Access:	RO

The lower 32 bits of the Destination DMA address register. The Address 0D308h is accessible in the MCI register space.

DWord	Bit	Description	
0	31:17	**Reserved**	
		Format:	MBZ
	16:6	**DMA Destination Address**	
		Access:	R/W
		Format:	U11
		SRAM address bits [16:6] Must be 64B cache line aligned	
	5:0	**Reserved**	
		Format:	MBZ

HUC DMA Control

HUC_DMA_CTRL - HUC DMA Control

Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32

Address:	0D314h
Name:	HUC0 MMIO Address
Valid Projects:	CHV, BSW

Programming Notes

The HUC front-side bus address is FFE0_D314h and the access is R/W.

DWord	Bit	Description
0	31:2	**Reserved** Format: MBZ
	1	**Write** Format: U1 Set/Cleared by FW When 1, will cause DMA to read from the DMA_INT_ADDRESS in 96KB SRAM and WRITE to DMA_EXT_LOW_ADDRESS in DDR (through virtual addressing). DMA_SRC_EXT_HIGH_ADDRESS is ignored when DMA Write is a 1. When 0, DMA will read from the DMA_EXT_LOW_ADDRESS (in ddr through virtual address if fw initiated), and write the data into the 96KB sram at the DMA_INT_ADDRESS. The SRAM refers to the L2 cache. **Value / Name** 1 — SRAM to DDR Transfer 0 — DDR to SRAM Transfer
	0	**Start DMA Transfer** Format: U1 This bit should be programmed last since it will trigger the DMA transfer. Hardware will clear this bit once DMA completes.

HUC DMA Copy Size

HUC_DMA_COPY_SIZE - HUC DMA Copy Size	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32

Address:	0D310h
Name:	HUC0 MMIO Address
Valid Projects:	CHV, BSW

 The lower 32 bits of the Destination DMA address register. The Address 0D310h is accessible in the MCI register space.

Programming Notes
The HUC front-side bus address is FFE0_D310h and the access is R/W.

DWord	Bit	Description
0	31:17	**Reserved** Format: MBZ
	16:6	**DMA Transfer Size** Format: U11 Size of the DMA transfer, in bytes. For smaller transfers SW should use the MinuteIA core directly (DMA programming overhead is higher than copying the data using the MinuteIA core. Approximate inflection point would be ~ 256 bits.) Programming Notes: Size must be a multiple of 64 bytes — Project: CHV, BSW
	5:0	**Reserved** Format: MBZ

HUC DMA External Low Address

HUC_DMA_EXT_LOW_ADDRESS - HUC DMA External Low Address	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	0D300h
Name:	HUC0 MMIO Address
Valid Projects:	CHV, BSW

HUC DMA external address lower 32 bits

Programming Notes
MMIO access is for debug purposes only.
The HUC front-side bus address is FFE0_D300h and the access is R/W.

DWord	Bit	Description
0	31:6	**DMA External Low Address** Format: U26
	5:0	**Reserved** Format: MBZ

HUC DMA Internal Address

HUC_DMA_INT_ADDRESS - HUC DMA Internal Address	

Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32

Address:	0D308h
Name:	HUC0 MMIO Address
Valid Projects:	CHV, BSW

HUC DMA internal address

Programming Notes
The HUC front-side bus address is FFE0_D308h and the access is R/W.

DWord	Bit	Description	
0	31:17	**Reserved**	
		Format:	MBZ
	16:6	**DMA Internal Address**	
		Format:	U11
	5:0	**Reserved**	
		Format:	MBZ

HUC Global Microcontroller Hardware Notify Error

HUC_HW_NOTIFY_ERR - HUC Global Microcontroller Hardware Notify Error	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	0D59Ch
Valid Projects:	CHV, BSW

This register is used to HW to log the type of error encountered by HUC during operation. Bits in the register indicate the type of error and HW sets the corresponding bit when a certain type of error occurs. Graphics driver is expected to inspect, respond and clear. To clear a bit, SW must write 1 to the appropriate bit.

DWord	Bit	Description	
0	31:25	**Reserved**	
		Format:	MBZ
	24	**SHIM notify Error**	
		Format:	U1
		Is set when any error is detected in the shim.	
	23:14	**Reserved**	
		Format:	MBZ
	13	**(INT)Recurrent DMA Interrupt Error**	
		Format:	U1
	12	**(INT)Recurrent Timer Interrupt Error**	
		Format:	U1
	11:0	**Reserved**	
		Format:	MBZ

HUC IMEM Attributes

HUC_IMEM_ATTR - HUC IMEM Attributes		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	VideoCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Address:	FF100164h	
Valid Projects:	CHV, BSW	

DWord	Bit	Description		
0	31:15	**Reserved**		
		Format:		MBZ
	14:9	**Reserved**		
		Project:		CHV, BSW
		Format:		MBZ
	8:7	**Arbitartion Priority**		
		Format:		U2
		Arbitration priority of the Surface at Virtual Adrress Region #{i}		
		Value	**Name**	
		0h	Highest	
		1h	Second Highest	
		2h	Third Highest	
		3h	Lowest	
	6:5	**Cacheablity Control**		
		Format:		U2
		Cacheabilty of the Surface at Virtual Adrress Region #{i}		
		Value	**Name**	
		0h	Use Cacheability Controls from page table	
		1h	UC uncacheable	
		2h	WT write-through	
		3h	WB write-through	
	4:3	**Target Cache**		
		Format:		U2
		Target Cache of the Surface at Virtual Adrress Region #{i}		

HUC_IMEM_ATTR - HUC IMEM Attributes

Value	Name
0h	eLLC
1h	LLC
2h	LLC and eLLC
3h	LLC and eLLC encoded as 3

2	**Reserved**	
	Format:	U1

1:0	**Age**	
	Format:	U2
	Age of the Surface at Virtual Adrress Region #{i}	

HUC Indirect Stream Address

HUC_IND_STREAM_START_ADDR - HUC Indirect Stream Address		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	VideoCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Address:	FF10015Ch	
Valid Projects:	CHV, BSW	
DWord	**Bit**	**Description**
0	31:29	**Reserved**
		Format: MBZ
	28:0	**Stream Out Start Address**
		Format: U29
		Specifies the byte-aligned graphics memory starting address of the slice bit stream relative to the BSD Indirect Stream Out Object Base Address. This is loaded from the HUC_STREAM_OBJECT command dword 3.

HUC Indirect Stream Length

HUC_IND_BSD_LEN - HUC Indirect Stream Length		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	VideoCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Address:	FF100158h	
Valid Projects:	CHV, BSW	

This register is written by the HUC_STREAM_OBJECT command

DWord	Bit	Description
0	31:28	**Reserved**
		Format: MBZ
	27:0	**Bitstream Length**
		Format: U28
		Specifies the length in bytes of the bit stream data plus header for the current slice. It includes the first byte of the slice header and the last non-zero byte of the slice data. Specifically, the zero-padding bytes (if present) and the next start-code are excluded.

HUC Instruction Pointer

HUC_INSTRUCTION_POINTER - HUC Instruction Pointer		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	VideoCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Address:	FFE0D0B0h	
Valid Projects:	CHV, BSW	
Address:	0D0B0h	
Valid Projects:	CHV, BSW	
The Address 0D0B0h is accessible in the MCI register space.		

DWord	Bit	Description
0	31:0	**MinuteIA Instruction Pointer**
		Format: U32

HUC Jump Location

HUC_JMP_DEST - HUC Jump Location	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoCS
Default Value:	0x00000000
Size (in bits):	32
Address:	0D018h
Name:	HUC0 MMIO Address
Valid Projects:	CHV, BSW
Access:	RO

HuC Jump Location

Programming Notes
The HUC front-side bus address is FFE0_D018h

DWord	Bit	Description
0	31:17	**Reserved**
		Format: MBZ
	16:6	**Jump Destination**
		Format: U11
		Base Address for Code Segment loads in the internal SRAM (from the kernel descriptor). P24C will jump to this address after reset.
	5:0	**Reserved**
		Format: MBZ

HUC Last Graphics Memory Fetch Address

HUC_LAST_GRAPHICS_MEMORY_FETCH_ADDRESS - HUC Last Graphics Memory Fetch Address		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	VideoCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Address:	0D160h	
Name:	HUC0 MMIO Address	
Valid Projects:	CHV, BSW	
The P24C last graphics memory fetch address		
Programming Notes		
The HUC front-side bus address is FFE0_D160h.		

DWord	Bit	Description
0	31:6	**Last Graphics Memory Fetch Address**
		Format: U26
		The 26 MSBs of the Last Graphics Memory Fetch Address
	5:0	**Reserved**
		Format: MBZ

HUC Last SRAMCODE Fetch Address

HUC_LAST_SRAMCODE_FETCH_ADDRESS - HUC Last SRAMCODE Fetch Address	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	0D16Ch
Name:	HUC0 MMIO Address
Valid Projects:	CHV, BSW

The P24C last SRAMCODE fetch address. The SRAM refers to the L2 cache in the HuC.

Programming Notes
The HUC front-side bus address is FFE0_D16Ch.

DWord	Bit	Description	
0	31:6	**Last SRAMCODE Fetch Address**	
		Format:	U26
		The 26 MSBs of the Last SRAMCODE Fetch Address	
	5:0	**Reserved**	
		Format:	MBZ

HUC Last SRAMDATA Fetch Address

<table>
<tr><td colspan="2">**HUC_LAST_SRAMDATA_FETCH_ADDRESS - HUC Last SRAMDATA Fetch Address**</td></tr>
<tr><td>Register Space:</td><td>MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td>CHV, BSW</td></tr>
<tr><td>Source:</td><td>VideoCS</td></tr>
<tr><td>Default Value:</td><td>0x00000000</td></tr>
<tr><td>Access:</td><td>RO</td></tr>
<tr><td>Size (in bits):</td><td>32</td></tr>
<tr><td>Address:</td><td>0D170h</td></tr>
<tr><td>Name:</td><td>HUC0 MMIO Address</td></tr>
<tr><td>Valid Projects:</td><td>CHV, BSW</td></tr>
</table>

The P24C last SRAMDATA fetch address

Programming Notes

The HUC front-side bus address is FFE0_D170h.

DWord	Bit	Description
0	31:6	**Last SRAMDATA Fetch Address** Format: U26 The 26 MSBs of the Last SRAMDATA Fetch Address
	5:0	**Reserved** Format: MBZ

HUC Last WOPCM Fetch Address

HUC_LAST_WOPCM_FETCH_ADDRESS - HUC Last WOPCM Fetch Address	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	0D168h
Name:	HUC0 MMIO Address
Valid Projects:	CHV, BSW

The P24C last graphics memory fetch address

Programming Notes
The HUC front-side bus address is FFE0_D168h.

DWord	Bit	Description
0	31:6	**Last WOPCM Fetch Address**
		Format: U26
		The 26 MSBs of the Last WOPCM Fetch Address
	5:0	**Reserved**
		Format: MBZ

HUC Minute IA Idle Status

HUC_MIA_IDLE - HUC Minute IA Idle Status	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32

Address:	0D028h
Name:	HUC0 MMIO Address
Valid Projects:	CHV, BSW

HuC Minute IA (P24C) Idle Status

Programming Notes
The HUC front-side bus address is FFE0_D028h.

DWord	Bit	Description
0	31:1	**Reserved** Format: MBZ
	0	**Idle** Format: U1 Whether the minute IA core is idle. If idle it is safe to remove the clocks from the Minute_IA core and enter RC6. When this field is set and a HALT request comes from MinuteIA, the Minute_IA including P24C are potentially IDLE (after FLUSH and FlushAck is received). If a HALT is received without this field set then MinuteIA is not really idle. This is the idle status register for the FW to communicate to the SHIM to indicate minuteIA is in HALT/idle state. Trigger by HALT command. Hardware will clear this bit on interrupt to minuteIA.

HUC SHIM Control 1

<table>
<tr><td colspan="3" align="center">**HUC_SHIM_CTRL_1 - HUC SHIM Control 1**</td></tr>
<tr><td colspan="3">Register Space: MMIO: 0/2/0</td></tr>
<tr><td colspan="3">Project: CHV, BSW</td></tr>
<tr><td colspan="3">Source: VideoCS</td></tr>
<tr><td colspan="3">Default Value: 0x00000000</td></tr>
<tr><td colspan="3">Size (in bits):   32</td></tr>
<tr><td colspan="3">Address: 0D064h</td></tr>
<tr><td colspan="3">Name: HUC0 MMIO Address</td></tr>
<tr><td colspan="3">Valid Projects: CHV, BSW</td></tr>
<tr><td colspan="3">HuC Shim Control 1</td></tr>
<tr><td colspan="3" align="center">**Programming Notes**</td></tr>
<tr><td colspan="3">The HUC front-side bus address is FFE0_D064h.</td></tr>
</table>

DWord	Bit	Description
0	31:19	**Reserved** Format: MBZ
	18	**128-bit CL Fill Optimization Disable** Format: Disable. Allows SW to disable the 128b CL fill optimization that was added for better performance on CL fills. Value 0 Enable **[Default]** Enables the full CL fill optimization for MinuteIA. Value 1 Disable Force the original behavior (no 128b CL fills)
	17	**Optimized FLUSH Mechanism Disable** Format: Disable. Allows SW to disable the optimized Flush. 0 Enable **[Default]** Default will be optimized implementation (evicts dirty only - no invalidate others). 1 Disable Roll back to original implementation of Evict and Invalidate
	16	**WB / WT Decode Support Disable** Format: Disable. Allows SW to disable WB/WT distinction provided by Shim for MinuteIA L1 cached lines. 0 Enable **[Default]** Assert the WBWT pin to indicate: WB for all cycles below top-of- WOPCM WT for all cycles going to GFX-MEM (above top-of- WOPCM) 1 Disable Force WB for all.

HUC_SHIM_CTRL_1 - HUC SHIM Control 1		
	15	**Clock Gate Enable**
		Format: | Enable
		SW is expected to always set this bit for normal operation. Default value of this register is set to 1, meaning clock gate is enabled. Disabling by writing '0' is not supported.
	14:3	**Reserved**
		Format: | MBZ
	2	**MinuteIA Caching Mode Enable**
		Format: | Enable
		Allows internal caching within MinIA core when set. SW is expected to set this bit for normal operation.
	1:0	**Reserved**
		Format: | MBZ

HUC SHIM Error Record

HUC_SHIM_ERR_TRAP - HUC SHIM Error Record	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	0D070h
Name:	HUC0 MMIO Address
Valid Projects:	CHV, BSW

HuC Shim Error Record (Trap)

Programming Notes
The HUC front-side bus address is FFE0_D070h.

DWord	Bit	Description
0	31:27	**Reserved** Format: MBZ
	26	**Code Write** Format: U1 Set when shim detects a FSB write to the code segment, cleared on the next IMEM command or when MIA is forced into reset.
	25:17	**Reserved** Format: MBZ
	16	**Shutdown cycle received from MinIA** Format: U1 Set when MIA issues a shutdown cycle, cleared on the next IMEM command or when MIA is forced into reset.
	15:0	**Reserved** Format: MBZ

HUC STATUS 2

<table>
<tr><td colspan="3" align="center">**HUC_STATUS2 - HUC STATUS 2**</td></tr>
<tr><td>Register Space:</td><td colspan="2">MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td colspan="2">CHV, BSW</td></tr>
<tr><td>Source:</td><td colspan="2">VideoCS</td></tr>
<tr><td>Default Value:</td><td colspan="2">0x00000000</td></tr>
<tr><td>Access:</td><td colspan="2">R/W</td></tr>
<tr><td>Size (in bits):</td><td colspan="2">32</td></tr>
<tr><td>Address:</td><td colspan="2">0D3B0h</td></tr>
<tr><td>Name:</td><td colspan="2">HUC0 MMIO Address</td></tr>
<tr><td>Valid Projects:</td><td colspan="2">CHV, BSW</td></tr>
<tr><td colspan="3">HUC Status 2</td></tr>
<tr><td colspan="3" align="center">**Programming Notes**</td></tr>
<tr><td colspan="3">The HUC front-side bus address is FFE0_D3B0h.</td></tr>
</table>

DWord	Bit	Description
0	31:21	**Reserved** Format: MBZ
	20	**Reserved** Project: CHV, BSW Format: MBZ
	19	**DISABLED REGION ACCESSED** Access: R/W Format: U1 Set by HW when HuC detects a read or write to a virtual addressing region that was not enabled. Can be cleared by FW writing a 1 to this bit.
	18	**WRITE MERGE BUFFER DATA VALID** Access: R/W Format: U1 Set/cleared by HW when HuC has data waiting to be written to ddr in the write merge buffer. FW can force this data to be flushed to DDR by writing a 1 to this bit or by going into HALT.
	17	**Reserved** Access: RO Format: U1
	16:15	**Reserved**

<table>
<tr><td colspan="4" align="center">**HUC_STATUS2 - HUC STATUS 2**</td></tr>
<tr><td></td><td></td><td>Access:</td><td>RO</td></tr>
<tr><td></td><td></td><td>Format:</td><td>U2</td></tr>
<tr><td></td><td>14</td><td colspan="2">**HUC_HWM_VCS_DONE**</td></tr>
<tr><td></td><td></td><td>Access:</td><td>RO</td></tr>
<tr><td></td><td></td><td>Format:</td><td>U1</td></tr>
<tr><td></td><td></td><td colspan="2">Status of handshake signal to HWM</td></tr>
<tr><td></td><td>13</td><td colspan="2">**DMA IDLE**</td></tr>
<tr><td></td><td></td><td>Access:</td><td>RO</td></tr>
<tr><td></td><td></td><td>Format:</td><td>U1</td></tr>
<tr><td></td><td></td><td colspan="2">Current status of the DMA engine</td></tr>
<tr><td></td><td>12</td><td colspan="2">**LAST STREAM OBJECT**</td></tr>
<tr><td></td><td></td><td>Access:</td><td>RO</td></tr>
<tr><td></td><td></td><td>Format:</td><td>U1</td></tr>
<tr><td></td><td></td><td colspan="2">Set/cleared by HUC_START cmd</td></tr>
<tr><td></td><td>11</td><td colspan="2">**FUSE_HUC_FW_VERIFICATION_BYPASS**</td></tr>
<tr><td></td><td></td><td>Access:</td><td>RO</td></tr>
<tr><td></td><td></td><td>Format:</td><td>U1</td></tr>
<tr><td></td><td></td><td colspan="2">Fuse status</td></tr>
<tr><td></td><td>10</td><td colspan="2">**FUSE_HUC_DISABLE**</td></tr>
<tr><td></td><td></td><td>Access:</td><td>RO</td></tr>
<tr><td></td><td></td><td>Format:</td><td>U1</td></tr>
<tr><td></td><td></td><td colspan="2">Fuse status indicates if the HuC is permanently disabled. At power on, the software driver must check the status of this bit prior to programming the HuC. If this bit is high, the software driver must not program the HuC. Programming the HuC when the HuC is disabled, could result in a hang condition.</td></tr>
<tr><td></td><td>9</td><td colspan="2">**FUSE_HUC_DEBUG_ENABLE**</td></tr>
<tr><td></td><td></td><td>Access:</td><td>RO</td></tr>
<tr><td></td><td></td><td>Format:</td><td>U1</td></tr>
<tr><td></td><td></td><td colspan="2">Fuse status</td></tr>
<tr><td></td><td>8</td><td colspan="2">**VCMD NO AUTHENTICATION ERROR**</td></tr>
<tr><td></td><td></td><td>Access:</td><td>RO</td></tr>
<tr><td></td><td></td><td>Format:</td><td>U1</td></tr>
<tr><td></td><td></td><td colspan="2">This bit is set when hardware detects a HuC VCS command without the authentication signal set.</td></tr>
</table>

		HUC_STATUS2 - HUC STATUS 2	
	7	**VCR FW VERFIFED**	
		Access:	RO
		Format:	U1
		Status of fw verified input signal	
	6	**VALID IMEM LOADED**	
		Access:	RO
		Format:	U1
		Set by hardware when an IMEM command completes without an Upper Bound Error or a VCMD Error. This bit will be cleared by HW at the end of a HUC workload (HUC_Start command with last start bit set).	
	5	**IMEM CONFIGURATION ERROR**	
		Access:	RO
		Format:	U1
		Hardware sets this bit when it detects an error in the WOPCM Kernel number or if the IMEM load would exceed the 96KB SRAM.	
	4	**DMA DMEM ERROR**	
		Access:	RO
		Format:	U1
		Hardware sets this bit when it detects an attempt by the DMEM STATE cmd to write data to address outside of the DMEM bottom to DMEM top addresses in the 96KB SRAM. This can be cleared by the async reset or by another IMEM command.	
	3	**HUC DMA UPPER BOUND ERROR**	
		Access:	RO
		Format:	U1
		Hardware sets this bit when it detects an attempt to read a WOPCM address that is larger than the upper bound offset input signal. This can occur during a VCS IMEM Load command or a code fetch outside of the 96KB SRAM that is larger than the secure storage upper bound offset. This can only be cleared by the async reset.	
	2	**MIA HALT DETECTED**	
		Access:	RO
		Format:	U1
		p24c is in a halt state	
	1	**Reserved**	
		Format:	MBZ
	0	**HuC BUSY Bit**	
		Access:	R/W
		Format:	U1
		Set by HW at the start of a VCS IMEM or DMEM command, can be set or cleared by FW.	

IA32 MTRR FIX4K_C0000 High

MTRR_FIX4K_C0000_H - IA32 MTRR FIX4K_C0000 High	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0F13Ch

Fixed MTRR to identify (C0000-C8000h).

DWord	Bit	Description
0	31:0	**Range0 to Range7 Memory Type**

Default Value:	00000000h
Access:	R/W

Bit[63:56]: Identifies the memory type 00h-FFh of range#7.
Bit[55:48]: Identifies the memory type 00h-FFh of range#6.
Bit[47:40]: Identifies the memory type 00h-FFh of range#5.
Bit[39:32]: Identifies the memory type 00h-FFh of range#4.

IA32 MTRR FIX4K_C0000 Low

MTRR_FIX4K_C0000_L - IA32 MTRR FIX4K_C0000 Low		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F138h	
Fixed MTRR to identify (C0000-C8000h).		
DWord	**Bit**	**Description**
0	31:0	**Range0 to Range7 Memory Type**
		Default Value: 00000000h
		Access: R/W
		Bit[31:24]: Identifies the memory type 00h-FFh of range#3. Bit[23:16]: Identifies the memory type 00h-FFh of range#2. Bit[15:8]: Identifies the memory type 00h-FFh of range#1. Bit[7:0]: Identifies the memory type 00h-FFh of range#0.

IA32 MTRR FIX4K_C8000 High

MTRR_FIX4K_C8000_H - IA32 MTRR FIX4K_C8000 High		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F144h	
Fixed MTRR to identify (C8000-D0000h).		

DWord	Bit	Description
0	31:0	**Range0 to Range7 Memory Type**

Default Value:	00000000h
Access:	R/W

Bit[63:56]: Identifies the memory type 00h-FFh of range#7.
Bit[55:48]: Identifies the memory type 00h-FFh of range#6.
Bit[47:40]: Identifies the memory type 00h-FFh of range#5.
Bit[39:32]: Identifies the memory type 00h-FFh of range#4.

IA32 MTRR FIX4K_C8000 Low

MTRR_FIX4K_C8000_L - IA32 MTRR FIX4K_C8000 Low		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F140h	
Fixed MTRR to identify (C8000-D0000h).		
DWord	**Bit**	**Description**
0	31:0	**Range0 to Range7 Memory Type**

		Default Value:	00000000h
		Access:	R/W

Bit[31:24]: Identifies the memory type 00h-FFh of range#3.
Bit[23:16]: Identifies the memory type 00h-FFh of range#2.
Bit[15:8]: Identifies the memory type 00h-FFh of range#1.
Bit[7:0]: Identifies the memory type 00h-FFh of range#0.

IA32 MTRR FIX4K_D0000 High

MTRR_FIX4K_D0000_H - IA32 MTRR FIX4K_D0000 High	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0F14Ch

Fixed MTRR to identify (D0000-D8000h)

DWord	Bit	Description
0	31:0	**Range0 to Range7 Memory Type**

	Default Value:	00000000h
	Access:	R/W

Bit[63:56]: Identifies the memory type 00h-FFh of range#7.
Bit[55:48]: Identifies the memory type 00h-FFh of range#6.
Bit[47:40]: Identifies the memory type 00h-FFh of range#5.
Bit[39:32]: Identifies the memory type 00h-FFh of range#4.

IA32 MTRR FIX4K_D0000 Low

MTRR_FIX4K_D0000_L - IA32 MTRR FIX4K_D0000 Low	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0F148h

Fixed MTRR to identify (D0000-D8000h)

DWord	Bit	Description	
0	31:0	**Range0 to Range7 Memory Type**	
		Default Value:	00000000h
		Access:	R/W
		Bit[31:24]: Identifies the memory type 00h-FFh of range#3. Bit[23:16]: Identifies the memory type 00h-FFh of range#2. Bit[15:8]: Identifies the memory type 00h-FFh of range#1. Bit[7:0]: Identifies the memory type 00h-FFh of range#0.	

IA32 MTRR FIX4K_D8000 High

MTRR_FIX4K_D8000_H - IA32 MTRR FIX4K_D8000 High		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F154h	
Fixed MTRR to identify (D8000-E0000h)		
DWord	**Bit**	**Description**
0	31:0	**Range0 to Range7 Memory Type**

Default Value:	00000000h
Access:	R/W

Bit[63:56]: Identifies the memory type 00h-FFh of range#7.
Bit[55:48]: Identifies the memory type 00h-FFh of range#6.
Bit[47:40]: Identifies the memory type 00h-FFh of range#5.
Bit[39:32]: Identifies the memory type 00h-FFh of range#4.

IA32 MTRR FIX4K_D8000 Low

MTRR_FIX4K_D8000_L - IA32 MTRR FIX4K_D8000 Low	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0F150h

Fixed MTRR to identify (D8000-E0000h)

DWord	Bit	Description
0	31:0	**Range0 to Range7 Memory Type**

Default Value:	00000000h
Access:	R/W

Bit[31:24]: Identifies the memory type 00h-FFh of range#3.
Bit[23:16]: Identifies the memory type 00h-FFh of range#2.
Bit[15:8]: Identifies the memory type 00h-FFh of range#1.
Bit[7:0]: Identifies the memory type 00h-FFh of range#0.

IA32 MTRR FIX4K_E0000 High

MTRR_FIX4K_E0000_H - IA32 MTRR FIX4K_E0000 High		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F15Ch	

Fixed MTRR to identify (E0000-E8000h).

DWord	Bit	Description
0	31:0	**Range0 to Range7 Memory Type**

Default Value:	00000000h
Access:	R/W

Bit[63:56]: Identifies the memory type 00h-FFh of range#7.
Bit[55:48]: Identifies the memory type 00h-FFh of range#6.
Bit[47:40]: Identifies the memory type 00h-FFh of range#5.
Bit[39:32]: Identifies the memory type 00h-FFh of range#4.

IA32 MTRR FIX4K_E0000 Low

MTRR_FIX4K_E0000_L - IA32 MTRR FIX4K_E0000 Low	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0F158h

Fixed MTRR to identify (E0000-E8000h).

DWord	Bit	Description	
0	31:0	**Range0 to Range7 Memory Type**	
		Default Value:	00000000h
		Access:	R/W
		Bit[31:24]: Identifies the memory type 00h-FFh of range#3. Bit[23:16]: Identifies the memory type 00h-FFh of range#2. Bit[15:8]: Identifies the memory type 00h-FFh of range#1. Bit[7:0]: Identifies the memory type 00h-FFh of range#0.	

IA32 MTRR FIX4K_E8000 High

<table>
<tr><td colspan="3" align="center">**MTRR_FIX4K_E8000_H - IA32 MTRR FIX4K_E8000 High**</td></tr>
<tr><td>Register Space:</td><td colspan="2">MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td colspan="2">CHV, BSW</td></tr>
<tr><td>Source:</td><td colspan="2">PRM</td></tr>
<tr><td>Default Value:</td><td colspan="2">0x00000000</td></tr>
<tr><td>Size (in bits):</td><td colspan="2">32</td></tr>
<tr><td>Address:</td><td colspan="2">0F164h</td></tr>
<tr><td colspan="3">Fixed MTRR to identify (E8000-F0000h).</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td>**Description**</td></tr>
<tr><td>0</td><td>31:0</td><td>**Range0 to Range7 Memory Type**

Default Value: 00000000h
Access: R/W

Bit[63:56]: Identifies the memory type 00h-FFh of range#7.
Bit[55:48]: Identifies the memory type 00h-FFh of range#6.
Bit[47:40]: Identifies the memory type 00h-FFh of range#5.
Bit[39:32]: Identifies the memory type 00h-FFh of range#4.</td></tr>
</table>

IA32 MTRR FIX4K_E8000 Low

MTRR_FIX4K_E8000_L - IA32 MTRR FIX4K_E8000 Low		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F160h	
Fixed MTRR to identify (E8000-F0000h).		
DWord	**Bit**	**Description**
0	31:0	**Range0 to Range7 Memory Type**
		Default Value: ⟶ 00000000h
		Access: ⟶ R/W
		Bit[31:24]: Identifies the memory type 00h-FFh of range#3. Bit[23:16]: Identifies the memory type 00h-FFh of range#2. Bit[15:8]: Identifies the memory type 00h-FFh of range#1. Bit[7:0]: Identifies the memory type 00h-FFh of range#0.

IA32 MTRR FIX4K_F0000 High

MTRR_FIX4K_F0000_H - IA32 MTRR FIX4K_F0000 High	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0F16Ch

Fixed MTRR to identify (F0000-F8000h).

DWord	Bit	Description	
0	31:0	**Range0 to Range7 Memory Type**	
		Default Value:	00000000h
		Access:	R/W
		Bit[63:56]: Identifies the memory type 00h-FFh of range#7. Bit[55:48]: Identifies the memory type 00h-FFh of range#6. Bit[47:40]: Identifies the memory type 00h-FFh of range#5. Bit[39:32]: Identifies the memory type 00h-FFh of range#4.	

IA32 MTRR FIX4K_F0000 Low

MTRR_FIX4K_F0000_L - IA32 MTRR FIX4K_F0000 Low	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0F168h

Fixed MTRR to identify (F0000-F8000h).

DWord	Bit	Description	
0	31:0	**Range0 to Range7 Memory Type**	
		Default Value:	00000000h
		Access:	R/W
		Bit[31:24]: Identifies the memory type 00h-FFh of range#3. Bit[23:16]: Identifies the memory type 00h-FFh of range#2. Bit[15:8]: Identifies the memory type 00h-FFh of range#1. Bit[7:0]: Identifies the memory type 00h-FFh of range#0.	

IA32 MTRR FIX4K_F8000 High

MTRR_FIX4K_F8000_H - IA32 MTRR FIX4K_F8000 High	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0F174h

Fixed MTRR to identify (F8000-100000h).

DWord	Bit	Description
0	31:0	**Range0 to Range7 Memory Type**

Default Value:	00000000h
Access:	R/W

Bit[63:56]: Identifies the memory type 00h-FFh of range#7.
Bit[55:48]: Identifies the memory type 00h-FFh of range#6.
Bit[47:40]: Identifies the memory type 00h-FFh of range#5.
Bit[39:32]: Identifies the memory type 00h-FFh of range#4.

IA32 MTRR FIX4K_F8000 Low

MTRR_FIX4K_F8000_L - IA32 MTRR FIX4K_F8000 Low	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0F170h

Fixed MTRR to identify (F8000-100000h).

DWord	Bit	Description	
0	31:0	**Range0 to Range7 Memory Type**	
		Default Value:	00000000h
		Access:	R/W
		Bit[31:24]: Identifies the memory type 00h-FFh of range#3. Bit[23:16]: Identifies the memory type 00h-FFh of range#2. Bit[15:8]: Identifies the memory type 00h-FFh of range#1. Bit[7:0]: Identifies the memory type 00h-FFh of range#0.	

IA32 MTRR FIX16K_80000 High

MTRR_FIX16K_80000_H - IA32 MTRR FIX16K_80000 High	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0F12Ch

Fixed MTRR to identify 512K-768K of the main memory (80000-A0000h).

DWord	Bit	Description
0	31:0	**Range0 to Range7 Memory Type** Default Value: 00000000h Access: R/W Bit[63:56]: Identifies the memory type 00h-FFh of range#7. Bit[55:48]: Identifies the memory type 00h-FFh of range#6. Bit[47:40]: Identifies the memory type 00h-FFh of range#5. Bit[39:32]: Identifies the memory type 00h-FFh of range#4.

IA32 MTRR FIX16K_80000 Low

<table>
<tr><td colspan="3" align="center">**MTRR_FIX16K_80000_L - IA32 MTRR FIX16K_80000 Low**</td></tr>
<tr><td colspan="3">Register Space: MMIO: 0/2/0</td></tr>
<tr><td colspan="3">Project: CHV, BSW</td></tr>
<tr><td colspan="3">Source: PRM</td></tr>
<tr><td colspan="3">Default Value: 0x00000000</td></tr>
<tr><td colspan="3">Size (in bits):   32</td></tr>
<tr><td colspan="3">Address: 0F128h</td></tr>
<tr><td colspan="3">Fixed MTRR to identify 512K-768K of the main memory (80000-A0000h).</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td>**Description**</td></tr>
<tr><td>0</td><td>31:0</td><td>**Range0 to Range7 Memory Type**

Default Value: 00000000h
Access: R/W

Bit[31:24]: Identifies the memory type 00h-FFh of range#3.
Bit[23:16]: Identifies the memory type 00h-FFh of range#2.
Bit[15:8]: Identifies the memory type 00h-FFh of range#1.
Bit[7:0]: Identifies the memory type 00h-FFh of range#.0</td></tr>
</table>

IA32 MTRR FIX16K_A0000 High

MTRR_FIX16K_A0000_H - IA32 MTRR FIX16K_A0000 High	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0F134h

Fixed MTRR to identify 768K-1024K of the main memory (A0000-C0000h).

DWord	Bit	Description
0	31:0	**Range0 to Range7 Memory Type**

Default Value:	00000000h
Access:	R/W

Bit[63:56]: Identifies the memory type 00h-FFh of range#7.
Bit[55:48]: Identifies the memory type 00h-FFh of range#6.
Bit[47:40]: Identifies the memory type 00h-FFh of range#5.
Bit[39:32]: Identifies the memory type 00h-FFh of range#4.

IA32 MTRR FIX64K_00000 High

MTRR_FIX64K_00000_H - IA32 MTRR FIX64K_00000 High	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0F124h

Fixed MTRR to identify 0-512K of the main memory (0-80000h).

DWord	Bit	Description
0	31:0	**Range0 to Range7 Memory Type**

	Default Value:	00000000h
	Access:	R/W

Bit[63:56]: Identifies the memory type 00h-FFh of range#7.
Bit[55:48]: Identifies the memory type 00h-FFh of range#6.
Bit[47:40]: Identifies the memory type 00h-FFh of range#5.
Bit[39:32]: Identifies the memory type 00h-FFh of range#4.

IA32 MTRR FIX64K_00000 Low

MTRR_FIX64K_00000_L - IA32 MTRR FIX64K_00000 Low	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0F120h

Fixed MTRR to identify 0-512K of the main memory (0-80000h).

DWord	Bit	Description	
0	31:0	**Range0 to Range7 Memory Type**	
		Default Value:	00000000h
		Access:	R/W
		Bit[31:24]: Identifies the memory type 00h-FFh of range#3. Bit[23:16]: Identifies the memory type 00h-FFh of range#2. Bit[15:8]: Identifies the memory type 00h-FFh of range#1. Bit[7:0]: Identifies the memory type 00h-FFh of range#0.	

IA32 MTRR PHYSBASE0 High

MTRR_PHYSBASE0_H - IA32 MTRR PHYSBASE0 High		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F184h	

Variable MTRR0		
DWord	**Bit**	**Description**
0	31:7	**Reserved**
		Default Value: 0000000000000000000000000b
		Access: RO
	6:0	**PhysBase**
		Default Value: 0000000b
		Access: R/W
		Physical Base address[38:32] of the variable MTRR.

IA32 MTRR PHYSBASE0 Low

MTRR_PHYSBASE0_L - IA32 MTRR PHYSBASE0 Low		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F180h	
Variable MTRR0		

DWord	Bit	Description	
0	31:12	**PhysBase**	
		Default Value:	00000h
		Access:	R/W
		Physical Base address[31:0] of the variable MTRR.	
	11:8	**Reserved**	
		Default Value:	0000b
		Access:	RO
	7:0	**Memory Type**	
		Default Value:	00h
		Access:	R/W
		Identifies the memory type 00h-FFh.	

IA32 MTRR PHYSBASE1 High

MTRR_PHYSBASE1_H - IA32 MTRR PHYSBASE1 High		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F194h	

Variable MTRR1		
DWord	**Bit**	**Description**
0	31:7	**Reserved**
		Default Value: 00000000000000000000000000b
		Access: RO
	6:0	**PhysBase**
		Default Value: 0000000b
		Access: R/W
		Physical Base address[38:32] of the variable MTRR.

IA32 MTRR PHYSBASE1 Low

MTRR_PHYSBASE1_L - IA32 MTRR PHYSBASE1 Low		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F190h	
Variable MTRR1		

DWord	Bit	Description
0	31:12	**PhysBase**
		Default Value: 00000h
		Access: R/W
		Physical Base address[31:0] of the variable MTRR.
	11:8	**Reserved**
		Default Value: 0000b
		Access: RO
	7:0	**Memory Type**
		Default Value: 00h
		Access: R/W
		Identifies the memory type 00h-FFh.

IA32 MTRR PHYSBASE2 High

MTRR_PHYSBASE2_H - IA32 MTRR PHYSBASE2 High		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F1A4h	
Variable MTRR2		

DWord	Bit	Description
0	31:7	**Reserved**
		Default Value: 0000000000000000000000000b
		Access: RO
	6:0	**PhysBase**
		Default Value: 0000000b
		Access: R/W
		Physical Base address[38:32] of the variable MTRR.

IA32 MTRR PHYSBASE2 Low

MTRR_PHYSBASE2_L - IA32 MTRR PHYSBASE2 Low		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F1A0h	
Variable MTRR2		

DWord	Bit	Description		
0	31:12	**PhysBase**		
		Default Value:		00000h
		Access:		R/W
		Physical Base address[31:0] of the variable MTRR.		
	11:8	**Reserved**		
		Default Value:		0000b
		Access:		RO
	7:0	**Memory Type**		
		Default Value:		00h
		Access:		R/W
		Identifies the memory type 00h-FFh.		

IA32 MTRR PHYSBASE3 High

MTRR_PHYSBASE3_H - IA32 MTRR PHYSBASE3 High			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0F1B4h		
Variable MTRR3			
DWord	**Bit**	**Description**	
0	31:7	**Reserved**	
		Default Value:	0000000000000000000000000b
		Access:	RO
	6:0	**PhysBase**	
		Default Value:	0000000b
		Access:	R/W
		Physical Base address[38:32] of the variable MTRR.	

IA32 MTRR PHYSBASE3 Low

MTRR_PHYSBASE3_L - IA32 MTRR PHYSBASE3 Low		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F1B0h	
Variable MTRR3		

DWord	Bit	Description		
0	31:12	**PhysBase**		
		Default Value:		00000h
		Access:		R/W
		Physical Base address[31:0] of the variable MTRR.		
	11:8	**Reserved**		
		Default Value:		0000b
		Access:		RO
	7:0	**Memory Type**		
		Default Value:		00h
		Access:		R/W
		Identifies the memory type 00h-FFh.		

IA32 MTRR PHYSBASE4 High

MTRR_PHYSBASE4_H - IA32 MTRR PHYSBASE4 High		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F1C4h	
Variable MTRR4		

DWord	Bit	Description
0	31:7	**Reserved**
		Default Value: 0000000000000000000000000b
		Access: RO
	6:0	**PhysBase**
		Default Value: 0000000b
		Access: R/W
		Physical Base address[38:32] of the variable MTRR.

IA32 MTRR PHYSBASE4 Low

MTRR_PHYSBASE4_L - IA32 MTRR PHYSBASE4 Low		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F1C0h	
Variable MTRR4		

DWord	Bit	Description
0	31:12	**PhysBase**
		Default Value: / 00000h
		Access: / R/W
		Physical Base address[31:0] of the variable MTRR.
	11:8	**Reserved**
		Default Value: / 0000b
		Access: / RO
	7:0	**Memory Type**
		Default Value: / 00h
		Access: / R/W
		Identifies the memory type 00h-FFh

IA32 MTRR PHYSBASE5 High

MTRR_PHYSBASE5_H - IA32 MTRR PHYSBASE5 High		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F1D4h	
Variable MTRR5		

DWord	Bit	Description
0	31:7	**Reserved**
		Default Value: 0000000000000000000000000b
		Access: RO
	6:0	**PhysBase**
		Default Value: 0000000b
		Access: R/W
		Physical Base address[38:32] of the variable MTRR.

IA32 MTRR PHYSBASE5 Low

<table>
<tr>
<td colspan="4" align="center">**MTRR_PHYSBASE5_L - IA32 MTRR PHYSBASE5 Low**</td>
</tr>
<tr>
<td colspan="4">Register Space: MMIO: 0/2/0</td>
</tr>
<tr>
<td colspan="4">Project: CHV, BSW</td>
</tr>
<tr>
<td colspan="4">Source: PRM</td>
</tr>
<tr>
<td colspan="4">Default Value: 0x00000000</td>
</tr>
<tr>
<td colspan="4">Size (in bits):   32</td>
</tr>
<tr>
<td colspan="4">Address: 0F1D0h</td>
</tr>
<tr>
<td colspan="4">Variable MTRR5</td>
</tr>
<tr>
<td>**DWord**</td>
<td>**Bit**</td>
<td colspan="2">**Description**</td>
</tr>
<tr>
<td>0</td>
<td>31:12</td>
<td colspan="2">**PhysBase**</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Default Value:</td>
<td>00000h</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Access:</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td></td>
<td colspan="2">Physical Base address[31:0] of the variable MTRR.</td>
</tr>
<tr>
<td></td>
<td>11:8</td>
<td colspan="2">**Reserved**</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Default Value:</td>
<td>0000b</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Access:</td>
<td>RO</td>
</tr>
<tr>
<td></td>
<td>7:0</td>
<td colspan="2">**Memory Type**</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Default Value:</td>
<td>00h</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Access:</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td></td>
<td colspan="2">Identifies the memory type 00h-FFh.</td>
</tr>
</table>

IA32 MTRR PHYSBASE6 High

MTRR_PHYSBASE6_H - IA32 MTRR PHYSBASE6 High		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F1E4h	
Variable MTRR6		

DWord	Bit	Description
0	31:7	**Reserved**
		Default Value: 0000000000000000000000000b
		Access: RO
	6:0	**PhysBase**
		Default Value: 0000000b
		Access: R/W
		Physical Base address[38:32] of the variable MTRR.

IA32 MTRR PHYSBASE6 Low

MTRR_PHYSBASE6_L - IA32 MTRR PHYSBASE6 Low			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0F1E0h		
Variable MTRR6			
DWord	**Bit**	**Description**	
0	31:12	**PhysBase**	
		Default Value:	00000h
		Access:	R/W
		Physical Base address[31:0] of the variable MTRR.	
	11:8	**Reserved**	
		Default Value:	0000b
		Access:	RO
	7:0	**Memory Type**	
		Default Value:	00h
		Access:	R/W
		Identifies the memory type 00h-FFh.	

IA32 MTRR PHYSBASE7 High

MTRR_PHYSBASE7_H - IA32 MTRR PHYSBASE7 High			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0F1F4h		
Variable MTRR7			
DWord	**Bit**	**Description**	
0	31:7	**Reserved**	
		Default Value:	0000000000000000000000000b
		Access:	RO
	6:0	**PhysBase**	
		Default Value:	0000000b
		Access:	R/W
		Physical Base address[38:32] of the variable MTRR.	

IA32 MTRR PHYSBASE7 Low

MTRR_PHYSBASE7_L - IA32 MTRR PHYSBASE7 Low				
Register Space:	MMIO: 0/2/0			
Project:	CHV, BSW			
Source:	PRM			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0F1F0h			
Variable MTRR7				
DWord	**Bit**	**Description**		
0	31:12	**PhysBase**		
		Default Value:		00000h
		Access:		R/W
		Physical Base address[31:0] of the variable MTRR.		
	11:8	**Reserved**		
		Default Value:		0000b
		Access:		RO
	7:0	**Memory Type**		
		Default Value:		00h
		Access:		R/W
		Identifies the memory type 00h-FFh.		

IA32 MTRR PHYSBASE8 High

MTRR_PHYSBASE8_H - IA32 MTRR PHYSBASE8 High		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F204h	
Variable MTRR8		

DWord	Bit	Description
0	31:7	**Reserved**
		Default Value: 0000000000000000000000000b
		Access: RO
	6:0	**PhysBase**
		Default Value: 0000000b
		Access: R/W
		Physical Base address[38:32] of the variable MTRR.

IA32 MTRR PHYSBASE8 Low

MTRR_PHYSBASE8_L - IA32 MTRR PHYSBASE8 Low		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F200h	
Variable MTRR8		

DWord	Bit	Description
0	31:12	**PhysBase**
		Default Value: 00000h
		Access: R/W
		Physical Base address[31:0] of the variable MTRR
	11:8	**Reserved**
		Default Value: 0000b
		Access: RO
	7:0	**Memory Type**
		Default Value: 00h
		Access: R/W
		Identifies the memory type 00h-FFh.

IA32 MTRR PHYSBASE9 High

MTRR_PHYSBASE9_H - IA32 MTRR PHYSBASE9 High		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F214h	
Variable MTRR9		

DWord	Bit	Description
0	31:7	**Reserved**
		Default Value: 0000000000000000000000000b
		Access: RO
	6:0	**PhysBase**
		Default Value: 0000000b
		Access: R/W
		Physical Base address[38:32] of the variable MTRR.

IA32 MTRR PHYSBASE9 Low

MTRR_PHYSBASE9_L - IA32 MTRR PHYSBASE9 Low		

Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0F210h

Variable MTRR9			
DWord	**Bit**	**Description**	
0	31:12	**PhysBase**	
		Default Value:	00000h
		Access:	R/W
		Physical Base address[31:0] of the variable MTRR.	
	11:8	**Reserved**	
		Default Value:	0000b
		Access:	RO
	7:0	**Memory Type**	
		Default Value:	00h
		Access:	R/W
		Identifies the memory type 00h-FFh.	

IA32 MTRR PHYSMASK0 High

MTRR_PHYSMASK0_H - IA32 MTRR PHYSMASK0 High		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F18Ch	

Variable MTRR0		
DWord	**Bit**	**Description**
0	31:7	**Reserved**
		Default Value: 0000000000000000000000000b
		Access: RO
	6:0	**PhysMask**
		Default Value: 0000000b
		Access: R/W
		Physical MASK for the address[38:32] of the variable MTRR.

IA32 MTRR PHYSMASK0 Low

MTRR_PHYSMASK0_L - IA32 MTRR PHYSMASK0 Low	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0F188h

Variable MTRR0		
DWord	**Bit**	**Description**
0	31:12	**PhysMask**
		Default Value: 00000h
		Access: R/W
		Physical MASK for the address[31:0] of the variable MTRR.
	11	**Valid**
		Default Value: 0b
		Access: R/W
		Valid bit showing that MTRR decode is active.
	10:0	**Reserved**
		Default Value: 00000000000b
		Access: RO

IA32 MTRR PHYSMASK1 High

MTRR_PHYSMASK1_H - IA32 MTRR PHYSMASK1 High		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F19Ch	

Variable MTRR1		
DWord	**Bit**	**Description**
0	31:7	**Reserved**
		Default Value: 0000000000000000000000000b
		Access: RO
	6:0	**PhysMask**
		Default Value: 0000000b
		Access: R/W
		Physical MASK for the address[38:32] of the variable MTRR.

IA32 MTRR PHYSMASK1 Low

<table>
<tr>
<td colspan="4" align="center">**MTRR_PHYSMASK1_L - IA32 MTRR PHYSMASK1 Low**</td>
</tr>
<tr>
<td colspan="4">Register Space: MMIO: 0/2/0</td>
</tr>
<tr>
<td colspan="4">Project: CHV, BSW</td>
</tr>
<tr>
<td colspan="4">Source: PRM</td>
</tr>
<tr>
<td colspan="4">Default Value: 0x00000000</td>
</tr>
<tr>
<td colspan="4">Size (in bits):   32</td>
</tr>
<tr>
<td colspan="4">Address: 0F198h</td>
</tr>
<tr>
<td colspan="4">Variable MTRR1</td>
</tr>
</table>

DWord	Bit	Description	
0	31:12	**PhysMask**	
		Default Value:	00000h
		Access:	R/W
		Physical MASK for the address[31:0] of the variable MTRR.	
	11	**Valid**	
		Default Value:	0b
		Access:	R/W
		Valid bit showing that MTRR decode is active.	
	10:0	**Reserved**	
		Default Value:	00000000000b
		Access:	RO

IA32 MTRR PHYSMASK2 High

MTRR_PHYSMASK2_H - IA32 MTRR PHYSMASK2 High		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F1ACh	

Variable MTRR2		

DWord	Bit	Description
0	31:7	**Reserved**
		Default Value: 0000000000000000000000000b
		Access: RO
	6:0	**PhysMask**
		Default Value: 0000000b
		Access: R/W
		Physical MASK for the address[38:32] of the variable MTRR.

IA32 MTRR PHYSMASK2 Low

MTRR_PHYSMASK2_L - IA32 MTRR PHYSMASK2 Low	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0F1A8h

Variable MTRR2

DWord	Bit	Description	
0	31:12	**PhysMask**	
		Default Value:	00000h
		Access:	R/W
		Physical MASK for the address[31:0] of the variable MTRR.	
	11	**Valid**	
		Default Value:	0b
		Access:	R/W
		Valid bit showing that MTRR decode is active.	
	10:0	**Reserved**	
		Default Value:	00000000000b
		Access:	RO

IA32 MTRR PHYSMASK3 High

MTRR_PHYSMASK3_H - IA32 MTRR PHYSMASK3 High	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0F1BCh

Variable MTRR3

DWord	Bit	Description	
0	31:7	**Reserved**	
		Default Value:	00000000000000000000000000b
		Access:	RO
	6:0	**PhysMask**	
		Default Value:	0000000b
		Access:	R/W
		Physical MASK for the address[38:32] of the variable MTRR.	

IA32 MTRR PHYSMASK3 Low

MTRR_PHYSMASK3_L - IA32 MTRR PHYSMASK3 Low		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F1B8h	
Variable MTRR3		

DWord	Bit	Description
0	31:12	**PhysMask**
		Default Value: 00000h
		Access: R/W
		Physical MASK for the address[31:0] of the variable MTRR.
	11	**Valid**
		Default Value: 0b
		Access: R/W
		Valid bit showing that MTRR decode is active.
	10:0	**Reserved**
		Default Value: 00000000000b
		Access: RO

IA32 MTRR PHYSMASK4 High

MTRR_PHYSMASK4_H - IA32 MTRR PHYSMASK4 High	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0F1CCh

Variable MTRR4		

DWord	Bit	Description
0	31:7	**Reserved**
		Default Value: / 0000000000000000000000000b
		Access: / RO
	6:0	**PhysMask**
		Default Value: / 0000000b
		Access: / R/W
		Physical MASK for the address[38:32] of the variable MTRR.

IA32 MTRR PHYSMASK4 Low

MTRR_PHYSMASK4_L - IA32 MTRR PHYSMASK4 Low		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F1C8h	
Variable MTRR4		

DWord	Bit	Description
0	31:12	**PhysMask**
			Default Value:	00000h	
			Access:	R/W	
		Physical MASK for the address[31:0] of the variable MTRR.
	11	**Valid**
			Default Value:	0b	
			Access:	R/W	
		Valid bit showing that MTRR decode is active.
	10:0	**Reserved**
			Default Value:	00000000000b	
			Access:	RO	

IA32 MTRR PHYSMASK5 High

MTRR_PHYSMASK5_H - IA32 MTRR PHYSMASK5 High		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F1DCh	
Variable MTRR5		

DWord	Bit	Description	
0	31:7	**Reserved**	
		Default Value:	0000000000000000000000000b
		Access:	RO
	6:0	**PhysMask**	
		Default Value:	0000000b
		Access:	R/W
		Physical MASK for the address[38:32] of the variable MTRR.	

IA32 MTRR PHYSMASK5 Low

MTRR_PHYSMASK5_L - IA32 MTRR PHYSMASK5 Low		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F1D8h	
Variable MTRR5		

DWord	Bit	Description		
0	31:12	**PhysMask**			
		Default Value:		00000h
		Access:		R/W
		Physical MASK for the address[31:0] of the variable MTRR.			
	11	**Valid**			
		Default Value:		0b
		Access:		R/W
		Valid bit showing that MTRR decode is active.			
	10:0	**Reserved**			
		Default Value:		00000000000b
		Access:		RO

IA32 MTRR PHYSMASK6 High

MTRR_PHYSMASK6_H - IA32 MTRR PHYSMASK6 High		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F1ECh	
Variable MTRR6		

DWord	Bit	Description
0	31:7	**Reserved**
		Default Value: 0000000000000000000000000b
		Access: RO
	6:0	**PhysMask**
		Default Value: 0000000b
		Access: R/W
		Physical MASK for the address[38:32] of the variable MTRR.

IA32 MTRR PHYSMASK6 Low

MTRR_PHYSMASK6_L - IA32 MTRR PHYSMASK6 Low		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F1E8h	
Variable MTRR6		

DWord	Bit	Description
0	31:12	**PhysMask**
		Default Value: / 00000h
		Access: / R/W
		Physical MASK for the address[31:0] of the variable MTRR.
	11	**Valid**
		Default Value: / 0b
		Access: / R/W
		Valid bit showing that MTRR decode is active.
	10:0	**Reserved**
		Default Value: / 00000000000b
		Access: / RO

IA32 MTRR PHYSMASK7 High

MTRR_PHYSMASK7_H - IA32 MTRR PHYSMASK7 High	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0F1FCh

Variable MTRR7

DWord	Bit	Description	
0	31:7	**Reserved**	
		Default Value:	0000000000000000000000000b
		Access:	RO
	6:0	**PhysMask**	
		Default Value:	0000000b
		Access:	R/W
		Physical MASK for the address[38:32] of the variable MTRR.	

IA32 MTRR PHYSMASK7 Low

MTRR_PHYSMASK7_L - IA32 MTRR PHYSMASK7 Low	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0F1F8h

Variable MTRR7

DWord	Bit	Description
0	31:12	**PhysMask**
		Default Value: 00000h
		Access: R/W
		Physical MASK for the address[31:0] of the variable MTRR.
	11	**Valid**
		Default Value: 0b
		Access: R/W
		Valid bit showing that MTRR decode is active.
	10:0	**Reserved**
		Default Value: 00000000000b
		Access: RO

IA32 MTRR PHYSMASK8 High

MTRR_PHYSMASK8_H - IA32 MTRR PHYSMASK8 High		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F20Ch	
Variable MTRR8		

DWord	Bit	Description
0	31:7	**Reserved**
		Default Value: 00000000000000000000000000b
		Access: RO
	6:0	**PhysMask**
		Default Value: 0000000b
		Access: R/W
		Physical MASK for the address[38:32] of the variable MTRR.

IA32 MTRR PHYSMASK8 Low

MTRR_PHYSMASK8_L - IA32 MTRR PHYSMASK8 Low		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F208h	
Variable MTRR8		

DWord	Bit	Description
0	31:12	**PhysMask**
		Default Value:	00000h
		Access:	R/W
		Physical MASK for the address[31:0] of the variable MTRR.
	11	**Valid**
		Default Value:	0b
		Access:	R/W
		Valid bit showing that MTRR decode is active.
	10:0	**Reserved**
		Default Value:	00000000000b
		Access:	RO

IA32 MTRR PHYSMASK9 High

MTRR_PHYSMASK9_H - IA32 MTRR PHYSMASK9 High		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F21Ch	
Variable MTRR9		

DWord	Bit	Description
0	31:7	**Reserved**
		Default Value: 0000000000000000000000000b
		Access: RO
	6:0	**PhysMask**
		Default Value: 0000000b
		Access: R/W
		Physical MASK for the address[38:32] of the variable MTRR.

IA32 MTRR PHYSMASK9 Low

MTRR_PHYSMASK9_L - IA32 MTRR PHYSMASK9 Low		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F218h	
Variable MTRR9		

DWord	Bit	Description
0	31:12	**PhysMask** <table><tr><td>Default Value:</td><td>00000h</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> Physical MASK for the address[31:0] of the variable MTRR.
	11	**Valid** <table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> Valid bit showing that MTRR decode is active.
	10:0	**Reserved** <table><tr><td>Default Value:</td><td>00000000000b</td></tr><tr><td>Access:</td><td>RO</td></tr></table>

IA Vertices Count

IA_VERTICES_COUNT - IA Vertices Count	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Trusted Type:	1

Address:	02310h
Valid Projects:	

This register stores the count of vertices processed by VF. This register is part of the context save and restore.

DWord	Bit	Description
0	63:32	**IA Vertices Count Report UDW** Total number of vertices fetched by the VF stage. This count is updated for every input vertex as long as Statistics Enable is set in VF_STATE (see the Vertex Fetch Chapter in the 3D Volume.)
	31:0	**IA Vertices Count Report LDW** Total number of vertices fetched by the VF stage. This count is updated for every input vertex as long as Statistics Enable is set in VF_STATE (see the Vertex Fetch Chapter in the 3D Volume.)

IDLE Messaging Register for Blitter Engine

MSG_IDLE_BCS - IDLE Messaging Register for Blitter Engine		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	16	
Address:	0800Ch	
Message registers have bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16]. In order to set bit0, for example, the data would be 0x0001_0001. In order to clear bit0, for example, the data would be 0x0001_0000. Note that mask bit is the data bit offset + 16. Message registers are protected from non-GT writes via the Message Channel.		

DWord	Bit	Description
0	15:6	**Reserved**
		Access: RO
	5	**Flush and Block Acknowledgement**
		Access: R/W
		Flush and Block Acknowledgement 1'b0 : Not flushed and blocked \<default\> 1'b1 : Unit has flushed and blocked its pipeline
	4	**Preparation for Reset Acknowledgement**
		Access: R/W
		Go Acknowledgement 1'b0 : Go=0 Ack \<default\> 1'b1 : Go=1 Ack Requirement is that when Go=0 request is sent, the agent has to indicate busy before sending the Go=0 acknowledgement. It can only go idle again once Go=1 is received.
	3:0	**Idle Messaging**
		Access: R/W
		Idle Messaging Bit[3] Secondary Pipe Clock Gating 1'b0 : Secondary pipe clock must be on \<default\> 1'b1 : Secondary pipe clock may be gated Bit[2] Primary Pipe Clock Gating 1'b0 : Primary pipe clock must be on \<default\> 1'b1 : Primary pipe clock may be gated

MSG_IDLE_BCS - IDLE Messaging Register for Blitter Engine

		Bit[1] C6 Allowed 1'b0 : Do not allow GT to enter C6 <default> 1'b1 : GT may enter C6 Bit[0] Idle Indication 1'b0 : Pipe is busy <default> 1'b1 : Pipe is idle ** See "Valid Combinations for Idle Messaging" Table

IDLE Messaging Register for Media0 Engine

MSG_IDLE_VCS0 - IDLE Messaging Register for Media0 Engine	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	16
Address:	08004h

Message registers have bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16]. In order to set bit0, for example, the data would be 0x0001_0001. In order to clear bit0, for example, the data would be 0x0001_0000. Note that mask bit is the data bit offset + 16. Message registers are protected from non-GT writes via the Message Channel.

DWord	Bit	Description	
0	15:6	**Reserved**	
		Access:	RO
	5	**Flush and Block Acknowledgement**	
		Access:	R/W
		Flush and Block Acknowledgement 1'b0 : Not flushed and blocked <default> 1'b1 : Unit has flushed and blocked its pipeline	
	4	**Preparation for Reset Acknowledgement**	
		Access:	R/W
		Go Acknowledgement 1'b0 : Go=0 Ack <default> 1'b1 : Go=1 Ack Requirement is that when Go=0 request is sent, the agent has to indicate busy before sending the Go=0 acknowledgement. It can only go idle again once Go=1 is received.	
	3:0	**Idle Messaging**	
		Access:	R/W
		Idle Messaging Bit[3] Secondary Pipe Clock Gating 1'b0 : Secondary pipe clock must be on <default> 1'b1 : Secondary pipe clock may be gated Bit[2] Primary Pipe Clock Gating 1'b0 : Primary pipe clock must be on <default> 1'b1 : Primary pipe clock may be gated Bit[1]	

MSG_IDLE_VCS0 - IDLE Messaging Register for Media0 Engine

		C6 Allowed
		1'b0 : Do not allow GT to enter C6 <default>
		1'b1 : GT may enter C6
		Bit[0]
		IDLE Indication - Media done
		1'b0 : Pipe is busy <default>
		1'b1 : Pipe is idle
		Refer to bits A024[10:9] for different Media turbo scenarios.
		** See "Valid Combinations for Idle Messaging" Table

IDLE Messaging Register for Media1 Engine

MSG_IDLE_VCS1 - IDLE Messaging Register for Media1 Engine	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	16
Address:	08008h

Message registers have bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16]. In order to set bit0, for example, the data would be 0x0001_0001. In order to clear bit0, for example, the data would be 0x0001_0000. Note that mask bit is the data bit offset + 16. Message registers are protected from non-GT writes via the Message Channel.

DWord	Bit	Description
0	15:6	**Reserved**
		Access: RO
	5	**Flush and Block Acknowledgement**
		Access: R/W
		Flush and Block Acknowledgement 1'b0 : Not flushed and blocked \<default> 1'b1 : Unit has flushed and blocked its pipeline
	4	**Preparation for Reset Acknowledgement**
		Access: R/W
		Go Acknowledgement 1'b0 : Go=0 Ack \<default> 1'b1 : Go=1 Ack Requirement is that when Go=0 request is sent, the agent has to indicate busy before sending the Go=0 acknowledgement. It can only go idle again once Go=1 is received.
	3:0	**Idle Messaging**
		Access: R/W
		Idle Messaging Bit[3] Secondary Pipe Clock Gating 1'b0 : Secondary pipe clock must be on \<default> 1'b1 : Secondary pipe clock may be gated Bit[2] Primary Pipe Clock Gating 1'b0 : Primary pipe clock must be on \<default> 1'b1 : Primary pipe clock may be gated Bit[1]

MSG_IDLE_VCS1 - IDLE Messaging Register for Media1 Engine

		C6 Allowed 1'b0 : Do not allow GT to enter C6 <default> 1'b1 : GT may enter C6 Bit[0] Idle Indication 1'b0 : Pipe is busy <default> 1'b1 : Pipe is idle ** See "Valid Combinations for Idle Messaging" Table

IDLE Messaging Register for Render Engine

MSG_IDLE_CS - IDLE Messaging Register for Render Engine	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	08000h

Message registers have bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16]. In order to set bit0, for example, the data would be 0x0001_0001. In order to clear bit0, for example, the data would be 0x0001_0000. Note that mask bit is the data bit offset + 16. Message registers are protected from non-GT writes via the Message Channel.
NOTE - GPGPU_ACTIVE and MEDIA_ACTIVE are context saved and restored; the other bits are cleared out before saving context

DWord	Bit	Description
0	31:16	**Context Save Mask**
		Access: R/W
		When context save is in progress, mask is forced to particular value to save off messages that need to be retained across an RC6 event. Currently for this register, the following fields are context saved and restored for an RC6 event: [7] GPGPU_ACTIVE [6] MEDIA_ACTIVE
	15:8	**Reserved**
		Access: RO
	7	**GPGPU Active Load Indication**
		Access: R/W
		Active Load Indication - bits[7:6] of this register 2'b00 : Render load is being executed <default> 2'b01 : Media load is being executed 2'b10 : GPGPU load is being executed 2'b11 : Undefined gpmunit self-clears this bit upon sampling.
	6	**Media Active Load Indication**
		Access: R/W
		Active Load Indication - bits[7:6] of this register 2'b00 : Render load is being executed <default> 2'b01 : Media load is being executed 2'b10 : GPGPU load is being executed

MSG_IDLE_CS - IDLE Messaging Register for Render Engine

		2'b11 : Undefined gpmunit self-clears this bit upon sampling.
	5	**Flush and Block Acknowledgement** Access: R/W Flush and Block Acknowledgement 1'b0 : Not flushed and blocked <default> 1'b1 : Unit has flushed and blocked its pipeline
	4	**Preparation for Reset Acknowledgement** Access: R/W Go Acknowledgement 1'b0 : Go=0 Ack <default> 1'b1 : Go=1 Ack Requirement is that when Go=0 request is sent, the agent has to indicate busy before sending the Go=0 acknowledgement. It can only go idle again once Go=1 is received. Also, Refer to the table in the description for bits A024[10:9]
	3:0	**Idle Messaging** Access: R/W Idle Messaging Bit[3] Secondary Pipe Clock Gating 1'b0 : Secondary pipe clock must be on <default> 1'b1 : Secondary pipe clock may be gated Bit[2] Primary Pipe Clock Gating 1'b0 : Primary pipe clock must be on <default> 1'b1 : Primary pipe clock may be gated Bit[1] C6 Allowed 1'b0 : Do not allow GT to enter C6 <default> 1'b1 : GT may enter C6 Bit[0] Idle Indication 1'b0 : Pipe is busy <default> 1'b1 : Pipe is idle ** See "Valid Combinations for Idle Messaging" Table Also, Refer to the table in the description for bits A024[10:9]

IDLE Messaging Register for VEBox

MSG_IDLE_VECS - IDLE Messaging Register for VEBox	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	16
Address:	08010h

Message registers have bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16]. In order to set bit0, for example, the data would be 0x0001_0001. In order to clear bit0, for example, the data would be 0x0001_0000. Note that mask bit is the data bit offset + 16. Message registers are protected from non-GT writes via the Message Channel.

DWord	Bit	Description
0	15:6	**Reserved**
		Access: RO
	5	**Flush and Block Acknowledgement**
		Access: R/W
		Flush and Block Acknowledgement 1'b0 : Not flushed and blocked <default> 1'b1 : Unit has flushed and blocked its pipeline
	4	**Preparation for Reset Acknowledgement**
		Access: R/W
		Go Acknowledgement 1'b0 : Go=0 Ack <default> 1'b1 : Go=1 Ack Requirement is that when Go=0 request is sent, the agent has to indicate busy before sending the Go=0 acknowledgement. It can only go idle again once Go=1 is received.
	3:0	**Idle Messaging**
		Access: R/W
		Idle Messaging Bit[3] Secondary Pipe Clock Gating 1'b0 : Secondary pipe clock must be on <default> 1'b1 : Secondary pipe clock may be gated Bit[2] Primary Pipe Clock Gating 1'b0 : Primary pipe clock must be on <default> 1'b1 : Primary pipe clock may be gated Bit[1]

MSG_IDLE_VECS - IDLE Messaging Register for VEBox

		C6 Allowed 1'b0 : Do not allow GT to enter C6 <default> 1'b1 : GT may enter C6 Bit[0] Idle Indication 1'b0 : Pipe is busy <default> 1'b1 : Pipe is idle ** See "Valid Combinations for Idle Messaging" Table

IDLE Messaging Register for Wi-Di

MSG_IDLE_WIN - IDLE Messaging Register for Wi-Di	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	16
Address:	08014h
Message registers have bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16]. In order to set bit0, for example, the data would be 0x0001_0001. In order to clear bit0, for example, the data would be 0x0001_0000. Note that mask bit is the data bit offset + 16. Message registers are protected from non-GT writes via the Message Channel.	

DWord	Bit	Description	
0	15:5	**Reserved**	
		Access:	RO
	4	**Preparation for Reset Acknowledgement**	
		Access:	R/W
		Go Acknowledgement 1'b0 : Go=0 Ack <default> 1'b1 : Go=1 Ack Requirement is that when Go=0 request is sent, the agent has to indicate busy before sending the Go=0 acknowledgement. It can only go idle again once Go=1 is received.	
	3:0	**Idle Messaging**	
		Access:	R/W
		Idle Messaging Bit[3] Secondary Pipe Clock Gating 1'b0 : Secondary pipe clock must be on <default> 1'b1 : Secondary pipe clock may be gated Bit[2] Primary Pipe Clock Gating 1'b0 : Primary pipe clock must be on <default> 1'b1 : Primary pipe clock may be gated Bit[1] C6 Allowed 1'b0 : Do not allow GT to enter C6 <default> 1'b1 : GT may enter C6 Bit[0] Idle Indication 1'b0 : Pipe is busy <default>	

MSG_IDLE_WIN - IDLE Messaging Register for Wi-Di		
		1'b1 : Pipe is idle ** See "Valid Combinations for Idle Messaging" Table

Idle Switch Delay

IDLEDLY - Idle Switch Delay	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	0223Ch
Address:	1223Ch-1223Fh
Name:	Idle Switch Delay
ShortName:	IDLEDLY_VCSUNIT0
Address:	1A23Ch-1A23Fh
Name:	Idle Switch Delay
ShortName:	IDLEDLY_VECSUNIT
Address:	1C23Ch-1C23Fh
Name:	Idle Switch Delay
ShortName:	IDLEDLY_VCSUNIT1
Address:	2223Ch-2223Fh
Name:	Idle Switch Delay
ShortName:	IDLEDLY_BCSUNIT

The IDLEDLY register contains an Idle Delay field which specifies the minimum number of microseconds allowed for command streamer to wait before a context is switched out leading to IDLE state in Execlist mode, i.e following this context switch there is no active element available in HW to execute.
A default value of 0, means that by default, there is no restriction to wait on a context switch leading to IDLE. This register has no significance when Execlists are not enabled.

DWord	Bit	Description	
0	31:21	**Reserved**	
		Format:	MBZ
	20:0	**IDLE Delay**	
		Project:	All
		Format:	U21
		Minimum number of micro-seconds allowed	

Indirect Context Offset Pointer

INDIRECT_CTX_OFFSET - Indirect Context Offset Pointer	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x000005C0 CHV, BSW
Access:	R/W
Size (in bits):	32
Trusted Type:	1

Address:	021C8h-021CBh
Name:	Indirect Context Offset Pointer
ShortName:	INDIRECT_CTX_OFFSET_RCSUNIT

Address:	121C8h-121CBh
Name:	Indirect Context Offset Pointer
ShortName:	INDIRECT_CTX_OFFSET_VCSUNIT0

Address:	1A1C8h-1A1CBh
Name:	Indirect Context Offset Pointer
ShortName:	INDIRECT_CTX_OFFSET_VECSUNIT

Address:	1C1C8h-1C1CBh
Name:	Indirect Context Offset Pointer
ShortName:	INDIRECT_CTX_OFFSET_VCSUNIT1

Address:	221C8h-221CBh
Name:	Indirect Context Offset Pointer
ShortName:	INDIRECT_CTX_OFFSET_BCSUNIT

This register is used to program the offset where commands RCS_INDIRECT_CTX points to will be executed as part of engine context restore.

Programming Notes	Project
Offset of Indirect CS context must be made programmable only for debug purposes.	
Offset of Indirect CS context must be always programmed to a command boundary and cacheline boundary inside the context image.	
Indirect context pointer itself is restored during context restore and hence Indirect Context Offset must not be programmed with value less than 0x5.	
Must not be programmed to 0x5, 0x6A as these fall on arbitration boundaries.	CHV, BSW

DWord	Bit	Description
0	31:16	**Reserved**

INDIRECT_CTX_OFFSET - Indirect Context Offset Pointer

		Format:		MBZ

	15:6	**Offset of Indirect CS Context**		

		Format:		U10

This is the cache line offset for the Indirect CS context. This defaults to execute between CS and SVG context. It is not valid to program this to a value that is greater or equal to the starting offset for RS context. If context must be programmed at the end of engine context then program then use BB_PER_CTX_PTR.

Value	Name	Project
17h	**[Default]**	CHV, BSW

	5:0	**Reserved**	

		Format:	MBZ

Indirect Context Pointer

<table>
<tr><td colspan="2" align="center">**INDIRECT_CTX - Indirect Context Pointer**</td></tr>
<tr><td>Register Space:</td><td>MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td>CHV, BSW</td></tr>
<tr><td>Source:</td><td>PRM</td></tr>
<tr><td>Default Value:</td><td>0x00000000</td></tr>
<tr><td>Access:</td><td>R/W</td></tr>
<tr><td>Size (in bits):</td><td>32</td></tr>
<tr><td>Trusted Type:</td><td>1</td></tr>
<tr><td>Address:</td><td>021C4h-021C7h</td></tr>
<tr><td>Name:</td><td>Indirect Context Pointer</td></tr>
<tr><td>ShortName:</td><td>INDIRECT_CTX_RCSUNIT</td></tr>
<tr><td>Address:</td><td>121C4h-121C7h</td></tr>
<tr><td>Name:</td><td>Indirect Context Pointer</td></tr>
<tr><td>ShortName:</td><td>INDIRECT_CTX_VCSUNIT0</td></tr>
<tr><td>Address:</td><td>1A1C4h-1A1C7h</td></tr>
<tr><td>Name:</td><td>Indirect Context Pointer</td></tr>
<tr><td>ShortName:</td><td>INDIRECT_CTX_VECSUNIT</td></tr>
<tr><td>Address:</td><td>1C1C4h-1C1C7h</td></tr>
<tr><td>Name:</td><td>Indirect Context Pointer</td></tr>
<tr><td>ShortName:</td><td>INDIRECT_CTX_VCSUNIT1</td></tr>
<tr><td>Address:</td><td>221C4h-221C7h</td></tr>
<tr><td>Name:</td><td>Indirect Context Pointer</td></tr>
<tr><td>ShortName:</td><td>INDIRECT_CTX_BCSUNIT</td></tr>
</table>

This register is used to program the indirect address to be executed between CS and SVG engine context if enabled. This will only get executed due to regular context save/restore and not during power restore. This register is part of the execution list context and will be executed per context. Only supported if execution list is enabled. There is no preempting workloads within this context.

Programming Notes	Source
The following commands are not supported within Render CS indirect context:	RenderCS

Command Name
MI_WAIT_FOR_EVENT
MI_SEMAPHORE_SIGNAL
MI_ARB_CHECK
MI_RS_CONTROL
MI_REPORT_HEAD

INDIRECT_CTX - Indirect Context Pointer

MI_URB_ATOMIC_ALLOC	
MI_SUSPEND_FLUSH	
MI_TOPOLOGY_FILTER	
MI_RS_CONTEXT	
MI_SET_CONTEXT	
MI_URB_CLEAR	
MI_SEMAPHORE_WAIT in Memory Poll Mode is not supported. [BXT]: MI_SEMAPHORE_WAIT in register poll mode is supported.	
MI_BATCH_BUFFER_START	
MI_CONDITIONAL_BATCH_BUFFER_END	
MEDIA_OBJECT_WALKER	
GPGPU_WALKER	
3DPRIMITIVE	
3DSTATE_BINDING_TABLE_POINTERS_VS	
3DSTATE_BINDING_TABLE_POINTERS_HS	
3DSTATE_BINDING_TABLE_POINTERS_DS	
3DSTATE_BINDING_TABLE_POINTERS_GS	
3DSTATE_BINDING_TABLE_POINTERS_PS	
3DSTATE_GATHER_CONSTANT_VS	
3DSTATE_GATHER_CONSTANT_GS	
3DSTATE_GATHER_CONSTANT_HS	
3DSTATE_GATHER_CONSTANT_DS	
3DSTATE_GATHER_CONSTANT_PS	
3DSTATE_DX9_CONSTANTF_VS	
3DSTATE_DX9_CONSTANTF_HS	
3DSTATE_DX9_CONSTANTF_DS	
3DSTATE_DX9_CONSTANTF_GS	
3DSTATE_DX9_CONSTANTF_PS	
3DSTATE_DX9_CONSTANTI_VS	
3DSTATE_DX9_CONSTANTI_HS	
3DSTATE_DX9_CONSTANTI_DS	
3DSTATE_DX9_CONSTANTI_GS	
3DSTATE_DX9_CONSTANTI_PS	
3DSTATE_DX9_CONSTANTB_VS	
3DSTATE_DX9_CONSTANTB_HS	

INDIRECT_CTX - Indirect Context Pointer

3DSTATE_DX9_CONSTANTB_DS	
3DSTATE_DX9_CONSTANTB_GS	
3DSTATE_DX9_CONSTANTB_PS	
3DSTATE_DX9_LOCAL_VALID_VS	
3DSTATE_DX9_LOCAL_VALID_DS	
3DSTATE_DX9_LOCAL_VALID_HS	
3DSTATE_DX9_LOCAL_VALID_GS	
3DSTATE_DX9_LOCAL_VALID_PS	
3DSTATE_DX9_GENERATE_ACTIVE_VS	
3DSTATE_DX9_GENERATE_ACTIVE_HS	
3DSTATE_DX9_GENERATE_ACTIVE_DS	
3DSTATE_DX9_GENERATE_ACTIVE_GS	
3DSTATE_DX9_GENERATE_ACTIVE_PS	
3DSTATE_BINDING_TABLE_EDIT_VS	
3DSTATE_BINDING_TABLE_EDIT_GS	
3DSTATE_BINDING_TABLE_EDIT_HS	
3DSTATE_BINDING_TABLE_EDIT_DS	
3DSTATE_BINDING_TABLE_EDIT_PS	
3DSTATE_CONSTANT_VS	
3DSTATE_CONSTANT_GS	
3DSTATE_CONSTANT_PS	
3DSTATE_CONSTANT_HS	
3DSTATE_CONSTANT_DS	
MI_BATCH_BUFFER_END	

INDIRECT_CTX - Indirect Context Pointer

Workaround
Workaround: [Render CS Only][Execlist Mode of Scheduling]: SW must ensure arbitration is switched off while context restore is in progress for any given context. This is achieved by disabling arbitration by programming MI_ARB_ON_OFF to "Arbitration Disable" in RCS_INDIRECT_CTX buffer and by enabling back the arbitration by programming MI_ARB_ON_OFF to "Arbitration Enable" as the last command prior to MI_BATCH_END in the BB_PER_CTX_PTR buffer of every context submitted. Note that RCS_INDIRECT_CTX_OFFSET could be set to default value or any other legitimate value as per the programming notes of the register definition. Arbitration disable by programming MI_ARB_ON_OFF (Arbitration Disabled) in RCS_INDIRECT_CTX buffer. Arbitration enabled by programming MI_ARB_ON_OFF (Arbitration Enabled) as the last command prior to MI_BATCH_BUFFER_END in BB_PER_CTX_PTR buffer. Additional Note: This WA need not be applied when it is guaranteed for no preemption to occur during execution of GPGPU workload. Preemption of GPGPU workload can be avoided by Bracketing the GPGPU workload with MI_ARB_ON_OFF (Arbitration Disable) and MI_ARB_ON_OFF (Arbitration Enable) command. MI_ARB_ON_OFF is a privileged command and can only be programmed in ring buffer or in privileged batch buffer (batch buffer in GGTT memory). Pending execlist submitted must not trigger preemption of the ongoing GPGPU workload due to following reasons First context of the pending execlist submitted is not the same as the ongoing GPGPU context. Force restore bit set for the submitted pending execlist.

DWord	Bit	Description
0	31:6	**Indirect CS Context Address** Format: GraphicsAddress[31:6] Pointer to the Context in memory to be executed as a batch.
	5:0	**Size of Indirect CS Context** Format: U6 This is the size of the Indirect Context for CS. This size supports up to 63 cache lines worth of commands where a cache line is 64B. If programmed to zero then the indirect fetch of the CS context is disabled. **Value** / **Name** [0,63]

Instruction Parser Mode Register

INSTPM - Instruction Parser Mode Register	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00004080 [CHV:B, CHV:C, CHV:K]
	0x00006080 [CHV:A]
Access:	R/W, RO
Size (in bits):	32
Trusted Type:	1
Address:	020C0h
Address:	120C0h-120C3h
Name:	Instruction Parser Mode Register
ShortName:	INSTPM_VCSUNIT0
Address:	1A0C0h-1A0C3h
Name:	Instruction Parser Mode Register
ShortName:	INSTPM_VECSUNIT
Address:	1C0C0h-1C0C3h
Name:	Instruction Parser Mode Register
ShortName:	INSTPM_VCSUNIT1
Address:	220C0h-220C3h
Name:	Instruction Parser Mode Register
ShortName:	INSTPM_BCSUNIT

The INSTPM register is used to control the operation of the Instruction Parser. Certain classes of instructions can be disabled (ignored) - often useful for detecting performance bottlenecks. Also, Synchronizing Flush operations can be initiated - useful for ensuring the completion (vs. only parsing) of rendering instructions.

Programming Notes
• If an instruction type is disabled, the parser will read those instructions but not process them. • Error checking will be performed even if the instruction is ignored. • All Reserved bits are implemented. • This Register is saved and restored as part of Context.

DWord	Bit	Description

| 0 | 31:16 | **Mask Bits** |

| | | Format: | Mask[15:0] |

 Masks: These bits serve as write enables for bits 15:0. If this register is written with any of these bits clear the corresponding bit in the field 15:0 will not be modified. Reading these bits always returns 0s.

| | 15 | **Reserved** |

		Project:	CHV, BSW
		Access:	RO
		Format:	MBZ

| | 14 | **Replay Mode** |

| | | Project: | CHV, BSW |
| | | Format: | U1 |

This field controls the granularity of the replay mechanism when coming back into a previously preempted context.

Value	Name	Description
1h	Object Level Preemption **[Default]**	Object Level. Preemption is done on an Object Level Boundary in VF. Objects send down by VF are completely rendered. Pipeline is flushed before switching to the next context. On resubmission of the context VF starts parsing form the object where it got preempted last time.
0h		Drawcall Level. Pipeline is flushed before switching to the next context. Commands parsed are committed to completing before a context switch.

Programming Notes
This bit ust be set to 0 prior to any 3DPRIMITVE using trifan, polygon, lineloop or quadstrip topology. This bit ust be set to 0 prior to any 3DPRIMITVE using linestrip_adjacency and 3dstate_GS.enable is set to 1.

| | 14:13 | **Reserved** |

		Default Value:	11b
		Project:	CHV, BSW
		Format:	Must Be One

| | 13 | **Reserved** |

| | | Project: | CHV, BSW |
| | | Format: | Must Be One |

| | 12 | **Reserved** |

| | | Project: | CHV, BSW |

| | 11 | **CLFLUSH Toggle** |

DWord	Bit	Description

		Project:	CHV, BSW
		Access:	RO
		Format:	U1
		This bit changes polarity each time the MI_CLFLUSH command completes. This bit is Read Only.	

	10	**Implied Atomic Fences To Write Fences**	
		Project:	CHV, BSW
		Format:	U1
		If set, all implied atomic fences generated by Render Command Streamer during various operations (Flushes, Context Switch) are converted to regular write fences. Setting this bit will affect data ordering functionality and must be only used in debug mode. When reset HW behaves as expected.	

	9:8	**Reserved**	
		Project:	CHV, BSW
		Format:	MBZ

	7	**Force Sync Command Ordering**	
		Default Value:	1b
		Project:	CHV, BSW
		Format:	Enable
		By default, driver/OS synchronization commands (MI_STORE_DATA_IMM, for instance) can execute out of order with respect to 3D state and 3D primitive commands. When set, this bit forces ordering of these commands. See section 3.2.2 for a list of these commands.	

	6	**CONSTANT_BUFFER Address Offset Disable**	
		Project:	CHV, BSW
		Format:	Disable
		When this bit is clear, the 3DSTATE_CONSTANT_* Buffers' Starting Address is used as a DynamicStateOffset. That is, it serves as an offset from the Dynamic State Base Address. Accesses will be subject to Dynamic State bounds checking. When this bit is set, the 3DSTATE_CONSTANT_* Buffers' Starting Address is used as a true GraphicsAddress (not an offset). No bounds checking will be performed during access.	

	5	**Reserved**	
		Project:	CHV, BSW
		Format:	MBZ

	4	**Reserved**	
		Project:	CHV, BSW

DWord	Bit	Description
	3	**Media Instruction Disable**
		Project: CHV, BSW
		Format: U1
		This bit instructs the Renderer instruction parser to parse and error-check Media instructions, but not execute them. Format = Disable
	2	**3D Rendering Instruction Disable**
		Project: CHV, BSW
		Format: U1
		This bit instructs the Renderer instruction parser to parse and error-check 3D Rendering instructions, but not execute them. This bit must always be set by software if 3D State Instruction Disable is set. Setting this bit without setting 3D State Instruction Disable is allowed. Format = Disable
	1	**3D State Instruction Disable**
		Project: CHV, BSW
		Format: Disable
	0	**Texture Palette Load Instruction Disable**
		Project: CHV, BSW
		Format: U1
		This bit instructs the Renderer instruction parser to parse and error-check Texture Palette Load instructions, but not execute them. Format = Disable

Internal GAM State

INTSTATE - Internal GAM State		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	040C0h	

DWord	Bit	Description
0	31:0	**Reserved**

INTERRUPT LINE

<table>
<tr><td colspan="3" align="center">**INTRLINE - INTERRUPT LINE**</td></tr>
<tr><td>Register Space:</td><td colspan="2">PCI: 0/2/0</td></tr>
<tr><td>Project:</td><td colspan="2">CHV, BSW</td></tr>
<tr><td>Source:</td><td colspan="2">PRM</td></tr>
<tr><td>Default Value:</td><td colspan="2">0x00000100</td></tr>
<tr><td>Size (in bits):</td><td colspan="2">16</td></tr>
<tr><td>Address:</td><td colspan="2">0003Ch</td></tr>
<tr><td colspan="3">3C - Interrupt. This register is programmed by SBIOS. It is not used by the graphics/display driver. This 8-bit register is used to communicate interrupt line routing information. It is read/write and must be implemented by the device. POST software will write the routing information into this register as it initializes and configures the system.
The value in this register tells which input of the system interrupt controller(s) the device's interrupt pin is connected to. The device itself does not use this value, rather it is used by device drivers and operating systems to determine priority and vector information.
3D - Interrupt. This register is programmed by SBIOS. It is not used by the graphics/display driver</td></tr>
</table>

DWord	Bit	Description		
0	15:8	**INTERRUPT_PIN**		
		Default Value:		01h
		Access:		RO
		IPIN: Value indicates which interrupt pin this device uses. 01h: INTA		
	7:0	**INTRLINE**		
		Default Value:		00h
		Access:		R/W
		ILIN: BIOS written value to communicate interrupt line routing information to the device driver. Used to communicate interrupt line routing information. POST software writes the routing information into this register as it initializes and configures the system. The value in this register indicates to which input of the system interrupt controller the device's interrupt pin is connected.		

Interrupt Mask Register

IMR - Interrupt Mask Register	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0xFFFFFFFF
Access:	R/W, RO
Size (in bits):	32
Address:	020A8h
Address: Name: ShortName:	120A8h-120ABh Interrupt Mask Register IMR_VCSUNIT0
Address: Name: ShortName:	1A0A8h-1A0ABh Interrupt Mask Register IMR_VECSUNIT
Address: Name: ShortName:	1C0A8h-1C0ABh Interrupt Mask Register IMR_VCSUNIT1
Address: Name: ShortName:	220A8h-220ABh Interrupt Mask Register IMR_BCSUNIT

The IMR register is used by software to control which Interrupt Status Register bits are masked or unmasked. Unmasked bits will be reported in the IIR, possibly triggering a CPU interrupt, and will persist in the IIR until cleared by software. Masked bits will not be reported in the IIR and therefore cannot generate CPU interrupts.

DWord	Bit	Description
0	31:0	**Interrupt Mask Bits**

Format:	InterruptMask[32] Refer to the Interrupt Control Register section for bit definitions.

This field contains a bit mask which selects which interrupt bits (from the ISR) are reported in the IIR. Reserved bits in the Interrupt Control Register are RO.

Value	Name	Description
FFFF FFFFh	**[Default]**	
0h	Not Masked	Will be reported in the IIR
1h	Masked	Will not be reported in the IIR

IOBAR

<table>
<tr><td colspan="3" align="center">**IOBAR - IOBAR**</td></tr>
<tr><td>Register Space:</td><td colspan="2">PCI: 0/2/0</td></tr>
<tr><td>Project:</td><td colspan="2">CHV, BSW</td></tr>
<tr><td>Source:</td><td colspan="2">PRM</td></tr>
<tr><td>Default Value:</td><td colspan="2">0x00000001</td></tr>
<tr><td>Size (in bits):</td><td colspan="2">32</td></tr>
<tr><td>Address:</td><td colspan="2">00020h</td></tr>
<tr><td colspan="3">I/O Base Address. This is used only by SBIOS. This register is the base address for the MMIO_INDEX and MMIO_DATA registers.</td></tr>
<tr><td colspan="3">This register provides the Base offset of the I/O registers within Device #2. Access to the 8Bs of IO space is allowed in PM state D0 when IO Enable (PCICMD bit 0) set. Access is disallowed :
* in PM states D1-D3 or
* if IO Enable is clear or
* if Device #2 is turned off or
* if Internal graphics is disabled thru the fuse or fuse override mechanisms.
Note that access to this IO BAR is independent of VGA functionality within Device #2.
If accesses to this IO bar is allowed then the GMCH claims all 8, 16 or 32 bit IO cycles from the CPU that falls within the 8B claimed.</td></tr>
</table>

DWord	Bit	Description
0	31:16	**RESERVED**
		Default Value: 0000h
		Access: RO
		Reserved
	15:6	**BASE_ADDRESS**
		Default Value: 0000h
		Access: R/W
		BA: Set by the OS, these bits correspond to address signals [15:6]. IOBAR is to be used for both GTLC register programming and GTT table programming. This is an indirect access method.
	5:1	**RESERVED**
		Default Value: 0h
		Access: RO
	0	**RESOURCE_TYPE_RTE**
		Default Value: 1b
		Access: RO
		Indicates a request for I/O space

L3 Bank Status

<table>
<tr><td colspan="3" align="center">**L3STAT - L3 Bank Status**</td></tr>
<tr><td colspan="3">Register Space: MMIO: 0/2/0</td></tr>
<tr><td colspan="3">Project: CHV, BSW</td></tr>
<tr><td colspan="3">Source: PRM</td></tr>
<tr><td colspan="3">Default Value: 0x00000000</td></tr>
<tr><td colspan="3">Size (in bits):   32</td></tr>
<tr><td colspan="3">Address: 0B128h</td></tr>
<tr><td colspan="3">L3 Status register</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td>**Description**</td></tr>
<tr><td>0</td><td>31</td><td>**L3 Fill Access Status bit**
Access: RO
This register is Hardware Set and Clear.
Set condition: set when the first command is seen on LTCC-LTCD interface.
Reset condition: reset when the first Pipeline Flush command is seen on the LTCC-LTCD interface.
Reset condition: This Flag will be reset only if we have atleast 1 modified line in the cache written by DC client.</td></tr>
<tr><td></td><td>30:0</td><td>**Reserved**
Project: CHV, BSW
Access: RO</td></tr>
</table>

L3CD Error Status register 1

L3CDERRST - L3CD Error Status register 1		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000080	
Size (in bits):	32	
Address:	0B1F0h	

DWord	Bit	Description
0	31:25	**Reserved** Access: RO
	24	**Double bit ECC error detected** Default Value: 0b Access: R/W One Clear Indicates if bank detected a double bit ECC error. When ltcd_lbcf_ecc_2bit_err_valid is set.
	23:14	**Parity row address error** Default Value: 0000000000b Access: R/W One Clear Data array address which has parity B1. Report the data array address which has the Error. ltcd_lbcf_parity_err_rownum[9:0].Once set by HW, it can be cleared only by MMIO Write of 1 to this register bit 13. Driver needs to write 1 to clear this bit.
	13	**Parity Error Valid** Access: R/W One Clear Parity Error valid. Report the Parity Error. ltcd_lbcf_parity_err_valid. Once set by HW, it can be cleared only by MMIO Write of 1 to this register bit 13. Driver needs to write 1 to clear this bit. when ltcd_lbcf_parity_err_valid is asserted, lbcf generates interrupt to ltiseqsl lbcf_ltiseqsl_parity_intr.
	12:11	**Parity error bank number** Access: R/W One Clear bank number which has parity error. Report the bank no. which has the Error. ltcd_lbcf_parity_err_banknum[1:0].Once set by HW, it can be cleared only by MMIO Write of 1 to this register bit 13. Driver needs to write 1 to clear this bit.

L3CDERRST - L3CD Error Status register 1

	10:8	**Parity Error sub-bank no**		
		Access:		R/W One Clear
		Parity Error in sub bank: ltcd0_lbcf_parity_err_subanknum[2:0].Once set by HW, it can be cleared only by MMIO Write of 1 to this register bit 13. Driver needs to write 1 to clear this bit.		
	7	**Parity report enable**		
		Default Value:		1b
		Access:		R/W
		Parity report enable (LCPRTYRPTEN): lbcf_csr_lc_parity_report_en. This is the parity reporting enable, by default it is enabled. When enabled parity is reported by ltcd to sarb. When disabled by driver, ltcd should not send out any parity error to SARB. Driver needs to write 1 to clear this bit.		
	6:0	**Reserved**		
		Access:		RO

L3 Control Register

L3CNTLREG - L3 Control Register	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000 CHV, BSW
Access:	R/W
Size (in bits):	32
Address:	07034h

Programming Notes	**Project**
The L3 allocation programming should assign all ways of the cache with no left over ways. Refer to L3 section for the recommended settings.	
Any L3 configuration change that reduces the data cache allocation when strong IA coherency is used requires the full flush of L3 prior to the programming update. An explicit or implicit flush of L3 (DC Flush) through the command streamer doesn't result in flushing/invalidating the IA Coherent lines from L3. However this can be achieved by setting the "**Pipe line flush Coherent lines**" control bit in the "L3SQCREG4" register.	
SLM comes up in an in-consistent state post reconfiguration and must be initialized by the driver for proper parity generation	CHV, BSW

DWord	**Bit**	**Description**
0	31:25	**All L3 Client Pool**

Project:	All
Access:	R/W

Number of ways allocated for the all client pool. This is a combined pool for all clients.

Value	**Name**	**Project**
30h	**[Default]**	CHV, BSW

Programming Notes
When this field is non-zero, **DC Way Assignment** and **Read Only Client Pool** should be 0KB. Odd number values are not allowed. **Please refer to L3 Section with Allocation and Programming for recommended settings.**

	24:18	**DC Way Assignment**

Project:	All
Access:	R/W

Number of ways allocated for DC. Note this allocation is only for DC data types.

Programming Notes
Note: This field must be 0KB if All L3 Client Pool is non-zero. Odd number values are not allowed. **Please refer to L3 HAS for valid programming values**

L3CNTLREG - L3 Control Register

17:11	**Read Only Client Pool**	
	Project:	All
	Access:	R/W

Number of ways allocated for Read Only L3 clients. This is a combined pool for all Read Only clients.

Programming Notes
Note: This field must be 0KB if All L3 Client Pool is non-zero. Odd number values are not allowed. **Please refer to L3 HAS for valid programming values**

10	**Reserved**	
	Access:	R/W
	Format:	PBC

9	**Error Detection Behavior Control**	
	Project:	CHV, BSW
	Access:	R/W
	Format:	Enable

The L3 error detection can be enabled to hang the GPU on a non-recoverable error due to SER type events. Such option will be used when corresponding context has data consistency requirements. Once error detection is enabled, s/w has to initialize URB or SLM to all 0's (based on usage model) prior to execution of the workload. Initialization is required to clean up the error detection logic and syndrome tracking.

Value	Name	Description	Project
0h	**[Default]**	RTL does not hang on parity errors or double bit error	CHV, BSW
1h		RTL enforces a hang on parity errors or double bit error	CHV, BSW

8	**GPGPU L3 Credit Mode Enable**	
	Project:	All
	Access:	R/W
	Format:	Enable

This bit is required to be enabled under GPGPU workloads to provide the MAX latency coverage from L3 cache. It will override the registers 0xB100[18:14] and 0xB100[23:19], to 0 and the maximum value respectively.

7:1	**URB Allocation**	
	Project:	All
	Access:	R/W

Number of ways allocated for URB usage

Value	Name	Project
30h	**[Default]**	CHV, BSW

Programming Notes
Odd number values are not allowed. **Please refer to L3 HAS for valid programming values**

L3CNTLREG - L3 Control Register		
	0	**SLM Mode Enable**
		Project: All
		Access: R/W
		Format: Enable
		When enabled, a 64KB (per bank) region of L3 is reserved for SLM.

L3 Control Register1

L3CNTLREG1 - L3 Control Register1	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x8C47FF80 CHV, BSW
Size (in bits):	32
Address:	0B10Ch

DWord	Bit	Description
0	31:28	**Data Fifo Depth Control**

Access: R/W

Data Fifo Depth Control (TS mode).

Value cannot be zero for normal operation.
lbcf_csr_lc_datafifo_depth[3:0].

Value	Name	Project
1000b	**[Default]**	CHV, BSW

27:24 Data Clock off time

Default Value:	1100b
Access:	R/W

Data Clock off time (DATACLKOFF):
Data Clock off time - Data block is shut off after these many number of clocks programmed in this register bits.
lbcf_csr_lc_dataclkoff_time[3:0].Min value to be 4'h0100.
It should be between 4'h4 : 4'hf.

23:20 TAG CLK OFF TIME

Default Value:	0100b
Access:	R/W

19 L3 Aging Disable Bit

Default Value:	0b
Access:	R/W

L3 Aging Disable Bit (L3AGDIS):
Aging Disable.
lbcf_csr_lc_agingdis.

18:15 Fill aging

Default Value:	1111b

L3CNTLREG1 - L3 Control Register1

		Access:		R/W

Fill aging (L3AGF):
Aging Counter for Fill.
lbcf_csr_lc_fill_aging_cnt[3:0].If bit B103.19 is 0 then this register value has to be nonzero.

14:11	**Aging Counter for Read 1 Port**		
	Default Value:		1111b
	Access:		R/W

Aging Counter for Read 1 Port (L3AGR1):
Aging Counter for Read 1 Port.
lbcf_csr_lc_r1_aging_cnt[3:0].If bit B103.19 is 0 then this register value has to be nonzero.

10:7	**L3 Aging Counter for R0**		
	Default Value:		1111b
	Access:		R/W

L3 Aging Counter for R0 (L3AGR0):
Aging Counter for R0 Port.
lbcf_csr_lc_r0_aging_cnt[3:0].If bit B103.19 is 0 then this register value has to be nonzero.

6:0	**Reserved**		
	Default Value:		000000b
	Project:		CHV, BSW
	Access:		RO

Reserved.

L3 LRA 0

	L3_LRA_0 - L3 LRA 0	
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x0E037C00	
Size (in bits):	32	
Exists If:	Device[Platform] == 'Client'	
Address:	04A10h	

DWord	Bit	Description	
0	31:30	**L3**	
		Default Value:	00b
		Access:	R/W
		Which LRA should L3 use.	
	29:20	**L3 LRA1 Min**	
		Default Value:	0011100000b
		Access:	R/W
		Minimum value of programmable LRA1.	
	19:10	**L3 LRA0 Max**	
		Default Value:	0011011111b
		Access:	R/W
		Maximum value of programmable LRA0.	
	9:0	**L3 LRA0 Min**	
		Default Value:	0000000000b
		Access:	R/W
		Minimum value of programmable LRA0.	

L3 LRA 0 GPGPU

L3_LRA_0_GPGPU - L3 LRA 0 GPGPU		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x0400FC00	
Size (in bits):	32	
Address:	04DD0h	

DWord	Bit	Description	
0	31:30	**L3 GPGPU**	
		Default Value:	00b
		Access:	R/W
		Which LRA should L3 use.	
	29:20	**L3 LRA1 Min GPGPU**	
		Default Value:	0001000000b
		Access:	R/W
		Minimum value of programmable LRA1.	
	19:10	**L3 LRA0 Max GPGPU**	
		Default Value:	0000111111b
		Access:	R/W
		Maximum value of programmable LRA0.	
	9:0	**L3 LRA0 Min GPGPU**	
		Default Value:	0000000000b
		Access:	R/W
		Minimum value of programmable LRA0.	

L3 LRA 1

L3_LRA_1 - L3 LRA 1		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x67F701BF	
Size (in bits):	32	
Exists If:	Device[Platform] == 'Client'	
Address:	04A14h	

DWord	Bit	Description	
0	31:30	**DC**	
		Default Value:	01b
		Access:	R/W
		Which LRA should DC use.	
	29:20	**L3 LRA2 Max**	
		Default Value:	1001111111b
		Access:	R/W
		Maximum value of programmable LRA2.	
	19:10	**L3 LRA2 Min**	
		Default Value:	0111000000b
		Access:	R/W
		Minimum value of programmable LRA2.	
	9:0	**L3 LRA1 Max**	
		Default Value:	0110111111b
		Access:	R/W
		Maximum value of programmable LRA1.	

L3 LRA 1 GPGPU

L3_LRA_1_GPGPU - L3 LRA 1 GPGPU	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x5FF6C1AF
Size (in bits):	32
Address:	04DD4h

DWord	Bit	Description	
0	31:30	**DC GPGPU**	
		Default Value:	01b
		Access:	R/W
		Which LRA should DC use.	
	29:20	**L3 LRA2 Max GPGPU**	
		Default Value:	0111111111b
		Access:	R/W
		Maximum value of programmable LRA2.	
	19:10	**L3 LRA2 Min GPGPU**	
		Default Value:	0110110000b
		Access:	R/W
		Minimum value of programmable LRA2.	
	9:0	**L3 LRA1 Max GPGPU**	
		Default Value:	0110101111b
		Access:	R/W
		Maximum value of programmable LRA1.	

L3 LRA 2

L3_LRA_2 - L3 LRA 2		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000002	
Size (in bits):	32	
Exists If:	Device[Platform] == 'Client'	
Address:	04A18h	
DWord	**Bit**	**Description**
0	31:2	**Reserved**
		Default Value: 00000000000000000000000000000b
		Access: RO
	1:0	**Texture**
		Default Value: 10b
		Access: R/W
		Which LRA should Texture use.

L3 LRA 2 GPGPU

L3_LRA_2_GPGPU - L3 LRA 2 GPGPU		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000002	
Size (in bits):	32	
Address:	04DD8h	

DWord	Bit	Description
0	31:2	**Reserved**
		Default Value: 00000000000000000000000000000b
		Access: RO
	1:0	**Texture GPGPU**
		Default Value: 10b
		Access: R/W
		Which LRA should Texture use.

L3 LRA 0 3D

L3_LRA_0_3D - L3 LRA 0 3D	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x0400FC00
Size (in bits):	32
Address:	04A10h

DWord	Bit	Description	
0	31:30	**L3 3D**	
		Default Value:	00b
		Access:	R/W
		Which LRA should L3 use.	
	29:20	**L3 LRA1 Min 3D**	
		Default Value:	0001000000b
		Access:	R/W
		Minimum value of programmable LRA1.	
	19:10	**L3 LRA0 Max 3D**	
		Default Value:	0000111111b
		Access:	R/W
		Maximum value of programmable LRA0.	
	9:0	**L3 LRA0 Min 3D**	
		Default Value:	0000000000b
		Access:	R/W
		Minimum value of programmable LRA0.	

L3 LRA 1 3D

<table>
<tr><td colspan="3" align="center">**L3_LRA_1_3D - L3 LRA 1 3D**</td></tr>
<tr><td>Register Space:</td><td colspan="2">MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td colspan="2">CHV, BSW</td></tr>
<tr><td>Source:</td><td colspan="2">PRM</td></tr>
<tr><td>Default Value:</td><td colspan="2">0x5FF2408F CHV, BSW</td></tr>
<tr><td>Size (in bits):</td><td colspan="2">32</td></tr>
<tr><td>Address:</td><td colspan="2">04A14h</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td>**Description**</td></tr>
<tr>
<td>0</td>
<td>31:30</td>
<td>

DC 3D

Default Value:	01b
Access:	R/W

Which LRA should DC use.

</td>
</tr>
<tr>
<td></td>
<td>29:20</td>
<td>

L3 LRA2 Max 3D

Access:	R/W

Maximum value of programmable LRA2.

Value	Name	Project
0111111111b	**[Default]**	CHV, BSW

</td>
</tr>
<tr>
<td></td>
<td>19:10</td>
<td>

L3 LRA2 Min 3D

Default Value:	0010010000b
Access:	R/W

Minimum value of programmable LRA2.

</td>
</tr>
<tr>
<td></td>
<td>9:0</td>
<td>

L3 LRA1 Max 3D

Default Value:	0010001111b
Access:	R/W

Maximum value of programmable LRA1.

</td>
</tr>
</table>

L3 LRA 2 3D

L3_LRA_2_3D - L3 LRA 2 3D		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW, :GT2:B	
Source:	PRM	
Default Value:	0x00000002	
Size (in bits):	32	
Address:	04A18h	

DWord	Bit	Description
0	31:2	**Reserved**
		Default Value: 00000000000000000000000000000b
		Access: RO
	1:0	**Texture 3D**
		Default Value: 10b
		Access: R/W
		Which LRA should Texture use.

L3 Messaging Register

<table>
<tr><td colspan="3" align="center">**MSG_L3_LPFC - L3 Messaging Register**</td></tr>
<tr><td colspan="3">Register Space: MMIO: 0/2/0</td></tr>
<tr><td colspan="3">Project: CHV, BSW</td></tr>
<tr><td colspan="3">Source: PRM</td></tr>
<tr><td colspan="3">Default Value: 0x00000000</td></tr>
<tr><td colspan="3">Size (in bits):   16</td></tr>
<tr><td colspan="3">Address: 08038h</td></tr>
<tr><td colspan="3">Message registers have bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16]. In order to set bit0, for example, the data would be 0x0001_0001. In order to clear bit0, for example, the data would be 0x0001_0000. Note that mask bit is the data bit offset + 16. Message registers are protected from non-GT writes via the Message Channel.</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td>**Description**</td></tr>
<tr><td>0</td><td>15:2</td><td>**Reserved**

Access: RO</td></tr>
<tr><td></td><td>1</td><td>**Acknowledge that L3 Unblock Completed**

Access: R/W

Acknowledge that L3 Unblock Completed
1'b0 : L3 unblock not complete yet (default)
1'b1 : L3 unblock has completed
gpmunit self-clears this bit upon sampling.</td></tr>
<tr><td></td><td>0</td><td>**Acknowledge that L3 Flush and Block Completed**

Access: R/W

Acknowledge that L3 Flush and Block Completed
1'b0 : L3 flush and block not complete yet (default)
1'b1 : L3 flush and block has completed
gpmunit self-clears this bit upon sampling.</td></tr>
</table>

L3 SLM Register

<table>
<tr><th colspan="3">L3SLMREG - L3 SLM Register</th></tr>
<tr><td>Register Space:</td><td colspan="2">MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td colspan="2">CHV, BSW</td></tr>
<tr><td>Source:</td><td colspan="2">PRM</td></tr>
<tr><td>Default Value:</td><td colspan="2">0x40000000</td></tr>
<tr><td>Size (in bits):</td><td colspan="2">32</td></tr>
<tr><td>Address:</td><td colspan="2">0B110h</td></tr>
<tr><th>DWord</th><th>Bit</th><th>Description</th></tr>
<tr>
<td>0</td><td>31</td>
<td>

Disable Periodic SLM/SQ slot allocation

Default Value:	0b
Access:	R/W

Disable Periodic SLM/SQ slot allocation: When cfg_lslm_livelock_fairarb_dis=1 lslm unit always has the higher priority and lslm_lsqc_block to lsqcunit is asserted as long as there are requests in SLM FIFO.
lbcf_csr_lslm_livelock_fairarb_dis.

</td>
</tr>
<tr>
<td></td><td>30:26</td>
<td>

LSLM_SQ_PENDING_MAX

Default Value:	10000b
Access:	R/W

If lslmunit has read data to be sent to lcbrunit this cfg register specifies the maximum number of clocks for which LSLMunit can block SQ request from being sent o lcbrunit.
Default value = 8.
Value cannot be zero.
lbcf_csr_lslm_sqpend_max[4:0].

</td>
</tr>
<tr>
<td></td><td>25</td>
<td>

LSLM address disable

Default Value:	0b
Access:	R/W

Description
0 - Enable b2b addr matching fix. lslmunit should not block the cycle in fifo if there is a match in the pipeline. 1 - Disable b2b addr matching fix. lslmunit should block the cycle in fifo if there is a match in the pipeline. lbcf_csr_lslm_same_addr_dis. Default = 0.
Set this bit to 1'b1 to workaround Atomic b2b bug on SLM for CHV, BSW A-step only.

</td>
</tr>
<tr>
<td></td><td>24:0</td>
<td>

Reserved

Access:	RO

</td>
</tr>
</table>

L3 SQC register 4

<table>
<tr><td colspan="3" align="center">**L3SQCREG4 - L3 SQC register 4**</td></tr>
<tr><td colspan="3">Register Space: MMIO: 0/2/0</td></tr>
<tr><td colspan="3">Project: CHV, BSW</td></tr>
<tr><td colspan="3">Source: PRM</td></tr>
<tr><td colspan="3">Default Value: 0x40400000 CHV, BSW</td></tr>
<tr><td colspan="3">Size (in bits):   32</td></tr>
<tr><td colspan="3">Address: 0B118h</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td align="center">**Description**</td></tr>
<tr><td rowspan="4">0</td><td>31</td><td>**Reserved**</td></tr>
<tr><td>30</td><td>

L3SQ URB Read CAM Match Disable

Default Value:	1b
Access:	R/W

L3SQ URB Read CAM Match Disable (SQURBRDCAMDIS):
Disables the L3SQ Cam Match ability for URB Reads. By disabling, this allows a performance mode where URB reads are not dependent upon one another but only on any previous URB writes to the same address. This allows many URB reads to the same cacheline at any given time instead of serializing the requests.
1 = URB Read CAM matching is disabled; multiple URB reads to the same cacheline are allowed to be concurrent (default).
0 = URB Read CAM matching is enabled; multiple URB reads to the same cacheline are serialized.
lbcf_csr_lsqc_urbrdcam_dis.

</td></tr>
<tr><td>29:28</td><td>

Traffic regulation in LSQC for URB lookup traffic

Default Value:	00b
Access:	R/W

Traffic regulation in LSQC for URB lookup traffic (URB lookups are issued to ltcc these many clocks apart).
00b - Continuous.
01b - 4 clocks apart.
10b - 8 clocks apart.
11b - 16 clocks apart.
lbcf_lsqc_urb_traffic.

</td></tr>
<tr><td>27</td><td>

LQSC RO PERF DIS

Default Value:	0b
Access:	R/W

Default: 0.
when set, RO performance mode is disabled and all Reads proceed only after Parent recycles.
lbcf_csr_lsqc_roperf_dis.

</td></tr>
</table>

L3SQCREG4 - L3 SQC register 4

26	**Order Cam Snp Reject**	
	Default Value:	0b
	Access:	R/W

Default: 0.
when set, all slots resulting in matches to snp addr result in snprsp as REJECT instead of MISS.
lbcf_csr_lsqc_ordercam_snpreject.

25	**LQSC RW PERF DIS**	
	Default Value:	0b
	Access:	R/W

Default: 0.
0: Performance mode is enabled.
when set, Rd to RW performance mode is disabled and all cycles proceed only after Parent recycles.

lbcf_csr_lsqc_rwperf_dis.

24	**LSQC read rtrn local crdt pre-consume disable**	
	Default Value:	0b
	Access:	R/W

0 - Default, LSQD consumes the LNE local slicecredit when read return pending.
1 - LSQD consumes read rtrn credit in the clock it is ready to send read return data.
lbcf_csr_lsqd_rdtrn_precrdt_dis.

23	**LSQC Mem Write sqcam HITM response disable**	
	Default Value:	0b
	Access:	R/W

0 - Default.
1 - This disables any Memory Write from cache with HitM tag response to respond for SQCAMs.
lbcf_csr_lsqc_sqcam_l3tagrsphitm_dis.

22	**Non-IA coherent atomics enable**	
	Default Value:	1b
	Access:	R/W

0: Atomics in GTI.
1: Atomics in L3 (non-IA atomic) (default).
lbcf_csr_lsqc_glblatmcs_l3.
Value of this bit should be same as LNCF register bit 0xb008[0].Value of this bit should be same as LBCF register bit 0xb11c[8].

L3SQCREG4 - L3 SQC register 4		
21	**Pipe line flush Coherent lines**	
	Default Value:	0b
	Project:	CHV, BSW
	Access:	R/W
	1: Treat pipeline flush as invalidating even coherent lines along with non coherent lines . 0: Flush invalidates non coherent lines only. lbcf_csr_lsqc_pipeflush_coh.	
20:0	**Reserved**	
	Project:	CHV, BSW
	Access:	RO

L3 SQC registers 1

<table>
<tr><td colspan="3" align="center">**L3SQCREG1 - L3 SQC registers 1**</td></tr>
<tr><td>Register Space:</td><td colspan="2">MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td colspan="2">CHV, BSW</td></tr>
<tr><td>Source:</td><td colspan="2">PRM</td></tr>
<tr><td>Default Value:</td><td colspan="2">0x00810000 CHV, BSW</td></tr>
<tr><td>Size (in bits):</td><td colspan="2">32</td></tr>
<tr><td>Address:</td><td colspan="2">0B100h</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td align="center">**Description**</td></tr>
</table>

DWord	Bit	Description
0	31:24	**Reserved**

Access:	RO

Reserved.

	23:19	**L3SQ General Priority Credit Initialization**

Project:	CHV, BSW
Access:	R/W

Description
L3SQ General Priority Credit Initialization (SQGPCI): Number of general and high priority credits that SQ presents to L3 Arbiter blocks This inherently also determines the depth of the SQ; reduce the number of credits and SQ uses fewer slots. Any value not listed here is considered Reserved. Gen priority credits is always greater than high priority credits. When this register is programmed through KMD, the crclk DOP clk gating should be disabled before the programming and be enabled ~100 clocks after the programming is done. Value # General Credits 00000b 0 00001b 2 00010b 4 00011b 6 00100b 8 00101b 10 00110b 12 00111b

L3SQCREG1 - L3 SQC registers 1

<table>
<tr><td></td><td></td><td>
14
01000b
16
01001b
18
01010b
20
01011b
22
01100b
24 (default)
01101b
26
01110b
28
01111b
30
10000b
32
Other values are not possible.
Need to go up to 32 credits.
lbcf_csr_lsqc_gen_credit_init[4:0].
</td></tr>
<tr><td></td><td></td><td>
34
10010
36
10011
38
10100
40
Other values are not possible.
^M
need to go upto 40 credits
</td></tr>
</table>

Value	Name	Project
10000b	**[Default]**	CHV, BSW

18:14	**L3SQ High Priority Credit Initialization**

Default Value:	00100b
Project:	CHV, BSW
Access:	R/W

L3SQ High Priority Credit Initialization (SQHPCI):
Number of general and high priority credits that SQ presents to L3 Arbiter blocks. This inherently also determines the depth of the SQ; reduce the number of credits and SQ uses fewer slots.
Any value not listed here is considered Reserved.
gen priority credits is always greater than high priority credits.

L3SQCREG1 - L3 SQC registers 1

		When this register is programmed through KMD, the crclk DOP clk gating should be disabled before the programming and be enabled ~100 clocks after the programming is done. Value # High Pri Credits 00000b 0 00001b 2 00010b 4 00011b 6 00100b 8 (default) 00101b 10 00110b 12 00111b 14 01000b 16 01001b 18 01010b 20 01011b 22 01100b 24 01101b 26 01110b 28 01111b 30 10000b 32 Other values are not possible. lbcf_csr_lsqc_hp_credit_init[4:0].lbcf_csr_lsqc_hp_credit_init[4:0] ++ lbcf_csr_lsqc_gen_credit_init[4:0] should always be less than or equal to 32.
	13:10	**Reserved**
		Access:
		RO
		Reserved.

L3SQCREG1 - L3 SQC registers 1

	9	**L3SQ Read Once Enable for Sampler Client**	
		Access:	R/W
		L3SQ Read Once Enable for Sampler Client (SQROE): Enables Read Once indications to L3 Cache from SQ. Once enabled, any reads from Sampler client (MT) are sent as Read Once. 0 = (default) Reads from Sampler clients issue Read to L3 Cache. 1 = Reads from Sampler clients issue Read Once to L3 Cache. lbcf_csr_sampler_readonce_en.	
	8:6	**Reserved**	
		Access:	RO
		Reserved.	
	5:3	**L3SQ Outstanding L3 Fills**	
		Access:	R/W
		L3SQ Outstanding L3 Fills (SQOUTSL3F): Identifies the number of L3 Fills that can be outstanding before SQ throttles the fill requests to L3 Cache. This is not an exact limit, but instead it is used as a threshold to throttling. Once the fill count is greater than or equal to the threshold, then no fills are issued until the fill responses are received to bring the outstanding count back below the threshold. 000b = (default) No limit. 001b = 1 fill. 010b = 2 fills. 011b = 4 fills. 100b = 8 fills. 101b = 16 fills. 11Xb = Reserved. lbcf_csr_lsqc_outs_fill[2:0].	
	2:0	**L3SQ Outstanding L3 Lookups**	
		Access:	R/W
		L3SQ Outstanding L3 Lookups (SQOUTSL3L): Identifies the number of L3 lookups that can be outstanding before SQ throttles the lookup requests to L3 Cache. This is not an exact limit, but instead it is used as a threshold to throttling. once the lookup count is greater than or equal to the threshold, then no lookups are issued until the lookup responses are received to bring the outstanding count back below the threshold. 000b = (default) No limit. 001b = 1 lookup. 010b = 2 lookups. 011b = 4 lookups. 100b = 8 lookups. 101b = 16 lookups. 11Xb = Reserved. lbcf_csr_lsqc_outs_lookup[2:0].	

L3 SQC registers 2

L3SQCREG2 - L3 SQC registers 2		

Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00004567
Size (in bits):	32
Address:	0B104h

DWord	Bit	Description
0	31:17	**Reserved**
		Access: RO
		Reserved.
	16	**L3SQ Priority Selection Disable**
		Access: R/W
		Description
		L3SQ Priority Selection Disable (SQPRIDIS): Enables the use of priority selection based on client ID decodes. If disabled, all cycles in SQ are treated as same priority. 0 = (default) Priority selection is enabled. 1 = Priority selection is disabled. Should not be set when RO perf mode is enabled (by default this is enabled which is bit[27] of B118-B11Bh). lbcf_csr_priority_cnt_disable.
		Workaround: If this bit is set to 1 then the following bits in register B108-B10B should have identical values 29:28, 27:26, 25:24, 23:22, 21:20, 19:18, 17:16, 15:14, 13:12, 11:10, 9:8, 7:6, 5:4, 3:2, 1:0.
	15	**L3SQ Priority 3 Pool Count Disable**
		Access: R/W
		Description
		L3SQ Priority 3 Pool Count Disable (SQPRI3CNTDIS): When set, priority3 pool becomes unlimited. And priority3 pool count value should not be used in reset of the remaining counters. 0 = (default) Priority 3 pool count is enabled. 1 = Priority 3 pool count is disabled. Should not be set when RO perf mode is enabled (by default this is enabled which is bit[27] of B118-B11Bh). lbcf_csr_priority3_cnt_disable.

L3SQCREG2 - L3 SQC registers 2

		Workaround: If this bit is set to 1 then the following bits in register B108-B10B should have identical values 29:28, 27:26, 25:24, 23:22, 21:20, 19:18, 17:16, 15:14, 13:12, 11:10, 9:8, 7:6, 5:4, 3:2, 1:0.

14:12	**L3SQ Priority 3 Pool Counter**

Default Value:	100b
Access:	R/W

L3SQ Priority 3 Pool Counter (SQPRI3CNT):
The count of cycles is selected from priority3 pool before switching to other priority pools. Count is used as the power of 2.
000b = 1 request.
001b = 2 requests.
010b = 4 requests.
011b = 8 requests.
...
111b = 128 requests.
lbcf_csr_priority3_cnt[2:0].

11	**L3SQ Priority 2 Pool Count Disable**

Access:	R/W

Description
L3SQ Priority 2 Pool Count Disable (SQPRI2CNTDIS): When set, priority2 pool becomes unlimited. And priority2 pool count value should not be used in reset of the remaining counters. 0 = (default) Priority 2 pool count is enabled. 1 = Priority 2 pool count is disabled. Should not be set when RO perf mode is enabled (by default this is enabled which is bit[27] of B118-B11Bh). lbcf_csr_priority2_cnt_disable.
Workaround: If this bit is set to 1 then the following bits in register B108-B10B should have identical values 29:28, 27:26, 25:24, 23:22, 21:20, 19:18, 17:16, 15:14, 13:12, 11:10, 9:8, 7:6, 5:4, 3:2, 1:0.

10:8	**L3SQ Priority 2 Pool Counter**

Default Value:	101b
Access:	R/W

L3SQ Priority 2 Pool Counter (SQPRI2CNT):
The count of cycles is selected from priority2 pool before switching to other priority pools. Count is used as the power of 2.
000b = 1 request.
001b = 2 requests.
010b = 4 requests.
011b = 8 requests.
...
111b = 128 requests.

L3SQCREG2 - L3 SQC registers 2

		lbcf_csr_priority2_cnt[2:0].
	7	**L3SQ Priority 1 Pool Count Disable**

Access:	R/W

Description
L3SQ Priority 1 Pool Count Disable (SQPRI1CNTDIS): When set, priority1 pool becomes unlimited. And priority1 pool count value should not be used in reset of the remaining counters. 0 = (default) Priority 1 pool count is enabled. 1 = Priority 1 pool count is disabled. Should not be set when RO perf mode is enabled (by default this is enabled which is bit[27] of B118-B11Bh). lbcf_csr_priority1_cnt_disable.
Workaround: If this bit is set to 1 then the following bits in register B108-B10B should have identical values 29:28, 27:26, 25:24, 23:22, 21:20, 19:18, 17:16, 15:14, 13:12, 11:10, 9:8, 7:6, 5:4, 3:2, 1:0.

	6:4	**L3SQ Priority 1 Pool Counter**

Default Value:	110b
Access:	R/W

L3SQ Priority 1 Pool Counter (SQPRI1CNT):
The count of cycles is selected from priority1 pool before switching to other priority pools. Count is used as the power of 2.
000b = 1 request.
001b = 2 requests.
010b = 4 requests.
011b = 8 requests.
…
111b = 128 requests.
lbcf_csr_priority1_cnt[2:0].

	3	**L3SQ Priority 0 Pool Count Disable**

Access:	R/W

Description
L3SQ Priority 0 Pool Count Disable (SQPRI0CNTDIS): When set, priority0 pool becomes unlimited. And priority0 pool count value should not be used in reset of the remaining counters. 0 = (default) Priority 0 pool count is enabled. 1 = Priority 0 pool count is disabled. Should not be set when RO perf mode is enabled (by default this is enabled which is bit[27] of B118-B11Bh). lbcf_csr_priority0_cnt_disable.

L3SQCREG2 - L3 SQC registers 2

		Workaround: If this bit is set to 1 then the following bits in register B108-B10B should have identical values 29:28, 27:26, 25:24, 23:22, 21:20, 19:18, 17:16, 15:14, 13:12, 11:10, 9:8, 7:6, 5:4, 3:2, 1:0.	
	2:0	**L3SQ Priority 0 Pool Counter**	
		Default Value:	111b
		Access:	R/W
		L3SQ Priority 0 Pool Counter (SQPRI0CNT): The count of cycles is selected from priority0 pool before switching to other priority pools. Count is used as the power of 2. 000b = 1 request. 001b = 2 requests. 010b = 4 requests. 011b = 8 requests. … 111b = (default) 128 requests. lbcf_csr_priority0_cnt[2:0].	

L3 SQC registers 3

		L3SQCREG3 - L3 SQC registers 3

Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00001ABF
Size (in bits):	32

Address:	0B108h

DWord	Bit	Description
0	31:30	**Reserved**
		Access: / RO
		Reserved.
	29:28	**SOLunit Priority Value**
		Access: / R/W
		SOLunit Priority Value (SQSOLPRIVAL): Identifies the priority value for all cycles that are initiated by SOLunit. Priority is used in the L3 Super Queue (L3SQ). 00b = Priority 0 (default). 01b = Priority 1. 10b = Priority 2. 11b = Priority 3. lbcf_csr_sol_priority[1:0].
	27:26	**GSunit Priority Value**
		Access: / R/W
		GSunit Priority Value (SQGSPRIVAL): Identifies the priority value for all cycles that are initiated by GSunit. Priority is used in the L3 Super Queue (L3SQ). 00b = Priority 0 (default). 01b = Priority 1. 10b = Priority 2. 11b = Priority 3. lbcf_csr_gs_priority[1:0].
	25:24	**TEunit Priority Value**
		Access: / R/W
		TEunit Priority Value (SQTEPRIVAL): Identifies the priority value for all cycles that are initiated by TEunit. Priority is used in the L3 Super Queue (L3SQ). 00b = Priority 0 (default). 01b = Priority 1. 10b = Priority 2. 11b = Priority 3.

L3SQCREG3 - L3 SQC registers 3

		lbcf_csr_te_priority[1:0].

23:22	**CLunit Priority Value**	
	Access:	R/W

CLunit Priority Value (SQCLPRIVAL):
Identifies the priority value for all cycles that are initiated by CLunit. Priority is used in the L3
Super Queue (L3SQ).
00b = Priority 0 (default).
01b = Priority 1.
10b = Priority 2.
11b = Priority 3.
lbcf_csr_cl_priority[1:0].

21:20	**TSunit Priority Value**	
	Access:	R/W

TSunit Priority Value (SQTSPRIVAL):
Identifies the priority value for all cycles that are initiated by TSunit. Priority is used in the L3
Super Queue (L3SQ).
00b = Priority 0 (default).
01b = Priority 1.
10b = Priority 2.
11b = Priority 3.
lbcf_csr_ts_priority[1:0].

19:18	**SFunit Priority Value**	
	Access:	R/W

SFunit Priority Value (SQSFPRIVAL):
Identifies the priority value for all cycles that are initiated by SFunit. Priority is used in the L3
Super Queue (L3SQ).
00b = Priority 0 (default).
01b = Priority 1.
10b = Priority 2.
11b = Priority 3.
lbcf_csr_sf_priority[1:0].

17:16	**SVSM Priority Value**	
	Access:	R/W

SVSM Priority Value (SQSVSMPRIVAL):
Identifies the priority value for all cycles that are initiated by SVSM. Priority is used in the L3
Super Queue (L3SQ).
00b = Priority 0 (default).
01b = Priority 1.
10b = Priority 2.
11b = Priority 3.
lbcf_csr_svsm_priority[1:0].

15:14	**SARB Priority Value**	
	Access:	R/W

L3SQCREG3 - L3 SQC registers 3

		SARB Priority Value (SQSARBPRIVAL): Identifies the priority value for all cycles that are initiated by State Arbiter (SARB). Priority is used in the L3 Super Queue (L3SQ). 00b = Priority 0 (default). 01b = Priority 1. 10b = Priority 2. 11b = Priority 3. lbcf_csr_sarb_priority[1:0].
	13:12	**SBE Priority Value**
		Default Value: 01b
		Access: R/W
		SBE Priority Value (SQSBEPRIVAL): Identifies the priority value for all cycles that are initiated by SBE. Priority is used in the L3 Super Queue (L3SQ). 00b = Priority 0. 01b = Priority 1 (default). 10b = Priority 2. 11b = Priority 3. lbcf_csr_sbe_priority[1:0].
	11:10	**IC$ Priority Value**
		Default Value: 10b
		Access: R/W
		IC$ Priority Value (SQICPRIVAL): Identifies the priority value for all cycles that are initiated by Instruction Cache (IC$). Priority is used in the L3 Super Queue (L3SQ). 00b = Priority 0. 01b = Priority 1. 10b = Priority 2 (default). 11b = Priority 3. lbcf_csr_ic_priority[1:0].
	9:8	**TDL Priority Value**
		Default Value: 10b
		Access: R/W
		TDL Priority Value (SQTDLPRIVAL): Identifies the priority value for all cycles that are initiated by TDL. Priority is used in the L3 Super Queue (L3SQ). 00b = Priority 0. 01b = Priority 1. 10b = Priority 2 (default). 11b = Priority 3. lbcf_csr_tdl_priority[1:0].
	7:6	**DCunit Priority Value**
		Default Value: 10b

L3SQCREG3 - L3 SQC registers 3

		Access:	R/W
		DCunit Priority Value (SQDCPRIVAL): Identifies the priority value for all cycles that are initiated by DC. Priority is used in the L3 Super Queue (L3SQ). 00b = Priority 0. 01b = Priority 1. 10b = Priority 2 (default). 11b = Priority 3. lbcf_csr_dc_priority[1:0].	
	5:4	**DAPR Priority Value**	
		Default Value:	11b
		Access:	R/W
		DAPR Priority Value (SQDAPRPRIVAL): Identifies the priority value for all cycles that are initiated by DAPR. Priority is used in the L3 Super Queue (L3SQ). 00b = Priority 0. 01b = Priority 1. 10b = Priority 2. 11b = Priority 3 (default). lbcf_csr_dapr_priority[1:0].	
	3:2	**MTunit Priority Value**	
		Default Value:	11b
		Access:	R/W
		MTunit Priority Value (SQMTPRIVAL): Identifies the priority value for all cycles that are initiated by Sampler (MT). Priority is used in the L3 Super Queue (L3SQ). 00b = Priority 0. 01b = Priority 1. 10b = Priority 2. 11b = Priority 3 (default). lbcf_csr_mt_priority[1:0].	
	1:0	**LSQCunit Priority Value**	
		Default Value:	11b
		Access:	R/W
		LSQCunit Priority Value (SQPRIVAL): Identifies the priority value for all cycles that are initiated by Super Queue (L3 Evictions). Priority is used in the L3 Super Queue (L3SQ). 00b = Priority 0. 01b = Priority 1. 10b = Priority 2. 11b = Priority 3 (default). lbcf_csr_lsqc_priority[1:0].	

LBCF config save msg

LBCFCSR - LBCF config save msg		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0B2FCh	
This register is not context saved and is written by PM unit.		
DWord	**Bit**	**Description**
0	31:10	**Reserved**
		Access: RO
	9:0	**Context save bit**
		Access: R/W Hardware Clear
		Bit[9]: Power Context Save Request. 0: Power context save is not being requested (default). 1: Power context save is being requested. Unit needs to self-clear this bit upon sampling. Bits[8:0]: QWord Credits for Power Context Save Request. Minimum Credits = 1: Unit may send 1 QWord pair (enough for first LRI at least). Maximum Credits = 511: Unit may send 511 QWord pairs. A QWord pair is defined as a 32-bit register address and the corresponding 32-bits of register data. Note that the LRI header and END commands are 64-bits each (32-bit command followed by 32-bit NOOP) and consumes one QWord credit. Only valid with PWRCTX_SAVE_REQ (Bit9).

LBCF DPF Error log register 0

LBCFPM00 - LBCF DPF Error log register 0	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32

Address:	0B130h

Slice0 Bank 0 subbank0 Error log register

DWord	Bit	Description	
0	31:21	**Row Number for Error 1**	
		Access:	R/W
		Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. lbcf_sb0_error_addr1[9:0].	
	20:17	**Reserved**	
		Access:	RO
	16	**Valid Error 1**	
		Access:	R/W
		Valid Error: The Address located in field 31:21 is valid. lbcf_sb0_valid_error1.	
	15:5	**Row Number for Error0**	
		Access:	R/W
		Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. lbcf_sb0_error_addr0[9:0].	
	4:1	**Reserved**	
		Access:	RO
	0	**Valid Error 0**	
		Access:	R/W
		Valid Error: The address located in field 15:5 is valid. lbcf_sb0_valid_error0.	

LBCF DPF Error log register 1

LBCFPM01 - LBCF DPF Error log register 1	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0B134h

Slice0 Bank 0 subbank1 Error log register

DWord	Bit	Description	
0	31:21	**Row Number for Error 1**	
		Access:	R/W
		Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. lbcf_sb1_error_addr1[9:0].	
	20:17	**Reserved**	
		Access:	RO
	16	**Valid Error 1**	
		Access:	R/W
		Valid Error: The Address located in field 31:21 is valid. lbcf_sb1_error_addr0[9:0].	
	15:5	**Row Number for Error0**	
		Access:	R/W
		Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. lbcf_sb1_error_addr0[9:0].	
	4:1	**Reserved**	
		Access:	RO
	0	**Valid Error 0**	
		Access:	R/W
		Valid Error: The address located in field 15:5 is valid. lbcf_sb1_valid_error0.	

LBCF DPF Error log register 2

LBCFPM02 - LBCF DPF Error log register 2	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0B138h

Slice0 Bank0 Subbank 2 Error log register

DWord	Bit	Description
0	31:21	**Row Number for Error 1**
		Access: _____ R/W
		Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. lbcf_sb2_error_addr1[9:0].
	20:17	**Reserved**
		Access: _____ RO
	16	**Valid Error 1**
		Access: _____ R/W
		Valid Error: The Address located in field 31:21 is valid. lbcf_sb2_valid_error1.
	15:5	**Row Number for Error0**
		Access: _____ R/W
		Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. lbcf_sb2_error_addr0[9:0].
	4:1	**Reserved**
		Access: _____ RO
	0	**Valid Error 0**
		Access: _____ R/W
		Valid Error: The address located in field 15:5 is valid. lbcf_sb2_valid_error0.

LBCF DPF Error log register 3

LBCFPM03 - LBCF DPF Error log register 3	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0B13Ch

Slice0 Bank0 subbank3 Error log register

DWord	Bit	Description
0	31:21	**Row Number for Error 1**
		Access: R/W
		Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. lbcf_sb3_error_addr1[9:0].
	20:17	**Reserved**
		Access: RO
	16	**Valid Error 1**
		Access: R/W
		Valid Error: The Address located in field 31:21 is valid. lbcf_sb3_valid_error1.
	15:5	**Row Number for Error0**
		Access: R/W
		Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. lbcf_sb3_error_addr0[9:0].
	4:1	**Reserved**
		Access: RO
	0	**Valid Error 0**
		Access: R/W
		Valid Error: The address located in field 15:5 is valid. lbcf_sb3_valid_error0.

LBCF DPF Error log register 4

LBCFERRLOG01 - LBCF DPF Error log register 4		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0B140h	
Slice 0 Bank 1 Subbank0 Error log register		

DWord	Bit	Description
0	31:21	**Row Number for Error 1**
		Access: R/W
		Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 0 Bank 1 Error log register 00.
	20:17	**Reserved**
		Access: RO
	16	**Valid Error 1**
		Access: R/W
		Valid Error: The error located in field 31:21 is valid. Slice 0 Bank 1 Error log register 00.
	15:5	**Row Number for Error0**
		Access: R/W
		Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 0 Bank 1 Error log register 00.
	4:1	**Reserved**
		Access: RO
	0	**Valid Error 0**
		Access: R/W
		Valid Error: The error located in field 15:5 is valid. Slice 0 Bank 1 Error log register 00.

LBCF DPF Error log register 5

LBCFERRLOG02 - LBCF DPF Error log register 5

Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32

Address:	0B144h

Slice 0 Bank 1 Subbank1 Error log register

DWord	Bit	Description
0	31:21	**Row Number for Error 1**
		Access: / R/W
		Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 0 Bank 1 Error log register 00.
	20:17	**Reserved**
		Access: / RO
	16	**Valid Error 1**
		Access: / R/W
		Valid Error: The Address located in field 31:21 is valid. Slice 0 Bank 1 Error log register 00.
	15:5	**Row Number for Error0**
		Access: / R/W
		Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 0 Bank 1 Error log register 00.
	4:1	**Reserved**
		Access: / RO
	0	**Valid Error 0**
		Access: / R/W
		Valid Error: The address located in field 15:5 is valid

LBCF DPF Error log register 6

LBCFERRLOG03 - LBCF DPF Error log register 6		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0B148h	
Slice 0 Bank 1 subbank2 Error log register		

DWord	Bit	Description
0	31:21	**Row Number for Error 1**
		Access: ... R/W
		Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 0 Bank 1 Error log register 00.
	20:17	**Reserved**
		Access: ... RO
	16	**Valid Error 1**
		Access: ... R/W
		Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 0 Bank 1 Error log register 00.
	15:5	**Row Number for Error0**
		Access: ... R/W
		Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 0 Bank 1 Error log register 00.
	4:1	**Reserved**
		Access: ... RO
	0	**Valid Error 0**
		Access: ... R/W
		Valid Error: The address located in field 15:5 is valid. Slice 0 Bank 1 Error log register 00.

LBCF DPF Error log register 7

LBCFERRLOG04 - LBCF DPF Error log register 7	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0B14Ch

Slice0 Bank1 subbank3 Error log register

DWord	Bit	Description	
0	31:21	**Row Number for Error 1**	
		Access:	R/W
		Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 0 Bank 1 Error log register 00.	
	20:17	**Reserved**	
		Access:	RO
	16	**Valid Error 1**	
		Access:	R/W
		Valid Error: The Address located in field 31:21 is valid. Slice 0 Bank 1 Error log register 00.	
	15:5	**Row Number for Error0**	
		Access:	R/W
		Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 0 Bank 1 Error log register 00.	
	4:1	**Reserved**	
		Access:	RO
	0	**Valid Error 0**	
		Access:	R/W
		Valid Error: The address located in field 15:5 is valid. Slice 0 Bank 1 Error log register 00.	

LBCF DPF Error log register 8

LBCFERRLOG05 - LBCF DPF Error log register 8		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0B150h	

Slice 0 Bank 2 Subbank0 Error log register		
DWord	**Bit**	**Description**
0	31:21	**Row Number for Error 1**
		Access: R/W
		Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. The number of rows varies between 4K vs. 8K/16K subbanks which requires 10 bits vs 11 bits respectively. This field contains the row# with the error. Slice 0 Bank 2 Error log register 00.
	20:17	**Reserved**
		Access: RO
	16	**Valid Error 1**
		Access: R/W
		Valid Error: The error located in field 16:5 is valid and Slice 0 Bank 2 Error log register 00.
	16:5	**Row Number for Error0**
		Access: R/W
		Valid Error: The error located in field 16:5 is valid and Slice 0 Bank 2 Error log register 00.
	4:1	**Reserved**
		Access: RO
	0	**Valid Error 0**
		Access: R/W
		Valid Error: The error located in field 16:5 is valid. Slice 0 Bank 2 Error log register 00.

LBCF DPF Error log register 9

LBCFERRLOG06 - LBCF DPF Error log register 9		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0B154h	
Slice 0 Bank 2 subbank1 Error log register		

DWord	Bit	Description
0	31:21	**Row Number for Error 1**
		Access: · R/W
		Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank.
		The number of rows varies between 4K vs. 8K/16K subbanks which requires 10 bits vs 11 bits respectively.
		This field contains the row# with the error.
		Slice 0 Bank 2 Error log register 00.
	20:17	**Reserved**
		Access: · RO
	16	**Valid Error 1**
		Access: · R/W
		Valid Error: The error located in field 31:21 is valid.
		Slice 0 Bank 2 Error log register 00.
	15:5	**Row Number for Error0**
		Access: · R/W
		Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank.
		Slice 0 Bank 2 Error log register 00.
	4:1	**Reserved**
		Access: · RO
	0	**Valid Error 0**
		Access: · R/W
		Valid Error: The error located in field 15:5 is valid.

LBCF DPF Error log register 10

LBCFERRLOG07 - LBCF DPF Error log register 10		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0B158h	
Slice 0 Bank 2 subbank2 Error log register		

DWord	Bit	Description
0	31:21	**Row Number for Error 1**
		Access: R/W
		Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. The number of rows varies between 4K vs. 8K/16K subbanks which requires 10 bits vs. 11 bits respectively. This field contains the row# with the error. Slice 0 Bank 2 Error log register 00.
	20:17	**Reserved**
		Access: RO
	16	**Valid Error 1**
		Access: R/W
		Valid Error: The error located in field 31:21 is valid. Slice 0 Bank 2 Error log register 00.
	15:5	**Row Number for Error0**
		Access: R/W
		Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 0 Bank 2 Error log register 00.
	4:1	**Reserved**
		Access: RO
	0	**Valid Error 0**
		Access: R/W
		Valid Error: The error located in field 15:5 is valid. Slice 0 Bank 2 Error log register 00.

LBCF DPF Error log register 11

LBCFERRLOG08 - LBCF DPF Error log register 11		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0B15Ch	
slice0 Bank 2 subbank3 Error log register		

DWord	Bit	Description
0	31:21	**Row Number for Error 1**
		Access: R/W
		Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. The number of rows varies between 4K vs. 8K/16K subbanks which requires 10 bits vs. 11 bits respectively. This field contains the row# with the error. Slice 0 Bank 2 Error log register 00.
	20:17	**Reserved**
		Access: RO
	16	**Valid Error 1**
		Access: R/W
		Valid Error: The error located in field 31:21 is valid. Slice 0 Bank 2 Error log register 00.
	15:5	**Row Number for Error0**
		Access: R/W
		Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 0 Bank 2 Error log register 00.
	4:1	**Reserved**
		Access: RO
	0	**Valid Error 0**
		Access: R/W
		Valid Error: The error located in field 15:5 is valid. Slice 0 Bank 2 Error log register 00.

LBCF DPF Error log register 12

LBCFERRLOG09 - LBCF DPF Error log register 12		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0B160h	
Slice 0 Bank 3 subbank0 Error log register		

DWord	Bit	Description
0	31:21	**Row Number for Error 1**
		Access: / R/W
		Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 0 Bank 3 Error log register 00.
	20:17	**Reserved**
		Access: / RO
	16	**Valid Error 1**
		Access: / R/W
		Valid Error: The error located in field 31:21 is valid. Slice 0 Bank 3 Error log register 00.
	15:5	**Row Number for Error0**
		Access: / R/W
		Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 0 Bank 3 Error log register 00.
	4:1	**Reserved**
		Access: / RO
	0	**Valid Error 0**
		Access: / R/W
		Valid Error: The error located in field 15:5 is valid. Slice 0 Bank 3 Error log register 00.

LBCF DPF Error log register 13

LBCFERRLOG10 - LBCF DPF Error log register 13		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0B164h	
Slice 0 Bank 3 subbank1 Error log register 00		

DWord	Bit	Description
0	31:21	**Row Number for Error 1**
		Access: R/W
		Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 0 Bank 3 Error log register 00.
	20:17	**Reserved**
		Access: RO
	16	**Valid Error 1**
		Access: R/W
		Valid Error: The error located in field 31:21 is valid. Slice 0 Bank 3 Error log register 00.
	15:5	**Row Number for Error0**
		Access: R/W
		Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 0 Bank 3 Error log register 00.
	4:1	**Reserved**
		Access: RO
	0	**Valid Error 0**
		Access: R/W
		Valid Error: The error located in field 15:5 is valid.

LBCF DPF Error log register 14

LBCFERRLOG11 - LBCF DPF Error log register 14		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0B168h	
Slice 0 Bank 3 subbank2 Error log register 00		
DWord	**Bit**	**Description**
0	31:21	**Row Number for Error 1**
		Access: R/W
		Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 0 Bank 3 Error log register 00.
	20:17	**Reserved**
		Access: RO
	16	**Valid Error 1**
		Access: R/W
		Valid Error: The error located in field 31:21 is valid. Slice 0 Bank 3 Error log register 00.
	15:5	**Row Number for Error0**
		Access: R/W
		Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 0 Bank 3 Error log register 00.
	4:1	**Reserved**
		Access: RO
	0	**Valid Error 0**
		Access: R/W
		Valid Error: The error located in field 15:5 is valid. Slice 0 Bank 3 Error log register 00.

LBCF DPF Error log register 15

LBCFERRLOG12 - LBCF DPF Error log register 15	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0B16Ch

Slice0 Bank 3 subbank3 Error log register

DWord	Bit	Description
0	31:21	**Row Number for Error 1**
		Access: R/W
		Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 0 Bank 3 Error log register 00.
	20:17	**Reserved**
		Access: RO
	16	**Valid Error 1**
		Access: R/W
		Valid Error: The error located in field 31:21 is valid. Slice 0 Bank 3 Error log register 00.
	15:5	**Row Number for Error0**
		Access: R/W
		Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 0 Bank 3 Error log register 00.
	4:1	**Reserved**
		Access: RO
	0	**Valid Error 0**
		Access: R/W
		Valid Error: The error located in field 15:5 is valid. Slice 0 Bank 3 Error log register 00.

LBCF DPF Error log register 17

LBCFERRLOG14 - LBCF DPF Error log register 17		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0B174h	
Slice 1 bank 0 subbank1 Error log register		

DWord	Bit	Description
0	31:21	**Row Number for Error 1**
		Access: R/W
		Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 bank 1 Error log register 00.
	20:17	**Reserved**
		Access: RO
	16	**Valid Error 1**
		Access: R/W
		Valid Error: The error located in field 31:21 is valid. Slice 1 bank 1 Error log register 00.
	15:5	**Row Number for Error0**
		Access: R/W
		Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 bank 1 Error log register 00.
	4:1	**Reserved**
		Access: RO
	0	**Valid Error 0**
		Access: R/W
		Valid Error: The error located in field 15:5 is valid.

LBCF DPF Error log register 18

LBCFERRLOG15 - LBCF DPF Error log register 18	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0B178h

Slice 1 bank 0 subbank2 Error log register

DWord	Bit	Description
0	31:21	**Row Number for Error 1**
		Access: _____ R/W
		Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 bank 1 Error log register 00.
	20:17	**Reserved**
		Access: _____ RO
	16	**Valid Error 1**
		Access: _____ R/W
		Valid Error: The error located in field 31:21 is valid. Slice 1 bank 1 Error log register 00.
	15:5	**Row Number for Error0**
		Access: _____ R/W
		Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 bank 1 Error log register 00.
	4:1	**Reserved**
		Access: _____ RO
	0	**Valid Error 0**
		Access: _____ R/W
		Valid Error: The error located in field 15:5 is valid. Slice 1 bank 1 Error log register 00.

LBCF DPF Error log register 19

LBCFERRLOG16 - LBCF DPF Error log register 19		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0B17Ch	
Slice1 bank 0 subbank3 Error log register		

DWord	Bit	Description
0	31:21	**Row Number for Error 1**
		Access: R/W
		Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 bank 1 Error log register 00.
	20:17	**Reserved**
		Access: RO
	16	**Valid Error 1**
		Access: R/W
		Valid Error: The error located in field 31:21 is valid. Slice 1 bank 1 Error log register 00.
	15:5	**Row Number for Error0**
		Access: R/W
		Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 bank 1 Error log register 00.
	4:1	**Reserved**
		Access: RO
	0	**Valid Error 0**
		Access: R/W
		Valid Error: The error located in field 15:5 is valid. Slice 1 bank 1 Error log register 00.

LBCF DPF Error log register 20

LBCFERRLOG17 - LBCF DPF Error log register 20		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0B180h	
Slice 1 bank 1 subbank0 Error log register		

DWord	Bit	Description
0	31:21	**Row Number for Error 1**
		Access: R/W
		Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 bank 0 Error log register 00.
	20:17	**Reserved**
		Access: RO
	16	**Valid Error 1**
		Access: R/W
		Valid Error: The error located in field 31:21 is valid. Slice 1 bank 0 Error log register 00.
	15:5	**Row Number for Error0**
		Access: R/W
		Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 bank 0 Error log register 00.
	4:1	**Reserved**
		Access: RO
	0	**Valid Error 0**
		Access: R/W
		Valid Error: The error located in field 15:5 is valid. Slice 1 bank 0 Error log register 00.

LBCF DPF Error log register 21

LBCFERRLOG18 - LBCF DPF Error log register 21		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0B184h	
Slice 1 bank 1 subbank1 Error log register		

DWord	Bit	Description
0	31:21	**Row Number for Error 1**
		Access: R/W
		Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 bank 0 Error log register 00.
	20:17	**Reserved**
		Access: RO
	16	**Valid Error 1**
		Access: R/W
		Valid Error: The error located in field 31:21 is valid. Slice 1 bank 0 Error log register 00.
	15:5	**Row Number for Error0**
		Access: R/W
		Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 bank 0 Error log register 00.
	4:1	**Reserved**
		Access: RO
	0	**Valid Error 0**
		Access: R/W
		Valid Error: The error located in field 15:5 is valid.

LBCF DPF Error log register 22

LBCFERRLOG19 - LBCF DPF Error log register 22		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0B188h	
Slice 1 bank 1 subbank2 Error log register		

DWord	Bit	Description
0	31:21	**Row Number for Error 1**
		Access: R/W
		Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 bank 0 Error log register 00.
	20:17	**Reserved**
		Access: RO
	16	**Valid Error 1**
		Access: R/W
		Valid Error: The error located in field 31:21 is valid. Slice 1 bank 0 Error log register 00.
	15:5	**Row Number for Error0**
		Access: R/W
		Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 bank 0 Error log register 00.
	4:1	**Reserved**
		Access: RO
	0	**Valid Error 0**
		Access: R/W
		Valid Error: The error located in field 15:5 is valid. Slice 1 bank 0 Error log register 00.

LBCF DPF Error log register 23

LBCFERRLOG20 - LBCF DPF Error log register 23		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0B18Ch	
slice1 bank1 subbbank 3 Error log register		

DWord	Bit	Description
0	31:21	**Row Number for Error 1**
		Access: R/W
		Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 bank 0 Error log register 00.
	20:17	**Reserved**
		Access: RO
	16	**Valid Error 1**
		Access: R/W
		Valid Error: The error located in field 31:21 is valid. Slice 1 bank 0 Error log register 00.
	15:5	**Row Number for Error0**
		Access: R/W
		Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 bank 0 Error log register 00.
	4:1	**Reserved**
		Access: RO
	0	**Valid Error 0**
		Access: R/W
		Valid Error: The error located in field 15:5 is valid. Slice 1 bank 0 Error log register 00.

LBCF DPF Error log register 24

LBCFERRLOG21 - LBCF DPF Error log register 24		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0B190h	
Slice 1 bank 2 subbank0 Error log register 00		

DWord	Bit	Description
0	31:21	**Row Number for Error 1**
		Access: R/W
		Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 bank 2 Error log register 00.
	20:17	**Reserved**
		Access: RO
	16	**Valid Error 1**
		Access: R/W
		Valid Error: The error located in field 31:21 is valid. Slice 1 bank 2 Error log register 00.
	15:5	**Row Number for Error0**
		Access: R/W
		Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 bank 2 Error log register 00.
	4:1	**Reserved**
		Access: RO
	0	**Valid Error 0**
		Access: R/W
		Valid Error: The error located in field 15:5 is valid. Slice 1 bank 2 Error log register 00.

LBCF DPF Error log register 25

LBCFERRLOG22 - LBCF DPF Error log register 25		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0B194h	
Slice 1 bank 2 subbank 1 Error log register 00		

DWord	Bit	Description
0	31:21	**Row Number for Error 1**
		Access: R/W
		Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 bank 2 Error log register 00.
	20:17	**Reserved**
		Access: RO
	16	**Valid Error 1**
		Access: R/W
		Valid Error: The error located in field 31:21 is valid. Slice 1 bank 2 Error log register 00.
	15:5	**Row Number for Error0**
		Access: R/W
		Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 bank 2 Error log register 00.
	4:1	**Reserved**
		Access: RO
	0	**Valid Error 0**
		Access: R/W
		Valid Error: The error located in field 15:5 is valid.

LBCF DPF Error log register 26

LBCFERRLOG23 - LBCF DPF Error log register 26	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0B198h

Slice 1 bank 2 subbank 2 Error log register

DWord	Bit	Description
0	31:21	**Row Number for Error 1**
		Access: R/W
		Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 bank 2 Error log register 00.
	20:17	**Reserved**
		Access: RO
	16	**Valid Error 1**
		Access: R/W
		Valid Error: The error located in field 31:21 is valid. Slice 1 bank 2 Error log register 00.
	15:5	**Row Number for Error0**
		Access: R/W
		Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 bank 2 Error log register 00.
	4:1	**Reserved**
		Access: RO
	0	**Valid Error 0**
		Access: R/W
		Valid Error: The error located in field 15:5 is valid. Slice 1 bank 2 Error log register 00.

LBCF DPF Error log register 27

LBCFERRLOG24 - LBCF DPF Error log register 27		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0B19Ch	
Slice 1 bank 2 subbank 3 Error log register		

DWord	Bit	Description
0	31:21	**Row Number for Error 1**
		Access: R/W
		Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 bank 2 Error log register 00.
	20:17	**Reserved**
		Access: RO
	16	**Valid Error 1**
		Access: R/W
		Valid Error: The error located in field 31:21 is valid. Slice 1 bank 2 Error log register 00.
	15:5	**Row Number for Error0**
		Access: R/W
		Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 bank 2 Error log register 00.
	4:1	**Reserved**
		Access: RO
	0	**Valid Error 0**
		Access: R/W
		Valid Error: The error located in field 15:5 is valid. Slice 1 bank 2 Error log register 00.

LBCF DPF Error log register 28

LBCFERRLOG25 - LBCF DPF Error log register 28		

Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32

Address:	0B1A0h

Slice 1 Bank 3 subbank 0 Error log register

DWord	Bit	Description
0	31:21	**Row Number for Error 1**
		Access: R/W
		Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 Bank 3 Error log register 00.
	20:17	**Reserved**
		Access: RO
	16	**Valid Error 1**
		Access: R/W
		Valid Error: The error located in field 31:21 is valid. Slice 1 Bank 3 Error log register 00.
	15:5	**Row Number for Error0**
		Access: R/W
		Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 Bank 3 Error log register 00.
	4:1	**Reserved**
		Access: RO
	0	**Valid Error 0**
		Access: R/W
		Valid Error: The error located in field 15:5 is valid. Slice 1 Bank 3 Error log register 00.

LBCF DPF Error log register 29

LBCFERRLOG26 - LBCF DPF Error log register 29		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0B1A4h	
Slice 1 Bank 3 subbank 1 Error log register		

DWord	Bit	Description
0	31:21	**Row Number for Error 1**
		Access: / R/W
		Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 Bank 3 Error log register 00.
	20:17	**Reserved**
		Access: / RO
	16	**Valid Error 1**
		Access: / R/W
		Valid Error: The error located in field 31:21 is valid. Slice 1 Bank 3 Error log register 00.
	15:5	**Row Number for Error0**
		Access: / R/W
		Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 Bank 3 Error log register 00.
	4:1	**Reserved**
		Access: / RO
	0	**Valid Error 0**
		Access: / R/W
		Valid Error: The error located in field 15:5 is valid.

LBCF DPF Error log register 30

LBCFERRLOG27 - LBCF DPF Error log register 30	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0B1A8h

Slice 1 Bank 3 subbank 2 Error log register

DWord	Bit	Description
0	31:21	**Row Number for Error 1**
		Access: R/W
		Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 Bank 3 Error log register 00.
	20:17	**Reserved**
		Access: RO
	16	**Valid Error 1**
		Access: R/W
		Valid Error: The error located in field 31:21 is valid. Slice 1 Bank 3 Error log register 00.
	15:5	**Row Number for Error0**
		Access: R/W
		Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 Bank 3 Error log register 00.
	4:1	**Reserved**
		Access: RO
	0	**Valid Error 0**
		Access: R/W
		Valid Error: The error located in field 15:5 is valid. Slice 1 Bank 3 Error log register 00.

LBCF DPF Error log register 31

LBCFERRLOG28 - LBCF DPF Error log register 31		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0B1ACh	
slice1 Bank 3 subbank 3 Error log register		
DWord	**Bit**	**Description**
0	31:21	**Row Number for Error 1**
		Access: / R/W
		Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 Bank 3 Error log register 00.
	20:17	**Reserved**
		Access: / RO
	16	**Valid Error 1**
		Access: / R/W
		Valid Error: The error located in field 31:21 is valid. Slice 1 Bank 3 Error log register 00.
	15:5	**Row Number for Error0**
		Access: / R/W
		Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 Bank 3 Error log register 00.
	4:1	**Reserved**
		Access: / RO
	0	**Valid Error 0**
		Access: / R/W
		Valid Error: The error located in field 15:5 is valid. Slice 1 Bank 3 Error log register 00.

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LBCF DPF Error log register 32

<table>
<tr><td colspan="3" align="center">**LBCFERRLOG29 - LBCF DPF Error log register 32**</td></tr>
<tr><td colspan="3">Register Space: MMIO: 0/2/0</td></tr>
<tr><td colspan="3">Project: CHV, BSW</td></tr>
<tr><td colspan="3">Source: PRM</td></tr>
<tr><td colspan="3">Default Value: 0x00000000</td></tr>
<tr><td colspan="3">Size (in bits):   32</td></tr>
<tr><td colspan="3">Address: 0B1B0h</td></tr>
<tr><td colspan="3">Slice 2 Bank 0 subbank0 Error log register</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td>**Description**</td></tr>
<tr><td>0</td><td>31:21</td><td>**Row Number for Error 1**
Access: R/W
Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank.
Slice 2 Bank 0 Error log register 00.</td></tr>
<tr><td></td><td>20:17</td><td>**Reserved**
Access: RO</td></tr>
<tr><td></td><td>16</td><td>**Valid Error 1**
Access: R/W
Valid Error: The error located in field 31:21 is valid.
Slice 2 Bank 0 Error log register 00.</td></tr>
<tr><td></td><td>15:5</td><td>**Row Number for Error0**
Access: R/W
Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank.
Slice 2 Bank 0 Error log register 00.</td></tr>
<tr><td></td><td>4:1</td><td>**Reserved**
Access: RO</td></tr>
<tr><td></td><td>0</td><td>**Valid Error 0**
Access: R/W
Valid Error: The error located in field 15:5 is valid.
Slice 2 Bank 0 Error log register 00.</td></tr>
</table>

LBCF DPF Error log register 33

LBCFERRLOG30 - LBCF DPF Error log register 33		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0B1B4h	
Slice 2 Bank 0 subbank 1 Error log register		

DWord	Bit	Description
0	31:21	**Row Number for Error 1**
		Access: R/W
		Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 0 Error log register 00.
	20:17	**Reserved**
		Access: RO
	16	**Valid Error 1**
		Access: R/W
		Valid Error: The error located in field 31:21 is valid. Slice 2 Bank 0 Error log register 00.
	15:5	**Row Number for Error0**
		Access: R/W
		Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 0 Error log register 00.
	4:1	**Reserved**
		Access: RO
	0	**Valid Error 0**
		Access: R/W
		Valid Error: The error located in field 15:5 is valid.

LBCF DPF Error log register 34

LBCFERRLOG31 - LBCF DPF Error log register 34	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0B1B8h

Slice 2 Bank 0 Subbank 2 Error log register 00

DWord	Bit	Description
0	31:21	**Row Number for Error 1**
		Access: ... R/W
		Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 0 Error log register 00.
	20:17	**Reserved**
		Access: ... RO
	16	**Valid Error 1**
		Access: ... R/W
		Valid Error: The error located in field 31:21 is valid. Slice 2 Bank 0 Error log register 00.
	15:5	**Row Number for Error0**
		Access: ... R/W
		Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 0 Error log register 00.
	4:1	**Reserved**
		Access: ... RO
	0	**Valid Error 0**
		Access: ... R/W
		Valid Error: The error located in field 15:5 is valid. Slice 2 Bank 0 Error log register 00.

LBCF DPF Error log register 35

LBCFERRLOG32 - LBCF DPF Error log register 35		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0B1BCh	
Slice2 Bank 0 Subbank 3 Error log register		

DWord	Bit	Description
0	31:21	**Row Number for Error 1**
		Access: R/W
		Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 0 Error log register 00.
	20:17	**Reserved**
		Access: RO
	16	**Valid Error 1**
		Access: R/W
		Valid Error: The error located in field 31:21 is valid. Slice 2 Bank 0 Error log register 00.
	15:5	**Row Number for Error0**
		Access: R/W
		Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 0 Error log register 00.
	4:1	**Reserved**
		Access: RO
	0	**Valid Error 0**
		Access: R/W
		Valid Error: The error located in field 15:5 is valid. Slice 2 Bank 0 Error log register 00.

LBCF DPF Error log register 36

LBCFERRLOG33 - LBCF DPF Error log register 36		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0B1C0h	
Slice 2 Bank 1 Subbank 0 Error log register		

DWord	Bit	Description
0	31:21	**Row Number for Error 1**
		Access: R/W
		Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 1 Error log register 00.
	20:17	**Reserved**
		Access: RO
	16	**Valid Error 1**
		Access: R/W
		Valid Error: The error located in field 31:21 is valid. Slice 2 Bank 1 Error log register 00.
	15:5	**Row Number for Error0**
		Access: R/W
		Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 1 Error log register 00.
	4:1	**Reserved**
		Access: RO
	0	**Valid Error 0**
		Access: R/W
		Valid Error: The error located in field 15:5 is valid. Slice 2 Bank 1 Error log register 00.

LBCF DPF Error log register 37

LBCFERRLOG34 - LBCF DPF Error log register 37		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0B1C4h	
Slice 2 Bank 1 Subbank 1 Error log register		
DWord	**Bit**	**Description**
0	31:21	**Row Number for Error 1**
		Access: R/W
		Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 1 Error log register 00.
	20:17	**Reserved**
		Access: RO
	16	**Valid Error 1**
		Access: R/W
		Valid Error: The error located in field 31:21 is valid. Slice 2 Bank 1 Error log register 00.
	15:5	**Row Number for Error0**
		Access: R/W
		Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 1 Error log register 00.
	4:1	**Reserved**
		Access: RO
	0	**Valid Error 0**
		Access: R/W
		Valid Error: The error located in field 15:5 is valid.

LBCF DPF Error log register 38

LBCFERRLOG35 - LBCF DPF Error log register 38	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0B1C8h

Slice 2 Bank 1 Subbank 2 Error log register 00

DWord	Bit	Description
0	31:21	**Row Number for Error 1**
		Access: R/W
		Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 1 Error log register 00.
	20:17	**Reserved**
		Access: RO
	16	**Valid Error 1**
		Access: R/W
		Valid Error: The error located in field 31:21 is valid. Slice 2 Bank 1 Error log register 00.
	15:5	**Row Number for Error0**
		Access: R/W
		Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 1 Error log register 00.
	4:1	**Reserved**
		Access: RO
	0	**Valid Error 0**
		Access: R/W
		Valid Error: The error located in field 15:5 is valid. Slice 2 Bank 1 Error log register 00.

LBCF DPF Error log register 39

LBCFERRLOG36 - LBCF DPF Error log register 39		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0B1CCh	
Slice 2 Bank 1 subbank 3 Error log register		

DWord	Bit	Description
0	31:21	**Row Number for Error 1**
		Access: R/W
		Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 1 Error log register 00.
	20:17	**Reserved**
		Access: RO
	16	**Valid Error 1**
		Access: R/W
		Valid Error: The error located in field 31:21 is valid. Slice 2 Bank 1 Error log register 00.
	15:5	**Row Number for Error0**
		Access: R/W
		Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 1 Error log register 00.
	4:1	**Reserved**
		Access: RO
	0	**Valid Error 0**
		Access: R/W
		Valid Error: The error located in field 15:5 is valid. Slice 2 Bank 1 Error log register 00.

LBCF DPF Error log register 40

LBCFERRLOG37 - LBCF DPF Error log register 40		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0B1D0h	
Slice 2 Bank 2 subbank 0 Error log register		

DWord	Bit	Description
0	31:21	**Row Number for Error 1**
		Access: R/W
		Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 2 Error log register 00.
	20:17	**Reserved**
		Access: RO
	16	**Valid Error 1**
		Access: R/W
		Valid Error: The error located in field 31:21 is valid. Slice 2 Bank 2 Error log register 00.
	15:5	**Row Number for Error0**
		Access: R/W
		Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 2 Error log register 00.
	4:1	**Reserved**
		Access: RO
	0	**Valid Error 0**
		Access: R/W
		Valid Error: The error located in field 15:5 is valid. Slice 2 Bank 2 Error log register 00.

LBCF DPF Error log register 41

LBCFERRLOG38 - LBCF DPF Error log register 41		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0B1D4h	
Slice 2 Bank 2 subbank 1 Error log register		

DWord	Bit	Description
0	31:21	**Row Number for Error 1**
		Access: R/W
		Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 2 Error log register 00.
	20:17	**Reserved**
		Access: RO
	16	**Valid Error 1**
		Access: R/W
		Valid Error: The error located in field 31:21 is valid. Slice 2 Bank 2 Error log register 00.
	15:5	**Row Number for Error0**
		Access: R/W
		Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 2 Error log register 00.
	4:1	**Reserved**
		Access: RO
	0	**Valid Error 0**
		Access: R/W
		Valid Error: The error located in field 15:5 is valid.

LBCF DPF Error log register 42

LBCFERRLOG39 - LBCF DPF Error log register 42	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0B1D8h

Slice 2 Bank 2 subbank 2 Error log register

DWord	Bit	Description	
0	31:21	**Row Number for Error 1**	
		Access:	R/W
		Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 2 Error log register 00.	
	20:17	**Reserved**	
		Access:	RO
	16	**Valid Error 1**	
		Access:	R/W
		Valid Error: The error located in field 31:21 is valid. Slice 2 Bank 2 Error log register 00.	
	15:5	**Row Number for Error0**	
		Access:	R/W
		Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 2 Error log register 00.	
	4:1	**Reserved**	
		Access:	RO
	0	**Valid Error 0**	
		Access:	R/W
		Valid Error: The error located in field 15:5 is valid. Slice 2 Bank 2 Error log register 00.	

LBCF DPF Error log register 43

LBCFERRLOG40 - LBCF DPF Error log register 43		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0B1DCh	
Slice 2 Bank 2 subbank 3 Error log register		

DWord	Bit	Description
0	31:21	**Row Number for Error 1**
		Access: R/W
		Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 2 Error log register 00.
	20:17	**Reserved**
		Access: RO
	16	**Valid Error 1**
		Access: R/W
		Valid Error: The error located in field 31:21 is valid. Slice 2 Bank 2 Error log register 00.
	15:5	**Row Number for Error0**
		Access: R/W
		Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 2 Error log register 00.
	4:1	**Reserved**
		Access: RO
	0	**Valid Error 0**
		Access: R/W
		Valid Error: The error located in field 15:5 is valid. Slice 2 Bank 2 Error log register 00.

LBCF DPF Error log register 44

LBCFERRLOG41 - LBCF DPF Error log register 44		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0B1E0h	

Slice 2 Bank 3 subbank 0 Error log register		
DWord	**Bit**	**Description**
0	31:21	**Row Number for Error 1**
		Access: R/W
		Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 3 Error log register 00.
	20:17	**Reserved**
		Access: RO
	16	**Valid Error 1**
		Access: R/W
		Valid Error: The error located in field 31:21 is valid. Slice 2 Bank 3 Error log register 00.
	15:5	**Row Number for Error0**
		Access: R/W
		Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. and Slice 2 Bank 3 Error log register 00.
	4:1	**Reserved**
		Access: RO
	0	**Valid Error 0**
		Access: R/W
		Valid Error: The error located in field 15:5 is validcorresponding logical 16KB group should bypass this row. Slice 2 Bank 3 Error log register 00.

LBCF DPF Error log register 45

LBCFERRLOG42 - LBCF DPF Error log register 45	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0B1E4h

Slice 2 Bank 3 subbank 1 Error log register

DWord	Bit	Description
0	31:21	**Row Number for Error 1**
		Access: R/W
		Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 3 Error log register 00.
	20:17	**Reserved**
		Access: RO
	16	**Valid Error 1**
		Access: R/W
		Valid Error: The error located in field 31:21 is valid. Slice 2 Bank 3 Error log register 00.
	15:5	**Row Number for Error0**
		Access: R/W
		Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 3 Error log register 00.
	4:1	**Reserved**
		Access: RO
	0	**Valid Error 0**
		Access: R/W
		Valid Error: The error located in field 15:5 is valid.

LBCF DPF Error log register 46

LBCFERRLOG43 - LBCF DPF Error log register 46		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0B1E8h	
Slice 2 Bank 3 subbank 2 Error log register		

DWord	Bit	Description
0	31:21	**Row Number for Error 1**
		Access: ⎮ R/W
		Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 3 Error log register 00.
	20:17	**Reserved**
		Access: ⎮ RO
	16	**Valid Error 1**
		Access: ⎮ R/W
		Valid Error: The error located in field 31:21 is valid. Slice 2 Bank 3 Error log register 00.
	15:5	**Row Number for Error0**
		Access: ⎮ R/W
		Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 3 Error log register 00.
	4:1	**Reserved**
		Access: ⎮ RO
	0	**Valid Error 0**
		Access: ⎮ R/W
		Valid Error: The error located in field 15:5 is valid. Slice 2 Bank 3 Error log register 00.

LBCF DPF Error log register 47

LBCFERRLOG44 - LBCF DPF Error log register 47		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0B1ECh	

slice 2 Bank 3 subbank 3 Error log register

DWord	Bit	Description
0	31:21	**Row Number for Error 1**
		Access: R/W
		Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 3 Error log register 00.
	20:17	**Reserved**
		Access: RO
	16	**Valid Error 1**
		Access: R/W
		Valid Error: The error located in field 31:21 is valid. Slice 2 Bank 3 Error log register 00.
	15:5	**Row Number for Error0**
		Access: R/W
		Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 3 Error log register 00.
	4:1	**Reserved**
		Access: RO
	0	**Valid Error 0**
		Access: R/W
		Valid Error: The error located in field 15:5 is valid. Slice 2 Bank 3 Error log register 00.

LBS config bits

LBSREG - LBS config bits		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x46000000 CHV, BSW	
Size (in bits):	32	
Address:	0B124h	
Config Bits for LBS unit		

DWord	Bit	Description
0	31:27	**Retry timer for lookup into LSQC**
		Default Value: 01000b
		Access: R/W
		Time between receiving Reject Response from LSQC and doing a snoop lookup request again onto LSQCunit. 00000b: 0 clocks. 00001b: 1 clocks. 00010b: 2 clocks. … 01000b: 8 clocks (default value). … 11111b: 32 clocks. lbcf_retry_timer[4:0].
	26	**Recycle parent faster in R/W perf mode**
		Default Value: 1b
		Access: R/W
		Arc into recycle as soon as parent becomes eligible to be recycled. 0: Disabled (recycle possible only when parent is recycled). 1: Enabled (default). lbcf_csr_lsqc_rwperf_quickrec.
	25	**Perf mode for Writes to same address**
		Default Value: 1b
		Project: CHV, BSW
		Access: R/W
		Performance improvement for writes to same address in L3: 0 - Performance mode is not enabled. 1 - Performance mode is enabled (default). lbcf_csr_lsqc_erlyrec.
	24:0	**Reserved**
		Access: RO

LEAKAGECOUNTER

<td colspan="3" align="center">**LEAKAGECOUNTER - LEAKAGECOUNTER**</td>

Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	1300D4h

Leakage counter readout

DWord	Bit	Description
0	31:0	**Leakage_Counter** Default Value: 00000000h Access: RO This is a live read of the 32-bit leakage counter. Reading this register does not cause the counter to clear. Only the write-write protocol from Punit to Gunit will casue the leakage counter to clear.

LEAKAGECOUNTERCTL

LEAKAGECOUNTERCTL - LEAKAGECOUNTERCTL		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	1300D0h	
Leakage counter control.		

DWord	Bit	Description
0	31	**leakage_lock**
		Default Value: / 0b
		Access: / R/W Lock
		This is the lock bit for the leakage counter registers. 13_00D0-13_00DC.
	30:1	**Reserved**
		Default Value: / 00000000h
		Access: / RO
		Reserved
	0	**leakage_count_en**
		Default Value: / 0b
		Access: / R/W Lock
		Enable the leakage counters. When zero, the counters will be held to zero. As this transitions to 0-1, counting is enabled. Like the EMON Energy Counters, the leakage counter will perform a "sum of weights" for the 16 events(/subwells) described in 13_00D8 and 13_00DC.

LEAKAGEWEIGHT1

LEAKAGEWEIGHT1 - LEAKAGEWEIGHT1		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	1300D8h	
Leakage weights for wells types 1 to 4.		

DWord	Bit	Description
0	31:24	**leakage_vdve**
		Default Value: 00h
		Access: R/W Lock
		Leakage weight for 'vdve' well type. One of these wells are expected on CHV, BSW.
	23:16	**Reserved**
		Default Value: 00h
		Access: R/W Lock
	15:8	**Reserved**
		Default Value: 00h
		Access: R/W Lock
	7:0	**leakage_aon**
		Default Value: 00h
		Access: R/W Lock
		Leakage weight for 'aon' well type. One of these wells are expected on CHV, BSW.

LEAKAGEWEIGHT2

LEAKAGEWEIGHT2 - LEAKAGEWEIGHT2	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	1300DCh
Leakage weights for wells types 5 to 8.	

DWord	Bit	Description
0	31:24	**leakage_eupair**
		Default Value: 00h
		Access: R/W Lock
		Leakage weight for 'eupair' well type. Eight of these wells are expected on CHV, BSW.
	23:16	**leakage_ss**
		Default Value: 00h
		Access: R/W Lock
		Leakage weight for 'ss' well type. Two of these wells are expected on CHV, BSW.
	15:8	**leakage_l3**
		Default Value: 00h
		Access: R/W Lock
		Leakage weight for 'l3' well type. One of these wells are expected on CHV, BSW.
	7:0	**leakage_ffsc**
		Default Value: 00h
		Access: R/W Lock
		Leakage weight for 'ffsc' well type. One of these wells are expected on CHV, BSW.

LNCF config save msg

LNCFCSR - LNCF config save msg	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0B0FCh

This register is not context saved and is written by pm unit.

DWord	Bit	Description
0	31:10	**Reserved** Access: RO
	9:0	**Context save bit** Access: R/W Hardware Clear Bit[9].Power Context Save Request 0: Power context save is not being requested (default). 1: Power context save is being requested. Unit needs to self-clear this bit upon sampling. Bits[8:0].QWord Credits for Power Context Save Request. Minimum Credits = 1: Unit may send 1 QWord pair (enough for first LRI at least). Maximum Credits = 511: Unit may send 511 QWord pairs. A QWord pair is defined as a 32-bit register address and the corresponding 32-bits of register data. Note that the LRI header and END commands are 64-bits each (32-bit command followed by 32-bit NOOP) and consume one QWord credit. Only valid with PWRCTX_SAVE_REQ (Bit9).

Load Indirect Base Vertex

3DPRIM_BASE_VERTEX - Load Indirect Base Vertex	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02440h-02443h
Valid Projects:	

DWord	Bit	Description
0	31:0	**Base Vertex** Format: S31 This register is used to store the Base Vertex of the 3D_PRIMITIVE command when Load Indirect Enable is set.

Load Indirect Instance Count

3DPRIM_INSTANCE_COUNT - Load Indirect Instance Count	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02438h-0243Bh
Valid Projects:	

DWord	Bit	Description
0	31:0	**Instance Count** This register is used to store the Instance Count of the 3D_PRIMITIVE command when Load Indirect Enable is set.

Load Indirect Start Instance

3DPRIM_START_INSTANCE - Load Indirect Start Instance	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	0243Ch-0243Fh
Valid Projects:	

DWord	Bit	Description
0	31:0	**Start Vertex**
		Format: U32
		This register is used to store the Start Instance of the 3D_PRIMITIVE command when Load Indirect Enable is set.

Load Indirect Start Vertex

3DPRIM_START_VERTEX - Load Indirect Start Vertex	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02430h-02433h
Valid Projects:	

DWord	Bit	Description
0	31:0	**Start Vertex**

Format:	U32

This register is used to store the Start Vertex of the 3D_PRIMITIVE command when Load Indirect Enable is set.

Load Indirect Vertex Count

3DPRIM_VERTEX_COUNT - Load Indirect Vertex Count	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02434h-02437h
Valid Projects:	

DWord	Bit	Description
0	31:0	**Vertex Count**
		Format: U32
		This register is used to store the Vertex Count of the 3D_PRIMITIVE command when Load Indirect Enable is set.

LOW 2X FREQUENCY THRESHOLD

LOW2XFREQTHRESH - LOW 2X FREQUENCY THRESHOLD	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x000000A0
Size (in bits):	32
Address:	101128h

New for CHV, BSW.

BIOS/Driver programs the Low2x frequency threshold.

DWord	Bit	Description
0	31:16	**RESERVED**
		Default Value: 0000h
		Access: RO
		Reserved
	15:0	**L3FREQREG**
		Default Value: 00A0h
		Access: R/W
		This is control signal needed from clock unit that can be set at 1 when 2X clock frequency is less than or equal to 1GHz. It needs to be at 0 when 2X clock frequency is > 1GHz. Value when in HPLL mode: low2xthresh=0x00B4. This sets low2xfreq high whenever cu2x frequency is less than or equal to 800, 800, 1000, 800, and 800 for CZ400, CZ320, CZ333, CZ266, and CZ200 respectively. Value when in GPLL mode: low2xthresh=0x00A0. This sets low2xfreq high whenever cu2x frequency is less than or equal to 1000, 800, 834, 889, and 800 for CZ400, CZ320, CZ333, CZ266, and CZ200 respectively.

LPFC control register

LPFCCNTL - LPFC control register		

Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32

Address:	0B01Ch

LPFC control register.

DWord	Bit	Description
0	31	**LPFC enable signal**
			Access:	R/W	
		LPPC event collection enable signal. Incf_lpfc_cnt_en.
	30:0	**Reserved**
			Project:	CHV, BSW	
			Access:	RO	
		Reserved.

LTCD Error Injection Register

<table>
<tr><td colspan="4" align="center">**LBCFERR - LTCD Error Injection Register**</td></tr>
<tr><td colspan="4">Register Space: MMIO: 0/2/0</td></tr>
<tr><td colspan="4">Project: CHV, BSW</td></tr>
<tr><td colspan="4">Source: PRM</td></tr>
<tr><td colspan="4">Default Value: 0x00000000 CHV, BSW</td></tr>
<tr><td colspan="4">Size (in bits):   32</td></tr>
<tr><td colspan="4">Address: 0B12Ch</td></tr>
<tr><td colspan="4">LTCD Error Inject control bits in LBCF</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td colspan="2">**Description**</td></tr>
<tr><td>0</td><td>31:25</td><td colspan="2">**Reserved**</td></tr>
<tr><td></td><td></td><td>Project:</td><td>CHV, BSW</td></tr>
<tr><td></td><td></td><td>Access:</td><td>RO</td></tr>
<tr><td></td><td>24</td><td colspan="2">**LTISEQSL parity error interupt**</td></tr>
<tr><td></td><td></td><td>Default Value:</td><td>0b</td></tr>
<tr><td></td><td></td><td>Project:</td><td>CHV, BSW</td></tr>
<tr><td></td><td></td><td>Access:</td><td>R/W</td></tr>
<tr><td></td><td></td><td colspan="2">Parity error interrupt to LTISEQ Slice.</td></tr>
<tr><td></td><td>23</td><td colspan="2">**Bank hang on parity disable**</td></tr>
<tr><td></td><td></td><td>Default Value:</td><td>0b</td></tr>
<tr><td></td><td></td><td>Project:</td><td>CHV, BSW</td></tr>
<tr><td></td><td></td><td>Access:</td><td>R/W</td></tr>
<tr><td></td><td>22</td><td colspan="2">**Parity Error Injection Enable**</td></tr>
<tr><td></td><td></td><td>Project:</td><td>CHV, BSW</td></tr>
<tr><td></td><td></td><td>Access:</td><td>R/W</td></tr>
<tr><td></td><td></td><td colspan="2">0: Disable parity error injection.
1: Enable parity error injection.
lbcf_parity_err_inject_en.
Do not Enable this when ECC Error injection is enabled.</td></tr>
<tr><td></td><td>21</td><td colspan="2">**Double Bit Error injection**</td></tr>
<tr><td></td><td></td><td>Project:</td><td>CHV, BSW</td></tr>
<tr><td></td><td></td><td>Access:</td><td>R/W</td></tr>
<tr><td></td><td></td><td colspan="2">0: Default No error injected.
1: Double bit error is injected.
lbcf_ecc_2bit_err_inject.
Single bit Error Injection and double bit error injection are mutually exclusive.</td></tr>
</table>

LBCFERR - LTCD Error Injection Register

		Do not Enable this when Parity Error injection is enabled.
20		**Single Bit Error injection**
			Project:	CHV, BSW	
			Access:	R/W	
		0: Default No error injected. 1: Single bit error is injected. lbcf_ecc_1bit_err_inject. Single bit Error Injection and double bit error injection are mutually exclusive. Do not Enable this when Parity Error injection is enabled.
19		**ECC Error Injection Enable**
			Project:	CHV, BSW	
			Access:	R/W	
		0: Disable ECC error injection. 1: Enable ECC error injection. lbcf_ecc_err_inject_en. Do not Enable this when Parity Error injection is enabled.
18:4		**Row address for error injection**
			Project:	CHV, BSW	
			Access:	R/W	
		Row address for which error is injected. For ECC error injection, the same row address is overloaded to inject ECC error for that particular row address. SLM configuration. For Address: Rowaddress [16:7] is applicable for SLM banks and Parity injection is enabled and Rowaddress[18:7] is applicable for ECC (for both NonSLM/SLM banks). Sub bank is applicable only for Parity injection. Only Subbank 0, 1, 2, 3 are supported and are only related to SLM Banks (4KB). Total 12 bits address. Bits 18:7: Row address. Bits 6:4: Sub-Bank number. lbcf_parity_err_inject_rowaddr[9:0].lbcf_parity_err_inject_subank[2:0].16:7 - For SLM parity only. lbcf_parity_err_inject_rowaddr[9:0].lbcf_ecc_err_inject_rowaddr[11:0].For ECC error injection, the same row address is overloaded to inject ECC error for that particular row address.
3:2		**Bank ID for error injection**
			Project:	CHV, BSW	
			Access:	R/W	
		00b: Inject in Bank 0. 01b: Inject in Bank 1. 10b: Inject in Bank 2. 11b: Inject in Bank 3 (error injection not supported for SLM bank3).

LBCFERR - LTCD Error Injection Register		
		lbcf_err_inject_bankid[1:0].
	1:0	**Slice ID for Error injection**
		Project:	CHV, BSW
		Access:	R/W
		00b: Inject error in Slice 0. 01b: Inject error in Slice 1. 10b: Inject error in Slice 2. lbcf_err_inject_sliceid.	

MA

<table>
<tr><td colspan="3" align="center">**MA - MA**</td></tr>
<tr><td>Register Space:</td><td colspan="2">PCI: 0/2/0</td></tr>
<tr><td>Project:</td><td colspan="2">CHV, BSW</td></tr>
<tr><td>Source:</td><td colspan="2">PRM</td></tr>
<tr><td>Default Value:</td><td colspan="2">0x00000000</td></tr>
<tr><td>Size (in bits):</td><td colspan="2">32</td></tr>
<tr><td>Address:</td><td colspan="2">00094h</td></tr>
<tr><td colspan="3">Message Address</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td align="center">**Description**</td></tr>
<tr><td>0</td><td>31:2</td><td>

ADDRESS

Default Value:	00000000h
Access:	R/W

MA: Lower 32-bits of the system specified message address, always DW aligned. When GVD issues an MSI interrupt as a MEMWR on the SCL, the memory address corresponds to the value of this field.

</td></tr>
<tr><td></td><td>1:0</td><td>

RESERVED

Default Value:	00b
Access:	RO

Reserved

</td></tr>
</table>

Main Graphic Arbiter Error Report

<table>
<tr><td colspan="4" align="center">**ERROR - Main Graphic Arbiter Error Report**</td></tr>
<tr><td colspan="2">Register Space:</td><td colspan="2">MMIO: 0/2/0</td></tr>
<tr><td colspan="2">Project:</td><td colspan="2">CHV, BSW</td></tr>
<tr><td colspan="2">Source:</td><td colspan="2">PRM</td></tr>
<tr><td colspan="2">Default Value:</td><td colspan="2">0x00000000</td></tr>
<tr><td colspan="2">Size (in bits):</td><td colspan="2">32</td></tr>
<tr><td colspan="2">Address:</td><td colspan="2">040A0h</td></tr>
<tr><td colspan="4">This register is used to report different error conditions. Error bits are writable.</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td colspan="2">**Description**</td></tr>
<tr><td rowspan="18">0</td><td rowspan="3">31</td><td colspan="2">**Reserved Error Bits 31**</td></tr>
<tr><td>Default Value:</td><td>0b</td></tr>
<tr><td>Access:</td><td>R/W</td></tr>
<tr><td></td><td colspan="2">Future Use.</td></tr>
</table>

	Bit		
	31	**Reserved Error Bits 31**	
		Default Value:	0b
		Access:	R/W
		Future Use.	
	30	**Reserved Error Bits 30**	
		Default Value:	0b
		Access:	R/W
		Future Use.	
	29	**Reserved Error Bits 29**	
		Default Value:	0b
		Access:	R/W
		Future Use.	
	28	**Reserved Error Bits 28**	
		Default Value:	0b
		Access:	R/W
		Future Use.	
	27	**Reserved Error Bits 27**	
		Default Value:	0b
		Access:	R/W
		Future Use.	
	26	**Reserved Error Bits 26**	
		Default Value:	0b
		Access:	R/W

ERROR - Main Graphic Arbiter Error Report

		Future Use.	
	25	**Reserved Error Bits 25**	
		Default Value:	0b
		Access:	R/W
		Future Use.	
	24	**Reserved Error Bits 24**	
		Default Value:	0b
		Access:	R/W
		Future Use.	
	23	**Reserved Error Bits 23**	
		Default Value:	0b
		Access:	R/W
		Future Use.	
	22	**Reserved Error Bits 22**	
		Default Value:	0b
		Access:	R/W
		Future Use.	
	21	**Reserved Error Bits 21**	
		Default Value:	0b
		Access:	R/W
		Future Use.	
	20	**Reserved Error Bits 20**	
		Default Value:	0b
		Access:	R/W
		Future Use.	
	19	**Reserved Error Bits 19**	
		Default Value:	0b
		Access:	R/W
		Future Use.	
	18	**Reserved Error Bits 18**	
		Default Value:	0b

ERROR - Main Graphic Arbiter Error Report

		Access:	R/W
		Future Use.	

17	**Reserved Error Bits 17**		
		Default Value:	0b
		Access:	R/W
		Future Use.	

16	**Reserved Error Bits 16**		
		Default Value:	0b
		Access:	R/W
		Future Use.	

15	**Reserved Error Bits 15**		
		Default Value:	0b
		Access:	R/W
		ctx_fault_ctxt_not_prsmt_err - The Present (P) field in the context-entry used to process the DMA request is Clear.	

14	**Reserved Error Bits 14**		
		Default Value:	0b
		Access:	R/W
		ctx_fault_root_not_prsmt_err - The present (UP/LP) field in the root-entry used to process the untranslated request with PASID is 0.	

13	**Reserved Error Bits 13**		
		Default Value:	0b
		Access:	R/W
		ctx_fault_pasid_not_prsnt_err - PASID Table entry to be used does not have the PRESENT flag set. This means the PASID entry is not valid.	

12	**Reserved Error Bits 12**		
		Default Value:	0b
		Access:	R/W
		ctx_fault_pasid_ovflw_err - PASID Table size in extended context entry defines the number of PASIDs that will be supported. If hardware receives a PASID number outside the supported boundary, report as an error.	

11	**Reserved Error Bits 11**		
		Default Value:	0b

ERROR - Main Graphic Arbiter Error Report

		Access:	R/W

ctx_fault_pasid_dis_err - Submission of advanced context where the PASID field is not enabled in the extended context entry.

10	**Reserved Error Bits 10**		
	Default Value:		0b
	Access:		R/W

rstrm_fault_nowb_atomic_err - All page table accesses in advanced context with A/D bits are considered as atomic operations in WB space. However if the memory type for the page table accesses come out as anything but WB, that is an error.

9	**Reserved**

8	**Unloaded PD Error**		
	Default Value:		0b
	Access:		R/W

The Cache Line containing a PD entry being accessed, was marked as invalid in the last PD load cycle.

7	**Reserved Error Bits 7**		
	Default Value:		0b
	Access:		R/W

Future Use.

6	**Reserved**
5	**Reserved**
4	**Reserved**
3	**Reserved**

2	**Invalid Page Directory Entry Error**		
	Default Value:		0b
	Access:		R/W

PD entry's valid bit is 0.

1	**Reserved**

0	**TLB Page Fault Error**		
	Default Value:		0b
	Access:		R/W

A TLB Page's GTT translation generated a page fault (GTT entry not valid).

Main Graphic Arbiter Error Report 2

<table>
<tr><td colspan="4" align="center">**ERROR_2 - Main Graphic Arbiter Error Report 2**</td></tr>
<tr><td>Register Space:</td><td colspan="3">MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td colspan="3">CHV, BSW</td></tr>
<tr><td>Source:</td><td colspan="3">PRM</td></tr>
<tr><td>Default Value:</td><td colspan="3">0x00000000</td></tr>
<tr><td>Size (in bits):</td><td colspan="3">32</td></tr>
<tr><td>Address:</td><td colspan="3">040A4h</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td colspan="2">**Description**</td></tr>
<tr><td>0</td><td>31:0</td><td colspan="2">**Main Graphic Arbiter Error Report 2**</td></tr>
<tr><td></td><td></td><td>Default Value:</td><td>00000000h</td></tr>
<tr><td></td><td></td><td>Access:</td><td>RO</td></tr>
<tr><td></td><td></td><td colspan="2">Bit [31:6] - Reserved.
Bit [5:0] - tlbpend_reg_faultcnt[5:0].</td></tr>
</table>

Main Graphic Arbiter Error Report 3

ERROR_3 - Main Graphic Arbiter Error Report 3		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000 CHV, BSW	
Size (in bits):	32	
Address:	040A8h	
This register is used to report different error conditions. Error bits are writable.		

DWord	Bit	Description	
0	31:16	**Reserved**	
		Default Value:	0000h
		Access:	RO
	15	**Error3 Bits 15**	
		Default Value:	0b
		Access:	R/W
		Future Use.	
	14	**Error3 Error Bits 14**	
		Default Value:	0b
		Access:	R/W
		Future Use.	
	13	**Error3 Error Bits 13**	
		Default Value:	0b
		Access:	R/W
		Future Use.	
	12	**Error3 Error Bits 12**	
		Default Value:	0b
		Access:	R/W
		Future Use.	
	11	**Error3 Error Bits 11**	
		Default Value:	0b
		Project:	CHV, BSW
		Access:	R/W
		invalid_varmtrr_overlap_memtype_rd.	

ERROR_3 - Main Graphic Arbiter Error Report 3

	10	**Error3 Error Bits 10**	
		Default Value:	0b
		Project:	CHV, BSW
		Access:	R/W
		invalid_varmtrr_overlap_memtype_wr.	
	9	**Error3 Error Bits 9**	
		Default Value:	0b
		Project:	CHV, BSW
		Access:	R/W
		invalid_default_memtype_value_rd.	
	8	**Error3 Error Bits 8**	
		Default Value:	0b
		Project:	CHV, BSW
		Access:	R/W
		invalid_default_memtype_value_wr.	
	7	**Error3 Error Bits 7**	
		Default Value:	0b
		Project:	CHV, BSW
		Access:	R/W
		invalid_varmtrr_memtype_value_rd.	
	6	**Error3 Error Bits 6**	
		Default Value:	0b
		Project:	CHV, BSW
		Access:	R/W
		invalid_varmtrr_memtype_value_wr.	
	5	**Error3 Error Bits 5**	
		Default Value:	0b
		Project:	CHV, BSW
		Access:	R/W
		invalid_fixedmtrr_memtype_value_rd.	
	4	**Error3 Error Bits 4**	

ERROR_3 - Main Graphic Arbiter Error Report 3

		Default Value:	0b
		Project:	CHV, BSW
		Access:	R/W
		invalid_fixedmtrr_memtype_value_wr.	
	3	**Error3 Error Bits 3**	
		Default Value:	0b
		Project:	CHV, BSW
		Access:	R/W
		gttc_internal_error.	
	2	**Error3 Error Bits 2**	
		Default Value:	0b
		Project:	CHV, BSW
		Access:	R/W
		ctrl_pavp_invalidate_err.	
	1	**Error3 Error Bits 1**	
		Default Value:	0b
		Access:	R/W
		tlbpend_internal_error.	
	0	**Error3 Error Bits 0**	
		Default Value:	0b
		Access:	R/W
		reg_wrid_internal_error.	

Main Graphic Arbiter Error Report Register

GFX_ARB_ERROR_RPT - Main Graphic Arbiter Error Report Register		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	040A0h	
This register is used to report error conditions. Error bits are writable.		

DWord	Bit	Description
0	31:16	**Reserved** Format: MBZ
	15:9	**Reserved**
	8	**Unloaded PD Error** The Cache Line containing a PD entry being accessed was marked as invalid in the last PD load cycle.
	7	**Reserved**
	6	**Reserved**
	5	**Reserved**
	4	**Reserved**
	3	**Hardware Status Page Fault Error** HWSP's GTT translation generated a page fault (GTT entry not valid).
	2	**Invalid Page Directory entry error** PD entry's valid bit is 0.
	1	**Context Page Fault Error** A Context Page's GTT translation generated a page fault (GTT entry not valid).
	0	**TLB Page Fault Error** A TLB Page's GTT translation generated a page fault (GTT entry not valid).

MASTER_INT_CTL

MASTER_INT_CTL - MASTER_INT_CTL	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	44200h

This register has the master enable for graphics interrupts and gives an overview of what interrupts are pending.
An interrupt pending bit will read 1b while one or more interrupts of that category are set (IIR) and enabled (IER).
All Pending Interrupts are ORed together to generate the combined interrupt.
The combined interrupt is ANDed with the Master Interrupt enable to create the master enabled interrupt.
The master enabled interrupt goes to PCI device 2 interrupt processing.
The master interrupt enable must be set before any of these interrupts will propagate to PCI device 2 interrupt processing.

DWord	Bit	Description
0	31	**MASTER_INTERRUPT_ENABLE**
		Default Value: 0b
		Access: R/W
		THIS IS THE MASTER CONTROL FOR GRAPHICS INTERRUPT. this must be enabled for any of these interrupts to propagate to PCI dev2 interrupt processing. 0b - master interrupt disable, 1b - master interrupt enable
	30	**PCU_INTERRUPT_PENDING**
		Default Value: 0b
		Access: RO
		This field indicates if iterrups of this category is pending.
	29:8	**Reserved**
		Default Value: 00000b
		Access: RO
		Reserved
	7	**WDBOX_OACS_INTERRUPT_PENDING**
		Default Value: 0b
		Access: RO
		This field indicates if iterrups of this category is pending.
	6	**VEBOX_INTERRUPT_PENDING**
		Default Value: 0b

MASTER_INT_CTL - MASTER_INT_CTL

		Access:	RO
		This field indicates if iterrups of this category is pending.	
	5	**Reserved**	
	4	**GTPM_INTERRUPT_PENDING**	
		Default Value:	0b
		Access:	RO
		This field indicates if iterrups of this category is pending.	
	3	**VCS2_INTERRUPT_PENDING**	
		Default Value:	0b
		Access:	RO
		This field indicates if iterrups of this category is pending.	
	2	**VCS1_INTERRUPT_PENDING**	
		Default Value:	0b
		Access:	RO
		This field indicates if iterrups of this category is pending.	
	1	**BLITTER_INTERRUPT_PENDING**	
		Default Value:	0b
		Access:	RO
		This field indicates if iterrups of this category is pending.	
	0	**RENDER_INTERRUPT_PENDING**	
		Default Value:	0b
		Access:	RO
		This field indicates if iterrups of this category is pending.	

Master start timer

MASTIMER - Master start timer		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000001	
Size (in bits):	32	
Address:	0B438h	
DWord	**Bit**	**Description**
0	31:0	**Master start timer value**

Default Value:	00000000000000000000000000000001b
Access:	R/W

Master Start Timer (MSTSTTMR).
lpconf_lpfc_master_start_timer [31:0].So many clocks are expired before starting the rest of the counters. Time to wait is 256 * value clocks.
Value for this register cannot be 0.

Max Outstanding Pending TLB Requests 0

GFX_PEND_TLB_0 - Max Outstanding Pending TLB Requests 0	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	04034h

DWord	Bit	Description
0	31	**TEX Limit Enable Bit**
		Default Value: 0b
		Access: R/W
		This bit is used to enable the pending TLB requests limitation function for the Texture Cache. When set, the number of internal pending read requests which require a TLB read does not exceed the programmed counter value.
	30	**Reserved**
		Default Value: 0b
		Access: RO
	29:24	**TEX TLB Limit Count**
		Default Value: 000000b
		Access: R/W
		This is the MAX number of Allowed internal pending read requests which require a TLB read.
	23	**DC Limit Enable Bit**
		Default Value: 0b
		Access: R/W
		This bit is used to enable the pending TLB requests limitation function for the Instruction Cache. When set, the number of internal pending read requests which require a TLB read does not exceed the programmed counter value.
	22	**Reserved**
		Default Value: 0b
		Access: RO
	21:16	**DC TLB Limit Count**
		Default Value: 000000b
		Access: R/W
		This is the MAX number of Allowed internal pending read requests which require a TLB read.

GFX_PEND_TLB_0 - Max Outstanding Pending TLB Requests 0

<table>
<tr><td>15</td><td colspan="2">VF Limit Enable Bit</td></tr>
<tr><td></td><td>Default Value:</td><td>0b</td></tr>
<tr><td></td><td>Access:</td><td>R/W</td></tr>
<tr><td></td><td colspan="2">This bit is used to enable the pending TLB requests limitation function for the Vertex Fetch. When set, the number of internal pending read requests which require a TLB read does not exceed the programmed counter value.</td></tr>
<tr><td>14</td><td colspan="2">Reserved</td></tr>
<tr><td></td><td>Default Value:</td><td>0b</td></tr>
<tr><td></td><td>Access:</td><td>RO</td></tr>
<tr><td>13:8</td><td colspan="2">VF TLB Limit Count</td></tr>
<tr><td></td><td>Default Value:</td><td>000000b</td></tr>
<tr><td></td><td>Access:</td><td>R/W</td></tr>
<tr><td></td><td colspan="2">This is the MAX number of Allowed internal pending read requests which require a TLB read.</td></tr>
<tr><td>7</td><td colspan="2">VMC Limit Enable bit</td></tr>
<tr><td></td><td>Default Value:</td><td>0b</td></tr>
<tr><td></td><td>Access:</td><td>R/W</td></tr>
<tr><td></td><td colspan="2">This bit is used to enable the pending TLB requests limitation function for the Video Motion Compensation. When set, the number of internal pending read requests which require a TLB read does not exceed the programmed counter value.</td></tr>
<tr><td>6</td><td colspan="2">Reserved</td></tr>
<tr><td></td><td>Default Value:</td><td>0b</td></tr>
<tr><td></td><td>Access:</td><td>RO</td></tr>
<tr><td>5:0</td><td colspan="2">VMC TLB Limit Count</td></tr>
<tr><td></td><td>Default Value:</td><td>000000b</td></tr>
<tr><td></td><td>Access:</td><td>R/W</td></tr>
<tr><td></td><td colspan="2">This is the MAX number of Allowed internal pending read requests which require a TLB read.</td></tr>
</table>

Max Outstanding Pending TLB Requests 1

GFX_PEND_TLB_1 - Max Outstanding Pending TLB Requests 1	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	04038h

DWord	Bit	Description
0	31	**SOL Limit Enable Bit** Default Value: 0b Access: R/W This bit is used to enable the pending TLB requests limitation function for the SOL. When set, the number of internal pending read requests which require a TLB read does not exceed the programmed counter value.
	30	**Reserved** Default Value: 0b Access: RO
	29:24	**SOL TLB Limit Count** Default Value: 000000b Access: R/W This is the MAX number of Allowed internal pending read requests which require a TLB read.
	23	**L3 Limit Enable Bit** Default Value: 0b Access: R/W This bit is used to enable the pending TLB requests limitation function for the L3. When set, the number of internal pending read requests which require a TLB read does not exceed the programmed counter value.
	22	**Reserved** Default Value: 0b Access: RO
	21:16	**L3 TLB Limit Count** Default Value: 000000b Access: R/W This is the MAX number of Allowed internal pending read requests which require a TLB read.

GFX_PEND_TLB_1 - Max Outstanding Pending TLB Requests 1

15	**RCZ Limit Enable Bit**	
	Default Value:	0b
	Access:	R/W
	This bit is used to enable the pending TLB requests limitation function for the Render Depth Cache. When set, the number of internal pending read requests which require a TLB read does not exceed the programmed counter value.	

14	**Reserved**	
	Default Value:	0b
	Access:	RO

13:8	**RCZ TLB Limit Count**	
	Default Value:	000000b
	Access:	R/W
	RCZ TLB Limit Count Project: All Format: U6 This is the MAX number of Allowed internal pending read requests which require a TLB read.	

7	**RCC Limit Enable bit**	
	Default Value:	0b
	Access:	R/W
	This bit is used to enable the pending TLB requests limitation function for the Render Color Cache. When set, the number of internal pending read requests which require a TLB read does not exceed the programmed counter value.	

6	**Reserved**	
	Default Value:	0b
	Access:	RO

5:0	**RCC TLB Limit Count**	
	Default Value:	000000b
	Access:	R/W
	This is the MAX number of Allowed internal pending read requests which require a TLB read.	

MAX Requests Allowed - GAM

GFX_MAX_REQ_COUNT - MAX Requests Allowed - GAM	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x43F20101
Size (in bits):	32
Address:	04AA4h

Programmable Request Count - GAM

DWord	Bit	Description
0	31:26	**GAP Writes Max Request Limit Count** <table><tr><td>Default Value:</td><td>010000b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> This is the MAX number of Allowed Write Requests Count - These counters keep track of the accepted write requests from all GAP clients (RCZ, HiZ, Stc, RCC, L3). Minimum count value must be = 1.
	25:20	**CVS Max Request Limit Count** <table><tr><td>Default Value:</td><td>111111b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> This is the MAX number of Allowed Requests Count - These counters keep track of the accepted requests from each client. Requests are counted, regardless of kind of cycle (Miss/Hit/Present). Minimum count value must be = 1.
	19	**Reserved** <table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>RO</td></tr></table>
	18:13	**L3 Max Request Limit Count** <table><tr><td>Default Value:</td><td>010000b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> This is the MAX number of Allowed Requests Count - These counters keep track of the accepted requests from each client. Requests are counted, regardless of kind of cycle (Miss/Hit/Present). Minimum count value must be = 1.
	12	**Reserved** <table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>RO</td></tr></table>

GFX_MAX_REQ_COUNT - MAX Requests Allowed - GAM

	11:6	**Z Request Limit Count**	
		Default Value:	000100b
		Access:	R/W
		This is the MAX number of Allowed Requests Count - These counters keep track of the accepted requests from each client. Requests are counted, regardless of kind of cycle (Miss/Hit/Present). Minimum count value must be = 1.	
	5:0	**RCC Request Limit Count**	
		Default Value:	000001b
		Access:	R/W
		This is the MAX number of Allowed Requests Count - These counters keep track of the accepted requests from each client. Requests are counted, regardless of kind of cycle (Miss/Hit/Present). Minimum count value must be = 1.	

MAX Requests Allowed - MFX

MEDIA_MAX_REQ_COUNT - MAX Requests Allowed - MFX	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x10201020
Size (in bits):	32
Address:	04AA0h

Programmable Request Count - MFX

DWord	Bit	Description
0	31:24	**GFX Max Request Limit Count**
		Default Value: 00010000b
		Access: R/W
		This is the MAX number of Allowed Requests Count - These counters keep track of the accepted requests from each engine. Requests are counted, regardless of kind of cycle (Miss/Hit/Present). Minimum count value must be = 1.
	23:16	**MFX Max Request Limit Count**
		Default Value: 00100000b
		Access: R/W
		This is the MAX number of Allowed Requests Count - These counters keep track of the accepted requests from each engine. Requests are counted, regardless of kind of cycle (Miss/Hit/Present). Minimum count value must be = 1.
	15:14	**Reserved**
		Default Value: 00b
		Access: RO
	13:8	**VLF Max Request Limit Count**
		Default Value: 010000b
		Access: R/W
		This is the MAX number of Allowed Requests Count - These counters keep track of the accepted requests from each client. Requests are counted, regardless of kind of cycle (Miss/Hit/Present). Minimum count value must be = 1.
	7:6	**Reserved**
		Default Value: 00b
		Access: RO

MEDIA_MAX_REQ_COUNT - MAX Requests Allowed - MFX

5:0	**MFX Max Request Limit Count**	
	Default Value:	100000b
	Access:	R/W
	This is the MAX number of Allowed Requests Count - These counters keep track of the accepted requests from each client. Requests are counted, regardless of kind of cycle (Miss/Hit/Present). Minimum count value must be = 1.	

MAX Requests Allowed - VEBX and BLT

VEBX_BLIT_MAX_REQ_COUNT - MAX Requests Allowed - VEBX and BLT	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x08081020
Size (in bits):	32
Address:	04AA8h

Programmable Request Count - VEBX and BLT

DWord	Bit	Description	
0	31:24	**BLT Max Request Limit Count**	
		Default Value:	00001000b
		Access:	R/W
		This is the MAX number of Allowed Requests Count - These counters keep track of the accepted requests from each engine. Requests are counted, regardless of kind of cycle (Miss/Hit/Present).	
	23:16	**VEBX Max Request Limit Count**	
		Default Value:	00001000b
		Access:	R/W
		This is the MAX number of Allowed Requests Count - These counters keep track of the accepted requests from each engine. Requests are counted, regardless of kind of cycle (Miss/Hit/Present).	
	15:8	**VLF1 Max Request Limit Count**	
		Default Value:	00010000b
		Access:	R/W
		This is the MAX number of Allowed Requests Count - These counters keep track of the accepted requests from each engine. Requests are counted, regardless of kind of cycle (Miss/Hit/Present).	
	7:0	**MFX1 Max Request Limit Count**	
		Default Value:	00100000b
		Access:	R/W
		This is the MAX number of Allowed Requests Count - These counters keep track of the accepted requests from each engine. Requests are counted, regardless of kind of cycle (Miss/Hit/Present).	

MBC Control Register

<table>
<tr><td colspan="3" align="center">**MBCTL - MBC Control Register**</td></tr>
<tr><td colspan="3">Register Space: MMIO: 0/2/0</td></tr>
<tr><td colspan="3">Project: CHV, BSW</td></tr>
<tr><td colspan="3">Source: PRM</td></tr>
<tr><td colspan="3">Default Value: 0x00000000</td></tr>
<tr><td colspan="3">Size (in bits):   32</td></tr>
<tr><td colspan="3">Address: 0907Ch</td></tr>
<tr><td colspan="3">MBC Control Register</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td align="center">**Description**</td></tr>
<tr><td>0</td><td>31:17</td><td>**ECORSVD**

Access: R/W

ECO purposes Reserved</td></tr>
<tr><td></td><td>16</td><td>**Fuse Write to VCR as Nonposted**

Access: R/W

0 - Default - MBCunit will send the VCR (Fuse) writes as Posted Write cycles
1 - MBCunit will send the VCR (Fuse) writes as Non Posted Write cycles</td></tr>
<tr><td></td><td>15:8</td><td>**RSVD**

Access: RO

RSVD</td></tr>
<tr><td></td><td>7</td><td>**Disable Wait for G3d Outbound emtpy in MAE**

Access: R/W

0 - Wait for SQempty for MAE update Flow
1 - MBC MAE update FSM will not wait for the SQempty to complete the FSM</td></tr>
<tr><td></td><td>6:5</td><td>**RSVD**

Access: RO

RSVD</td></tr>
<tr><td></td><td>4</td><td>**RSVD**

Access: RO

RSVD</td></tr>
<tr><td></td><td>3</td><td>**RSVD**

Access: RO

RSVD</td></tr>
</table>

MBCTL - MBC Control Register

	2	**BME Update Enable**
		<table><tr><td>Access:</td><td>R/W</td></tr></table> BME update Enable - 0 - Default Mae Update is not Enable. MBC will ignore all theBME updates from SA. 1- BME update is Enabled.
	1	**MAE Update Enable**
		<table><tr><td>Access:</td><td>R/W</td></tr></table> MAE update Enable - 0 - Default Mae Update is not Enable. MBC will ignore all the MAE updates from SA. 1- MAE update is Enabled. MBC will respond to the MAE updates.
	0	**RSVD**
		<table><tr><td>Access:</td><td>RO</td></tr></table> 0 = Use MBC to GAM path with 8B reads (default) 1 = Use MBC to Config Agent register interface with 4B reads

MBDSM

<table>
<tr><td colspan="3" align="center">**MBDSM - MBDSM**</td></tr>
<tr><td>Register Space:</td><td colspan="2">MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td colspan="2">CHV, BSW</td></tr>
<tr><td>Source:</td><td colspan="2">PRM</td></tr>
<tr><td>Default Value:</td><td colspan="2">0x00000000</td></tr>
<tr><td>Size (in bits):</td><td colspan="2">32</td></tr>
<tr><td>Address:</td><td colspan="2">1080C0h</td></tr>
<tr><td colspan="3">Mirror of base of data stolen memory. Simply a read-only alias to the configuration registers.
Used by the MBC for boot context fetches.
This register contains the base address of Graphics Data Stolen DRAM memory. Note: This register is in device 0, 0xB0. Mirrored into device2, 0x5C.Graphics Stolen Memory is within DRAM space. The base of stolen memory will always be below 4G</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td>**Description**</td></tr>
<tr><td>0</td><td>31:20</td><td>**BDSM**
<table><tr><td>Default Value:</td><td>000h</td></tr><tr><td>Access:</td><td>RO</td></tr></table>BDSM: BASE_OF_Data_STOLEN_MEMORY.
This register contains bits 31 to 20 of the base address of Data stolen DRAM memory. For certain GTLC generated accesses, this base register will be added to GTLC provided offset address, forming the full physical address for the PFI fabric. This is also used as a base for VGA paged accesses.</td></tr>
<tr><td></td><td>19:1</td><td>**RESERVED**
<table><tr><td>Default Value:</td><td>00000h</td></tr><tr><td>Access:</td><td>RO</td></tr></table>Reserved</td></tr>
<tr><td></td><td>0</td><td>**BDSM_LOCK**
<table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>RO</td></tr></table>When set to 1b, this bit will lock all the bits in this register, including itself</td></tr>
</table>

MBGSM

<table>
<tr><td colspan="3" align="center">**MBGSM - MBGSM**</td></tr>
<tr><td>Register Space:</td><td colspan="2">MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td colspan="2">CHV, BSW</td></tr>
<tr><td>Source:</td><td colspan="2">PRM</td></tr>
<tr><td>Default Value:</td><td colspan="2">0x00000000</td></tr>
<tr><td>Size (in bits):</td><td colspan="2">32</td></tr>
<tr><td>Address:</td><td colspan="2">108100h</td></tr>
<tr><td colspan="3">Mirror of base of graphics stolen memory. Simply a read-only alias to the configuration registers.
Used by the MBC for boot context fetches.
Base of GTT table in Gfx Stolen Memory Note : This register is located in device 0, 0xB4. Mirrored into Device 2.
The GTT table is located within Graphics Stolen Memory in DRAM space.
The base of stolen memory will always be below 4G.</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td>**Description**</td></tr>
<tr><td>0</td><td>31:20</td><td>**BGSM**

Default Value: 000h

Access: RO

BGSM: Gfx Base of GTT Stolen Memory. This register contains bits 31 to 20 of the base address of GTT Table in stolen DRAM memory.
BIOS determines base of GTT stolen memory by subtracting the GTT graphics stolen memory size (PCI offset 50 bits 9:8) from the
Graphics Base of Data stolen(PCI offset 5C bits 31:20).</td></tr>
<tr><td></td><td>19:1</td><td>**RESERVED**

Default Value: 00000h

Access: RO

Reserved</td></tr>
<tr><td></td><td>0</td><td>**BGSM_LOCK**

Default Value: 0b

Access: RO

This bit will lock all writeable settings in this register including itself</td></tr>
</table>

MD

<table>
<tr><td colspan="4" align="center">**MD - MD**</td></tr>
<tr><td colspan="4">Register Space: PCI: 0/2/0</td></tr>
<tr><td colspan="4">Project: CHV, BSW</td></tr>
<tr><td colspan="4">Source: PRM</td></tr>
<tr><td colspan="4">Default Value: 0x00000000</td></tr>
<tr><td colspan="4">Size (in bits):   32</td></tr>
<tr><td colspan="4">Address: 00098h</td></tr>
<tr><td colspan="4">Message Data</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td colspan="2">**Description**</td></tr>
<tr><td>0</td><td>31:16</td><td colspan="2">**RESERVED**</td></tr>
<tr><td></td><td></td><td>Default Value:</td><td>0000h</td></tr>
<tr><td></td><td></td><td>Access:</td><td>RO</td></tr>
<tr><td></td><td></td><td colspan="2">Reserved</td></tr>
<tr><td></td><td>15:0</td><td colspan="2">**DATA**</td></tr>
<tr><td></td><td></td><td>Default Value:</td><td>0000h</td></tr>
<tr><td></td><td></td><td>Access:</td><td>R/W</td></tr>
<tr><td></td><td></td><td colspan="2">MD: This 16-bit field is programmed by system software. This forms the lower word of data for the MSI write transaction.</td></tr>
</table>

MEDFW_ACK

MEDFW_ACK - MEDFW_ACK	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	1300BCh

This register contains the per thread force wake acknowledge bits for the Media power well.

DWord	Bit	Description	
0	31:16	**RESERVED**	
		Default Value:	0000h
		Access:	RO
		Reserved.	
	15:0	**FWAKEMEDIAACK**	
		Default Value:	0000h
		Access:	RO
		Force Wake Media request bits. Driver must poll on the corresponding bit to confirm that the well has woken. For example, if 13_00B8[0] is written to a 1 (along with 13_00B8[16]='1'), then bit0 of this register indicates when the force wake request has been completed.	

Media 1 TLB Control Register

<table>
<tr><td colspan="3" align="center">**M1TCR - Media 1 TLB Control Register**</td></tr>
<tr><td colspan="3">Register Space: MMIO: 0/2/0</td></tr>
<tr><td colspan="3">Project: CHV, BSW</td></tr>
<tr><td colspan="3">Source: PRM</td></tr>
<tr><td colspan="3">Default Value: 0x00000000</td></tr>
<tr><td colspan="3">Size (in bits):   32</td></tr>
<tr><td colspan="3">Address: 04264h</td></tr>
</table>

DWord	Bit	Description
0	31:1	**Reserved** Default Value: 0000000000000000000000000000000b Access: RO
	0	**Invalidate TLBs on the corresponding Engine** Default Value: 0b Access: R/W SW writes 1 to invalidate the TLBs for the associated engine and HW clears the bit when invalidation is complete. To ensure proper invalidation of the TLBs, SW has to ensure the corresponding engine's HW pipeline is flushed and cleared from all its memory accesses. Otherwise HW cannot guarantee the proper invalidation for TLBs. This bit is self clear.

Media 2 TLB Control Register

M2TCR - Media 2 TLB Control Register	

Register Space: MMIO: 0/2/0

Project: CHV, BSW

Source: PRM

Default Value: 0x00000000

Size (in bits): 32

Address: 04268h

DWord	Bit	Description
0	31:1	**Reserved**
		Default Value: 0000000000000000000000000000000b
		Access: RO
	0	**Invalidate TLBs on the corresponding Engine**
		Default Value: 0b
		Access: R/W
		SW writes 1 to invalidate the TLBs for the associated engine and HW clears the bit when invalidation is complete. To ensure proper invalidation of the TLBs, SW has to ensure the corresponding engine's HW pipeline is flushed and cleared from all its memory accesses. Otherwise HW cannot guarantee the proper invalidation for TLBs. This bit is self clear.

Media forcewake request

<table>
<tr><td colspan="2" align="center">**MEDFW_REQ - Media forcewake request**</td></tr>
<tr><td>Register Space:</td><td>MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td>CHV, BSW</td></tr>
<tr><td>Source:</td><td>PRM</td></tr>
<tr><td>Default Value:</td><td>0x00000000</td></tr>
<tr><td>Size (in bits):</td><td>32</td></tr>
<tr><td>Address:</td><td>1300B8h</td></tr>
</table>

This register contains per thread force wake request bits for the Render power Well. The upper 16 bits act as masks for the lower 16 bits. Bit 31 masks bit 15 and bit 16 masks bit 0.

1. Driver writes to GPM force wake request bit. (VV will have a Render(13_00B0(15:0)) and a Media (13_00B8(15:0)) bits.)

2. The GPM responds by writing (via PLINK) to 1300B4[15:0] or 1300BC[15:0] register.

3. Driver polls (1300B4[15:0] and/or 1300BC[15:0])status until 1... indicating that that well has completed wake sequence.

Since the registers are per thread, only the specific bit that was forced should be checked for status.

DWord	Bit	Description
0	31:16	**FWAKEMEDIAREQMSK**
		<table><tr><td>Default Value:</td><td>0000h</td></tr><tr><td>Access:</td><td>RO</td></tr></table> Mask bits for lower 16 bits to avoid a read modify/write. If '0', the corresponding bit in [15:0] is not changed. If '1', the corresponding bit in [15:0] is changed to the value in [15:0]
	15	**FWAKEMEDIAREQ15**
		<table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> Force Wake Media request 15.
	14	**FWAKEMEDIAREQ14**
		<table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> Force Wake Render request 14.
	13	**FWAKEMEDIAREQ13**
		<table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table>

MEDFW_REQ - Media forcewake request

		Force Wake Render request 13.	
	12	**FWAKEMEDIAREQ12**	
		Default Value:	0b
		Access:	R/W
		Force Wake Render request 12.	
	11	**FWAKEMEDIAREQ11**	
		Default Value:	0b
		Access:	R/W
		Force Wake Render request 11.	
	10	**FWAKEMEDIAREQ10**	
		Default Value:	0b
		Access:	R/W
		Force Wake Render request 10.	
	9	**FWAKEMEDIAREQ9**	
		Default Value:	0b
		Access:	R/W
		Force Wake Render request 9.	
	8	**FWAKEMEDIAREQ8**	
		Default Value:	0b
		Access:	R/W
		Force Wake Render request 8.	
	7	**FWAKEMEDIAREQ7**	
		Default Value:	0b
		Access:	R/W
		Force Wake Render request 7.	
	6	**FWAKEMEDIAREQ6**	
		Default Value:	0b
		Access:	R/W
		Force Wake Render request 6.	
	5	**FWAKEMEDIAREQ5**	
		Default Value:	0b

MEDFW_REQ - Media forcewake request

			Access:	R/W
		Force Wake Render request 5.		
	4	**FWAKEMEDIAREQ4**		
			Default Value:	0b
			Access:	R/W
		Force Wake Render request 4.		
	3	**FWAKEMEDIAREQ3**		
			Default Value:	0b
			Access:	R/W
		Force Wake Render request 3.		
	2	**FWAKEMEDIAREQ2**		
			Default Value:	0b
			Access:	R/W
		Force Wake Render request 2.		
	1	**FWAKEMEDIAREQ1**		
			Default Value:	0b
			Access:	R/W
		Force Wake Render request 1.		
	0	**FWAKEMEDIAREQ0**		
			Default Value:	0b
			Access:	R/W
		Force Wake Render request 0.		

Media Power Meter Counter

MPMCNT - Media Power Meter Counter		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A270h-0A273h	

DWord	Bit	Description	
0	31	**Media Power Meter Counter Overflow**	
		Access:	RO
	30:0	**Media PWRMTR Counter**	
		Access:	RO

Media Power Meter Counter No Clear

MPMCNTCLR - Media Power Meter Counter No Clear		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A288h-0A28Bh	
Formerly cleared the count and the overflow bit, but now it is just a read-only value.		
DWord	**Bit**	**Description**
0	31	**Media Power Meter Counter Overflow No Clear**
		Access: RO
		Formerly cleared the overflow bit, but now it is just a read-only value.
	30:0	**Media PWRMTR Counter No Clear**
		Access: RO
		Formerly cleared the count, but now is just a read-only value.

MEDIARC0COUNTER

MEDIARC0COUNTER - MEDIARC0COUNTER	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	13811Ch

Description	Project
This register contains the total RC0 residency (Media powered on and clocks running) time that Media was in since boot. SOXi Context Save/Restore : No The 40-bit HW counter will wrap around. The only clear condition is CZ reset. When 0x13_8104[15] is set to zero, bits 31:0 of the 40-bit counter are reported. When 0x13_8104[15] is set to one, bits 39:8 of the 40-bit counter are reported. The units are CZ clock cycles. It is up to SW to periodically read this register and do a difference from the last time it was read. The primary usage for this register is for power characterization. 0x13_8104[5] controls if this register should count or if it should be gated: 0= clear, 1=count This register will be cleared when A024[8] is set to 1	CHV, BSW
This register contains the total RC0 residency (Media powered on and clocks running) time that Media was in since boot. SOXi Context Save/Restore : No The 40-bit HW counter will wrap around. The only clear condition is CZ reset. When 0x13_8104[15] is set to zero, bits 31:0 of the 40-bit counter are reported. When 0x13_8104[15] is set to one, bits 39:8 of the 40-bit counter are reported. The units are CZ clock cycles. It is up to SW to periodically read this register and do a difference from the last time it was read. The primary usage for this register is for power characterization. 0x13_8104[5] controls if this register should count or if it should be gated: 0= clear, 1=count	CHV, BSW

DWord	Bit	Description	
0	31:0	**MEDIARC0TIME**	
		Default Value:	00000000h
		Access:	RO
		Media RC0 Residency Counter.	

MEDIARC1COUNTER

MEDIARC1COUNTER - MEDIARC1COUNTER	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	138114h

This register contains the total RC1 residency (Media powered on and clock gated) time that Media was in since boot.

SOXi Context Save/Restore : No

The 40-bit HW counter will wrap around. The only clear condition is CZ reset.

When 0x13_8104[15] is set to zero, bits 31:0 of the 40-bit counter are reported. When 0x13_8104[15] is set to one, bits 39:8 of the 40-bit counter are reported.

The units are CZ clock cycles.

It is up to SW to periodically read this register and do a difference from the last time it was read. The primary usage for this register is for power characterization.

0x13_8104[3] controls if this register should count or if it should be gated: 0= clear, 1=count

DWord	Bit	Description	
0	31:0	**MEDIARC1TIME**	
		Default Value:	00000000h
		Access:	RO
		Media RC1 Residency Counter.	

MEMBOUNDCOUNTER

MEMBOUNDCOUNTER - MEMBOUNDCOUNTER		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	138120h	

SOXi Context Save/Restore : No
The 40-bit HW counter will wrap around. The only clear condition is CZ reset.
When 0x13_8104[15] is set to zero, bits 31:0 of the 40-bit counter are reported. When 0x13_8104[15] is set to one, bits 39:8 of the 40-bit counter are reported.
The units are CZ clock cycles.
It is up to SW to periodically read this register and do a difference from the last time it was read. The primary usage for this register is for power characterization.
0x13_8104[6] controls if this register should count or if it should be gated: 0= clear, 1=count

DWord	Bit	Description	
0	31:0	**MEMBOUNDTIME**		
		Default Value:	00000000h
		Access:	RO
		Render RC0 Residency Counter.	

Message Register

<table>
<tr><td colspan="3" align="center">**MSGREG - Message Register**</td></tr>
<tr><td>Register Space:</td><td colspan="2">MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td colspan="2">CHV, BSW</td></tr>
<tr><td>Source:</td><td colspan="2">PRM</td></tr>
<tr><td>Default Value:</td><td colspan="2">0x00000001</td></tr>
<tr><td>Size (in bits):</td><td colspan="2">32</td></tr>
<tr><td>Address:</td><td colspan="2">040D4h</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td>**Description**</td></tr>
<tr><td rowspan="7">0</td><td>31:16</td><td>**Mask Bits**
Default Value: 0000h
Access: RO
Reserved.</td></tr>
<tr><td>15</td><td>**GO_PROTOCOL_GAM_REQUEST15**
Default Value: 0b
Access: R/W
Reserved.</td></tr>
<tr><td>14</td><td>**GO_PROTOCOL_GAM_REQUEST14**
Default Value: 0b
Access: R/W
Reserved.</td></tr>
<tr><td>13</td><td>**GO_PROTOCOL_GAM_REQUEST13**
Default Value: 0b
Access: R/W
Reserved.</td></tr>
<tr><td>12</td><td>**GO_PROTOCOL_GAM_REQUEST12**
Default Value: 0b
Access: R/W
Reserved.</td></tr>
<tr><td>11</td><td>**GO_PROTOCOL_GAM_REQUEST11**
Default Value: 0b
Access: R/W
Reserved.</td></tr>
<tr><td>10</td><td>**GO_PROTOCOL_GAM_REQUEST10**
Default Value: 0b
Access: R/W
Reserved.</td></tr>
</table>

		MSGREG - Message Register		
	9	**GO_PROTOCOL_GAM_REQUEST9**		
		Default Value:		0b
		Access:		R/W
		Reserved.		
	8	**GO_PROTOCOL_GAM_REQUEST8**		
		Default Value:		0b
		Access:		R/W
		Reserved.		
	7	**GO_PROTOCOL_GAM_REQUEST7**		
		Default Value:		0b
		Access:		R/W
		Reserved.		
	6	**GO_PROTOCOL_GAM_REQUEST6**		
		Default Value:		0b
		Access:		R/W
		Reserved.		
	5	**GO_PROTOCOL_GAM_REQUEST5**		
		Default Value:		0b
		Access:		R/W
		Reserved.		
	4	**GO_PROTOCOL_GAM_REQUEST4**		
		Default Value:		0b
		Access:		R/W
		Reserved.		
	3	**GO_PROTOCOL_GAM_REQUEST3**		
		Default Value:		0b
		Access:		R/W
		Reserved.		
	2	**GO_PROTOCOL_GAM_REQUEST2**		
		Default Value:		0b
		Access:		R/W
		Reserved.		
	1	**GO_PROTOCOL_GAM_REQUEST1**		
		Default Value:		0b
		Access:		R/W
		Reserved.		
	0	**GO_PROTOCOL_GAM_REQUEST0**		
		Default Value:		1b

MSGREG - Message Register				
		Access:		R/W
		0 - GPM to GAM Busy Ack Indication.		
		1 - GPM to GAM Idle Ack Indication.		

Messaging Register for GPMunit

MSG_GPM - Messaging Register for GPMunit	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Default Value:	0x00000000
Size (in bits):	32
Address:	00C00h

Message registers have bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16].
To set bit0, for example, the data would be 0x0001_0001.
To clear bit0, for example, the data would be 0x0001_0000.
Note that mask bit is the data bit offset + 16. Message registers are protected from non-GT writes via the Message Channel.

DWord	Bit	Description	
0	31:16	**Reserved**	
		Access:	RO
	15	**GPM Messages Bit 15**	
		Access:	R/W
		Placeholder for GPM Messsages. RPMunit could self-clear these bits upon sampling.	
	14	**GPM Messages Bit 14**	
		Access:	R/W
		Placeholder for GPM Messsages. RPMunit could self-clear these bits upon sampling.	
	13	**GPM Messages Bit 13**	
		Access:	R/W
		Placeholder for GPM Messsages. RPMunit could self-clear these bits upon sampling.	
	12	**GPM Messages Bit 12**	
		Access:	R/W
		Placeholder for GPM Messsages. RPMunit could self-clear these bits upon sampling.	
	11	**GPM Messages Bit 11**	
		Access:	R/W
		Placeholder for GPM Messsages. RPMunit could self-clear these bits upon sampling.	

MSG_GPM - Messaging Register for GPMunit

10	**GPM Messages Bit 10**	
	Access:	R/W
	Placeholder for GPM Messsages. RPMunit could self-clear these bits upon sampling.	

9	**GPM Messages Bit 9**	
	Access:	R/W
	Placeholder for GPM Messsages. RPMunit could self-clear these bits upon sampling.	

8	**GPM Messages Bit 8**	
	Access:	R/W
	Placeholder for GPM Messsages. RPMunit could self-clear these bits upon sampling.	

7	**GPM Messages Bit 7**	
	Project:	CHV, BSW
	Access:	R/W
	Placeholder for GPM Messsages RPMunit could self-clear these bits upon sampling.	

6	**GPM Messages Bit 6**	
	Project:	CHV, BSW
	Access:	R/W
	Placeholder for GPM Messsages. RPMunit could self-clear these bits upon sampling.	

5	**GPM Messages Bit 5**	
	Project:	CHV, BSW
	Access:	R/W
	Placeholder for GPM Messsages. RPMunit could self-clear these bits upon sampling.	

4	**Request to send CPD Exit Ack Message on EventBus (U2C)**	
	Access:	R/W
	Request from GPMunit for RPMunit to send CPD_EXIT_ACK message on the Eventbus. RPMunit self-clears this bit upon sampling.	

3	**Request to send CPD Enter Ack Message on EventBus (U2C)**	
	Access:	R/W
	Request from GPMunit for RPMunit to send CPD_ENTER_ACK message on the Eventbus. RPMunit self-clears this bit upon sampling.	

		MSG_GPM - Messaging Register for GPMunit	
	2	**Request to send Credit Active Deassert Message on EventBus (U2C)**	
		Access:	R/W
		Request from GPMunit for RPMunit to send CREDIT_ACTIVE_DEASSERT message on the Eventbus. RPMunit self-clears this bit upon sampling.	
	1	**Request to send Credit Active Assert Message on EventBus (U2C)**	
		Access:	R/W
		Request from GPMunit for RPMunit to send CREDIT_ACTIVE_ASSERT message on the Eventbus. RPMunit self-clears this bit upon sampling.	
	0	**Request to send IDI Shutdown Ack Message on EventBus (U2C)**	
		Access:	R/W
		Request from GPMunit for RPMunit to send IDI_SHUTDOWN_ACK message on the Eventbus. RPMunit self-clears this bit upon sampling.	

Messaging Register for MDRBunit

MSG_MDRB - Messaging Register for MDRBunit		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Default Value:	0x00000001	
Size (in bits):	32	
Address:	00C08h	
Message registers have bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16]. To set bit0, for example, the data would be 0x0001_0001. To clear bit0, for example, the data would be 0x0001_0000. Note that mask bit is the data bit offset + 16. Message registers are protected from non-GT writes via the Message Channel.		

DWord	Bit	Description
0	31:16	**Reserved**
			Access:	RO	
	15:2	**MDRB Messages**
			Access:	R/W	
		Placeholder for MDRB Messsages. MDRBunit could self-clear these bits upon sampling.
	1	**RFO Enable/Disable Ack for RPM (internal) RFO Request**
			Access:	R/W	
		RFO Enable/Disable Ack for Internal RFO Request. Enable Ack = 1'b1 Disable Ack = 1'b0
	0	**RFO Enable/Disable Ack for U2C (Evtentbus) RFO Request**
			Default Value:	1b	
			Access:	R/W	
		RFO Enable/Disable Ack for U2C RFO Request. Enable Ack = 1'b1 Disable Ack = 1'b0

Messaging Register for MGSRunit

MSG_MGSR - Messaging Register for MGSRunit		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	00C04h	
Message registers have bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16]. To set bit0, for example, the data would be 0x0001_0001. To clear bit0, for example, the data would be 0x0001_0000. Note that mask bit is the data bit offset + 16. Message registers are protected from non-GT writes via the Message Channel.		

DWord	Bit	Description	
0	31:16	**Reserved**	
		Access:	RO
	15:0	**MGSR Messages**	
		Access:	R/W
		Placeholder for MGSR Messsages. MGSRunit could self-clear these bits upon sampling.	

MFC_AVC_CABAC_INSERTION_COUNT

AVC_CABAC_INSERTION_COUNT - MFC_AVC_CABAC_INSERTION_COUNT	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	128ACh
Valid Projects:	CHV, BSW

This register stores the count in bytes of **CABAC ZERO_WORD insertion. It is primarily provided for statistical data gathering.**

DWord	Bit	Description
0	31:0	**MFC AVC Cabac Insertion Count** Total number of bytes in the bitstream output before for the CABAC zero word insertion. This count is updated each time when the insertion count is incremented.

MFC_AVC Bitstream Decoding Front-End Parsing Logic Error Counter

<table>
<tr><td colspan="4" align="center">MFC_VIN_AVD_ERROR_CNTR - MFC_AVC Bitstream Decoding Front-End Parsing Logic Error Counter</td></tr>
<tr><td>Register Space:</td><td colspan="3">MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td colspan="3">CHV, BSW</td></tr>
<tr><td>Source:</td><td colspan="3">VideoCS</td></tr>
<tr><td>Default Value:</td><td colspan="3">0x00000000</td></tr>
<tr><td>Access:</td><td colspan="3">R/W</td></tr>
<tr><td>Size (in bits):</td><td colspan="3">32</td></tr>
<tr><td>Trusted Type:</td><td colspan="3">1</td></tr>
<tr><td>Address:</td><td colspan="3">12804h</td></tr>
<tr><td>Valid Projects:</td><td colspan="3">CHV, BSW</td></tr>
<tr><td align="center">DWord</td><td align="center">Bit</td><td colspan="2" align="center">Description</td></tr>
<tr><td align="center">0

avd_error_flagsR[31:0]</td><td align="center">31:0</td><td colspan="2">Reserved
<table><tr><td>Format:</td><td>MBZ</td></tr></table></td></tr>
</table>

MFC Image Status Control

<table>
<tr><td colspan="3" align="center">**MFC_IMAGE_STATUS_CONTROL - MFC Image Status Control**</td></tr>
<tr><td>Register Space:</td><td colspan="2">MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td colspan="2">CHV, BSW</td></tr>
<tr><td>Source:</td><td colspan="2">VideoCS</td></tr>
<tr><td>Default Value:</td><td colspan="2">0x00000000</td></tr>
<tr><td>Access:</td><td colspan="2">RO</td></tr>
<tr><td>Size (in bits):</td><td colspan="2">32</td></tr>
<tr><td>Trusted Type:</td><td colspan="2">1</td></tr>
<tr><td>Address:</td><td colspan="2">128B8h</td></tr>
<tr><td>Valid Projects:</td><td colspan="2">CHV, BSW</td></tr>
<tr><td colspan="3">This register stores the suggested data for next frame in multi-pass.</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td>**Description**</td></tr>
<tr><td>0</td><td>31:24</td><td>**Cumulative slice delta QP**</td></tr>
<tr><td></td><td>23:16</td><td>**QP Value**
suggested slice QP delta value for frame level Rate control. This value can be +ve or -ve</td></tr>
<tr><td></td><td>15</td><td>**QP-Polarity Change**
Cumulative slice delta QP polarity change.</td></tr>
<tr><td></td><td>14:13</td><td>**Num-Pass Polarity Change**
Number of passes after cumulative slice delta QP polarity changes.</td></tr>
<tr><td></td><td>12</td><td>**Reserved**
Project: CHV, BSW
Format: MBZ</td></tr>
<tr><td></td><td>11:8</td><td>**Total Num-Pass**</td></tr>
<tr><td></td><td>7:4</td><td>**Reserved**
Format: MBZ</td></tr>
<tr><td></td><td>3</td><td>**Missing Huffman Code**
Project: CHV, BSW
Jpeg HW encoder reports if Huffman table entry is missing.</td></tr>
<tr><td></td><td>2</td><td>**Panic**
Panic triggered to avoid too big packed file.</td></tr>
<tr><td></td><td>1</td><td>**Frame Bit Count**
Frame Bit count over-run/under-run flag</td></tr>
<tr><td></td><td>0</td><td>**Max Conformance Flag**
Max Macroblock conformance flag or Frame Bit count over-run/under-run</td></tr>
</table>

MFC Image Status Mask

MFC_IMAGE_STATUS_MASK - MFC Image Status Mask	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	128B4h
Valid Projects:	CHV, BSW

This register stores the image status(flags).

DWord	Bit	Description
0	31:0	**Control Mask** Control Mask for dynamic frame repeat.

MFC QP Status Count

MFC_QUP_CT - MFC QP Status Count	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	128BCh
Valid Projects:	CHV, BSW

This register stores the suggested QP COUNTS in multi-pass.

DWord	Bit	Description
0	31:24	**Cumulative QP Adjust**
		Format: U8
		Cumulative QP adjustment after multiple passes. If there is no need to multi-pass, this value would be zero. (This is in sign magnitude form).
	23:0	**Cumulative QP**
		Format: U24
		Cumulative QP for all MB of a Frame (Can be used for computing average QP).

MFD Error Status

MFD_ERROR_STATUS - MFD Error Status	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	12800h
Valid Projects:	CHV, BSW

This register stores the error status flags and count reports by the bit-stream decoder. This register is not part of hardware context save and restore. Driver should read the content prior to starting a new batch/frame.

DWord	Bit	Description
0	31:20	**Reserved** Format: MBZ This field is currently reserved
	19:16	**AVC Short Format Error Flags** Exists If: // AVC Short Format == Ture Bit-stream error detected by VLD short format bit-stream decoder. These flags are reset at the beginning of a frame and updated until starting of another frame. [19] – Slice Type SE Error Flag – Invalid Slice Type SE [18] – MMCO SE Error Flag – Invalid memory management control operation SE. MMCO Loop does not end (mmco control != 0) even after all MMCO SEs are decoded OR MMCO SEs are still being decoded and MMCO SE loop end (mmco control == 0) is hit [17] – Reordering IDC Error Flag – Syntax Element modification_of_pic_nums_idc >= 6 OR modification_of_pic_nums_idc != 3 (end of reordering loop) but reordering count has already hit maximum value [16] – Premature bitstream end is hit before finishing slice header decode
	15:0	**Bit-stream Error flags** Exists If: // AVC CAVLC, AVC CABAC, VC1 and MPEG2 == True Bitstream error detected by the VLD bit-steram decoder. These flags are reset at the beginning of a frame and updated until starting of another frame. AVC CAVLC: Please refer to AVC CAVLC table for each bit field AVC CABAC: Please refer to AVC CABAC table for each bit field VC1: Please refer to VC1 table for each bit field MPEG2: Please refer to MPEG2 table for each bit field

MFD Picture Parameter

<table>
<tr><td colspan="3" align="center">**MFD_PICTURE_PARAM - MFD Picture Parameter**</td></tr>
<tr><td>Register Space:</td><td colspan="2">MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td colspan="2">CHV, BSW</td></tr>
<tr><td>Source:</td><td colspan="2">VideoCS</td></tr>
<tr><td>Default Value:</td><td colspan="2">0x00000000</td></tr>
<tr><td>Access:</td><td colspan="2">R/W</td></tr>
<tr><td>Size (in bits):</td><td colspan="2">32</td></tr>
<tr><td>Trusted Type:</td><td colspan="2">1</td></tr>
<tr><td>Address:</td><td colspan="2">12820h</td></tr>
<tr><td>Valid Projects:</td><td colspan="2">CHV, BSW</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td>**Description**</td></tr>
<tr><td>0</td><td>31:0</td><td>**Reserved**

<table><tr><td>Format:</td><td>MBZ</td></tr></table></td></tr>
</table>

MFX_Memory_Latency_Count1

MFX_LAT_CT1 - MFX_Memory_Latency_Count1	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	12870h
Valid Projects:	CHV, BSW

This register stores the max and min memory latency counts reported on reference read requests. This register is not part of hardware context save and restore.

DWord	Bit	Description
0	31:24	**Max Request Count** This field indicates the maximum number of requests allowed by the memory sub-system channel.
	23:16	**Current Request Count** This field indicates the number of requests currently outstanding in the memory sub-system. This field should report with a value of zero at the end of frame; otherwise the motion compensation engine is most likely hung waiting for read data to be returned from sub-system.
	15:8	**MFX Reference picture read request - Max Latency Count in 8xMedia clock cycles** This field reports the maximum memory latency count on all reference reads requested by the motion compensation engine.
	7:0	**MFX Reference picture read request - Min Latency Count in 8xMedia clock cycles** This field reports the minimum memory latency count on all reference reads requested by the motion compensation engine.

MFX0 Context Element Descriptor (High Part)

MFX0_CTX_EDR_H - MFX0 Context Element Descriptor (High Part)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04444h	

DWord	Bit	Description
0	31:0	**MFX0 Context Element Descriptor (High Part)**
		Default Value: 00000000h
		Access: R/W

MFX0 Context Element Descriptor (Low Part)

MFX0_CTX_EDR_L - MFX0 Context Element Descriptor (Low Part)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000009	
Size (in bits):	32	
Address:	04440h	

DWord	Bit	Description	
0	31:0	**MFX0 Context Element Descriptor (Low Part)**	
		Default Value:	00000009h
		Access:	R/W

MFX0 Context Element Descriptor (Low Part)

MFX0_CTX_EDR_L - MFX0 Context Element Descriptor (Low Part)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000009	
Size (in bits):	32	
Address:	04440h	

DWord	Bit	Description	
0	31:0	**MFX0 Context Element Descriptor**	
		Default Value:	00000009h
		Access:	R/W

MFX0 Fault Counter

MFX0_FAULT_CNTR - MFX0 Fault Counter		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	045A8h	

DWord	Bit	Description
0	31:0	**MFX0 Fault Counter**
		Default Value: 00000000h
		Access: RO
		This counter only applies to advance context when fault and stream mode is selected.

MFX0 Fixed Counter

<table>
<tr><td colspan="2" align="center">**MFX0_FIXED_CNTR - MFX0 Fixed Counter**</td></tr>
<tr><td>Register Space:</td><td>MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td>CHV, BSW</td></tr>
<tr><td>Source:</td><td>PRM</td></tr>
<tr><td>Default Value:</td><td>0x00000000</td></tr>
<tr><td>Size (in bits):</td><td>32</td></tr>
<tr><td>Address:</td><td>045ACh</td></tr>
</table>

DWord	Bit	Description
0	31:0	**MFX0 Fixed Counter**

		Default Value:	00000000h
		Access:	RO

This counter only applies to advance context when fault and stream mode is selected.

MFX0 PDP0/PML4/PASID Descriptor (High Part)

MFX0_CTX_PDP0_H - MFX0 PDP0/PML4/PASID Descriptor (High Part)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0444Ch	

DWord	Bit	Description	
0	31:0	**MFX0 PDP0/PML4/PASID Descriptor (High Part)**	
		Default Value:	00000000h
		Access:	R/W

ers**

MFX0 PDP0/PML4/PASID Descriptor (Low Part)

MFX0_CTX_PDP0_L - MFX0 PDP0/PML4/PASID Descriptor (Low Part)	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	04448h

DWord	Bit	Description	
0	31:0	**MFX0 PDP0/PML4/PASID Descriptor (Low Part)**	
		Default Value:	00000000h
		Access:	R/W

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MFX0 PDP1 Descriptor Register (High Part)

MFX0_CTX_PDP1_H - MFX0 PDP1 Descriptor Register (High Part)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04454h	

DWord	Bit	Description	
0	31:0	**MFX0 PDP1 Descriptor Register (High Part)**	
		Default Value:	00000000h
		Access:	R/W

MFX0 PDP1 Descriptor Register (Low Part)

MFX0_CTX_PDP1_L - MFX0 PDP1 Descriptor Register (Low Part)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04450h	

DWord	Bit	Description
0	31:0	**MFX0 PDP1 Descriptor Register (Low Part)**
		Default Value: 00000000h
		Access: R/W

MFX0 PDP2 Descriptor Register (High Part)

MFX0_CTX_PDP2_H - MFX0 PDP2 Descriptor Register (High Part)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0445Ch	

DWord	Bit	Description
0	31:0	**MFX0 PDP2 Descriptor Register (High Part)**
		Default Value: 00000000h
		Access: R/W

MFX0 PDP2 Descriptor Register (Low Part)

MFX0_CTX_PDP2_L - MFX0 PDP2 Descriptor Register (Low Part)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04458h	

DWord	Bit	Description	
0	31:0	**MFX0 PDP2 Descriptor Register (Low Part)**	
		Default Value:	00000000h
		Access:	R/W

MFX0 PDP3 Descriptor Register (High Part)

MFX0_CTX_PDP3_H - MFX0 PDP3 Descriptor Register (High Part)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04464h	

DWord	Bit	Description	
0	31:0	**MFX0 PDP3 Descriptor Register (High Part)**	
		Default Value:	00000000h
		Access:	R/W

MFX0 PDP3 Descriptor Register (Low Part)

MFX0_CTX_PDP3_L - MFX0 PDP3 Descriptor Register (Low Part)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04460h	

DWord	Bit	Description	
0	31:0	**MFX0 PDP3 Descriptor Register (Low Part)**	
		Default Value:	00000000h
		Access:	R/W

MFX1 Context Element Descriptor (High Part)

MFX1_CTX_EDR_H - MFX1 Context Element Descriptor (High Part)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04484h	

DWord	Bit	Description
0	31:0	**MFX1 Context Element Descriptor (High Part)**
		Default Value: 00000000h
		Access: R/W

MFX1 Context Element Descriptor (Low Part)

MFX1_CTX_EDR_L - MFX1 Context Element Descriptor (Low Part)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000009	
Size (in bits):	32	
Address:	04480h	

DWord	Bit	Description	
0	31:0	**MFX1 Context Element Descriptor (Low Part)**	
		Default Value:	00000009h
		Access:	R/W

MFX1 Context Element Descriptor (Low Part)

MFX1_CTX_EDR_L - MFX1 Context Element Descriptor (Low Part)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000009	
Size (in bits):	32	
Address:	04480h	

DWord	Bit	Description	
0	31:0	**MFX1 Context Element Descriptor**	
		Default Value:	00000009h
		Access:	R/W

MFX1 Fixed Counter

MFX1_FIXED_CNTR - MFX1 Fixed Counter		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	045B4h	

DWord	Bit	Description
0	31:0	**MFX1 Fixed Counter**
		Default Value: 00000000h
		Access: RO
		This counter only applies to advance context when fault and stream mode is selected.

MFX1 PDP0/PML4/PASID Descriptor (High Part)

MFX1_CTX_PDP0_H - MFX1 PDP0/PML4/PASID Descriptor (High Part)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0448Ch	

DWord	Bit	Description
0	31:0	**MFX1 PDP0/PML4/PASID Descriptor (High Part)**
		Default Value: · 00000000h
		Access: · R/W

MFX1 PDP0/PML4/PASID Descriptor (Low Part)

MFX1_CTX_PDP0_L - MFX1 PDP0/PML4/PASID Descriptor (Low Part)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04488h	
DWord	**Bit**	**Description**
0	31:0	**MFX1 PDP0/PML4/PASID Descriptor (Low Part)**
		Default Value: 00000000h
		Access: R/W

MFX1 PDP1 Descriptor Register (High Part)

MFX1_CTX_PDP1_H - MFX1 PDP1 Descriptor Register (High Part)	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	04494h

DWord	Bit	Description	
0	31:0	**MFX1 PDP1 Descriptor Register (High Part)**	
		Default Value:	00000000h
		Access:	R/W

MFX1 PDP1 Descriptor Register (Low Part)

MFX1_CTX_PDP1_L - MFX1 PDP1 Descriptor Register (Low Part)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04490h	

DWord	Bit	Description	
0	31:0	**MFX1 PDP1 Descriptor Register (Low Part)**	
		Default Value:	00000000h
		Access:	R/W

MFX1 PDP2 Descriptor Register (High Part)

MFX1_CTX_PDP2_H - MFX1 PDP2 Descriptor Register (High Part)	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0449Ch

DWord	Bit	Description	
0	31:0	**MFX1 PDP2 Descriptor Register (High Part)**	
		Default Value:	00000000h
		Access:	R/W

MFX1 PDP2 Descriptor Register (Low Part)

<table>
<tr><td colspan="3" align="center">**MFX1_CTX_PDP2_L - MFX1 PDP2 Descriptor Register (Low Part)**</td></tr>
<tr><td colspan="3">Register Space: MMIO: 0/2/0</td></tr>
<tr><td colspan="3">Project: CHV, BSW</td></tr>
<tr><td colspan="3">Source: PRM</td></tr>
<tr><td colspan="3">Default Value: 0x00000000</td></tr>
<tr><td colspan="3">Size (in bits):   32</td></tr>
<tr><td colspan="3">Address: 04498h</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td>**Description**</td></tr>
<tr><td>0</td><td>31:0</td><td>**MFX1 PDP2 Descriptor Register (Low Part)**

Default Value:	00000000h
Access:	R/W
</td></tr>
</table>

MFX1 PDP3 Descriptor Register (High Part)

MFX1_CTX_PDP3_H - MFX1 PDP3 Descriptor Register (High Part)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	044A4h	

DWord	Bit	Description	
0	31:0	**MFX1 PDP3 Descriptor Register (High Part)**	
		Default Value:	00000000h
		Access:	R/W

MFX1 PDP3 Descriptor Register (Low Part)

MFX1_CTX_PDP3_L - MFX1 PDP3 Descriptor Register (Low Part)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	044A0h	

DWord	Bit	Description	
0	31:0	**MFX1 PDP3 Descriptor Register (Low Part)**	
		Default Value:	00000000h
		Access:	R/W

MFX Frame BitStream SE/BIN Count

MFX_SE-BIN_CT - MFX Frame BitStream SE/BIN Count	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	1286Ch
Valid Projects:	CHV, BSW

This register stores the number of BINs (AVC CABAC) and SEs (CAVLD, VLD) decoded in a frame. This register is not part of hardware context save and restore.

DWord	Bit	Description
0	31:0	**MFX Frame Bit-stream SE/BIN Count** Total number of BINs/SEs decoded in current frame. This number is used with frame performance count to derive Bin/clk or SE/clk.

MFX Frame Macroblock Count

MFX_MB_COUNT - MFX Frame Macroblock Count	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	12868h
Valid Projects:	CHV, BSW

This register stores the number of Macro-blocks decoded/encoded in current frame. This register is not part of hardware context save and restore.

DWord	Bit	Description
0	31:20	**MBZ**
		<table><tr><td>Exists If:</td><td>// JPEG == True</td></tr><tr><td>Format:</td><td>MBZ</td></tr></table> This field is currently reserved
	31:16	**Intra MB Count**
		<table><tr><td>Exists If:</td><td>// AVC CAVLC, AVC CABAC, VC1 and MPEG2 == True</td></tr><tr><td>Format:</td><td>U16</td></tr></table>
	19:0	**JPEG Block Count**
		<table><tr><td>Exists If:</td><td>// JPEG == True</td></tr><tr><td>Format:</td><td>U20</td></tr></table> This 20-bit field indicates the number of 8x8 blocks within the JPEG frame. This field is clear at the start of decoding a new frame.
	15:0	**Number of MB Concealment**
		<table><tr><td>Exists If:</td><td>// AVC CAVLC, AVC CABAC, VC1 and MPEG2 == True</td></tr></table> This 16-bit field indicates the number of MB is concealed by hardware. This field is clear at the start of decoding a new frame.

MFX Frame Motion Comp Miss Count

MFX_MISS_CT - MFX Frame Motion Comp Miss Count	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	12888h
Valid Projects:	CHV, BSW

This register stores the total number of cacheline hits occurred in the motion compensation cache per frame. This register is not part of hardware context save and restore.

DWord	Bit	Description
0	31:16	**Reserved**
		Format: MBZ
	15:0	**MFX Frame Motion Comp cache miss Count** Total number of CL misses occurred in the 12KB cache of the motion compensation engine per frame. This number is used along with **MFX Frame Motion Comp Read Count** to derive motion comp cache miss/hit ratio.

MFX Frame Motion Comp Read Count

MFX_READ_CT - MFX Frame Motion Comp Read Count	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	12484h

 This register stores the total number of reference picture read requests made by the Motion Compensation engine per frame. This register is not part of hardware context save and restore.

DWord	Bit	Description
0	31:20	**Reserved**
		Format: MBZ
	19:0	**MFX Frame Motion Comp CL read request Count** Total number of reference picture read requests by the motion compensation engine per frame.

MFX Frame Row-Stored/BitStream Read Count

MFX_ROW-PER-BS_COUNT - MFX Frame Row-Stored/BitStream Read Count	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	12880h
Valid Projects:	CHV, BSW

This register stores the total number of row-stored/bit-stream read requests made by the pre-fetch engine per frame. This register is not part of hardware context save and restore.

DWord	Bit	Description
0	31:16	**Reserved**
		Format: MBZ
	15:0	**MFX row-stored/bit-stream read request Count** Total number of row-stored/bit-stream read requests sent by the memory pre-fetch engine per frame.

MFX LRA 0

<table>
<tr><th colspan="3">MFX_LRA_0 - MFX LRA 0</th></tr>
<tr><td>Register Space:</td><td colspan="2">MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td colspan="2">CHV, BSW</td></tr>
<tr><td>Source:</td><td colspan="2">PRM</td></tr>
<tr><td>Default Value:</td><td colspan="2">0x7F403F00</td></tr>
<tr><td>Size (in bits):</td><td colspan="2">32</td></tr>
<tr><td>Address:</td><td colspan="2">04A50h</td></tr>
<tr><th>DWord</th><th>Bit</th><th>Description</th></tr>
<tr><td rowspan="12">0</td><td rowspan="3">31:24</td><td>**MFX LRA1 Max**</td></tr>
<tr><td>Default Value: 01111111b</td></tr>
<tr><td>Access: R/W</td></tr>
<tr><td colspan="1"></td><td>Maximum value of programmable LRA1.</td></tr>
</table>

DWord	Bit	Description	
0	31:24	**MFX LRA1 Max**	
		Default Value:	01111111b
		Access:	R/W
		Maximum value of programmable LRA1.	
	23:16	**MFX LRA1 Min**	
		Default Value:	01000000b
		Access:	R/W
		Minimum value of programmable LRA1.	
	15:8	**MFX LRA0 Max**	
		Default Value:	00111111b
		Access:	R/W
		Maximum value of programmable LRA0.	
	7:0	**MFX LRA0 Min**	
		Default Value:	00000000b
		Access:	R/W
		Minimum value of programmable LRA0.	

MFX LRA 1

MFX_LRA_1 - MFX LRA 1	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0xFFC0BF80
Size (in bits):	32
Address:	04A54h

DWord	Bit	Description	
0	31:24	**MFX LRA3 Max**	
		Default Value:	11111111b
		Access:	R/W
		Maximum value of programmable LRA3.	
	23:16	**MFX LRA3 Min**	
		Default Value:	11000000b
		Access:	R/W
		Minimum value of programmable LRA3.	
	15:8	**MFX LRA2 Max**	
		Default Value:	10111111b
		Access:	R/W
		Maximum value of programmable LRA2.	
	7:0	**MFX LRA2 Min**	
		Default Value:	10000000b
		Access:	R/W
		Minimum value of programmable LRA2.	

MFX LRA 2

MFX_LRA_2 - MFX LRA 2

Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x0000001B
Size (in bits):	32

Address:	04A58h

DWord	Bit	Description
0	31:8	**Reserved**
		Default Value: 000000h
		Access: RO
	7:6	**VCS LRA**
		Default Value: 00b
		Access: R/W
		Which LRA should VCS use.
	5:4	**VMX LRA**
		Default Value: 01b
		Access: R/W
		Which LRA should VMX use.
	3:2	**VMC LRA**
		Default Value: 10b
		Access: R/W
		Which LRA should VMC use.
	1:0	**VCR LRA**
		Default Value: 11b
		Access: R/W
		Which LRA should VCRSL1 use.

MFX LRA SL1 0

MFX_LRA_SL1_0 - MFX LRA SL1 0		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x7F403F00	
Size (in bits):	32	
Address:	04A60h	

DWord	Bit	Description	
0	31:24	**MFX SL1 LRA1 Max**	
		Default Value:	01111111b
		Access:	R/W
		Maximum value of programmable LRA1.	
	23:16	**MFX SL1 LRA1 Min**	
		Default Value:	01000000b
		Access:	R/W
		Minimum value of programmable LRA1.	
	15:8	**MFX SL1 LRA0 Max**	
		Default Value:	00111111b
		Access:	R/W
		Maximum value of programmable LRA0.	
	7:0	**MFX SL1 LRA0 Min**	
		Default Value:	00000000b
		Access:	R/W
		Minimum value of programmable LRA0.	

MFX LRA SL1 1

<table>
<tr><td colspan="3" align="center">MFX_LRA_SL1_1 - MFX LRA SL1 1</td></tr>
<tr><td>Register Space:</td><td colspan="2">MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td colspan="2">CHV, BSW</td></tr>
<tr><td>Source:</td><td colspan="2">PRM</td></tr>
<tr><td>Default Value:</td><td colspan="2">0xFFC0BF80</td></tr>
<tr><td>Size (in bits):</td><td colspan="2">32</td></tr>
<tr><td>Address:</td><td colspan="2">04A64h</td></tr>
<tr><td>DWord</td><td>Bit</td><td>Description</td></tr>
<tr><td rowspan="4">0</td><td>31:24</td><td>MFX SL1 LRA3 Max

Default Value:	11111111b
Access:	R/W

Maximum value of programmable LRA3.</td></tr>
<tr><td>23:16</td><td>MFX SL1 LRA3 Min

Default Value:	11000000b
Access:	R/W

Minimum value of programmable LRA3.</td></tr>
<tr><td>15:8</td><td>MFX SL1 LRA2 Max

Default Value:	10111111b
Access:	R/W

Maximum value of programmable LRA2.</td></tr>
<tr><td>7:0</td><td>MFX SL1 LRA2 Min

Default Value:	10000000b
Access:	R/W

Minimum value of programmable LRA2.</td></tr>
</table>

MFX LRA SL1 2

MFX_LRA_SL1_2 - MFX LRA SL1 2		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x0000001B	
Size (in bits):	32	
Address:	04A68h	

DWord	Bit	Description	
0	31:8	**Reserved**	
		Default Value:	000000h
		Access:	RO
	7:6	**VCSSL1 LRA**	
		Default Value:	00b
		Access:	R/W
		Which LRA should VCSSL1 use.	
	5:4	**VMXSL1 LRA**	
		Default Value:	01b
		Access:	R/W
		Which LRA should VMXSL1 use.	
	3:2	**VMCSL1 LRA**	
		Default Value:	10b
		Access:	R/W
		Which LRA should VMCSL1 use.	
	1:0	**VCRSL1 LRA**	
		Default Value:	11b
		Access:	R/W
		Which LRA should VCRSL1 use.	

MFX Memory Latency Count2

MFX_LAT_CT2 - MFX Memory Latency Count2	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	12874h
Valid Projects:	CHV, BSW

This register stores the accumulative memory latency count on reference picture read requests. This register is not part of hardware context save and restore.

DWord	Bit	Description
0	31:26	**Reserved**
		Format: MBZ
	25:0	**MFX Reference picture read request - Accumulative Memory Latency Count for the entire frame in 8xMedia clock cycles** The accumulative memory latency count of all reference reads requested by motion compensative engine per frame. This number is used with **MFX Frame Motion Comp Read Count** to derive average memory latency.

MFX Memory Latency Count3

MFX_LAT_CT3 - MFX Memory Latency Count3	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	12878h
Valid Projects:	CHV, BSW

This register stores the max and min memory latency counts reported on row-stored/bit-stream read requests. Max and current requests into memory sub-system engine. This register is not part of hardware context save and restore.

DWord	Bit	Description
0	31:24	**Max Request Count** This field indicates the maximum number of requests allowed by the memory sub-system channel.
	23:16	**Current Request Count** This field indicates the number of requests currently outstanding in the memory sub-system. This field should report with a value of zero at the end of frame; otherwise the pre-fetch engine most likely hung waiting for read data to be returned from sub-system.
	15:8	**MFX row-stored/bit-stream read request - Max Latency Count in 8xMedia clock cycles** This field reports the maximum memory latency count on all row-stored/bit-stream reads requested by the memory pre-fetch engine.
	7:0	**MFX row-stored/bit-stream read request - Min Latency Count in 8xMedia clock cycles** This field reports the minimum memory latency count on all row-stored/bit-stream reads requested by the memory pre-fetch engine.

MFX Memory Latency Count4

MFX_LAT_CT4 - MFX Memory Latency Count4		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	VideoCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	1287Ch	
Valid Projects:	CHV, BSW	

This register stores the accumulative memory latency count on row-stored/bit-stream read requests. This register is not part of hardware context save and restore.

DWord	Bit	Description
0	31:26	**Reserved**
		Format: MBZ
	25:0	**MFX row-stored/bit-stream read request - Accumulative Memory Latency Count for the entire frame in 8xMedia clock cycles** The accumulative memory latency count of all row-stored/bit-stream reads requested by pre-fetch engine per frame. This number is used with **Frame row-stored/bit-stream memory read count** to derive average memory latency.

MFX Pipeline Status Flags

MFX_STATUS_FLAGS - MFX Pipeline Status Flags	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	12838h
Valid Projects:	CHV, BSW

This register stores the various pipeline status flags. This register is not part of hardware context save and restore.

DWord	Bit	Description
0	31:17	**Reserved**
	16	**MFX Active** Frame decoding/encoding is in progress. Set on frame_start; clear on frame_end.
	15:10	**Reserved**
	9	**Streamout Enable**
	8	**Reserved**
	7	**Post Deblocking Mode Enable**
	6	**Pre Deblocking Mode Enable**
	5	**Decoder Mode Select** <table><tr><th>Value</th><th>Name</th></tr><tr><td>0</td><td>Configure the MFD Engine for VLD Mode</td></tr><tr><td>1</td><td>Configure the MFD Engine for IT Mode</td></tr></table>
	4	**Codec Select** <table><tr><th>Value</th><th>Name</th></tr><tr><td>0</td><td>Decode</td></tr><tr><td>1</td><td>Encode</td></tr></table>
	3:2	**Video Mode** <table><tr><th>Value</th><th>Name</th></tr><tr><td>00b</td><td>MPEG2</td></tr><tr><td>01b</td><td>VC1</td></tr><tr><td>10b</td><td>AVC</td></tr><tr><td>11b</td><td>JPEG</td></tr></table>

		MFX_STATUS_FLAGS - MFX Pipeline Status Flags		
	1	**Decoder Short Format Mode**		
		Value	Name	Description
		0		AVC/VC1 Short Format Mode is in use
		1		AVC/VC1 Long Format Mode is in use
	0	**Stitch Mode**		
		Value	Name	Description
		0b		Not in Stitch Mode
		1b		In the Special Stitch Mode

MFX Slice Performance Count

MFX_SLICE_PERFORM_CT - MFX Slice Performance Count	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	12864h
Valid Projects:	CHV, BSW

This register stores the number of clock cycles spent decoding/encoding the current slice. This register is not part of hardware context save and restore.

DWord	Bit	Description
0	31:0	**MFX Frame Performance Count** Total number of clocks between slice start and slice end. This count is incremented on crm_clk

MGGC - MGGC

7:3	**GMS**	
	Default Value:	00101b
	Access:	RO

Graphics Mode Select(GMS): This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics device in VGA (non-linear) and Native (linear) modes. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled. Hardware does not clear or set any of these bits automatically based on IGD being disabled/enabled. BIOS Requirement: BIOS must not set this field to 0h if IVD (bit 1 of this register) is 0.
0h = 0MB 1h = 32MB 2h = 64MB 3h = 96MB 4h = 128MB 5h = 160MB 6h = 192MB 7h = 224MB 8h = 256MB 9h = 288MB Ah = 320MB Bh = 352MB Ch = 384MB Dh = 416MB Eh = 448MB Fh = 480MB 10h = 512MB 11h = 8MB 12h = 12MB 13h = 16MB 14h = 20MB 15h = 24MB 16h = 28MB 17h = 36MB 18h = 40MB 19h = 44MB 1Ah = 48MB 1Bh = 52MB 1Ch = 56MB 1Dh = 60MB 1Eh = Reserved 1Fh = Reserved ..... 20h:1024MB (Not supported for CHV, BSW)

MGGC - MGGC

		..... 30h:1536MB (Not supported for CHV, BSW) ...... 40h:2048MB (Not supported for CHV, BSW) ...... 80h:4096MB (Not supported for CHV, BSW) 81h - FF:Reserved Other = Reserved When GMS != '0 (and VD=0): Address[31:0] is compared with VGA memory range. (The VGA memory range is A_0000h to B_FFFFh.). If there is a match and MSE = 1 and MEMRD or MEMWR, the access will route as a Rmdwvgamemen_cr cycle on the RMbus. If the RMbus returns a hit the GVD will select the command. As well, when 0 the GVD will check if scldown3_address[15:0] is one of the VGA IO register range. (The VGA IO range is 03B0h - 03BBh and 03C0h - 03DFh.) If there is a match and IOSE = 1 and the SCL command is either an IORD or IOWR, the GVD will intiate a (VGA) register cycle on the RMbus. If the RMbus returns a hit the GVD will select the command When GMS == '0 : No address compare will occur against VGA memory range or the VGA IO register range. Also, CC[15:8] is changed to 8'h80 from 8'h00		

	2	**RESERVED**		
		Default Value:		0b
		Access:		RO
		Reserved		

	1	**VGA_DISABLE**		
		Default Value:		0b
		Access:		RO
		VGA Disable (VD): 0: Enable. Device 2 (IGD) claims VGA memory and IO cycles, the Sub-Class Code within Device 2 Class Code register is 00. 1: Disable. Device 2 (IGD) does not claim VGA cycles (Mem and IO), and the Sub- Class Code field within Device 2 function 0 Class Code register is 80. BIOS Requirement: BIOS must not set this bit to 0 if the GMS field pre-allocates no memory. This bit MUST be set to 1 if Device 2 is disabled either via a fuse or fuse override (CAPID0[38] = 1) or via a register (DEVEN[3] = 0).		

	0	**GGCLCK**		
		Default Value:		0b
		Access:		RO
		When set to 1b, this will lock all the bits in this register, including itself		

MGSR2GAM Message Register

MGSR2GAM_MSGREG - MGSR2GAM Message Register		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	040D8h	

DWord	Bit	Description
0	31:16	**Mask Bits**
		Default Value: / 0000h
		Access: / RO
		Mask Bits act as Write Enables for the bits[15:0] of this register.
	15	**MGSR2GAM Message Register 15**
		Default Value: / 0b
		Access: / R/W
		For Future Use. This bit is self clear.
	14	**MGSR2GAM Message Register 14**
		Default Value: / 0b
		Access: / R/W
		For Future Use. This bit is self clear.
	13	**MGSR2GAM Message Register 13**
		Default Value: / 0b
		Access: / R/W
		For Future Use. This bit is self clear.
	12	**MGSR2GAM Message Register 12**
		Default Value: / 0b
		Access: / R/W
		For Future Use. This bit is self clear.
	11	**MGSR2GAM Message Register 11**
		Default Value: / 0b
		Access: / R/W
		For Future Use.

MGSR2GAM_MSGREG - MGSR2GAM Message Register

		This bit is self clear.	
	10	**MGSR2GAM Message Register 10**	
		Default Value:	0b
		Access:	R/W
		For Future Use. This bit is self clear.	
	9	**MGSR2GAM Message Register 9**	
		Default Value:	0b
		Access:	R/W
		For Future Use. This bit is self clear.	
	8	**MGSR2GAM Message Register 8**	
		Default Value:	0b
		Access:	R/W
		For Future Use. This bit is self clear.	
	7	**MGSR2GAM Message Register 7**	
		Default Value:	0b
		Access:	R/W
		For Future Use. This bit is self clear.	
	6	**MGSR2GAM Message Register 6**	
		Default Value:	0b
		Access:	R/W
		For Future Use. This bit is self clear.	
	5	**MGSR2GAM Message Register 5**	
		Default Value:	0b
		Access:	R/W
		For Future Use. This bit is self clear.	
	4	**MGSR2GAM Message Register 4**	
		Default Value:	0b
		Access:	R/W
		For Future Use. This bit is self clear.	
	3	**MGSR2GAM Message Register 3**	
		Default Value:	0b
		Access:	R/W
		For Future Use. This bit is self clear.	

MGSR2GAM_MSGREG - MGSR2GAM Message Register

	2	**MGSR2GAM Message Register 2**	
		Default Value:	0b
		Access:	R/W
		For Future Use. This bit is self clear.	
	1	**MGSR2GAM Message Register 1**	
		Default Value:	0b
		Access:	R/W
		For Future Use. This bit is self clear.	
	0	**MGSR2GAM Message Register 0**	
		Default Value:	0b
		Access:	R/W
		Bit0 - Tail Update Ack Message. This bit is self clear.	

Misc. Clocking / Reset Control Registers

MISCCPCTL - Misc. Clocking / Reset Control Registers		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000002	
Size (in bits):	32	
Address:	09424h	
Miscellaneous Clocking / Reset Control Registers.		

DWord	Bit	Description
0	31:8	**Bonus ECO bits**
		Access: R/W
		Bonus ECO bits
	7	**DOP clock gating enable for VEbox clks**
		Access: R/W
		Controls the Enabling of the DOP-level Vebox (cvclk) Clock Gating via PM event messages 1 - Clock gating is enabled 0 - Clock gating is disabled
	6	**DOP clock gating enable for Media clocks**
		Access: R/W
		Controls the Enabling of the DOP-level Media (cmclk) Clock Gating via PM event messages 1 - Clock gating is enabled 0 - Clock gating is disabled
	5	**Reserved**
		Access: RO
		Made Reserved field as we dont have Media 1 in CHV, BSW Controls the Enabling of the DOP-level Render (cmclk for 2nd media block) Clock Gating via PM event messages 1 - Clock gating is enabled 0 - Clock gating is disabled
	4	**Reserved**
	3	**DOP CLock gating Enable for Widi clocks**
		Access: R/W
		Controls the Enabling of the DOP-level Render (cwclk) Clock Gating via PM event messages 1 - Clock gating is enabled 0 - Clock gating is disabled

MISCCPCTL - Misc. Clocking / Reset Control Registers

<table>
<tr><td>2</td><td colspan="2">**DOP clock gating Enable for Fix clocks (cfclk)**</td></tr>
<tr><td></td><td>Access:</td><td>R/W</td></tr>
<tr><td></td><td colspan="2">Controls the Enabling of the DOP-level Render (cfclk/cf2xclk) Clock Gating via PM event messages
1 - Clock gating is enabled
0 - Clock gating is disabled</td></tr>
<tr><td>1</td><td colspan="2">**L1 Clock Ungate Enabling Control During Reset**</td></tr>
<tr><td></td><td>Default Value:</td><td>1b</td></tr>
<tr><td></td><td>Access:</td><td>R/W</td></tr>
<tr><td></td><td colspan="2">Control to enable/disable L1 clock gating during soft resets and FLR reset processing
1 - disable L1 clock gating during soft resets and FLR
0 - enable L1 clock gating during soft resets and FLR (default op)</td></tr>
<tr><td>0</td><td colspan="2">**DOP Clock Gating Enable for Render Clocks**</td></tr>
<tr><td></td><td>Access:</td><td>R/W</td></tr>
<tr><td></td><td colspan="2">Controls the Enabling of the DOP-level Render (crclk/cr2xclk) Clock Gating via PM event messages
1 - Clock gating is enabled
0 - Clock gating is disabled</td></tr>
</table>

MISC. CTX control register

MISCCTXCTL - MISC. CTX control register		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0942Ch	

DWord	Bit	Description
0	31:1	**Reserved**
		Access: RO
		Reserved.
	0	**Context Restore ACk indication from Csunit**
		Access: R/W Set
		Context Restore ACk indication from Csunit 1'b1 : Csunit has completed restoring CPunits address space Once set, CPunit hardware clears this bit after sending the ctx save ack done message to CS 1'b0 : Csunit has NOT completed restoring CPunits address space

Misc. Reset Control Register

RSTCTL - Misc. Reset Control Register		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	09420h	
Miscellaneous reset control registers.		

DWord	Bit	Description
0	31:4	**Reserved**
		Access: RO
		Reserved
	3:2	**Reset Staggering Period Control**
		Access: R/W
		Reset assertion staggering period between reset domains during FLR and soft-resets: 00: 24 cs clocks 01: 48 cs clocks 10: 72 cs clocks 11: 96 cs clocks
	1:0	**Reset Residency Control**
		Access: R/W
		Reset assertion residency period for FLR and soft-resets. 00: 24 cs clocks 01: 48 cs clocks 10: 96 cs clocks 11: 192 cs clocks

MISR0

<table>
<tr><td colspan="3" align="center">**MISR0 - MISR0**</td></tr>
<tr><td>Register Space:</td><td colspan="2">MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td colspan="2">CHV, BSW</td></tr>
<tr><td>Source:</td><td colspan="2">PRM</td></tr>
<tr><td>Default Value:</td><td colspan="2">0x00000000</td></tr>
<tr><td>Size (in bits):</td><td colspan="2">32</td></tr>
<tr><td>Address:</td><td colspan="2">182040h</td></tr>
<tr><td colspan="3">Spare0 registers. Note: Changed for CHV, BSW.</td></tr>
</table>

DWord	Bit	Description	
0	31:17	**Spare0**	
		Default Value:	0000h
		Access:	R/W
		Spare bits in case an ECO is needed.	
	16	**Standby Threshold Periodic Enable**	
		Default Value:	0000h
		Access:	R/W
		Standby Threshold Periodic Enable	
	15:0	**Standby Threshold**	
		Default Value:	0000h
		Access:	R/W

Description	Project
Standby Threshold For 33MHz cz freq (200MHz, 267MHz, 320MHz, 333MHz, 400MHz, 467MHz, 533MHz) 0 = 0 us 1 = 15.36 us 2 = 30.72 us 3 = 46.08 us FFFF ~= 1s For non-33MHz cz freq (350MHz, 356MHz, 360MHz, 373MHz), standby threshold will be in increments of (15.36us + (1-7)%)	CHV, BSW

MISR1

MISR1 - MISR1		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	182044h	
Spare1 registers. Note: Changed for CHV, BSW.		
DWord	**Bit**	**Description**
0	31:0	**Spare1**
		Default Value: 00000000h
		Access: R/W
		Spare bits in case an ECO is needed.

MISR2

MISR2 - MISR2		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	182048h	
Spare2 registers. Note: Changed for CHV, BSW.		
DWord	**Bit**	**Description**
0	31:0	**Spare2**
		Default Value: 00000000h
		Access: R/W
		Spare bits in case an ECO is needed.

MISR3

<table>
<tr><td colspan="3" align="center">**MISR3 - MISR3**</td></tr>
<tr><td>Register Space:</td><td colspan="2">MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td colspan="2">CHV, BSW</td></tr>
<tr><td>Source:</td><td colspan="2">PRM</td></tr>
<tr><td>Default Value:</td><td colspan="2">0x00000000</td></tr>
<tr><td>Size (in bits):</td><td colspan="2">32</td></tr>
<tr><td>Address:</td><td colspan="2">18204Ch</td></tr>
<tr><td colspan="3">Spare3 registers. Note: Changed for CHV, BSW.</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td>**Description**</td></tr>
<tr><td>0</td><td>31:0</td><td>**Spare3**

<table><tr><td>Default Value:</td><td>00000000h</td></tr><tr><td>Access:</td><td>R/W</td></tr></table>Spare bits in case an ECO is needed.</td></tr>
</table>

MISR4

MISR4 - MISR4			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	182050h		
Spare4 registers. Note: Changed for CHV, BSW.			
DWord	**Bit**	**Description**	
0	31:0	**Spare4**	
		Default Value:	00000000h
		Access:	R/W
		Spare bits in case an ECO is needed.	

MMIO_INDEX

MMIO_INDEX - MMIO_INDEX	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	00000h

Contains address and target.
Punit cannot access IO space from message channel.
A 32 bit IO write to this port loads the offset of the MMIO register or offsetinto the GTT that needs to be accessed.
An IO Read returns the current value of this register. An 8/16 bit IO write to this register is completed but does not update this register.
This mechanism to access internal graphics MMIO registers must not be used to access VGA IO registers which are mapped through the MMIO space. VGA registers must be accessed directly through the dedicated VGA IO ports. This is used by SBIOS. It is not used by graphics driver.
This register is only accessible through the IOSF Primary bus. The base register is defined by IOBAR.

DWord	Bit	Description
0	31:2	**Register_offset**
		Default Value: 00000000h
		Access: R/W
		This field selects GTT entry or any one of the Dword registers within the MMIO register space of this device.
	1:0	**Target**
		Default Value: 00b
		Access: R/W
		00 = MMIO Registers, 01 = GTT, 1X =Reserved

Mode Register for GAB

GAB_MODE - Mode Register for GAB		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	BlitterCS	
Default Value:	0x00000000	
Access:	r/w	
Size (in bits):	32	
Address:	220A0h-220A3h	

The GAB_MODE register contains information that controls configurations in the GAB.

DWord	Bit	Description	
0	31:16	**Mask**	
		Access:	WO
		Format:	Mask
	15:6	**Reserved** Read/Write	
	5:3	**BLB Arbitration Priority**	
		Format:	U3
	2:0	**BCS Arbitration Priority**	
		Format:	U3

Mode Register for GAC

GAC_MODE - Mode Register for GAC	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoCS
Default Value:	0x00000000 CHV, BSW
Access:	r/w
Size (in bits):	32
Address:	120A0h-120A3h
ShortName:	GAC_MODE
Valid Projects:	CHV, BSW

The GAC_MODE register contains information that controls configurations in the GAC.

DWord	Bit	Description		
0	31:16	**Mask**		
		Access:		WO
		Format:		Mask
	15:1	**Reserved**		
		Access:		r/w
	0	**Reserved**		
		Project:		CHV, BSW
		Access:		r/w

Mode Register for GAFS

GAFS_MODE - Mode Register for GAFS	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00000000
Access:	r/w
Size (in bits):	32
Trusted Type:	1
Address:	0212Ch

DWord	Bit	Description
0	31:16	**Mask Bits**
		Access: WO
		Format: Mask
		Masks: These bits serve as write enables for bits 15:0. If this register is written with any of these bits clear the corresponding bit in the field 15:0 will not be modified. Reading these bits always returns 0s.
	15:11	**Reserved**
		Format: MBZ
	10	**Reserved**
		Project: CHV, BSW
		Format: MBZ
	9	**Reserved**
	8:2	**Reserved**
		Format: MBZ
	1:0	**Reserved**
		Project: CHV, BSW
		Format: MBZ

MSAC

<table>
<tr><td colspan="3" align="center">**MSAC - MSAC**</td></tr>
<tr><td>Register Space:</td><td colspan="2">PCI: 0/2/0</td></tr>
<tr><td>Project:</td><td colspan="2">CHV, BSW</td></tr>
<tr><td>Source:</td><td colspan="2">PRM</td></tr>
<tr><td>Default Value:</td><td colspan="2">0x00010000</td></tr>
<tr><td>Size (in bits):</td><td colspan="2">32</td></tr>
<tr><td>Address:</td><td colspan="2">00060h</td></tr>
<tr><td colspan="3">This register determines the size of the graphics memory aperture. Only the system BIOS will write this register based on pre-boot address allocation efforts. Graphics may read this register to determine the correct aperture size. System BIOS needs to save this value on boot so that it can reset it correctly during S3 resume. The size of the aperture must not be modified by software after its location is written into GMADR (offset 18h).</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td>**Description**</td></tr>
<tr><td>0</td><td>31:21</td><td>**RESERVED**
<table><tr><td>Default Value:</td><td>000h</td></tr><tr><td>Access:</td><td>RO</td></tr></table>Reserved</td></tr>
<tr><td></td><td>20</td><td>**APSZ_4**
<table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table>This field is used to determine the size of Aperture (GMADR) and controls affects certain bits of GMADR register.
00000 = 128MB =>GMADR.B [26:4] is hardwired to 0
00001 = 256MB =>GMADR.B[27] = 0, RO
00010 = illegal (hardware will treat this as 00011)
00011 = 512MB =>GMADR.B[28:27] = 0, RO
00100-00110 = illegal (hardware will treat this as 00111)
00111 = 1024MB =>GMADR.B[29:27] = 0, RO
01000-01110= illegal (hardware will treat this as 01111)
01111= 2048MB=> GMADR.B[30:27] = 0, RO
10000-11110 = illegal (hardware will treat this as 11111)
11111= 4096MB => GMADR.B[31:27] = 0, RO</td></tr>
<tr><td></td><td>19</td><td>**APSZ_3**
<table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table>This field is used to determine the size of Aperture (GMADR) and controls affects certain bits of GMADR register.
00000 = 128MB =>GMADR.B [26:4] is hardwired to 0
00001 = 256MB =>GMADR.B[27] = 0, RO
00010 = illegal (hardware will treat this as 00011)</td></tr>
</table>

MSAC - MSAC

		00011 = 512MB =>GMADR.B[28:27] = 0, RO 00100-00110 = illegal (hardware will treat this as 00111) 00111 = 1024MB =>GMADR.B[29:27] = 0, RO 01000-01110= illegal (hardware will treat this as 01111) 01111= 2048MB=> GMADR.B[30:27] = 0, RO 10000-11110 = illegal (hardware will treat this as 11111) 11111= 4096MB => GMADR.B[31:27] = 0, RO

	18	**APSZ_2**	
		Default Value:	0b
		Access:	R/W
		This field is used to determine the size of Aperture (GMADR) and controls affects certain bits of GMADR register. 00000 = 128MB =>GMADR.B [26:4] is hardwired to 0 00001 = 256MB =>GMADR.B[27] = 0, RO 00010 = illegal (hardware will treat this as 00011) 00011 = 512MB =>GMADR.B[28:27] = 0, RO 00100-00110 = illegal (hardware will treat this as 00111) 00111 = 1024MB =>GMADR.B[29:27] = 0, RO 01000-01110= illegal (hardware will treat this as 01111) 01111= 2048MB=> GMADR.B[30:27] = 0, RO 10000-11110 = illegal (hardware will treat this as 11111) 11111= 4096MB => GMADR.B[31:27] = 0, RO	

	17	**APSZ_1**	
		Default Value:	0b
		Access:	R/W
		This field is used to determine the size of Aperture (GMADR) and controls affects certain bits of GMADR register. 00000 = 128MB =>GMADR.B [26:4] is hardwired to 0 00001 = 256MB =>GMADR.B[27] = 0, RO 00010 = illegal (hardware will treat this as 00011) 00011 = 512MB =>GMADR.B[28:27] = 0, RO 00100-00110 = illegal (hardware will treat this as 00111) 00111 = 1024MB =>GMADR.B[29:27] = 0, RO 01000-01110= illegal (hardware will treat this as 01111) 01111= 2048MB=> GMADR.B[30:27] = 0, RO 10000-11110 = illegal (hardware will treat this as 11111) 11111= 4096MB => GMADR.B[31:27] = 0, RO	

	16	**APSZ_0**	
		Default Value:	1b
		Access:	R/W

MSAC - MSAC

		This field is used to determine the size of Aperture (GMADR) and controls affects certain bits of GMADR register. 00000 = 128MB =>GMADR.B [26:4] is hardwired to 0 00001 = 256MB =>GMADR.B[27] = 0, RO 00010 = illegal (hardware will treat this as 00011) 00011 = 512MB =>GMADR.B[28:27] = 0, RO 00100-00110 = illegal (hardware will treat this as 00111) 00111 = 1024MB =>GMADR.B[29:27] = 0, RO 01000-01110= illegal (hardware will treat this as 01111) 01111= 2048MB=> GMADR.B[30:27] = 0, RO 10000-11110 = illegal (hardware will treat this as 11111) 11111= 4096MB => GMADR.B[31:27] = 0, RO
	15:0	**RESERVED**
		Default Value: 0000h
		Access: RO
		Reserved

MSI_CAPID_MC

MSI_CAPID_MC - MSI_CAPID_MC	
Register Space:	PCI: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x0000B005
Size (in bits):	32
Address:	00090h

90-91h: Message Signaled Interrupts Capability ID
92-93h: Message Signaled Control Register

DWord	Bit	Description
0	31:24	**RESERVED**
		Default Value: 00h
		Access: RO
		Reserved
	23	**MODE_64B_ADDRCAP**
		Default Value: 0b
		Access: RO
		C64: 32-bit capable only
	22:20	**MULTIPLE_MESSAGE_ENABLE**
		Default Value: 000b
		Access: R/W
		MME: This field is RW for software compatibility, but only a single message is ever generated. System software programs this field to indicate the actual number of messages allocated to this device. This number will be equal to or less than the number actually requested. The encoding is the same as for the MMC field below.
	19:17	**MULTIPLE_MESSAGE_CAPABLE**
		Default Value: 000b
		Access: RO
		MMC: This device is only single message capable. System Software reads this field to determine the number of messages being requested by this device. Value: Number of requests 000: 1 001-111: Reserved

**MSI_CAPID_MC - MSI_CAPID_MC**		

	16	**MSI_ENABLE**	
		Default Value:	0b
		Access:	R/W
			MSIE: If set, MSI is enabled and traditional interrupts are not used to generate interrupts. PCICMDSTS.BME must be set for an MSI to be generated. 0 : MSI interrupts are disabled. 1 : MSI interrupts are enabled. Permits sending an MSI interrupt.
	15:8	**POINTER_TO_NEXT_CAPABILITY**	
		Default Value:	B0h
		Access:	R/W Once
			Points to the next item in the list(B0=VCID support). This register should be programmed by BIOS during boot-up. Once written, this register becomes Read_Only. This register can only be cleared by a Reset.
	7:0	**CAPABILITY_ID**	
		Default Value:	05h
		Access:	RO
			CAPID: Indicates an MSI capability

MTRR Capability Register 0

MTRR_CR_0 - MTRR Capability Register 0	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x0000050A
Size (in bits):	32
Address:	0F100h

Register to define MTRR - range register capabilities.

DWord	Bit	Description		
0	31:11	**Reserved**		
		Default Value:	00000000000000000000b	
		Access:	RO	
	10	**Write Combining Support**		
		Default Value:		1b
		Access:		RO
		0: Write Combining (WC) memory type is not supported. 1: Write Combining (WC) memory type is supported. GFX Implementation: More details on memory type section however WC support in GFX looks like streamlining non-cacheable accesses. This is the existing UC concept used in GFX architecture.		
	9	**Reserved**		
		Default Value:		0b
		Access:		RO
	8	**Fixed Range MTRRs Support**		
		Default Value:		1b
		Access:		RO
		0: No Fixed range MTRRs are supported. 1: Fixed Range MTRRs (IA32_MTRR_FIX64K_00000 through IA32_MTRR_FIX4K_0F8000) are supported.		
	7:0	**Variable Range MTRR Count**		
		Default Value:		0Ah
		Access:		RO
		Indicates the number of variable ranges implemented.		

MTRR Capability Register 1

MTRR_CR_1 - MTRR Capability Register 1		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F104h	
Register to define MTRR - range register capabilities		

DWord	Bit	Description	
0	31:0	**MTRR Capability Register 1 Reserved**	
		Default Value:	00000000h
		Access:	RO
		Bit[63:32]: Reserved.	

MTRR Default Type Register 0

MTRR_DT_0 - MTRR Default Type Register 0	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0F108h

Register to define MTRR - range register capabilities.

DWord	Bit	Description	
0	31:12	**Reserved**	
		Default Value:	0000000000000000000b
		Access:	RO
	11	**Reserved**	
	10	**Fixed Range MTRR Enable/Disable**	
		Default Value:	0b
		Access:	R/W
		0: Disable fixed-range MTRRs. 1: Enable fixed-range MTRRs. When the fixed-range MTRRs are enabled, they take priority over the variable-range MTRRs when overlaps in ranges occur. If the fixed-range MTRRs are disabled, the variable range MTRRs can still be used and can map the range ordinarily covered by the fixed-range MTRRs. GFX Implementation: GFX uses this field as a specific enable/disable for fixed range MTRRs.	
	9:8	**Reserved**	
		Default Value:	00b
		Access:	RO
	7:0	**Default Memory Type**	
		Default Value:	00h
		Access:	R/W
		Indicates default memory type used for physical memory address ranges that do not have a memory type specified for them by an MTRR. Legal values for this field are 0, 1, 4, 5, and 6. GFX Implementation: GFX uses this field to assign memory regions that are not assigned as part of the fixed and variable range registers.	

MTRR Default Type Register 1

MTRR_DT_1 - MTRR Default Type Register 1		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F10Ch	
Register to define MTRR - range register capabilities.		
DWord	**Bit**	**Description**
0	31:0	**MTRR Default Type Register 1 Reserved**
		Default Value: 00000000h
		Access: RO
		Bit[63:32]: Reserved.

MT Virtual Page Address Registers

MTTLB_VA - MT Virtual Page Address Registers	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	04800h-04803h

DWord	Bit	Description		
0	31:12	**Address**		
		Format:	GraphicsAddress[31:12]	
		Page virtual address.		
	11:0	**Reserved**		
		Project:	CHV, BSW	
		Format:	MBZ	

Doc Ref # IHD-OS-CHV-BSW-Vol 2c-06.15

NOP Identification Register

<table>
<tr><td colspan="2" align="center">**NOPID - NOP Identification Register**</td></tr>
<tr><td>Register Space:</td><td>MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td>CHV, BSW</td></tr>
<tr><td>Source:</td><td>RenderCS</td></tr>
<tr><td>Default Value:</td><td>0x00000000</td></tr>
<tr><td>Size (in bits):</td><td>32</td></tr>
<tr><td>Trusted Type:</td><td>1</td></tr>
<tr><td>Address:</td><td>02094h</td></tr>
<tr><td>Address:
Name:
ShortName:</td><td>12094h-12097h
NOP Identification Register
NOPID_VCSUNIT0</td></tr>
<tr><td>Address:
Name:
ShortName:</td><td>1A094h-1A097h
NOP Identification Register
NOPID_VECSUNIT</td></tr>
<tr><td>Address:
Name:
ShortName:</td><td>1C094h-1C097h
NOP Identification Register
NOPID_VCSUNIT1</td></tr>
<tr><td>Address:
Name:
ShortName:</td><td>22094h-22097h
NOP Identification Register
NOPID_BCSUNIT</td></tr>
</table>

Description	Project
Access: RW	CHV, BSW
The NOPID register contains the Noop Identification value specified by the last MI_NOOP instruction that enabled this register to be updated.	

DWord	Bit	Description	
0	31:22	**Reserved**	
		Format:	MBZ
	21:0	**Reserved**	

P2GCONTROL

P2GCONTROL - P2GCONTROL		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	1300F0h	
Punit to Gunit Control. Punit will context save/restore this register.		

DWord	Bit	Description
0	31:1	**Reserved**
		Access: RO
	0	**P2GCONTROL_POLICY**
		Access: R/W
		0: Let Gunit do the context save. (Power-On default) 1: Context save will be handled by Punit and driver.

PAGE_FAULT_MODE

PAGE_FAULT_MODE - PAGE_FAULT_MODE	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0E454h
Name:	PAGE_FAULT_MODE
ShortName:	PAGE_FAULT_MODE
Valid Projects:	CHV, BSW

This is a basic register template

DWord	Bit	Description	
0	31:8	**Reserved**	
		Default Value:	000000000000000b
		Access:	RO
	7:6	**FAULT_MODE**	
		Project:	CHV, BSW
		Access:	R/W
		Fault Model: Applicable only in advanced context "00": Fault & Hang (chicken bit to survive). Same mode as gen7.5 "01": Fault & Halt "10": Fault & Continue & Switch "11": Reserved	

Value	Name
00b	**[Default]**
01b	

DWord	Bit	Description	
	5:0	**Reserved**	
		Project:	CHV, BSW

ff

PDP0 - Page Directory Pointer Descriptor - PDP0/PML4/PASID

Ring Buffer Based Scheduling: A write via MMIO to PDP0_DESCRIPROR (lower Dword) triggers the Page Directory Restore in HW when PPGTT is enabled. SW should ensure PDP1/2/3 registers are programmed appropriately prior to programming PDP0. PDP0_DESCRIPTOR lower dword should be programmed at the end. Per-Process GTT Enable Bit in GFX_MODE register controls the PPGTT enabling and disabling. Programming Per-Process GTT Enable Bit in GFX_MODE register doesn't enable/disable the PPGTT translation of memory access immediately; the change comes in to affect only when the Page Directory registers are programmed. Programming Per-Process GTT Enable Bit in GFX_MODE register bit must be followed by programming Page Directory Registers in order to enable or disable the PPGTT translation of memory access. PDP* DESCRIPTOR registers must always be programmed through MI_LOAD_REGISTER_IMMEDIATE command in ring buffer with PDP0_DESCRIPRTOR lower dword written at the end. PDP0/12/3 registers are context save restored. PDP descriptors are power context save restored in VCS, BCS and VECS engines. PDP descriptors are context save restored per render context in RCS and must be programmed following MI_SET_CONTEXT command, in case of PDP descriptors programmed without context set (MI_SET_CONTEXT) will get lost on C6 entry/exit. PDP descriptor registers should be programmed after ensuring the pipe is completely flushed and TLB's invalidated.	CHV, BSW

DWord	Bit	Description
0	63	**PD Load Busy**
		Project: CHV, BSW
		Access: RO
		Format: Valid
		This read-only field gets set when PDP0 is written to indicating Page Directory Restore activity is in progress and will get reset once the activity is completed.
	62:0	**PDP0 Descriptor**
		Project: CHV, BSW

Page Directory Pointer Descriptor - PDP1

<table>
<tr><td colspan="2" align="center">**PDP1 - Page Directory Pointer Descriptor - PDP1**</td></tr>
<tr><td>Register Space:</td><td>MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td>CHV, BSW</td></tr>
<tr><td>Source:</td><td>PRM</td></tr>
<tr><td>Default Value:</td><td>0x00000000, 0x00000000</td></tr>
<tr><td>Access:</td><td>R/W</td></tr>
<tr><td>Size (in bits):</td><td>64</td></tr>
<tr><td>Address:</td><td>02278h-0227Fh</td></tr>
<tr><td>Name:</td><td>Page Directory Pointer Descriptor - PDP1</td></tr>
<tr><td>ShortName:</td><td>PDP1_RCSUNIT</td></tr>
<tr><td>Address:</td><td>12278h-1227Fh</td></tr>
<tr><td>Name:</td><td>Page Directory Pointer Descriptor - PDP1</td></tr>
<tr><td>ShortName:</td><td>PDP1_VCSUNIT0</td></tr>
<tr><td>Address:</td><td>1A278h-1A27Fh</td></tr>
<tr><td>Name:</td><td>Page Directory Pointer Descriptor - PDP1</td></tr>
<tr><td>ShortName:</td><td>PDP1_VECSUNIT</td></tr>
<tr><td>Address:</td><td>1C278h-1C27Fh</td></tr>
<tr><td>Name:</td><td>Page Directory Pointer Descriptor - PDP1</td></tr>
<tr><td>ShortName:</td><td>PDP1_VCSUNIT1</td></tr>
<tr><td>Address:</td><td>22278h-2227Fh</td></tr>
<tr><td>Name:</td><td>Page Directory Pointer Descriptor - PDP1</td></tr>
<tr><td>ShortName:</td><td>PDP1_BCSUNIT</td></tr>
</table>

PDP1[38:12]: Pointer to one of the four page directory pointer (lowest+1) and defines the first 1-2GB of memory mapping. This is valid when Legacy Context Flag is set and 64bit virtual addressing is not supported. *Note: This is a guest physical address.*

DWord	Bit	Description
0	63:0	**PDP1 Descriptor**

Page Directory Pointer Descriptor - PDP2

PDP2 - Page Directory Pointer Descriptor - PDP2	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Address:	02280h-02287h
Name:	Page Directory Pointer Descriptor - PDP2
ShortName:	PDP2_RCSUNIT
Address:	12280h-12287h
Name:	Page Directory Pointer Descriptor - PDP2
ShortName:	PDP2_VCSUNIT0
Address:	1A280h-1A287h
Name:	Page Directory Pointer Descriptor - PDP2
ShortName:	PDP2_VECSUNIT
Address:	1C280h-1C287h
Name:	Page Directory Pointer Descriptor - PDP2
ShortName:	PDP2_VCSUNIT1
Address:	22280h-22287h
Name:	Page Directory Pointer Descriptor - PDP2
ShortName:	PDP2_BCSUNIT

PDP2[38:12]: Pointer to one of the four page directory pointer (lowest+2) and defines the first 2-3GB of memory mapping. This is valid when Legacy Context Flag is set and 64bit virtual addressing is not supported. *Note: This is a guest physical address.*

DWord	Bit	Description
0	63:0	**PDP2 Descriptor**

Page Directory Pointer Descriptor - PDP3

PDP3 - Page Directory Pointer Descriptor - PDP3	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Address:	02288h-0228Fh
Name:	Page Directory Pointer Descriptor - PDP3
ShortName:	PDP3_RCSUNIT
Address:	12288h-1228Fh
Name:	Page Directory Pointer Descriptor - PDP3
ShortName:	PDP3_VCSUNIT0
Address:	1A288h-1A28Fh
Name:	Page Directory Pointer Descriptor - PDP3
ShortName:	PDP3_VECSUNIT
Address:	1C288h-1C28Fh
Name:	Page Directory Pointer Descriptor - PDP3
ShortName:	PDP3_VCSUNIT1
Address:	22288h-2228Fh
Name:	Page Directory Pointer Descriptor - PDP3
ShortName:	PDP3_BCSUNIT

PDP3[38:12]: Pointer to one of the four page directory pointer (lowest+3) and defines the first 3-4GB of memory mapping. This is valid when Legacy Context Flag is set and 64bit virtual addressing is not supported. *Note: This is a guest physical address.*

DWord	Bit	Description
0	63:0	**PDP3 Descriptor**

Page Request Queue Address Register 0

PAGEREQ_QADDR_0 - Page Request Queue Address Register 0	
Register Space:	MMIO: 0/2/0
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0F0D0h

Register to configure the base address and size of the page request queue.

DWord	Bit	Description
0	31:12	**Page Request Queue Base Register**
		Default Value: 00000h
		Access: R/W
		This field points to the base of 4KB aligned invalidation request queue. Hardware may ignore and not implement bits 63:HAW, where HAW is the host address width. Reads of this field return the value that was last programmed to it.
	11:3	**Reserved**
		Default Value: 000000000b
		Access: RO
	2:0	**Queue Size**
		Default Value: 000b
		Access: R/W
		This field specifies the size of the page request queue. A value of X in this field indicates a page request queue of (2X) 4KB pages. The number of entries in the invalidation queue is 2(X+8).

Page Request Queue Address Register 1

PAGEREQ_QADDR_1 - Page Request Queue Address Register 1

Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32

Address:	0F0D4h

Register to configure the base address and size of the page request queue.

DWord	Bit	Description
0	31:0	**Page Request Queue Base Register**

Default Value:	00000000h
Access:	R/W

This field points to the base of 4KB aligned invalidation request queue. Hardware may ignore and not implement bits 63:HAW, where HAW is the host address width.
Reads of this field return the value that was last programmed to it.

Page Request Queue Head Register 0

PAGEREQ_QHEAD_0 - Page Request Queue Head Register 0	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0F0C0h

Register indicating the page request queue head.

DWord	Bit	Description	
0	31:19	**Reserved**	
		Default Value:	0000000000000b
		Access:	RO
	18:4	**Queue Head**	
		Default Value:	000000000000000b
		Access:	R/W
		Specifies the offset (128-bit aligned) to the page request queue for the command that is processed next by software. GFX implementation: GFX has to read the content of the Head pointer as tail pointer gets close to it to prevent overflows in page request queue.	
	3:0	**Reserved**	
		Default Value:	0h
		Access:	RO

Page Request Queue Head Register 1

PAGEREQ_QHEAD_1 - Page Request Queue Head Register 1	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0F0C4h

Register indicating the page request queue head.

DWord	Bit	Description
0	31:0	**Page Request Queue Head Register 1 Reserved**
		Default Value: 00000000h
		Access: RO
		Bit[63:32]: Reserved.

Page Request Queue Tail Register 0

<table>
<tr>
<td colspan="3" align="center">**PAGEREQ_QTAIL_0 - Page Request Queue Tail Register 0**</td>
</tr>
<tr>
<td colspan="3">Register Space: MMIO: 0/2/0</td>
</tr>
<tr>
<td colspan="3">Project: CHV, BSW</td>
</tr>
<tr>
<td colspan="3">Source: PRM</td>
</tr>
<tr>
<td colspan="3">Default Value: 0x00000000</td>
</tr>
<tr>
<td colspan="3">Size (in bits):   32</td>
</tr>
<tr>
<td colspan="3">Address: 0F0C8h</td>
</tr>
<tr>
<td colspan="3">Register indicating the page request queue tail.</td>
</tr>
<tr>
<td>**DWord**</td>
<td>**Bit**</td>
<td>**Description**</td>
</tr>
<tr>
<td>0</td>
<td>31:1</td>
<td>

Queue Tail

Default Value:	0000000000000000000000000000000b
Access:	R/W

Bit[31:19]: Reserved.
Bit[18:4]:
Specifies the offset (128-bit aligned) to the page request queue for the request that is written next by hardware.
GFX Implementation: GT manages the tail pointer value as part of page requests. The value can be acquired as part of the RC6 exit.
Bit[3:1]: Reserved.

</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>

Valid Bit

Default Value:	0b
Access:	R/W

This bit can only be cleared by SW, which also clears the other fields.

</td>
</tr>
</table>

Page Request Queue Tail Register 1

PAGEREQ_QTAIL_1 - Page Request Queue Tail Register 1		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F0CCh	
Register indicating the page request queue tail.		

DWord	Bit	Description
0	31:0	**Page Request Queue Tail Register 1 Reserved**
		Default Value: 00000000h
		Access: RO
		Bit[63:32]: Reserved.

PAK_Stream-Out Report (Errors)

PAK_ERR - PAK_Stream-Out Report (Errors)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	VideoCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	128E8h	
Valid Projects:	CHV, BSW	

DWord	Bit	Description
0	31:22	**Reserved** Format: MBZ
	21	**Incorrect IntraMBFlag in I-slice(AVCf)**
	20	**Out of Range Symbol Code(AVC/mpeg2)**
	19	**Incorrect MBType(AVC/mpeg2**
	18	**Motion Vectors are not inside the frame boundary(mpeg2)**
	17	**Scale code is zero(mpeg2)**
	16	**Incorrect DCTtype for given motionType(mpeg2)**
	15:8	**MB Y-position** This field indicates Macro Block(MB) Y- position where an error occured while encoding.
	7:0	**MB X-position** This field indicates Macro Block(MB) X- position where an error occured while encoding.

PAK_Stream-Out Report (Warnings)

PAK_WARN - PAK_Stream-Out Report (Warnings)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	VideoCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	128E4h	
Valid Projects:	CHV, BSW	

DWord	Bit	Description	
0	31:22	**Reserved**	
		Project:	All
		Format:	MBZ
	21	**Skip Run > 8192 (AVC)**	
	20	**Incorrect SkipMB (AVC and mpeg2)**	
	19	**Incorrect MV difference for dual-prime MB (mpeg2)**	
	18	**End of Slice signal missing on last MB of a Row(mpeg2)**	
	17	**Incorrect DCT type for field picture**	
	16	**MVs are not within defined range by fcode**	
	15:8	**MB Y-position**	
	7:0	**MB X-position**	

PAK Report Running Status

<table>
<tr><td colspan="2" align="center">**PAK_REPORT_STAT - PAK Report Running Status**</td></tr>
<tr><td>Register Space:</td><td>MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td>CHV, BSW</td></tr>
<tr><td>Source:</td><td>VideoCS</td></tr>
<tr><td>Default Value:</td><td>0x00000000</td></tr>
<tr><td>Access:</td><td>RO</td></tr>
<tr><td>Size (in bits):</td><td>32</td></tr>
<tr><td>Trusted Type:</td><td>1</td></tr>
<tr><td>Address:</td><td>128ECh</td></tr>
<tr><td>Valid Projects:</td><td>CHV, BSW</td></tr>
</table>

DWord	Bit	Description
0	31:1	**Reserved**
	0	**PAK Status**

Value	Name	Description
0		PAK engine is IDLE
1		PAK engine is currently generating bit stream.

PAT Index

<table>
<tr><td colspan="2" align="center">**PAT_INDEX - PAT Index**</td></tr>
<tr><td>Register Space:</td><td>MMIO: 0/2/0</td></tr>
<tr><td>Source:</td><td>PRM</td></tr>
<tr><td>Default Value:</td><td>0x00000003</td></tr>
<tr><td>Access:</td><td>R/W</td></tr>
<tr><td>Size (in bits):</td><td>32</td></tr>
</table>

DWord	Bit	Description
0	31:10	**Reserved** Default Value: 0000000000000000000000b
	9:8	**Class of Service** Default Value: 00b This field controls the Class of Service sent to the LLC to determine which sub-set of Ways the surface will be stored in. The allocation of certain LLC ways to different class of service settings is a project dependent decision and listed in the PRM 00: Class0 01: Class1 10: Class2 11: Class3
	7:6	**Reserved** Default Value: 00b
	5:4	**LRU AGE** Default Value: 00b 00: Take the age value from Uncore CRs 01: Assign the age of "0" 10: Do not change the age on a hit 11: Assign the age of "3"
	3:2	**Target Cache** Default Value: 00b 00: eLLC only 01: LLC only 10: LLC/eLLC allowed 11: LLC/eLLC allowed
	1:0	**Mem Type** Default Value: 11b 00: Uncacheable(UC) 01: Write Combining(WC) 10: Write through(WT) 11: Write back(WB)

PAT Index High

<table>
<tr><td colspan="3" align="center">**PAT_INDEX_H - PAT Index High**</td></tr>
<tr><td>Register Space:</td><td colspan="2">MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td colspan="2">CHV, BSW</td></tr>
<tr><td>Source:</td><td colspan="2">PRM</td></tr>
<tr><td>Default Value:</td><td colspan="2">0x03030303</td></tr>
<tr><td>Size (in bits):</td><td colspan="2">32</td></tr>
<tr><td>Address:</td><td colspan="2">040E4h</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td>**Description**</td></tr>
<tr><td>0</td><td>31:0</td><td>

PAT Index High

Default Value:	03030303h
Access:	R/W

Description

Bit[31:24]: PAT Index#7: Index#7 definition for page tables.
(See bit[7:0] for definition.)
Bit[23:16]: PAT Index#6: Index#6 definition for page tables.
(See bit[7:0] for definition.)
Bit[15:8]: PAT Index#5: Index#5 definition for page tables.
(See bit[7:0] for definition.)
Bit[7:0]: PAT Index#4: Index#4 definition for page tables.
Bit[7]: Reserved.
Bit[6]: Snoop Required [CHV, BSW Only]
1: System agent will snoop the IA cores
0: System agent will not snoop the IA cores
Bit[5:4]: (See below.)
00b: Age is 0.
01b: Age is 1.
10b: Age is 2.
11b: Age is 3.
Bit[3:2]: (See below.)
00b: eLLC only.
01b: LLC only.
10b: LLC and eLLC allowed.
11b: L3, LLC, and eLLC are allowed.
Bit[1:0]: (see below):
00b: Uncacheable (UC).
01b: Write Combining (WC).
10b: Write Through (WT).
11b: Write Back (WB).

</td></tr>
</table>

PAT Index Low

PAT_INDEX_L - PAT Index Low	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x03030303
Size (in bits):	32
Address:	040E0h

DWord	Bit	Description
0	31:0	**PAT Index Low** <table><tr><td>Default Value:</td><td>03030303h</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> **Description** Bit[31:24]: PAT Index#3: Index#3 definition for page tables. (See bit[7:0] for definition.) Bit[23:16]: PAT Index#2: Index#2 definition for page tables. (See bit[7:0] for definition.) Bit[15:8]: PAT Index#1: Index#1 definition for page tables. (See bit[7:0] for definition.) Bit[7:0]: PAT Index#0: Index#0 definition for page tables. Bit[7]: Reserved. Bit[6]: Snoop Required [CHV, BSW Only] 1: System agent will snoop the IA cores 0: System agent will not snoop the IA cores Bit[5:4]: (See below.) 00b: Age is 0. 01b: Age is 1. 10b: Age is 2. 11b: Age is 3. Bit[3:2]: (See below.) 00b: eLLC only. 01b: LLC only. 10b: LLC and eLLC allowed. 11b: L3, LLC, and eLLC are allowed. Bit[1:0]: (see below): 00b: Uncacheable (UC). 01b: Write Combining (WC). 10b: Write Through (WT). 11b: Write Back (WB).

PCBR

<table>
<tr><td colspan="3" align="center">**PCBR - PCBR**</td></tr>
<tr><td>Register Space:</td><td colspan="2">MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td colspan="2">CHV, BSW</td></tr>
<tr><td>Source:</td><td colspan="2">PRM</td></tr>
<tr><td>Default Value:</td><td colspan="2">0x00000000</td></tr>
<tr><td>Size (in bits):</td><td colspan="2">32</td></tr>
<tr><td>Address:</td><td colspan="2">182120h</td></tr>
<tr><td colspan="3">This provides a base address for context save/restore of GT and Media power context to DRAM. Gunit adds the GAM provided offsets to this base register for power context reads and writes.
GTLC stores Power Context in DRAM.
The BIOS is expected to program this register and ensure proper allocation within Gfx stolen memory.

Removing bits 63:32 since this will always be below 4GB.</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td>**Description**</td></tr>
<tr><td>0</td><td>31:12</td><td>**Power_Context_Address**

<table><tr><td>Default Value:</td><td>0000000h</td></tr><tr><td>Access:</td><td>R/W Lock</td></tr></table>4KB aligned address. Locked with bit 0.</td></tr>
<tr><td></td><td>11:1</td><td>**Reserved**

<table><tr><td>Default Value:</td><td>000h</td></tr><tr><td>Access:</td><td>RO</td></tr></table>Reserved</td></tr>
<tr><td></td><td>0</td><td>**Power_Context_Register_Lock**

<table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W Lock</td></tr></table>Writing a '1' to this register locks this bit - preventing further updates. The Power Context Address bits are also locked.</td></tr>
</table>

PCICMD_STS

PCICMD_STS - PCICMD_STS		
Register Space:	PCI: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00100000	
Size (in bits):	32	
Address:	00004h	

04h: PCI Command Register. 06h: PCI Status Register

DWord	Bit	Description		
0	31:21	**RESERVED**		
		Default Value:		000h
		Access:		RO
	20	**CAPABILITY_LIST**		
		Default Value:		1b
		Access:		RO
		CAP: Indicates that the CAPPOINT register at 34h provides an offset into PCI Configuration Space containing a pointer to the location of the first item in the list		
	19	**INTERRUPT_STATUS**		
		Default Value:		0b
		Access:		RO
	18:16	**RESERVED**		
		Default Value:		000b
		Access:		RO
	15:11	**RESERVED**		
		Default Value:		00h
	10	**INTERRUPT_DISABLE**		
		Default Value:		0b
		Access:		R/W
		ID: 0 : Legacy interrupt message is enabled. ID: 1 : Disables legacy interrupt message generation on IOSF Sideband. Note : The interrupt status is not blocked from being reflected in PCISTS.IS. Note: MSI interrupt generation : (PCISTS.IS and PCICMD.BME and MSI_CAPID.MSIE) changes from 0 to 1. Note: Message bus interrupt assert is sent : (PCISTS.IS and ~PCICMD.ID and ~MSI_CAPID.MSIE) changes from 0 to 1. Note: Message bus interrupt de-assert is sent : (PCISTS.IS and ~PCICMD.ID and ~MSI_CAPID.MSIE) changes from 1 to 0.		

PCICMD_STS - PCICMD_STS

9:3	**RESERVED**	
	Default Value:	00h
	Access:	RO
	Reserved	
2	**BUS_MASTER_ENABLE**	
	Default Value:	0b
	Access:	R/W
	BME: (BME and MAE are observed. But context save/restore can occur.) 0 : Blocks the sending of MSI interrupts. 1 : Permits the sending of MSI interrupts	
1	**Reserved**	
0	**IO_SPACE_ENABLE**	
	Default Value:	0b
	Access:	R/W
	IOSE: 0 : I/O space is disabled. IORD and IOWr cycles will not be claimed. 1 : I/O space is enabled. VGA_IO and Gfx_IOBAR are checked. If an IORD/IOWR matches (VGA IO address range or GFX_IOBAR), the cycle will be claimed. Care should be taken in setting up GFX_IOBAR that more than 1 match is not made as this will result in unpredictable behavior. VGA_IO : Address[15:0] is checked to determine if it falls in the VGA IO range. (The VGA IO range is 03B0h - 03BBh and 03C0h - 03DFh.) Gfx_IOBAR : Address[15:3] is compared to GFX_IOBAR[15:3].	

PCU INTERRUPT ENABLE REGISTER

PCU_INTERRUPT_IER - PCU INTERRUPT ENABLE REGISTER		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	444ECh-444EFh	
This table indicates which events are mapped to each bit of the GT interrupt 1 register. The IER enabled PCU interrupt IIR sticky bits are ORed together to generate PCU interrupt pending bit in the master interrupt control register.		

DWord	Bit	Description
0	31:26	**UNUSED0**
		Access: R/W
	25	**PCU_MAILBOX_EVT**
		Access: R/W
		PCU Pcode 2 driver mailbox event
	24	**PCU_THERMAL_EVT**
		Access: R/W
		PCU thermal event
	23:0	**UNUSED1**
		Access: R/W

PCU INTERRUPT IDENTITY REGISTER

PCU_INTERRUPT_IIR - PCU INTERRUPT IDENTITY REGISTER		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	444E8h-444EBh	

This table indicates which events are mapped to each bit of the GT interrupt 1 register.
The IER enabled PCU interrupt IIR sticky bits are ORed together
to generate PCU interrupt pending bit in the master interrupt control register.

DWord	Bit	Description
0	31:26	**UNUSED0**
		Access: R/W One Clear
	25	**PCU_MAILBOX_EVT**
		Access: R/W One Clear
		PCU Pcode 2 driver mailbox event
	24	**PCU_THERMAL_EVT**
		Access: R/W One Clear
		PCU thermal event
	23:0	**UNUSED1**
		Access: R/W One Clear

PCU INTERRUPT MASK REGISTER

PCU_INTERRUPT_IMR - PCU INTERRUPT MASK REGISTER		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x03000000	
Size (in bits):	32	
Address:	444E4h-444E7h	

This table indicates which events are mapped to each bit of the GT interrupt 1 register.
The IER enabled PCU interrupt IIR sticky bits are ORed together
to generate PCU interrupt pending bit in the master interrupt control register.

DWord	Bit	Description	
0	31:26	**UNUSED0**	
		Access:	R/W
	25	**PCU_MAILBOX_EVT**	
		Default Value:	1b
		Access:	R/W
		PCU Pcode 2 driver mailbox event	
	24	**PCU_THERMAL_EVT**	
		Default Value:	1b
		Access:	R/W
		PCU thermal event	
	23:0	**UNUSED1**	
		Access:	R/W

PCU INTERRUPT STATUS REGISTER

PCU_INTERRUPT_ISR - PCU INTERRUPT STATUS REGISTER		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	444E0h-444E3h	
This table indicates which events are mapped to each bit of the GT interrupt 1 register. The IER enabled PCU interrupt IIR sticky bits are ORed together to generate PCU interrupt pending bit in the master interrupt control register.		

DWord	Bit	Description
0	31:26	**UNUSED0**
		Access: RO
	25	**PCU_MAILBOX_EVT**
		Access: RO
		PCU Pcode 2 driver mailbox event
	24	**PCU_THERMAL_EVT**
		Access: RO
		PCU thermal event
	23:0	**UNUSED1**
		Access: RO

Pending Head Pointer Register

UHPTR - Pending Head Pointer Register	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02134h-02137h
Name:	Pending Head Pointer Register
ShortName:	UHPTR_RCSUNIT
Address:	12134h-12137h
Name:	Pending Head Pointer Register
ShortName:	UHPTR_VCSUNIT0
Address:	1A134h-1A137h
Name:	Pending Head Pointer Register
ShortName:	UHPTR_VECSUNIT
Address:	1C134h-1C137h
Name:	Pending Head Pointer Register
ShortName:	UHPTR_VCSUNIT1
Address:	22134h-22137h
Name:	Pending Head Pointer Register
ShortName:	UHPTR_BCSUNIT

Programming Notes	Source
Once SW uses UHPTR to preempt the existing workload, should explicitly program MI_SET_CONTEXT to save the preempted context status before submitting the new workload. In case SW doesn't want to save the state of the preempted context, it should at the minimum program RS_PREEMPT_STATUS to 0x0 so that the register status doesn't interfere with the new workloads.	RenderCS

DWord	Bit	Description
0	31:3	**Head Pointer Address**

Format:	GraphicsAddress[31:3]

Description
This register represents the GFX address offset where execution should continue in the ring buffer following execution of a Preemptable Command. Refer to the Preemption section for the list of preemptable commands supported in ring buffer mode of scheduling.

　　　　　　　　　　　　　　　　　　　　　　　　Doc Ref # IHD-OS-CHV-BSW-Vol 2c-06.15

UHPTR - Pending Head Pointer Register

	2:1	**Reserved**	
		Format:	MBZ

	0	**Head Pointer Valid**

Description
This bit is set by the software to request a pre-emption.
It is reset by hardware when a Preemptable command is parsed by the command streamer. The hardware uses the head pointer programmed in this register at the time the reset is generated. Refer to the Preemption section for the list of preemptable commands supported in ring buffer mode of scheduling.
This bit is treated as set by command streamer only when arbitration is not disabled using MI_ARB_ON_OFF command. Preemption will not occur on MI_ARB_CHEK command when UHPTR is valid if the arbitration is disabled using MI_ARB_ON_OFF command.

Value	Name	Description
0	InValid	No valid updated head pointer register, resume execution at the current location in the ring buffer
1	Valid	Indicates that there is an updated head pointer programmed in this register

Plink G2H Spare

SPAREG2H - Plink G2H Spare		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A194h-0A197h	

DWord	Bit	Description
0	31:9	**Reserved**
		Access: RO
	8:0	**Plink_G2H_Spare**
		Access: R/W
		These are spares for ECO use.

PM_PWR_CLK_STATE

PM_PWR_CLK_STATE - PM_PWR_CLK_STATE		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00008288	
Size (in bits):	32	
Address:	0A200h	
PM Power Clock State Request		

DWord	Bit	Description
0	31	**Enable**
		Access: R/W
		Power Clock State Enable: 0 : No specific power state set, no message/wait with PMunit 1 : CSunit sends the contents of this register to PMunit each time it is written, Send contents of this register to PMunit, wait for Ack. When CS writes to A200, requesting new set of resources: Actual EUs used = Async_EU if EUmin < Async_EU < EUmax Actual EUs used = EUmax if Async_EU > equal to EUmax Actual EUs used = EUmin if EUmin > equal to Async_EU Actual SSs used = Async_SS if SScountEn=0 Actual SSs used = SScount if SScountEn=1 After new resources are set by GPMunit, GPM replies to CS by writing 0001_0001 to 0x00_300c
	30:19	**RSVD**
		Access: RO
		Reserved (CSunit implements full 32b storage)
	18	**SCountEn**
		Access: R/W

Programming Notes	Project
Not supported in CHV, BSW. Must be zero (MBZ).	CHV, BSW

	17:15	**SliceCount**
		Default Value: 001b
		Access: R/W

Programming Notes	Project
Not supported in CHV, BSW. Must be zero (MBZ).	CHV, BSW

PM_PWR_CLK_STATE - PM_PWR_CLK_STATE

14:13	**RSVD**	
	Access:	RO
	Reserved (CSunit implements full 32b storage)	

12	**Spare**	
	Access:	R/W
	Spare bit for CHV, BSW	

Programming Notes	**Project**
Must be zero (MBZ).	CHV, BSW

11	**SSCountEn**	
	Access:	R/W
	Enable Subslice Count Request 0 = Use async PMunit subslice count request 1 = Use SliceCount from this register	

10:8	**SScount**	
	Default Value:	010b
	Access:	R/W
	Number of subslices to power: 001 : 1 subslice 010 : 2 subslices (GT1-based CHV, BSW only)	

7:4	**EUmax**	
	Default Value:	1000b
	Access:	R/W
	Maximum number of EUs to power (per subslice if multiple subslices enabled). To specify an exact number of subslices, set EUmax equal to EUmin MinEU and MaxEU need to be even and that odd numbers are illegal	

3:0	**EUmin**	
	Default Value:	1000b
	Access:	R/W
	Minimum number of EUs to power (per subslice if multiple subslices enabled): 0010 : 2 EUs 0100 : 4 EUs 0110 : 6 EUs 1000 :8 EUs MinEU and MaxEU need to be even and that odd numbers are illegal When both subslices are enabled (ie 0x18_2168[11:10] = 2'b00)	

PM_PWR_CLK_STATE - PM_PWR_CLK_STATE

Config	Disabled Column	FUSE_GT_EU_DISABLE - 0x18_2168[31:16]	Desired Config	Actual/Driver Config
2x8	none	0x0000	2x8	2x8
2x8	none	0x0000	2x6	2x6
2x8	none	0x0000	2x4	2x4
2x8	none	0x0000	2x2	2x2
2x6	1	0x1111	2x8	NA
2x6	1	0x1111	2x6	2x8
2x6	1	0x1111	2x4	2x6
2x6	1	0x1111	2x2	2x4
2x6	2	0x2222	2x8	NA
2x6	2	0x2222	2x6	2x8
2x6	2	0x2222	2x4	2x6
2x6	2	0x2222	2x2	2x2
2x6	3	0x4444	2x8	NA
2x6	3	0x4444	2x6	2x8
2x6	3	0x4444	2x4	2x4
2x6	3	0x4444	2x2	2x2
2x6	4	0x8888	2x8	NA
2x6	4	0x8888	2x6	2x6
2x6	4	0x8888	2x4	2x4
2x6	4	0x8888	2x2	2x2
2x5	1+EU3	0x1919	2x8	NA
2x5	1+EU3	0x1919	2x5	2x8
2x5	1+EU3	0x1919	2x4	2x6
2x5	1+EU3	0x1919	2x2	2x4
2x5	2+EU3	0x2A2A	2x8	NA
2x5	2+EU3	0x2A2A	2x5	2x8
2x5	2+EU3	0x2A2A	2x4	2x6
2x5	2+EU3	0x2A2A	2x2	2x2

PM_PWR_CLK_STATE - PM_PWR_CLK_STATE

2x5	3+EU3	0x4C4C		2x8	NA
2x5	3+EU3	0x4C4C		2x5	2x8
2x5	3+EU3	0x4C4C		2x4	2x4
2x5	3+EU3	0x4C4C		2x2	2x2
2x5	4+EU2	0x8C8C		2x8	NA
2x5	4+EU2	0x8C8C		2x5	2x6
2x5	4+EU2	0x8C8C		2x4	2x4
2x5	4+EU2	0x8C8C		2x2	2x2

PMCAPID

<table>
<tr><td colspan="3" align="center">**PMCAPID - PMCAPID**</td></tr>
<tr><td colspan="3">Register Space: PCI: 0/2/0
Project: CHV, BSW
Source: PRM
Default Value: 0x00229001
Size (in bits):   32</td></tr>
<tr><td colspan="3">Address: 000D0h</td></tr>
<tr><td colspan="3">PCI Address: D0-D1h Description : Power Management Capabilities ID
PCI Address: D2-D3h Description : Power Management Capabilities</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td>**Description**</td></tr>
<tr><td>0</td><td>31:27</td><td>**PME_SUPPORT**
<table><tr><td>Default Value:</td><td>00h</td></tr><tr><td>Access:</td><td>RO</td></tr></table>PMES The graphics controller does not generate PME.</td></tr>
<tr><td></td><td>26</td><td>**D2_SUPPORT**
<table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>RO</td></tr></table>D2S: D2 power management state is not supported.</td></tr>
<tr><td></td><td>25</td><td>**D1_SUPPORT**
<table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>RO</td></tr></table>D1S: D1 power management state is not supported.</td></tr>
<tr><td></td><td>24:22</td><td>**RESERVED**
<table><tr><td>Default Value:</td><td>000b</td></tr><tr><td>Access:</td><td>RO</td></tr></table>Reserved</td></tr>
<tr><td></td><td>21</td><td>**DEVICE_SPECIFIC_INITIALIZATION**
<table><tr><td>Default Value:</td><td>1b</td></tr><tr><td>Access:</td><td>RO</td></tr></table>Hardwired to 1 to indicate that special initialization of the graphics controller is required before generic class device driver is to use it.</td></tr>
<tr><td></td><td>20:19</td><td>**RESERVED**
<table><tr><td>Default Value:</td><td>00b</td></tr></table></td></tr>
</table>

PMCAPID - PMCAPID

		Access:		RO
		Reserved		
	18:16	**VERSION**		
		Default Value:		010b
		Access:		RO
		Verion compliance with revision 1.1 of PCI Power management spec.		
	15:8	**NEXT_POINTER**		
		Default Value:	90h	
		Access:	R/W Once	
		Indicates the next item in the capabilities list(90=MSI) This register should be programmed by BIOS during boot-up. Once written, this register becomes Read_Only. This register can only be cleared by a Reset. Write once allowing changing of the capabilities list.		
	7:0	**CAPABILITIES_ID**		
		Default Value:	01h	
		Access:	RO	
		CAPID: SIG defines this ID is 01h for power management.		

PMCS

<table>
<tr><td colspan="3" align="center">**PMCS - PMCS**</td></tr>
<tr><td>Register Space:</td><td colspan="2">PCI: 0/2/0</td></tr>
<tr><td>Project:</td><td colspan="2">CHV, BSW</td></tr>
<tr><td>Source:</td><td colspan="2">PRM</td></tr>
<tr><td>Default Value:</td><td colspan="2">0x00000000</td></tr>
<tr><td>Size (in bits):</td><td colspan="2">32</td></tr>
<tr><td>Address:</td><td colspan="2">000D4h</td></tr>
<tr><td colspan="3">Power Management Control/Status. Driver does not use this register. SBIOS does not use this register</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td>**Description**</td></tr>
<tr><td>0</td><td>31:2</td><td>**RESERVED**

Default Value:	00000000h
Access:	RO

Reserved</td></tr>
<tr><td></td><td>1:0</td><td>**POWER_STATE_PS**

Default Value:	00b
Access:	R/W

This field indicates the current power state of the IGD and can be used to set the IGD into a new power state. If software attempts to write an unsupported state to this field, write operation must complete normally on the bus, but the data is discarded and no state change occurs. On a transition from D3 to D0 the graphics controller is optionally reset to initial values. Behavior of the graphics controller in supported states is detailed in the power management section of the PRM. Bits[1:0] Power state 00: D0 Default 01: D1 Not Supported 10: D2 Not Supported 11: D3</td></tr>
</table>

POWER_WELL_SS0_SIG1

POWER_WELL_SS0_SIG1 - POWER_WELL_SS0_SIG1	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x02020242
Size (in bits):	32
Address:	0A720h

Subwell signals to be driven out to subslice0 wells: Subwells 1-4.
This register is modified by HW based on sub-power domain configuration and SW should not be writing to this register.

DWord	Bit	Description	
0	31:30	**Reserved**	
		Default Value:	00b
		Access:	RO
		Reserved	
	29	**ss0_eu210_rst_b**	
		Default Value:	0b
		Access:	R/W
		Subwell control signal 'rst_b' for subwell 'ss0_eu210'	
	28	**ss0_eu210_fwenb**	
		Default Value:	0b
		Access:	R/W
		Subwell control signal 'fwenb' for subwell 'ss0_eu210'	
	27	**ss0_eu210_pwrok**	
		Default Value:	0b
		Access:	R/W
		Subwell control signal 'pwrok' for subwell 'ss0_eu210'	
	26	**ss0_eu210_asyncrst_b**	
		Default Value:	0b
		Access:	R/W
		Subwell control signal 'asyncrst_b' for subwell 'ss0_eu210'	
	25	**ss0_eu210_pgenb**	

POWER_WELL_SS0_SIG1 - POWER_WELL_SS0_SIG1

		Default Value:	1b
		Access:	R/W

Subwell control signal 'pgenb' for subwell 'ss0_eu210'
0 = sub-well is powered on.
1 = sub-well is powered off.

	24	**ss0_eu210_clocken**	
		Default Value:	0b
		Access:	R/W

Subwell control signal 'clocken' for subwell 'ss0_eu210'

	23:22	**Reserved**	
		Default Value:	00b
		Access:	RO

Reserved

	21	**ss0_eu19_rst_b**	
		Default Value:	0b
		Access:	R/W

Subwell control signal 'rst_b' for subwell 'ss0_eu19'

	20	**ss0_eu19_fwenb**	
		Default Value:	0b
		Access:	R/W

Subwell control signal 'fwenb' for subwell 'ss0_eu19'

	19	**ss0_eu19_pwrok**	
		Default Value:	0b
		Access:	R/W

Subwell control signal 'pwrok' for subwell 'ss0_eu19'

	18	**ss0_eu19_asyncrst_b**	
		Default Value:	0b
		Access:	R/W

Subwell control signal 'asyncrst_b' for subwell 'ss0_eu19'

	17	**ss0_eu19_pgenb**	
		Default Value:	1b
		Access:	R/W

POWER_WELL_SS0_SIG1 - POWER_WELL_SS0_SIG1

		Subwell control signal 'pgenb' for subwell 'ss0_eu19' 0 = sub-well is powered on. 1 = sub-well is powered off.	
	16	**ss0_eu19_clocken**	
		Default Value:	0b
		Access:	R/W
		Subwell control signal 'clocken' for subwell 'ss0_eu19'	
	15:14	**Reserved**	
		Default Value:	00b
		Access:	RO
		Reserved	
	13	**ss0_eu08_rst_b**	
		Default Value:	0b
		Access:	R/W
		Subwell control signal 'rst_b' for subwell 'ss0_eu08'	
	12	**ss0_eu08_fwenb**	
		Default Value:	0b
		Access:	R/W
		Subwell control signal 'fwenb' for subwell 'ss0_eu08'	
	11	**ss0_eu08_pwrok**	
		Default Value:	0b
		Access:	R/W
		Subwell control signal 'pwrok' for subwell 'ss0_eu08'	
	10	**ss0_eu08_asyncrst_b**	
		Default Value:	0b
		Access:	R/W
		Subwell control signal 'asyncrst_b' for subwell 'ss0_eu08'	
	9	**ss0_eu08_pgenb**	
		Default Value:	1b
		Access:	R/W
		Subwell control signal 'pgenb' for subwell 'ss0_eu08' 0 = sub-well is powered on. 1 = sub-well is powered off.	

POWER_WELL_SS0_SIG1 - POWER_WELL_SS0_SIG1

	8	**ss0_eu08_clocken**	
		Default Value:	0b
		Access:	R/W
		Subwell control signal 'clocken' for subwell 'ss0_eu08'	
	7	**Reserved**	
		Default Value:	0b
		Access:	RO
		Reserved	
	6	**ss0_pgenb_sig1**	
		Default Value:	1b
		Access:	R/W
		Subwell control signal 'pgenb' for subwell 'ss0_ss0'	
	5	**ss0_rst_b**	
		Default Value:	0b
		Access:	R/W
		Subwell control signal 'rst_b' for subwell 'ss0_ss0'	
	4	**ss0_fwenb**	
		Default Value:	0b
		Access:	R/W
		Subwell control signal 'fwenb' for subwell 'ss0_ss0'	
	3	**ss0_pwrok**	
		Default Value:	0b
		Access:	R/W
		Subwell control signal 'pwrok' for subwell 'ss0_ss0'	
	2	**ss0_asyncrst_b**	
		Default Value:	0b
		Access:	R/W
		Subwell control signal 'asyncrst_b' for subwell 'ss0_ss0'	
	1	**ss0_pgenb_sig0**	
		Default Value:	1b
		Access:	R/W

POWER_WELL_SS0_SIG1 - POWER_WELL_SS0_SIG1

		Subwell control signal 'pgenb' for subwell 'ss0_ss0' 0 = sub-well is powered on. 1 = sub-well is powered off.	
	0	**ss0_clocken**	
		Default Value:	0b
		Access:	R/W
		Subwell control signal 'clocken' for subwell 'ss0_ss0'	

POWER_WELL_SS0_SIG2

POWER_WELL_SS0_SIG2 - POWER_WELL_SS0_SIG2		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000002	
Size (in bits):	32	
Address:	0A724h	
Subwell signals to be driven out to subslice0 wells: subwell 5. This register is modified by HW based on sub-power domain configuration and SW should not be writing to this register.		

DWord	Bit	Description	
0	31:6	**Reserved**	
		Default Value:	0000000h
		Access:	RO
		Reserved	
	5	**ss0_eu311_rst_b**	
		Default Value:	0b
		Access:	R/W
		Subwell control signal 'rst_b' for subwell 'ss0_eu311'	
	4	**ss0_eu311_fwenb**	
		Default Value:	0b
		Access:	R/W
		Subwell control signal 'fwenb' for subwell 'ss0_eu311'	
	3	**ss0_eu311_pwrok**	
		Default Value:	0b
		Access:	R/W
		Subwell control signal 'pwrok' for subwell 'ss0_eu311'	
	2	**ss0_eu311_asyncrst_b**	
		Default Value:	0b
		Access:	R/W
		Subwell control signal 'asyncrst_b' for subwell 'ss0_eu311'	
	1	**ss0_eu311_pgenb**	

POWER_WELL_SS0_SIG2 - POWER_WELL_SS0_SIG2

		Default Value:	1b
		Access:	R/W

Subwell control signal 'pgenb' for subwell 'ss0_eu311'
0 = sub-well is powered on.
1 = sub-well is powered off.

0	**ss0_eu311_clocken**		
	Default Value:	0b
	Access:	R/W

Subwell control signal 'clocken' for subwell 'ss0_eu311'

POWER_WELL_SS1_SIG1

POWER_WELL_SS1_SIG1 - POWER_WELL_SS1_SIG1

Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x02020242
Size (in bits):	32
Address:	0A728h

Subwell signals to be driven out to subslice1 wells: Subwells 1-4.
This register is modified by HW based on sub-power domain configuration and SW should not be writing to this register.

DWord	Bit	Description
0	31:30	**Reserved**
		Default Value: 00b
		Access: RO
		Reserved
	29	**ss1_eu210_rst_b**
		Default Value: 0b
		Access: R/W
		Subwell control signal 'rst_b' for subwell 'ss1_eu210'
	28	**ss1_eu210_fwenb**
		Default Value: 0b
		Access: R/W
		Subwell control signal 'fwenb' for subwell 'ss1_eu210'
	27	**ss1_eu210_pwrok**
		Default Value: 0b
		Access: R/W
		Subwell control signal 'pwrok' for subwell 'ss1_eu210'
	26	**ss1_eu210_asyncrst_b**
		Default Value: 0b
		Access: R/W
		Subwell control signal 'asyncrst_b' for subwell 'ss1_eu210'
	25	**ss1_eu210_pgenb**

POWER_WELL_SS1_SIG1 - POWER_WELL_SS1_SIG1

		Default Value:	1b
		Access:	R/W

Subwell control signal 'pgenb' for subwell 'ss1_eu210'
0 = sub-well is powered on.
1 = sub-well is powered off.

24	**ss1_eu210_clocken**		
		Default Value:	0b
		Access:	R/W

Subwell control signal 'clocken' for subwell 'ss1_eu210'

23:22	**Reserved**		
		Default Value:	00b
		Access:	RO

Reserved

21	**ss1_eu19_rst_b**		
		Default Value:	0b
		Access:	R/W

Subwell control signal 'rst_b ' for subwell 'ss1_eu19'

20	**ss1_eu19_fwenb**		
		Default Value:	0b
		Access:	R/W

Subwell control signal 'fwenb' for subwell 'ss1_eu19'

19	**ss1_eu19_pwrok**		
		Default Value:	0b
		Access:	R/W

Subwell control signal 'pwrok' for subwell 'ss1_eu19'

18	**ss1_eu19_asyncrst_b**		
		Default Value:	0b
		Access:	R/W

Subwell control signal 'asyncrst_b' for subwell 'ss1_eu19'

17	**ss1_eu19_pgenb**		
		Default Value:	1b
		Access:	R/W

POWER_WELL_SS1_SIG1 - POWER_WELL_SS1_SIG1

	Subwell control signal 'pgenb' for subwell 'ss1_eu19' 0 = sub-well is powered on. 1 = sub-well is powered off.	

16	**ss1_eu19_clocken**	
	Default Value:	0b
	Access:	R/W
	Subwell control signal 'clocken' for subwell 'ss1_eu19'	

15:14	**Reserved**	
	Default Value:	00b
	Access:	RO
	Reserved	

13	**ss1_eu08_rst_b**	
	Default Value:	0b
	Access:	R/W
	Subwell control signal 'rst_b ' for subwell 'ss1_eu08'	

12	**ss1_eu08_fwenb**	
	Default Value:	0b
	Access:	R/W
	Subwell control signal 'fwenb' for subwell 'ss1_eu08'	

11	**ss1_eu08_pwrok**	
	Default Value:	0b
	Access:	R/W
	Subwell control signal 'pwrok' for subwell 'ss1_eu08'	

10	**ss1_eu08_asyncrst_b**	
	Default Value:	0b
	Access:	R/W
	Subwell control signal 'asyncrst_b' for subwell 'ss1_eu08'	

9	**ss1_eu08_pgenb**	
	Default Value:	1b
	Access:	R/W
	Subwell control signal 'pgenb' for subwell 'ss1_eu08' 0 = sub-well is powered on. 1 = sub-well is powered off.	

POWER_WELL_SS1_SIG1 - POWER_WELL_SS1_SIG1

8	**ss1_eu08_clocken**	
	Default Value:	0b
	Access:	R/W
	Subwell control signal 'clocken' for subwell 'ss1_eu08'	

7	**Reserved**	
	Default Value:	0b
	Access:	RO
	Reserved	

6	**ss1_pgenb_sig1**	
	Default Value:	1b
	Access:	R/W
	Subwell control signal 'pgenb' for subwell 'ss1_ss1'	

5	**ss1_rst_b**	
	Default Value:	0b
	Access:	R/W
	Subwell control signal 'rst_b ' for subwell 'ss1_ss1'	

4	**ss1_fwenb**	
	Default Value:	0b
	Access:	R/W
	Subwell control signal 'fwenb' for subwell 'ss1_ss1'	

3	**ss1_pwrok**	
	Default Value:	0b
	Access:	R/W
	Subwell control signal 'pwrok' for subwell 'ss1_ss1'	

2	**ss1_asyncrst_b**	
	Default Value:	0b
	Access:	R/W
	Subwell control signal 'asyncrst_b' for subwell 'ss1_ss1'	

1	**ss1_pgenb_sig0**	
	Default Value:	1b
	Access:	R/W

POWER_WELL_SS1_SIG1 - POWER_WELL_SS1_SIG1			
		Subwell control signal 'pgenb' for subwell 'ss1_ss1' 0 = sub-well is powered on. 1 = sub-well is powered off.	
	0	**ss1_clocken**	
		Default Value:	0b
		Access:	R/W
		Subwell control signal 'clocken' for subwell 'ss1_ss1'	

POWER_WELL_SS1_SIG2

POWER_WELL_SS1_SIG2 - POWER_WELL_SS1_SIG2	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000002
Size (in bits):	32
Address:	0A72Ch
Subwell signals to be driven out to subslice1 wells: subwell 5. This register is modified by HW based on sub-power domain configuration and SW should not be writing to this register.	

DWord	Bit	Description
0	31:6	**Reserved**
		<table><tr><td>Default Value:</td><td>0000000h</td></tr><tr><td>Access:</td><td>RO</td></tr></table> Reserved
	5	**ss1_eu311_rst_b**
		<table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> Subwell control signal 'rst_b' for subwell 'ss1_eu311'
	4	**ss1_eu311_fwenb**
		<table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> Subwell control signal 'fwenb' for subwell 'ss1_eu311'
	3	**ss1_eu311_pwrok**
		<table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> Subwell control signal 'pwrok' for subwell 'ss1_eu311'
	2	**ss1_eu311_asyncrst_b**
		<table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> Subwell control signal 'asyncrst_b' for subwell 'ss1_eu311'

POWER_WELL_SS1_SIG2 - POWER_WELL_SS1_SIG2

	1	**ss1_eu311_pgenb**	
		Default Value:	1b
		Access:	R/W
		Subwell control signal 'pgenb' for subwell 'ss1_eu311' 0 = sub-well is powered on. 1 = sub-well is powered off.	
	0	**ss1_eu311_clocken**	
		Default Value:	0b
		Access:	R/W
		Subwell control signal 'clocken' for subwell 'ss1_eu311'	

Power Context Save

PWRCTXSAVE - Power Context Save		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04A04h	

DWord	Bit	Description
0	31:16	**Mask Bits**
		<table><tr><td>Default Value:</td><td>0000h</td></tr><tr><td>Access:</td><td>RO</td></tr></table>
	15	**Extra Bits15**
		<table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> Extra Bits for future use.
	14	**Extra Bits14**
		<table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> Extra Bits for future use.
	13	**Extra Bits13**
		<table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> Extra Bits for future use.
	12	**Extra Bits12**
		<table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> Extra Bits for future use.
	11	**Extra Bits11**
		<table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> Extra Bits for future use.
	10	**Extra Bits10**
		<table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> Extra Bits for future use.

PWRCTXSAVE - Power Context Save

	9	**Power Context Save Request**		
		Default Value:		0b
		Access:		R/W
		Power Context Save. Bit[9].Power Context Save Request. 1'b0: Power context save is not being requested (default). 1'b1: Power context save is being requested. Unit needs to self-clear this bit upon sampling. This bit is self clear.		
	8:0	**Power Context Save Quad Word Credits**		
		Default Value:	000000000b	
		Access:	R/W	
		Power Context Save. Bits[8:0].QWord Credits for Power Context Save Request. An initial length packet is required per power context save session, but that packet does not consume a credit. See protocol description for more details. Minimum Credits = 1: Unit may send 1 QWord pair. Maximum Credits = 511: Unit may send 511 QWord pairs. A QWord pair is defined as a 32-bit register address and the corresponding 32-bits of register data. Only valid with PWRCTX_SAVE_REQ (Bit9).		

Power context Save Register for LPFC

LPCSR - Power context Save Register for LPFC		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0B408h	

DWord	Bit	Description
0	31:10	**Reserved**
		Access: RO
		Reserved.
	9:0	**Power context save register command**
		Access: R/W Hardware Clear
		Bit[9].Power Context Save Request. 1'b0: Power context save is not being requested (default). 1'b1: Power context save is being requested. Unit needs to self-clear this bit upon sampling. Bits[8:0].QWord Credits for Power Context Save Request. Minimum Credits = 1: Unit may send 1 QWord pair (enough for first LRI at least). Maximum Credits = 511: Unit may send 511 QWord pairs. A QWord pair is defined as a 32-bit register address and the corresponding 32-bits of register data. Note that the LRI header and END commands are 64-bits each (32-bit command followed by 32-bit NOOP) and consume one QWord credit. Only valid with PWRCTX_SAVE_REQ (Bit9).

Power Context Save request

	PCTXSAVEREQ - Power Context Save request	
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	08110h	

DWord	Bit	Description
0	31:16	**Message Mask**
		Access: RO
		Message Mask bots for lower 16 bits
	15:10	**Reserved**
		Access: RO
		Reserved
	9	**Power context save req**
		Access: R/W Set
		Power Context Save Request 1'b0 : Power context save is not being requested (default) 1'b1 : Power context save is being requested CPUnit self-clears this bit upon sampling.
	8:0	**Power Context Save request credit count**
		Access: R/W
		QWord Credits for Power Context Save Request Minimum Credits = 1 : Unit may send 1 QWord pair (enough for first LRI at least) Maximum Credits = 511 : Unit may send 511 QWord pairs A QWord pair is defined as a 32-bit register address and the corresponding 32-bits of register data. Note that the LRI header and END commands are 64-bits each (32-bit command followed by 32-bit NOOP) and will consume one QWord credit. Only valid with PWRCTX_SAVE_REQ (Bit9).

POWERDOWN_STATE

	POWERDOWN_STATE - POWERDOWN_STATE	
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x66654321	
Size (in bits):	32	
Address:	0A710h	
Subwell Power down state description.		

DWord	Bit	Description	
0	31:28	**pmcr_powerdown_state8**	
		Default Value:	0110b
		Access:	R/W
		The 8th state/signal that needs to be driven	
	27:24	**pmcr_powerdown_state7**	
		Default Value:	0110b
		Access:	R/W
		The 7th state/signal that needs to be driven	
	23:20	**pmcr_powerdown_state6**	
		Default Value:	0110b
		Access:	R/W
		The 6th state/signal that needs to be driven	
	19:16	**pmcr_powerdown_state5**	
		Default Value:	0101b
		Access:	R/W
		The 5th state/signal that needs to be driven	
	15:12	**pmcr_powerdown_state4**	
		Default Value:	0100b
		Access:	R/W
		The 4th state/signal that needs to be driven	
	11:8	**pmcr_powerdown_state3**	
		Default Value:	0011b
		Access:	R/W

POWERDOWN_STATE - POWERDOWN_STATE

		The 3rd state/signal that needs to be driven	
	7:4	**pmcr_powerdown_state2**	
		Default Value:	0010b
		Access:	R/W
		The 2nd state/signal that needs to be driven	
	3:0	**pmcr_powerdown_state1**	
		Default Value:	0001b
		Access:	R/W
		This is the very first state and the signal that needs to be driven appropriately Encodings: 001 = Reset Sync Reset 010 = Reset Firewall 011 = Set Power EnB 100 = Reset Clock En 101 = Reset Async Reset 110 = Done 111 = Reserved. Open: Do we want to have an extra bit for future support	

POWERDOWN_WAIT1

POWERDOWN_WAIT1 - POWERDOWN_WAIT1

Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x01010101
Size (in bits):	32

Address:	0A714h

Subwell power down state wait time 1.

DWord	Bit	Description
0	31:24	**pmcr_powerdown_wait_state4_5**
		Default Value: 01h
		Access: R/W
		This is the programmed value as to how long there is a wait from the time signal 4 is driven before signal 5 can be driven
	23:16	**pmcr_powerdown_wait_state3_4**
		Default Value: 01h
		Access: R/W
		This is the programmed value as to how long there is a wait from the time signal 3 is driven before signal 4 can be driven
	15:8	**pmcr_powerdown_wait_state2_3**
		Default Value: 01h
		Access: R/W
		This is the programmed value as to how long there is a wait from the time signal 2 is driven before signal 3 can be driven
	7:0	**pmcr_powerdown_wait_state1_2**
		Default Value: 01h
		Access: R/W
		This is the programmed value as to how long there is a wait from the time signal 1 is driven before signal 2 can be driven. Note: The granularity of these are in 30ns intervals meaning the counters will increment/decrement every 30ns pulse

POWERDOWN_WAIT2

POWERDOWN_WAIT2 - POWERDOWN_WAIT2	

Register Space: MMIO: 0/2/0

Project: CHV, BSW

Source: PRM

Default Value: 0x01010101

Size (in bits): 32

Address: 0A718h

Subwell power down state wait time 2.

DWord	Bit	Description
0	31:24	**pmcr_powerdown_interval**
		Default Value: 01h
		Access: R/W
		Stagger between different power gate enables for power down.
	23:16	**pmcr_powerdown_wait_state7_8**
		Default Value: 01h
		Access: R/W
		This is the programmed value as to how long there is a wait from the time signal 7 is driven before signal 8 can be driven
	15:8	**pmcr_powerdown_wait_state6_7**
		Default Value: 01h
		Access: R/W
		This is the programmed value as to how long there is a wait from the time signal 6 is driven before signal 7 can be driven
	7:0	**pmcr_powerdown_wait_state5_6**
		Default Value: 01h
		Access: R/W
		This is the programmed value as to how long there is a wait from the time signal 5 is driven before signal 6 can be driven

Power Down/Up Control

PWRDWNUPCTL - Power Down/Up Control		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A294h-0A297h	

DWord	Bit	Description
0	31:4	**Reserved** Access: RO
	3	**Block Signaling Policy** Access: R/W BlockAll signaling policy register. Applies to signaling sent to Wake FIFO (ie. IA GT FIFO and HW FIFO). 0 (default) : BlockALL signal only asserts for CPD. 1 : BlockALL signal can assert for CPD and for a timeperiod during RC6 entry. Note : This affects MMIO requests crossing from CZ clock domain to message channel in Gfx clock domain.
	2	**Serialize Power Requests** Access: R/W Determines whether simultaneous requests to REMOVE power are presented to the Punit at the same time or whether the handshake for one must complete before the handshake for the other may start. 0=simultaneous 1=serial
	1	**Powerdown Request Order** Access: R/W Determines which well is disabled first if both wells are requesting to enter standby simultaneously, if serialized. 0=render well power is removed first 1=media well power is removed first.
	0	**Wake Media First** Access: R/W When waking both wells, it determines which well wakes first. 0=wake render first 1=wake media first. (It is NOT possible to wake both simultaneously for di/dt reasons)

Power Enable stagger control

PWRENSTAGCNTRL - Power Enable stagger control		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000001	
Size (in bits):	32	
Address:	0A70Ch	
Power Enable Stagger Control		
DWord	**Bit**	**Description**
0	31:8	**Reserved**
		Access: RO
	7:0	**pgen_phase_interval**
		Default Value: 01h
		Access: R/W
		It is the separation between pgen0 and pgen1 on SSx. (units = 30ns) Default value 0x01. (Real silicon settings will be determined by circuit simulation, but expect it to be no higher than 0x21. Nominally, expect it to be 0x0A)

Power Meter Weight for gti_idle_cz

PMWGICZ - Power Meter Weight for gti_idle_cz	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	1300A4h

This register contains the power meter weight for the idleness in CZ clock domain.

DWord	Bit	Description	
0	31:16	**RESERVED**	
		Default Value:	0000h
		Access:	RO
		Reserved	
	15:0	**PMWGICZ**	
		Default Value:	0000h
		Access:	R/W
		This 16-bit value is used to indicate how often to accumulate power within the CZ clock domain. When this field is set to zero, CZ clock domain will not contribute to the overall energy count. Otherwise, the value in this register will dictate how often to add CZ power contribution.	

Power Meter Weight for gti_idle_gs

PWRMTR_WT_GTI - Power Meter Weight for gti_idle_gs		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0AABCh	
DWord	**Bit**	**Description**
0	31:16	**Reserved**
		Access: _____ RO
	15:0	**Power Meter Weight GTI**
		Access: _____ R/W
		Power meter weight for gti_idle_gs.

Power Meter Weight for media/render

PWRMTR_WT_MEDREN - Power Meter Weight for media/render	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0AAB8h

DWord	Bit	Description
0	31:16	**Power Meter Weight Render** Access: R/W Power meter weight for render_idle.
	15:0	**Power Meter Weight Media** Access: R/W Power meter event weight media_idle.

POWERUP_STATE

POWERUP_STATE - POWERUP_STATE		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x76543210	
Size (in bits):	32	
Address:	0A700h	
Subwell Power up state description.		

DWord	Bit	Description	
0	31:28	**pmcr_powerup_state8**	
		Default Value:	0111b
		Access:	R/W
		The 8th state/signal that needs to be driven	
	27:24	**pmcr_powerup_state7**	
		Default Value:	0110b
		Access:	R/W
		The 7th state/signal that needs to be driven	
	23:20	**pmcr_powerup_state6**	
		Default Value:	0101b
		Access:	R/W
		The 6th state/signal that needs to be driven	
	19:16	**pmcr_powerup_state5**	
		Default Value:	0100b
		Access:	R/W
		The 5th state/signal that needs to be driven	
	15:12	**pmcr_powerup_state4**	
		Default Value:	0011b
		Access:	R/W
		The 4th state/signal that needs to be driven	
	11:8	**pmcr_powerup_state3**	
		Default Value:	0010b
		Access:	R/W

POWERUP_STATE - POWERUP_STATE

		The 3rd state/signal that needs to be driven
	7:4	**pmcr_powerup_state2**
		Default Value: | 0001b
		Access: | R/W
		The 2nd state/signal that needs to be driven
	3:0	**pmcr_powerup_state1**
		Default Value: | 0000b
		Access: | R/W

This is the very first state and the signal that needs to be driven appropriately

Encodings:

0000 = First Set Clock En

0001 = Reset Power EnB

0010 = Reset Clock En

0011 = Set Firewall

0100 = Set Async Reset/ Set Pwrok

0101 = Final Set clock en

0110 = Set Sync Reset.

0111 = Done

1xxx = Reserved for future

POWERUP_WAIT1

POWERUP_WAIT1 - POWERUP_WAIT1		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x01010101	
Size (in bits):	32	
Address:	0A704h	
Subwell power up state wait time 1		

DWord	Bit	Description
0	31:24	**pmcr_powerup_wait_state4_5**
		<table><tr><td>Default Value:</td><td>01h</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> This is the programmed value as to how long there is a wait from the time signal 4 is driven before signal 5 can be driven
	23:16	**pmcr_powerup_wait_state3_4**
		<table><tr><td>Default Value:</td><td>01h</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> This is the programmed value as to how long there is a wait from the time signal 3 is driven before signal 4 can be driven
	15:8	**pmcr_powerup_wait_state2_3**
		<table><tr><td>Default Value:</td><td>01h</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> This is the programmed value as to how long there is a wait from the time signal 2 is driven before signal 3 can be driven
	7:0	**pmcr_powerup_wait_state1_2**
		<table><tr><td>Default Value:</td><td>01h</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> This is the programmed value as to how long there is a wait from the time signal 1 is driven before signal 2 can be driven. Note: The granularity of these are in 30ns intervals meaning the counters will increment or decrement every 30ns pulse unless we are asserting clocken in which case it is on a usync boundary

POWERUP_WAIT2

POWERUP_WAIT2 - POWERUP_WAIT2		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x01010101	
Size (in bits):	32	
Address:	0A708h	
Subwell power up state wait time 2.		
DWord	**Bit**	**Description**
0	31:24	**pmcr_powerup_interval**
		Default Value: / 01h
		Access: / R/W
		Stagger between different power gate enables on power up
	23:16	**pmcr_powerup_wait_state7_8**
		Default Value: / 01h
		Access: / R/W
		This is the programmed value as to how long there is a wait from the time signal 7 is driven before signal 8 can be driven
	15:8	**pmcr_powerup_wait_state6_7**
		Default Value: / 01h
		Access: / R/W
		This is the programmed value as to how long there is a wait from the time signal 6 is driven before signal 7 can be driven
	7:0	**pmcr_powerup_wait_state5_6**
		Default Value: / 01h
		Access: / R/W
		This is the programmed value as to how long there is a wait from the time signal 5 is driven before signal 6 can be driven

PPGTT Page Fault Data Registers

PP_PFD[0:31] - PPGTT Page Fault Data Registers	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	04580h

The GTT Page Fault Log entries can be read from these registers.
4580h-4583h: Fault Entry 0
…
45FCh-45FFh: Fault Entry 31

DWord	Bit	Description
0	31:12	**Fault Entry Page Address**
		Format: GraphicsAddress[31:12]
		This RO field contains the faulting page address for this Fault Log entry. This field will contain a valid fault address only if the bit in the GTT Page Fault Indication Register corresponding with the address offset of this entry is set.
	11:0	**Reserved**
		Format: MBZ

Predicate Rendering Data Result

	MI_PREDICATE_RESULT - Predicate Rendering Data Result		
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	RenderCS		
Default Value:	0x00000000		
Access:	R/W		
Size (in bits):	32		
Address:	02418h		
Valid Projects:			

DWord	Bit	Description	
0	31:1	**Reserved**	
		Format:	MBZ
	0	**MI_PREDICATE_RESULT** This bit is the result of the last MI_PREDICATE.	

Predicate Rendering Data Result 1

MI_PREDICATE_RESULT_1 - Predicate Rendering Data Result 1	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	0241Ch-0241Fh
Name:	Predicate Rendering Data Result 1
ShortName:	MI_PREDICATE_RESULT_1_RCSUNIT
Address:	1241Ch-1241Fh
Name:	Predicate Rendering Data Result 1
ShortName:	MI_PREDICATE_RESULT_1_VCSUNIT0
Address:	1A41Ch-1A41Fh
Name:	Predicate Rendering Data Result 1
ShortName:	MI_PREDICATE_RESULT_1_VECSUNIT
Address:	1C41Ch-1C41Fh
Name:	Predicate Rendering Data Result 1
ShortName:	MI_PREDICATE_RESULT_1_VCSUNIT1
Address:	2241Ch-2241Fh
Name:	Predicate Rendering Data Result 1
ShortName:	MI_PREDICATE_RESULT_1_BCSUNIT

DWord	Bit	Description	
0	31:1	**Reserved**	
		Format:	MBZ
	0	**MI_PREDICATE_RESULT_1** This bit is used to predicate MI_BATCH_BUFFER_START commands in the RCS command stream. Usage Model: MI_MATH command will be used to do some ALU operations over GPR followed by a MI_LOAD_REGISTER_REGISTER to move the result from GPR to MI_PREDICATE_RESULT_1.	

Predicate Rendering Data Result 2

MI_PREDICATE_RESULT_2 - Predicate Rendering Data Result 2	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	023BCh-023BFh
Name:	Predicate Rendering Data Result 2
ShortName:	MI_PREDICATE_RESULT_2_RCSUNIT
Valid Projects:	CHV, BSW
Address:	123BCh-123BFh
Name:	Predicate Rendering Data Result 2
ShortName:	MI_PREDICATE_RESULT_2_VCSUNIT0
Valid Projects:	CHV, BSW
Address:	1A3BCh-1A3BFh
Name:	Predicate Rendering Data Result 2
ShortName:	MI_PREDICATE_RESULT_2_VECSUNIT
Valid Projects:	CHV, BSW
Address:	1C3BCh-1C3BFh
Name:	Predicate Rendering Data Result 2
ShortName:	MI_PREDICATE_RESULT_2_VCSUNIT1
Valid Projects:	CHV, BSW
Address:	223BCh-223BFh
Name:	Predicate Rendering Data Result 2
ShortName:	MI_PREDICATE_RESULT_2_BCSUNIT

DWord	Bit	Description
0	31:1	**Reserved**
		Format: MBZ
	0	**MI_PREDICATE_RESULT_2**
		This bit must be loaded with by SW based on GT mode of operation. This register must be loaded appropriately before using MI_SET_PREDICATE command.

Value	Name	Description
0h	**[Default]**	Indicates GT2 mode and lower slice is disabled.
1h		Indicates GT3 mode and lower slice is enabled.

Predicate Rendering Data Storage

MI_PREDICATE_DATA - Predicate Rendering Data Storage	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Address:	02410h-02417h
Valid Projects:	

DWord	Bit	Description
0	63:32	**MI_PREDICATE_DATA_UDW** This register is used either as computed value based off the MI_PREDICATE_SRC0 and MI_PREDICATE_SRC1 or a temporary register. See Predicate Rendering section for more details.
	31:0	**MI_PREDICATE_DATA_LDW** This register is used either as computed value based off the MI_PREDICATE_SRC0 and MI_PREDICATE_SRC1 or a temporary register. See Predicate Rendering section for more details.

Predicate Rendering Temporary Register0

MI_PREDICATE_SRC0 - Predicate Rendering Temporary Register0	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Address:	02400h-02407h
Valid Projects:	

DWord	Bit	Description
0	63:0	**MI_PREDICATE_SRC0** This register is a temporary register for Predicate Rendering. See Predicate Rendering section for more details.

Predicate Rendering Temporary Register1

MI_PREDICATE_SRC1 - Predicate Rendering Temporary Register1	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Address:	02408h-0240Fh
Valid Projects:	CHV, BSW

DWord	Bit	Description
0	63:0	**MI_PREDICATE_SRC1** This register is a temporary register for Predicate Rendering. See Predicate Rendering section for more details.

Previous Idle/Busy/Avg Count for Freq Down Recommendation

RPPREVDN - Previous Idle/Busy/Avg Count for Freq Down Recommendation		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A064h-0A067h	

DWord	Bit	Description
0	31:24	**Reserved**
		Access: RO
		Reserved
	23:0	**Previous Busy in Down EI**
		Access: RO
		Previous Busy in Down EI (PRVBSYTAVG): Reports the busyness at the end of the previous down evaluation interval 0 = 0 usec 1 = 1.28 usec 2 = 2.56 usec 3 = 3.84 usec FF FFFF = 21.474 sec pmcr_previous_ei_down_busy[23:0]

Previous Idle/Busy/Avg Count for Freq Up Recommendation

RPPREVUP - Previous Idle/Busy/Avg Count for Freq Up Recommendation		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A058h-0A05Bh	

DWord	Bit	Description
0	31:24	**Reserved** Access: RO Reserved
	23:0	**Previous Busy in UP EI** Access: RO Reports the busyness at the end of the previous Up evaluation interval 0 = 0 usec 1 = 1.28 usec 2 = 2.56 usec 3 = 3.84 usec FF FFFF = 21.474 sec pmcr_previous_ei_up_busy[23:0]

Primitives Generated By VF

IA_PRIMITIVES_COUNT - Primitives Generated By VF	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Trusted Type:	1
Address:	02318h
Valid Projects:	

This register stores the count of primitives generated by VF. This register is part of the context save and restore.

DWord	Bit	Description
0	63:32	**IA Primitives Count Report UDW** Total number of primitives output by the Vertex Fetch (IA) stage. This count is updated for every primitive output by the VF stage, as long as Statistics Enable is set in VF_STATE (see the Vertex Fetch Chapter in the 3D Volume.)
	31:0	**IA Primitives Count Report LDW** Total number of primitives output by the Vertex Fetch (IA) stage. This count is updated for every primitive output by the VF stage, as long as Statistics Enable is set in VF_STATE (see the Vertex Fetch Chapter in the 3D Volume.)

Private PAT

PRIV_PAT - Private PAT		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000003	
Size (in bits):	32	
Address:	040E8h	

DWord	Bit	Description		
0	31:0	**Private PAT**		
		Default Value:		00000003h
		Access:		R/W

Description	Project
Bit[31:8]: Reserved.	
Bit[7]: Reserved. Bit[6]: Snoop Required [CHV, BSW Only] 1: System agent will snoop the IA cores 0: System agent will not snoop the IA cores Bit[5:4]: (See below.) 00b: Age is 0. 01b: Age is 1. 10b: Age is 2. 11b: Age is 3. Bit[3:2]: (See below.) 00b: eLLC only. 01b: LLC only. 10b: LLC and eLLC allowed. 11b: L3, LLC, and eLLC are allowed. Bit[1:0]: (see below): 00b: Uncacheable (UC). 01b: Write Combining (WC). 10b: Write Through (WT). 11b: Write Back (WB).	CHV, BSW

Private PAT

PRIV_PAT - Private PAT		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	040E8h	
DWord	**Bit**	**Description**
0	31:0	**Private PAT**

Default Value:	00000000h
Access:	R/W

Bit[31:16]: Reserved.
Bit[15:8]: PPGTT Private PAT.
(See bit[7:0] for definition.)

Bit[7:6]: Reserved.
Bit[5:4]: (See below.)
00b: Age is 0.
01b: Age is 1.
10b: Age is 2.
11b: Age is 3.
Bit[3:2]: (See below.)
00b: Override to eLLC Only. (This setting overrides the memory_object_control_state via surface state to be eLLC target only.)
01b: eLLC only.
10b: LLC only.
11b: eLLC/LLC.
Bit[1:0]: (see below):
00b: Uncached with fence.
01b: Write Combining (traditional UC).
10b: Write Through.
11b: Write Back.

PS Depth Count

PS_DEPTH_COUNT - PS Depth Count	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Trusted Type:	1
Address:	02350h

This register stores the value of the count of samples that have passed the depth test. This register is part of the context save and restore. Note that the value of this register can be obtained in a pipeline-synchronous fashion without a pipeline flush by using the 3DCONTROL command. See 3D Overview in the 3D volume.

DWord	Bit	Description
0..1	63:32	**Depth Count UDW** This register reflects the total number of samples that have passed the depth test (i.e., will be visible). All samples are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Samples that pass the depth test but fail the stencil test will not be counted.
	31:0	**Depth Count LDW** This register reflects the total number of samples that have passed the depth test (i.e., will be visible). All samples are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Samples that pass the depth test but fail the stencil test will not be counted.

PS Depth Count for Slice0

PS_DEPTH_COUNT_SLICE0 - PS Depth Count for Slice0	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Trusted Type:	1
Address:	022D8h

This register stores the value of the count of pixels that have passed the depth test in Slice0. This register is part of the context save and restore. This register should not be programmed by SW.Note: In GT3 mode there are two slices Slice0 (Upper Slice) and Slice1 (Lower slice).

DWord	Bit	Description
0..1	63:32	**Depth Count UDW** This register reflects the total number of pixels that have passed the depth test in Slice0(i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.
	31:0	**Depth Count LDW** This register reflects the total number of pixels that have passed the depth test in Slice0(i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.

PS Depth Count for Slice1

PS_DEPTH_COUNT_SLICE1 - PS Depth Count for Slice1	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Trusted Type:	1
Address:	022F8h

This register stores the value of the count of pixels that have passed the depth test in Slice1. This register is part of the context save and restore. This register should not be programmed by SW.Note: In GT3 mode there are two slices Slice0 (Upper Slice) and Slice1 (Lower slice).

DWord	Bit	Description
0..1	63:32	**Depth Count UDW** This register reflects the total number of pixels that have passed the depth test in Slice1(i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.
	31:0	**Depth Count LDW** This register reflects the total number of pixels that have passed the depth test in Slice1(i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.

PS Depth Count for Slice2

PS_DEPTH_COUNT_SLICE2 - PS Depth Count for Slice2	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Trusted Type:	1
Address:	02450h

This register stores the value of the count of pixels that have passed the depth test in Slice2. This register is part of the render context save and restore. This register should not be programmed by SW.

DWord	Bit	Description
0..1	63:32	**Depth Count UDW** This register reflects the depth test in slice2 (i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.
	31:0	**Depth Count LDW** This register reflects the depth test in slice2 (i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.

PS Depth Count for Slice3

PS_DEPTH_COUNT_SLICE3 - PS Depth Count for Slice3	

Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Trusted Type:	1

Address:	02460h

This register stores the value of the count of pixels that have passed the depth test in Slice3. This register is part of the render context save and restore. This register should not be programmed by SW.

DWord	Bit	Description
0..1	63:32	**Depth Count UDW** This register reflects the depth test in slice3 (i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.
	31:0	**Depth Count LDW** This register reflects the depth test in slice3 (i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.

PS Invocation Count

PS_INVOCATION_COUNT - PS Invocation Count		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000, 0x00000000	
Access:	R/W	
Size (in bits):	64	
Trusted Type:	1	
Address:	02348h	
DWord	**Bit**	**Description**
0..1	63:32	**PS Invocation Count UDW** Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.
	31:0	**PS Invocation Count LDW** Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.

PS Invocation Count for Slice0

PS_INVOCATION_COUNT_SLICE0 - PS Invocation Count for Slice0	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Trusted Type:	1
Address:	022C8h

This register stores the value of the count of pixels that get shaded in Slice0. This register is part of the context save and restore. This register should not be programmed by SW.Note: In GT3 mode there are two slices Slice0 (Upper Slice) and Slice1 (Lower slice).

Workaround
HW reports this count 4X the actual value and therefore SW must divide the count by 4 for correct reporting.

DWord	Bit	Description
0..1	63:32	**PS Invocation Count UDW** Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice0. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.
	31:0	**PS Invocation Count LDW** Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice0. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.

PS Invocation Count for Slice1

PS_INVOCATION_COUNT_SLICE1 - PS Invocation Count for Slice1	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Trusted Type:	1
Address:	022F0h

This register stores the value of the count of pixels that get shaded in Slice0. This register is part of the context save and restore. This register should not be programmed by SW.Note: In GT3 mode there are two slices Slice0 (Upper Slice) and Slice1 (Lower slice).

Workaround
Workaround: HW reports this count 4X the actual value and therefore SW must divide the count by 4 for correct reporting.

DWord	Bit	Description
0..1	63:32	**PS Invocation Count UDW** Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice1. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.
	31:0	**PS Invocation Count LDW** Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice1. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.

PS Invocation Count for Slice2

PS_INVOCATION_COUNT_SLICE2 - PS Invocation Count for Slice2	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Trusted Type:	1
Address:	02448h

This register stores the value of the count of pixels that get shaded in Slice2. This register is part of the render context save and restore. This register should not be programmed by SW.

DWord	Bit	Description
0..1	63:32	**PS Invocation Count UDW** Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice2. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.
	31:0	**PS Invocation Count LDW** Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice2. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.

PS Invocation Count for Slice3

PS_INVOCATION_COUNT_SLICE3 - PS Invocation Count for Slice3	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Trusted Type:	1
Address:	02458h

This register stores the value of the count of pixels that get shaded in Slice3. This register is part of the render context save and restore. This register should not be programmed by SW.

DWord	Bit	Description
0..1	63:32	**PS Invocation Count UDW** Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice3. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.
	31:0	**PS Invocation Count LDW** Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice3. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.

PTBR_PAGE_POOL_OOM_EVENT_REGISTER

PTBR_PAGE_POOL_OOM_EVENT_REGISTER	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PositionCS
Default Value:	0x00000000
Size (in bits):	32
Address:	1A5A4h
Name:	Register Template Address
ShortName:	ADDR_SHORT_NAME

Indicates the number of times the POSH pipe has encountered Out of Memory at any given point of time.. This register is engine context save/restored.

DWord	Bit	Description	
0	31:17	**Reserved**	
		Default Value:	000000000000000b
		Access:	RO

PTBR Page Pool Size on Out Of Memory

PTBR_PAGE_POOL_SIZE_ON_OOM_REGISTER	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PositionCS
Default Value:	0x00000000
Size (in bits):	32
Address:	18594h
Name:	Register Template Address
ShortName:	PTBR_PAGE_POOL_SIZE_ON_OOM_REGISTER

Indicates the PTBR_PAGE_POOL_SIZE when POSH pipe has encountered out of memory. This register is engine context save/restored.

DWord	Bit	Description	
0	31:17	**Reserved**	
		Default Value:	000000000000000b
		Access:	RO

PTE SW Fault Repair High

PTESWC_H - PTE SW Fault Repair High		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04104h	

DWord	Bit	Description
0	31:0	**PTE SW Fault Repair High**
		Default Value: ⁣ 00000000h
		Access: ⁣ R/W
		Fixed PTE entry is written by SW here.

PTE SW Fault Repair Low

<table>
<tr><td colspan="3" align="center">**PTESWC_L - PTE SW Fault Repair Low**</td></tr>
<tr><td>Register Space:</td><td colspan="2">MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td colspan="2">CHV, BSW</td></tr>
<tr><td>Source:</td><td colspan="2">PRM</td></tr>
<tr><td>Default Value:</td><td colspan="2">0x00000000</td></tr>
<tr><td>Size (in bits):</td><td colspan="2">32</td></tr>
<tr><td>Address:</td><td colspan="2">04100h</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td>**Description**</td></tr>
<tr><td>0</td><td>31:0</td><td>**PTE SW Fault Repair Low**

Default Value: 00000000h
Access: R/W

Fixed PTE entry is written by SW here.</td></tr>
</table>

Punit to Gunit Message

P2GMESSAGE - Punit to Gunit Message	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	1300A8h

This register is used for messaging communication between Punit and Gunit.

DWord	Bit	Description
0	31:16	**P2GMSGMSK**
		<table><tr><td>Default Value:</td><td>0000h</td></tr><tr><td>Access:</td><td>RO</td></tr></table> Mask bits for lower 16 bits to avoid a read/modify write if '0' the corresponding bit in [15:0] is not changed if '1' the corresponding bit in [15:0] is changed to the value in [15:0]
	15	**Punit to Gunit Ack for (EU/SS) resource profile change**
		<table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>WO</td></tr></table> New for CHV, BSW. Punit sends an ack to proceed with changing the EU/SS requested by CS. This is self clearing bit. Both this bit and bit 31 should be '1 and byte enables should be set for writing into this bit. Once written, ack will stay high for one czclk wide and self clears. Reads will always return '0. Other bits that are involved in the flow are A11C[28] and A11C[27].Sequencing. 1) CS sends (EU/SS) resource request to GPM. 2) GPM writes to offset 0xDA in Punit config space showing what the intended new configuration will be, when config bit allows. 3) Punit has opportunity to do whatever is needed, but can not wait for CPDack as it will result in a hang. 4) Based on a config unit setting, GPM will wait for an acknowledge from Punit. By default, GPM does not wait for ack due to large latency. 5) GPM continues to change the (EU/SS) resource profile. 6) GPM replies to CS with the new resource profile. 7) Execute the workload or arbitrate CPD.
	14:1	**P2G_MSG_RSVD**
		<table><tr><td>Default Value:</td><td>0000h</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> P2GMSGReserved

P2GMESSAGE - Punit to Gunit Message

0	**P2GMSG0**	
	Default Value:	0b
	Access:	R/W

Context restore. this bit is used as part of the hardware context restore process.

Step1: Punit writes '1(with mask bit 16 set) to initiate the HW context restore(for registers driver would normally restore)

Step2: Gunit goes through context restore.

Step3: Gunit writes a 1 to Punit register DB[0] indicating context restore has completed.

This bit is cleared automatically when Gunit is powered down. Punit must do the same.

The specific usage of this bit limits it to only be set once, for initial context restore request after an s0ix exit. Any subsequent write is undefined.

PWRCTXSAVE Message Register for Power Managment Unit

MSG_PWRCTXSAVE_GPM - PWRCTXSAVE Message Register for Power Managment Unit	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	16
Address:	08044h

Message registers have bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16]. In order to set bit0, for example, the data would be 0x0001_0001. In order to clear bit0, for example, the data would be 0x0001_0000. Note that mask bit is the data bit offset + 16. Message registers are protected from non-GT writes via the Message Channel.

DWord	Bit	Description	
0	15:10	**Reserved**	
		Access:	RO
	9	**Power Context Save Request**	
		Access:	R/W
		Power Context Save Request 1'b0 : Power context save is not being requested <default> 1'b1 : Power context save is being requested Unit needs to self-clear this bit upon sampling.	
	8:0	**QWord Credits for Power Context Save Request**	
		Access:	R/W
		QWord Credits for Power Context Save Request Minimum Credits = 1 : Unit may send 1 QWord pair (enough for first LRI at least) Maximum Credits = 511 : Unit may send 511 QWord pairs A QWord pair is defined as a 32-bit register address and the corresponding 32-bits of register data. Note that the LRI header and END commands are 64-bits each (32-bit command followed by 32-bit NOOP) and will consume one QWord credit. Only valid with PWRCTXSAVE_REQ (Bit9).	

PWRMTR_WT1_EEVT1TO4

PWRMTR_WT1_EEVT1TO4 - PWRMTR_WT1_EEVT1TO4	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0A850h

PWRMTR_WT1_EEVT1to4

DWord	Bit	Description	
0	31:24	**PWRMTR_WT1_EU_TH_EVT4**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_EU_TH_EVT4 This event measured by this field can be overwritten by AACC[3].	
	23:16	**PWRMTR_WT1_EU_GA_EVT3**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_EU_GA_EVT3 This event measured by this field can be overwritten by AACC[2].	
	15:8	**PWRMTR_WT1_EU_GA_EVT2**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_EU_GA_EVT2 This event measured by this field can be overwritten by AACC[1].	
	7:0	**PWRMTR_WT1_EU_GA_EVT1**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_EU_GA_EVT1 This event measured by this field can be overwritten by AACC[0].	

PWRMTR_WT1_EEVT5TO8

PWRMTR_WT1_EEVT5TO8 - PWRMTR_WT1_EEVT5TO8	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0A854h

PWRMTR_WT1_EEVT5to8

DWord	Bit	Description
0	31:24	**PWRMTR_WT1_E0_HP_EVT8**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_E0_HP_EVT8 This event measured by this field can be overwritten by AACC[7].
	23:16	**PWRMTR_WT1_E0_HP_EVT7**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_E0_HP_EVT7 This event measured by this field can be overwritten by AACC[6].
	15:8	**PWRMTR_WT1_E0_HP_EVT6**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_E0_HP_EVT6 This event measured by this field can be overwritten by AACC[5].
	7:0	**PWRMTR_WT1_EU_IO_EVT5**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_EU_IO_EVT5 This event measured by this field can be overwritten by AACC[4].

PWRMTR_WT1_EEVT9TO12

PWRMTR_WT1_EEVT9TO12 - PWRMTR_WT1_EEVT9TO12		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A858h	
PWRMTR_WT1_EEVT9to12		

DWord	Bit	Description
0	31:24	**PWRMTR_WT1_E0_SP_EVT12**
		<table><tr><td>Default Value:</td><td>00h</td></tr><tr><td>Access:</td><td>R/W Lock</td></tr></table> PWRMTR_WT1_E0_SP_EVT12 This event measured by this field can be overwritten by AACC[11].
	23:16	**PWRMTR_WT1_E0_SP_EVT11**
		<table><tr><td>Default Value:</td><td>00h</td></tr><tr><td>Access:</td><td>R/W Lock</td></tr></table> PWRMTR_WT1_E0_SP_EVT11 This event measured by this field can be overwritten by AACC[10].
	15:8	**PWRMTR_WT1_E0_SP_EVT10**
		<table><tr><td>Default Value:</td><td>00h</td></tr><tr><td>Access:</td><td>R/W Lock</td></tr></table> PWRMTR_WT1_E0_SP_EVT10 This event measured by this field can be overwritten by AACC[9].
	7:0	**PWRMTR_WT1_E0_HP_EVT9**
		<table><tr><td>Default Value:</td><td>00h</td></tr><tr><td>Access:</td><td>R/W Lock</td></tr></table> PWRMTR_WT1_E0_HP_EVT9 This event measured by this field can be overwritten by AACC[8].

PWRMTR_WT1_EEVT13TO16

| PWRMTR_WT1_EEVT13TO16 - PWRMTR_WT1_EEVT13TO16 |

PWRMTR_WT1_EEVT13TO16 - PWRMTR_WT1_EEVT13TO16

Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0A85Ch

PWRMTR_WT1_EEVT13to16

DWord	Bit	Description
0	31:24	**PWRMTR_WT1_E0_DP_EVT16**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_E0_DP_EVT16 This event measured by this field can be overwritten by AACC[15].
		Programming Notes
		Must be 0 at all times.
	23:16	**PWRMTR_WT1_E0_DP_EVT15**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_E0_DP_EVT15 This event measured by this field can be overwritten by AACC[14].
		Programming Notes
		Must be 0 at all times.
	15:8	**PWRMTR_WT1_E0_DP_EVT14**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_E0_DP_EVT14 This event measured by this field can be overwritten by AACC[13].
		Programming Notes
		Must be 0 at all times.
	7:0	**PWRMTR_WT1_E0_SP_EVT13**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_E0_SP_EVT13 This event measured by this field can be overwritten by AACC[12].

PWRMTR_WT1_EEVT17TO20

PWRMTR_WT1_EEVT17TO20 - PWRMTR_WT1_EEVT17TO20		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A860h	
PWRMTR_WT1_EEVT17to20		

DWord	Bit	Description
0	31:24	**PWRMTR_WT1_E0INT_EVT20**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_E0INT_EVT20 This event measured by this field can be overwritten by AACC[19].
	23:16	**PWRMTR_WT1_E0INT_EVT19**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_E0INT_EVT19 This event measured by this field can be overwritten by AACC[18].
		Programming Notes
		Must be 0 at all times.
	15:8	**PWRMTR_WT1_E0INT_EVT18**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_E0INT_EVT18 This event measured by this field can be overwritten by AACC[17].
	7:0	**PWRMTR_WT1_E0_DP_EVT17**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_E0_DP_EVT17 This event measured by this field can be overwritten by AACC[16].
		Programming Notes
		Must be 0 at all times.

PWRMTR_WT1_EEVT21TO24

PWRMTR_WT1_EEVT21TO24 - PWRMTR_WT1_EEVT21TO24		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A864h	
PWRMTR_WT1_EEVT21to24		

DWord	Bit	Description
0	31:24	**PWRMTR_WT1_E0_QP_EVT24**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_E0_QP_EVT24 This event measured by this field can be overwritten by AACC[23].
		Programming Notes
		Must be 0 at all times.
	23:16	**PWRMTR_WT1_E0_QP_EVT23**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_E0_QP_EVT23 This event measured by this field can be overwritten by AACC[22].
		Programming Notes
		Must be 0 at all times.
	15:8	**PWRMTR_WT1_E0_QP_EVT22**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_E0_QP_EVT22 This event measured by this field can be overwritten by AACC[21].
	7:0	**PWRMTR_WT1_E0INT_EVT21**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_E0INT_EVT21 This event measured by this field can be overwritten by AACC[20].

PWRMTR_WT1_EEVT25TO28

PWRMTR_WT1_EEVT25TO28 - PWRMTR_WT1_EEVT25TO28		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A868h	

PWRMTR_WT1_EEVT25to28

DWord	Bit	Description
0	31:24	**PWRMTR_WT1_EFPU0_EVT28**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_EFPU0_EVT28 This event measured by this field can be overwritten by AACC[27].
	23:16	**PWRMTR_WT1_EFPU0_EVT27**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_EFPU0_EVT27 This event measured by this field can be overwritten by AACC[26].
	15:8	**PWRMTR_WT1_EFPU0_EVT26**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_EFPU0_EVT26 This event measured by this field can be overwritten by AACC[25].
	7:0	**PWRMTR_WT1_E0_QP_EVT25**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_E0_QP_EVT25 This event measured by this field can be overwritten by AACC[24].
		Programming Notes
		Must be 0 at all times.

PWRMTR_WT1_EEVT29TO32

PWRMTR_WT1_EEVT29TO32 - PWRMTR_WT1_EEVT29TO32		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A86Ch	
PWRMTR_WT1_EEVT29to32		

DWord	Bit	Description	
0	31:24	**PWRMTR_WT1_E1_HP_EVT32**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_E1_HP_EVT32 This event measured by this field can be overwritten by AACC[31].	
	23:16	**PWRMTR_WT1_E1_HP_EVT31**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_E1_HP_EVT31 This event measured by this field can be overwritten by AACC[30].	
	15:8	**PWRMTR_WT1_E1_HP_EVT30**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_E1_HP_EVT30 This event measured by this field can be overwritten by AACC[29].	
	7:0	**PWRMTR_WT1_EFPU0_EVT29**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_EFPU0_EVT29 This event measured by this field can be overwritten by AACC[28].	

PWRMTR_WT1_EEVT33TO36

PWRMTR_WT1_EEVT33TO36 - PWRMTR_WT1_EEVT33TO36		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A870h	

PWRMTR_WT1_EEVT33to36

DWord	Bit	Description	
0	31:24	**PWRMTR_WT1_E1_SP_EVT36**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_E1_SP_EVT36 This event measured by this field can be overwritten by AAD0[3].	
	23:16	**PWRMTR_WT1_E1_SP_EVT35**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_E1_SP_EVT35 This event measured by this field can be overwritten by AAD0[2].	
	15:8	**PWRMTR_WT1_E1_SP_EVT34**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_E1_SP_EVT34 This event measured by this field can be overwritten by AAD0[1].	
	7:0	**PWRMTR_WT1_E1_HP_EVT33**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_E1_HP_EVT33 This event measured by this field can be overwritten by AAD0[0].	

PWRMTR_WT1_EEVT37TO40

PWRMTR_WT1_EEVT37TO40 - PWRMTR_WT1_EEVT37TO40		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A874h	
PWRMTR_WT1_EEVT37to40		

DWord	Bit	Description
0	31:24	**PWRMTR_WT1_E1_DP_EVT40**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_E1_DP_EVT40 This event measured by this field can be overwritten by AAD0[7].
	23:16	**PWRMTR_WT1_E1_DP_EVT39**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_E1_DP_EVT39 This event measured by this field can be overwritten by AAD0[6].
	15:8	**PWRMTR_WT1_E1_DP_EVT38**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_E1_DP_EVT38 This event measured by this field can be overwritten by AAD0[5].
	7:0	**PWRMTR_WT1_E1_SP_EVT37**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_E1_SP_EVT37 This event measured by this field can be overwritten by AAD0[4].

PWRMTR_WT1_EEVT41TO44

PWRMTR_WT1_EEVT41TO44 - PWRMTR_WT1_EEVT41TO44	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0A878h

PWRMTR_WT1_EEVT41to44

DWord	Bit	Description
0	31:24	**PWRMTR_WT1_E1INT_EVT44**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_E1INT_EVT44 This event measured by this field can be overwritten by AAD0[11].
	23:16	**PWRMTR_WT1_E1INT_EVT43**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_E1INT_EVT43 This event measured by this field can be overwritten by AAD0[10].
		Programming Notes
		Must be 0 at all times.
	15:8	**PWRMTR_WT1_E1INT_EVT42**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_E1INT_EVT42 This event measured by this field can be overwritten by AAD0[9].
	7:0	**PWRMTR_WT1_E1_DP_EVT41**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_E1_DP_EVT41 This event measured by this field can be overwritten by AAD0[8].

PWRMTR_WT1_EEVT45TO48

PWRMTR_WT1_EEVT45TO48 - PWRMTR_WT1_EEVT45TO48		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A87Ch	
PWRMTR_WT1_EEVT45to48		

DWord	Bit	Description
0	31:24	**PWRMTR_WT1_E1_QP_EVT48**
		<table><tr><td>Default Value:</td><td>00h</td></tr><tr><td>Access:</td><td>R/W Lock</td></tr></table> PWRMTR_WT1_E1_QP_EVT48 This event measured by this field can be overwritten by AAD0[15].
	23:16	**PWRMTR_WT1_E1_QP_EVT47**
		<table><tr><td>Default Value:</td><td>00h</td></tr><tr><td>Access:</td><td>R/W Lock</td></tr></table> PWRMTR_WT1_E1_QP_EVT47 This event measured by this field can be overwritten by AAD0[14].
		Programming Notes
		Must be 0 at all times.
	15:8	**PWRMTR_WT1_E1_QP_EVT46**
		<table><tr><td>Default Value:</td><td>00h</td></tr><tr><td>Access:</td><td>R/W Lock</td></tr></table> PWRMTR_WT1_E1_QP_EVT46 This event measured by this field can be overwritten by AAD0[13].
	7:0	**PWRMTR_WT1_E1INT_EVT45**
		<table><tr><td>Default Value:</td><td>00h</td></tr><tr><td>Access:</td><td>R/W Lock</td></tr></table> PWRMTR_WT1_E1INT_EVT45 This event measured by this field can be overwritten by AAD0[12].

PWRMTR_WT1_EEVT49TO52

PWRMTR_WT1_EEVT49TO52 - PWRMTR_WT1_EEVT49TO52		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A880h	

PWRMTR_WT1_EEVT49to52

DWord	Bit	Description
0	31:24	**PWRMTR_WT1_EFPU1_EVT52**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_EFPU1_EVT52 This event measured by this field can be overwritten by AAD0[19].
	23:16	**PWRMTR_WT1_EFPU1_EVT51**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_EFPU1_EVT51 This event measured by this field can be overwritten by AAD0[18].
	15:8	**PWRMTR_WT1_EFPU1_EVT50**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_EFPU1_EVT50 This event measured by this field can be overwritten by AAD0[17].
	7:0	**PWRMTR_WT1_E1_QP_EVT49**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_E1_QP_EVT49 This event measured by this field can be overwritten by AAD0[16].

PWRMTR_WT1_EEVT53TO56

PWRMTR_WT1_EEVT53TO56 - PWRMTR_WT1_EEVT53TO56		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A884h	

PWRMTR_WT1_EEVT53to56

DWord	Bit	Description
0	31:24	**PWRMTR_WT1_EEMEM_EVT56**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_EEMEM_EVT56 This event measured by this field can be overwritten by AAD0[23].
	23:16	**PWRMTR_WT1_EEMEM_EVT55**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_EEMEM_EVT55 This event measured by this field can be overwritten by AAD0[22].
	15:8	**PWRMTR_WT1_EEMEM_EVT54**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_EEMEM_EVT54 This event measured by this field can be overwritten by AAD0[21].
	7:0	**PWRMTR_WT1_EFPU1_EVT53**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_EFPU1_EVT53 This event measured by this field can be overwritten by AAD0[20].

PWRMTR_WT1_EEVT57TO58

PWRMTR_WT1_EEVT57TO58 - PWRMTR_WT1_EEVT57TO58		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A888h	
PWRMTR_WT1_EEVT57to58		

DWord	Bit	Description
0	31:16	**Reserved**
		Default Value: 0000h
		Access: RO
		Reserved
	15:8	**PWRMTR_WT1_EBUSS_EVT58**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_EBUSS_EVT58 This event measured by this field can be overwritten by AAD0[25].
	7:0	**PWRMTR_WT1_EEMEM_EVT57**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_EEMEM_EVT57 This event measured by this field can be overwritten by AAD0[24].

PWRMTR_WT1_MEVT1TO4

		PWRMTR_WT1_MEVT1TO4 - PWRMTR_WT1_MEVT1TO4	

Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32

Address:	0A890h

PWRMTR_WT1_MEVT1to4

DWord	Bit	Description	
0	31:24	**PWRMTR_WT1_MMDOI_EVT4**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_MMDOI_EVT4 This event measured by this field can be overwritten by AAD4[3].	
	23:16	**PWRMTR_WT1_MMSOI_EVT3**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_MMSOI_EVT3 This event measured by this field can be overwritten by AAD4[2].	
	15:8	**PWRMTR_WT1_MMSOI_EVT2**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_MMSOI_EVT2 This event measured by this field can be overwritten by AAD4[1].	
	7:0	**PWRMTR_WT1_MMSOI_EVT1**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_MMSOI_EVT1 This event measured by this field can be overwritten by AAD4[0].	

PWRMTR_WT1_MEVT5TO8

PWRMTR_WT1_MEVT5TO8 - PWRMTR_WT1_MEVT5TO8
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0A894h

PWRMTR_WT1_MEVT5to8

DWord	Bit	Description
0	31:24	**PWRMTR_WT1_MMDOI_EVT8**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_MMDOI_EVT8 This event measured by this field can be overwritten by AAD4[7].
	23:16	**PWRMTR_WT1_MMDOI_EVT7**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_MMDOI_EVT7 This event measured by this field can be overwritten by AAD4[6].
	15:8	**PWRMTR_WT1_MMDOI_EVT6**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_MMDOI_EVT6 This event measured by this field can be overwritten by AAD4[5].
	7:0	**PWRMTR_WT1_MMDOI_EVT5**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_MMDOI_EVT5 This event measured by this field can be overwritten by AAD4[4].

PWRMTR_WT1_MEVT9TO12

PWRMTR_WT1_MEVT9TO12 - PWRMTR_WT1_MEVT9TO12		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A898h	
PWRMTR_WT1_MEVT9to12		

DWord	Bit	Description
0	31:24	**PWRMTR_WT1_MMDCN_EVT12**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_MMDCN_EVT12 This event measured by this field can be overwritten by AAD4[11].
	23:16	**PWRMTR_WT1_MMDCN_EVT11**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_MMDCN_EVT11 This event measured by this field can be overwritten by AAD4[10].
	15:8	**PWRMTR_WT1_MMDCN_EVT10**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_MMDCN_EVT10 This event measured by this field can be overwritten by AAD4[9].
	7:0	**PWRMTR_WT1_MMDCN_EVT9**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_MMDCN_EVT9 This event measured by this field can be overwritten by AAD4[8].

PWRMTR_WT1_MEVT13TO16

PWRMTR_WT1_MEVT13TO16 - PWRMTR_WT1_MEVT13TO16

Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32

Address:	0A89Ch

PWRMTR_WT1_MEVT13to16

DWord	Bit	Description
0	31:24	**PWRMTR_WT1_MMDCN_EVT16**
		<table><tr><td>Default Value:</td><td>00h</td></tr><tr><td>Access:</td><td>R/W Lock</td></tr></table>
		PWRMTR_WT1_MMDCN_EVT16 This event measured by this field can be overwritten by AAD4[15].
	23:16	**PWRMTR_WT1_MMDCN_EVT15**
		<table><tr><td>Default Value:</td><td>00h</td></tr><tr><td>Access:</td><td>R/W Lock</td></tr></table>
		PWRMTR_WT1_MMDCN_EVT15 This event measured by this field can be overwritten by AAD4[14].
	15:8	**PWRMTR_WT1_MMDCN_EVT14**
		<table><tr><td>Default Value:</td><td>00h</td></tr><tr><td>Access:</td><td>R/W Lock</td></tr></table>
		PWRMTR_WT1_MMDCN_EVT14 This event measured by this field can be overwritten by AAD4[13].
	7:0	**PWRMTR_WT1_MMDCN_EVT13**
		<table><tr><td>Default Value:</td><td>00h</td></tr><tr><td>Access:</td><td>R/W Lock</td></tr></table>
		PWRMTR_WT1_MMDCN_EVT13 This event measured by this field can be overwritten by AAD4[12].

PWRMTR_WT1_MEVT17TO20

PWRMTR_WT1_MEVT17TO20 - PWRMTR_WT1_MEVT17TO20	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0A8A0h

PWRMTR_WT1_MEVT17to20

DWord	Bit	Description	
0	31:24	**PWRMTR_WT1_MMDMH_EVT20**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_MMDMH_EVT20 This event measured by this field can be overwritten by AAD4[19].	
	23:16	**PWRMTR_WT1_MMDCN_EVT19**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_MMDCN_EVT19 This event measured by this field can be overwritten by AAD4[18].	
	15:8	**PWRMTR_WT1_MMDCN_EVT18**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_MMDCN_EVT18 This event measured by this field can be overwritten by AAD4[17].	
	7:0	**PWRMTR_WT1_MMDCN_EVT17**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_MMDCN_EVT17 This event measured by this field can be overwritten by AAD4[16].	

PWRMTR_WT1_MEVT21TO24

PWRMTR_WT1_MEVT21TO24 - PWRMTR_WT1_MEVT21TO24		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A8A4h	

PWRMTR_WT1_MEVT21to24

DWord	Bit	Description
0	31:24	**PWRMTR_WT1_MMDOH_EVT24**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_MMDOH_EVT24 This event measured by this field can be overwritten by AAD4[23].
	23:16	**PWRMTR_WT1_MMDMH_EVT23**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_MMDMH_EVT23 This event measured by this field can be overwritten by AAD4[22].
	15:8	**PWRMTR_WT1_MMDMH_EVT22**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_MMDMH_EVT22 This event measured by this field can be overwritten by AAD4[21].
	7:0	**PWRMTR_WT1_MMDMH_EVT21**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_MMDMH_EVT21 This event measured by this field can be overwritten by AAD4[20].

PWRMTR_WT1_MEVT25TO28

PWRMTR_WT1_MEVT25TO28 - PWRMTR_WT1_MEVT25TO28	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0A8A8h

PWRMTR_WT1_MEVT25to28

DWord	Bit	Description
0	31:24	**PWRMTR_WT1_MMDCN_EVT28**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_MMDCN_EVT28 This event measured by this field can be overwritten by AAD4[27].
	23:16	**PWRMTR_WT1_MMDCN_EVT27**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_MMDCN_EVT27 This event measured by this field can be overwritten by AAD4[26].
	15:8	**PWRMTR_WT1_MMDCN_EVT26**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_MMDCN_EVT26 This event measured by this field can be overwritten by AAD4[25].

Programming Notes	Project
Must be 0 at all times.	CHV, BSW

DWord	Bit	Description
	7:0	**PWRMTR_WT1_MMDOH_EVT25**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_MMDOH_EVT25 This event measured by this field can be overwritten by AAD4[24].

PWRMTR_WT1_MEVT29TO32

PWRMTR_WT1_MEVT29TO32 - PWRMTR_WT1_MEVT29TO32		

Register Space: MMIO: 0/2/0

Project: CHV, BSW

Source: PRM

Default Value: 0x00000000

Size (in bits):   32

Address: 0A8ACh

PWRMTR_WT1_MEVT29to32

DWord	Bit	Description
0	31:24	**PWRMTR_WT1_MHECN_EVT32** Default Value: 00h Access: R/W Lock PWRMTR_WT1_MHECN_EVT32 This event measured by this field can be overwritten by AAD4[31].
	23:16	**PWRMTR_WT1_MHECN_EVT31** Default Value: 00h Access: R/W Lock PWRMTR_WT1_MHECN_EVT31 This event measured by this field can be overwritten by AAD4[30].
	15:8	**PWRMTR_WT1_MHECN_EVT30** Default Value: 00h Access: R/W Lock PWRMTR_WT1_MHECN_EVT30 This event measured by this field can be overwritten by AAD4[29].
	7:0	**PWRMTR_WT1_MMDCN_EVT29** Default Value: 00h Access: R/W Lock PWRMTR_WT1_MMDCN_EVT29 This event measured by this field can be overwritten by AAD4[28].

PWRMTR_WT1_MEVT33TO36

		PWRMTR_WT1_MEVT33TO36 - PWRMTR_WT1_MEVT33TO36	
Register Space:		MMIO: 0/2/0	
Project:		CHV, BSW	
Source:		PRM	
Default Value:		0x00000000	
Size (in bits):		32	
Address:		0A8B0h	
PWRMTR_WT1_MEVT33to36			
DWord	**Bit**	**Description**	
0	31:24	**PWRMTR_WT1_MHECN_EVT36**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_MHECN_EVT36 This event measured by this field can be overwritten by AAD8[3].	
	23:16	**PWRMTR_WT1_MHECN_EVT35**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_MHECN_EVT35 This event measured by this field can be overwritten by AAD8[2].	
	15:8	**PWRMTR_WT1_MHECN_EVT34**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_MHECN_EVT34 This event measured by this field can be overwritten by AAD8[1].	
	7:0	**PWRMTR_WT1_MHECN_EVT33**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_MHECN_EVT33 This event measured by this field can be overwritten by AAD8[0].	

PWRMTR_WT1_REVT1TO4

PWRMTR_WT1_REVT1TO4 - PWRMTR_WT1_REVT1TO4	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0A800h

PWRMTR_WT1_REVT1to4

DWord	Bit	Description
0	31:24	**PWRMTR_WT1_RFFOI_EVT4**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_RFFOI_EVT4. This event measured by this field can be overwritten by AAC0[3].
	23:16	**PWRMTR_WT1_RFFOI_EVT3**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_RFFOI_EVT3. This event measured by this field can be overwritten by AAC0[2].
	15:8	**PWRMTR_WT1_RFFOI_EVT2**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_RFFOI_EVT2. This event measured by this field can be overwritten by AAC0[1].
	7:0	**PWRMTR_WT1_RFFOI_EVT1**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_RFFOI_EVT1.This event measured by this field can be overwritten by AAC0[0].

PWRMTR_WT1_REVT5TO8

<table>
<tr><td colspan="3" align="center">**PWRMTR_WT1_REVT5TO8 - PWRMTR_WT1_REVT5TO8**</td></tr>
<tr><td colspan="3">Register Space: MMIO: 0/2/0</td></tr>
<tr><td colspan="3">Project: CHV, BSW</td></tr>
<tr><td colspan="3">Source: PRM</td></tr>
<tr><td colspan="3">Default Value: 0x00000000</td></tr>
<tr><td colspan="3">Size (in bits):   32</td></tr>
<tr><td colspan="3">Address: 0A804h</td></tr>
<tr><td colspan="3">PWRMTR_WT1_REVT5to8</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td>**Description**</td></tr>
<tr><td>0</td><td>31:24</td><td>**PWRMTR_WT1_RFFOI_EVT8**
Default Value: 00h
Access: R/W Lock
PWRMTR_WT1_RFFOI_EVT8. This event measured by this field can be overwritten by AAC0[7].</td></tr>
<tr><td></td><td>23:16</td><td>**PWRMTR_WT1_RFFOI_EVT7**
Default Value: 00h
Access: R/W Lock
PWRMTR_WT1_RFFOI_EVT7. This event measured by this field can be overwritten by AAC0[6].</td></tr>
<tr><td></td><td>15:8</td><td>**PWRMTR_WT1_RFFOI_EVT6**
Default Value: 00h
Access: R/W Lock
PWRMTR_WT1_RFFOI_EVT6.This event measured by this field can be overwritten by AAC0[5].</td></tr>
<tr><td></td><td>7:0</td><td>**PWRMTR_WT1_RFFOI_EVT5**
Default Value: 00h
Access: R/W Lock
PWRMTR_WT1_RFFOI_EVT5.This event measured by this field can be overwritten by AAC0[4].</td></tr>
</table>

PWRMTR_WT1_REVT9TO12

PWRMTR_WT1_REVT9TO12 - PWRMTR_WT1_REVT9TO12	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0A808h

PWRMTR_WT1_REVT9to12

DWord	Bit	Description	
0	31:24	**PWRMTR_WT1_RFFOI_EVT12**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RFFOI_EVT12.This event measured by this field can be overwritten by AAC0[11].	
	23:16	**PWRMTR_WT1_RFFOI_EVT11**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RFFOI_EVT11.This event measured by this field can be overwritten by AAC0[10].	
	15:8	**PWRMTR_WT1_RFFOI_EVT10**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RFFOI_EVT10. This event measured by this field can be overwritten by AAC0[9].	
	7:0	**PWRMTR_WT1_RFFOI_EVT9**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RFFOI_EVT9.This event measured by this field can be overwritten by AAC0[8].	

PWRMTR_WT1_REVT13TO16

PWRMTR_WT1_REVT13TO16 - PWRMTR_WT1_REVT13TO16	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0A80Ch

PWRMTR_WT1_REVT13to16

DWord	Bit	Description
0	31:24	**PWRMTR_WT1_RFFCN_EVT16**

Default Value:	00h
Access:	R/W Lock

PWRMTR_WT1_RFFCN_EVT16.This event measured by this field can be overwritten by AAC0[15].

Programming Notes	Project
Must be 0 at all times.	CHV, BSW

	23:16	**PWRMTR_WT1_RFFCN_EVT15**

Default Value:	00h
Access:	R/W Lock

PWRMTR_WT1_RFFCN_EVT15. This event measured by this field can be overwritten by AAC0[14].

	15:8	**PWRMTR_WT1_RFFOI_EVT14**

Default Value:	00h
Access:	R/W Lock

PWRMTR_WT1_RFFOI_EVT14.This event measured by this field can be overwritten by AAC0[13].

	7:0	**PWRMTR_WT1_RFFOI_EVT13**

Default Value:	00h
Access:	R/W Lock

PWRMTR_WT1_RFFOI_EVT13.This event measured by this field can be overwritten by AAC0[12].

PWRMTR_WT1_REVT17TO20

PWRMTR_WT1_REVT17TO20 - PWRMTR_WT1_REVT17TO20		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A810h	
PWRMTR_WT1_REVT17to20		

DWord	Bit	Description
0	31:24	**PWRMTR_WT1_RFFCN_EVT20**
		<table><tr><td>Default Value:</td><td>00h</td></tr><tr><td>Access:</td><td>R/W Lock</td></tr></table> PWRMTR_WT1_RFFCN_EVT20.ThiseventmeasuredbythisfieldcanbeoverwrittenbyAAC0[19].
	23:16	**PWRMTR_WT1_RFFCN_EVT19**
		<table><tr><td>Default Value:</td><td>00h</td></tr><tr><td>Access:</td><td>R/W Lock</td></tr></table> PWRMTR_WT1_RFFCN_EVT19 ThiseventmeasuredbythisfieldcanbeoverwrittenbyAAC0[18].
	15:8	**PWRMTR_WT1_RFFCN_EVT18**
		<table><tr><td>Default Value:</td><td>00h</td></tr><tr><td>Access:</td><td>R/W Lock</td></tr></table> PWRMTR_WT1_RFFCN_EVT18 This event measured by this field can be overwritten by AAC0[17].
	7:0	**PWRMTR_WT1_RFFCN_EVT17**
		<table><tr><td>Default Value:</td><td>00h</td></tr><tr><td>Access:</td><td>R/W Lock</td></tr></table> PWRMTR_WT1_RFFCN_EVT17 This event measured by this field can be overwritten by AAC0[16]. <table><tr><th>Programming Notes</th><th>Project</th></tr><tr><td>Must be 0 at all times.</td><td>CHV, BSW</td></tr></table>

PWRMTR_WT1_REVT21TO24

**PWRMTR_WT1_REVT21TO24 - PWRMTR_WT1_REVT21TO24**
Register Space:		MMIO: 0/2/0
Project:		CHV, BSW
Source:		PRM
Default Value:		0x00000000
Size (in bits):		32
Address:		0A814h
PWRMTR_WT1_REVT21to24

DWord	Bit	Description
0	31:24	**PWRMTR_WT1_RSCOI_EVT24**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_RSCOI_EVT24 This event measured by this field can be overwritten by AAC0[23].
	23:16	**PWRMTR_WT1_RSCOI_EVT23**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_RSCOI_EVT23 This event measured by this field can be overwritten by AAC0[22].
	15:8	**PWRMTR_WT1_RSCOI_EVT22**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_RSCOI_EVT22 This event measured by this field can be overwritten by AAC0[21].
	7:0	**PWRMTR_WT1_RSCOI_EVT21**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_RSCOI_EVT21 This event measured by this field can be overwritten by AAC0[20].

PWRMTR_WT1_REVT25TO28

PWRMTR_WT1_REVT25TO28 - PWRMTR_WT1_REVT25TO28		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A818h	
PWRMTR_WT1_REVT25to28		

DWord	Bit	Description
0	31:24	**PWRMTR_WT1_RSCOI_EVT28**
		Default Value: · 00h
		Access: · R/W Lock
		PWRMTR_WT1_RSCOI_EVT28 This event measured by this field can be overwritten by AAC0[27].
	23:16	**PWRMTR_WT1_RSCOI_EVT27**
		Default Value: · 00h
		Access: · R/W Lock
		PWRMTR_WT1_RSCOI_EVT27 This event measured by this field can be overwritten by AAC0[26].
	15:8	**PWRMTR_WT1_RSCOI_EVT26**
		Default Value: · 00h
		Access: · R/W Lock
		PWRMTR_WT1_RSCOI_EVT26 This event measured by this field can be overwritten by AAC0[25].
	7:0	**PWRMTR_WT1_RSCOI_EVT25**
		Default Value: · 00h
		Access: · R/W Lock
		PWRMTR_WT1_RSCOI_EVT25 This event measured by this field can be overwritten by AAC0[24].

PWRMTR_WT1_REVT29TO32

PWRMTR_WT1_REVT29TO32 - PWRMTR_WT1_REVT29TO32		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A81Ch	

PWRMTR_WT1_REVT29to32

DWord	Bit	Description	
0	31:24	**PWRMTR_WT1_RSCOI_EVT32**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RSCOI_EVT32 This event measured by this field can be overwritten by AAC0[31].	
	23:16	**PWRMTR_WT1_RSCOI_EVT31**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RSCOI_EVT31 This event measured by this field can be overwritten by AAC0[30].	
	15:8	**PWRMTR_WT1_RSCOI_EVT30**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RSCOI_EVT30 This event measured by this field can be overwritten by AAC0[29].	
	7:0	**PWRMTR_WT1_RSCOI_EVT29**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RSCOI_EVT29 This event measured by this field can be overwritten by AAC0[28].	

PWRMTR_WT1_REVT33TO36

PWRMTR_WT1_REVT33TO36 - PWRMTR_WT1_REVT33TO36		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A820h	

PWRMTR_WT1_REVT33to36

DWord	Bit	Description	
0	31:24	**PWRMTR_WT1_RL3MI_EVT36**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RL3MI_EVT36 This event measured by this field can be overwritten by AAC4[3].	
	23:16	**PWRMTR_WT1_RL3CN_EVT35**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RL3CN_EVT35 This event measured by this field can be overwritten by AAC4[2].	
	15:8	**PWRMTR_WT1_RSCCN_EVT34**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RSCCN_EVT34 This event measured by this field can be overwritten by AAC4[1].	
	7:0	**PWRMTR_WT1_RSCOI_EVT33**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RSCOI_EVT33 This event measured by this field can be overwritten by AAC4[0].	

PWRMTR_WT1_REVT37TO40

PWRMTR_WT1_REVT37TO40 - PWRMTR_WT1_REVT37TO40	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0A824h

PWRMTR_WT1_REVT37to40

DWord	Bit	Description	
0	31:24	**PWRMTR_WT1_RTAOI_EVT40**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RTAOI_EVT40 This event measured by this field can be overwritten by AAC4[7].	
	23:16	**PWRMTR_WT1_RL3MI_EVT39**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RL3MI_EVT39 This event measured by this field can be overwritten by AAC4[6].	
	15:8	**PWRMTR_WT1_RL3MI_EVT38**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RL3MI_EVT38 This event measured by this field can be overwritten by AAC4[5].	
	7:0	**PWRMTR_WT1_RL3MI_EVT37**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RL3MI_EVT37 This event measured by this field can be overwritten by AAC4[4].	

PWRMTR_WT1_REVT41TO44

		PWRMTR_WT1_REVT41TO44 - PWRMTR_WT1_REVT41TO44

Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	

Address:	0A828h

PWRMTR_WT1_REVT41to44

DWord	Bit	Description
0	31:24	**PWRMTR_WT1_RTAOI_EVT44**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_RTAOI_EVT44 This event measured by this field can be overwritten by AAC4[11].
	23:16	**PWRMTR_WT1_RTAOI_EVT43**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_RTAOI_EVT43 This event measured by this field can be overwritten by AAC4[10].
	15:8	**PWRMTR_WT1_RTAOI_EVT42**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_RTAOI_EVT42 This event measured by this field can be overwritten by AAC4[9].
	7:0	**PWRMTR_WT1_RTAOI_EVT41**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_RTAOI_EVT41 This event measured by this field can be overwritten by AAC4[8].

PWRMTR_WT1_REVT45TO48

PWRMTR_WT1_REVT45TO48 - PWRMTR_WT1_REVT45TO48		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A82Ch	
PWRMTR_WT1_REVT45to48		

DWord	Bit	Description
0	31:24	**PWRMTR_WT1_RTAOI_EVT48**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_RTAOI_EVT48 This event measured by this field can be overwritten by AAC4[15].
	23:16	**PWRMTR_WT1_RTAOI_EVT47**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_RTAOI_EVT47 This event measured by this field can be overwritten by AAC4[14].
	15:8	**PWRMTR_WT1_RTAOI_EVT46**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_RTAOI_EVT46 This event measured by this field can be overwritten by AAC4[13].
	7:0	**PWRMTR_WT1_RTAOI_EVT45**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_RTAOI_EVT45 This event measured by this field can be overwritten by AAC4[12].

PWRMTR_WT1_REVT49TO52

PWRMTR_WT1_REVT49TO52 - PWRMTR_WT1_REVT49TO52	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0A830h

PWRMTR_WT1_REVT49to52

DWord	Bit	Description	
0	31:24	**PWRMTR_WT1_RTAOH_EVT52**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RTAOH_EVT52 This event measured by this field can be overwritten by AAC4[19].	
	23:16	**PWRMTR_WT1_RTAOH_EVT51**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RTAOH_EVT51 This event measured by this field can be overwritten by AAC4[18].	
	15:8	**PWRMTR_WT1_RTAOI_EVT50**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RTAOI_EVT50 This event measured by this field can be overwritten by AAC4[17].	
	7:0	**PWRMTR_WT1_RTAOI_EVT49**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RTAOI_EVT49 This event measured by this field can be overwritten by AAC4[16].	

PWRMTR_WT1_REVT53TO56

	PWRMTR_WT1_REVT53TO56 - PWRMTR_WT1_REVT53TO56
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0A834h

PWRMTR_WT1_REVT53to56

DWord	Bit	Description	
0	31:24	**PWRMTR_WT1_RTSOI_EVT56**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RTS OI_EVT56 This event measured by this field can be overwritten by AAC4[23].	
	23:16	**PWRMTR_WT1_RTACN_EVT55**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RTACN_EVT55 This event measured by this field can be overwritten by AAC4[22].	
	15:8	**PWRMTR_WT1_RTACN_EVT54**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RTACN_EVT54 This event measured by this field can be overwritten by AAC4[21].	
	7:0	**PWRMTR_WT1_RTACN_EVT53**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RTACN_EVT53 This event measured by this field can be overwritten by AAC4[20].	

PWRMTR_WT1_REVT57TO60

PWRMTR_WT1_REVT57TO60 - PWRMTR_WT1_REVT57TO60	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0A838h

PWRMTR_WT1_REVT57to60

DWord	Bit	Description	
0	31:24	**PWRMTR_WT1_RTSOI_EVT60**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RTS OI_EVT60 This event measured by this field can be overwritten by AAC4[27].	
	23:16	**PWRMTR_WT1_RTSOI_EVT59**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RTS OI_EVT59 This event measured by this field can be overwritten by AAC4[26].	
	15:8	**PWRMTR_WT1_RTSOI_EVT58**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RTS OI_EVT58 This event measured by this field can be overwritten by AAC4[25].	
		Programming Notes	
		Must be set to zero at all times.	
	7:0	**PWRMTR_WT1_RTSOI_EVT57**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RTS OI_EVT57 This event measured by this field can be overwritten by AAC4[24].	
		Programming Notes	
		Must be set to zero at all times.	

PWRMTR_WT1_REVT61TO64

PWRMTR_WT1_REVT61TO64 - PWRMTR_WT1_REVT61TO64	

Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32

Address:	0A83Ch

PWRMTR_WT1_REVT61to64

DWord	Bit	Description
0	31:24	**PWRMTR_WT1_RTOOI_EVT64**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_RTOOI_EVT64 This event measured by this field can be overwritten by AAC4[31].
	23:16	**PWRMTR_WT1_RTOOI_EVT63**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_RTOOI_EVT63 This event measured by this field can be overwritten by AAC4[30].
	15:8	**PWRMTR_WT1_RTOOI_EVT62**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_RTOOI_EVT62 This event measured by this field can be overwritten by AAC4[29].
	7:0	**PWRMTR_WT1_RTOOI_EVT61**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT1_RTOOI_EVT61 This event measured by this field can be overwritten by AAC4[28].

PWRMTR_WT1_REVT65TO68

PWRMTR_WT1_REVT65TO68 - PWRMTR_WT1_REVT65TO68	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0A840h

PWRMTR_WT1_REVT65to68

DWord	Bit	Description	
0	31:24	**PWRMTR_WT1_RGTCN_EVT68**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RGTCN_EVT68 This event measured by this field can be overwritten by AAC8[3].	
	23:16	**PWRMTR_WT1_RGTCN_EVT67**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RGTCN_EVT67 This event measured by this field can be overwritten by AAC8[2].	
	15:8	**PWRMTR_WT1_RGTCN_EVT66**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RGTCN_EVT66 This event measured by this field can be overwritten by AAC8[1].	
	7:0	**PWRMTR_WT1_RGTOI_EVT65**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RGTOI_EVT65 This event measured by this field can be overwritten by AAC8[0].	

PWRMTR_WT1_REVT69TO70

PWRMTR_WT1_REVT69TO70 - PWRMTR_WT1_REVT69TO70	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0A844h

PWRMTR_WT1_REVT69to70

DWord	Bit	Description	
0	31:16	**Reserved**	
		Default Value:	0000h
		Access:	RO
		Reserved	
	15:8	**PWRMTR_WT1_RGTCN_EVT70**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RGTCN_EVT70 This event measured by this field can be overwritten by AAC8[5].	
	7:0	**PWRMTR_WT1_RGTCN_EVT69**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT1_RGTCN_EVT69 This event measured by this field can be overwritten by AAC8[4].	

PWRMTR_WT2_EEVT1TO4

PWRMTR_WT2_EEVT1TO4 - PWRMTR_WT2_EEVT1TO4	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0A950h

PWRMTR_WT2_EEVT1to4

DWord	Bit	Description
0	31:24	**PWRMTR_WT2_EU_TH_EVT4**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT2_EU_TH_EVT4 This event measured by this field can be overwritten by AACC[3].
	23:16	**PWRMTR_WT2_EU_GA_EVT3**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT2_EU_GA_EVT3 This event measured by this field can be overwritten by AACC[2].
	15:8	**PWRMTR_WT2_EU_GA_EVT2**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT2_EU_GA_EVT2 This event measured by this field can be overwritten by AACC[1].
	7:0	**PWRMTR_WT2_EU_GA_EVT1**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT2_EU_GA_EVT1 This event measured by this field can be overwritten by AACC[0].

PWRMTR_WT2_EEVT5TO8

PWRMTR_WT2_EEVT5TO8 - PWRMTR_WT2_EEVT5TO8		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A954h	
PWRMTR_WT2_EEVT5to8		

DWord	Bit	Description		
0	31:24	**PWRMTR_WT2_E0_HP_EVT8**		
		Default Value:		00h
		Access:		R/W Lock
		PWRMTR_WT2_E0_HP_EVT8 This event measured by this field can be overwritten by AACC[7].		
	23:16	**PWRMTR_WT2_E0_HP_EVT7**		
		Default Value:		00h
		Access:		R/W Lock
		PWRMTR_WT2_E0_HP_EVT7 This event measured by this field can be overwritten by AACC[6].		
	15:8	**PWRMTR_WT2_E0_HP_EVT6**		
		Default Value:		00h
		Access:		R/W Lock
		PWRMTR_WT2_E0_HP_EVT6 This event measured by this field can be overwritten by AACC[5].		
	7:0	**PWRMTR_WT2_EU_IO_EVT5**		
		Default Value:		00h
		Access:		R/W Lock
		PWRMTR_WT2_EU_IO_EVT5 This event measured by this field can be overwritten by AACC[4].		

PWRMTR_WT2_EEVT9TO12

PWRMTR_WT2_EEVT9TO12 - PWRMTR_WT2_EEVT9TO12		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A958h	
PWRMTR_WT2_EEVT9to12		

DWord	Bit	Description
0	31:24	**PWRMTR_WT2_E0_SP_EVT12**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT2_E0_SP_EVT12 This event measured by this field can be overwritten by AACC[11].
	23:16	**PWRMTR_WT2_E0_SP_EVT11**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT2_E0_SP_EVT11 This event measured by this field can be overwritten by AACC[10].
	15:8	**PWRMTR_WT2_E0_SP_EVT10**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT2_E0_SP_EVT10 This event measured by this field can be overwritten by AACC[9].
	7:0	**PWRMTR_WT2_E0_HP_EVT9**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT2_E0_HP_EVT9 This event measured by this field can be overwritten by AACC[8].

PWRMTR_WT2_EEVT13TO16

PWRMTR_WT2_EEVT13TO16 - PWRMTR_WT2_EEVT13TO16		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A95Ch	

PWRMTR_WT2_EEVT13to16		
DWord	**Bit**	**Description**
0	31:24	**PWRMTR_WT2_E0_DP_EVT16**
		Default Value: / 00h
		Access: / R/W Lock
		PWRMTR_WT2_E0_DP_EVT16 This event measured by this field can be overwritten by AACC[15].
		Programming Notes
		Must be 0 at all times.
	23:16	**PWRMTR_WT2_E0_DP_EVT15**
		Default Value: / 00h
		Access: / R/W Lock
		PWRMTR_WT2_E0_DP_EVT15 This event measured by this field can be overwritten by AACC[14].
		Programming Notes
		Must be 0 at all times.
	15:8	**PWRMTR_WT2_E0_DP_EVT14**
		Default Value: / 00h
		Access: / R/W Lock
		PWRMTR_WT2_E0_DP_EVT14 This event measured by this field can be overwritten by AACC[13].
		Programming Notes
		Must be 0 at all times.
	7:0	**PWRMTR_WT2_E0_SP_EVT13**
		Default Value: / 00h
		Access: / R/W Lock
		PWRMTR_WT2_E0_SP_EVT13 This event measured by this field can be overwritten by AACC[12].

PWRMTR_WT2_EEVT17TO20

PWRMTR_WT2_EEVT17TO20 - PWRMTR_WT2_EEVT17TO20	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0A960h

PWRMTR_WT2_EEVT17to20

DWord	Bit	Description
0	31:24	**PWRMTR_WT2_E0INT_EVT20**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT2_E0INT_EVT20 This event measured by this field can be overwritten by AACC[19].
	23:16	**PWRMTR_WT2_E0INT_EVT19**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT2_E0INT_EVT19 This event measured by this field can be overwritten by AACC[18].
		Programming Notes
		Must be 0 at all times.
	15:8	**PWRMTR_WT2_E0INT_EVT18**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT2_E0INT_EVT18 This event measured by this field can be overwritten by AACC[17].
	7:0	**PWRMTR_WT2_E0_DP_EVT17**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT2_E0_DP_EVT17 This event measured by this field can be overwritten by AACC[16].
		Programming Notes
		Must be 0 at all times.

PWRMTR_WT2_EEVT21TO24

PWRMTR_WT2_EEVT21TO24 - PWRMTR_WT2_EEVT21TO24		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A964h	
PWRMTR_WT2_EEVT21to24		

DWord	Bit	Description
0	31:24	**PWRMTR_WT2_E0_QP_EVT24**
		<table><tr><td>Default Value:</td><td>00h</td></tr><tr><td>Access:</td><td>R/W Lock</td></tr></table> PWRMTR_WT2_E0_QP_EVT24 This event measured by this field can be overwritten by AACC[23]. **Programming Notes** Must be 0 at all times.
	23:16	**PWRMTR_WT2_E0_QP_EVT23**
		<table><tr><td>Default Value:</td><td>00h</td></tr><tr><td>Access:</td><td>R/W Lock</td></tr></table> PWRMTR_WT2_E0_QP_EVT23 This event measured by this field can be overwritten by AACC[22]. **Programming Notes** Must be 0 at all times.
	15:8	**PWRMTR_WT2_E0_QP_EVT22**
		<table><tr><td>Default Value:</td><td>00h</td></tr><tr><td>Access:</td><td>R/W Lock</td></tr></table> PWRMTR_WT2_E0_QP_EVT22 This event measured by this field can be overwritten by AACC[21].
	7:0	**PWRMTR_WT2_E0INT_EVT21**
		<table><tr><td>Default Value:</td><td>00h</td></tr><tr><td>Access:</td><td>R/W Lock</td></tr></table> PWRMTR_WT2_E0INT_EVT21 This event measured by this field can be overwritten by AACC[20].

PWRMTR_WT2_EEVT25TO28

PWRMTR_WT2_EEVT25TO28 - PWRMTR_WT2_EEVT25TO28	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0A968h

PWRMTR_WT2_EEVT25to28

DWord	Bit	Description
0	31:24	**PWRMTR_WT2_EFPU0_EVT28**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT2_EFPU0_EVT28 This event measured by this field can be overwritten by AACC[27].
	23:16	**PWRMTR_WT2_EFPU0_EVT27**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT2_EFPU0_EVT27 This event measured by this field can be overwritten by AACC[26].
	15:8	**PWRMTR_WT2_EFPU0_EVT26**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT2_EFPU0_EVT26 This event measured by this field can be overwritten by AACC[25].
	7:0	**PWRMTR_WT2_E0_QP_EVT25**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT2_E0_QP_EVT25 This event measured by this field can be overwritten by AACC[24].
		Programming Notes
		Must be 0 at all times.

PWRMTR_WT2_EEVT29TO32

PWRMTR_WT2_EEVT29TO32 - PWRMTR_WT2_EEVT29TO32		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A96Ch	

PWRMTR_WT2_EEVT29to32		
DWord	**Bit**	**Description**
0	31:24	**PWRMTR_WT2_E1_HP_EVT32**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT2_E1_HP_EVT32 This event measured by this field can be overwritten by AACC[31].
	23:16	**PWRMTR_WT2_E1_HP_EVT31**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT2_E1_HP_EVT31 This event measured by this field can be overwritten by AACC[30].
	15:8	**PWRMTR_WT2_E1_HP_EVT30**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT2_E1_HP_EVT30 This event measured by this field can be overwritten by AACC[29].
	7:0	**PWRMTR_WT2_EFPU0_EVT29**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT2_EFPU0_EVT29 This event measured by this field can be overwritten by AACC[28].

PWRMTR_WT2_EEVT33TO36

PWRMTR_WT2_EEVT33TO36 - PWRMTR_WT2_EEVT33TO36	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0A970h

PWRMTR_WT2_EEVT33to36

DWord	Bit	Description	
0	31:24	**PWRMTR_WT2_E1_SP_EVT36**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT2_E1_SP_EVT36 This event measured by this field can be overwritten by AAD0[3].	
	23:16	**PWRMTR_WT2_E1_SP_EVT35**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT2_E1_SP_EVT35 This event measured by this field can be overwritten by AAD0[2].	
	15:8	**PWRMTR_WT2_E1_SP_EVT34**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT2_E1_SP_EVT34 This event measured by this field can be overwritten by AAD0[1].	
	7:0	**PWRMTR_WT2_E1_HP_EVT33**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT2_E1_HP_EVT33 This event measured by this field can be overwritten by AAD0[0].	

PWRMTR_WT2_EEVT37TO40

PWRMTR_WT2_EEVT37TO40 - PWRMTR_WT2_EEVT37TO40	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0A974h

PWRMTR_WT2_EEVT37to40

DWord	Bit	Description	
0	31:24	**PWRMTR_WT2_E1_DP_EVT40**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT2_E1_DP_EVT40 This event measured by this field can be overwritten by AAD0[7].	
	23:16	**PWRMTR_WT2_E1_DP_EVT39**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT2_E1_DP_EVT39 This event measured by this field can be overwritten by AAD0[6].	
	15:8	**PWRMTR_WT2_E1_DP_EVT38**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT2_E1_DP_EVT38 This event measured by this field can be overwritten by AAD0[5].	
	7:0	**PWRMTR_WT2_E1_SP_EVT37**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT2_E1_SP_EVT37 This event measured by this field can be overwritten by AAD0[4].	

PWRMTR_WT2_EEVT41TO44

PWRMTR_WT2_EEVT41TO44 - PWRMTR_WT2_EEVT41TO44		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A978h	
PWRMTR_WT2_EEVT41to44		

DWord	Bit	Description
0	31:24	**PWRMTR_WT2_E1INT_EVT44**
		<table><tr><td>Default Value:</td><td>00h</td></tr><tr><td>Access:</td><td>R/W Lock</td></tr></table>
		PWRMTR_WT2_E1INT_EVT44 This event measured by this field can be overwritten by AAD0[11].
	23:16	**PWRMTR_WT2_E1INT_EVT43**
		<table><tr><td>Default Value:</td><td>00h</td></tr><tr><td>Access:</td><td>R/W Lock</td></tr></table>
		PWRMTR_WT2_E1INT_EVT43 This event measured by this field can be overwritten by AAD0[10].
		Programming Notes
		Must be 0 at all times.
	15:8	**PWRMTR_WT2_E1INT_EVT42**
		<table><tr><td>Default Value:</td><td>00h</td></tr><tr><td>Access:</td><td>R/W Lock</td></tr></table>
		PWRMTR_WT2_E1INT_EVT42 This event measured by this field can be overwritten by AAD0[9].
	7:0	**PWRMTR_WT2_E1_DP_EVT41**
		<table><tr><td>Default Value:</td><td>00h</td></tr><tr><td>Access:</td><td>R/W Lock</td></tr></table>
		PWRMTR_WT2_E1_DP_EVT41 This event measured by this field can be overwritten by AAD0[8].

PWRMTR_WT2_EEVT45TO48

PWRMTR_WT2_EEVT45TO48 - PWRMTR_WT2_EEVT45TO48	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0A97Ch

PWRMTR_WT2_EEVT45to48

DWord	Bit	Description	
0	31:24	**PWRMTR_WT2_E1_QP_EVT48**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT2_E1_QP_EVT48 This event measured by this field can be overwritten by AAD0[15].	
	23:16	**PWRMTR_WT2_E1_QP_EVT47**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT2_E1_QP_EVT47 This event measured by this field can be overwritten by AAD0[14].	
		Programming Notes	
		Must be 0 at all times.	
	15:8	**PWRMTR_WT2_E1_QP_EVT46**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT2_E1_QP_EVT46 This event measured by this field can be overwritten by AAD0[13].	
	7:0	**PWRMTR_WT2_E1INT_EVT45**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT2_E1INT_EVT45 This event measured by this field can be overwritten by AAD0[12].	

PWRMTR_WT2_EEVT49TO52

PWRMTR_WT2_EEVT49TO52 - PWRMTR_WT2_EEVT49TO52	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0A980h

PWRMTR_WT2_EEVT49to52

DWord	Bit	Description	
0	31:24	**PWRMTR_WT2_EFPU1_EVT52**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT2_EFPU1_EVT52 This event measured by this field can be overwritten by AAD0[19].	
	23:16	**PWRMTR_WT2_EFPU1_EVT51**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT2_EFPU1_EVT51 This event measured by this field can be overwritten by AAD0[18].	
	15:8	**PWRMTR_WT2_EFPU1_EVT50**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT2_EFPU1_EVT50 This event measured by this field can be overwritten by AAD0[17].	
	7:0	**PWRMTR_WT2_E1_QP_EVT49**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT2_E1_QP_EVT49 This event measured by this field can be overwritten by AAD0[16].	

PWRMTR_WT2_EEVT53TO56

PWRMTR_WT2_EEVT53TO56 - PWRMTR_WT2_EEVT53TO56	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0A984h

PWRMTR_WT2_EEVT53to56

DWord	Bit	Description	
0	31:24	**PWRMTR_WT2_EEMEM_EVT56**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT2_EEMEM_EVT56 This event measured by this field can be overwritten by AAD0[23].	
	23:16	**PWRMTR_WT2_EEMEM_EVT55**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT2_EEMEM_EVT55 This event measured by this field can be overwritten by AAD0[22].	
	15:8	**PWRMTR_WT2_EEMEM_EVT54**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT2_EEMEM_EVT54 This event measured by this field can be overwritten by AAD0[21].	
	7:0	**PWRMTR_WT2_EFPU1_EVT53**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT2_EFPU1_EVT53 This event measured by this field can be overwritten by AAD0[20].	

PWRMTR_WT2_EEVT57TO58

PWRMTR_WT2_EEVT57TO58 - PWRMTR_WT2_EEVT57TO58		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A988h	
PWRMTR_WT2_EEVT57to58		

DWord	Bit	Description
0	31:16	**Reserved**
		Default Value: 0000h
		Access: RO
		Reserved
	15:8	**PWRMTR_WT2_EBUSS_EVT58**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT2_EBUSS_EVT58 This event measured by this field can be overwritten by AAD0[25].
	7:0	**PWRMTR_WT2_EEMEM_EVT57**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT2_EEMEM_EVT57 This event measured by this field can be overwritten by AAD0[24].

PWRMTR_WT2_REVT5TO8

PWRMTR_WT2_REVT5TO8 - PWRMTR_WT2_REVT5TO8	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0A904h

PWRMTR_WT2_REVT5to8

DWord	Bit	Description	
0	31:24	**Reserved**	
		Default Value:	00h
		Access:	RO
		Reserved	
	23:16	**Reserved**	
		Default Value:	00h
		Access:	RO
		Reserved	
	15:8	**Reserved**	
		Default Value:	00h
		Access:	RO
		Reserved	
	7:0	**PWRMTR_WT2_RFFOI_EVT5**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT2_RFFOI_EVT5 This event measured by this field can be overwritten by AAC0[4].	

PWRMTR_WT2_REVT33TO36

PWRMTR_WT2_REVT33TO36 - PWRMTR_WT2_REVT33TO36		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A920h	
PWRMTR_WT2_REVT33to36		

DWord	Bit	Description	
0	31:24	**PWRMTR_WT2_RL3MI_EVT36**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT2_RL3MI_EVT36 This event measured by this field can be overwritten by AAC4[3].	
	23:16	**Reserved**	
		Default Value:	00h
		Access:	RO
		Reserved	
	15:8	**Reserved**	
		Default Value:	00h
		Access:	RO
		Reserved	
	7:0	**Reserved**	
		Default Value:	00h
		Access:	RO
		Reserved	

PWRMTR_WT2_REVT37TO40

PWRMTR_WT2_REVT37TO40 - PWRMTR_WT2_REVT37TO40	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0A924h
PWRMTR_WT2_REVT37to40	

DWord	Bit	Description
0	31:24	**PWRMTR_WT2_RTAOI_EVT40**
		Default Value: / 00h
		Access: / R/W Lock
		PWRMTR_WT2_RTAOI_EVT40 This event measured by this field can be overwritten by AAC4[7].
	23:16	**Reserved**
		Default Value: / 00h
		Access: / RO
		Reserved
	15:8	**Reserved**
		Default Value: / 00h
		Access: / RO
		Reserved
	7:0	**PWRMTR_WT2_RL3MI_EVT37**
		Default Value: / 00h
		Access: / R/W Lock
		PWRMTR_WT2_RL3MI_EVT37 This event measured by this field can be overwritten by AAC4[4].

PWRMTR_WT2_REVT41TO44

PWRMTR_WT2_REVT41TO44 - PWRMTR_WT2_REVT41TO44		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A928h	
PWRMTR_WT2_REVT41to44		

DWord	Bit	Description		
0	31:24	**Reserved**		
		Default Value:		00h
		Access:		RO
		Reserved		
	23:16	**Reserved**		
		Default Value:		00h
		Access:		RO
		Reserved		
	15:8	**Reserved**		
		Default Value:		00h
		Access:		RO
		Reserved		
	7:0	**PWRMTR_WT2_RTAOI_EVT41**		
		Default Value:		00h
		Access:		R/W Lock
		PWRMTR_WT2_RTAOI_EVT41 This event measured by this field can be overwritten by AAC4[8].		

PWRMTR_WT2_REVT49TO52

PWRMTR_WT2_REVT49TO52 - PWRMTR_WT2_REVT49TO52		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A930h	
PWRMTR_WT2_REVT49to52		

DWord	Bit	Description
0	31:24	**PWRMTR_WT2_RTAOH_EVT52**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT2_RTAOH_EVT52 This event measured by this field can be overwritten by AAC4[19].
	23:16	**PWRMTR_WT2_RTAOH_EVT51**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT2_RTAOH_EVT51 This event measured by this field can be overwritten by AAC4[18].
	15:8	**Reserved**
		Default Value: 00h
		Access: RO
		Reserved
	7:0	**PWRMTR_WT2_RTAOI_EVT49**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT2_RTAOI_EVT49 This event measured by this field can be overwritten by AAC4[16].

PWRMTR_WT2_REVT53TO56

PWRMTR_WT2_REVT53TO56 - PWRMTR_WT2_REVT53TO56		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A934h	
PWRMTR_WT2_REVT53to56		

DWord	Bit	Description
0	31:24	**PWRMTR_WT2_RTSOI_EVT56**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT2_RTS OI_EVT56 This event measured by this field can be overwritten by AAC4[23].
	23:16	**PWRMTR_WT2_RTACN_EVT55**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT2_RTACN_EVT55 This event measured by this field can be overwritten by AAC4[22].
	15:8	**PWRMTR_WT2_RTACN_EVT54**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT2_RTACN_EVT54 This event measured by this field can be overwritten by AAC4[21].
	7:0	**Reserved**
		Default Value: 00h
		Access: RO
		Reserved

PWRMTR_WT2_REVT65TO68

PWRMTR_WT2_REVT65TO68 - PWRMTR_WT2_REVT65TO68	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0A940h

PWRMTR_WT2_REVT65to68

DWord	Bit	Description	
0	31:24	**Reserved**	
		Default Value:	00h
		Access:	RO
		Reserved	
	23:16	**Reserved**	
		Default Value:	00h
		Access:	RO
		Reserved	
	15:8	**PWRMTR_WT2_RGTCN_EVT66**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT2_RGTCN_EVT66 This event measured by this field can be overwritten by AAC8[1].	
	7:0	**PWRMTR_WT2_RGTOI_EVT65**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT2_RGTOI_EVT65 This event measured by this field can be overwritten by AAC8[0].	

PWRMTR_WT2_REVT69TO70

PWRMTR_WT2_REVT69TO70 - PWRMTR_WT2_REVT69TO70	

Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0A944h

PWRMTR_WT2_REVT69to70

DWord	Bit	Description
0	31:16	**Reserved**
		Default Value: 0000h
		Access: RO
		Reserved
	15:8	**PWRMTR_WT2_RGTCN_EVT70**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT2_RGTCN_EVT70 This event measured by this field can be overwritten by AAC8[5].
	7:0	**PWRMTR_WT2_RGTCN_EVT69**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT2_RGTCN_EVT69 This event measured by this field can be overwritten by AAC8[4].

PWRMTR_WT3_EEVT1TO4

PWRMTR_WT3_EEVT1TO4 - PWRMTR_WT3_EEVT1TO4	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0AA50h

PWRMTR_WT3_EEVT1to4

DWord	Bit	Description
0	31:24	**PWRMTR_WT3_EU_TH_EVT4**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT3_EU_TH_EVT4 This event measured by this field can be overwritten by AACC[3].
	23:16	**PWRMTR_WT3_EU_GA_EVT3**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT3_EU_GA_EVT3 This event measured by this field can be overwritten by AACC[2].
	15:8	**PWRMTR_WT3_EU_GA_EVT2**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT3_EU_GA_EVT2 This event measured by this field can be overwritten by AACC[1].
	7:0	**PWRMTR_WT3_EU_GA_EVT1**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT3_EU_GA_EVT1 This event measured by this field can be overwritten by AACC[0].

PWRMTR_WT3_EEVT5TO8

PWRMTR_WT3_EEVT5TO8 - PWRMTR_WT3_EEVT5TO8	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0AA54h

PWRMTR_WT3_EEVT5to8

DWord	Bit	Description	
0	31:24	**PWRMTR_WT3_E0_HP_EVT8**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT3_E0_HP_EVT8 This event measured by this field can be overwritten by AACC[7].	
	23:16	**PWRMTR_WT3_E0_HP_EVT7**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT3_E0_HP_EVT7 This event measured by this field can be overwritten by AACC[6].	
	15:8	**PWRMTR_WT3_E0_HP_EVT6**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT3_E0_HP_EVT6 This event measured by this field can be overwritten by AACC[5].	
	7:0	**PWRMTR_WT3_EU_IO_EVT5**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT3_EU_IO_EVT5 This event measured by this field can be overwritten by AACC[4].	

PWRMTR_WT3_EEVT9TO12

		PWRMTR_WT3_EEVT9TO12 - PWRMTR_WT3_EEVT9TO12
Register Space:		MMIO: 0/2/0
Project:		CHV, BSW
Source:		PRM
Default Value:		0x00000000
Size (in bits):		32
Address:		0AA58h

PWRMTR_WT3_EEVT9to12

DWord	Bit	Description
0	31:24	**PWRMTR_WT3_E0_SP_EVT12**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT3_E0_SP_EVT12 This event measured by this field can be overwritten by AACC[11].
	23:16	**PWRMTR_WT3_E0_SP_EVT11**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT3_E0_SP_EVT11 This event measured by this field can be overwritten by AACC[10].
	15:8	**PWRMTR_WT3_E0_SP_EVT10**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT3_E0_SP_EVT10 This event measured by this field can be overwritten by AACC[9].
	7:0	**PWRMTR_WT3_E0_HP_EVT9**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT3_E0_HP_EVT9 This event measured by this field can be overwritten by AACC[8].

PWRMTR_WT3_EEVT13TO16

PWRMTR_WT3_EEVT13TO16 - PWRMTR_WT3_EEVT13TO16		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0AA5Ch	
PWRMTR_WT3_EEVT13to16		

DWord	Bit	Description
0	31:24	**PWRMTR_WT3_E0_DP_EVT16**
		Default Value: 00h / Access: R/W Lock
		PWRMTR_WT3_E0_DP_EVT16 This event measured by this field can be overwritten by AACC[15].
		Programming Notes
		Must be 0 at all times.
	23:16	**PWRMTR_WT3_E0_DP_EVT15**
		Default Value: 00h / Access: R/W Lock
		PWRMTR_WT3_E0_DP_EVT15 This event measured by this field can be overwritten by AACC[14].
		Programming Notes
		Must be 0 at all times.
	15:8	**PWRMTR_WT3_E0_DP_EVT14**
		Default Value: 00h / Access: R/W Lock
		PWRMTR_WT3_E0_DP_EVT14 This event measured by this field can be overwritten by AACC[13].
		Programming Notes
		Must be 0 at all times.
	7:0	**PWRMTR_WT3_E0_SP_EVT13**
		Default Value: 00h / Access: R/W Lock
		PWRMTR_WT3_E0_SP_EVT13 This event measured by this field can be overwritten by AACC[12].

PWRMTR_WT3_EEVT17TO20

PWRMTR_WT3_EEVT17TO20 - PWRMTR_WT3_EEVT17TO20	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0AA60h

PWRMTR_WT3_EEVT17to20

DWord	Bit	Description
0	31:24	**PWRMTR_WT3_E0INT_EVT20**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT3_E0INT_EVT20 This event measured by this field can be overwritten by AACC[19].
	23:16	**PWRMTR_WT3_E0INT_EVT19**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT3_E0INT_EVT19 This event measured by this field can be overwritten by AACC[18].
		Programming Notes
		Must be 0 at all times.
	15:8	**PWRMTR_WT3_E0INT_EVT18**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT3_E0INT_EVT18 This event measured by this field can be overwritten by AACC[17].
	7:0	**PWRMTR_WT3_E0_DP_EVT17**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT3_E0_DP_EVT17 This event measured by this field can be overwritten by AACC[16].
		Programming Notes
		Must be 0 at all times.

PWRMTR_WT3_EEVT21TO24

PWRMTR_WT3_EEVT21TO24 - PWRMTR_WT3_EEVT21TO24		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0AA64h	
PWRMTR_WT3_EEVT21to24		

DWord	Bit	Description
0	31:24	**PWRMTR_WT3_E0_QP_EVT24**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT3_E0_QP_EVT24 This event measured by this field can be overwritten by AACC[23].
		Programming Notes
		Must be 0 at all times.
	23:16	**PWRMTR_WT3_E0_QP_EVT23**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT3_E0_QP_EVT23 This event measured by this field can be overwritten by AACC[22].
		Programming Notes
		Must be 0 at all times.
	15:8	**PWRMTR_WT3_E0_QP_EVT22**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT3_E0_QP_EVT22 This event measured by this field can be overwritten by AACC[21].
	7:0	**PWRMTR_WT3_E0INT_EVT21**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT3_E0INT_EVT21 This event measured by this field can be overwritten by AACC[20].

PWRMTR_WT3_EEVT25TO28

	PWRMTR_WT3_EEVT25TO28 - PWRMTR_WT3_EEVT25TO28	
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0AA68h	

PWRMTR_WT3_EEVT25to28

DWord	Bit	Description	
0	31:24	**PWRMTR_WT3_EFPU0_EVT28**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT3_EFPU0_EVT28 This event measured by this field can be overwritten by AACC[27].	
	23:16	**PWRMTR_WT3_EFPU0_EVT27**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT3_EFPU0_EVT27 This event measured by this field can be overwritten by AACC[26].	
	15:8	**PWRMTR_WT3_EFPU0_EVT26**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT3_EFPU0_EVT26 This event measured by this field can be overwritten by AACC[25].	
	7:0	**PWRMTR_WT3_E0_QP_EVT25**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT3_E0_QP_EVT25 This event measured by this field can be overwritten by AACC[24].	
		Programming Notes	
		Must be 0 at all times.	

PWRMTR_WT3_EEVT29TO32

PWRMTR_WT3_EEVT29TO32 - PWRMTR_WT3_EEVT29TO32	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0AA6Ch

PWRMTR_WT3_EEVT29to32

DWord	Bit	Description	
0	31:24	**PWRMTR_WT3_E1_HP_EVT32**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT3_E1_HP_EVT32 This event measured by this field can be overwritten by AACC[31].	
	23:16	**PWRMTR_WT3_E1_HP_EVT31**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT3_E1_HP_EVT31 This event measured by this field can be overwritten by AACC[30].	
	15:8	**PWRMTR_WT3_E1_HP_EVT30**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT3_E1_HP_EVT30 This event measured by this field can be overwritten by AACC[29].	
	7:0	**PWRMTR_WT3_EFPU0_EVT29**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT3_EFPU0_EVT29 This event measured by this field can be overwritten by AACC[28].	

PWRMTR_WT3_EEVT33TO36

			PWRMTR_WT3_EEVT33TO36 - PWRMTR_WT3_EEVT33TO36	
Register Space:		MMIO: 0/2/0		
Project:		CHV, BSW		
Source:		PRM		
Default Value:		0x00000000		
Size (in bits):		32		
Address:		0AA70h		
PWRMTR_WT3_EEVT33to36				
DWord	**Bit**	**Description**		
0	31:24	**PWRMTR_WT3_E1_SP_EVT36**		
		Default Value:		00h
		Access:		R/W Lock
		PWRMTR_WT3_E1_SP_EVT36 This event measured by this field can be overwritten by AAD0[3].		
	23:16	**PWRMTR_WT3_E1_SP_EVT35**		
		Default Value:		00h
		Access:		R/W Lock
		PWRMTR_WT3_E1_SP_EVT35 This event measured by this field can be overwritten by AAD0[2].		
	15:8	**PWRMTR_WT3_E1_SP_EVT34**		
		Default Value:		00h
		Access:		R/W Lock
		PWRMTR_WT3_E1_SP_EVT34 This event measured by this field can be overwritten by AAD0[1].		
	7:0	**PWRMTR_WT3_E1_HP_EVT33**		
		Default Value:		00h
		Access:		R/W Lock
		PWRMTR_WT3_E1_HP_EVT33 This event measured by this field can be overwritten by AAD0[0].		

PWRMTR_WT3_EEVT37TO40

PWRMTR_WT3_EEVT37TO40 - PWRMTR_WT3_EEVT37TO40		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0AA74h	

PWRMTR_WT3_EEVT37to40

DWord	Bit	Description
0	31:24	**PWRMTR_WT3_E1_DP_EVT40**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT3_E1_DP_EVT40 This event measured by this field can be overwritten by AAD0[7].
	23:16	**PWRMTR_WT3_E1_DP_EVT39**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT3_E1_DP_EVT39 This event measured by this field can be overwritten by AAD0[6].
	15:8	**PWRMTR_WT3_E1_DP_EVT38**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT3_E1_DP_EVT38 This event measured by this field can be overwritten by AAD0[5].
	7:0	**PWRMTR_WT3_E1_SP_EVT37**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT3_E1_SP_EVT37 This event measured by this field can be overwritten by AAD0[4].

PWRMTR_WT3_EEVT41TO44

PWRMTR_WT3_EEVT41TO44 - PWRMTR_WT3_EEVT41TO44		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0AA78h	
PWRMTR_WT3_EEVT41to44		

DWord	Bit	Description
0	31:24	**PWRMTR_WT3_E1INT_EVT44**
		<table><tr><td>Default Value:</td><td>00h</td></tr><tr><td>Access:</td><td>R/W Lock</td></tr></table> PWRMTR_WT3_E1INT_EVT44 This event measured by this field can be overwritten by AAD0[11].
	23:16	**PWRMTR_WT3_E1INT_EVT43**
		<table><tr><td>Default Value:</td><td>00h</td></tr><tr><td>Access:</td><td>R/W Lock</td></tr></table> PWRMTR_WT3_E1INT_EVT43 This event measured by this field can be overwritten by AAD0[10]. **Programming Notes** Must be 0 at all times.
	15:8	**PWRMTR_WT3_E1INT_EVT42**
		<table><tr><td>Default Value:</td><td>00h</td></tr><tr><td>Access:</td><td>R/W Lock</td></tr></table> PWRMTR_WT3_E1INT_EVT42 This event measured by this field can be overwritten by AAD0[9].
	7:0	**PWRMTR_WT3_E1_DP_EVT41**
		<table><tr><td>Default Value:</td><td>00h</td></tr><tr><td>Access:</td><td>R/W Lock</td></tr></table> PWRMTR_WT3_E1_DP_EVT41 This event measured by this field can be overwritten by AAD0[8].

PWRMTR_WT3_EEVT45TO48

PWRMTR_WT3_EEVT45TO48 - PWRMTR_WT3_EEVT45TO48		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0AA7Ch	
PWRMTR_WT3_EEVT45to48		

DWord	Bit	Description
0	31:24	**PWRMTR_WT3_E1_QP_EVT48**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT3_E1_QP_EVT48 This event measured by this field can be overwritten by AAD0[15].
	23:16	**PWRMTR_WT3_E1_QP_EVT47**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT3_E1_QP_EVT47 This event measured by this field can be overwritten by AAD0[14].
		Programming Notes
		Must be 0 at all times.
	15:8	**PWRMTR_WT3_E1_QP_EVT46**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT3_E1_QP_EVT46 This event measured by this field can be overwritten by AAD0[13].
	7:0	**PWRMTR_WT3_E1INT_EVT45**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT3_E1INT_EVT45 This event measured by this field can be overwritten by AAD0[12].

PWRMTR_WT3_EEVT49TO52

PWRMTR_WT3_EEVT49TO52 - PWRMTR_WT3_EEVT49TO52	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0AA80h

PWRMTR_WT3_EEVT49to52

DWord	Bit	Description	
0	31:24	**PWRMTR_WT3_EFPU1_EVT52**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT3_EFPU1_EVT52 This event measured by this field can be overwritten by AAD0[19].	
	23:16	**PWRMTR_WT3_EFPU1_EVT51**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT3_EFPU1_EVT51 This event measured by this field can be overwritten by AAD0[18].	
	15:8	**PWRMTR_WT3_EFPU1_EVT50**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT3_EFPU1_EVT50 This event measured by this field can be overwritten by AAD0[17].	
	7:0	**PWRMTR_WT3_E1_QP_EVT49**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT3_E1_QP_EVT49 This event measured by this field can be overwritten by AAD0[16].	

PWRMTR_WT3_EEVT53TO56

PWRMTR_WT3_EEVT53TO56 - PWRMTR_WT3_EEVT53TO56

Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32

Address:	0AA84h

PWRMTR_WT3_EEVT53to56

DWord	Bit	Description
0	31:24	**PWRMTR_WT3_EEMEM_EVT56**
		Default Value: 00h / Access: R/W Lock
		PWRMTR_WT3_EEMEM_EVT56 This event measured by this field can be overwritten by AAD0[23].
	23:16	**PWRMTR_WT3_EEMEM_EVT55**
		Default Value: 00h / Access: R/W Lock
		PWRMTR_WT3_EEMEM_EVT55 This event measured by this field can be overwritten by AAD0[22].
	15:8	**PWRMTR_WT3_EEMEM_EVT54**
		Default Value: 00h / Access: R/W Lock
		PWRMTR_WT3_EEMEM_EVT54 This event measured by this field can be overwritten by AAD0[21].
	7:0	**PWRMTR_WT3_EFPU1_EVT53**
		Default Value: 00h / Access: R/W Lock
		PWRMTR_WT3_EFPU1_EVT53 This event measured by this field can be overwritten by AAD0[20].

PWRMTR_WT3_EEVT57TO58

PWRMTR_WT3_EEVT57TO58 - PWRMTR_WT3_EEVT57TO58		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0AA88h	
PWRMTR_WT3_EEVT57to58		

DWord	Bit	Description
0	31:16	**Reserved**
		Default Value: ... 0000h
		Access: ... RO
		Reserved
	15:8	**PWRMTR_WT3_EBUSS_EVT58**
		Default Value: ... 00h
		Access: ... R/W Lock
		PWRMTR_WT3_EBUSS_EVT58 This event measured by this field can be overwritten by AAD0[25].
	7:0	**PWRMTR_WT3_EEMEM_EVT57**
		Default Value: ... 00h
		Access: ... R/W Lock
		PWRMTR_WT3_EEMEM_EVT57 This event measured by this field can be overwritten by AAD0[24].

PWRMTR_WT3_REVT5TO8

PWRMTR_WT3_REVT5TO8 - PWRMTR_WT3_REVT5TO8	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0AA04h

PWRMTR_WT3_REVT5to8

DWord	Bit	Description
0	31:24	**Reserved**
		Default Value: 00h
		Access: RO
		Reserved
	23:16	**Reserved**
		Default Value: 00h
		Access: RO
		Reserved
	15:8	**Reserved**
		Default Value: 00h
		Access: RO
		Reserved
	7:0	**PWRMTR_WT3_RFFOI_EVT5**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT3_RFFOI_EVT5 This event measured by this field can be overwritten by AAC0[4].

PWRMTR_WT3_REVT33TO36

PWRMTR_WT3_REVT33TO36 - PWRMTR_WT3_REVT33TO36	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0AA20h

PWRMTR_WT3_REVT33to36

DWord	Bit	Description	
0	31:24	**PWRMTR_WT3_RL3MI_EVT36**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT3_RL3MI_EVT36 This event measured by this field can be overwritten by AAC4[3].	
	23:16	**Reserved**	
		Default Value:	00h
		Access:	RO
		Reserved	
	15:8	**Reserved**	
		Default Value:	00h
		Access:	RO
		Reserved	
	7:0	**Reserved**	
		Default Value:	00h
		Access:	RO
		Reserved	

PWRMTR_WT3_REVT37TO40

PWRMTR_WT3_REVT37TO40 - PWRMTR_WT3_REVT37TO40		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0AA24h	
PWRMTR_WT3_REVT37to40		

DWord	Bit	Description
0	31:24	**PWRMTR_WT3_RTAOI_EVT40**
		<table><tr><td>Default Value:</td><td>00h</td></tr><tr><td>Access:</td><td>R/W Lock</td></tr></table> PWRMTR_WT3_RTAOI_EVT40 This event measured by this field can be overwritten by AAC4[7].
	23:16	**Reserved**
		<table><tr><td>Default Value:</td><td>00h</td></tr><tr><td>Access:</td><td>RO</td></tr></table> Reserved
	15:8	**Reserved**
		<table><tr><td>Default Value:</td><td>00h</td></tr><tr><td>Access:</td><td>RO</td></tr></table> Reserved
	7:0	**PWRMTR_WT3_RL3MI_EVT37**
		<table><tr><td>Default Value:</td><td>00h</td></tr><tr><td>Access:</td><td>R/W Lock</td></tr></table> PWRMTR_WT3_RL3MI_EVT37 This event measured by this field can be overwritten by AAC4[4].

PWRMTR_WT3_REVT41TO44

PWRMTR_WT3_REVT41TO44 - PWRMTR_WT3_REVT41TO44		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0AA28h	
PWRMTR_WT3_REVT41to44		

DWord	Bit	Description
0	31:24	**Reserved**
		Default Value: ... 00h
		Access: ... RO
		Reserved
	23:16	**Reserved**
		Default Value: ... 00h
		Access: ... RO
		Reserved
	15:8	**Reserved**
		Default Value: ... 00h
		Access: ... RO
		Reserved
	7:0	**PWRMTR_WT3_RTAOI_EVT41**
		Default Value: ... 00h
		Access: ... R/W Lock
		PWRMTR_WT3_RTAOI_EVT41 This event measured by this field can be overwritten by AAC4[8].

PWRMTR_WT3_REVT49TO52

PWRMTR_WT3_REVT49TO52 - PWRMTR_WT3_REVT49TO52	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0AA30h

PWRMTR_WT3_REVT49to52

DWord	Bit	Description	
0	31:24	**PWRMTR_WT3_RTAOH_EVT52**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT3_RTAOH_EVT52 This event measured by this field can be overwritten by AAC4[19].	
	23:16	**PWRMTR_WT3_RTAOH_EVT51**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT3_RTAOH_EVT51 This event measured by this field can be overwritten by AAC4[18].	
	15:8	**Reserved**	
		Default Value:	00h
		Access:	RO
		Reserved	
	7:0	**PWRMTR_WT3_RTAOI_EVT49**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT3_RTAOI_EVT49 This event measured by this field can be overwritten by AAC4[16].	

PWRMTR_WT3_REVT53TO56

PWRMTR_WT3_REVT53TO56 - PWRMTR_WT3_REVT53TO56	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0AA34h

PWRMTR_WT3_REVT53to56

DWord	Bit	Description	
0	31:24	**PWRMTR_WT3_RTSOI_EVT56**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT3_RTS OI_EVT56 This event measured by this field can be overwritten by AAC4[23].	
	23:16	**PWRMTR_WT3_RTACN_EVT55**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT3_RTACN_EVT55 This event measured by this field can be overwritten by AAC4[22].	
	15:8	**PWRMTR_WT3_RTACN_EVT54**	
		Default Value:	00h
		Access:	R/W Lock
		PWRMTR_WT3_RTACN_EVT54 This event measured by this field can be overwritten by AAC4[21].	
	7:0	**Reserved**	
		Default Value:	00h
		Access:	RO
		Reserved	

PWRMTR_WT3_REVT65TO68

PWRMTR_WT3_REVT65TO68 - PWRMTR_WT3_REVT65TO68		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0AA40h	
PWRMTR_WT3_REVT65to68		

DWord	Bit	Description
0	31:24	**Reserved**
		Default Value: 00h
		Access: RO
		Reserved
	23:16	**Reserved**
		Default Value: 00h
		Access: RO
		Reserved
	15:8	**PWRMTR_WT3_RGTCN_EVT66**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT3_RGTCN_EVT66 This event measured by this field can be overwritten by AAC8[1].
	7:0	**PWRMTR_WT3_RGTOI_EVT65**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT3_RGTOI_EVT65 This event measured by this field can be overwritten by AAC8[0].

PWRMTR_WT3_REVT69TO70

PWRMTR_WT3_REVT69TO70 - PWRMTR_WT3_REVT69TO70		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0AA44h	
PWRMTR_WT3_REVT69to70		

DWord	Bit	Description
0	31:16	**Reserved**
		Default Value: 0000h
		Access: RO
		Reserved
	15:8	**PWRMTR_WT3_RGTCN_EVT70**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT3_RGTCN_EVT70 This event measured by this field can be overwritten by AAC8[5].
	7:0	**PWRMTR_WT3_RGTCN_EVT69**
		Default Value: 00h
		Access: R/W Lock
		PWRMTR_WT3_RGTCN_EVT69 This event measured by this field can be overwritten by AAC8[4].

 Command Reference: Registers.

PWRMTREVTORE0

PWRMTREVTORE0 - PWRMTREVTORE0	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0AACCh

GT_CR_POWER_METER_EVENT_OVERRIDE_EU1_32

DWord	Bit	Description
0	31:0	**PMEVORE0**

Default Value:	00000000h
Access:	R/W Lock

Power Meter Event Override for Render Events.Allows user to override signal coming in from Gfx engine and count event every cycle on a per event basis.
For each event:
0: Power Meter works normally with event input taken from Gfx engine.
1: Force event input to weighting logic high every cuclk, overriding event data coming in from Gfx engine.
This register is the override for events 1 through 32, where bit 0 corresponds to event 1, and bit 31 corresponds to event 32. "

PWRMTREVTORE1

PWRMTREVTORE1 - PWRMTREVTORE1		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0AAD0h	
GT_CR_POWER_METER_EVENT_OVERRIDE_EU33_58		

DWord	Bit	Description	
0	31:26	**Reserved**	
		Default Value:	00000000h
		Access:	RO
		Reserved	
	25:0	**PMEVORE1**	
		Default Value:	00000000h
		Access:	R/W Lock
		Power Meter Event Override for Render Events.Allows user to override signal coming in from Gfx engine and count event every cycle on a per event basis. For each event: 0: Power Meter works normally with event input taken from Gfx engine. 1: Force event input to weighting logic high every cuclk, overriding event data coming in from Gfx engine. This register is the override for events 33 through 64, where bit 0 corresponds to event 33, and bit 25 corresponds to event 58. "	

PWRMTREVTORM0

PWRMTREVTORM0 - PWRMTREVTORM0	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0AAD4h

GT_CR_POWER_METER_EVENT_OVERRIDE_MEDIA1_32

DWord	Bit	Description
0	31:0	**PMEVORM0**
			Default Value:	00000000h	
			Access:	R/W Lock	
		Power Meter Event Override for Media Events.Allows user to override signal coming in from Gfx engine and count event every cycle on a per event basis. For each event: 0: Power Meter works normally with event input taken from Gfx engine. 1: Force event input to weighting logic high every cuclk, overriding event data coming in from Gfx engine. This register is the override for events 1 through 32, where bit 0 corresponds to event 1, and bit 31 corresponds to event 32. "

PWRMTREVTORM1

PWRMTREVTORM1 - PWRMTREVTORM1	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0AAD8h

GT_CR_POWER_METER_EVENT_OVERRIDE_MEDIA33_36

DWord	Bit	Description
0	31:4	**Reserved**
		Default Value: 00000000h
		Access: RO
		Reserved
	3:0	**PMEVORM1**
		Default Value: 0h
		Access: R/W Lock
		Power Meter Event Override for Media Events.Allows user to override signal coming in from Gfx engine and count event every cycle on a per event basis. For each event: 0: Power Meter works normally with event input taken from Gfx engine. 1: Force event input to weighting logic high every cuclk, overriding event data coming in from Gfx engine. This register is the override for events 33 through 36, where bit 0 corresponds to event 33, and bit 3 corresponds to event 36. "

PWRMTREVTORR0

PWRMTREVTORR0 - PWRMTREVTORR0	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0AAC0h

GT_CR_POWER_METER_EVENT_OVERRIDE_RENDER1_32

DWord	Bit	Description
0	31:0	**PMEVORR0**
		Default Value: 00000000h
		Access: R/W Lock
		Power Meter Event Override for Render Events.Allows user to override signal coming in from Gfx engine and count event every cycle on a per event basis. For each event: 0: Power Meter works normally with event input taken from Gfx engine. 1: Force event input to weighting logic high every cuclk, overriding event data coming in from Gfx engine. This register is the override for events 1 through 32, where bit 0 corresponds to event 1, and bit 31 corresponds to event 32.

PWRMTREVTORR1

PWRMTREVTORR1 - PWRMTREVTORR1

Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32

Address:	0AAC4h

GT_CR_POWER_METER_EVENT_OVERRIDE_RENDER33_64

DWord	Bit	Description
0	31:0	**PMEVORR1**

	Default Value:	00000000h
	Access:	R/W Lock

Power Meter Event Override for Render Events.Allows user to override signal coming in from Gfx engine and count event every cycle on a per event basis.
For each event:
0: Power Meter works normally with event input taken from Gfx engine.
1: Force event input to weighting logic high every cuclk, overriding event data coming in from Gfx engine.
This register is the override for events 33 through 64, where bit 0 corresponds to event 33, and bit 31 corresponds to event 64.

PWRMTREVTORR2


<table>
<tr><td colspan="4" align="center">PWRMTREVTORR2 - PWRMTREVTORR2</td></tr>
<tr><td>Register Space:</td><td colspan="3">MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td colspan="3">CHV, BSW</td></tr>
<tr><td>Source:</td><td colspan="3">PRM</td></tr>
<tr><td>Default Value:</td><td colspan="3">0x00000000</td></tr>
<tr><td>Size (in bits):</td><td colspan="3">32</td></tr>
<tr><td>Address:</td><td colspan="3">0AAC8h</td></tr>
<tr><td colspan="4">GT_CR_POWER_METER_EVENT_OVERRIDE_RENDER65_70</td></tr>
<tr><td>DWord</td><td>Bit</td><td colspan="2">Description</td></tr>
<tr><td>0</td><td>31:6</td><td colspan="2">Reserved
Default Value: 00000000h
Access: RO
Reserved</td></tr>
<tr><td></td><td>5:0</td><td colspan="2">PMEVORR2
Default Value: 00h
Access: R/W Lock
Power Meter Event Override for Render Events.Allows user to override signal coming in from Gfx engine and count event every cycle on a per event basis.
For each event:
0: Power Meter works normally with event input taken from Gfx engine.
1: Force event input to weighting logic high every cuclk, overriding event data coming in from Gfx engine.
This register is the override for events 65 through 70, where bit 0 corresponds to event 65, and bit 5 corresponds to event 70. "</td></tr>
</table>

RAM Clock Gating Control 1

RCGCTL1 - RAM Clock Gating Control 1		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	09410h	
RAM Clock Gating Control Registers.		

DWord	Bit	Description
0	31	**USBunit RAM Clock Gating Disable**
		Access: R/W
		USBunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	30	**VLFunit RAM Clock Gating Disable**
		Access: R/W
		VLFunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	29	**VISunit RAM Clock Gating Disable**
		Access: R/W
		VISunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	28	**STCunit RAM Clock Gating Disable**
		Access: R/W
		STCunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

RCGCTL1 - RAM Clock Gating Control 1

<table>
<tr><td>27</td><td colspan="2">TDSunit RAM Clock Gating Disable</td></tr>
<tr><td></td><td>Access:</td><td>R/W</td></tr>
<tr><td></td><td colspan="2">TDSunit RAM Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</td></tr>
<tr><td>26</td><td colspan="2">VMCunit RAM Clock Gating Disable</td></tr>
<tr><td></td><td>Access:</td><td>R/W</td></tr>
<tr><td></td><td colspan="2">VMCunit RAM Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</td></tr>
<tr><td>25</td><td colspan="2">QRCunit RAM Clock Gating Disable</td></tr>
<tr><td></td><td>Access:</td><td>R/W</td></tr>
<tr><td></td><td colspan="2">QRCunit RAM Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</td></tr>
<tr><td>24</td><td colspan="2">SCunit RAM Clock Gating Disable</td></tr>
<tr><td></td><td>Access:</td><td>R/W</td></tr>
<tr><td></td><td colspan="2">SCunit RAM Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</td></tr>
<tr><td>23</td><td colspan="2">SVLunit RAM Clock Gating Disable</td></tr>
<tr><td></td><td>Access:</td><td>R/W</td></tr>
<tr><td></td><td colspan="2">SVLunit RAM Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</td></tr>
<tr><td>22</td><td colspan="2">VFunit RAM Clock Gating Disable</td></tr>
<tr><td></td><td>Access:</td><td>R/W</td></tr>
<tr><td></td><td colspan="2">VFunit RAM Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</td></tr>
</table>

RCGCTL1 - RAM Clock Gating Control 1

	21	**URBunit RAM Clock Gating Disable**	
		Access:	R/W
		URBunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	20	**GAMWunit RAM Clock Gating Disable**	
		Access:	R/W
		GAMWunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	19	**SVGunit RAM Clock Gating Disable**	
		Access:	R/W
		SVGunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	18	**RCZunit RAM Clock Gating Disable**	
		Access:	R/W
		RCZunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	17	**RCPBEunit RAM Clock Gating Disable**	
		Access:	R/W
		RCPBEunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	16	**RCCunit RAM Clock Gating Disable**	
		Access:	R/W
		RCCunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	

RCGCTL1 - RAM Clock Gating Control 1

15	**PSDunit RAM Clock Gating Disable**	
	Access:	R/W

PSDunit RAM Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

14	**MTunit RAM Clock Gating Disable**	
	Access:	R/W

MTunit RAM Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

13	**SBEunit RAM Clock gating Disable**	
	Access:	R/W

SBEunit RAM Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

12	**IZunit RAM Clock Gating Disable**	
	Access:	R/W

IZunit RAM Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

11	**Reserved**	
	Access:	R/W

10	**ICunit RAM Clock Gating Disable**	
	Access:	R/W

ICunit RAM Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

9	**HIZunit RAM Clock Gating Disable**	
	Access:	R/W

HIZunit RAM Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

RCGCTL1 - RAM Clock Gating Control 1

	8	**GAMunit RAM Clock Gating Disable**	
		Default Value:	0b
		Access:	R/W

GAMunit RAM Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

	7	**BCunit RAM Clock Gating Disable**	
		Access:	R/W

BCunit RAM Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

	6	**HDCunit RAM Clock Gating Disable**	
		Access:	R/W

GAFSunit RAM Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

	5	**DMunit RAM Clock Gating Disable**	
		Access:	R/W

DMunit RAM Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

	4	**WMFEunit RAM Clock Gating Disable**	
		Access:	R/W

WMFEunit RAM Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

	3	**CSunit RAM Clock Gating Disable**	
		Access:	R/W

CSunit RAM Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

RCGCTL1 - RAM Clock Gating Control 1

	2	**BLBunit RAM Clock Gating Disable**	
		Access:	R/W
		BLBunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	1	**MPCunit RAM Clock Gating Disable**	
		Access:	R/W
		MPCunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	0	**BFunit RAM Clock Gating Disable**	
		Access:	R/W
		BFunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	

RAM Clock Gating Control 1

<table>
<tr><td colspan="3" align="center">**RCGCTL1 - RAM Clock Gating Control 1**</td></tr>
<tr><td colspan="3">Register Space: MMIO: 0/2/0</td></tr>
<tr><td colspan="3">Project: CHV, BSW</td></tr>
<tr><td colspan="3">Source: PRM</td></tr>
<tr><td colspan="3">Default Value: 0x00000100</td></tr>
<tr><td colspan="3">Size (in bits):   32</td></tr>
<tr><td colspan="3">Address: 09410h</td></tr>
<tr><td colspan="3">RAM Clock Gating Control Registers.</td></tr>
</table>

DWord	Bit	Description
0	31	**USBunit RAM Clock Gating Disable** Access: R/W USBunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	30	**VLFunit RAM Clock Gating Disable** Access: R/W VLFunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	29	**VISunit RAM Clock Gating Disable** Access: R/W VISunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	28	**STCunit RAM Clock Gating Disable** Access: R/W STCunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

RCGCTL1 - RAM Clock Gating Control 1

21	**URBunit RAM Clock Gating Disable**	
	Access:	R/W

URBunit RAM Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

20	**GAMWunit RAM Clock Gating Disable**	
	Access:	R/W

GAMWunit RAM Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

19	**SVGunit RAM Clock Gating Disable**	
	Access:	R/W

SVGunit RAM Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

18	**RCZunit RAM Clock Gating Disable**	
	Access:	R/W

RCZunit RAM Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

17	**RCPBEunit RAM Clock Gating Disable**	
	Access:	R/W

RCPBEunit RAM Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

16	**RCCunit RAM Clock Gating Disable**	
	Access:	R/W

RCCunit RAM Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

RCGCTL1 - RAM Clock Gating Control 1

	8	**GAMunit RAM Clock Gating Disable**		
		Default Value:		1b
		Access:		R/W
		GAMunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
	7	**BCunit RAM Clock Gating Disable**		
		Access:		R/W
		BCunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
	6	**HDCunit RAM Clock Gating Disable**		
		Access:		R/W
		GAFSunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
	5	**DMunit RAM Clock Gating Disable**		
		Access:		R/W
		DMunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
	4	**WMFEunit RAM Clock Gating Disable**		
		Access:		R/W
		WMFEunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
	3	**CSunit RAM Clock Gating Disable**		
		Access:		R/W
		CSunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		

RCGCTL1 - RAM Clock Gating Control 1

	2	**BLBunit RAM Clock Gating Disable**	
		Access:	R/W
		BLBunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	1	**MPCunit RAM Clock Gating Disable**	
		Access:	R/W
		MPCunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	0	**BFunit RAM Clock Gating Disable**	
		Access:	R/W
		BFunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	

RAM Clock Gating Control 2

DWord	Bit	Description
		**RCGCTL2 - RAM Clock Gating Control 2**

Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x7FC00000
Size (in bits):	32

Address:	09414h

RAM Clock Gating Control Registers.

DWord	Bit	Description
0	31	**SPARE 2 clock gate disable**
		Access: / R/W
		SPARE 2 unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	30:28	**VMCRunit clock gate disable**
		Default Value: / 111b
		Access: / R/W
		VMCR unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	27:25	**SMCRunit clock gate disable**
		Default Value: / 111b
		Access: / R/W
		SMCR unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	24:22	**MCRunit clock gate disable**
		Default Value: / 111b
		Access: / R/W
		MCR unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

RCGCTL2 - RAM Clock Gating Control 2

	21	**Reserved**	

	20	**WVISunit clock gate disable**	
		Access:	R/W

WVIS unit RAM Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

	19	**WAVM unit RAM clock gate disable**	
		Access:	R/W

WAVM unit RAM Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

	18	**WHME unit RAM clock gate disable bit**	
		Access:	R/W

WHME unit RAM Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

	17	**WIME unit RAM clock gate disable**	
		Access:	R/W

WIME unit RAM Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

	16	**WMPC unit RAM clock gating disable**	
		Access:	R/W

WMPC unit RAM Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

	15	**SDEunit RAM clock gate disable**	
		Access:	R/W

SDE unit RAM Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

RCGCTL2 - RAM Clock Gating Control 2

	14	**VSHM unit clock gate disable**		
		Access:		R/W
		VSHM unit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
	13	**DAPRTS unit RAM clock gate disable**		
		Access:		R/W
		DAPRTS unit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled.		
	12	**GS unit RAM clock gate disable**		
		Access:		R/W
		GS unit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
	11	**Reserved**		
	10	**GAMTunit RAM clock gate disable bit**		
		Access:		R/W
		GAMT unit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
	9	**VCW unit RAM clock gate disable**		
		Access:		R/W
		VCW unit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
	8	**VEO unit RAm clock gate disable**		
		Access:		R/W
		VEO unit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		

RCGCTL2 - RAM Clock Gating Control 2

	7	**IMEunit RAM clock gate disable**	
		Access:	R/W
		IMEunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	6	**CREunit RAM clock gate disable**	
		Access:	R/W
		CREunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	5	**RSunit RAM clock gate disable**	
		Access:	R/W
		RSunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	4	**MSCunit RAM Clock Gating Disable**	
		Access:	R/W
		MSCunit RAM Clock Gating Disable Control '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	3	**VMXunit RAM Clock Gating Disable**	
		Access:	R/W
		VMXunit RAM Clock Gating Disable Control '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	2	**GAunit RAM Clock Gating Disable for all EUs**	
		Access:	R/W
		GAunit RAM Clock Gating Disable Control For all EUs in each Row: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	

RCGCTL2 - RAM Clock Gating Control 2

	1	**VSunit RAM Clock Gating Disable**

Access:	R/W

VSunit RAM Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

	0	**HSunit RAM Clock Gating Disable**

Access:	R/W

HSunit RAM Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

RAM Clock Gating Control 2

RCGCTL2 - RAM Clock Gating Control 2		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0xFFC00000	
Size (in bits):	32	
Address:	09414h	
RAM Clock Gating Control Registers.		

DWord	Bit	Description
0	31	**1x2X Assign fub XOR clock gate disable**
		Default Value: · · · 1b
		Access: · · · R/W
		XOR based unit level clock gating disable in 1x2x_asgn fub: '0' : XOR Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : XOR Clock Gating Disabled. (i.e., clocks are toggling, always)
	30:28	**VMCRunit clock gate disable**
		Default Value: · · · 111b
		Access: · · · R/W
		VMCR unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	27:25	**SMCRunit clock gate disable**
		Default Value: · · · 111b
		Access: · · · R/W
		SMCR unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	24:22	**MCRunit clock gate disable**
		Default Value: · · · 111b
		Access: · · · R/W
		MCR unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

RCGCTL2 - RAM Clock Gating Control 2

	21	**MUCunit RAM clock gate disable**	
		Access:	R/W
		MUC unit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	20	**WVISunit clock gate disable**	
		Access:	R/W
		WVIS unit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	19	**WAVM unit RAM clock gate disable**	
		Access:	R/W
		WAVM unit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	18	**WHME unit RAM clock gate disable bit**	
		Access:	R/W
		WHME unit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	17	**WIME unit RAM clock gate disable**	
		Access:	R/W
		WIME unit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	16	**WMPC unit RAM clock gating disable**	
		Access:	R/W
		WMPC unit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	

RCGCTL2 - RAM Clock Gating Control 2

	15	**SDEunit RAM clock gate disable**	
		Access:	R/W
		SDE unit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	14	**VSHM unit clock gate disable**	
		Access:	R/W
		VSHM unit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	13	**DAPRTS unit RAM clock gate disable**	
		Access:	R/W
		DAPRTS unit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled.	
	12	**GS unit RAM clock gate disable**	
		Access:	R/W
		GS unit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	11	**Reserved**	
		Access:	R/W
	10	**GAMTunit RAM clock gate disable bit**	
		Access:	R/W
		GAMT unit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	9	**VCW unit RAM clock gate disable**	
		Access:	R/W
		VCW unit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	

RCGCTL2 - RAM Clock Gating Control 2

	8	**VEO unit RAm clock gate disable**	
		Access:	R/W
		VEO unit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	7	**IMEunit RAM clock gate disable**	
		Access:	R/W
		IMEunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	6	**CREunit RAM clock gate disable**	
		Access:	R/W
		CREunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	5	**RSunit RAM clock gate disable**	
		Access:	R/W
		RSunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	4	**MSCunit RAM Clock Gating Disable**	
		Access:	R/W
		MSCunit RAM Clock Gating Disable Control '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	3	**VMXunit RAM Clock Gating Disable**	
		Access:	R/W
		VMXunit RAM Clock Gating Disable Control '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	

RCGCTL2 - RAM Clock Gating Control 2

	2	**GAunit RAM Clock Gating Disable for all EUs**		
		Access:		R/W
		GAunit RAM Clock Gating Disable Control For all EUs in each Row: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
	1	**VSunit RAM Clock Gating Disable**		
		Access:		R/W
		VSunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
	0	**HSunit RAM Clock Gating Disable**		
		Access:		R/W
		HSunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		

RAM Clock Gating Control 3

RCGCTL3 - RAM Clock Gating Control 3		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	09434h	

DWord	Bit	Description
0	31:13	**RSVD** Access: RO Reserved
	12	**cp_ramcgdis_huc** Access: R/W HUC unit Clock Gating Disable (cp_ramcgdis_huc) HUC unit Clock Gating Disable Control '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	11	**cp_ramcgdis_hwm** Access: R/W HWM unit Clock Gating Disable (cp_ramcgdis_hwm) HWM unit Clock Gating Disable Control '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	10	**cp_ramcgdis_hed** Access: R/W HED unit Clock Gating Disable (cp_ramcgdis_hed) HED unit Clock Gating Disable Control '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	9	**cp_ramcgdis_hpp** Access: R/W HPP unit Clock Gating Disable (cp_ramcgdis_hpp) HPP unit Clock Gating Disable Control '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

RCGCTL3 - RAM Clock Gating Control 3

<table>
<tr>
<td>8</td>
<td colspan="2">cp_ramcgdis_hpr</td>
</tr>
<tr>
<td></td>
<td>Access:</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td colspan="2">HPR unit Clock Gating Disable (cp_ramcgdis_hpr)
HPR unit Clock Gating Disable Control
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</td>
</tr>
<tr>
<td>7</td>
<td colspan="2">cp_ramcgdis_hmc</td>
</tr>
<tr>
<td></td>
<td>Access:</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td colspan="2">HMC unit Clock Gating Disable (cp_ramcgdis_hmc)
HMC unit Clock Gating Disable Control
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</td>
</tr>
<tr>
<td>6</td>
<td colspan="2">cp_ramcgdis_hlf</td>
</tr>
<tr>
<td></td>
<td>Access:</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td colspan="2">HLF unit Clock Gating Disable (cp_ramcgdis_hlf)
HLF unit Clock Gating Disable Control
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</td>
</tr>
<tr>
<td>5</td>
<td colspan="2">cp_ramcgdis_hmx</td>
</tr>
<tr>
<td></td>
<td>Access:</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td colspan="2">HMX unit Clock Gating Disable (cp_ramcgdis_hmx)
HMX unit Clock Gating Disable Control
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</td>
</tr>
<tr>
<td>4</td>
<td colspan="2">cp_ramcgdis_vmm</td>
</tr>
<tr>
<td></td>
<td>Access:</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td colspan="2">VMM unit Clock Gating Disable (cp_ramcgdis_vmm)
VMM unit Clock Gating Disable Control
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</td>
</tr>
</table>

RCGCTL3 - RAM Clock Gating Control 3

		3	**cp_ramcgdis_mpd**	
			Access:	R/W
			MPD unit Clock Gating Disable (cp_ramcgdis_mpd) MPD unit Clock Gating Disable Control '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
		2	**cp_ramcgdis_mbd**	
			Access:	R/W
			MBD unit Clock Gating Disable (cp_ramcgdis_mbd) MBD unit Clock Gating Disable Control '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
		1	**cp_ramcgdis_mmx**	
			Access:	R/W
			MMX unit Clock Gating Disable (cp_ramcgdis_mmx) MMX unit Clock Gating Disable Control '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
		0	**cp_ramcgdis_vmpc**	
			Access:	R/W
			VMPC unit Clock Gating Disable (cp_ramcgdis_vmpc) VMPC unit Clock Gating Disable Control '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	

RC6 Wake Rate Limit

RCXWRL - RC6 Wake Rate Limit	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0A09Ch-0A09Fh

DWord	Bit	Description	
0	31:16	**RC6WRL**	
		Access:	R/W
		RC Promotion Time Modulated by wake rate limits when using EI method: Even though the RC6 promotion time is met, if the wake limit is exceeded, no promotion pmcr_rc6_wake_rate_limit[15:0]	
	15:0	**Reserved**	
		Access:	RO

RCC LRA 0

RCC_LRA_0 - RCC LRA 0		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x7F403F00	
Size (in bits):	32	
Address:	04A40h	

DWord	Bit	Description	
0	31:24	**RCC LRA1 Max**	
		Default Value:	01111111b
		Access:	R/W
		Maximum value of programmable LRA1.	
	23:16	**RCC LRA1 Min**	
		Default Value:	01000000b
		Access:	R/W
		Minimum value of programmable LRA1.	
	15:8	**RCC LRA0 Max**	
		Default Value:	00111111b
		Access:	R/W
		Maximum value of programmable LRA0.	
	7:0	**RCC LRA0 Min**	
		Default Value:	00000000b
		Access:	R/W
		Minimum value of programmable LRA0.	

RCC LRA 1

<table>
<tr>
<td colspan="3" align="center">**RCC_LRA_1 - RCC LRA 1**</td>
</tr>
<tr>
<td>Register Space:</td>
<td colspan="2">MMIO: 0/2/0</td>
</tr>
<tr>
<td>Project:</td>
<td colspan="2">CHV, BSW</td>
</tr>
<tr>
<td>Source:</td>
<td colspan="2">PRM</td>
</tr>
<tr>
<td>Default Value:</td>
<td colspan="2">0x00000001</td>
</tr>
<tr>
<td>Size (in bits):</td>
<td colspan="2">32</td>
</tr>
<tr>
<td>Address:</td>
<td colspan="2">04A44h</td>
</tr>
</table>

DWord	Bit	Description
0	31:2	**Reserved**
		<table><tr><td>Default Value:</td><td>00000000000000000000000000000000b</td></tr><tr><td>Access:</td><td>RO</td></tr></table>
	1	**MSC LRA**
		<table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> Which LRA should MSC use.
	0	**RCC LRA**
		<table><tr><td>Default Value:</td><td>1b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> Which LRA should RCC use.

RCC Virtual page Address Registers

<table>
<tr><td colspan="4" align="center">**RCCTLB_VA - RCC Virtual page Address Registers**</td></tr>
<tr><td>Register Space:</td><td colspan="3">MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td colspan="3">CHV, BSW</td></tr>
<tr><td>Source:</td><td colspan="3">RenderCS</td></tr>
<tr><td>Default Value:</td><td colspan="3">0x00000000</td></tr>
<tr><td>Access:</td><td colspan="3">RO</td></tr>
<tr><td>Size (in bits):</td><td colspan="3">32</td></tr>
<tr><td>Trusted Type:</td><td colspan="3">1</td></tr>
<tr><td>Address:</td><td colspan="3">04A00h-04A03h</td></tr>
<tr><td colspan="4">These registers are directly mapped to the current Virtual Addresses in the RCCTLB (Render Cache for Color TLB).</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td colspan="2">**Description**</td></tr>
<tr><td rowspan="2">0</td><td>31:12</td><td colspan="2">**Address**
<table><tr><td>Project:</td><td>All</td></tr><tr><td>Format:</td><td>GraphicsAddress[31:12]</td></tr></table>Page virtual address.</td></tr>
<tr><td>11:0</td><td colspan="2">**Reserved**
<table><tr><td>Project:</td><td>CHV, BSW</td></tr><tr><td>Format:</td><td>MBZ</td></tr></table></td></tr>
</table>

RC Evaluation Interval

<table>
<tr><td colspan="3" align="center">**RCI - RC Evaluation Interval**</td></tr>
<tr><td>Register Space:</td><td colspan="2">MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td colspan="2">CHV, BSW</td></tr>
<tr><td>Source:</td><td colspan="2">PRM</td></tr>
<tr><td>Default Value:</td><td colspan="2">0x00000000</td></tr>
<tr><td>Size (in bits):</td><td colspan="2">32</td></tr>
<tr><td>Address:</td><td colspan="2">0A0A8h-0A0ABh</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td>**Description**</td></tr>
<tr><td rowspan="2">0</td><td>31:24</td><td>**Reserved**
Access: RO</td></tr>
<tr><td>23:0</td><td>**Render Standby Evaluation Interval**
Access: R/W
0 = 0 usec
1 = 1.28 usec
2 = 2.56 usec
3 = 3.84 usec
FF FFFF = 21.474 sec
pmcr_rc_ei[23:0]</td></tr>
</table>

RC Idle Hysteresis

RCIHYST - RC Idle Hysteresis	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0A0ACh-0A0AFh

DWord	Bit	Description
0	31:24	**Reserved**
		Access: ... RO
	23:0	**RC Idle Hysteresis Detection**
		Access: ... R/W
		Idle intervals must be longer than this value to be considered idle. 0 = 0 usec means disabled 1 = 1.28 usec 2 = 2.56 usec 3 = 3.84 usec FF FFFF = 21.474 sec This must not be set to more than 5ms to prevent the PCU from timing out on an S state entry

RCS_PREEMPTION_HINT

RCS_PREEMPTION_HINT - RCS_PREEMPTION_HINT	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	024BCh

Description
This register contains the Head pointer offset in to the Ring Buffer or the Dword aligned Graphics address in to the Batch Buffer corresponding to either MI_ARB_CHECK called Preemption Hint Address. When Preemption Hint Address is enabled, RCS will honor UHPTR only on parsing MI_ARB_CHK at Preemption Hint Address.
This register contains the Head pointer offset into the Ring Buffer or the Dword aligned Graphics address into the Batch Buffer corresponding to the below listed commands in execlist mode of operation   - MI_ARB_CHECK   - MI_WAIT_FOR_EVENT   - MI_SEMAPHORE_WAIT   3D_PRIMITIVE   - GPGPU_WALKER   - MEDIA_STATE_FLUSH   - PIPE_CONTROL (Only in GPGPU mode of pipeline selection)   - MI_ATOMIC (Post Sync Operation set in GPGPU mode of pipeline selection)   - MI_SEMAPHORE_SIGNAL (Post Sync Operation set in GPGPU mode of pipeline selection)

Programming Notes
Programming Restriction: **This register should NEVER be programmed in functional mode, this should be used only in validation mode to achieve deterministic behavior of UHPTR being sampled by a given MI_ARB_CHECK in command stream. Programmer has to ensure that RCS Preemption Hint register gets programmed before UHPTR is programmed and well before RCS crosses the corresponding execution point. Preemption hint for both RingBuffer and Batch Buffer can't be enabled simultaneously.**
User must ensure the Preempted Hint Address programmed matches either Ring Head Offset or Batch Buffer Graphics Virtual Address and not both of them. User must also ensure the Preempted Hint Address[19:0] programmed matches either Ring Head Offset[19:0] or Batch Buffer Graphics Virtual Address[19:0] and not both of them.

RCS_PREEMPTION_HINT - RCS_PREEMPTION_HINT

DWord	Bit	Description
0	31:2	**Preempted Hint Address**

Project:	CHV, BSW
Format:	U30

This field contains the Head offset in to the Ring Buffer when Preemption Hint is set to Ring Buffer and Dword aligned Graphics Address in to the batch buffer when Preemption Hint is set to Batch Buffer.

	1	**Batch Buffer Preemption Hint**

Project:	CHV, BSW
Format:	Enabled

Value	Name	Description	Project
0h	Disabled	Preemption hint is disabled in batch buffer.	CHV, BSW
1h	Enabled	Preemption hint is enabled in ring buffer and preemption hint address corresponds to the instruction in Batch Buffer.	CHV, BSW

	0	**Ring Preemption Hint**

Project:	CHV, BSW
Format:	Enable

Value	Name	Description	Project
0h	Disable	Preemption hint is disabled in ring buffer.	CHV, BSW
1h	Enabled	Preemption hint is enabled in ring buffer and preemption hint address corresponds to the instruction in Ring Buffer.	CHV, BSW

RCS_PREEMPTION_HINT_UDW

RCS_PREEMPTION_HINT_UDW - RCS_PREEMPTION_HINT_UDW	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	024C8h

This register contains the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space of the Batch Buffer corresponding to MI_ARB_CHECK command called Preemption Hint Address.

Programming Notes
Programming Restriction: **This register should NEVER be programmed in functional mode, this should be used only in validation mode to achieve deterministic behavior of UHPTR being sampled by a given MI_ARB_CHK in command stream.**

DWord	Bit	Description
0	31:16	**Reserved**
		Format: ⎟ MBZ
	15:0	**Preempted Hint Address Upper DWORD**
		Format: ⎟ GraphicsAddress[47:32]
		This field contains the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space of the batch buffer when Preemption Hint is set to Batch Buffer. This field is not valid when Preemption Hint is set to Ring Buffer.

RCS Batch Buffer State Register

RCS_BB_STATE - RCS Batch Buffer State Register
Register Space: MMIO: 0/2/0
Project: CHV, BSW
Source: RenderCS
Default Value: 0x00000000 CHV, BSW
Access: RO
Size (in bits):   32

Address: 02110h

This register contains the attributes of the current batch buffer initiated from the Ring Buffer.

This register should not be written by software. These fields should only get written by a context restore. Software should always set these fields via the MI_BATCH_BUFFER_START command when initiating a batch buffer. This register is saved and restored with context.

DWord	Bit	Description
0	31:9	**Reserved**
		Format: MBZ
	8	**Reserved**
		Format: MBZ
	7	**Resource Streamer Enable**
		Project: CHV, BSW
		Format: U1
		When this bit is set, the Resource Streamer will execute the batch buffer. When this bit is clear the Resource Streamer will not execute the batch buffer.
	6	**Reserved**
	5	**Address Space Indicator**
		Project: CHV, BSW
		Note: This field reflects the effective address space indicator security level and may not be the same as the Address Space Indicator written using MI_BATCH_BUFFER_START.
	4	**Reserved**
		Project: CHV, BSW
		Format: MBZ
	3:0	**Reserved**
		Format: MBZ

For bit 5 (Address Space Indicator):

Value	Name	Description
0h	GGTT **[Default]**	This Batch buffer is located in GGTT memory and is privileged
1h	PPGTT	This Batch buffer is located in PPGTT memory and is non-privileged.

RCS Context Preemption Hint

RCS_CTXID_PREEMPTION_HINT - RCS Context Preemption Hint	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	024CCh
Address:	124CCh-124CFh
Name:	Context ID Preemption Hint
ShortName:	RCS_CTXID_PREEMPTION_HINT_VCSUNIT0
Address:	1A4CCh-1A4CFh
Name:	Context ID Preemption Hint
ShortName:	RCS_CTXID_PREEMPTION_HINT_VECSUNIT
Address:	1C4CCh-1C4CFh
Name:	Context ID Preemption Hint
ShortName:	RCS_CTXID_PREEMPTION_HINT_VCSUNIT1
Address:	224CCh-224CFh
Name:	Context ID Preemption Hint
ShortName:	RCS_CTXID_PREEMPTION_HINT_BCSUNIT

This register contains the Context ID of a context in execlist mode of operation. In execlist mode of operation RCS_PREEMPTION_HINT and RS_PREEMPTION_HINT registers are looked at by Render Command Streamer and Resource Streamer only on executing a context having Context ID that matches with the contents of this register. This register contents are valid and looked at only in execlist mode of operation

Programming Restriction:
This register should NEVER be programmed in functional mode, this must be used only in validation mode to achieve deterministic preemption behavior in execlist mode of operation.

DWord	Bit	Description
0	31:0	**Context ID Preemption Hint**
		Format: U32
		If 0 this field has no effect. If nonzero it indicates the only context ID that can be preempted when execlists are enabled. A preemption attempt when the context ID of the currently executing ring context does not match this field will be ignored.

RC Wake Counter

<table>
<tr><td colspan="3" align="center">**RCWC - RC Wake Counter**</td></tr>
<tr><td>Register Space:</td><td colspan="2">MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td colspan="2">CHV, BSW</td></tr>
<tr><td>Source:</td><td colspan="2">PRM</td></tr>
<tr><td>Default Value:</td><td colspan="2">0x00000000</td></tr>
<tr><td>Size (in bits):</td><td colspan="2">32</td></tr>
<tr><td>Address:</td><td colspan="2">0A0A4h-0A0A7h</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td>**Description**</td></tr>
<tr><td>0</td><td>31:16</td><td>**Wake Counter Render**

Access: RO

Incremented for each wake event , wraps around wake_counter[15:0]</td></tr>
<tr><td></td><td>15:0</td><td>**Wake Counter Media**

Access: RO

Incremented for each wake event , wraps around wake_counter[15:0]</td></tr>
</table>

RCZ Virtual Page Address Registers

RCZTLB_VA - RCZ Virtual Page Address Registers	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	04B00h-04B03h

These registers are directly mapped to the current Virtual Addresses in the RCZTLB (Render Cache for Z (Depth), Hi Z, and Stencil TLB).

DWord	Bit	Description
0	31:12	**Address**
		Format: GraphicsAddress[31:12]
		Page virtual address.
	11:0	**Reserved**
		Format: MBZ

Ready Bit Vector 0 for TLBPEND registers

TLBPEND_RDY0 - Ready Bit Vector 0 for TLBPEND registers		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	04708h-0470Bh	
This register contains the ready bits for entries 0-31 of TLBPEND structure (Cycles pending TLB translation).		
DWord	**Bit**	**Description**
0	31:0	**Ready bits per entry**

Ready Bit Vector 1 for TLBPEND registers

TLBPEND_RDY1 - Ready Bit Vector 1 for TLBPEND registers		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	0470Ch-0470Fh	
This register contains the ready bits for entries 32-63 of TLBPEND structure (Cycles pending TLB translation).		
DWord	**Bit**	**Description**
0	31:0	**Ready bits per entry**

Render C State Control 1

<table>
<tr><td colspan="3" align="center">**RCCTL1 - Render C State Control 1**</td></tr>
<tr><td>Register Space:</td><td colspan="2">MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td colspan="2">CHV, BSW</td></tr>
<tr><td>Source:</td><td colspan="2">PRM</td></tr>
<tr><td>Default Value:</td><td colspan="2">0x00000000</td></tr>
<tr><td>Size (in bits):</td><td colspan="2">32</td></tr>
<tr><td>Address:</td><td colspan="2">0A090h-0A093h</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td>**Description**</td></tr>
<tr><td rowspan="7">0</td><td>31:29</td><td>**Reserved**

Access: RO</td></tr>
<tr><td>28</td><td>**TO - HW RC Promotion (i.e., Depth) Selection**

Access: R/W

0: Timeout method disabled
1: TO method enabled
pmcr_to_enable</td></tr>
<tr><td>27</td><td>**EI - HW RC Promotion (i.e., Depth) Selection**

Access: R/W

0: EI disabled
1: Evaluation Interval (EI) method enabled
pmcr_ei_enable</td></tr>
<tr><td>26:25</td><td>**Reserved**

Access: RO</td></tr>
<tr><td>24</td><td>**Reserved**

Access: R/W</td></tr>
<tr><td>23</td><td>**Reserved**

Access: R/W</td></tr>
<tr><td>22:0</td><td>**Reserved**

Access: RO</td></tr>
</table>

Render forcewake acknowledge

RENFW_ACK - Render forcewake acknowledge		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	1300B4h	

This register contains the per thread force wake acknowledge bits for the Render power well.

DWord	Bit	Description	
0	31:16	**RESERVED**	
		Default Value:	0000h
		Access:	RO
		Reserved.	
	15:0	**FWAKERENDERACK**	
		Default Value:	0000h
		Access:	RO
		Force Wake Render request bits. Driver must poll on the corresponding bit to confirm that the well has woken. For example, if 13_00B0[0] is written to a '1' (along with 13_00B0[16]='1'), then bit0 of this register indicates when the force wake request has been completed.	

Render forcewake request

RENFW_REQ - Render forcewake request	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	1300B0h

This register contains per thread force wake request bits for the Render power Well. The upper 16 bits act as masks for the lower 16 bits. Bit 31 masks bit 15 and bit 16 masks bit 0.

1. Driver writes to GPM force wake request bit. (VV will have a Render(13_00B0(15:0)) and a Media (13_00B8(15:0)) bits.)
2. The GPM responds by writing (via PLINK) to 1300B4[15:0] or 1300BC[15:0] register.
3. Driver polls (1300B4[15:0] and/or 1300BC[15:0])status until 1... indicating that that well has completed wake sequence.

Since the registers are per thread, only the specific bit that was forced should be checked for status.

DWord	Bit	Description	
0	31:16	**FWAKERENDERREQMSK**	
		Default Value:	0000h
		Access:	RO
		Mask bits for lower 16 bits to avoid a read modify/write. If '0', the corresponding bit in [15:0] is not changed. If '1', the corresponding bit in [15:0] is changed to the value in [15:0]	
	15	**FWAKERENDERREQ15**	
		Default Value:	0b
		Access:	R/W
		Force Wake Render request 15.	
	14	**FWAKERENDERREQ14**	
		Default Value:	0b
		Access:	R/W
		Force Wake Render request 14.	
	13	**FWAKERENDERREQ13**	
		Default Value:	0b
		Access:	R/W
		Force Wake Render request 13.	

RENFW_REQ - Render forcewake request

	12	**FWAKERENDERREQ12**	
		Default Value:	0b
		Access:	R/W
		Force Wake Render request 12.	
	11	**FWAKERENDERREQ11**	
		Default Value:	0b
		Access:	R/W
		Force Wake Render request 11.	
	10	**FWAKERENDERREQ10**	
		Default Value:	0b
		Access:	R/W
		Force Wake Render request 10.	
	9	**FWAKERENDERREQ9**	
		Default Value:	0b
		Access:	R/W
		Force Wake Render request 9.	
	8	**FWAKERENDERREQ8**	
		Default Value:	0b
		Access:	R/W
		Force Wake Render request 8.	
	7	**FWAKERENDERREQ7**	
		Default Value:	0b
		Access:	R/W
		Force Wake Render request 7.	
	6	**FWAKERENDERREQ6**	
		Default Value:	0b
		Access:	R/W
		Force Wake Render request 6.	
	5	**FWAKERENDERREQ5**	
		Default Value:	0b
		Access:	R/W
		Force Wake Render request 5.	

RENFW_REQ - Render forcewake request

	4	**FWAKERENDERREQ4**	
		Default Value:	0b
		Access:	R/W
		Force Wake Render request 4.	
	3	**FWAKERENDERREQ3**	
		Default Value:	0b
		Access:	R/W
		Force Wake Render request 3.	
	2	**FWAKERENDERREQ2**	
		Default Value:	0b
		Access:	R/W
		Force Wake Render request 2.	
	1	**FWAKERENDERREQ1**	
		Default Value:	0b
		Access:	R/W
		Force Wake Render request 1.	
	0	**FWAKERENDERREQ0**	
		Default Value:	0b
		Access:	R/W
		Force Wake Render request 0.	

Render Geyserville Mode Control 1

		RPMODECTL1 - Render Geyserville Mode

Register Space: MMIO: 0/2/0
Project: CHV, BSW
Source: PRM
Default Value: 0x00000000
Size (in bits): 32

Address: 0A024h-0A027h

DWord	Bit	Description
0	31:12	**Reserved** Access:
	11	**RP Video Turbo Enable for Media Engine** Access: Refer to bits A024[10:9] for different Media turbo scenarios. Refer to the table in the description for bits A024[10:9].
	10:9	**RP Software Mode Control** Access: 11 - Media_active (8000[6]), Media_done and RPVTENMEDIA(A024[11]) are don't care. Media turbo freq is sele 10 - Media_active (8000[6]), Media_done and RPVTENMEDIA(A024[11]) are don't care. Normal freq(Hard coded 01 - Based on the status either the media-turbo or normal frequency will be selected. If Media_active(8000[6]) is set, Media_done and RPVTENMEDIA(A024[11]) are don't care. Media turbo freq is se Else If RPVTENMEDIA(A024[11]) is 0, Media_done is don't care. Normal freq is selected. Else If RPVTENMEDIA(A024[11]) is 1, Media turbo freq is selected based on internal status. if Media_done is set 00 - Media_active (8000[6]), Media_done and RPVTENMEDIA(A024[11]) are don't care. Current frequency is ma Note: Media is done only when both VCS(8004[0] =1) and VECS(8010[0] = 1) are idle. Media_done = 8004[0] a

pmcr_rpsw_ctl_mode[1]	pmcr_rpsw_ctl_mode[0]	pmmr_media_active	pmcr_rpsw_vten_vcs	pmmr_vcs
A024[10]	A024[9]	8000[4]	A024[11]	8000[1]
1	1	x	x	x
1	0	x	x	x
0	1	1	x	x
0	1	0	0	0
0	1	0	0	1
0	1	0	1	0

Doc Ref # IHD-OS-CHV-BSW-Vol 2c-06.15

RPMODECTL1 - Render Geyserville Mod

0	1	0	1	1
0	0	x	x	x

CHV, BSW description

pmcr_rpsw_ctl_mode[1]	pmcr_rpsw_ctl_mode[0]	pmmr_media_active	pmcr_rpsw_vten_vcs	pmmr_vcs_
A024[10]	A024[9]	8000[6]	A024[11]	8004[0]
1	1	x	x	x
1	0	x	x	x
0	1	1	x	x
0	1	0	0	0
0	1	0	0	1
0	1	0	1	0
0	1	0	1	1
0	0	x	x	x

8	**Mask Bits for Graphics Busyness**
	Access:

Description
Mask Bits for Graphics Busyness (MBGB) and enables MC0 counter: 0: MFX busyness is not counted as part of gfx busyness and media MC0 counter forced to a zero. 1: MFX busyness is counted as part of gfx busyness and media MC0 counter is allowed to count. Both VCS and VECS is counted towards media busyness. BIOS/driver should always set this bit to a one. pmcr_media_mask
Mask Bits for Graphics Busyness (MBGB): 0: MFX busyness is not counted as part of gfx busyness 1: MFX busyness is counted as part of gfx busyness Both VCS and VECS is counted towards media busyness pmcr_media_mask

7	**Render Geyserville HW Controlled Idle Mode Enable**
	Access:

0 - Disables Render Geyserville (RP) function (default).
1 - Turns on the Render Geyserville (RP) function and RP counters are enabled (program enable after counter v

RPMODECTL1 - Render Geyserville Mode

	6	**Reserved**
		Access:
		Reserved

	5:3	**Frequency Increase Utilization Metric Selection**
		Access:

Frequency Increase Utilization Metric selection
The selection of a metric below indicates which one is to be used in making decision. All the metrics should be
More than Busy Max Continuous (BMXC) time must be reached for a frequency increase
More than Busy Max Average (BMXA) at end of Evaluation Interval must be reached for a frequency increase
Less than Idle Min Continuous (IMNC) time must be reached for a frequency Increase
BMXC BMXA IMNC
0 0 0 : no metric enabled
0 0 1 : IMNC metric enabled (0 % val)
0 1 0 : BMXA metric enabled (90 % val)
0 1 1 : reserved
1 0 0 : BMXC metric enabled (10 % val)
1 0 1 : reserved
1 1 0 : reserved
1 1 1 : reserved
pmcr_freq_inc_utimet[2:0]

	2:0	**Frequency Decrease Utilization Metric Selection**
		Access:

The selection of a metric below indicates which one is to be used in making decision. All the metrics should be
Less than Busy Min Continuous must be reached for a frequency decrease
Less than Busy Min Average at end of Evaluation Interval must be reached for a frequency decrease
More than Idle Max Continuous must be reached for a frequency decrease
BMNC BMNA IMXC
0 0 0 : no metric enabled
0 0 1 : IMXC metric enabled (0 % val)
0 1 0 : BMNA metric enabled (100 % val)
0 1 1 : reserved
1 0 0 : BMNC metric enabled (0% val)
1 0 1 : reserved
1 1 0 : reserved
1 1 1 : reserved
pmcr_freq_dec_utimet[2:0]

Render Mode Register for Software Interface

<table>
<tr>
<td colspan="2" align="center">**MI_MODE - Render Mode Register for Software Interface**</td>
</tr>
<tr>
<td>Register Space:</td>
<td>MMIO: 0/2/0</td>
</tr>
<tr>
<td>Project:</td>
<td>CHV, BSW</td>
</tr>
<tr>
<td>Source:</td>
<td>RenderCS</td>
</tr>
<tr>
<td>Default Value:</td>
<td>0x00000000</td>
</tr>
<tr>
<td>Access:</td>
<td>R/W</td>
</tr>
<tr>
<td>Size (in bits):</td>
<td>32</td>
</tr>
<tr>
<td>Address:</td>
<td>0209Ch</td>
</tr>
<tr>
<td>Address:
Name:
ShortName:</td>
<td>1209Ch-1209Fh
Mode Register for Software Interface
MI_MODE_VCSUNIT0</td>
</tr>
<tr>
<td>Address:
Name:
ShortName:</td>
<td>1A09Ch-1A09Fh
Mode Register for Software Interface
MI_MODE_VECSUNIT</td>
</tr>
<tr>
<td>Address:
Name:
ShortName:</td>
<td>1C09Ch-1C09Fh
Mode Register for Software Interface
MI_MODE_VCSUNIT1</td>
</tr>
<tr>
<td>Address:
Name:
ShortName:</td>
<td>2209Ch-2209Fh
Mode Register for Software Interface
MI_MODE_BCSUNIT</td>
</tr>
</table>

The MI_MODE register contains information that controls software interface aspects of the Memory Interface function.

DWord	Bit	Description
0	31:16	**Masks**
		<table><tr><td>Format:</td><td>Mask[15:0]</td></tr></table>
		A 1 in a bit in this field allows the modification of the corresponding bit in Bits 15:0
	15	**Suspend Flush**
		<table><tr><td>Format:</td><td>U1</td></tr></table>
		<table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>0h</td><td>No Delay **[Default]**</td><td>HW will not delay flush, this bit will get cleared by MI_SUSPEND_FLUSH as well</td></tr><tr><td>1h</td><td>Delay Flush</td><td>Suspend flush is active</td></tr></table>

MI_MODE - Render Mode Register for Software Interface

Programming Notes
This should only be written to from the ring using MI_SUSPEND_FLUSH. It is considered undefined if written by software through MMIO

14	**Async Flip Performance mode**

Format:	U1

Value	Name	Description
0h	Performance mode enabled **[Default]**	The stall of the flip event is in the windower
1h	Performance mode disabled	The stall of the flip event is in the command stream

Programming Notes
This bit must be set to '1' on all projects disabling Async Flip Performance mode.
When Async Flip Performance mode is enabled stall is in the Windower allowing the commands following the MI_WAIT_FOR_EVENT to be parsed by command streamer, this breaks the usage model of controlling the display message generation in display engine using MI_LOAD_REGISTER_IMMEDIATE commands from ring buffer.

13	**Flush Performance mode**

Format:	U1

Value	Name	Description
0h	run fast restore **[Default]**	No NonPipelined SV flush.
1h	run slow legacy restore	With NonPipelined SV flush.

12	**Reserved**

Format:	MBZ

11	**Invalidate UHPTR enable**

Format:	Enable

If bit set H/W clears the valid bit of UHPTR (2134h, bit 0) when current active head pointer is equal to UHPTR.

10	**Atomic Read Return for MI_COPY_MEM_MEM**

Project:	CHV, BSW
Format:	U1

Value	Name	Description
0h	Disable **[Default]**	Hardware does a regular memory fence write to complete the write to the destination address before moving to the next instruction.
1h	Enable	Hardware does Atomic Move with Read Return to complete the write to the destination address before moving to the next instruction.

MI_MODE - Render Mode Register for Software Interface

9	**Rings Idle**		

Format:		U1

Read Only Status bit

Value	Name	Description
0h	Not Idle **[Default]**	Parser not Idle or Ring Arbiter not Idle.
1h	Idle	Parser Idle and Ring Arbiter Idle.

Programming Notes
Writes to this bit are not allowed.

8	**Stop Rings**

Format:		U1

Value	Name	Description
0h	**[Default]**	Normal Operation.
1h		Parser is turned off and Ring arbitration is turned off.

Programming Notes
Software must set this bit to force the Rings and Command Parser to Idle. Software must read a 1 in the Ring Idle bit after setting this bit to ensure that the hardware is idle.
Software must clear this bit for Rings to resume normal operation.
Due to known HW issue when Stop Rings occur during execution of a batch buffer, memory access type of the batch buffer is reset and hence on resuming the memory access type can be inconsistent with the desired memory access type. SW must not set/reset Stop Rings to achieve stall and resume function in command streamer execution, however Stop Rings can be used by SW before resetting the engine.

7	**Reserved**

Format:		MBZ

6	**Vertex Shader Timer Dispatch Enable**

Project:		CHV, BSW
Format:		Enable

Value	Name	Description
0h	Disable **[Default]**	Disable the timer for dispatch of single vertices from the vertex shader. Vertex shader will try to collect 2 vertices before a dispatch
1h	Enable	Enable the timer for dispatch of single vertices. Dispatch a single vertex shader thread after the timer expires.

5	**Reserved**

Format:		MBZ

MI_MODE - Render Mode Register for Software Interface

	4:1	**Predicate Enable**		
		Project:		CHV, BSW

This field gets set when "MI_SET_PREDICATE" command is parsed by render command streamer. Predicate Disable is the default mode of operation.

Value	Name	Description
0h	Predicate Disable	Predication is Disabled and RCS will process commands as usual.
1h	Predicate on Result2 clear	Following Commands will be NOOPED by RCS only if the MI_PREDICATE_RESULT_2 is clear.
2h	Predicate on Result2 set	Following Commands will be NOOPED by RCS only if the MI_PREDICATE_RESULT_2 is set.
3h	Predicate on Result clear	Following Commands will be NOOPED by RCS only if the MI_PREDICATE_RESULT is clear.
4h	Predicate on Result set	Following Commands will be NOOPED by RCS only if the MI_PREDICATE_RESULT is set.
5h	Predicate when two or more slices enabled	Following Commands will be NOOPED by RCS only when one slice is enabled, NOOPED when more than one slice is enabled.
6h	Predicate when one or three slices enabled	Following Commands will be Executed by RCS only when two slices are enabled, NOOPED when one or three slices are enabled.
7h	Predicate when one or two slices enabled	Following Commands will be Executed by RCS only when all the three slices are enabled, NOOPED when less than three slices are enabled.
8h-Eh	Reserved	
Fh	Predicate Always	Following Commands will be NOOPED by RCS unconditionally.

Programming Notes
SW must use MI_SET_PREDICATE instead of MMIO access.

	0	**Mask IIR disable**		
		Format:		Disable

Mask IIR disable. Nominally the Interrupt controller masks interrupts in the IIR register if an interrupt acknowledge from the 3gio interface is pending. Setting this bit to a 1 allows interrupts to be visible to the interrupt controller while an interrupt acknowledge is pending.

Render Performance Status 1

RPSTAT1 - Render Performance Status 1	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0A01Ch-0A01Fh

This register reflects real-time values and thus will not have a pre-determined default value out of reset.

DWord	Bit	Description	
0	31:16	**Reserved**	
		Access:	RO
	15	**Last Requested Video Turbo Mode**	
		Access:	RO
		Last Requested Video Turbo Mode (CRTM): 0 = Most recent request was a normal request (from RPNSWREQ) 1 = Most recent request was a Video Turbo request (from RPVSWREQ)	
	14:8	**Reserved**	
		Access:	RO
	7:0	**Reserved**	
		Access:	RO

Render Performance Status Register

RP_STATUS0 - Render Performance Status Register	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0A01Ch

This register reflects real-time values and thus does not have a pre-determined default value out of reset.

DWord	Bit	Description
0	31:20	**Reserved**
		Access: RO
	19:18	**Current Actual Gear Ratio**
		Access: RO
	17:16	**Previous Actual Gear Ratio**
		Access: RO
		Previous Actual Gear Ratio (PAGR).
	15	**Last Requested Video Turbo Mode**
		Access: RO
		Last Requested Video Turbo Mode (CRTM):
		0 = Most recent request was a normal request (from RPNSWREQ).
		1 = Most recent request was a Video Turbo request (from RPVSWREQ).
	14	**Reserved**
		Access: RO
	13:7	**Current Actual GFX Freq**
		Access: RO
		This is the MLC ratio that the core is actually running.
	6:0	**Previous Actual GFX Freq**
		Access: RO
		This is the MLC ratio that the core was actually running before the current actual GFX frequency.

Render Power Clock State Register

R_PWR_CLK_STATE - Render Power Clock State Register	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00000288 CHV, BSW
Access:	R/W
Size (in bits):	32
Address:	020C8h

This register contains the mode selection for configuring render engine to attain desired performance and power requirements for a given context. This register is render context save/restored. This register must be initialized correctly when the context is submitted for the first time. This register is context save/restored as part of Exec-List context image in both Exec-List and Ring-Buffer mode of scheduling. This register contents are valid only when "Enable" bit [31] of the register is set.

Programming Notes
This register must not be programmed directly through CPU MMIO cycle. Exec-List Scheduling Mode: Every context can have its own required render engine configuration by programming this register appropriately in the logical render context image in memory (LRCA) before submitting the context to the execlist submit port. This register must not be programmed using MI_LOAD_REGISTER_IMM command in ring buffer or in batch buffer, however programming "NON-SLM Indication" field through MI_LOAD_REGISTER_IMM is an exception defined below. If a need arises to change the render configuration for a context being executed in HW, Scheduler must preempt the context and update the desired render configuration in the logical render context image in memory and resubmit the context. Only "NON-SLM Indictaion" field in R_PWR_CLK_STATE register is allowed to be modified through MI_LOAD_REGISTER_IMM command in ring_buffer or privileged_batch_buffer. SW must modify only "NON-SLM Indication" field and must ensure to program other fields with the same value as in LRCA. SW must ensure to program PIPECONTROl flush command with CS Stall and HDC Flush prior to programming MI_LOAD_REGISTER_IMM command to modify "NON-SLM Indication" in R_PWR_CLK_STATE register. Example: //R_PWR_CLK_STATE register value in LRCA configured with two slices and NON-SLM indication reset: 0x80005_0000 //SW desires to set NON-SLM Indication filed in ring buffer MI_LOAD_REGISTER_IMM 0x20C8, 0x8005_0100 Ring Buffer Scheduling: This register must be programmed using MI_LOAD_REGISTER_IMM command in the ring buffer. When this register is being programmed to re-configure the number of slices, SW must context save the state before programming this register and restore the state after programming the register via dummy MI_SET_CONTEXT command, this will ensure the existing state is programmed to all the new slices that are powered up, in case of slice shutdown this is not required. EX: MI_SET_CONTEXT → CXTA MI_BATCH_BUFFER_START MI_BATCH_BUFFER_START MI_SET_CONTEXT → CXTB //Dummy Context to save existing render state to be restored latter. MI_LOAD_REGISTER_IMM : R_PWR_CLK_STATE (1 Slice to 3 Slices) // Slice configuration done. MI_SET_CONTEXT → CXTA // Context restore of valid state to all the slices powered up.

R_PWR_CLK_STATE - Render Power Clock State Register

DWord	Bit	Description
0	31	**Power Clock State Enable**

Project:	CHV, BSW
Format:	U1

Value	Name	Description
0h	Power Clock State Disabled	No specific power state set, bits[30:0] are ignored.
1h	Power Clock State Enabled	Power Clock is set and bit[30:0] are valid and have the desired state.

	30:0	**Render Power Clock State**

Project:	CHV, BSW
Format:	Power Clock State Format CHV, BSW

Render Power Meter Counter

RPMCNT - Render Power Meter Counter		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A274h-0A277h	
DWord	**Bit**	**Description**
0	31	**Render Power Meter Counter Overflow**
		Access: RO
	30:0	**Render PWRMTR Counter**
		Access: RO

Render Power Meter Counter No Clear

RPMCNTCLR - Render Power Meter Counter No Clear	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0A28Ch-0A28Fh
Formerly cleared the count and the overflow bit, but now it is just a read-only value.	

DWord	Bit	Description
0	31	**Render Power Meter Counter Overflow No Clear**
		Access: RO
		Formerly cleared the overflow bit, but now it is just a read-only value.
	30:0	**Render PWRMTR Counter No Clear**
		Access: RO
		Formerly cleared the count, but now is just a read-only value.

Render Promotion Timer - RC6

RC6TIMER - Render Promotion Timer - RC6		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A0B8h-0A0BBh	

DWord	Bit	Description
0	31:24	**Reserved**
		Access: RO
	23:0	**RC6 Promote Time**
		Access: R/W
		Absolute time starting from post-hyst idle. 0 = 0 usec 1 = 1.28 usec 2 = 2.56 usec 3 = 3.84 usec FF FFFF = 21.474 sec pmcr_rc6_promotion_time[23:0]

RENDERRC0COUNTER

RENDERRC0COUNTER - RENDERRC0COUNTER	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	138118h

This register contains the total RC0 residency (Render powered on and clocks running) time that Render was in since boot.
SOXi Context Save/Restore : No
The 40-bit HW counter will wrap around. The only clear condition is CZ reset.
When 0x13_8104[15] is set to zero, bits 31:0 of the 40-bit counter are reported. When 0x13_8104[15] is set to one, bits 39:8 of the 40-bit counter are reported.
The units are CZ clock cycles.
It is up to SW to periodically read this register and do a difference from the last time it was read. The primary usage for this register is for power characterization.
0x13_8104[4] controls if this register should count or if it should be gated: 0= clear, 1=count

DWord	Bit	Description	
0	31:0	**RENDERRC0TIME**	
		Default Value:	00000000h
		Access:	RO
		Render RC0 Residency Counter.	

RENDERRC1COUNTER

RENDERRC1COUNTER - RENDERRC1COUNTER	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	138110h

This register contains the total RC1 residency (Render powered on and clock gated) time that Render was in since boot.

SOXi Context Save/Restore : No

The 40-bit HW counter will wrap around. The only clear condition is CZ reset.

When 0x13_8104[15] is set to zero, bits 31:0 of the 40-bit counter are reported. When 0x13_8104[15] is set to one, bits 39:8 of the 40-bit counter are reported.

The units are CZ clock cycles.

It is up to SW to periodically read this register and do a difference from the last time it was read. The primary usage for this register is for power characterization.

0x13_8104[2] controls if this register should count or if it should be gated: 0= clear, 1=count

DWord	Bit	Description	
0	31:0	**RENDERRC1TIME**	
		Default Value:	00000000h
		Access:	RO
		Render RC1 Residency Counter.	

RENDERRC6COUNTER

RENDERRC6COUNTER - RENDERRC6COUNTER	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	138108h

This register contains the total RC6 residency (Render power gated and clock gated) time that Render power well was in since boot. The counter will wrap around.

SOXi Context Save/Restore : No

The time is given in units of CZ clock cycles. The counter will reset on CZ reset going high.

This means that a warm reset will also reset this counter and it will also wrap around when it reaches max with no indication that an overflow occurred.

This register will freeze the count value (stop counting, but not reset) when pmu_gvd_renwakeack_nczfwoh=1. This register will count whenever pmu_gvd_renwakeack_nczfwoh=0.

When 0x13_8104[15] is set to zero, bits 31:0 of the 40-bit counter are reported. When 0x13_8104[15] is set to one, bits 39:8 of the 40-bit counter are reported.

The units are CZ clock cycles.

It is up to SW to periodically read this register and do a difference from the last time it was read. The primary usage for this register is for power characterization.

0x13_8104[0] controls if this register should count or if it should be gated: 0= clear, 1=count.

DWord	Bit	Description	
0	31:0	**RENDERRC6TIME**	
		Default Value:	00000000h
		Access:	RO
		Render Residency Counter.	

Render TLB Control Register

RTCR - Render TLB Control Register		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04260h	
DWord	**Bit**	**Description**
0	31:1	**Reserved**
		Default Value: 0000000000000000000000000000000b
		Access: RO
	0	**Invalidate TLBs on the corresponding Engine**
		Default Value: 0b
		Access: R/W
		SW writes 1 to invalidate the TLBs for the associated engine and HW clears the bit when invalidation is complete. To ensure proper invalidation of the TLBs, SW has to ensure the corresponding engine's HW pipeline is flushed and cleared from all its memory accesses. Otherwise HW cannot guarantee the proper invalidation for TLBs. This bit is self clear.

Render Watchdog Counter

PR_CTR - Render Watchdog Counter	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	02190h
Address:	12190h-12193h
Name:	Watchdog Counter
ShortName:	PR_CTR_VCSUNIT0
Address:	1A190h-1A193h
Name:	Watchdog Counter
ShortName:	PR_CTR_VECSUNIT
Address:	1C190h-1C193h
Name:	Watchdog Counter
ShortName:	PR_CTR_VCSUNIT1
Address:	22190h-22193h
Name:	Watchdog Counter
ShortName:	PR_CTR_BCSUNIT

DWord	Bit	Description
0	31:0	**Counter Value**
		Format: U32
		This register reflects the render watchdog counter value itself. It cannot be written to.

Render Watchdog Counter Threshold

PR_CTR_THRSH - Render Watchdog Counter Threshold	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00150000
Access:	R/W
Size (in bits):	32
Address:	0217Ch
Address:	1217Ch-1217Fh
Name:	Watchdog Counter Threshold
ShortName:	PR_CTR_THRSH_VCSUNIT0
Address:	1A17Ch-1A17Fh
Name:	Watchdog Counter Threshold
ShortName:	PR_CTR_THRSH_VECSUNIT
Address:	1C17Ch-1C17Fh
Name:	Watchdog Counter Threshold
ShortName:	PR_CTR_THRSH_VCSUNIT1
Address:	2217Ch-2217Fh
Name:	Watchdog Counter Threshold
ShortName:	PR_CTR_THRSH_BCSUNIT

DWord	Bit	Description	
0	31:0	**Counter logic Threshold**	
		Default Value:	00150000h
		Format:	U32
		This field specifies the threshold that the hardware checks against for the value of the render clock counter before generating an interrupt. The counter in hardware generates an interrupt when the threshold is reached, rolls over and starts counting again. The interrupt generated is the "Media Hang Notify" interrupt since this watchdog timer is intended primarily to remedy VLD hangs on the main pipeline.	

Reported BitRateControl Convergence Status

MFX_VP8_BRC_CONVERGENCE_STATUS - Reported BitRateControl Convergence Status		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	VideoCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	12928h	
Valid Projects:	CHV, BSW	

This register stores BitRateControl Convergence Status Segmentation support for BRC is not validated in CHV, BSW. Only Segment0 value should be used for CHV, BSW.
Also, this is Read Only register on CHV, BSW A0.

DWord	Bit	Description
0	31	**Segment3 Qindex Polarity Change**
		Format: U1
		This bit indicates current pass has CumulativeDeltaQindex Polarity Change This feature is not validated and should be used for debug purpose only.
	30:28	**Segment3 Num-Pass with Polarity Change**
		Format: U3
		This bit indicates the number of Multipass with CumulativeDeltaQindex Polarity Change in segment3. This feature is not validated and should be used for debug purpose only.
	27	**Segment2 Qindex Polarity Change**
		Format: U1
		This bit indicates current pass has CumulativeDeltaQindex Polarity Change This feature is not validated and should be used for debug purpose only.
	26:24	**Segment2 Num-Pass with Polarity Change**
		Format: U3
		This bit indicates the number of Multipass with CumulativeDeltaQindex Polarity Change in segment2. This feature is not validated and should be used for debug purpose only.
	23	**Segment1 Qindex Polarity Change**
		Format: U1

MFX_VP8_BRC_CONVERGENCE_STATUS - Reported BitRateControl Convergence Status

This bit indicates current pass has CumulativeDeltaQindex Polarity Change This feature is not validated and should be used for debug purpose only.

22:20 Segment1 Num-Pass with Polarity Change

Format:	U3

This bit indicates the number of Multipass with CumulativeDeltaQindex Polarity Change in segment1. This feature is not validated and should be used for debug purpose only.

19 Segment0 Qindex Polarity Change

Format:	U1

This bit indicates current pass has CumulativeDeltaQindex Polarity Change This feature is not validated and should be used for debug purpose only.

18:16 Segment0 Num-Pass with Polarity Change

Format:	U3

This bit indicates the number of Multipass with CumulativeDeltaQindex Polarity Change in segment0. This feature is not validated and should be used for debug purpose only.

15:12 Reserved

Format:	MBZ

11:8 Total Num of Pass

Format:	U4

This bit indicates the number of Multipass including current frame. Note that Initial Pass is not counted.

7:2 Reserved

Format:	MBZ

1 Overflow OR Underflow Flag

Format:	U1

This bit indicates the current frame has BRC overflow OR underflow.

0 MB Max. Conformance Flag

Format:	U1

This contains flag that indicate Inter MB or Intra MB Max. Conformance is not met. This is legacy support and this feature is not validated

Reported BitRateControl CumulativeDeltaLoopFilter and LoopFilter 01

MFX_VP8_BRC_CUMULATIVE_D_LOOP_FILTER01 - Reported BitRateControl CumulativeDeltaLoopFilter and LoopFilter 01	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	12920h
Valid Projects:	CHV, BSW

This register stores per segement Bit Rate Control DeltaLoopFilter. Segmentation support for BRC is not validated in CHV, BSW. Only Segment0 value should be used for CHV, BSW.
Also, this is Read Only register on CHV, BSW A0

DWord	Bit	Description
0	31	**Reserved**
		Format: MBZ
	23:22	**Reserved**
		Format: MBZ
	15	**Reserved**
		Format: MBZ
	14:8	**Segment0 CumulativeDeltaLoopFilter**
		Format: S6
		This contains Segment0 CumulativeDeltaLoopFilter in Bit Rate Control. It accumulates all Segment0 DeltaQindices per pass in Multipass. This register is valid after a BRC pass is done. If Segmentation is not enabled, this field reflects CumulativeDeltaLoopFilter. If Segmentation is enabled, this field reflects Segment0 CumulativeDeltaLoopFilter.
	7:6	**Reserved**
		Format: MBZ
	5:0	**Segment0 LoopFilter**
		Format: U6
		This contains Segment0 LoopFilter used in current frame. This register is valid after a BRC pass is done. If Segmentation is not enabled, this field reflects LoopFilter. If Segmentation is enabled, this field reflects Segment0 LoopFilter.

Reported BitRateControl CumulativeDeltaLoopFilter and LoopFilter 23

<table>
<tr><td colspan="3" align="center">**MFX_VP8_BRC_CUMULATIVE_D_LOOP_FILTER23 - Reported BitRateControl CumulativeDeltaLoopFilter and LoopFilter 23**</td></tr>
<tr><td colspan="3">Register Space: MMIO: 0/2/0</td></tr>
<tr><td colspan="3">Project: CHV, BSW</td></tr>
<tr><td colspan="3">Source: VideoCS</td></tr>
<tr><td colspan="3">Default Value: 0x00000000</td></tr>
<tr><td colspan="3">Access: R/W</td></tr>
<tr><td colspan="3">Size (in bits):   32</td></tr>
<tr><td colspan="3">Trusted Type: 1</td></tr>
<tr><td colspan="3">This register stores per segement Bit Rate Control DeltaLoopFilter. Segmentation support for BRC is not validated in CHV, BSW. Only Segment0 value should be used for CHV, BSW.
Also, this is Read Only register for CHV, BSW A0.</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td>**Description**</td></tr>
<tr><td>0</td><td>31</td><td>**Reserved**
Format: MBZ</td></tr>
<tr><td></td><td>30:24</td><td>**Segment3 CumulativeDeltaLoopFilter**
Format: S6
This contains Segment3 CumulativeDeltaLoopFilter in Bit Rate Control. It accumulates all Segment3 DeltaQindices per pass in Multipass. This register is valid after a BRC pass is done.</td></tr>
<tr><td></td><td>23:22</td><td>**Reserved**
Format: MBZ</td></tr>
<tr><td></td><td>21:16</td><td>**Segment3 LoopFilter**
Format: U6
This contains Segment3 LoopFilter used in current frame. This register is valid after a BRC pass is done.</td></tr>
<tr><td></td><td>15</td><td>**Reserved**</td></tr>
<tr><td></td><td>14:8</td><td>**Segment2 CumulativeDeltaLoopFilter**
Format: S6
This contains Segment2 CumulativeDeltaLoopFilter in Bit Rate Control. It accumulates all Segment2 DeltaQindices per pass in Multipass. This register is valid after a BRC pass is done.</td></tr>
<tr><td></td><td>7:6</td><td>**Reserved**</td></tr>
<tr><td></td><td>5:0</td><td>**Segment2 LoopFilter**
Format: U6
This contains Segment2 LoopFilter used in current frame. This register is valid after a BRC pass is done.</td></tr>
</table>

Reported BitRateControl CumulativeDeltaQindex and Qindex 01

MFX_VP8_BRC_CUMULATIVE_DQ_INDEX01 - Reported BitRateControl CumulativeDeltaQindex and Qindex 01	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	12918h
Valid Projects:	CHV, BSW

This register stores per segement Bit Rate Control CumulativeDeltaQindex and Qindex Segmentation support for BRC is not validated in CHV, BSW. Only Segment0 value should be used for CHV, BSW.
Also, this register is Read Only on CHV, BSW A0

DWord	Bit	Description		
0	31:24	**Reserved**		
		Project:	CHV, BSW	
		Format:	MBZ	
	23	**Reserved**		
		Format:		MBZ
	22:16	**Reserved**		
		Project:	CHV, BSW	
		Format:	MBZ	
	15:8	**Segment0 CumulativeDeltaQindex**		
		Format:		S7
		TThis contains Segment0 CumulativeDeltaQindex in Bit Rate Control. It accumulates all Segment0 DeltaQindices per pass in Multipass. This register is valid after a BRC pass is done. If Segmentation is not enabled, this field reflects CumulativeDeltaQindex. If Segmentation is enabled, this field reflects Segment0 CumulativeDeltaQindex.		
	7	**Reserved**		
		Format:		MBZ
	6:0	**Segment0 Qindex**		
		Format:		U7
		This contains Segment0 Qindex used in current frame. This register is valid after a BRC pass is done. If Segmentation is not enabled, this field reflects Qindex. If Segmentation is enabled, this field reflects Segment0 Qindex.		

Reported BitRateControl CumulativeDeltaQindex and Qindex 23

<table>
<tr>
<td colspan="3" align="center">**MFX_VP8_BRC_CUMULATIVE_DQ_INDEX23 - Reported BitRateControl CumulativeDeltaQindex and Qindex 23**</td>
</tr>
<tr>
<td colspan="3">Register Space: MMIO: 0/2/0</td>
</tr>
<tr>
<td colspan="3">Project: CHV, BSW</td>
</tr>
<tr>
<td colspan="3">Source: VideoCS</td>
</tr>
<tr>
<td colspan="3">Default Value: 0x00000000</td>
</tr>
<tr>
<td colspan="3">Access: R/W</td>
</tr>
<tr>
<td colspan="3">Size (in bits):   32</td>
</tr>
<tr>
<td colspan="3">Trusted Type: 1</td>
</tr>
<tr>
<td colspan="3">This register stores per segement Bit Rate Control CumulativeDeltaQindex and Qindex Segmentation support for BRC is not validated in CHV, BSW. Only Segment0 value should be used for CHV, BSW.
Also, this is Read Only register on CHV, BSW A0.</td>
</tr>
</table>

DWord	Bit	Description
0	31:24	**Segment3 CumulativeDeltaQindex** Format: .... S7 This contains Segment3 CumulativeDeltaQindex in Bit Rate Control. It accumulates all Segment3 DeltaQindices per pass in Multipass. This register is valid after a BRC pass is done.
	23	**Reserved** Format: .... MBZ
	22:16	**Segment3 Qindex** Format: .... U7 This contains Segment3 Qindex used in current frame. This register is valid after a BRC pass is done.
	15:8	**Segment2 CumulativeDeltaQindex** Format: .... S7 This contains Segment2 CumulativeDeltaQindex in Bit Rate Control. It accumulates all Segment2 DeltaQindices per pass in Multipass. This register is valid after a BRC pass is done.
	7	**Reserved** Format: .... MBZ
	6:0	**Segment2 Qindex** Format: .... U7 This contains Segment2 Qindex used in current frame. This register is valid after a BRC pass is done.

Reported BitRateControl DeltaLoopFilter

MFX_VP8_BRC_D_LOOP_FILTER - Reported BitRateControl DeltaLoopFilter	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	12914h
Valid Projects:	CHV, BSW

This register stores per segement Bit Rate Control DeltaLoopFilter. Segmentation support for BRC is not validated in CHV, BSW. Only Segment0 value should be used for CHV, BSW

DWord	Bit	Description
0	31	**Reserved**
		Format: MBZ
	23	**Reserved**
		Format: MBZ
	15	**Reserved**
		Format: MBZ
	7	**Reserved**
		Format: MBZ
	6:0	**Segment0 DeltaLoopFilter**
		Format: S6
		This contains Segment0 DeltaLoopFilter in Bit Rate Control. This register is valid after a BRC pass is done. If Segmentation is not enabled, this field reflects DeltaLoopFilter. If Segmentation is enabled, this field reflects Segment0 DeltaLoopFilter.

Reported BitRateControl DeltaQindex

MFX_VP8_BRC_DQ_INDEX - Reported BitRateControl DeltaQindex	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	12910h
Valid Projects:	CHV, BSW

This register stores per segement Bit Rate Control DeltaQindex. Segmentation support for BRC is not validated in CHV, BSW. Only Segment0 value should be used for CHV, BSW

DWord	Bit	Description
0	7:0	**Segment0 DeltaQindex**

Format:	S7

This contains Segment0 DeltaQindex in Bit Rate Control. This register is valid after a BRC pass is done. If Segmentation is not enabled, this field reflects DeltaQindex. If Segmentation is enabled, this field reflects Segment0 DeltaQindex.

Reported BitRateControl parameter Mask

MFX_VP8_CNTRL_MASK - Reported BitRateControl parameter Mask	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	12900h
Valid Projects:	CHV, BSW

This register stores the count of bytes of the bitstream output per frame

DWord	Bit	Description
0	31:6	**Reserved** Format: MBZ
	5	**Final Bitstream Buffer Overrun Mask** Format: U1 This is same bit reflected in MFX_VP8_ENC_CFG DW2 bit5. This denotes Final bitstream buffer overrun feature is enabled.
	4	**Intermediate Bitstream Buffer Overrun Mask** Format: U1 This is same bit reflected in MFX_VP8_ENC_CFG DW2 bit4. This denotes intermediate bitstream buffer overrun feature is enabled.
	3	**Intra MB Bit Count Conformance Mask** Format: U1 This is legacy support as AVC for Intra MB Bit Count conformance. This is same bit reflected in MFX_VP8_ENC_CFG DW2 bit3. This feature is not validated.
	2	**Inter MB Bit Count Conformance Mask** Format: U1 This is legacy support as AVC for Inter MB Bit Count conformance. This is same bit reflected in MFX_VP8_ENC_CFG DW2 bit2. This feature is not validated.

MFX_VP8_CNTRL_MASK - Reported BitRateControl parameter Mask

	1	**Frame Bit Rate Overflow Mask**	
		Format:	U1
		This is same bit reflected in MFX_VP8_ENC_CFG DW2 bit0. It denotes if Frame Bit Rate Overflow is enabled for Bit Rate Control	
	0	**Frame Bit Rate Underflow Mask**	
		Format:	U1
		This is same bit reflected in MFX_VP8_ENC_CFG DW2 bit1. It denotes if Frame Bit Rate Underflow is enabled for Bit Rate Control	

Reported BitRateControl parameter Status

MFX_VP8_CNTRL_STATUS - Reported BitRateControl parameter Status		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	VideoCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	12904h	
Valid Projects:	CHV, BSW	

This register stores the count of bytes of the bitstream output per frame

DWord	Bit	Description
0	31:8	**Reserved**
		Format: MBZ
	7	**QindexClampHigh Status**
		Format: U1
		This denotes if Qindex is clamped by QindexClampHigh value programmed in MFX_VP8_PIC_STATE.DW7.
	6	**QindexClampLow Status**
		Format: U1
		This denotes if Qindex is clamped by QindexClampLow value programmed in MFX_VP8_PIC_STATE.DW7.
	5	**Final Bitstream Buffer Overrun Status**
		Format: U1
		This denotes if Final bitstream buffer overrun.
	4	**Intermediate Bitstream Buffer Overrun Status**
		Format: U1
		This denotes if any of the Intermediate bitstream buffer overrun. (including FrameHeader, Partition1 to Partition8)
	3	**Intra MB Bit Count Conformance Status**
		Format: U1
		This is legacy support as AVC for Intra MB Bit Count conformance. It denotes if Intra MB Bit Count meets conformance size. This feature is not validated.

MFX_VP8_CNTRL_STATUS - Reported BitRateControl parameter Status

	2	**Inter MB Bit Count Conformance Status**	
		Format:	U1
		This is legacy support as AVC for Inter MB Bit Count conformance. It denotes if Inter MB Bit Count meets conformance size. This feature is not validated.	
	1	**Frame Bit Rate Overflow Status**	
		Format:	U1
		It denotes if Frame Bit Rate Overflow in current frame	
	0	**Frame Bit Rate Underflow Status**	
		Format:	U1
		It denotes if Frame Bit Rate Underflow in current frame	

Reported Bitstream Output Bit Count for Syntax Elements Only Register

<table>
<tr>
<td colspan="2">MFC_BITSTREAM_SE_BITCOUNT_FRAME - Reported Bitstream Output Bit Count for Syntax Elements Only Register</td>
</tr>
<tr>
<td>Register Space:</td>
<td>MMIO: 0/2/0</td>
</tr>
<tr>
<td>Project:</td>
<td>CHV, BSW</td>
</tr>
<tr>
<td>Source:</td>
<td>VideoCS</td>
</tr>
<tr>
<td>Default Value:</td>
<td>0x00000000</td>
</tr>
<tr>
<td>Access:</td>
<td>RO</td>
</tr>
<tr>
<td>Size (in bits):</td>
<td>32</td>
</tr>
<tr>
<td>Trusted Type:</td>
<td>1</td>
</tr>
<tr>
<td>Address:</td>
<td>128A4h</td>
</tr>
<tr>
<td>Valid Projects:</td>
<td>CHV, BSW</td>
</tr>
</table>

This register stores the count of number of bits in the bitstream due to syntax elements only. This excludes header/ byte alignment /tail/EMU/CABAC-0word/padding bits but includes the stop-one-bit. This register is part of the context save and restore.

DWord	Bit	Description
0	31:0	**MFC Bitstream Syntax Element Only Bit Count** Total number of bits in the bitstream output due to syntax elements only. It includes the data bytes only. This count is updated for every time the internal bitstream counter is incremented and its reset at image start.

Reported Bitstream Output Byte Count per Frame Register

MFC_BITSTREAM_BYTECOUNT_FRAME - Reported Bitstream Output Byte Count per Frame Register	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	128A0h
Valid Projects:	CHV, BSW

This register stores the count of bytes of the bitstream output per frame

DWord	Bit	Description
0	31:0	**MFC Bitstream Byte Count per Frame** Total number of bytes in the bitstream output per frame from the encoder. This includes header/tail/byte alignment/data bytes/EMU (emulation) bytes/cabac-zero word insertion/padding insertion. This count is updated for every time the internal bitstream counter is incremented and its reset at image start.

Reported Bitstream Output CABAC Bin Count Register

MFC_AVC_CABAC_BIN_COUNT_FRAME - Reported Bitstream Output CABAC Bin Count Register	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	128A8h
Valid Projects:	CHV, BSW

This register stores the count of number of bins per frame.

DWord	Bit	Description
0	31:0	**MFC AVC Cabac Bin Count** Total number of BINs in the bitstream output per frame from the encoder. This count is updated for every time the bin counter is incremented and its reset at image start.

Reported Final Bitstream Byte Count

MFX_VP8_FRM_BYTE_CNT - Reported Final Bitstream Byte Count	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	12908h
Valid Projects:	CHV, BSW

This register stores the count of bytes of the bitstream output per frame

DWord	Bit	Description
0	31:0	**Final BitStream Byte Count**
		Format: U32
		This register contains Final Bitstream byte count

Reported Frame Zero Padding Byte Count

MFX_VP8_FRM_ZERO_PAD - Reported Frame Zero Padding Byte Count	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	1290Ch
Valid Projects:	CHV, BSW

This register stores Frame Zero Padding Byte Count

DWord	Bit	Description
0	31:16	**Reserved**
		Format: MBZ
	15:0	**Frame Zero Padding Byte Count**
		Format: U16
		This register contains Frame Zero Padding byte count This is legacy support. This feature is not validated.

Reported Timestamp Count

TIMESTAMP - Reported Timestamp Count	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00000000h, 00000000 CHV, BSW
Access:	RO. This register is not set by the context restore.
Size (in bits):	64
Address:	02358h
Address:	12358h-1235Fh
Name:	Reported Timestamp Count
ShortName:	TIMESTAMP_VCSUNIT0
Address:	1A358h-1A35Fh
Name:	Reported Timestamp Count
ShortName:	TIMESTAMP_VECSUNIT
Address:	1C358h-1C35Fh
Name:	Reported Timestamp Count
ShortName:	TIMESTAMP_VCSUNIT1
Address:	22358h-2235Fh
Name:	Reported Timestamp Count
ShortName:	TIMESTAMP_BCSUNIT

Description
This register provides an elapsed real-time value that can be used as a timestamp for GPU events over short periods of time. Note that the value of this register can be obtained in a 3D pipeline-synchronous fashion without a pipeline flush by using the PIPE_CONTROL command. See 3D Geometry Pipeline in the "3D and Media" volume. This register (effectively) counts at a constant frequency by adjusting the increment amount according to the actual reference clock frequency. SW therefore does not need to know the reference clock frequency. This register is not reset by a graphics reset. It will maintain its value unless a full chipset reset is performed.
Note: On Core platforms, the TIMESTAMP register is initialized with the value of the PCU ART and hence tracks bits 38:3 of the 100 MHz ART fairly closely. However, due to variability in the actual time it takes to download the ART value to GT, the value of the TIMESTAMP register will be lower than the value of the PCU ART by an amount dependent on the relative IA/CLR/GT frequencies at the time the timestamp was downloaded to GT (expected to range between 100 and 600 ns). When comparing the value sampled from this register by GT HW to values read from the PCU timer by other system agents, timing differences between GT HW reading the TIMESTAMP register and the involved non-GT agent(s) reading the PCU ART must also be comprehended.

TIMESTAMP - Reported Timestamp Count

DWord	Bit	Description	
0	63:36	**Reserved**	
		Project:	CHV, BSW
		Format:	MBZ
	35:0	**Timestamp Value**	
		Project:	CHV, BSW
		Format:	U36

Description
This register toggles based on time stamp granularity (base unit) defined in the "Time Stamp Bases" subsection in Power Management chapter.

Reset Flow Control Messages

<table>
<tr><td colspan="3" align="center">**RSTFCTLMSG - Reset Flow Control Messages**</td></tr>
<tr><td>Register Space:</td><td colspan="2">MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td colspan="2">CHV, BSW</td></tr>
<tr><td>Source:</td><td colspan="2">PRM</td></tr>
<tr><td>Default Value:</td><td colspan="2">0x00000000</td></tr>
<tr><td>Size (in bits):</td><td colspan="2">32</td></tr>
<tr><td>Address:</td><td colspan="2">08108h</td></tr>
<tr><td colspan="3">Soft-Reset and FLR Flow Control Message Registers</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td>**Description**</td></tr>
<tr><td>0</td><td>31:16</td><td>**Message Mask**

Access: RO

Message Mask
In order to write to bits 15:0, the corresponding message mask bits must be written.
For example, for bit 14 to be set, bit 30 needs to be 1 : 40004000</td></tr>
<tr><td></td><td>15:12</td><td>**Reserved**</td></tr>
<tr><td></td><td>11</td><td>**MEDIA 1 Reset flow acknowledgement message**

Access: R/W

PM Acknowledgement Messages for Media 1 reset:
'1' : PREP_RST_MEDIA1_ACK
- Acknowledgement that graphics media1 (or 2nd vbox) is prepared for reset assertion.
'0' : DONE_MEDIA1_RST_ACK
- Acknowledgement that graphics media1 (or 2nd vbox) reset is de-asserted</td></tr>
<tr><td></td><td>10</td><td>**WIDI Reset flow acknowledgement message**

Access: R/W

PM Acknowledgement Messages for WIDI reset:
'1' : PREP_RST_WIDI_ACK
- Acknowledgement that graphics widi is prepared for reset assertion.
'0' : DONE_WIDI_RST_ACK
- Acknowledgement that graphics widi reset is de-asserted</td></tr>
<tr><td></td><td>9</td><td>**Reserved**</td></tr>
<tr><td></td><td>8</td><td>**Vebox Reset flow Acknowledge Message**

Access: R/W

PM Acknowledgement Messages for Vebox reset:
'1' : PREP_RST_VEBOX_ACK
- Acknowledgement that graphics VE is prepared for reset assertion.
'0' : DONE_VEBOX_RST_ACK
- Acknowledgement that graphics VE reset is de-asserted</td></tr>
</table>

RSTFCTLMSG - Reset Flow Control Messages

7	**Blitter Reset Flow Acknowledgement Messages**		
	Access:		R/W
	PM Acknowledgement Messages for Blitter reset: '1' : PREP_RST_BLIT_ACK - Acknowledgement that graphics blitter is prepared for reset assertion. '0' : DONE_BLIT_RST_ACK - Acknowledgement that graphics blitter reset is de-asserted		
6	**Media Reset Flow Acknowledgement Messages**		
	Access:		R/W
	PM Acknowledgement Messages for Media reset: '1' : PREP_RST_MEDIA_ACK - Acknowledgement that graphics media block is prepared for reset assertion. '0' : DONE_MEDIA_RST_ACK - Acknowledgement that the graphics media reset is de-asserted		
5	**Render Reset Flow Acknowledgement Messages**		
	Access:		R/W
	PM Acknowledgement Messages for Render reset: '1' : PREP_RST_RENDER_ACK - Acknowledgement that the graphics render block is prepared for reset assertion. '0' : DONE_RENDER_RST_ACK - Acknowledgement that the graphics render reset is de-asserted		
4	**GTI-Device Reset Flow Acknowledgement Messages**		
	Access:		R/W
	PM Acknowledgement Messages for GTI-Device reset: '1' : PREP_RST_GTIDEV_ACK - Acknowledgement that the GTI device is prepared for reset assertion. '0' : DONE_GTIDEV_RST_ACK - Acknowledgement that the GTI device reset is de-asserted		
3	**Reserved**		
	Access:		RO
	Reserved		
2	**FLR Done ack from Pmunit**		
	Access:	R/W Set	
	FLR Done ack from Pmunit: 1: PM unit sets this bit to acknowledge the FLR done message has been forwarded to SA through GAM interface. 0: Default Value. If the bit was set by PM then Cpunit hardware clears it once FLR is completed.		

		RSTFCTLMSG - Reset Flow Control Messages	
	1	**Global Resource Arbitration Acknowledgement Messages**	
		Access:	R/W
		Global Resource Arbitration Acknowledgement Message from PM: '1' : CP_ARB_REQ_ACK - Acknowledgement for CPunit's global resource arbitration request '0' : CP_ARB_RELEASE_ACK - Acknowledgement to CPunit's release of global resources	
	0	**CP Busy / Idle Status Acknowledgement Messages**	
		Access:	R/W
		CP Busy / Idle Status Acknowledgement Message from PM: '0' : CP_NOT_BUSY_ACK - Acknowledgement that the CPunit is idle. '1' : CP_BUSY_ACK - Acknowledgement that the CPunit is busy.	

RESET Messaging Register for Clocking Unit

MSG_RESET_GCP - RESET Messaging Register for Clocking Unit		

Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	16

Address:	08030h

Message registers have bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16]. In order to set bit0, for example, the data would be 0x0001_0001. In order to clear bit0, for example, the data would be 0x0001_0000. Note that mask bit is the data bit offset + 16. Message registers are protected from non-GT writes via the Message Channel.
Request to Prepare for Reset
1'b0 : Reset complete <default>
1'b1 : Prepare for reset

DWord	Bit	Description	
0	15:8	**Reserved**	
		Access:	RO
	7	**Request to Prepare for FLR**	
		Access:	R/W
		[7] Prepare for devrst_b Domain Reset (FLR) Note: All resets except busrst_b will be asserted for an FLR	
	6	**Request to Prepare for Media1 Reset**	
		Access:	R/W
		[6] Prepare for cmrst_b Domain Reset (vcs1unit)	
	5	**Request to Prepare for Wi-Di Reset**	
		Access:	R/W
		[5] Prepare for cwrst_b Domain Reset (winunit)	
	4	**Reserved**	
	3	**Request to Prepare for Blitter Reset**	
		Access:	R/W
		[3] Prepare for crblitrst_b Domain Reset (bcsunit)	
	2	**Request to Prepare for VEBox Reset**	
		Access:	R/W
		[2] Prepare for cvrst_b Domain Reset (vecsunit)	

MSG_RESET_GCP - RESET Messaging Register for Clocking Unit

	1	**Request to Prepare for Media0 Reset**	
		Access:	R/W
		[1] Prepare for cmrst_b Domain Reset (vcs0unit)	
	0	**Request to Prepare for Render Reset**	
		Access:	R/W
		[0] Prepare for crrst_b Domain Reset (csunit)	

Resource Streamer Context Offset

RS_CXT_OFFSET - Resource Streamer Context Offset

Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00003B00
Access:	Read/32 bit Write Only
Size (in bits):	32
Address:	021B4h

DWord	Bit	Description
0	31:6	**RS Offset** Format: U26 This field indicates the offset (64bytes granular) in to the logical rendering context to which Resource Streamer context is save/restored when enabled. This field register must not be written directly (via MMIO) unless the Command Streamer is completely idle (i.e., the Ring Buffer is empty and the pipeline is idle) and RC6 is disabled. On way to program this register is via Load Register Immediate command in the ring buffer as part of initialization sequence. Value: ECh / Name: [Default] / Description: DefaultValueDesc
	5:0	**Reserved** Format: MBZ

Resource Streamer Preemption Status

RS_PREEMPT_STATUS - Resource Streamer Preemption Status	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	0215Ch

Preemption from First Level Batch Buffer: This register contains the offset in to the Batch Buffer on which Resource streamer got preempted. Note that it is offset from the Batch Start Address and not the graphics address corresponding to the preempted instruction on Batch Buffer. This register's contents will be looked at by Command Streamer on the next RS Start Trigger to provide the appropriate batch start address. Following preemption, context save happens on which this register is context saved, after context save the register gets auto reset by Command Streamer. This register gets context save/restored by Render Command Streamer as part of its render context. **Preemption from Second Level Batch Buffer:** This register contains the graphics address of the instruction in Second Level Batch Buffer on which Resource streamer got preempted. This register's contents will be looked at by Command Streamer on the next RS Start Trigger to provide the appropriate batch start address. Following preemption, context save happens on which this register is context saved, after context save the register gets auto reset by Command Streamer. This register gets context save/restored by Render Command Streamer as part of its render context.

Programming Notes
• This register is accessed by Render Command Streamer as part of render context save/restore; this register should be exercised by S/W only for resetting the register contents if required. • Following preemption if there is no context save, SW should program this register with 0x0 so that it does not interfere with proceeding workloads.

DWord	Bit	Description
0	31:2	**Batch Buffer Offset**
		Format: Offset[31:2]
		This field specifies the DWord-aligned offset from the batch start address on which Resource Streamer got preempted.
	1	**RS_PREEMPT_STATUS**
		Format: MBZ
		This field when not set indicates RS got preempted on a natural sync point else it got preempted on a draw call.

RS_PREEMPT_STATUS - Resource Streamer Preemption Status

	0	**RS_PREEMPTED**	
		Default Value:	0
		Format:	Enable
		If this bit is set indicates Resource Streamer got preempted. Other fields of this register are valid only when this bit is set.	

Restored Timestamp LSDW

RTSLSDW - Restored Timestamp LSDW	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0A530h-0A533h

DWord	Bit	Description	
0	31:0	**Restored Time Stamp Storage**	
		Access:	R/W
		Restored Time Stamp Storage	

Restored timestamp MSDW

RTSMSDW - Restored timestamp MSDW		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A534h-0A537h	
DWord	**Bit**	**Description**
0	31:0	**Restored Time Stamp Storage**
		Access: R/W
		Restored Time Stamp Storage

RID_CC

RID_CC - RID_CC	
Register Space:	PCI: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	00008h

Revision Identification and Class code register. SOXi Context Save/Restore: Yes.

DWord	Bit	Description
0	31:24	**BASE_CLASS_CODE** <table><tr><td>Access:</td><td>RO</td></tr></table>
	23:16	**SUB_CLASS_CODE** <table><tr><td>Access:</td><td>RO</td></tr></table> When MGGC0[VAMEN] is 1, this value is 80h, indicating other multimedia device. When MGGC0[VAMEN] is 0 this value will be determined based on GGC register, GMS and IVD fields. When GGC[1] = 1 or GGC[7:3] = 5'b00000 this value is 80h, otherwise its 00h 00h: VGA compatible 80h: Non VGA (GMS = '00h' or IVD = '1b')
	15:8	**PROGRAMMING_INTERFACE** <table><tr><td>Default Value:</td><td>00h</td></tr><tr><td>Access:</td><td>RO</td></tr></table>
	7:0	**REVISION_ID** <table><tr><td>Default Value:</td><td>00000000b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> RID: The value in this field reflects the value of strapRID[7:0] (which is an input pin of GVD). For VV: The reset value will be the same as MID bits 23:16 (reference the MID register for MID register details). This register is read-able by any agent. Under SAI protection, the PMC and Punit (ie. 'Trusted_FW') can write this register and change the default value. No other agent has the ability to update this register. The PMC implementation will consider SRID and CRID before updating this register. Any PMC updates will be prior to Device 2 configuration. Note : The MID register will always reflect the stepping information. Even if PMC updates this register, the MID is available as a SRID reference.

RING_BUFFER_HEAD_PREEMPT_REG

RING_BUFFER_HEAD_PREEMPT_REG - RING_BUFFER_HEAD_PREEMPT_REG	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32

Address:	0214Ch-0214Fh
Name:	RING_BUFFER_HEAD_PREEMPT_REG
ShortName:	RING_BUFFER_HEAD_PREEMPT_REG_RCSUNIT

Address:	1214Ch-1214Fh
Name:	RING_BUFFER_HEAD_PREEMPT_REG
ShortName:	RING_BUFFER_HEAD_PREEMPT_REG_VCSUNIT0

Address:	1A14Ch-1A14Fh
Name:	RING_BUFFER_HEAD_PREEMPT_REG
ShortName:	RING_BUFFER_HEAD_PREEMPT_REG_VECSUNIT

Address:	1C14Ch-1C14Fh
Name:	RING_BUFFER_HEAD_PREEMPT_REG
ShortName:	RING_BUFFER_HEAD_PREEMPT_REG_VCSUNIT1

Address:	2214Ch-2214Fh
Name:	RING_BUFFER_HEAD_PREEMPT_REG
ShortName:	RING_BUFFER_HEAD_PREEMPT_REG_BCSUNIT

Description
This register contains the Head pointer offset in the ring when the last PREEMPTABLE command was executed and caused the head pointer to move due to the UHPTR register being valid. If the PREEMPTABLE command is executed as part of the batch buffer then the value of the register will be the offset in the ring of the command past the batch buffer start that contained the preemptable command.   This is a global register and context save/restored as part of power context image.

Preemptable Commands	Source
• MI_ARB_CHECK • 3D_PRIMITIVE • GPGPU_WALKER • MEDIA_STATE_FLUSH • PIPE_CONTROL (Only in GPGPU mode of pipeline selection)	RenderCS

RING_BUFFER_HEAD_PREEMPT_REG - RING_BUFFER_HEAD_PREEMPT_REG

- MI_ATOMIC (Post Sync Operation set in GPGPU mode of pipeline selection)
- MI_SEMAPHORE_SIGNAL (Post Sync Operation set in GPGPU mode of pipeline selection)

Programming Notes
Programming Restriction: **This register should NEVER be programmed by driver. This is for HW internal use only.**

DWord	Bit	Description
0	31:21	**Last Wrap Count**
	20:2	**Preempted Head Offset**
		Format: ⎮ U19
		This field contains the Head pointer offset in the ring when the last MI_ARB_CHECK command was executed and caused the head pointer to move due to the UHPTR register being valid.
	1:0	**Ring/Batch Indicator**
		Format: ⎮ Enabled

Value	Name	Description
0h	Ring	Preemptable command was executed in ring and caused head pointer to be updated.
1h	Batch	Preemptable command was executed in batch and caused head pointer to be updated.
2h	2nd level batch	Preemptable command was executed in second level batch and caused head pointer to be updated.

Ring Buffer Control

<table>
<tr><td colspan="2" align="center">**RING_BUFFER_CTL - Ring Buffer Control**</td></tr>
<tr><td>Register Space:</td><td>MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td>CHV, BSW</td></tr>
<tr><td>Source:</td><td>PRM</td></tr>
<tr><td>Default Value:</td><td>0x00000000</td></tr>
<tr><td>Access:</td><td>R/W</td></tr>
<tr><td>Size (in bits):</td><td>32</td></tr>
<tr><td>Address:</td><td>0203Ch-0203Fh</td></tr>
<tr><td>Name:</td><td>Ring Buffer Control</td></tr>
<tr><td>ShortName:</td><td>RING_BUFFER_CTL_RCSUNIT</td></tr>
<tr><td>Address:</td><td>1203Ch-1203Fh</td></tr>
<tr><td>Name:</td><td>Ring Buffer Control</td></tr>
<tr><td>ShortName:</td><td>RING_BUFFER_CTL_VCSUNIT0</td></tr>
<tr><td>Address:</td><td>1A03Ch-1A03Fh</td></tr>
<tr><td>Name:</td><td>Ring Buffer Control</td></tr>
<tr><td>ShortName:</td><td>RING_BUFFER_CTL_VECSUNIT</td></tr>
<tr><td>Address:</td><td>1C03Ch-1C03Fh</td></tr>
<tr><td>Name:</td><td>Ring Buffer Control</td></tr>
<tr><td>ShortName:</td><td>RING_BUFFER_CTL_VCSUNIT1</td></tr>
<tr><td>Address:</td><td>2203Ch-2203Fh</td></tr>
<tr><td>Name:</td><td>Ring Buffer Control</td></tr>
<tr><td>ShortName:</td><td>RING_BUFFER_CTL_BCSUNIT</td></tr>
</table>

Description	Source
These registers are used to define and operate the ring buffer mechanism which can be used to pass instructions to the command interface. The buffer itself is located in a physical memory region. The ring buffer is defined by a 4 Dword register set that includes starting address, length, head offset, tail offset, and control information. Refer to the Programming Interface chapter for a detailed description of the parameters specified in this ring buffer register set, restrictions on the placement of ring buffer memory, arbitration rules, and in how the ring buffer can be used to pass instructions.	RenderCS
Ring Buffer Head and Tail Offsets must be properly programmed before it is enabled. A Ring Buffer can be enabled when empty.	BlitterCS, VideoCS, VideoEnhancementCS

RING_BUFFER_CTL - Ring Buffer Control

Graphics Engine doesn't go IDLE when head offset is not equal to tail offset when ring buffer is disabled. PSMI controller waits for HW to go Idle as part of the PSMI flow. When PSMI flow happens in middle of ring buffer initialization where in Head offset is not equal to Tail offset and Ring Buffer disabled, PMSI flow will hang waiting for Graphics Engine to go IDLE. (During ring buffer initialization SW programs Head and Tail offsets prior to enabling Ring Buffer). In order to avoid this dead lock PSMI controller must detect this case and program head and tail offset to be equal to allow Graphics Engine to go IDLE, before exiting PSMI flow original head and tail offsets should be restored.	

DWord	Bit	Description
0	31:21	**Reserved**

Format:	MBZ

	20:12	**Buffer Length**

Format:	U9-1 in 4 KB pages - 1

This field is written by SW to specify the length of the ring buffer in 4 KB Pages.Range = [0 = 1 page = 4 KB, 1FFh = 512 pages = 2 MB]

Value	Name	Description
0		1 page = 4 KB
1FFh		512 pages = 2 MB

	11	**RBWait**

Description	Source
Indicates that this ring has executed a WAIT_FOR_EVENT instruction and is currently waiting. Software can write a "1" to clear this bit, write of "0" has no effect. When the RB is waiting for an event and this bit is cleared, the wait will be terminated and the RB will be returned to arbitration.	
RenderCS: RBWait is not set on executing WAIIT_FOR_EVENT instruction waiting on Async Flip Pending.	RenderCS

	10	**Semaphore Wait**

Description
Indicates that this ring has executed a MI_SEMAPHORE_WAIT instruction and is currently waiting for wait condition to satisfy.

	9	**Reserved**

Format:	MBZ

	8	**Reserved**

Project:	CHV, BSW
Format:	MBZ

	7:3	**Reserved**

Format:	MBZ

	2:1	**Automatic Report Head Pointer**

RING_BUFFER_CTL - Ring Buffer Control

Project:	CHV, BSW
Source:	PRM

Description
This field is written by software to control the automatic reporting (write) of this ring buffer's Head Pointer register (register DWord 1) to the corresponding location within the Hardware Status Page. Automatic reporting can either be disabled or enabled at 4KB, 64KB or 128KB boundaries within the ring buffer.
When Execlist Enable bit is set the head pointer will be reported to the head pointer location in the Per-Process Hardware Status Page. MI_AUTOREPORT_4KB option is not supported on A stepping.

Value	Name	Description
0	MI_AUTOREPORT_OFF	Automatic reporting disabled
1	MI_AUTOREPORT_64KB	Report every 16 pages (64KB)
2	MI_AUTOREPORT_4KB	Report every page (4KB) This mode must not be enabled in Ring Buffer mode of scheduling to minimize the auto reports.
2	MI_AUTOREPORT_4KB	Report every page (4KB) This mode must not be enabled in Ring Buffer mode of scheduling to minimize the auto reports.
3	MI_AUTOREPORT_128KB	Report every 32 pages (128KB)

0 — **Ring Buffer Enable**

Format:	Enable

This field is used to enable or disable this ring buffer. It can be enabled or disabled regardless of whether there are valid instructions pending. If disabled and the ring head equals ring tail, all state currently loaded in hardware is considered invalid.

Programming Notes	Source
Ring Buffer Mode of Scheduling: SW must follow the below programming notes during SW initialization phase or while enabling render engine's ring buffer for the first time, this would be coming out of boot, standby, hibernate or reset. This flow must be also followed during ring replay when ring buffer is disabled and enabled during debug. • SW must set the Force Wakeup bit to prevent GT from entering C6. • SW must dispatch workload (dummy context) to initialize render engine with default state such that any context switches that occur subsequently (Power Save) will save and restore coherent device state. Indirect pointers used in 3D states must point to valid graphics surface existing in memory. PP_DCLV followed by PP_DIR_BASE register should be programmed as part of initialization workload if PPGTT is enabled in GFX_MODE register. • SW must ensure all the register (MMIO) initialization/programming through CPU happens in this block or latter, this ensures the MMIO state is save/restored on subsequent context switches (Power Sequences).	RenderCS

RING_BUFFER_CTL - Ring Buffer Control		
	• Once the render engine is programmed with valid state and the configuration, Force Wakeup bit should be reset to enable C6 entry.	
	Render CS Only: Ring Buffer Mode of Scheduling: SW must follow the below programming notes before disabling ring buffer to ensure HW is not in middle of the IDLE flows. • SW must set the Force Wakeup bit to prevent GT from entering C6. • Disable IDLE messaging in CS (Write 0x2050[31:0] = 0x00010001) • Poll/Wait for register bits of <u>0x22AC[6:0]</u> turn to 0x30 value. • Disable Ring Buffer • Enable IDLE messaging in CS (Write 0x2050[31:0] = 0x00010000) • Force Wakeup bit should be reset to enable C6 entry.	RenderCS

Ring Buffer Current Context ID Register

BCS_RCCID - Ring Buffer Current Context ID Register		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	BlitterCS	
Default Value:	0x00000000, 0x00000000	
Access:	R/W	
Size (in bits):	64	
Address:	22190h-22197h	
This register contains the current ring context ID associated with the ring buffer.		
Programming Notes		
The current context registers must not be written directly (via MMIO). The RCCID register should only be updated indirectly from RNCID.		
DWord	**Bit**	**Description**
0	63:0	**Unnamed** See Context Descriptor for BCS.

Ring Buffer Head

RING_BUFFER_HEAD - Ring Buffer Head	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02034h-02037h
Name:	Ring Buffer Head
ShortName:	RING_BUFFER_HEAD_RCSUNIT
Address:	12034h-12037h
Name:	Ring Buffer Head
ShortName:	RING_BUFFER_HEAD_VCSUNIT0
Address:	1A034h-1A037h
Name:	Ring Buffer Head
ShortName:	RING_BUFFER_HEAD_VECSUNIT
Address:	1C034h-1C037h
Name:	Ring Buffer Head
ShortName:	RING_BUFFER_HEAD_VCSUNIT1
Address:	22034h-22037h
Name:	Ring Buffer Head
ShortName:	RING_BUFFER_HEAD_BCSUNIT

Description
This register is used to define and operate the ring buffer mechanism which can be used to pass instructions to the command interface. The buffer itself is located in a physical memory region. The ring buffer is defined by a 4 Dword register set that includes starting address, length, head offset, tail offset, and control information. Refer to the Programming Interface chapter for a detailed description of the parameters specified in this ring buffer register set, restrictions on the placement of ring buffer memory, arbitration rules, and in how the ring buffer can be used to pass instructions. **Ring Buffer Head Offsets must be properly programmed before ring is enabled. A Ring Buffer can be enabled when empty.**

DWord	Bit	Description	
0	31:21	**Wrap Count**	
		Format:	U11 count of ring buffer wraps
		This field is incremented by 1 whenever the **Head Offset** wraps from the end of the buffer back to the start (i.e., whenever it wraps back to 0). Appending this field to the **Head Offset** field effectively creates a virtual 4GB Head "Pointer" which can be used as a tag associated with instructions placed in a ring buffer. The Wrap Count itself will wrap to 0 upon overflow.	

RING_BUFFER_HEAD - Ring Buffer Head

	20:2	**Head Offset**	
		Format:	GraphicsAddress[20:2] DWord Offset

 This field indicates the offset of the *next* instruction DWord to be parsed. Software will initialize this field to select the first DWord to be parsed once the RB is enabled. (Writing the Head Offset while the RB is enabled is UNDEFINED). Subsequently, the device will increment this offset as it executes instructions - until it reaches the QWord specified by the **Tail Offset**. At this point the ring buffer is considered "empty".

<div align="center">

Programming Notes
</div>

A RB can be enabled empty or containing some number of valid instructions.

	1	**Reserved**	
		Format:	MBZ

	0	**Reserved**	
		Project:	CHV, BSW
		Format:	MBZ

Ring Buffer Start

RING_BUFFER_START - Ring Buffer Start	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02038h-0203Bh
Name:	Ring Buffer Start
ShortName:	RING_BUFFER_START_RCSUNIT
Address:	12038h-1203Bh
Name:	Ring Buffer Start
ShortName:	RING_BUFFER_START_VCSUNIT0
Address:	1A038h-1A03Bh
Name:	Ring Buffer Start
ShortName:	RING_BUFFER_START_VECSUNIT
Address:	1C038h-1C03Bh
Name:	Ring Buffer Start
ShortName:	RING_BUFFER_START_VCSUNIT1
Address:	22038h-2203Bh
Name:	Ring Buffer Start
ShortName:	RING_BUFFER_START_BCSUNIT

Description
These registers are used to define and operate the "ring buffer" mechanism which can be used to pass instructions to the command interface. The buffer itself is located in a physical memory region. The ring buffer is defined by a 4 Dword register set that includes starting address, length, head offset, tail offset, and control information. Refer to the Programming Interface chapter for a detailed description of the parameters specified in this ring buffer register set, restrictions on the placement of ring buffer memory, arbitration rules, and in how the ring buffer can be used to pass instructions.

DWord	Bit	Description	
0	31:12	**Starting Address**	
		Format:	GraphicsAddress[31:12]RingBuffer
		This field specifies Bits 31:12 of the 4KB-aligned starting Graphics Address of the ring buffer. Address bits 31 down to 29 must be zero. All ring buffer pages must map to Main Memory (uncached) pages. Ring Buffer addresses are always translated through the global GTT.	
	11:0	**Reserved**	

Ring Buffer Tail

RING_BUFFER_TAIL - Ring Buffer Tail	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02030h-02033h
Name:	Ring Buffer Tail
ShortName:	RING_BUFFER_TAIL_RCSUNIT
Address:	12030h-12033h
Name:	Ring Buffer Tail
ShortName:	RING_BUFFER_TAIL_VCSUNIT0
Address:	1A030h-1A033h
Name:	Ring Buffer Tail
ShortName:	RING_BUFFER_TAIL_VECSUNIT
Address:	1C030h-1C033h
Name:	Ring Buffer Tail
ShortName:	RING_BUFFER_TAIL_VCSUNIT1
Address:	22030h-22033h
Name:	Ring Buffer Tail
ShortName:	RING_BUFFER_TAIL_BCSUNIT

Description
These registers are used to define and operate the "ring buffer" mechanism which can be used to pass instructions to the command interface. The buffer itself is located in a linear memory region. The ring buffer is defined by a 4 Dword register set that includes starting address, length, head offset, tail offset, and control information. Refer to the Programming Interface chapter for a detailed description of the parameters specified in this ring buffer register set, restrictions on the placement of ring buffer memory, arbitration rules, and in how the ring buffer can be used to pass instructions. Ring Buffer Tail Offsets must be properly programmed before ring is enabled. A Ring Buffer can be enabled when empty.

DWord	Bit	Description	
0	31:21	**Reserved**	
		Format:	MBZ

		RING_BUFFER_TAIL - Ring Buffer Tail	
	20:3	**Tail Offset**	
		Format:	GraphicsAddress[20:3]
		This field is written by software to specify where the valid instructions placed in the ring buffer end. The value written points to the QWord past the last valid QWord of instructions. In other words, it can be defined as the next QWord that software will write instructions into. Software must write subsequent instructions to QWords following the Tail Offset, possibly wrapping around to the top of the buffer (i.e., software can't skip around within the buffer). Note that all DWords prior to the location indicated by the **Tail Offset** must contain valid instruction data - which may require instruction padding by software. See **Head Offset** for more information.	
		Programming Notes	
		[Ring Buffer Mode Of scheduling only][Video CS, Video Enhancement CS, Blitter CS]: HW loses Page Directory (PPGTT) information on becoming IDLE. SW must always program the PD information through MI_LOAD_REGISTER_IMM command in the ring buffer prior to programming workload begins on every ring dispatch. This will ensure Page Directory information is not lost due to IDLE flows.	
	2:0	**Reserved**	
		Format:	MBZ

Root Table Address Pointer Value First 31_0

RTAPV_1_310 - Root Table Address Pointer Value First 31_0		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0F500h	
This register is used to store local copy of the Root Table address pointer value.		

DWord	Bit	Description
0	31:0	**First Address 31 to 0**

		Default Value:	00000000h
		Access:	R/W

Bits 31:11 = Root Table Address Pointer Value 31:11.
Bits 10:1 = Reserved.
Bit 0 = Enabled for Root Table Address Pointer Value 31:11.

Root Table Address Pointer Value Second 31_0

RTAPV_2_310 - Root Table Address Pointer Value Second 31_0	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0F504h

This register is used to store local copy of the Root Table address pointer value.

DWord	Bit	Description	
0	31:0	**Second Address 31 to 0**	
		Default Value:	00000000h
		Access:	R/W
		Bits 31:8 = Reserved. Bits 7:1 = Root Table Address Pointer Value 38:32. Bit 0 = Enabled for Root Table Address Pointer Value 38:32.	

RP Decrease Limit

RPDECLIMIT - RP Decrease Limit		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A030h-0A033h	
DWord	**Bit**	**Description**
0	31:24	**Reserved**
		Access: / RO
	23:0	**Decrease Threshold**
		Access: / R/W
		Decrease Threshold (DECLIMIT): This register contains the threshold used to determine whether a switch to a higher higher frequency is desirable. FRQDUM determines the meaning of this register: Busy Min Continuous Limit Busy Min Average Limit Idle Max Continuous Limit The values are: 0 = 0 usec 1 = 1.28 usec 2 = 2.56 usec 3 = 3.84 usec FF FFFF = 21.474 sec

RP Down Timeout

RPDNTIMOUT - RP Down Timeout		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A010h-0A013h	
DWord	**Bit**	**Description**
0	31:24	**Reserved**
		Access: RO
	23:0	**Down Timeout**
		Access: R/W
		The value in this register contains the timeout value for gfx idleness due to stopped graphics clocks (CPD) necessary to trigger the Render Geyserville Downward Timeout interrupt. 0 = 0 usec 1 = 1.28 usec 2 = 2.56 usec 3 = 3.84 usec FF FFFF = 21.474 sec

RP Downwards Evaluation Interval

RPDNEI - RP Downwards Evaluation Interval		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A06Ch-0A06Fh	

DWord	Bit	Description
0	31:24	**Reserved**
		Access: RO
	23:0	**Evaluation Interval Period for Downwards Freq Direction**
		Access: R/W
		The geyserville performance status will be averaged over this interval, and the results will be used to possibly recommend a switch to the slower render clock frequency (either directly by hardware or via an interrupt activating a sw decision). 0 = 0 usec 1 = 1.28 usec 2 = 2.56 usec 3 = 3.84 usec FF FFFF = 21.474 sec pmcr_ei_down[23:0]

RP Increase Limit

<table>
<tr><td colspan="3" align="center">**RPINCLIMIT - RP Increase Limit**</td></tr>
<tr><td colspan="3">Register Space: MMIO: 0/2/0</td></tr>
<tr><td colspan="3">Project: CHV, BSW</td></tr>
<tr><td colspan="3">Source: PRM</td></tr>
<tr><td colspan="3">Default Value: 0x00000000</td></tr>
<tr><td colspan="3">Size (in bits):   32</td></tr>
<tr><td colspan="3">Address: 0A02Ch-0A02Fh</td></tr>
</table>

DWord	Bit	Description
0	31:24	**Reserved** Access: RO
	23:0	**Increase Threshold** Access: R/W Increase Threshold (INCLIMIT): This register contains the threshold used to determine whether a switch to a higher higher frequency is desirable. FRQIUM determines the meaning of this register: Busy Max Continuous Limit Busy Max Average Limit Idle Min Continuous Limit The values are: 0 = 0 usec 1 = 1.28 usec 2 = 2.56 usec 3 = 3.84 usec FF FFFF = 21.474 sec

RP Normal Software Frequency Request

RP_FREQ_NORMAL - RP Normal Software Frequency Request		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A008h	
This 32 bit value is written to the PCU IO_THREAD_P_REQ register when NOT in Video Turbo mode.		

DWord	Bit	Description
0	31	**Turbo Disable**
		Access: R/W
		The Turbo Disable bit is determined by SW. NOTE: If Turbo is disable for ANY thread, it will prevent turbo for ALL threads.
	30:24	**P State Request**
		Access: R/W
		This field indicates the maximum P-State request in units of 100MHz.
	23:18	**P State Offset**
		Access: R/W
		This field defined the number of steps that Energy Efficient P-State is allowed to fall in units of 100 MHz.
	17:14	**Energy Efficient policy**
		Access: R/W
		The energy efficiency policy is determined by SW.
	13:0	**Reserved**
		Access: RO

RP Software Frequency Request Hysteresis

RPSWFREQHYST - RP Software Frequency Request Hysteresis		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A004h	

DWord	Bit	Description
0	31:6	**Reserved**
		Access: RO
	5:0	**RP SW Freq Request Hysteresis**
		Access: R/W

Programming Notes	Project
Not supported. It must be 0 at all times.	CHV, BSW

RP Upwards Evaluation Interval

RPUPEI - RP Upwards Evaluation Interval		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A068h-0A06Bh	

DWord	Bit	Description
0	31:24	**Reserved**
		Access: RO
	23:0	**Evaluation Interval Period for Upwards Freq Direction**
		Access: R/W
		The geyserville performance status will be averaged over this interval, and the results will be used to possibly recommend a switch to the faster render clock frequency (either directly by hardware or via an interrupt activating a sw decision). 0 = 0 usec 1 = 1.28 usec 2 = 2.56 usec 3 = 3.84 usec FF FFFF = 21.474 sec pmcr_ei_up[23:0]

RP Video Turbo Software Frequency Request

RP_FREQ_VIDEOTURBO - RP Video Turbo Software Frequency Request		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A00Ch	
This 32 bit value is written to the PCU IO_THREAD_P_REQ register when in Video Turbo mode.		

DWord	Bit	Description
0	31	**Turbo Disable**
		Access: R/W
		The Turbo Disable bit is determined by SW. NOTE: If Turbo is disable for ANY thread, it will prevent turbo for ALL threads.
	30:24	**P State Request**
		Access: R/W
		This field indicates the maximum P-State request in units of 100MHz.
	23:18	**P State Offset**
		Access: R/W
		This field defined the number of steps that Energy Efficient P-State is allowed to fall in units of 100 MHz.
	17:14	**Energy Efficient policy**
		Access: R/W
		The energy efficiency policy is determined by SW.
	13:0	**Reserved**
		Access: RO

RS_PREEMPT_STATUS_UDW

RS_PREEMPT_STATUS_UDW - RS_PREEMPT_STATUS_UDW	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02174h

Preemption from First Level Batch Buffer: This register contains the offset in to the Batch Buffer on which Resource streamer got preempted. Note that it is offset from the Batch Start Address and not the graphics address corresponding to the preempted instruction on Batch Buffer. This register's contents will be looked at by Command Streamer on the next RS Start Trigger to provide the appropriate batch start address. Following preemption, context save happens on which this register is context saved, after context save the register gets auto reset by Command Streamer. This register gets context save/restored by Render Command Streamer as part of its render context. **Preemption from Second Level Batch Buffer:** This register contains the graphics address of the instruction in Second Level Batch Buffer on which Resource streamer got preempted. This register's contents will be looked at by Command Streamer on the next RS Start Trigger to provide the appropriate batch start address. Following preemption, context save happens on which this register is context saved, after context save the register gets auto reset by Command Streamer. This register gets context save/restored by Render Command Streamer as part of its render context.

Programming Notes
• This register is accessed by Render Command Streamer as part of render context save/restore; this register should be exercised by S/W only for resetting the register contents if required.
• Following preemption if there is no context save, SW should program this register with 0x0 so that it does not interfere with proceeding workloads.

DWord	Bit	Description
0	31:16	**Reserved**
		Format: MBZ
	15:0	**Batch Buffer Offset Upper DWORD**
		Format: GraphicsAddress[47:32]
		This field specifies the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space of the last preempted second level batch buffer in resource streamer.

RS Preemption Hint

RS_PRE_HINT - RS Preemption Hint	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	024C0h

This register contains the Dword aligned Graphics address in to the Batch Buffer corresponding to either 3D_PRIMITIVE or RCS-RS sync command called Preemption Hint Address. When Preemption Hint Address is enabled, RS will honor preemption request from RCS only on parsing 3D_PRIMITIVE/RCS-RS sync command at Preemption Hint Address.

Programming Notes
Programming Restriction: This register should NEVER be programmed in functional mode, this should be used only in validation mode to achieve deterministic behavior of preempting Resource Streamer in command stream. Programmer has to ensure that RS Preemption Hint register gets programmed well before RS gets preempted by RCS. Note that this register should be programmed with caution as it can lead to indefinite stalls in RS.
a. RS will preempt on receiving preemption request from RCS only on reaching the instruction in the batch buffer corresponding to the address mentioned in RS_PREEMPT_HINT. RS could hit an RCS-RS sync command before reaching the address mentioned in the RS_PREEMPT_HINT, in this case RS should preempt on the sync command. b. RS could hit the address mentioned in 3D_PREEMPT_HINT before receiving preempt request from RCS. In this case RS will stall at this command until it receives preemption request from RCS and then preempts.

DWord	Bit	Description
0	31:2	**Preemption Hint Address**
		Format: U30
		This field contains the Dword aligned Graphics Address in to the batch buffer as Preemption Hint.
	1	**Reserved**
	0	**Preemption Hint**
		Format: Enabled

Value	Name	Description
0h	Disabled	Preemption hint is disabled for Resource Streamer.
1h	Enabled	Preemption hint is enabled for Resource streamer.

RS Preemption Hint UDW

RS_PREEMPTION_HINT_UDW - RS Preemption Hint UDW	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	024C4h

This register contains the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space of the Batch Buffer corresponding to either 3D_PRIMITIVE or RCS-RS sync command called Preemption Hint Address. When Preemption Hint Address is enabled, RS will honor preemption request from RCS only on parsing 3D_PRIMITIVE/RCS-RS sync command at Preemption Hint Address.

Restriction
This register should NEVER be programmed in functional mode, this should be used only in validation mode to achieve deterministic behavior of preempting Resource Streamer in command stream. See RS_PRE_HINT definition for further restrictions.

DWord	Bit	Description
0	31:16	**Reserved**
		Format: MBZ
	15:0	**Preemption Hint Address Upper DWORD**
		Format: GraphicsAddress[47:32]
		This field contains the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space of the batch buffer as Preemption Hint.

Sampler control register

SAMPLER_CTL - Sampler control register	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	0E140h
Valid Projects:	CHV, BSW]

DWord	Bit	Description
0	31:16	**ECO Reserved 1** Reserved: MBZ
	15:8	**Reserved**
	7:3	**Sampler unit select**
	2	**ECO Reserved 2**
	1:0	**ECO Reserved 3**

SAMPLER Mode Register

<table>
<tr><td colspan="3" align="center">**SAMPLER_MODE - SAMPLER Mode Register**</td></tr>
<tr><td>Register Space:</td><td colspan="2">MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td colspan="2">CHV, BSW</td></tr>
<tr><td>Source:</td><td colspan="2">RenderCS</td></tr>
<tr><td>Default Value:</td><td colspan="2">0x00000000</td></tr>
<tr><td>Size (in bits):</td><td colspan="2">32</td></tr>
<tr><td>Trusted Type:</td><td colspan="2">1</td></tr>
<tr><td>Address:</td><td colspan="2">07028h</td></tr>
<tr><td>Valid Projects:</td><td colspan="2">CHV, BSW</td></tr>
<tr><td colspan="3">This register has bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16]. To set bit0, for example, the data would be 0x0001_0001. To clear bit0, for example, the data would be 0x0001_0000. Note that mask bit is the data bit offset + 16.</td></tr>
</table>

DWord	Bit	Description
0	31:16	**Reserved**
		Access: RO
	15:14	**ECO Reserved 1**
		Format: MBZ
	13:8	**ECO Reserved 2**
		Project: CHV, BSW
		Format: MBZ
	7:6	**ECO Reserved 3**
		Project: All
		Format: MBZ
	5	**ECO_SCRATCH3B**
		Project:
		Format: MBZ
	4:0	**Sample_d Quality Mode**
		Project: CHV, BSW
		Format: U5

This field configures the image quality mode for the sample_d message in the sampling engine. In general, performance will increase with each step of reduced quality.

Value	Name	Description	Project
00h	Disabled	Full quality is enabled, matching prior products	All
01h-1Fh		Quality degrades with each larger value, performance improves with each larger value	All

SAMPLER READ DATA

SAMPLER_RDATA - SAMPLER READ DATA	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0xFFFFFFFF
Access:	RO Variant
Size (in bits):	32
Address:	0E144h
Valid Projects:	CHV, BSW

DWord	Bit	Description	
0	31:0	**Reserved**	
		Default Value:	FFFFFFFFh

Save Timer

SVTIMER - Save Timer		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x60001000	
Size (in bits):	32	
Address:	0B434h	
DWord	**Bit**	**Description**
0	31	**Reserved**
	30:29	**Counter Enabling Selection**

Default Value:		11b
Access:		R/W

LPFC provides rudimentary compression by allowing software to select from several predefined levels of event reporting. Based on the value of this bitfield, only a certain number of the programmed events in the "Event Selection and Base Counters" registers (CNT0CL, CNT1CL, ..., CNT7CL) will be tracked and reported:

Value	Selected Counters
00	Counter 0
01	Counters 0 & 1
10	Counters 0, 1, 2, & 3
11	Counters 0 - 7

Signal - lpconf_lpfc_cnt_enabled [1:0].

28:24	**Reserved**
23:0	**Save Timer Interval**

Default Value:	00000000000001000000000000b
Access:	R/W

Save Timer Interval (SVTMRINT).
Save Timer Interval: This is the interval for sampling the performance counters and writing to memory. Each time it expires, the counters are sampled and packetized to be sent to DMA controller.
The minimum granularity of sampling period if 256clocks. The value in this register is used as 256 x value to find the sampling window. For a 1Ghz core clock it provides up to 4ns of sampling period while matching the maximum capability of the event counters.
1h - 256clks.
2h - 512clks.
...
8h - 2048clks.
Signal - lpconf_lpfc_savetimer_int [23:0].

SB_ADDRESS

SB_ADDRESS - SB_ADDRESS	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	182108h

The Sideband Address Register is used by the sideband transaction (triggered by Sideband Packet Register) for holding the address (of the internal register, within the destination unit).

IOSF SB access prevention: An IOSF SB write access targeting this register will complete with no affect.
An IOSF SB read access targeting this register will abort (with 1's being returned on IOSF SB).

DWord	Bit	Description
0	31:0	**SB_Addr**

Default Value:		00000000h
Access:		R/W

Address, written by IOSF primary, for triggered IOSF SB initiated access.
0x18_2100 (SB_Busy) bit 0 =1 then an IOSF primary write will NOT be captured.
0x18_2100 (SB_Busy) bit 0 = 0 then an IOSF primary write will be captured.
Dword aligned addresses must be used.

SB_DATA

SB_DATA - SB_DATA	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	182104h

The Sideband Data Register is used by the sideband register access mechanism (triggered by Sideband Packet Register) for holding write-data in write-transactions or read-data for read-transactions as explained below.

IOSF SB access prevention :An IOSF SB write access targeting this register will complete with no affect.
An IOSF SB read access targeting this register will abort (with 1's being returned on IOSF SB).
Requirement : IOSF primary write to this register should not occur when a pending IOSF SB return is pending.

DWord	Bit	Description	
0	31:0	**SB Data**	
		Default Value:	00000000h
		Access:	R/W
		Triggered IOSF SB write, this is the Data written in the IOSF SB initiated access. Triggered IOSF SB read, this is the Data read return from the IOSF SB initiated read access. 0x18_2100 (SB_Busy) bit 0 = 1 then an IOSF primary write will NOT be captured. 0x18_2100 (SB_Busy) bit 0 = 0 then an IOSF primary write will be captured.	

SB_REQ_TRIGGER

SB_REQ_TRIGGER - SB_REQ_TRIGGER	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	182100h

When the Sideband Packet Register is written, the Gunit creates a transaction towards the destination agent on the IOSF sideband channel.
The fields sent with the write operation as transaction parameters:

- The Sideband Rid field (bits 31:24) is used as the transaction Rid.

- The Sideband Opcode field (bits 23:15) is used as the transaction opcode.

- The Sideband Port field (bits 15:8) is used as the transaction destination port.

- The source port is hard-coded to 6h (Gunit port).

- The Sideband Byte Enable Field (bits 7:4) is used as the transaction Byte Enable.

If the opcode results in a data write semantic transaction, the write-data will be taken from the Sideband Data Register. If the opcode results in a data read semantic transaction, the read-data will be placed in the Sideband Data Register and may later be read by software. When Sideband Busy is set, Sideband Packet Register, Sideband Data Register and Sideband Address Register fields cannot be written. If the opcode results in a data read semantic transaction, data will be ready at Sideband Data register only when the Sideband Busy is cleared. Fuse block access prevention:To prevent an attacker from using this mechanism to read the fuse block, writing the Fuse Block PortID to the Sideband Port will prevent the SB_busy bit from being set. This effectively 'aborts' the access. The triggered write is effectively dropped. The triggered read would supply whatever happened to be in the IOSF Sideband Doorbell Data register. IOSF SB access prevention :No usage models require IOSF SB accesses to the doorbell registers. No IOSF SB sources should be using IOSF SB accesses to the doorbell register to trigger a doorbell generated IOSF SB message. Software and firmware are PROHIBITED from using IOSF SB accesses to target and trigger accesses from this registers.

Usage of the doorbell mechanism :
From IOSF primary, to initiate a write on IOSF Sideband :
a. Write Data (0x18_2104)
b. Write Address (0x18_2108)
c. Write Packet and Trigger (0x18_2100)
d. Read poll 0x18_2100. When bit 0 = '0', then the write has completed on IOSF Sideband.
From IOSF primary, to initiate a read on IOSF Sideband :
a. Write Address (0x18_2108)
b. Write Packet and Trigger (0x18_2100)
c. Read poll 0x18_2100. When bit 0 = '0', then the read has completed on IOSF Sideband and data is available.
d. Read IOSF SB returned Data (0x18_2104)
If software attempts a read to a register and the result is a UR (Unsupported Request), the busy bit will be cleared with no update of the doorbell data register.

SB_REQ_TRIGGER - SB_REQ_TRIGGER

DWord	Bit	Description
0	31:24	**SB_DevFn**
		Default Value: 00h
		Access: R/W
		Device and Function number to be used for the IOSF SB access. Per the IOSF Specification, this 8-bit field ('fid' in the IOSF Spec) is a unique identifier of a target in a hierarchy of PCI buses (indicates Device Number [31:27] / Function Number [26:24] or Function Number [31:24]). The target is free to utilize this in an agent-specific manner.
	23:16	**SB_Opcode**
		Default Value: 00h
		Access: R/W
		Opcode to be used for the IOSF SB access.
	15:8	**SB_Port**
		Default Value: 00h
		Access: R/W
		Port to be used for the IOSF SB access.
	7:4	**SB_ByteEnables**
		Default Value: 0h
		Access: R/W
		Byte enables to be used for the iOSF SB access.
	3:1	**SB_BAR**
		Default Value: 000b
		Access: R/W
		BAR value
	0	**SB_Busy**
		Default Value: 0b
		Access: RO
		A write to this register will set this bit = '1' and triggers a IOSF SB request. When this bit is '1', the following registers are not IOSF primary write-able (0x18_2100, 0x18_2104, 0x18_2108)The completion of the IOSF SB access will clear this bit. 0 - 0x18_2100, 0x18_2104 and 0x18_2108 are writeable via IOSF Sideband. 1 - An IOSF SB access is in-progress. 0x18_2100, 0x18_2104 and 0x18_2108 are NOT writeable via IOSF Sideband.

SCPD0

SCPD0 - SCPD0		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	18209Ch	
Scratch Pad 0 Register		
DWord	**Bit**	**Description**
0	31:0	**Scratch Pad**
		Default Value: 00000000h
		Access: R/W
		Software scratch pad

SCRATCH1

SCRATCH1 - SCRATCH1		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000 CHV, BSW	
Size (in bits):	32	
Address:	0B11Ch	

DWord	Bit	Description	
0 **Project:** CHV, BSW	31:0	**SCRATCH**	
		Project:	CHV, BSW
		Access:	R/W

SCRATCH for LNCFunit

SCRATCH_LNCF1 - SCRATCH for LNCFunit	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000001 CHV, BSW
Size (in bits):	32
Address:	0B008h

DWord	Bit	Description		
0	31:3	**SCRATCH register for LNCFunit**		
		Project:		CHV, BSW
		Access:		R/W
	2	**Memory fill delay**		
		Access:		R/W
		lncf_csr_lni_gt2_memfill_dis. 0:mem fills gt2 latency will be 1 . 1:mem fill gt2 latency will be same as gt3.		
	1	**flush start delay**		
		Access:		R/W
		lncf_csr_lni_disable_flush_start_delay. 0:Flush processing in LNIunit starts one clock after receiving the flush command default. 1:Flush processing in LNIunit starts in the same clock in which flush command is received.		
	0	**Non-IA coherent atomics enable**		
		Default Value:		1b
		Project:		CHV, BSW
		Access:		R/W
		0: atomics in GTI (). 1: atomics in L3 (non-IA atomic) (Default). Output signal from LNCF unit lncf_csr_lni_glblatmcs_l3. Value for this bit should be same as lbcf_csr_lsqc_glblatmcs_l3 b118[22].Value of this bit should be same as LBCF register bit 0xb11c[8].Adding Xbuf 8 MCP.		

Scratch Register 1

SCRATCH1 - Scratch Register 1		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A188h-0A18Bh	

DWord	Bit	Description
0	31:0	**Scratch1**
		Access: R/W
		Register bits that have no connection to design. Used to enable/disable changes to the design that were put in during the ECO process. none

Scratch Register 2

SCRATCH2 - Scratch Register 2	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0A198h

DWord	Bit	Description
0	31:0	**Scratch2**

Access:	R/W

Register bits that have no connection to design. Used to enable/disable changes to the design that were put in during the ECO process.

Second Buffer Size

<table>
<tr><td colspan="3" align="center">**SBS - Second Buffer Size**</td></tr>
<tr><td>Register Space:</td><td colspan="2">MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td colspan="2">CHV, BSW</td></tr>
<tr><td>Source:</td><td colspan="2">PRM</td></tr>
<tr><td>Default Value:</td><td colspan="2">0x00000000</td></tr>
<tr><td>Size (in bits):</td><td colspan="2">32</td></tr>
<tr><td>Address:</td><td colspan="2">0B424h</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td>**Description**</td></tr>
<tr><td rowspan="3">0</td><td>31:16</td><td>**Second Virtual Buffer Base**

Access: R/W

Second Virtual Buffer Base (SVBB0).
Second Virtual Buffer Base: Programmed by driver to allocate a memory space for performance data storage. The buffer size should be aligned to the size of the memory allocated so it naturally aligns to the base (i.e. for 128KB bit[16]=0, 256KB bit[17:16]=0, 512KB bit[18:16]=0).
Signal - lpconf_lpfc_virtual_base1 [31:16].</td></tr>
<tr><td>15:12</td><td>**Second Buffer Size 0**

Access: R/W

Second Buffer Size: Determines the allowed buffer size for performance data storage.
0000b: 64KB.
0001b: 128KB.
0010b: 256KB.
0011b: 512KB.
…
1111b: 2GB.
Signal - lpconf_lpfc_buffer_size1 [3:0].</td></tr>
<tr><td>11:0</td><td>**Reserved**

Access: RO

Reserved.</td></tr>
</table>

Second Level Batch Buffer Head Pointer Preemption Register

SBB_PREEMPT_ADDR - Second Level Batch Buffer Head Pointer Preemption Register	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	0213Ch-0213Fh
Name:	Second Level Batch Buffer Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_RCSUNIT
Address:	1213Ch-1213Fh
Name:	Second Level Batch Buffer Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_VCSUNIT0
Address:	1A13Ch-1A13Fh
Name:	Second Level Batch Buffer Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_VECSUNIT
Address:	1C13Ch-1C13Fh
Name:	Second Level Batch Buffer Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_VCSUNIT1
Address:	2213Ch-2213Fh
Name:	Second Level Batch Buffer Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_BCSUNIT
Description	
This register gets updated with the DWord-aligned graphics memory address of the PREEMPTABLE command in the second level batch buffer on which preemption has occurred. This register value should be looked at only when the preemption has occurred in the second level batch buffer. This is indicated by "Ring/Batch Indicator" in "RING_BUFFER_HEAD_PREEMPT_REG". This register value retains its previous value and doesn't change when the preemption occurs on a preemptable command in ring buffer or in batch buffer. Preemption is triggered by valid UHPTR in ring buffer mode of scheduling and by a pending execlist in Exec-List mode of scheduling. This is a global register and context save/restored as part of power context image.	

SBB_PREEMPT_ADDR - Second Level Batch Buffer Head Pointer Preemption Register

Preemptable Commands	Source
MI_ARB_CHECK 3D_PRIMITIVE GPGPU_WALKER MEDIA_STATE_FLUSH PIPE_CONTROL (Only in GPGPU mode of pipeline selection) MI_ATOMIC (Post Sync Operation set in GPGPU mode of pipeline selection) MI_SEMAPHORE_SIGNAL (Post Sync Operation set in GPGPU mode of pipeline selection)	RenderCS

Programming Notes
Programming Restriction: This register should NEVER be programmed by driver, this is for HW internal use only.

DWord	Bit	Description
0	31:2	**Second Level Batch Buffer Head Pointer** Format: GraphicsAddress[31:2] This field specifies the DWord-aligned Graphics Memory Address of the PREEMPTABLE command in a batch buffer where the Preemption has occurred.
	1:0	**Reserved** Format: MBZ

Second Level Batch Buffer Head Pointer Register

SBB_ADDR - Second Level Batch Buffer Head Pointer Register	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	CommandStreamer
Default Value:	0x00000000
Access:	RO
Size (in bits):	32

Address:	02114h-02117h
Name:	Second Level Batch Buffer Head Pointer Register
ShortName:	SBB_ADDR_RCSUNIT

Address:	12114h-12117h
Name:	Second Level Batch Buffer Head Pointer Register
ShortName:	SBB_ADDR_VCSUNIT0

Address:	1A114h-1A117h
Name:	Second Level Batch Buffer Head Pointer Register
ShortName:	SBB_ADDR_VECSUNIT

Address:	1C114h-1C117h
Name:	Second Level Batch Buffer Head Pointer Register
ShortName:	SBB_ADDR_VCSUNIT1

Address:	22114h-22117h
Name:	Second Level Batch Buffer Head Pointer Register
ShortName:	SBB_ADDR_BCSUNIT

This register contains the current DWord Graphics Memory Address of the last-initiated batch buffer.

Programming Notes
This register should NEVER be programmed by driver, this is for HW internal use only. This register should not be written by software. These fields should only get written by a context restore. Software should always set these fields via the MI_BATCH_BUFFER_START command when initiating a batch buffer. This register is saved and restored with context.

DWord	Bit	Description
0	31:2	**Second Level Batch Buffer Head Pointer**
		Format: GraphicsAddress[31:2]
		This field specifies the DWord-aligned Graphics Memory Address where the last initiated Second Level Batch Buffer is currently fetching commands. This field is meaningful only when Valid field is set to "1".
	1	**Reserved**
		Format: MBZ

SBB_ADDR - Second Level Batch Buffer Head Pointer Register

	0	**Valid**			
		Format:		U1	

Value	Name	Description	Project
0h	Invalid **[Default]**	Second Level Batch buffer Invalid	CHV, BSW
1h	Valid	Second Batch buffer Valid.	CHV, BSW

Second Level Batch Buffer State Register

SBB_STATE - Second Level Batch Buffer State Register	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00000000 CHV, BSW
Access:	R/W
Size (in bits):	32

Address:	02118h

Address:	12118h-1211Bh
Name:	Second Level Batch Buffer State Register
ShortName:	SBB_STATE_VCSUNIT0

Address:	1A118h-1A11Bh
Name:	Second Level Batch Buffer State Register
ShortName:	SBB_STATE_VECSUNIT

Address:	1C118h-1C11Bh
Name:	Second Level Batch Buffer State Register
ShortName:	SBB_STATE_VCSUNIT1

Address:	22118h-2211Bh
Name:	Second Level Batch Buffer State Register
ShortName:	SBB_STATE_BCSUNIT

This register contains the attributes of the second level batch buffer initiated from the batch Buffer.

This register should not be written by software. These fields should only get written by a context restore. Software should always set these fields via the MI_BATCH_BUFFER_START command when initiating a batch buffer. This register is saved and restored with context.

DWord	Bit	Description	
0	31:9	**Reserved**	
		Format:	MBZ
	8	**Reserved**	
		Project:	CHV, BSW
		Format:	MBZ
	7	**Resource Streamer Enable**	
		Format:	U1
		When this bit is set, the Resource Streamer will execute the batch buffer. When this bit is clear the Resource Streamer will not execute the batch buffer.	

SBB_STATE - Second Level Batch Buffer State Register

	6	**Reserved**	
		Project:	CHV, BSW
		Format:	MBZ

	5	**Address Space Indicator**	
		Project:	CHV, BSW

Note: This field reflects the effective address space indicator security level and may not be the same as the Address Space Indicator written using MI_BATCH_BUFFER_START.

Value	Name	Description
0h	GGTT **[Default]**	This second level batch buffer is located in GGTT memory and is privileged
1h	PPGTT	This second level batch buffer is located in PPGTT memory and is non-privileged.

	4	**Reserved**	
		Project:	CHV, BSW
		Format:	MBZ

	3:0	**Reserved**	
		Format:	MBZ

Second Level Batch Buffer Upper Head Pointer Preemption Register

SBB_PREEMPT_ADDR_UDW	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32

Address:	02138h-0213Bh
Name:	Second Level Batch Buffer Upper Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_UDW_RCSUNIT

Address:	12138h-1213Bh
Name:	Second Level Batch Buffer Upper Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_UDW_VCSUNIT0

Address:	1A138h-1A13Bh
Name:	Second Level Batch Buffer Upper Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_UDW_VECSUNIT

Address:	1C138h-1C13Bh
Name:	Second Level Batch Buffer Upper Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_UDW_VCSUNIT1

Address:	22138h-2213Bh
Name:	Second Level Batch Buffer Upper Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_UDW_BCSUNIT

This register contains the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space of the last preempted second level batch buffer. This register follows the same rules as the SBB_PREEMPT_ADDR register.

Programming Notes
Programming Restriction: This register should NEVER be programmed by driver, this is for HW internal use only.

DWord	Bit	Description
0	31:16	**Reserved**
	15:0	**Second Level Batch Buffer Head Pointer Upper DWORD**
		Format: GraphicsAddress[47:32]
		This field specifies the 4GB aligned base address of gfx 4GB virtual address space of the last preempted second level batch buffer.

Second Level Batch Buffer Upper Head Pointer Register

SBB_ADDR_UDW - Second Level Batch Buffer Upper Head Pointer Register	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address: Name: ShortName:	0211Ch-0211Fh Second Level Batch Buffer Upper Head Pointer Register SBB_ADDR_UDW_RCSUNIT
Address: Name: ShortName:	1211Ch-1211Fh Second Level Batch Buffer Upper Head Pointer Register SBB_ADDR_UDW_VCSUNIT0
Address: Name: ShortName:	1A11Ch-1A11Fh Second Level Batch Buffer Upper Head Pointer Register SBB_ADDR_UDW_VECSUNIT
Address: Name: ShortName:	1C11Ch-1C11Fh Second Level Batch Buffer Upper Head Pointer Register SBB_ADDR_UDW_VCSUNIT1
Address: Name: ShortName:	2211Ch-2211Fh Second Level Batch Buffer Upper Head Pointer Register SBB_ADDR_UDW_BCSUNIT

This register contains the current Upper DWord of Graphics Memory Address of the last-initiated batch buffer.
Programming Restriction:
This register should NEVER be programmed by driver. This is for HW internal use only.

DWord	Bit	Description
0	31:16	**Reserved**
		Format: _____ MBZ
	15:0	**Batch Buffer Head Pointer Upper DWORD**
		Format: _____ GraphicsAddress[47:32]
		This field specifies the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space where the last initiated Batch Buffer is currently fetching commands. If no batch buffer is currently active, the Valid bit in BB_ADDR will be 0 and this field is meaningless.

Semaphore Polling Interval on Wait

SEMA_WAIT_POLL - Semaphore Polling Interval on Wait	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	0224Ch
Address:	1224Ch-1224Fh
Name:	Semaphore Polling Interval on Wait
ShortName:	SEMA_WAIT_POLL_VCSUNIT0
Address:	1A24Ch-1A24Fh
Name:	Semaphore Polling Interval on Wait
ShortName:	SEMA_WAIT_POLL_VECSUNIT
Address:	1C24Ch-1C24Fh
Name:	Semaphore Polling Interval on Wait
ShortName:	SEMA_WAIT_POLL_VCSUNIT1
Address:	2224Ch-2224Fh
Name:	Semaphore Polling Interval on Wait
ShortName:	SEMA_WAIT_POLL_BCSUNIT

The SEMA_WAIT_POLL register contains Poll Interval field which specifies the minimum number of microseconds allowed for command streamer to wait before re-fetching the data from the address mentioned in the MI_SEMAPHORE_WAIT command on WAIT Mode set to POLL until the condition is satisfied while the context is not switched out.
When a value of 0 is written the poll interval will be equal to the memory latency of the read completion.

DWord	Bit	Description	
0	31:21	**Reserved**	
		Format:	MBZ
	20:0	**Poll Interval** Minimum number of micro-seconds allowed	

SSID_SID

SSID_SID - SSID_SID		
Register Space:	PCI: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0002Ch	
This register is used to uniquely identify the subsystem where the PCI device resides.		

DWord	Bit	Description
0	31:16	**SUBID**
		Default Value: / 0000h
		Access: / R/W Once
		This value is used to identify the vendor of the subsystem.This register is programmed by BIOS during boot-up.Once written, this register becomes Read_Only. This register is cleared by a Reset.
	15:0	**SUBVID**
		Default Value: / 0000h
		Access: / R/W Once
		This value is used to identify the vendor of the subsystem.This register is programmed by BIOS during boot-up.Once written, this register becomes Read_Only. This register is cleared by a Reset.

Staggered EU/SAMPLER PAUSE on Frequency Change

GFXPAUSE - Staggered EU/SAMPLER PAUSE on Frequency Change		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A000h-0A003h	

DWord	Bit	Description
0	31:19	**Reserved** Access: RO Reserved
	18	**Pause Lock** Access: R/W Lock 0 = Bits of EUPAUSE are R/W 1 = All bits of EUPAUSE are RO (including this lock bit)
	17	**EU Pause Enable** Access: R/W Lock 0 = Disabled; EUs will not be paused during frequency changes 1 = Enabled; EUs will be paused before graphics clocks are gated, and unpaused (staggered per EU) when the clocks are ungated
	16	**Sampler Stall Enable** Access: R/W Lock 0 = Disabled; Sampler will not be paused during frequency changes 1 = Enabled; Sampler will be paused before graphics clocks are gated, and unpaused when the clocks are ungated
	15:0	**Pause Count** Access: R/W Lock This is the minimum time the PMunit waits after asserting the EU or Sampler pause (if those are enabled) before allowing the core clocks to be gated. 0000 = Disabled 0001 - Count 1 CSclk … FFFF = Count 65535 CSclks

Storage 1

STORAGE1 - Storage 1

Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32

Address:		0A500h-0A503h

DWord	Bit	Description
0	31:16	**Wake Rate Counter Render**
		<table><tr><td>Access:</td><td>R/W</td></tr></table>
		When reading, this field holds the number of times that the render well has awakened from RC1 (i.e. the number of times that (pmmr_cs_done & ~gmcrgu_gpm_renderpower_req) changes from 1 to 0) within an evaluation interval. When writing this register, set the render wakerate counter to the value written. The only reason to read this register is preparation for S0ix, though it may be useful for validation. The only reason to write to this register is to resume from S0ix.
	15:0	**Wake Rate Counter Media**
		<table><tr><td>Access:</td><td>R/W</td></tr></table>
		When reading, this field holds the number of times that the media well has awakened from RC1 (i.e. the number of times that (pmmr_vcs_done & pmmr_bcs_done & ~gmcrgu_gpm_mediapower_req) changes from 1 to 0) within an evaluation interval. When writing this register, set the render wakerate counter to the value written. The only reason to read this register is preparation for S0ix, though it may be useful for validation. The only reason to write to this register is to resume from S0ix.

Storage 2

STORAGE2 - Storage 2		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A504h-0A507h	

DWord	Bit	Description	
0	31:24	**Reserved**	
		Access:	RO
	23:0	**RC EI Counter Media**	
		Access:	R/W

Storage 3

STORAGE3 - Storage 3		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A508h-0A50Bh	

DWord	Bit	Description	
0	31:24	**Reserved**	
		Access:	RO
	23:0	**RC EI Counter Render**	
		Access:	R/W

Storage 4

STORAGE4 - Storage 4		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A50Ch-0A50Fh	
DWord	**Bit**	**Description**
0	31:24	**Reserved**
		Access: RO
	23:0	**RC Idle Counter Media**
		Access: R/W

Storage 5

STORAGE5 - Storage 5		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A510h-0A513h	

DWord	Bit	Description	
0	31:24	**Reserved**	
		Access:	RO
	23:0	**RC Idle Counter Render**	
		Access:	R/W

Storage 6

STORAGE6 - Storage 6		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A514h-0A517h	

DWord	Bit	Description	
0	31:24	**Reserved**	
		Access:	RO
	23:0	**RP EI Up Counter**	
		Access:	R/W

Storage 7

STORAGE7 - Storage 7		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A518h-0A51Bh	

DWord	Bit	Description	
0	31:24	**Reserved**	
		Access:	RO
	23:0	**RP EI Up Busy Counter**	
		Access:	R/W

Storage 8

STORAGE8 - Storage 8		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A51Ch-0A51Fh	

DWord	Bit	Description
0	31:24	**Reserved**
		Access: RO
	23:0	**RP EI Down Counter**
		Access: R/W

Storage 9

STORAGE9 - Storage 9		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A520h-0A523h	
DWord	**Bit**	**Description**
0	31:24	**Reserved**
		Access: RO
	23:0	**RP EI Down Busy Counter**
		Access: R/W

Stream Output Num Primitives Written Counter

SO_NUM_PRIMS_WRITTEN[0:3] - Stream Output Num Primitives Written Counter	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Address:	05200h-0521Fh

There is one 64-bit register for each of the 4 supported streams:5200h-5207h SO_NUM_PRIMS_WRITTEN0 (for Stream Out Stream #0)5208h-520Fh SO_NUM_PRIMS_WRITTEN1 (for Stream Out Stream #1)5210h-5217h SO_NUM_PRIMS_WRITTEN2 (for Stream Out Stream #2)5218h-521Fh SO_NUM_PRIMS_WRITTEN3 (for Stream Out Stream #3)These registers are used to count the number of primitives (aka objects: points, lines, triangles) which the SO stage has successfully written to a particular "stream's" Streamed Vertex Output buffers, subject to buffer overflow detection. (See the Stream Output section of the 3D pipeline volume).These registers are part of the context save and restore.

DWord	Bit	Description
0	63:0	**Num Prims Written Count**
		Format: U64
		This count is incremented (by one) every time a GS thread outputs a DataPort Streamed Vertex Buffer Write message with the Increment Num Prims Written bit set in the message header (see the Geometry Shader and Data Port chapters in the 3D Volume.)

Stream Output Primitive Storage Needed Counters

SO_PRIM_STORAGE_NEEDED[0:3] - Stream Output Primitive Storage Needed Counters	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00000000, 0x00000000
Access:	RW. This register is set by the context restore.
Size (in bits):	64
Address:	05240h-0525Fh

There is one 64-bit register for each of the 4 supported streams:

5240h-5247h SO_PRIM_STORAGE_NEEDED0 (for Stream Out Stream #0)
5248h-524Fh SO_PRIM_STORAGE_NEEDED1 (for Stream Out Stream #1)
5250h-5257h SO_PRIM_STORAGE_NEEDED2 (for Stream Out Stream #2)
5258h-525Fh SO_PRIM_STORAGE_NEEDED3 (for Stream Out Stream #3)

These registers are used to count the number of primitives (aka objects: points, lines, triangles) which the SO stage has or would have written to a particular "stream's" Streamed Vertex Output buffers if all buffers had been large enough to accommodate the writes. (See the Stream Output section of the 3D pipeline volume).

These registers are part of the context save and restore.

DWord	Bit	Description
0	63:0	**Prim Storage Needed Count**

Project:	CHV, BSW
Format:	U64

This count is incremented (by one) by the SOL stage for each object (point, line, triangle) it writes or attempts to write to the corresponding stream's output buffers. The count is not affected by the actual number of buffers bound to the stream.

Stream Output Write Offsets

SO_WRITE_OFFSET[0:3] - Stream Output Write Offsets	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00000000
Access:	RW. This register is set by the context restore.
Size (in bits):	32
Address:	05280h-0528Fh

There is one R/W 32-bit register for each of the 4 supported stream output buffer slots:
5280h-5283h SO_WRITE_OFFSET0 (for Stream Out Buffer #0)
5284h-5287h SO_ WRITE_OFFSET1 (for Stream Out Buffer #1)
5288h-528Bh SO_ WRITE_OFFSET2 (for Stream Out Buffer #2)
528Ch-528Fh SO_ WRITE_OFFSET3 (for Stream Out Buffer #3)
These registers are used to set and track a DWord-granular Write Offset for each of the 4 Stream Output Buffer slots. Software can directly write them via MI_LOAD_REGxxx commands. The SOL stage will increment them as part of stream output processing. Software can cause them to be written to memory via MI_STORE_REGxxx commands. (See the Stream Output section of the 3D pipeline volume).
These registers are part of the context save and restore.

Programming Notes
• Software must ensure that no HW stream output operations can be in process or otherwise pending at the point that the MI_LOAD/STORE commands are processed. This will likely require a pipeline flush. • The SOL stage will effectively advance the write offset by the buffer's Surface Pitch after each vertex is written (assuming no overflow is detected in any targetted SO buffer). Under "normal" conditions one would expect software to initialize the WriteOffset to some (possibly zero) multiple of Surface Pitch in order to align vertex writes to the buffer's Base Address, though it is not required to do so.

DWord	Bit	Description	
0	31:2	**Write Offset**	
		Project:	CHV, BSW
		Format:	U30
		This field contains a DWord offset from the corresponding SO buffer's Base Address value. The SOL stage uses this value as a write offset when performing writes to the buffer. The SOL stage will increment this value as a part of performing stream output to the buffer. Note that the SOL stage uses the buffer's Surface Pitch to advance the Write Offset, without regard to the buffer's Base Address (see Programming Notes above).	
	1:0	**Reserved**	
		Format:	MBZ

SWF1

SWF1 - SWF1	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	4F000h
These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.	

DWord	Bit	Description
0	31:0	**SOFTWARE_FLAGS**
		<table><tr><td>Default Value:</td><td>00000000h</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.

SWF2

SWF2 - SWF2	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	4F004h

These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation.
The use of these register is defined by software architecture.

DWord	Bit	Description
0	31:0	**SOFTWARE_FLAGS**

	Default Value:	00000000h
	Access:	R/W

These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation.
The use of these register is defined by software architecture.

SWF3

	SWF3 - SWF3
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	4F008h

These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation.
The use of these register is defined by software architecture.

DWord	Bit	Description
0	31:0	**SOFTWARE_FLAGS**

Default Value:	00000000h
Access:	R/W

These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation.
The use of these register is defined by software architecture.

SWF4

<table>
<tr><td colspan="2" align="center">**SWF4 - SWF4**</td></tr>
<tr><td>Register Space:</td><td>MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td>CHV, BSW</td></tr>
<tr><td>Source:</td><td>PRM</td></tr>
<tr><td>Default Value:</td><td>0x00000000</td></tr>
<tr><td>Size (in bits):</td><td>32</td></tr>
<tr><td>Address:</td><td>4F00Ch</td></tr>
<tr><td colspan="2">These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation.
The use of these register is defined by software architecture.</td></tr>
</table>

DWord	Bit	Description
0	31:0	**SOFTWARE_FLAGS**

Default Value:		00000000h
Access:		R/W

These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation.
The use of these register is defined by software architecture.

SWF5

SWF5 - SWF5	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	4F010h
These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.	

DWord	Bit	Description
0	31:0	**SOFTWARE_FLAGS**

Default Value:	00000000h
Access:	R/W

These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation.
The use of these register is defined by software architecture.

SWF6

<table>
<tr><td colspan="2" align="center">**SWF6 - SWF6**</td></tr>
<tr><td>Register Space:</td><td>MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td>CHV, BSW</td></tr>
<tr><td>Source:</td><td>PRM</td></tr>
<tr><td>Default Value:</td><td>0x00000000</td></tr>
<tr><td>Size (in bits):</td><td>32</td></tr>
<tr><td>Address:</td><td>4F014h</td></tr>
<tr><td colspan="2">These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation.
The use of these register is defined by software architecture.</td></tr>
</table>

DWord	Bit	Description
0	31:0	**SOFTWARE_FLAGS**

		Default Value:	00000000h
		Access:	R/W

These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation.
The use of these register is defined by software architecture.

SWF7

SWF7 - SWF7	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	4F018h
These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.	

DWord	Bit	Description
0	31:0	**SOFTWARE_FLAGS**
		Default Value: 00000000h
		Access: R/W
		These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.

SWF8

<table>
<tr><td colspan="2" align="center">**SWF8 - SWF8**</td></tr>
<tr><td>Register Space:</td><td>MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td>CHV, BSW</td></tr>
<tr><td>Source:</td><td>PRM</td></tr>
<tr><td>Default Value:</td><td>0x00000000</td></tr>
<tr><td>Size (in bits):</td><td>32</td></tr>
<tr><td>Address:</td><td>4F01Ch</td></tr>
<tr><td colspan="2">These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation.
The use of these register is defined by software architecture.</td></tr>
</table>

DWord	Bit	Description
0	31:0	**SOFTWARE_FLAGS** <table><tr><td>Default Value:</td><td>00000000h</td></tr><tr><td>Access:</td><td>R/W</td></tr></table>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.

SWF9

SWF9 - SWF9	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	4F020h

These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation.
The use of these register is defined by software architecture.

DWord	Bit	Description
0	31:0	**SOFTWARE_FLAGS**
		Default Value: 00000000h
		Access: R/W
		These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.

SWF10

SWF10 - SWF10	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	4F024h
These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.	

DWord	Bit	Description
0	31:0	**SOFTWARE_FLAGS**
			Default Value:	00000000h	
			Access:	R/W	
		These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.

SWF11

SWF11 - SWF11	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	4F028h
These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.	

DWord	Bit	Description
0	31:0	**SOFTWARE_FLAGS** Default Value: 00000000h Access: R/W These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.

SWF12

SWF12 - SWF12	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	4F02Ch
These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.	

DWord	Bit	Description
0	31:0	**SOFTWARE_FLAGS**

	Default Value:	00000000h
	Access:	R/W

These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation.
The use of these register is defined by software architecture.

SWF13

SWF13 - SWF13	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	4F030h
These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.	

DWord	Bit	Description
0	31:0	**SOFTWARE_FLAGS**
		Default Value: 00000000h
		Access: R/W
		These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.

SWF14

SWF14 - SWF14	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	4F034h
These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.	

DWord	Bit	Description
0	31:0	**SOFTWARE_FLAGS**
		Default Value: ... 00000000h
		Access: ... R/W
		These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.

SWF15

SWF15 - SWF15	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	4F038h

These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation.
The use of these register is defined by software architecture.

DWord	Bit	Description
0	31:0	**SOFTWARE_FLAGS**
		Default Value: 00000000h
		Access: R/W
		These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.

SWF16

SWF16 - SWF16	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	4F03Ch
These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.	

DWord	Bit	Description
0	31:0	**SOFTWARE_FLAGS**
		Default Value: 00000000h
		Access: R/W
		These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.

SWF17

SWF17 - SWF17	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	4F040h
These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.	

DWord	Bit	Description
0	31:0	**SOFTWARE_FLAGS**

Default Value:	00000000h
Access:	R/W

These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation.
The use of these register is defined by software architecture.

SWF18

<table>
<tr><td colspan="2" align="center">**SWF18 - SWF18**</td></tr>
<tr><td>Register Space:</td><td>MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td>CHV, BSW</td></tr>
<tr><td>Source:</td><td>PRM</td></tr>
<tr><td>Default Value:</td><td>0x00000000</td></tr>
<tr><td>Size (in bits):</td><td>32</td></tr>
<tr><td>Address:</td><td>4F044h</td></tr>
<tr><td colspan="2">These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation.
The use of these register is defined by software architecture.</td></tr>
</table>

DWord	Bit	Description
0	31:0	**SOFTWARE_FLAGS**

		Default Value:	00000000h
		Access:	R/W

These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation.
The use of these register is defined by software architecture.

SWF19

SWF19 - SWF19

Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	4F048h

These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation.
The use of these register is defined by software architecture.

DWord	Bit	Description
0	31:0	**SOFTWARE_FLAGS**

Default Value:	00000000h
Access:	R/W

These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation.
The use of these register is defined by software architecture.

SWF20

SWF20 - SWF20	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	4F04Ch
These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.	

DWord	Bit	Description
0	31:0	**SOFTWARE_FLAGS**
		Default Value: ... 00000000h
		Access: ... R/W
		These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.

SWF21

SWF21 - SWF21	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	4F050h

These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation.
The use of these register is defined by software architecture.

DWord	Bit	Description
0	31:0	**SOFTWARE_FLAGS**
		Default Value: 00000000h
		Access: R/W
		These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.

SWF22

<table>
<tr><td colspan="2" align="center">**SWF22 - SWF22**</td></tr>
<tr><td>Register Space:</td><td>MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td>CHV, BSW</td></tr>
<tr><td>Source:</td><td>PRM</td></tr>
<tr><td>Default Value:</td><td>0x00000000</td></tr>
<tr><td>Size (in bits):</td><td>32</td></tr>
<tr><td>Address:</td><td>4F054h</td></tr>
<tr><td colspan="2">These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation.
The use of these register is defined by software architecture.</td></tr>
</table>

DWord	Bit	Description
0	31:0	**SOFTWARE_FLAGS**

		Default Value:	00000000h
		Access:	R/W

These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation.
The use of these register is defined by software architecture.

SWF23

SWF23 - SWF23	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	4F058h

These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation.
The use of these register is defined by software architecture.

DWord	Bit	Description
0	31:0	**SOFTWARE_FLAGS**

Default Value:	00000000h
Access:	R/W

These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation.
The use of these register is defined by software architecture.

SWF24

<table>
<tr><td colspan="2" align="center">**SWF24 - SWF24**</td></tr>
<tr><td>Register Space:</td><td>MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td>CHV, BSW</td></tr>
<tr><td>Source:</td><td>PRM</td></tr>
<tr><td>Default Value:</td><td>0x00000000</td></tr>
<tr><td>Size (in bits):</td><td>32</td></tr>
<tr><td>Address:</td><td>4F05Ch</td></tr>
<tr><td colspan="2">These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation.
The use of these register is defined by software architecture.</td></tr>
</table>

DWord	Bit	Description
0	31:0	**SOFTWARE_FLAGS**

Default Value:		00000000h
Access:		R/W

These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation.
The use of these register is defined by software architecture.

SWF25

<table>
<tr><td colspan="2" align="center">**SWF25 - SWF25**</td></tr>
<tr><td>Register Space:</td><td>MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td>CHV, BSW</td></tr>
<tr><td>Source:</td><td>PRM</td></tr>
<tr><td>Default Value:</td><td>0x00000000</td></tr>
<tr><td>Size (in bits):</td><td>32</td></tr>
<tr><td>Address:</td><td>4F060h</td></tr>
<tr><td colspan="2">These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation.
The use of these register is defined by software architecture.</td></tr>
</table>

DWord	Bit	Description
0	31:0	**SOFTWARE_FLAGS**

		Default Value:	00000000h
		Access:	R/W

These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation.
The use of these register is defined by software architecture.

SWF26

SWF26 - SWF26		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	4F064h	
These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.		
DWord	**Bit**	**Description**
0	31:0	**SOFTWARE_FLAGS**
		Default Value: 00000000h
		Access: R/W
		These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.

SWF27

<table>
<tr><td colspan="2" align="center">**SWF27 - SWF27**</td></tr>
<tr><td>Register Space:</td><td>MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td>CHV, BSW</td></tr>
<tr><td>Source:</td><td>PRM</td></tr>
<tr><td>Default Value:</td><td>0x00000000</td></tr>
<tr><td>Size (in bits):</td><td>32</td></tr>
<tr><td>Address:</td><td>4F068h</td></tr>
<tr><td colspan="2">These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation.
The use of these register is defined by software architecture.</td></tr>
</table>

DWord	Bit	Description
0	31:0	**SOFTWARE_FLAGS**

		Default Value:	00000000h
		Access:	R/W

These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation.
The use of these register is defined by software architecture.

SWF28

SWF28 - SWF28	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	4F06Ch
These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.	

DWord	Bit	Description
0	31:0	**SOFTWARE_FLAGS**

	Default Value:	00000000h
	Access:	R/W

These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation.
The use of these register is defined by software architecture.

SWF29

<table>
<tr><td colspan="2" align="center">**SWF29 - SWF29**</td></tr>
<tr><td>Register Space:</td><td>MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td>CHV, BSW</td></tr>
<tr><td>Source:</td><td>PRM</td></tr>
<tr><td>Default Value:</td><td>0x00000000</td></tr>
<tr><td>Size (in bits):</td><td>32</td></tr>
<tr><td>Address:</td><td>4F070h</td></tr>
<tr><td colspan="2">These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation.
The use of these register is defined by software architecture.</td></tr>
</table>

DWord	Bit	Description
0	31:0	**SOFTWARE_FLAGS**

Default Value:		00000000h
Access:		R/W

These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation.
The use of these register is defined by software architecture.

SWF30

<table>
<tr><td colspan="3" align="center">**SWF30 - SWF30**</td></tr>
<tr><td>Register Space:</td><td colspan="2">MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td colspan="2">CHV, BSW</td></tr>
<tr><td>Source:</td><td colspan="2">PRM</td></tr>
<tr><td>Default Value:</td><td colspan="2">0x00000000</td></tr>
<tr><td>Size (in bits):</td><td colspan="2">32</td></tr>
<tr><td>Address:</td><td colspan="2">4F074h</td></tr>
<tr><td colspan="3">These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation.
The use of these register is defined by software architecture.</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td>**Description**</td></tr>
<tr><td>0</td><td>31:0</td><td>**SOFTWARE_FLAGS**
<table><tr><td>Default Value:</td><td>00000000h</td></tr><tr><td>Access:</td><td>R/W</td></tr></table>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation.
The use of these register is defined by software architecture.</td></tr>
</table>

SWF31

SWF31 - SWF31	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	4F078h

These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation.
The use of these register is defined by software architecture.

DWord	Bit	Description
0	31:0	**SOFTWARE_FLAGS**
		Default Value: 00000000h
		Access: R/W
		These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.

SWF32

SWF32 - SWF32	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	4F07Ch

These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation.
The use of these register is defined by software architecture.

DWord	Bit	Description
0	31:0	**SOFTWARE_FLAGS**

Default Value:	00000000h
Access:	R/W

These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation.
The use of these register is defined by software architecture.

SWF33

SWF33 - SWF33

Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32

Address:	4F080h

These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation.
The use of these register is defined by software architecture.

DWord	Bit	Description
0	31:0	**SOFTWARE_FLAGS**
		<table><tr><td>Default Value:</td><td>00000000h</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.

SWF34

<table>
<tr><td colspan="2" align="center">**SWF34 - SWF34**</td></tr>
<tr><td>Register Space:</td><td>MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td>CHV, BSW</td></tr>
<tr><td>Source:</td><td>PRM</td></tr>
<tr><td>Default Value:</td><td>0x00000000</td></tr>
<tr><td>Size (in bits):</td><td>32</td></tr>
<tr><td>Address:</td><td>4F084h</td></tr>
<tr><td colspan="2">These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation.
The use of these register is defined by software architecture.</td></tr>
</table>

DWord	Bit	Description
0	31:0	**SOFTWARE_FLAGS** <table><tr><td>Default Value:</td><td>00000000h</td></tr><tr><td>Access:</td><td>R/W</td></tr></table>These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these register is defined by software architecture.

SWF35

SWF35 - SWF35	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	4F088h

These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation.
The use of these register is defined by software architecture.

DWord	Bit	Description
0	31:0	**SOFTWARE_FLAGS**

Default Value:	00000000h
Access:	R/W

These (36 DW) registers are used as scratch pad data storage space and have no direct effect on hardware operation.
The use of these register is defined by software architecture.

SWF36

SWSMISCI

<table>
<tr><td colspan="4" align="center">**SWSMISCI - SWSMISCI**</td></tr>
<tr><td>Register Space:</td><td colspan="3">PCI: 0/2/0</td></tr>
<tr><td>Project:</td><td colspan="3">CHV, BSW</td></tr>
<tr><td>Source:</td><td colspan="3">PRM</td></tr>
<tr><td>Default Value:</td><td colspan="3">0x00000000</td></tr>
<tr><td>Size (in bits):</td><td colspan="3">32</td></tr>
<tr><td>Address:</td><td colspan="3">000E0h</td></tr>
<tr><td colspan="4">Software SMI or SCI.</td></tr>
<tr><td colspan="4">The SCI mechanism for driver / BIOS communication. SMI is a system wide lock interrupt (halts all the cores) as opposed to SCI.</td></tr>
<tr><td colspan="4">The SMI is slowly being phased out.
This register serves 2 purposes: 1) Support selection of SMI or SCI event source (SMISCISEL - bit15) 2) Event trigger (bit 0).
To generate a SW SCI event, software (System BIOS/Graphics driver) should program bit 15 (SMISCISEL) to 1. This is typically programmed once (assuming SMIs are never triggered). On a '0' to '1' subsequent transition in bit 0 of this register (caused by a software write operation), GMCH sends a single SCI message. The SCI will set the DMISCI bit in its TCO1_STS register and TCOSCI_STS bit in its GPE0 register upon receiving this message from DMI.
Once written as 1, software must write a '0' to this bit to clear it, and all other write transitions (1->0, 0->0, 1->1) or if bit 15 is '0' will not cause GMCH to send SCI message to DMI link.
To generate a SW SMI event, software should program bit 15:0 and trigger SMI.</td></tr>
</table>

DWord	Bit	Description	
0	31:16	**RESERVED**	
	15	**SMI_OR_SCI_EVENT_SELECT**	
		Default Value:	0b
		Access:	R/W
		MCS: SMI or SCI event select. 0 = SMI,1 = SCI	
	14:1	**SOFTWARE_SCRATCH_BITS**	
		Default Value:	0000h
		Access:	R/W
		Used by driver to communicate information to SBIOS	
	0	**SMI_OR_SCI_EVENT**	
		Default Value:	0b
		Access:	R/W
		MCE: MCS=1, setting this bit causes an SCI. MCS=0, setting this bit causes an SMI. A 1 to 0, 0 to 0 or 1 to 1 transition of this bit does not trigger any events. The graphics driver writes to this register as a means to interrupt the SBIOS.	

Thread Dispatched Count Register

TDL_THR_DISP_COUNT - Thread Dispatched Count Register		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Address:	0E4BCh	
Valid Projects:	CHV, BSW	

This register provides the count of threads dispatched/valid in the subslice.

DWord	Bit	Description	
0	31:6	**Reserved**	
		Format:	MBZ
	5:0	**Thread Count**	
		Value	**Name**
		0-56	Valid Range

Thread Faulted Count Register

TDL_THR_PF_COUNT - Thread Faulted Count Register	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	0E5BCh
Valid Projects:	CHV, BSW

This register provides the count of threads faulted in each subslice.

DWord	Bit	Description
0	31	**Canonical fault indication bit to CS** The bit is set when a canonical fault on data fetch is reported by EU.
	30:6	**Reserved** Format: MBZ
	5:0	**Thread Count** Value: 0-56 Name: Valid Range

Thread Fault Status Register 0

TDL_THR_PF_STATUS0 - Thread Fault Status Register 0		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Address:	0E6B8h	
This register provides the status of each thread in the SubSlice. A bit set indicates the thread in the specific thread slot is faulted.		
DWord	**Bit**	**Description**
0	31:24	**Row0, EU3, [Reserved, T6-T0]**
	23:16	**Row0, EU2, [Reserved, T6-T0]**
	15:8	**Row0, EU1, [Reserved, T6-T0]**
	7:0	**Row0, EU0, [Reserved, T6-T0]**

Thread Fault Status Register 1

TDL_THR_PF_STATUS1 - Thread Fault Status Register 1	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	0E7B8h

This register provides the status of each thread in the SubSlice. A bit set indicates the thread in the specific thread slot is faulted.

DWord	Bit	Description
0	31:24	**Row1, EU3, [Reserved, T6-T0]**
	23:16	**Row1, EU2, [Reserved, T6-T0]**
	15:8	**Row1, EU1, [Reserved, T6-T0]**
	7:0	**Row1, EU0, [Reserved, T6-T0]**

Thread Load Status Register 0

TDL_THR_STATUS0 - Thread Load Status Register 0		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Address:	0E4B8h	
This register provides the status of each thread in the SubSlice.		
DWord	**Bit**	**Description**
0	31:24	**Row0, EU3, [Reserved, T6-T0]**
	23:16	**Row0, EU2, [Reserved, T6-T0]**
	15:8	**Row0, EU1, [Reserved, T6-T0]**
	7:0	**Row0, EU0, [Reserved, T6-T0]**

Thread Load Status Register 1

TDL_THR_STATUS1 - Thread Load Status Register 1		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Address:	0E5B8h	
This register provides the status of each thread in the SubSlice. A bit set indicates a valid thread is loaded in the thread slot.		
DWord	**Bit**	**Description**
0	31:24	**Row1, EU3, [Reserved, T6-T0]**
	23:16	**Row1, EU2, [Reserved, T6-T0]**
	15:8	**Row1, EU1, [Reserved, T6-T0]**
	7:0	**Row1, EU0, [Reserved, T6-T0]**

Thread Mode Register

<table>
<tr><td colspan="2" align="center">**FF_MODE - Thread Mode Register**</td></tr>
<tr><td>Register Space:</td><td>MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td>CHV, BSW</td></tr>
<tr><td>Source:</td><td>RenderCS</td></tr>
<tr><td>Default Value:</td><td>0x00A00000 CHV, BSW</td></tr>
<tr><td>Access:</td><td>R/W</td></tr>
<tr><td>Size (in bits):</td><td>32</td></tr>
<tr><td>Address:</td><td>020A0h</td></tr>
<tr><td>Valid Projects:</td><td></td></tr>
</table>

This register is used to program the FF shader Mode.

DWord	Bit	Description
0	31	**Reserved**

Project:	CHV, BSW
Format:	MBZ

30	**TDS external Cache Disable**

Project:	CHV, BSW

Value	Name	Description
0b	Enable **[Default]**	The external TDS Cache is enabled if there is enough handles to enable the cache.
1b	Disable	The external TDS Cache is disabled even if there is enough handles to enable the cache. Only the internal TDS Cache will be used.

29:26	**DS Hit Max Value**

Format:	U4

Description	Project
If the number of hits reaches the DS Hit Max Value and there is a pending miss to be dispatched, the DS will dispatch the pending miss vertex as a single dispatch.	
Programming the value beyond the range will have undefined behavior if DS Reference Count Full Force miss enable is 0. When DS Reference Count Full Force miss enable is 1 then the value can be [1, Fh].	CHV, BSW

Value	Name	Project
9	**[Default]**	CHV, BSW
[1,9]		CHV, BSW

FF_MODE - Thread Mode Register

	25:20	**VS Hit Max Value**

Format:	U6

Description
If the number of hits reaches the VS Hit Max Value and there is a pending miss to be dispatched, the VS will dispatch the pending miss vertex as a single dispatch.
Programming the value beyond the range will have undefined behavior if VS Reference Count Full Force miss enable is 0. When VS Reference Count Full Force miss enable is 1 then the value can be [1,3Fh].

Value	**Name**
10	**[Default]**
[1,26]	

	19	**DS Reference Count Full Force Miss Enable**

Project:	CHV, BSW
Format:	Enable

Value	**Name**	**Description**
0b	**[Default]**	On a hit to the DS cache and the associated handle's reference count is full then stall until a derefernce.
1b		On a hit to the DS cache and the associated handle's reference count is full then force the cycle as a miss and allocate a new handle.

Programming Notes
To work around bugs, this must be set to 0.

	18	**Reserved**
	17:16	**Reserved**
	15	**VS Reference Count Full Force Miss Enable**

Format:	U1

Value	**Name**	**Description**
[0,1]		
0b	**[Default]**	On a hit to the VS cache and the associated handle's reference count is full then stall until a derefernce.
1b		On a hit to the VS cache and the associated handle's reference count is full then force the cycle as a miss and allocate a new handle.

Programming Notes	**Project**
To work around bugs, this must be set to 0.	CHV, BSW

FF_MODE - Thread Mode Register

	14:13	**Reserved**	
		Project:	CHV, BSW
		Format:	MBZ
	12	**Reserved**	
		Default Value:	0h
		Project:	CHV, BSW
		Format:	MBZ
	11:7	**Reserved**	
		Format:	MBZ
	6:5	**Reserved**	
		Project:	CHV, BSW
		Format:	MBZ
	4	**Reserved**	
		Default Value:	0h
		Project:	CHV, BSW
		Format:	MBZ
	3:0	**Reserved**	
		Format:	MBZ

Thread Restart Control Register

TDL_THR_RESTART - Thread Restart Control Register	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Access:	WO
Size (in bits):	32
Address:	0E450h
This register provides control to restart page faulted and halted threads in each subslice.	

DWord	Bit	Description
0	31:1	**Reserved**
		Format: MBZ
	0	**Restart All Faulted Threads** A write of 1 to this register restarts all threads that have halted due to page fault.

TILECTL

TILECTL - TILECTL		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	101000h	

DWord	Bit	Description
0	31:3	**Reserved**
		Default Value: 00000000h
		Access: RO
		Reserved
	2	**Reserved**
		Default Value: 0b
		Access: RO
		Reserved.
	1	**TLBPF**
		Default Value: 0b
		Access: R/W
		Store multiple PTE enable 0: Only one Page Table Entry is stored in the Translation Lookaside Table Entry is stored in the Translation Lookaside Buffer cache for tiled cycles. 1: Multiple Page Table Entries are stored in the Translation Lookaside Buffer cache for tiled cycles. If tileX, then 4 entries are stored. If tileY, then 8 entries are stored.
	0	**SWZCTL**
		Default Value: 0b
		Access: R/W
		Not used for CHV, BSW. This register location is updated via GFX Driver prior to enabling DRAM accesses. The Driver needs to obtain the need for memory address swizzling via DRAM configuration registers and set the following bits. x0b - No Address Swizzling x1b - Address bit [6] needs to be swizzled for tiled surfaces

TiledResources Invalid Tile Detection Register

TRINVTILEDETCT - TiledResources Invalid Tile Detection Register	
Register Space:	MMIO: 0/2/0
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	04DECh
Name:	TiledResources Invalid Tile Detection Register
ShortName:	TRINVTILEDETCT

DWord	Bit	Description
0	31:0	**Invalid Tile Detection Value**

Access:		R/W

Value	Name	Description
00000000h	**[Default]**	A 32bit value programmed to enable h/w to perform a match of TR-VA TT entries to detect Invalid Tiles. Hardware will flag each entry and space behind it as Invalid Tile for matched entries.

Tiled Resources Translation Table Control Registers

TRTTE - Tiled Resources Translation Table Control Registers		
Register Space:	MMIO: 0/2/0	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	

Address:	04DF4h	
Name:	Tiled Resources Translation Table Control Register	
ShortName:	TRTTE	

DWord	Bit	Description
0	31:2	**Reserved**
			Access:		RO	
			Value	Name	Description	
			00000000000000000000000000000b	**[Default]**	Reserved	
	1	**TR-VA Translation Table Memory Location**
			Default Value:		0b	
			Access:		R/W	
		This field specifies whether the translation tables for TR to VA are in virtual address space v/s physical (GPA) address space. 0: Tables are in Physical (GPA) space 1: Tables are in Virtual address space
	0	**TR - TT Enable**
			Default Value:		0b	
			Access:		R/W	
		TR translation tables are disabled as default. This field needs to be enabled via s/w to get TR translation active.

TiledResources VA Detection Registers

TRVADR - TiledResources VA Detection Registers		
Register Space:	MMIO: 0/2/0	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04DF0h	
Name:	TiledResources VA Detection Registers	
ShortName:	TRVADR	

DWord	Bit	Description
0	31:8	**Reserved**
		Default Value: 000000h
		Access: RO
	7:4	**TR - VA Mask Value**
		Default Value: 0000b
		Access: R/W
		4bit MASK value that is mapped to incoming address bits[47:44]
		MASK bits are used to identify which address bits need to be considered for compare.
		If particular mask bit is "1", mapping address bit needs to be compared to DATA value provided.
		If "0", corresponding address bit is masked which makes it don't care for compare. (This field defaults to "0000" to disable detection.).
		Note: The only usage model for GFX driver to set this field to "1111". Behaviour of h/w for any other setiing is not defined.
		Note: GFX driver shall use same TRVA MASK value for all contexts.
	3:0	**TR- VA Data Value**
		Access: R/W

Value	Name	Description
0000b	**[Default]**	4bit Data value that is mapped to incoming address bits[47:44]. Data bits are used to compare address values that are not filtered by the TRVAMV for match. Note: GFX driver shall use same TRVA Data value for all contexts

Tiled Resources VA Translation Table L3 ptr - DW0

TRVATTL3PTRDW0 - Tiled Resources VA Translation Table L3 ptr - DW0	
Register Space:	MMIO: 0/2/0
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	04DE0h
Name:	Tiled Resources VA Translation Table L3 ptr - DW0
ShortName:	TRVATTL3PTRDW0

DWord	Bit	Description
0	31:12	**TR - VA transln Table L3 Pointer (Lower Address)**
		Access: R/W
		<table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>00000h</td><td>[Default]</td><td>Lower address bits for tiled resource VA to virtual address translation L3 table</td></tr></table>
	11:0	**Reserved**
		Default Value: 000h
		Access: RO
		Reserved

Tiled Resources VA Translation Table L3 ptr - DW1

TRVATTL3PTRDW1 - Tiled Resources VA Translation Table L3 ptr - DW1	
Register Space:	MMIO: 0/2/0
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	04DE4h
Name:	Tiled Resources VA Translation Table L3 ptr - DW1
ShortName:	TRVATTL3PTRDW1

DWord	Bit	Description
0	31:16	**Reserved**
		Access: RO
		<table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>0000h</td><td>**[Default]**</td><td>Reserved</td></tr></table>
	15:0	**TR - VA transln Table L3 Pointer (Upper Address)**
		Default Value: 0000h
		Access: R/W
		Upper address bits for tiled resource VA to virtual address translation L3 table

TLB_RD_ADDRESS Register

TLB_RD_ADDR - TLB_RD_ADDRESS Register		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04B00h	
DWord	**Bit**	**Description**
0	31:12	**Reserved**
		Default Value: 00000000000000000000b
		Access: RO
	11:0	**Reserved**

TLB_RD_DATA0 Register

TLB_RD_DATA0 - TLB_RD_DATA0 Register		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04B04h	

DWord	Bit	Description	
0	31:0	**TLB_READ_DATA0 Register**	
		Default Value:	00000000h
		Access:	RO
		address [43:12]	

TLB_RD_DATA1 Register

TLB_RD_DATA1 - TLB_RD_DATA1 Register		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04B08h	
DWord	**Bit**	**Description**
0	31:0	**TLB_READ_DATA1 Register**
		Default Value: 00000000h
		Access: RO
		Bit[31:5] Reserved Bit[4] Cycle GTT SEL (1-GGTT Cycle, 0-PPGTT Cycle) Bit[3:0] address [47:44]

Transcode Attack Status Register

TRANS_STAT - Transcode Attack Status Register		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	09034h	
Transcode Attack Status Register		
DWord	**Bit**	**Description**
0	31:1	**RSVD**
		Access: RO
		RSVD
	0	**GKEYS_STATUS**
		Access: RO
		Transcode Attack Status bit

TRNULLDETCT

REG_TEMPLATE - TRNULLDETCT		
Register Space:	MMIO: 0/2/0	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04DE8h	
Name:	TiledResources Null Tile Detection Register	
ShortName:	TRNULLDETCT	

DWord	Bit	Description
0	31:0	**Null Tile Detection Value**

Access: R/W

Value	Name	Description
00000000h	[Default]	A 32bit value programmed to enable h/w to perform a match of TR-VA TT entries to detect Null Tiles. Hardware will flag each entry and space behind it as Null Tile for matched entries.

Turbo Media Control

TMCTL - Turbo Media Control		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A190h-0A193h	

DWord	Bit	Description
0	31:9	**Reserved** <table><tr><td>Access:</td><td>RO</td></tr></table>
	8	**Bypass Media Idle Hysteresis Enable (aka Slice Shutdown)** <table><tr><td>Access:</td><td>R/W</td></tr></table> 1 - Bypass idle hysteresis requirements for making an RC wish. 0 - Honor idle hysteresis <default>
	7:1	**Reserved** <table><tr><td>Access:</td><td>RO</td></tr></table>
	0	**Bypass Render Idle Hysteresis Enable (aka Slice Shutdown)** <table><tr><td>Access:</td><td>R/W</td></tr></table> 1 - Bypass idle hysteresis requirements for making an RC wish. 0 - Honor idle hysteresis <default>

Unblock Message Act to Busy Detection Timer

RCUBMABDTMR - Unblock Message Act to Busy Detection Timer	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	0A0B0h-0A0B3h

When locked exit policy is chosen, the GT core can be woken up in parallel with the IA cores waking up so an MMIO write to GT core might not be coming, or may be later in coming. If after the time programmed in this register is met and graphics is still idle, then RC1(e)/RC6x is allowed to be entered.
0 = 0 usec
1 = 1.28 usec
2 = 2.56 usec
3 = 3.84 usec
FF FFFF = 21.474 sec
pmcr_rc_sleep[23:0]

DWord	Bit	Description
0	31:24	**Reserved**
		Access: RO
		Reserved
	23:0	**Unblock Message Ack to Busy Detection Timer**
		Access: R/W
		When locked exit policy is chosen, the GT core can be woken up in parallel with the IA cores waking up so an MMIO write to GT core might not be coming, or may be later in coming. If after the time programmed in this register is met and graphics is still idle, then RC1(e)/RC6x is allowed to be entered. 0 = 0 usec 1 = 1.28 usec 2 = 2.56 usec 3 = 3.84 usec FF FFFF = 21.474 sec pmcr_rc_sleep[23:0]

Unit Level Clock Gating Control 1

UCGCTL1 - Unit Level Clock Gating Control 1		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x02800000	
Size (in bits):	32	
Address:	09400h	
Unit Level Clock Gating Control Registers.Refer to the Programming notes mentioned near GT Interface Registers in PRM		

DWord	Bit	Description
0	31	**Sarbunit Clock Gating Disable** Access: R/W SARB unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	30	**Reserved** Access: R/W
	29	**Reserved** Access: R/W
	28	**ICunit Clock Gating Disable** Access: R/W ICunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	27	**HIZunit Clock Gating Disable** Access: R/W HIZunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	26	**GWunit Clock Gating Disable** Access: R/W GWunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

UCGCTL1 - Unit Level Clock Gating Control 1

25	**GTIunit Clock Gating Disable**	
	Default Value:	1b
	Access:	R/W

GTI Units Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

24	**GSunit Clock Gating Disable**	
	Access:	R/W

GSunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

23	**GPMunit Clock Gating Disable**	
	Default Value:	1b
	Access:	R/W

GPMunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

22	**GAMunit Clock Gating Disable**	
	Default Value:	0b
	Access:	R/W

GAMunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

21	**GACunit Clock Gating Disable**	
	Default Value:	0b
	Access:	R/W

GACunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

UCGCTL1 - Unit Level Clock Gating Control 1

20	**GABunit Clock Gating Disable**	
	Default Value:	0b
	Access:	R/W

GABunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

19	**FTunit Clock Gating Disable**	
	Access:	R/W

FTunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

18	**FLunit Clock Gating Disable**	
	Access:	R/W

FLunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

17	**EU_FPUunit Clock Gating Disable**	
	Access:	R/W

EU_FPUunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

16	**EU_TCunit Clock Gating Disable**	
	Access:	R/W

EU_TCunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

15	**EU_EMunit Clock Gating Disable**	
	Access:	R/W

EU_EMunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

UCGCTL1 - Unit Level Clock Gating Control 1

14	**EU_GAunit Clock Gating Disable**	
	Access:	R/W

EU_GAunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

13	**EUunit Clock Gating Disable**	
	Access:	R/W

EUunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

12	**SVLunit Clock Gating Disable**	
	Access:	R/W

SVLunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

11	**DTunit Clock Gating Disable**	
	Access:	R/W

DTunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

10	**DMunit Clock Gating Disable**	
	Access:	R/W

DMunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

9	**DGunit Clock Gating Disable**	
	Access:	R/W

DGunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

UCGCTL1 - Unit Level Clock Gating Control 1

	8	**DAPunit Clock Gating Disable**	
		Access:	R/W
		DAPunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	7	**CSunit Clock Gating Disable**	
		Access:	R/W
		CSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	6	**CLunit Clock Gating Disable**	
		Access:	R/W
		CLunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	5	**BLBunit Clock Gating Disable**	
		Access:	R/W
		BLBunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	4	**BFunit Clock Gating Disable**	
		Access:	R/W
		BFunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	3	**BDunit Clock Gating Disable**	
		Access:	R/W
		BDunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	

UCGCTL1 - Unit Level Clock Gating Control 1

	2	**BCSunit Clock Gating Disable**

Access:	R/W

BCSunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

	1	**AVSunit Clock Gating Disable**

Access:	R/W

AVSunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

	0	**SPARE RAM Clock Gating Disable**

Access:	R/W

SPARE RAM Clock Gating Disable Control:
'0' : RAM Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : RAM Clock Gating Disabled. (i.e., clocks are toggling, always)

Unit Level Clock Gating Control 1

		UCGCTL1 - Unit Level Clock Gating Control 1

Register Space: MMIO: 0/2/0

Project: CHV, BSW

Source: PRM

Default Value: 0x02F00000

Size (in bits):   32

Address: 09400h

Unit Level Clock Gating Control Registers.

DWord	Bit	Description
0	31	**Sarbunit Clock Gating Disable** Access: R/W SARB unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	30	**Reserved** Access: R/W
	29	**Reserved** Access: R/W
	28	**ICunit Clock Gating Disable** Access: R/W ICunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	27	**HIZunit Clock Gating Disable** Access: R/W HIZunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	26	**GWunit Clock Gating Disable** Access: R/W GWunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

UCGCTL1 - Unit Level Clock Gating Control 1

25	**GTIunit Clock Gating Disable**	
	Default Value:	1b
	Access:	R/W

GTI Units Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

24	**GSunit Clock Gating Disable**	
	Access:	R/W

GSunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

23	**GPMunit Clock Gating Disable**	
	Default Value:	1b
	Access:	R/W

GPMunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

22	**GAMunit Clock Gating Disable**	
	Default Value:	1b
	Access:	R/W

GAMunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

21	**GACunit Clock Gating Disable**	
	Default Value:	1b
	Access:	R/W

GACunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

20	**GABunit Clock Gating Disable**	
	Default Value:	1b

UCGCTL1 - Unit Level Clock Gating Control 1

	Access:	R/W

GABunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

	19	**FTunit Clock Gating Disable**

Access:		R/W

FTunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

	18	**FLunit Clock Gating Disable**

Access:		R/W

FLunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

	17	**EU_FPUunit Clock Gating Disable**

Access:		R/W

EU_FPUunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

	16	**EU_TCunit Clock Gating Disable**

Access:		R/W

EU_TCunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

	15	**EU_EMunit Clock Gating Disable**

Access:		R/W

EU_EMunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

UCGCTL1 - Unit Level Clock Gating Control 1

	14	**EU_GAunit Clock Gating Disable**	
		Access:	R/W

EU_GAunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

	13	**EUunit Clock Gating Disable**	
		Access:	R/W

EUunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

	12	**SVLunit Clock Gating Disable**	
		Access:	R/W

SVLunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

	11	**DTunit Clock Gating Disable**	
		Access:	R/W

DTunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

	10	**DMunit Clock Gating Disable**	
		Access:	R/W

DMunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

	9	**DGunit Clock Gating Disable**	
		Access:	R/W

DGunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

UCGCTL1 - Unit Level Clock Gating Control 1

8	**DAPunit Clock Gating Disable**	
	Access:	R/W
	DAPunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
7	**CSunit Clock Gating Disable**	
	Access:	R/W
	CSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
6	**CLunit Clock Gating Disable**	
	Access:	R/W
	CLunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
5	**BLBunit Clock Gating Disable**	
	Access:	R/W
	BLBunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
4	**BFunit Clock Gating Disable**	
	Access:	R/W
	BFunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
3	**BDunit Clock Gating Disable**	
	Access:	R/W
	BDunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	

UCGCTL1 - Unit Level Clock Gating Control 1

	2	**BCSunit Clock Gating Disable**	
		Access:	R/W
		BCSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	1	**AVSunit Clock Gating Disable**	
		Access:	R/W
		AVSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	0	**SPARE RAM Clock Gating Disable**	
		Access:	R/W
		SPARE RAM Clock Gating Disable Control: '0' : RAM Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : RAM Clock Gating Disabled. (i.e., clocks are toggling, always)	

Unit Level Clock Gating Control 2

UCGCTL2 - Unit Level Clock Gating Control 2		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	09404h	
Unit Level Clock Gating Control Registers.Refer to the Programming notes mentioned near GT Interface Registers in PRM		

DWord	Bit	Description
0	31	**VFunit Clock Gating Disable**
		Access: R/W
		VFunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	30	**VDSunit Clock Gating Disable**
		Access: R/W
		VDSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	29	**VDIunit Clock Gating Disable**
		Access: R/W
		VDIunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	28	**VCSunit Clock Gating Disable**
		Access: R/W
		VCSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

UCGCTL2 - Unit Level Clock Gating Control 2

27	**DTOunit Clock Gating Disable**	
	Access:	R/W
	DTOunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	

26	**VCPunit Clock Gating Disable**	
	Access:	R/W
	VCPunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	

25	**VCDunit Clock Gating Disable**	
	Access:	R/W
	VCDunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	

24	**URBMunit Clock Gating Disable**	
	Access:	R/W
	URBMunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	

23	**TSGunit Clock Gating Disable**	
	Access:	R/W
	TSGunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	

22	**TDLunit Clock Gating Disable**	
	Access:	R/W
	TDLunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	

UCGCTL2 - Unit Level Clock Gating Control 2

	21	**TDSunit Clock Gating Disable**	
		Access:	R/W
		TDSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	20	**SVSMunit Clock Gating Disable**	
		Access:	R/W
		SVSMunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	19	**SVGunit Clock Gating Disable**	
		Access:	R/W
		SVGunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	18	**SOunit Clock Gating Disable**	
		Access:	R/W
		SOunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	17	**SIunit Clock Gating Disable**	
		Access:	R/W
		SIunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	16	**SFunit Clock Gating Disable**	
		Access:	R/W
		SFunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	

UCGCTL2 - Unit Level Clock Gating Control 2

15	**SECunit Clock Gating Disable**	
	Access:	R/W

SECunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

14	**SCunit Clock Gating Disable**	
	Access:	R/W

SCunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

13	**RCZunit Clock Gating Disable**	
	Access:	R/W

RCZunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

12	**RCPBunit Clock Gating Disable**	
	Access:	R/W

RCPBunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

11	**RCCunit Clock Gating Disable**	
	Access:	R/W

RCCunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

10	**QCunit Clock Gating Disable**	
	Access:	R/W

QCunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

UCGCTL2 - Unit Level Clock Gating Control 2

	3	**TEunit Clock Gating Disable**	
		Access:	R/W
		TEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	2	**TETGunit Clock Gating Disable**	
		Access:	R/W
		TETGunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	1	**MAunit Clock Gating Disable**	
		Access:	R/W
		MAunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	0	**IZunit Clock Gating Disable**	
		Access:	R/W
		IZunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	

Unit Level Clock Gating Control 2

DWord	Bit	Description

<table>
<tr><th colspan="3">UCGCTL2 - Unit Level Clock Gating Control 2</th></tr>
</table>

UCGCTL2 - Unit Level Clock Gating Control 2

Register Space: MMIO: 0/2/0

Project: CHV, BSW

Source: PRM

Default Value: 0x00000000

Size (in bits): 32

Address: 09404h

Unit Level Clock Gating Control Registers.

DWord	Bit	Description
0	31	**VFunit Clock Gating Disable**
		Access: R/W
		VFunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	30	**VDSunit Clock Gating Disable**
		Access: R/W
		VDSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	29	**VDIunit Clock Gating Disable**
		Access: R/W
		VDIunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	28	**VCSunit Clock Gating Disable**
		Access: R/W
		VCSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

UCGCTL2 - Unit Level Clock Gating Control 2

	27	**DTOunit Clock Gating Disable**	
		Access:	R/W
		DTOunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	26	**VCPunit Clock Gating Disable**	
		Access:	R/W
		VCPunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	25	**VCDunit Clock Gating Disable**	
		Access:	R/W
		VCDunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	24	**URBMunit Clock Gating Disable**	
		Access:	R/W
		URBMunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	23	**TSGunit Clock Gating Disable**	
		Access:	R/W
		TSGunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	22	**TDLunit Clock Gating Disable**	
		Access:	R/W
		TDLunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	

UCGCTL2 - Unit Level Clock Gating Control 2

21	**TDSunit Clock Gating Disable**	
	Access:	R/W

TDSunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

20	**SVSMunit Clock Gating Disable**	
	Access:	R/W

SVSMunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

19	**SVGunit Clock Gating Disable**	
	Access:	R/W

SVGunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

18	**SOunit Clock Gating Disable**	
	Access:	R/W

SOunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

17	**SIunit Clock Gating Disable**	
	Access:	R/W

SIunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

16	**SFunit Clock Gating Disable**	
	Access:	R/W

SFunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

UCGCTL2 - Unit Level Clock Gating Control 2

	15	**SECunit Clock Gating Disable**	
		Access:	R/W

SECunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

	14	**SCunit Clock Gating Disable**	
		Access:	R/W

SCunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

	13	**RCZunit Clock Gating Disable**	
		Access:	R/W

RCZunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

	12	**RCPBunit Clock Gating Disable**	
		Access:	R/W

RCPBunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

	11	**RCCunit Clock Gating Disable**	
		Access:	R/W

RCCunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

	10	**QCunit Clock Gating Disable**	
		Access:	R/W

QCunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

UCGCTL2 - Unit Level Clock Gating Control 2

	3	**TEunit Clock Gating Disable**		
		Access:		R/W
		TEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
	2	**TETGunit Clock Gating Disable**		
		Access:		R/W
		TETGunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
	1	**MAunit Clock Gating Disable**		
		Access:		R/W
		MAunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
	0	**IZunit Clock Gating Disable**		
		Access:		R/W
		IZunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		

Unit Level Clock Gating Control 3

<table>
<tr>
<td colspan="3" align="center">**UCGCTL3 - Unit Level Clock Gating Control 3**</td>
</tr>
<tr>
<td>Register Space:</td>
<td colspan="2">MMIO: 0/2/0</td>
</tr>
<tr>
<td>Project:</td>
<td colspan="2">CHV, BSW</td>
</tr>
<tr>
<td>Source:</td>
<td colspan="2">PRM</td>
</tr>
<tr>
<td>Default Value:</td>
<td colspan="2">0x00000000 [CHV:B, CHV:C, CHV:K]</td>
</tr>
<tr>
<td></td>
<td colspan="2">0x04000000 [CHV:A]</td>
</tr>
<tr>
<td>Size (in bits):</td>
<td colspan="2">32</td>
</tr>
<tr>
<td>Address:</td>
<td colspan="2">09408h</td>
</tr>
<tr>
<td colspan="3">Unit Level Clock Gating Control Registers.Refer to the Programming notes mentioned near GT Interface Registers in PRM</td>
</tr>
<tr>
<td>**DWord**</td>
<td>**Bit**</td>
<td align="center">**Description**</td>
</tr>
<tr>
<td>0</td>
<td>31</td>
<td>

Flunits 2nd Clock Gating Disable

Access:	R/W

Flunits 2nd Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

</td>
</tr>
<tr>
<td></td>
<td>30</td>
<td>

SVRRunit Clock Gating Disable

Access:	R/W

SVRRunits' Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

</td>
</tr>
<tr>
<td></td>
<td>29</td>
<td>

VCRunit Clock Gating Disable

Access:	R/W

VCRunits' Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

</td>
</tr>
<tr>
<td></td>
<td>28</td>
<td>

EDTunit Clock Gating Disable

Access:	R/W

EDTunits' Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

</td>
</tr>
</table>

UCGCTL3 - Unit Level Clock Gating Control 3

	27	**VClunit Clock Gating Disable**	
		Access:	R/W

VClunits' Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

	26	**HEVC DOP Gating Enable**	
		Default Value:	1b
		Project:	CHV, BSW
		Access:	R/W

HEVCUNIT' Clock Gating Enable Control:
'0' : VIDPAR8/VIDPAR9 DOP gating is not affected by this bit (i.e., this bit does not affect functional DOP gating)
'1' : VIDPAR8/VIDPAR9 cmclk/cuclk DOP's are gated. (i.e., functional clocks aren't toggling, always)

	26	**HEVC DOP Gating Enable**	
		Default Value:	0b
		Project:	CHV, BSW
		Access:	R/W

HEVCUNIT' Clock Gating Enable Control:
'0' : VIDPAR8/VIDPAR9 DOP gating is not affected by this bit (i.e., this bit does not affect functional DOP gating)
'1' : VIDPAR8/VIDPAR9 cmclk/cuclk DOP's are gated. (i.e., functional clocks aren't toggling, always)

	25	**HSunit Clock Gating Disable**	
		Access:	R/W

HSunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

	24	**SOLunit Clock Gating Disable**	
		Access:	R/W

SOLunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

UCGCTL3 - Unit Level Clock Gating Control 3

23	**QRCunit Clock Gating Disable**	
	Access:	R/W
	QRCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	

22	**MSPBISTunit Clock Gating Disable**	
	Access:	R/W
	MSPBISTunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	

21	**BSPunit Clock Gating Disable**	
	Access:	R/W
	BSPunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	

20	**Reserved**

19	**SBEunit Clock Gating Disable**	
	Access:	R/W
	SBEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	

18	**BCunit Clock Gating Disable**	
	Access:	R/W
	BCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	

17	**WMBE Clock Gating Disable**	
	Access:	R/W
	WMBEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	

UCGCTL3 - Unit Level Clock Gating Control 3

16	**WMFEunit Clock Gating Disable**	
	Access:	R/W

WMFEunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

15	**VSCunit Clock Gating Disable**	
	Access:	R/W

VSCunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

14	**Reserved**

13	**USBunit Clock Gating Disable**	
	Access:	R/W

USBunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

12	**STCunit Clock Gating Disable**	
	Access:	R/W

STCunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

11	**VSunit Clock Gating Disable**	
	Access:	R/W

VSunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

10	**VOPunit Clock Gating Disable**	
	Access:	R/W

VOPunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

UCGCTL3 - Unit Level Clock Gating Control 3

9	**VMXunit Clock Gating Disable**	
	Access:	R/W

VMXunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

8	**VMEunit Clock Gating Disable**	
	Access:	R/W

VMEunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

7	**VMDunit Clock Gating Disable**	
	Access:	R/W

VMDunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

6	**VMCunit Clock Gating Disable**	
	Access:	R/W

VMCunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

5	**VLFunit Clock Gating Disable**	
	Access:	R/W

VLFunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

4	**VITunit Clock Gating Disable**	
	Access:	R/W

VITunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

UCGCTL3 - Unit Level Clock Gating Control 3

	3	**VIPunit Clock Gating Disable**

Access:	R/W

VIPunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

	2	**VINunit Clock Gating Disable**

Access:	R/W

VINunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

	1	**VFTunit Clock Gating Disable**

Access:	R/W

VFTunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

	0	**VFEunit Clock Gating Disable**

Access:	R/W

VFEunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

Unit Level Clock Gating Control 3

UCGCTL3 - Unit Level Clock Gating Control 3		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x04000000	
Size (in bits):	32	
Address:	09408h	
Unit Level Clock Gating Control Registers.		

DWord	Bit	Description
0	31	**Flunits 2nd Clock Gating Disable**
		Access: R/W
		Flunits 2nd Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	30	**SVRRunit Clock Gating Disable**
		Access: R/W
		SVRRunits' Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	29	**VCRunit Clock Gating Disable**
		Access: R/W
		VCRunits' Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	28	**EDTunit Clock Gating Disable**
		Access: R/W
		EDTunits' Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

UCGCTL3 - Unit Level Clock Gating Control 3

27	**VClunit Clock Gating Disable**	
	Access:	R/W

VClunits' Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

26	**2x Assign fub XOR Clock Gating Disable**	
	Default Value:	1b
	Access:	R/W

2x Assign fub XOR Clock Gating Disable Control:
'0' : 2x Assign fub XOR Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : 2x Assign fub XOR Clock Gating Disabled. (i.e., clocks are toggling, always)

25	**HSunit Clock Gating Disable**	
	Access:	R/W

HSunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

24	**SOLunit Clock Gating Disable**	
	Access:	R/W

SOLunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

23	**QRCunit Clock Gating Disable**	
	Access:	R/W

QRCunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

22	**MSPBISTunit Clock Gating Disable**	
	Access:	R/W

MSPBISTunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

UCGCTL3 - Unit Level Clock Gating Control 3

21	**BSPunit Clock Gating Disable**	
	Access:	R/W

BSPunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

20	**OACSunit Clock Gating Disable**	
	Access:	R/W

OACSunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

19	**SBEunit Clock Gating Disable**	
	Access:	R/W

SBEunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

18	**BCunit Clock Gating Disable**	
	Access:	R/W

BCunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

17	**WMBE Clock Gating Disable**	
	Access:	R/W

WMBEunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

16	**WMFEunit Clock Gating Disable**	
	Access:	R/W

WMFEunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

UCGCTL3 - Unit Level Clock Gating Control 3

	15	**VSCunit Clock Gating Disable**	
		Access:	R/W
		VSCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	14	**Reserved**	
		Access:	R/W
	13	**USBunit Clock Gating Disable**	
		Access:	R/W
		USBunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	12	**STCunit Clock Gating Disable**	
		Access:	R/W
		STCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	11	**VSunit Clock Gating Disable**	
		Access:	R/W
		VSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	10	**VOPunit Clock Gating Disable**	
		Access:	R/W
		VOPunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	

UCGCTL3 - Unit Level Clock Gating Control 3

<table>
<tr>
<td rowspan="2">9</td>
<td colspan="2">VMXunit Clock Gating Disable</td>
</tr>
<tr>
<td>Access:</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td colspan="2">VMXunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</td>
</tr>
<tr>
<td rowspan="2">8</td>
<td colspan="2">VMEunit Clock Gating Disable</td>
</tr>
<tr>
<td>Access:</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td colspan="2">VMEunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</td>
</tr>
<tr>
<td rowspan="2">7</td>
<td colspan="2">VMDunit Clock Gating Disable</td>
</tr>
<tr>
<td>Access:</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td colspan="2">VMDunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</td>
</tr>
<tr>
<td rowspan="2">6</td>
<td colspan="2">VMCunit Clock Gating Disable</td>
</tr>
<tr>
<td>Access:</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td colspan="2">VMCunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</td>
</tr>
<tr>
<td rowspan="2">5</td>
<td colspan="2">VLFunit Clock Gating Disable</td>
</tr>
<tr>
<td>Access:</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td colspan="2">VLFunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</td>
</tr>
<tr>
<td rowspan="2">4</td>
<td colspan="2">VITunit Clock Gating Disable</td>
</tr>
<tr>
<td>Access:</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td colspan="2">VITunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</td>
</tr>
</table>

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UCGCTL3 - Unit Level Clock Gating Control 3

	3	**VIPunit Clock Gating Disable**		
		Access:		R/W
		VIPunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
	2	**VINunit Clock Gating Disable**		
		Access:		R/W
		VINunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
	1	**VFTunit Clock Gating Disable**		
		Access:		R/W
		VFTunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
	0	**VFEunit Clock Gating Disable**		
		Access:		R/W
		VFEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		

Unit Level Clock Gating Control 4

UCGCTL4 - Unit Level Clock Gating Control 4	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00F80003
Size (in bits):	32
Address:	0940Ch
Unit Level Clock Gating Control Registers.Refer to the Programming notes mentioned near GT Interface Registers in PRM	

DWord	Bit	Description
0	31:30	**Reserved** Access: RO Reserved.
	29	**GAFSRRB unit Clock Gate Disable** Access: R/W GAFSRRB units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	28	**RAMDFT units Clock Gate Disable** Access: R/W RAMDFT units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	27	**TDCunit Clock Gate Disable** Access: R/W TDCunit Clock Gating Disable Control : '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	26	**L3 CBR 1x Clock Gate Disable** Access: R/W L3 CBR units 1x Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

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UCGCTL4 - Unit Level Clock Gating Control 4

<table>
<tr><td>25</td><td colspan="2">L3 BANK 2x Clock Gate Disable</td></tr>
<tr><td></td><td>Access:</td><td>R/W</td></tr>
<tr><td></td><td colspan="2">L3 BANK units 2x Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</td></tr>
<tr><td>24</td><td colspan="2">L3 BANK 1x Clock Gate Diable</td></tr>
<tr><td></td><td>Access:</td><td>R/W</td></tr>
<tr><td></td><td colspan="2">L3 BANK units 1x Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</td></tr>
<tr><td>23</td><td colspan="2">MBGFunit Clock Gate Disable</td></tr>
<tr><td></td><td>Default Value:</td><td>1b</td></tr>
<tr><td></td><td>Access:</td><td>R/W</td></tr>
<tr><td></td><td colspan="2">MBGFunits Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</td></tr>
<tr><td>22</td><td colspan="2">MSQDunit 2x Clock Gate Disable</td></tr>
<tr><td></td><td>Default Value:</td><td>1b</td></tr>
<tr><td></td><td>Access:</td><td>R/W</td></tr>
<tr><td></td><td colspan="2">MSQD units cu2x Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</td></tr>
<tr><td>21</td><td colspan="2">MSQDunit Clock Gate Disable</td></tr>
<tr><td></td><td>Default Value:</td><td>1b</td></tr>
<tr><td></td><td>Access:</td><td>R/W</td></tr>
<tr><td></td><td colspan="2">MSQD units 1x Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</td></tr>
<tr><td>20</td><td colspan="2">MISDunits 2x Clock Gate Disable</td></tr>
<tr><td></td><td>Default Value:</td><td>1b</td></tr>
<tr><td></td><td>Access:</td><td>R/W</td></tr>
<tr><td></td><td colspan="2">MISDunits cu2x Clock Gating Disable Control:</td></tr>
</table>

UCGCTL4 - Unit Level Clock Gating Control 4

		'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
19	**MISDunit Clock Gate Disable**		
	Default Value:		1b
	Access:		R/W
	MISDunits 1x Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
18	**GAFMunit Clock Gate Disable**		
	Access:	R/W	
	GAFMunit' Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
17	**GAPCunit Clock Gate Disable**		
	Access:	R/W	
	GAPCunits Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
16	**GAPZunit Clock Gate Disable**		
	Access:	R/W	
	GAPZunits' Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
15	**GAPL3unit Clock Gate Disable**		
	Access:	R/W	
	GAPL3 units' Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		

UCGCTL4 - Unit Level Clock Gating Control 4

14	**GAFSunit Clock Gate Disable**	
	Access:	R/W

GAFSunits' Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

13	**GAHSunit Clock Gate Disable**	
	Access:	R/W

GAHSunits' Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

12	**VISunit Clock Gate Disable**	
	Access:	R/W

VISunits' Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

11	**VACunit Clock Gate Disable**	
	Access:	R/W

VACunits' Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

10	**VAMunit Clock Gate Disable**	
	Access:	R/W

VAMunits Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

9	**VADuit Clock Gating Disable**	
	Access:	R/W

VADunits Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

UCGCTL4 - Unit Level Clock Gating Control 4

2	**VID1 VINunit Clock Gating Disable**	
	Access:	R/W

VID1 VINunits' Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

1:0	**MSQCunit Clock Gating Disable**	
	Default Value:	11b
	Access:	R/W

MSQCunits' Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

Unit Level Clock Gating Control 4

UCGCTL4 - Unit Level Clock Gating Control 4	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00F80003
Size (in bits):	32
Address:	0940Ch
Unit Level Clock Gating Control Registers.	

DWord	Bit	Description
0	31:30	**Reserved** Access: RO rsvd
	29	**GAFSRRB unit Clock Gate Disable** Access: R/W GAFSRRB units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	28	**RAMDFT units Clock Gate Disable** Access: R/W RAMDFT units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	27	**L3 CBR 2x Clock Gate Disable** Access: R/W L3 CBR units 2x Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	26	**L3 CBR 1x Clock Gate Disable** Access: R/W L3 CBR units 1x Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

UCGCTL4 - Unit Level Clock Gating Control 4

	25	**L3 BANK 2x Clock Gate Disable**	
		Access:	R/W
		L3 BANK units 2x Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	24	**L3 BANK 1x Clock Gate Diable**	
		Access:	R/W
		L3 BANK units 1x Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	23	**MBGFunit Clock Gate Disable**	
		Default Value:	1b
		Access:	R/W
		MBGFunits Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	22	**MSQDunit 2x Clock Gate Disable**	
		Default Value:	1b
		Access:	R/W
		MSQD units cu2x Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	21	**MSQDunit Clock Gate Disable**	
		Default Value:	1b
		Access:	R/W
		MSQD units 1x Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	20	**MISDunits 2x Clock Gate Disable**	
		Default Value:	1b
		Access:	R/W
		MISDunits cu2x Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	

UCGCTL4 - Unit Level Clock Gating Control 4

19	**MISDunit Clock Gate Disable**	
	Default Value:	1b
	Access:	R/W

MISDunits 1x Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

18	**GAFMunit Clock Gate Disable**	
	Access:	R/W

GAFMunit' Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

17	**GAPCunit Clock Gate Disable**	
	Access:	R/W

GAPCunits Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

16	**GAPZunit Clock Gate Disable**	
	Access:	R/W

GAPZunits' Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

15	**GAPL3unit Clock Gate Disable**	
	Access:	R/W

GAPL3 units' Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

14	**GAFSunit Clock Gate Disable**	
	Access:	R/W

GAFSunits' Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

UCGCTL4 - Unit Level Clock Gating Control 4

	13	**GAHSunit Clock Gate Disable**	
		Access:	R/W
		GAHSunits' Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	12	**VISunit Clock Gate Disable**	
		Access:	R/W
		VISunits' Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	11	**VACunit Clock Gate Disable**	
		Access:	R/W
		VACunits' Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	10	**VAMunit Clock Gate Disable**	
		Access:	R/W
		VAMunits Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	9	**VADuit Clock Gating Disable**	
		Access:	R/W
		VADunits Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	8	**JPGunit Clock Gating Disable**	
		Access:	R/W
		JPGunits Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	

UCGCTL4 - Unit Level Clock Gating Control 4

	7	**VBPunits Clock Gating Disable**	
		Access:	R/W
		VBPunits Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	6	**VHRunit Clock Gating Disable**	
		Access:	R/W
		VHRunits Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	5	**VID4 VINunit Clock Gating Disable**	
		Access:	R/W
		VID4 VINunits' Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	4	**VID3 VINunit Clock Gating Disable**	
		Access:	R/W
		VID3 VINunits' Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	3	**VID2 VINunit Clock Gating Disable**	
		Access:	R/W
		VID2 VINunits' Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	2	**VID1 VINunit Clock Gating Disable**	
		Access:	R/W
		VID1 VINunits' Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	

UCGCTL4 - Unit Level Clock Gating Control 4

	1:0	**MSQCunit Clock Gating Disable**	
		Default Value:	11b
		Access:	R/W

MSQCunits' Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

Unit Level Clock Gating Control 5

UCGCTL5 - Unit Level Clock Gating Control 5		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	09418h	

DWord	Bit	Description
0	31	**VCOPunit clock gating disable bit**
		Access: R/W
		WVCOP units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always).
	30	**VMBunit clock gate disable bit**
		Access: R/W
		VMB units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	29	**VDMunit clock gate disable bit**
		Access: R/W
		VDM units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	28	**L3BANK unit cuclkgating disable bit**
		Access: R/W
		L3bank units cuclk Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	27	**L3BANK cu2x clock gate disable bit**
		Access: R/W
		L3BANK units cu2x Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks

UCGCTL5 - Unit Level Clock Gating Control 5

<table>
<tr><td>26</td><td colspan="2">LNIunit clock gate disable bit</td></tr>
<tr><td></td><td>Access:</td><td>R/W</td></tr>
<tr><td></td><td colspan="2">LNI units Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</td></tr>
<tr><td>25</td><td colspan="2">LNEUNIT clock gate disable bit</td></tr>
<tr><td></td><td>Access:</td><td>R/W</td></tr>
<tr><td></td><td colspan="2">LNE units Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</td></tr>
<tr><td>24</td><td colspan="2">VVPunit clock gate disable bit</td></tr>
<tr><td></td><td>Access:</td><td>R/W</td></tr>
<tr><td></td><td colspan="2">VVP units Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</td></tr>
<tr><td>23</td><td colspan="2">WVFT unit clock gate disable bits</td></tr>
<tr><td></td><td>Access:</td><td>R/W</td></tr>
<tr><td></td><td colspan="2">WVFT units Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</td></tr>
<tr><td>22</td><td colspan="2">WBPS unit clock gate disable bit</td></tr>
<tr><td></td><td>Access:</td><td>R/W</td></tr>
<tr><td></td><td colspan="2">WBPS units Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</td></tr>
<tr><td>21</td><td colspan="2">WVMX unit clock gate disable bit</td></tr>
<tr><td></td><td>Access:</td><td>R/W</td></tr>
<tr><td></td><td colspan="2">WVMX units Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</td></tr>
</table>

UCGCTL5 - Unit Level Clock Gating Control 5

<table>
<tr><td>20</td><td colspan="2">WVIP unit clock gate disable bit</td></tr>
<tr><td></td><td>Access:</td><td>R/W</td></tr>
<tr><td></td><td colspan="2">WVIP unit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</td></tr>

<tr><td>19</td><td colspan="2">WVIT unit clock gate disable bit</td></tr>
<tr><td></td><td>Access:</td><td>R/W</td></tr>
<tr><td></td><td colspan="2">WVIT units Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</td></tr>

<tr><td>18</td><td colspan="2">WVIS unit clock gate disable</td></tr>
<tr><td></td><td>Access:</td><td>R/W</td></tr>
<tr><td></td><td colspan="2">WVIS units Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</td></tr>

<tr><td>17</td><td colspan="2">RPM units clock gate disable</td></tr>
<tr><td></td><td>Access:</td><td>R/W</td></tr>
<tr><td></td><td colspan="2">RPM units Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</td></tr>

<tr><td>16</td><td colspan="2">Reserved</td></tr>

<tr><td>15</td><td colspan="2">VECS unit clock gate disable</td></tr>
<tr><td></td><td>Access:</td><td>R/W</td></tr>
<tr><td></td><td colspan="2">VECS units Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</td></tr>

<tr><td>14</td><td colspan="2">GAHSV unit clock gate disable</td></tr>
<tr><td></td><td>Access:</td><td>R/W</td></tr>
<tr><td></td><td colspan="2">GAHSV units Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</td></tr>
</table>

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UCGCTL5 - Unit Level Clock Gating Control 5

	13	**GAHSD unit clock gate disable**	
		Access:	R/W

GAHSD units Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

	12	**GAV unit's clock gate disable**	
		Access:	R/W

GAV units Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

	11	**RSunit's clock gate disable**	
		Access:	R/W

RW units Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

	10	**VFW units clock gate disable**	
		Access:	R/W

VFW units Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

	9	**VCW unit's clock gate disable**	
		Access:	R/W

VCW units Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

	8	**VEO unit's clock gate disable**	
		Access:	R/W

VEO units Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

UCGCTL5 - Unit Level Clock Gating Control 5

	7	**VDN unit's clock gate disable**	
		Access:	R/W
		VDN units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	6	**VTQunit's clock gate disable**	
		Access:	R/W
		VTQunits Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	5	**VPRunit's clock gate disable**	
		Access:	R/W
		VPR units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	4	**IMEunit's clock gate disable**	
		Access:	R/W
		IME units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	3	**CREunit clock gate disable**	
		Access:	R/W
		CRE units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	2	**GAPSL unit clock gate disable**	
		Access:	R/W
		GAPSL units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	

		UCGCTL5 - Unit Level Clock Gating Control 5	

	1	**GAPSU Clock gate disable**	
		Access:	R/W

GAPSU units Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

	0	**SPMunit Clock gate disable**	
		Access:	R/W

SPM units Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

Unit Level Clock Gating Control 5

		UCGCTL5 - Unit Level Clock Gating Control 5

Register Space: MMIO: 0/2/0

Project: CHV, BSW

Source: PRM

Default Value: 0x00000000

Size (in bits): 32

Address: 09418h

DWord	Bit	Description
0	31	**VCOPunit clock gating disable bit**
		Access: R/W
		WVCOP units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always).
	30	**VMBunit clock gate disable bit**
		Access: R/W
		VMB units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	29	**VDMunit clock gate disable bit**
		Access: R/W
		VDM units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	28	**L3BANK unit cuclkgating disable bit**
		Access: R/W
		L3bank units cuclk Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	27	**L3BANK cu2x clock gate disable bit**
		Access: R/W
		L3BANK units cu2x Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks

UCGCTL5 - Unit Level Clock Gating Control 5

26	**LNIunit clock gate disable bit**	
	Access:	R/W

LNI units Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

25	**LNEUNIT clock gate disable bit**	
	Access:	R/W

LNE units Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

24	**VVPunit clock gate disable bit**	
	Access:	R/W

VVP units Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

23	**WVFT unit clock gate disable bits**	
	Access:	R/W

WVFT units Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

22	**WBPS unit clock gate disable bit**	
	Access:	R/W

WBPS units Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

21	**WVMX unit clock gate disable bit**	
	Access:	R/W

WVMX units Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

UCGCTL5 - Unit Level Clock Gating Control 5

20	**WVIP unit clock gate disable bit**	
	Access:	R/W

WVIP unit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

19	**WVIT unit clock gate disable bit**	
	Access:	R/W

WVIT units Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

18	**WVIS unit clock gate disable**	
	Access:	R/W

WVIS units Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

17	**RPM units clock gate disable**	
	Access:	R/W

RPM units Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

16	**OASC unit clock gating disable**	
	Access:	R/W

OASC units Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

15	**VECS unit clock gate disable**	
	Access:	R/W

VECS units Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

UCGCTL5 - Unit Level Clock Gating Control 5

	14	**GAHSV unit clock gate disable**	
		Access:	R/W

GAHSV units Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

	13	**GAHSD unit clock gate disable**	
		Access:	R/W

GAHSD units Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

	12	**GAV unit's clock gate disable**	
		Access:	R/W

GAV units Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

	11	**RSunit's clock gate disable**	
		Access:	R/W

RW units Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

	10	**VFW units clock gate disable**	
		Access:	R/W

VFW units Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

	9	**VCW unit's clock gate disable**	
		Access:	R/W

VCW units Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

UCGCTL5 - Unit Level Clock Gating Control 5

8	**VEO unit's clock gate disable**	
	Access:	R/W

VEO units Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

7	**VDN unit's clock gate disable**	
	Access:	R/W

VDN units Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

6	**VTQunit's clock gate disable**	
	Access:	R/W

VTQunits Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

5	**VPRunit's clock gate disable**	
	Access:	R/W

VPR units Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

4	**IMEunit's clock gate disable**	
	Access:	R/W

IME units Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

3	**CREunit clock gate disable**	
	Access:	R/W

CRE units Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

UCGCTL5 - Unit Level Clock Gating Control 5

2	**GAPSL unit clock gate disable**	
	Access:	R/W
	GAPSL units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
1	**GAPSU Clock gate disable**	
	Access:	R/W
	GAPSU units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
0	**SPMunit Clock gate disable**	
	Access:	R/W
	SPM units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	

Unit Level Clock Gating Control 6

UCGCTL6 - Unit Level Clock Gating Control 6		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	09430h	
Unit Level Clock Gating Disable bits		

DWord	Bit	Description
0	30:28	**HDCunit clock gate disable**
		Access: R/W
		HDC units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	27	**Reserved**
	26	**GACVunit cuclk gate disable**
		Access: R/W
		GACV units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	25	**GACBunit clock gate disable**
		Access: R/W
		GACB units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	24	**GAPSunit clock gate disable**
		Access: R/W
		GAPS units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

UCGCTL6 - Unit Level Clock Gating Control 6

	23	**GAMTunit clock gate disable**	
		Access:	R/W
		GAMT units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	22	**Reserved**	
	21	**Reserved**	
	20	**Reserved**	
	19	**GACVunit clock gate disable**	
		Access:	R/W
		GACV units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	18	**BDMunit clock gate disable**	
		Access:	R/W
		BDM units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	17	**GATSunit clock gate disable**	
		Access:	R/W
		GATS units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	16	**Reserved**	
	15	**STunit clock gate disable**	
		Access:	R/W
		ST units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	

UCGCTL6 - Unit Level Clock Gating Control 6

	14	**SDEunit clock gate disable**	
		Access:	R/W
		DE units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
		Programming Notes	
		Due to SDEUNIT bug HSD#1802092, this bit should be programmed to a 1 for CHV, BSW	
	13	**VIN(VID6) unit clock gate disable**	
		Access:	R/W
		VIN(VID6) units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	12	**VIN(VID5) unit clock gate disable**	
		Access:	R/W
		VIN(VID5) units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	11	**WVOPunit clock gate disable**	
		Access:	R/W
		WVOP units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	10	**WUSB unit clock gate disable**	
		Access:	R/W
		WUSB units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	9	**WSECunit clock gate disable**	
		Access:	R/W
		WSEC units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	

UCGCTL6 - Unit Level Clock Gating Control 6

8	**WRSunit clcok gate disable**	
	Access:	R/W

WRS units Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

7	**WQRCunit clock gate disable**	
	Access:	R/W

WQRC units Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

6	**WMPC unit level clock gate disable**	
	Access:	R/W

WMPC units Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

5	**WINunit Clock gate disable**	
	Access:	R/W

WIN units Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

4	**WIME unit clock gate disable**	
	Access:	R/W

WIME units Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

3	**WHME unit clock gate disable**	
	Access:	R/W

WHME units Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

UCGCTL6 - Unit Level Clock Gating Control 6

<table>
<tr><td>2</td><td colspan="2">**WAVMunit Clock Gate Disable**</td></tr>
<tr><td></td><td>Access:</td><td>R/W</td></tr>
<tr><td></td><td colspan="2">WAVM units Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</td></tr>
<tr><td>1</td><td colspan="2">**VSHMunit clock gate disable**</td></tr>
<tr><td></td><td>Access:</td><td>R/W</td></tr>
<tr><td></td><td colspan="2">VSHM units Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</td></tr>
<tr><td>0</td><td colspan="2">**VSLunit Clock gating disable**</td></tr>
<tr><td></td><td>Access:</td><td>R/W</td></tr>
<tr><td></td><td colspan="2">VSL units Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</td></tr>
</table>

Unit Level Clock Gating Control 6

UCGCTL6 - Unit Level Clock Gating Control 6		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	09430h	
Unit Level Clock Gating Disable bits		

DWord	Bit	Description
0	31	**SPARE 3 clock gate disable**
		Access: R/W
		SPARE 3 unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	30:28	**HDCunit clock gate disable**
		Access: R/W
		HDC units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	27	**MUCunit clock gate disable**
		Access: R/W
		MUC units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	26	**GACVunit cuclk gate disable**
		Access: R/W
		GACV units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

UCGCTL6 - Unit Level Clock Gating Control 6

	25	**GACBunit clock gate disable**	
		Access:	R/W
		GACB units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	24	**GAPSunit clock gate disable**	
		Access:	R/W
		GAPS units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	23	**GAMTunit clock gate disable**	
		Access:	R/W
		GAMT units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	22	**Reserved**	
		Access:	R/W
		GUC units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	21	**OASCREP**	
		Access:	R/W
		OASCREP units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	20	**OAADDRunit clock gate disable bit**	
		Access:	R/W
		OAADDR units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	

UCGCTL6 - Unit Level Clock Gating Control 6

19	**GACVunit clock gate disable**	
	Access:	R/W

GACV units Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

18	**BDMunit clock gate disable**	
	Access:	R/W

BDM units Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

17	**GATSunit clock gate disable**	
	Access:	R/W

GATS units Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

16	**OATREPunit clock gate disable**	
	Access:	R/W

OATREP units Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

15	**STunit clock gate disable**	
	Access:	R/W

ST units Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

14	**DEunit clock gate disable**	
	Access:	R/W

DE units Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

UCGCTL6 - Unit Level Clock Gating Control 6

	13	**VIN(VID6) unit clock gate disable**	
		Access:	R/W
		VIN(VID6) units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	12	**VIN(VID5) unit clock gate disable**	
		Access:	R/W
		VIN(VID5) units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	11	**WVOPunit clock gate disable**	
		Access:	R/W
		WVOP units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	10	**WUSB unit clock gate disable**	
		Access:	R/W
		WUSB units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	9	**WSECunit clock gate disable**	
		Access:	R/W
		WSEC units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	8	**WRSunit clcok gate disable**	
		Access:	R/W
		WRS units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	

UCGCTL6 - Unit Level Clock Gating Control 6

	7	**WQRCunit clock gate disable**	
		Access:	R/W
		WQRC units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	6	**WMPC unit level clock gate disable**	
		Access:	R/W
		WMPC units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	5	**WINunit Clock gate disable**	
		Access:	R/W
		WIN units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	4	**WIME unit clock gate disable**	
		Access:	R/W
		WIME units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	3	**WHME unit clock gate disable**	
		Access:	R/W
		WHME units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	2	**WAVMunit Clock Gate Disable**	
		Access:	R/W
		WAVM units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	

UCGCTL6 - Unit Level Clock Gating Control 6

<table>
<tr><td>1</td><td colspan="2">VSHMunit clock gate disable</td></tr>
<tr><td></td><td>Access:</td><td>R/W</td></tr>
<tr><td></td><td colspan="2">VSHM units Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</td></tr>
<tr><td>0</td><td colspan="2">VSLunit Clock gating disable</td></tr>
<tr><td></td><td>Access:</td><td>R/W</td></tr>
<tr><td></td><td colspan="2">VSL units Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</td></tr>
</table>

Unit Level Clock Gating Control 7

UCGCTL7 - Unit Level Clock Gating Control 7		

Register Space: MMIO: 0/2/0

Project: CHV, BSW

Source: PRM

Default Value: 0x00000000

Size (in bits):   32

Address: 09438h

DWord	Bit	Description
0	31:18	**RSVD**
	17	**cp_cg3ddis_huc**
		Access: R/W
		HUC unit Clock Gating Disable (cp_cg3ddis_huc) HUC unit Clock Gating Disable Control '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	16	**cp_cg3ddis_hwm**
		Access: R/W
		HWM unit Clock Gating Disable (cp_cg3ddis_hwm) HWM unit Clock Gating Disable Control '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	15	**cp_cg3ddis_hed**
		Access: R/W
		HED unit Clock Gating Disable (cp_cg3ddis_hed) HED unit Clock Gating Disable Control '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	14	**cp_cg3ddis_hpp**
		Access: R/W
		HPP unit Clock Gating Disable (cp_cg3ddis_hpp) HPP unit Clock Gating Disable Control '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

UCGCTL7 - Unit Level Clock Gating Control 7

13	**cp_cg3ddis_hpr**	
	Access:	R/W
	HPR unit Clock Gating Disable (cp_cg3ddis_hpr) HPR unit Clock Gating Disable Control '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
12	**cp_cg3ddis_hmc**	
	Access:	R/W
	HMC unit Clock Gating Disable (cp_cg3ddis_hmc) HMC unit Clock Gating Disable Control '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
11	**cp_cg3ddis_hlf**	
	Access:	R/W
	HLF unit Clock Gating Disable (cp_cg3ddis_hlf) HLF unit Clock Gating Disable Control '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
10	**cp_cg3ddis_hmx**	
	Access:	R/W
	HMX unit Clock Gating Disable (cp_cg3ddis_hmx) HMX unit Clock Gating Disable Control '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
9	**cp_cg3ddis_vmm**	
	Access:	R/W
	VMM unit Clock Gating Disable (cp_cg3ddis_vmm) VMM unit Clock Gating Disable Control '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
8	**cp_cg3ddis_mpd**	
	Access:	R/W
	MPD unit Clock Gating Disable (cp_cg3ddis_mpd) MPD unit Clock Gating Disable Control '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	

UCGCTL7 - Unit Level Clock Gating Control 7

	7	cp_cg3ddis_mbd	
		Access:	R/W

MBD unit Clock Gating Disable (cp_cg3ddis_mbd)
MBD unit Clock Gating Disable Control
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

	6	cp_cg3ddis_mlf	
		Access:	R/W

MLF unit Clock Gating Disable (cp_cg3ddis_mlf)
MLF unit Clock Gating Disable Control
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

	5	cp_cg3ddis_mmc	
		Access:	R/W

MMC unit Clock Gating Disable (cp_cg3ddis_mmc)
MMC unit Clock Gating Disable Control
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

	4	cp_cg3ddis_mmx	
		Access:	R/W

MMX unit Clock Gating Disable (cp_cg3ddis_mmx)
MMX unit Clock Gating Disable Control
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

	3	cp_cg3ddisvbsp	
		Access:	R/W

VBSP unit Clock Gating Disable (cp_cg3ddisvbsp)
VBSP unit Clock Gating Disable Control
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

	2	cp_cg3ddisvmpc	
		Access:	R/W

VMPC unit Clock Gating Disable (cp_cg3ddisvmpc)
VMPC unit Clock Gating Disable Control
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

UCGCTL7 - Unit Level Clock Gating Control 7

	1	**cp_cg3ddisvsec**		
		Access:		R/W

VSEC unit Clock Gating Disable (cp_cg3ddisvsec)
VSEC unit Clock Gating Disable Control
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

	0	**cp_cg3ddisjusb**		
		Access:		R/W

JUSB unit Clock Gating Disable (cp_cg3ddisjusb)
JUSB unit Clock Gating Disable Control
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

Unit Level Clock Gating Control 7

UCGCTL7 - Unit Level Clock Gating Control 7	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	09434h
Unit Level Clock Gating Disable bits	

DWord	Bit	Description		
0	31	**wrcunit Clock Gating Disable**		
		Access:		R/W
		wrcunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
	30	**mmcdunit Clock Gating Disable**		
		Access:		R/W
		mmcdunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
	29	**bfceunit Clock Gating Disable**		
		Access:		R/W
		bfceunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
	28	**ecpunit Clock Gating Disable**		
		Access:		R/W
		ecpunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		

UCGCTL7 - Unit Level Clock Gating Control 7

27	**vdlunit1 Clock Gating Disable**	
	Access:	R/W
	vdlunit1 Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	

26	**vhmeunit Clock Gating Disable**	
	Access:	R/W
	vhmeunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	

25	**vimeunit Clock Gating Disable**	
	Access:	R/W
	vimeunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	

24	**vcreunit Clock Gating Disable**	
	Access:	R/W
	vcreunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	

23	**vdxunit Clock Gating Disable**	
	Access:	R/W
	vdxunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	

22	**mdcunit Clock Gating Disable**	
	Access:	R/W
	mdcunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	

UCGCTL7 - Unit Level Clock Gating Control 7

	21	**hpounit Clock Gating Disable**	
		Access:	R/W

hpounit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

	20	**hrsunit Clock Gating Disable**	
		Access:	R/W

hrsunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

	19	**ftunit Clock Gating Disable**	
		Access:	R/W

ftunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

	18	**fqunit Clock Gating Disable**	
		Access:	R/W

fqunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

	17	**hleunit Clock Gating Disable**	
		Access:	R/W

hleunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

	16	**hlcunit Clock Gating Disable**	
		Access:	R/W

hlcunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

UCGCTL7 - Unit Level Clock Gating Control 7

<table>
<tr><td>15</td><td colspan="2">hhiunit Clock Gating Disable</td></tr>
<tr><td></td><td>Access:</td><td>R/W</td></tr>
<tr><td></td><td colspan="2">hhiunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</td></tr>
<tr><td>14</td><td colspan="2">mlfunit Clock Gating Disable</td></tr>
<tr><td></td><td>Access:</td><td>R/W</td></tr>
<tr><td></td><td colspan="2">mlfunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</td></tr>
<tr><td>13</td><td colspan="2">mmcunit Clock Gating Disable</td></tr>
<tr><td></td><td>Access:</td><td>R/W</td></tr>
<tr><td></td><td colspan="2">mmcunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</td></tr>
<tr><td>12</td><td colspan="2">mbdunit Clock Gating Disable</td></tr>
<tr><td></td><td>Access:</td><td>R/W</td></tr>
<tr><td></td><td colspan="2">mbdunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</td></tr>
<tr><td>11</td><td colspan="2">mpdunit Clock Gating Disable</td></tr>
<tr><td></td><td>Access:</td><td>R/W</td></tr>
<tr><td></td><td colspan="2">mpdunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</td></tr>
<tr><td>10</td><td colspan="2">mmxunit Clock Gating Disable</td></tr>
<tr><td></td><td>Access:</td><td>R/W</td></tr>
<tr><td></td><td colspan="2">mmxunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</td></tr>
</table>

UCGCTL7 - Unit Level Clock Gating Control 7

	9	**hedunit Clock Gating Disable**	
		Access:	R/W

hedunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

	8	**hlfunit Clock Gating Disable**	
		Access:	R/W

hlfunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

	7	**hmcunit Clock Gating Disable**	
		Access:	R/W

hmcunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

	6	**hmxunit Clock Gating Disable**	
		Access:	R/W

hmxunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

	5	**hppunit Clock Gating Disable**	
		Access:	R/W

hppunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

	4	**hprunit Clock Gating Disable**	
		Access:	R/W

hprunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

UCGCTL7 - Unit Level Clock Gating Control 7

	3	**hucunit Clock Gating Disable**		
		Access:		R/W

hucunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

	2	**hwmunit Clock Gating Disable**		
		Access:		R/W

hwmunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

	1	**vmpcunit Clock Gating Disable**		
		Access:		R/W

vmpcunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

	0	**vsecunit Clock Gating Disable**		
		Access:		R/W

vsecunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

Unit Level Clock Gating Control 8

UCGCTL8 - Unit Level Clock Gating Control 8	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	09438h
Unit Level Clock Gating Disable bits	

DWord	Bit	Description
0	31	**jusbunit Clock Gating Disable** Access: R/W jusbunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	30	**sfiunit Clock Gating Disable** Access: R/W sfiunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	29	**sfeunit Clock Gating Disable** Access: R/W sfeunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	28	**sfaunit Clock Gating Disable** Access: R/W sfaunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

UCGCTL8 - Unit Level Clock Gating Control 8

27	**sfounit Clock Gating Disable**	
	Access:	R/W

sfounit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

26	**sfxunit Clock Gating Disable**	
	Access:	R/W

sfxunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

25	**sfmunit Clock Gating Disable**	
	Access:	R/W

sfmunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

24	**vmmunit Clock Gating Disable**	
	Access:	R/W

vmmunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

23	**vrtunit Clock Gating Disable**	
	Access:	R/W

vrtunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

22	**ccunit Clock Gating Disable**	
	Access:	R/W

ccunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

UCGCTL8 - Unit Level Clock Gating Control 8

21	gassunit Clock Gating Disable		
	Access:		R/W
	gassunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		

20	gamdunit Clock Gating Disable		
	Access:		R/W
	gamdunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		

19	vdlunit1 Clock Gating Disable		
	Access:		R/W
	vdlunit1 Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		

18	vhmeunit Clock Gating Disable		
	Access:		R/W
	vhmeunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		

17	vcreunit Clock Gating Disable		
	Access:		R/W
	vcreunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		

16	hleunit Clock Gating Disable		
	Access:		R/W
	hleunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		

UCGCTL8 - Unit Level Clock Gating Control 8

<table>
<tr><td>15</td><td colspan="2">mbdunit Clock Gating Disable</td></tr>
<tr><td></td><td>Access:</td><td>R/W</td></tr>
<tr><td></td><td colspan="2">mbdunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</td></tr>

<tr><td>14</td><td colspan="2">mmxunit Clock Gating Disable</td></tr>
<tr><td></td><td>Access:</td><td>R/W</td></tr>
<tr><td></td><td colspan="2">mmxunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</td></tr>

<tr><td>13</td><td colspan="2">mpdunit Clock Gating Disable</td></tr>
<tr><td></td><td>Access:</td><td>R/W</td></tr>
<tr><td></td><td colspan="2">mpdunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</td></tr>

<tr><td>12</td><td colspan="2">hedunit Clock Gating Disable</td></tr>
<tr><td></td><td>Access:</td><td>R/W</td></tr>
<tr><td></td><td colspan="2">hedunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</td></tr>

<tr><td>11</td><td colspan="2">hlfunit Clock Gating Disable</td></tr>
<tr><td></td><td>Access:</td><td>R/W</td></tr>
<tr><td></td><td colspan="2">hlfunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</td></tr>

<tr><td>10</td><td colspan="2">hmcunit Clock Gating Disable</td></tr>
<tr><td></td><td>Access:</td><td>R/W</td></tr>
<tr><td></td><td colspan="2">hmcunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</td></tr>
</table>

UCGCTL8 - Unit Level Clock Gating Control 8

<table>
<tr><td>9</td><td colspan="2">hmxunit Clock Gating Disable</td></tr>
<tr><td></td><td>Access:</td><td>R/W</td></tr>
<tr><td></td><td colspan="2">hmxunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</td></tr>
<tr><td>8</td><td colspan="2">hppunit Clock Gating Disable</td></tr>
<tr><td></td><td>Access:</td><td>R/W</td></tr>
<tr><td></td><td colspan="2">hppunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</td></tr>
<tr><td>7</td><td colspan="2">hprunit Clock Gating Disable</td></tr>
<tr><td></td><td>Access:</td><td>R/W</td></tr>
<tr><td></td><td colspan="2">hprunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</td></tr>
<tr><td>6</td><td colspan="2">hucunit Clock Gating Disable</td></tr>
<tr><td></td><td>Access:</td><td>R/W</td></tr>
<tr><td></td><td colspan="2">hucunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</td></tr>
<tr><td>5</td><td colspan="2">hwmunit Clock Gating Disable</td></tr>
<tr><td></td><td>Access:</td><td>R/W</td></tr>
<tr><td></td><td colspan="2">hwmunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</td></tr>
<tr><td>4</td><td colspan="2">mdcunit Clock Gating Disable</td></tr>
<tr><td></td><td>Access:</td><td>R/W</td></tr>
<tr><td></td><td colspan="2">mdcunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</td></tr>
</table>

UCGCTL8 - Unit Level Clock Gating Control 8

	3	**vmpcunit Clock Gating Disable**	
		Access:	R/W
		vmpcunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	2	**sfmunit Clock Gating Disable ebb**	
		Access:	R/W
		sfmunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	1	**sfaunit Clock Gating Disable ebb**	
		Access:	R/W
		sfaunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	0	**sfeunit Clock Gating Disable ebb**	
		Access:	R/W
		sfeunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	

Unit Level Clock Gating Control 9

UCGCTL9 - Unit Level Clock Gating Control 9		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0943Ch	
Unit Level Clock Gating Disable bits		
DWord	**Bit**	**Description**
0	31:4	**Reserved**
		Access:	RO
		Reserved
	3	**vbspunit Clock Gating Disable**
		Access:	R/W
		vbspunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	2	**vmmunit Clock Gating Disable**
		Access:	R/W
		vmmunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	1	**AVSunit Clock Gating Disable**
		Access:	R/W
		AVSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	0	**daprssunit Clock Gating Disable**
		Access:	R/W
		daprssunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

URB Context Offset

URB_CXT_OFFSET - URB Context Offset		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00009AC0	
Access:	Read/32 bit Write Only	
Size (in bits):	32	
Address:	021B8h	

DWord	Bit	Description
0	31:6	**URB Offset**
		Default Value: 26Bh
		This field indicates the offset (64bytes granular) in to the logical rendering context to which URB contents are save/restored when enabled. This field register must not be written directly (via MMIO) unless the Command Streamer is completely idle (i.e., the Ring Buffer is empty and the pipeline is idle) and RC6 is disabled. One way to program this register is via Load Register Immediate command in the ring buffer as part of initialization sequence.
	5:0	**Reserved**
		Format: MBZ

Valid Bit Vector 0 for CVS

CVSTLB_VLD_0 - Valid Bit Vector 0 for CVS		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04C00h	
This register contains the valid bits for entries 0-31 of CVSTLB.		
DWord	**Bit**	**Description**
0	31:0	**Valid Bit Vector 0 for CVS**
		Default Value: 00000000h
		Access: RO
		Valid Bits per Entry.

Valid Bit Vector 0 for L3

L3TLB_VLD_0 - Valid Bit Vector 0 for L3		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04D00h	

This register contains the valid bits for entries 0-31 of L3TLB.

DWord	Bit	Description		
0	31:0	**Valid Bit Vector 0 for L3**		
		Default Value:		00000000h
		Access:		RO
		Valid Bits per Entry.		

Valid Bit Vector 0 for MFX

MFXTLB_VLD_0 - Valid Bit Vector 0 for MFX		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04BA0h	
This register contains the valid bits for entries 0-31 of MFXTLB.		
DWord	**Bit**	**Description**
0	31:0	**Valid Bit Vector 0 for MFX**
		Default Value: 00000000h
		Access: RO
		Valid Bits per Entry.

Valid Bit Vector 0 for MFX SL1

MFXTLB_VLD_SL1_0 - Valid Bit Vector 0 for MFX SL1	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	04BC0h

This register contains the valid bits for entries 0-31 of MFX SL1 TLB.

DWord	Bit	Description	
0	31:0	**Valid Bit Vector 0 for MFX SL1**	
		Default Value:	00000000h
		Access:	RO
		Valid Bits per Entry.	

Valid Bit Vector 0 for MTTLB

MTTLB_VLD0 - Valid Bit Vector 0 for MTTLB		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	04780h-04783h	
This register contains the valid bits for entries 0-31 of MTTLB (Texture and constant cache TLB).		
DWord	**Bit**	**Description**
0	31:0	**Valid bits per entry**

Valid Bit Vector 0 for MTVICTLB

<table>
<tr><td colspan="2" align="center">**VICTLB_VLD0 - Valid Bit Vector 0 for MTVICTLB**</td></tr>
<tr><td>Register Space:</td><td>MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td>CHV, BSW</td></tr>
<tr><td>Source:</td><td>RenderCS</td></tr>
<tr><td>Default Value:</td><td>0x00000000</td></tr>
<tr><td>Access:</td><td>RO</td></tr>
<tr><td>Size (in bits):</td><td>32</td></tr>
<tr><td>Trusted Type:</td><td>1</td></tr>
<tr><td>Address:</td><td>04788h-0478Bh</td></tr>
<tr><td colspan="2">This register contains the valid bits for entries 0-31 of VICTLB (Vertex Fetch, Instruction Cache, and Command Streamer TLB).</td></tr>
</table>

DWord	Bit	Description
0	31:0	**Valid bits per entry**

Valid Bit Vector 0 for RCC

RCCTLB_VLD_0 - Valid Bit Vector 0 for RCC		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04DA0h	
This register contains the valid bits for entries 0-31 of RCCTLB.		

DWord	Bit	Description
0	31:0	**Valid Bit Vector 0 for RCC**
		Default Value: / 00000000h
		Access: / RO
		Valid Bits per Entry.

Valid Bit Vector 0 for RCCTLB

RCCTLB_VLD0 - Valid Bit Vector 0 for RCCTLB		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	04790h-04793h	
This register contains the valid bits for entries 0-31 of RCCTLB (Render Cache for Color TLB).		
DWord	**Bit**	**Description**
0	31:0	**Valid bits per entry**

Valid Bit Vector 0 for RCZTLB

RCZTLB_VLD0 - Valid Bit Vector 0 for RCZTLB	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	04798h-0479Bh

 This register contains the valid bits for entries 0-31 of RCZTLB (Render Cache for Z (Depth), Hi Z, and Stencil TLB).

DWord	Bit	Description
0	31:0	**Valid bits per entry**

Valid Bit Vector 0 for TLBPEND registers

TLBPEND_VLD0 - Valid Bit Vector 0 for TLBPEND registers		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	04700h-04703h	
This register contains the valid bits for entries 0-31 of TLBPEND structure (Cycles pending TLB translation).		
DWord	**Bit**	**Description**
0	31:0	**Valid bits per entry**

Valid Bit Vector 0 for VEBX

VEBXTLB_VLD_0 - Valid Bit Vector 0 for VEBX		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04B20h	
This register contains the valid bits for entries 0-31 of VEBXTLB.		

DWord	Bit	Description
0	31:0	**Valid Bit Vector 0 for VEBX**

Default Value:	00000000h
Access:	RO
Valid Bits per Entry.	

Valid Bit Vector 0 for WIDI

BWDTLB_VLD_0 - Valid Bit Vector 0 for WIDI		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04DC0h	

This register contains the valid bits for entries 0-31 of BWDTLB.

DWord	Bit	Description
0	31:0	**Valid Bit Vector 0 for WIDI**
		Default Value: 00000000h
		Access: RO
		Valid Bits per Entry.

Valid Bit Vector 0 for Z

ZTLB_VLD_0 - Valid Bit Vector 0 for Z		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04B34h	
This register contains the valid bits for entries 0-31 of ZTLB.		

DWord	Bit	Description
0	31:0	**Valid Bit Vector 0 for Z**
		Default Value: 00000000h
		Access: RO
		Valid Bits per Entry.

Valid Bit Vector 1 for CVS

CVSTLB_VLD_1 - Valid Bit Vector 1 for CVS		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04C04h	
This register contains the valid bits for entries 0-31 of CVSTLB.		

DWord	Bit	Description	
0	31:0	**Valid Bit Vector 1 for CVS**	
		Default Value:	00000000h
		Access:	RO
		Valid Bits per Entry.	

Valid Bit Vector 1 for L3

L3TLB_VLD_1 - Valid Bit Vector 1 for L3		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04D04h	
This register contains the valid bits for entries 0-31 of L3TLB.		

DWord	Bit	Description
0	31:0	**Valid Bit Vector 1 for L3**
		Default Value: ⎮ 00000000h
		Access: ⎮ RO
		Valid Bits per Entry.

Valid Bit Vector 1 for MFX

MFXTLB_VLD_1 - Valid Bit Vector 1 for MFX	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	04BA4h

This register contains the valid bits for entries 0-31 of MFXTLB.

DWord	Bit	Description	
0	31:0	**Valid Bit Vector 1 for MFX**	
		Default Value:	00000000h
		Access:	RO
		Valid Bits per Entry.	

Valid Bit Vector 1 for MFX SL1

MFXTLB_VLD_SL1_1 - Valid Bit Vector 1 for MFX SL1		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04BC4h	
This register contains the valid bits for entries 0-31 of MFX SL1 TLB.		
DWord	**Bit**	**Description**
0	31:0	**Valid Bit Vector 1 for MFX SL1**
		Default Value:
		Access:
		Valid Bits per Entry.

Default Value:	00000000h
Access:	RO

Valid Bit Vector 1 for MTTLB

MTTLB_VLD1 - Valid Bit Vector 1 for MTTLB		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	04784h-04787h	
This register contains the valid bits for entries 0-31 of MTTLB (Texture and constant cache TLBVertex Fetch, Instruction Cache, and Command Streamer TLB).		
DWord	**Bit**	**Description**
0	31:0	**Valid bits per entry**

Valid Bit Vector 1 for MTVICTLB

MTVICTLB_VLD1 - Valid Bit Vector 1 for MTVICTLB		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	0478Ch-0478Fh	
This register contains the valid bits for entries 0-31 of VICTLB (Vertex Fetch, Instruction Cache, and Command Streamer TLB).		
DWord	**Bit**	**Description**
0	31:0	**Valid bits per entry**

Valid Bit Vector 1 for RCC

RCCTLB_VLD_1 - Valid Bit Vector 1 for RCC		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04DA4h	

This register contains the valid bits for entries 0-31 of RCCTLB.

DWord	Bit	Description	
0	31:0	**Valid Bit Vector 1 for RCC**	
		Default Value:	00000000h
		Access:	RO
		Valid Bits per Entry.	

Valid Bit Vector 1 for RCCTLB

RCCTLB_VLD1 - Valid Bit Vector 1 for RCCTLB		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	04794h-04797h	
This register is reserved for future RCC TLB extension.		
DWord	**Bit**	**Description**
0	31:0	**Reserved**
		Format: MBZ

Valid Bit Vector 1 for RCZTLB

RCZTLB_VLD1 - Valid Bit Vector 1 for RCZTLB	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	0479Ch-0479Fh
This register contains the valid bits for entries 0-31 of RCZTLB (Render Cache for Z (Depth), Hi Z, and Stencil TLB).	

DWord	Bit	Description
0	31:0	**Valid bits per entry**

Valid Bit Vector 1 for TLBPEND registers

TLBPEND_VLD1 - Valid Bit Vector 1 for TLBPEND registers	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	04704h-04707h

This register contains the valid bits for entries 32-63 of TLBPEND structure (Cycles pending TLB translation).

DWord	Bit	Description
0	31:0	**Valid bits per entry**

Valid Bit Vector 1 for VEBX

VEBXTLB_VLD_1 - Valid Bit Vector 1 for VEBX		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04B24h	
This register contains the valid bits for entries 0-31 of VEBXTLB.		

DWord	Bit	Description
0	31:0	**Valid Bit Vector 1 for VEBX**
		Default Value: 00000000h
		Access: RO
		Valid Bits per Entry.

Valid Bit Vector 1 for WIDI

BWDTLB_VLD_1 - Valid Bit Vector 1 for WIDI		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04DC4h	

This register contains the valid bits for entries 0-31 of BWDTLB.

DWord	Bit	Description
0	31:0	**Valid Bit Vector 1 for WIDI**
		Default Value: 00000000h
		Access: RO
		Valid Bits per Entry.

Valid Bit Vector 1 for Z

ZTLB_VLD_1 - Valid Bit Vector 1 for Z	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	04B38h

This register contains the valid bits for entries 0-31 of ZTLB.

DWord	Bit	Description	
0	31:0	**Valid Bit Vector 1 for Z**	
		Default Value:	00000000h
		Access:	RO
		Valid Bits per Entry.	

Valid Bit Vector 2 for CVS

CVSTLB_VLD_2 - Valid Bit Vector 2 for CVS		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04C08h	
This register contains the valid bits for entries 0-31 of CVSTLB.		

DWord	Bit	Description	
0	31:0	**Valid Bit Vector 2 for CVS**	
		Default Value:	00000000h
		Access:	RO
		Valid Bits per Entry.	

Valid Bit Vector 2 for GAB

BWDTLB_VLD_3 - Valid Bit Vector 2 for GAB		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04DCCh	

This register contains the valid bits for entries 0-31 of BWDTLB.

DWord	Bit	Description
0	31:0	**Valid Bit Vector 3 for GAB**
		Default Value: 00000000h
		Access: RO
		Valid Bits per Entry.

Valid Bit Vector 2 for L3

L3TLB_VLD_2 - Valid Bit Vector 2 for L3		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04D08h	
This register contains the valid bits for entries 0-31 of L3TLB.		

DWord	Bit	Description
0	31:0	**Valid Bit Vector 2 for L3**
		Default Value: 00000000h
		Access: RO
		Valid Bits per Entry.

Valid Bit Vector 2 for MFX

MFXTLB_VLD_2 - Valid Bit Vector 2 for MFX		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04BA8h	
This register contains the valid bits for entries 0-31 of MFXTLB.		

DWord	Bit	Description
0	31:0	**Valid Bit Vector 2 for MFX**
		Default Value: · 00000000h
		Access: · RO
		Valid Bits per Entry.

Valid Bit Vector 2 for MFX SL1

MFXTLB_VLD_SL1_2 - Valid Bit Vector 2 for MFX SL1		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04BC8h	
This register contains the valid bits for entries 0-31 of MFX SL1 TLB.		
DWord	**Bit**	**Description**
0	31:0	**Valid Bit Vector 2 for MFX SL1**
		Default Value:
		Access:
		Valid Bits per Entry.

DWord	Bit	Description
0	31:0	**Valid Bit Vector 2 for MFX SL1**
		Default Value: 00000000h
		Access: RO
		Valid Bits per Entry.

Valid Bit Vector 2 for RCC

RCCTLB_VLD_2 - Valid Bit Vector 2 for RCC		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04DA8h	
This register contains the valid bits for entries 0-31 of RCCTLB.		

DWord	Bit	Description
0	31:0	**Valid Bit Vector 2 for RCC**

		Default Value:	00000000h
		Access:	RO
		Valid Bits per Entry.	

Valid Bit Vector 2 for Z

ZTLB_VLD_2 - Valid Bit Vector 2 for Z	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	04B3Ch

This register contains the valid bits for entries 0-31 of ZTLB.

DWord	Bit	Description	
0	31:0	**Valid Bit Vector 2 for Z**	
		Default Value:	00000000h
		Access:	RO
		Valid Bits per Entry.	

Valid Bit Vector 3 for CVS

CVSTLB_VLD_3 - Valid Bit Vector 3 for CVS		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04C0Ch	
This register contains the valid bits for entries 0-31 of CVSTLB.		

DWord	Bit	Description
0	31:0	**Valid Bit Vector 3 for CVS**
		Default Value:
		Access:
		Valid Bits per Entry.

Detail of the Description cell:

Default Value:	00000000h
Access:	RO
Valid Bits per Entry.	

Valid Bit Vector 3 for L3

L3TLB_VLD_3 - Valid Bit Vector 3 for L3		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04D0Ch	
This register contains the valid bits for entries 0-31 of L3TLB.		

DWord	Bit	Description	
0	31:0	**Valid Bit Vector 3 for L3**	
		Default Value:	00000000h
		Access:	RO
		Valid Bits per Entry.	

Valid Bit Vector 3 for MFX

MFXTLB_VLD_3 - Valid Bit Vector 3 for MFX	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	04BACh

This register contains the valid bits for entries 0-31 of MFXTLB.

DWord	Bit	Description	
0	31:0	**Valid Bit Vector 3 for MFX**	
		Default Value:	00000000h
		Access:	RO
		Valid Bits per Entry.	

Valid Bit Vector 3 for MFX SL1

MFXTLB_VLD_SL1_3 - Valid Bit Vector 3 for MFX SL1	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	04BCCh

This register contains the valid bits for entries 0-31 of MFX SL1 TLB.

DWord	Bit	Description	
0	31:0	**Valid Bit Vector 3 for MFX SL1**	
		Default Value:	00000000h
		Access:	RO
		Valid Bits per Entry.	

Valid Bit Vector 3 for RCC

<table>
<tr>
<td colspan="3" align="center">**RCCTLB_VLD_3 - Valid Bit Vector 3 for RCC**</td>
</tr>
<tr>
<td>Register Space:</td>
<td colspan="2">MMIO: 0/2/0</td>
</tr>
<tr>
<td>Project:</td>
<td colspan="2">CHV, BSW</td>
</tr>
<tr>
<td>Source:</td>
<td colspan="2">PRM</td>
</tr>
<tr>
<td>Default Value:</td>
<td colspan="2">0x00000000</td>
</tr>
<tr>
<td>Size (in bits):</td>
<td colspan="2">32</td>
</tr>
<tr>
<td>Address:</td>
<td colspan="2">04DACh</td>
</tr>
<tr>
<td colspan="3">This register contains the valid bits for entries 0-31 of RCCTLB.</td>
</tr>
<tr>
<td>**DWord**</td>
<td>**Bit**</td>
<td>**Description**</td>
</tr>
<tr>
<td>0</td>
<td>31:0</td>
<td>

Valid Bit Vector 3 for RCC

Default Value:	00000000h
Access:	RO

Valid Bits per Entry.

</td>
</tr>
</table>

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Valid Bit Vector 3 for Z

ZTLB_VLD_3 - Valid Bit Vector 3 for Z		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04B40h	
This register contains the valid bits for entries 0-31 of ZTLB.		

DWord	Bit	Description
0	31:0	**Valid Bit Vector 3 for Z**
		Default Value: 00000000h
		Access: RO
		Valid Bits per Entry.

Valid Bit Vector 4 for L3

L3TLB_VLD_4 - Valid Bit Vector 4 for L3		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04D10h	
This register contains the valid bits for entries 0-31 of L3TLB.		

DWord	Bit	Description
0	31:0	**Valid Bit Vector 4 for L3**
		Default Value:
		00000000h
		Access:
		RO
		Valid Bits per Entry.

Valid Bit Vector 4 for MFX

MFXTLB_VLD_4 - Valid Bit Vector 4 for MFX		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04BB0h	
This register contains the valid bits for entries 0-31 of MFXTLB.		

DWord	Bit	Description
0	31:0	**Valid Bit Vector 4 for MFX**
		Default Value: 00000000h
		Access: RO
		Valid Bits per Entry.

Valid Bit Vector 4 for MFX SL1

MFXTLB_VLD_SL1_4 - Valid Bit Vector 4 for MFX SL1		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04BD0h	
This register contains the valid bits for entries 0-31 of MFX SL1 TLB.		
DWord	**Bit**	**Description**
0	31:0	**Valid Bit Vector 4 for MFX SL1**
		Default Value: 00000000h
		Access: RO
		Valid Bits per Entry.

Valid Bit Vector 4 for RCC

RCCTLB_VLD_4 - Valid Bit Vector 4 for RCC		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04DB0h	
This register contains the valid bits for entries 0-31 of RCCTLB.		

DWord	Bit	Description
0	31:0	**Valid Bit Vector 4 for RCC**
		Default Value: 00000000h
		Access: RO
		Valid Bits per Entry.

Valid Bit Vector 5 for L3

L3TLB_VLD_5 - Valid Bit Vector 5 for L3		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04D14h	
This register contains the valid bits for entries 0-31 of L3TLB.		

DWord	Bit	Description	
0	31:0	**Valid Bit Vector 5 for L3**	
		Default Value:	00000000h
		Access:	RO
		Valid Bits per Entry.	

Valid Bit Vector 5 for MFX

MFXTLB_VLD_5 - Valid Bit Vector 5 for MFX		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04BB4h	
This register contains the valid bits for entries 0-31 of MFXTLB.		

DWord	Bit	Description
0	31:0	**Valid Bit Vector 5 for MFX**
		Default Value: 00000000h
		Access: RO
		Valid Bits per Entry.

Valid Bit Vector 5 for MFX SL1

MFXTLB_VLD_SL1_5 - Valid Bit Vector 5 for MFX SL1

Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32

Address:	04BD4h

This register contains the valid bits for entries 0-31 of MFX SL1 TLB.

DWord	Bit	Description
0	31:0	**Valid Bit Vector 5 for MFX SL1**
		Default Value: 00000000h
		Access: RO
		Valid Bits per Entry.

Valid Bit Vector 5 for RCC

RCCTLB_VLD_5 - Valid Bit Vector 5 for RCC		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04DB4h	
This register contains the valid bits for entries 0-31 of RCCTLB.		

DWord	Bit	Description
0	31:0	**Valid Bit Vector 5 for RCC**

		Default Value:	00000000h
		Access:	RO
		Valid Bits per Entry.	

Valid Bit Vector 5 for Z

ZTLB_VLD_5 - Valid Bit Vector 5 for Z		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04B48h	
This register contains the valid bits for entries 0-31 of ZTLB.		

DWord	Bit	Description
0	31:0	**Valid Bit Vector 5 for Z**
		Default Value: 00000000h
		Access: RO
		Valid Bits per Entry.

Valid Bit Vector 6 for L3

L3TLB_VLD_6 - Valid Bit Vector 6 for L3		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04D18h	
This register contains the valid bits for entries 0-31 of L3TLB.		

DWord	Bit	Description	
0	31:0	**Valid Bit Vector 6 for L3**	
		Default Value:	00000000h
		Access:	RO
		Valid Bits per Entry.	

Valid Bit Vector 6 for MFX

MFXTLB_VLD_6 - Valid Bit Vector 6 for MFX		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04BB8h	
This register contains the valid bits for entries 0-31 of MFXTLB.		

DWord	Bit	Description
0	31:0	**Valid Bit Vector 6 for MFX**
		Default Value: 00000000h
		Access: RO
		Valid Bits per Entry.

Valid Bit Vector 6 for MFX SL1

MFXTLB_VLD_SL1_6 - Valid Bit Vector 6 for MFX SL1		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04BD8h	
This register contains the valid bits for entries 0-31 of MFX SL1 TLB.		
DWord	**Bit**	**Description**
0	31:0	**Valid Bit Vector 6 for MFX SL1**
		Default Value: 00000000h
		Access: RO
		Valid Bits per Entry.

Valid Bit Vector 6 for RCC

RCCTLB_VLD_6 - Valid Bit Vector 6 for RCC		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04DB8h	
This register contains the valid bits for entries 0-31 of RCCTLB.		

DWord	Bit	Description
0	31:0	**Valid Bit Vector 6 for RCC**
		<table><tr><td>Default Value:</td><td>00000000h</td></tr><tr><td>Access:</td><td>RO</td></tr></table> Valid Bits per Entry.

Valid Bit Vector 6 for Z

ZTLB_VLD_6 - Valid Bit Vector 6 for Z		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04B4Ch	
This register contains the valid bits for entries 0-31 of ZTLB.		
DWord	**Bit**	**Description**
0	31:0	**Valid Bit Vector 6 for Z**
		Default Value: ... 00000000h
		Access: ... RO
		Valid Bits per Entry.

Valid Bit Vector 7 for L3

L3TLB_VLD_7 - Valid Bit Vector 7 for L3		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04D1Ch	

This register contains the valid bits for entries 0-31 of L3TLB.

DWord	Bit	Description	
0	31:0	**Valid Bit Vector 7 for L3**	
		Default Value:	00000000h
		Access:	RO
		Valid Bits per Entry.	

Valid Bit Vector 7 for MFX

MFXTLB_VLD_7 - Valid Bit Vector 7 for MFX		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04BBCh	
This register contains the valid bits for entries 0-31 of MFXTLB.		

DWord	Bit	Description
0	31:0	**Valid Bit Vector 7 for MFX**
		Default Value: 00000000h
		Access: RO
		Valid Bits per Entry.

Valid Bit Vector 7 for MFX SL1

MFXTLB_VLD_SL1_7 - Valid Bit Vector 7 for MFX SL1	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	04BDCh

This register contains the valid bits for entries 0-31 of MFX SL1 TLB.

DWord	Bit	Description	
0	31:0	**Valid Bit Vector 7 for MFX SL1**	
		Default Value:	00000000h
		Access:	RO
		Valid Bits per Entry.	

Valid Bit Vector 7 for RCC

RCCTLB_VLD_7 - Valid Bit Vector 7 for RCC		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04DBCh	
This register contains the valid bits for entries 0-31 of RCCTLB.		

DWord	Bit	Description
0	31:0	**Valid Bit Vector 7 for RCC**
		Default Value: 00000000h
		Access: RO
		Valid Bits per Entry.

Valid Bit Vector 7 for Z

ZTLB_VLD_7 - Valid Bit Vector 7 for Z		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04B50h	
This register contains the valid bits for entries 0-31 of ZTLB.		

DWord	Bit	Description	
0	31:0	**Valid Bit Vector 7 for Z**	
		Default Value:	00000000h
		Access:	RO
		Valid Bits per Entry.	

Valid Bit Vector 8 for L3

L3TLB_VLD_8 - Valid Bit Vector 8 for L3		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04D20h	
This register contains the valid bits for entries 0-31 of L3TLB.		
DWord	**Bit**	**Description**
0	31:0	**Valid Bit Vector 8 for L3**

	Default Value:	00000000h
	Access:	RO

Valid Bits per Entry.

Valid Bit Vector 8 for Z

ZTLB_VLD_8 - Valid Bit Vector 8 for Z		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04B54h	
This register contains the valid bits for entries 0-31 of ZTLB.		

DWord	Bit	Description
0	31:0	**Valid Bit Vector 8 for Z**
		Default Value:
		00000000h
		Access:
		RO
		Valid Bits per Entry.

Valid Bit Vector 9 for L3

L3TLB_VLD_9 - Valid Bit Vector 9 for L3		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04D24h	

This register contains the valid bits for entries 0-31 of L3TLB.

DWord	Bit	Description
0	31:0	**Valid Bit Vector 9 for L3**
		Default Value: 00000000h
		Access: RO
		Valid Bits per Entry.

Valid Bit Vector 9 for Z

ZTLB_VLD_9 - Valid Bit Vector 9 for Z	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	04B58h

This register contains the valid bits for entries 0-31 of ZTLB.

DWord	Bit	Description	
0	31:0	**Valid Bit Vector 9 for Z**	
		Default Value:	00000000h
		Access:	RO
		Valid Bits per Entry.	

Valid Bit Vector 10 for L3

L3TLB_VLD_10 - Valid Bit Vector 10 for L3		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04D28h	
This register contains the valid bits for entries 0-31 of L3TLB.		
DWord	**Bit**	**Description**
0	31:0	**Valid Bit Vector 10 for L3**

Default Value:	00000000h
Access:	RO

Valid Bits per Entry.

Valid Bit Vector 10 for Z

ZTLB_VLD_10 - Valid Bit Vector 10 for Z	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	04B5Ch

This register contains the valid bits for entries 0-31 of ZTLB.

DWord	Bit	Description	
0	31:0	**Valid Bit Vector 10 for Z**	
		Default Value:	00000000h
		Access:	RO
		Valid Bits per Entry.	

Valid Bit Vector 11 for L3

L3TLB_VLD_11 - Valid Bit Vector 11 for L3		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04D2Ch	
This register contains the valid bits for entries 0-31 of L3TLB.		
DWord	**Bit**	**Description**
0	31:0	**Valid Bit Vector 11 for L3**
		Default Value: 00000000h
		Access: RO
		Valid Bits per Entry.

Valid Bit Vector 11 for Z

<table>
<tr>
<td colspan="4" align="center">ZTLB_VLD_11 - Valid Bit Vector 11 for Z</td>
</tr>
<tr>
<td>Register Space:</td>
<td colspan="3">MMIO: 0/2/0</td>
</tr>
<tr>
<td>Project:</td>
<td colspan="3">CHV, BSW</td>
</tr>
<tr>
<td>Source:</td>
<td colspan="3">PRM</td>
</tr>
<tr>
<td>Default Value:</td>
<td colspan="3">0x00000000</td>
</tr>
<tr>
<td>Size (in bits):</td>
<td colspan="3">32</td>
</tr>
<tr>
<td>Address:</td>
<td colspan="3">04B60h</td>
</tr>
<tr>
<td colspan="4">This register contains the valid bits for entries 0-31 of ZTLB.</td>
</tr>
<tr>
<td align="center">DWord</td>
<td align="center">Bit</td>
<td colspan="2" align="center">Description</td>
</tr>
<tr>
<td align="center">0</td>
<td align="center">31:0</td>
<td colspan="2">
Valid Bit Vector 11 for Z

<table>
<tr><td>Default Value:</td><td>00000000h</td></tr>
<tr><td>Access:</td><td>RO</td></tr>
</table>

Valid Bits per Entry.
</td>
</tr>
</table>

Valid Bit Vector 12 for L3

L3TLB_VLD_12 - Valid Bit Vector 12 for L3		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04D30h	
This register contains the valid bits for entries 0-31 of L3TLB.		
DWord	**Bit**	**Description**
0	31:0	**Valid Bit Vector 12 for L3**
		Default Value: 00000000h
		Access: RO
		Valid Bits per Entry.

Valid Bit Vector 12 for Z

ZTLB_VLD_12 - Valid Bit Vector 12 for Z	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	04B64h

This register contains the valid bits for entries 0-31 of ZTLB.

DWord	Bit	Description	
0	31:0	**Valid Bit Vector 12 for Z**	
		Default Value:	00000000h
		Access:	RO
		Valid Bits per Entry.	

Valid Bit Vector 13 for L3

L3TLB_VLD_13 - Valid Bit Vector 13 for L3		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04D34h	

This register contains the valid bits for entries 0-31 of L3TLB.

DWord	Bit	Description
0	31:0	**Valid Bit Vector 13 for L3**
		Default Value: 00000000h
		Access: RO
		Valid Bits per Entry.

Valid Bit Vector 13 for Z

ZTLB_VLD_13 - Valid Bit Vector 13 for Z	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	04B68h

This register contains the valid bits for entries 0-31 of ZTLB.

DWord	Bit	Description	
0	31:0	**Valid Bit Vector 13 for Z**	
		Default Value:	00000000h
		Access:	RO
		Valid Bits per Entry.	

Valid Bit Vector 14 for L3

L3TLB_VLD_14 - Valid Bit Vector 14 for L3		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04D38h	
This register contains the valid bits for entries 0-31 of L3TLB.		
DWord	**Bit**	**Description**
0	31:0	**Valid Bit Vector 14 for L3**
		Default Value: ... 00000000h
		Access: ... RO
		Valid Bits per Entry.

Valid Bit Vector 14 for Z

ZTLB_VLD_14 - Valid Bit Vector 14 for Z		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04B6Ch	
This register contains the valid bits for entries 0-31 of ZTLB.		

DWord	Bit	Description
0	31:0	**Valid Bit Vector 14 for Z**
		Default Value: 00000000h
		Access: RO
		Valid Bits per Entry.

Valid Bit Vector 15 for L3

L3TLB_VLD_15 - Valid Bit Vector 15 for L3		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04D3Ch	
This register contains the valid bits for entries 0-31 of L3TLB.		
DWord	**Bit**	**Description**
0	31:0	**Valid Bit Vector 15 for L3**
		Default Value: 00000000h
		Access: RO
		Valid Bits per Entry.

Valid Bit Vector 15 for Z

ZTLB_VLD_15 - Valid Bit Vector 15 for Z		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04B70h	
This register contains the valid bits for entries 0-31 of ZTLB.		
DWord	**Bit**	**Description**
0	31:0	**Valid Bit Vector 15 for Z**
		Default Value: 00000000h
		Access: RO
		Valid Bits per Entry.

Valid Bit Vector 16 for L3

L3TLB_VLD_16 - Valid Bit Vector 16 for L3	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	04D40h

This register contains the valid bits for entries 0-31 of L3TLB.

DWord	Bit	Description
0	31:0	**Valid Bit Vector 16 for L3**
		Default Value: 00000000h
		Access: RO
		Valid Bits per Entry.

Valid Bit Vector 17 for L3

L3TLB_VLD_17 - Valid Bit Vector 17 for L3		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04D44h	
This register contains the valid bits for entries 0-31 of L3TLB.		
DWord	**Bit**	**Description**
0	31:0	**Valid Bit Vector 17 for L3**
		Default Value: 00000000h
		Access: RO
		Valid Bits per Entry.

Valid Bit Vector 18 for L3

L3TLB_VLD_18 - Valid Bit Vector 18 for L3		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04D48h	
This register contains the valid bits for entries 0-31 of L3TLB.		

DWord	Bit	Description
0	31:0	**Valid Bit Vector 18 for L3**
		Default Value: 00000000h
		Access: RO
		Valid Bits per Entry.

Valid Bit Vector 19 for L3

L3TLB_VLD_19 - Valid Bit Vector 19 for L3		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04D4Ch	
This register contains the valid bits for entries 0-31 of L3TLB.		

DWord	Bit	Description
0	31:0	**Valid Bit Vector 19 for L3**

		Default Value:	00000000h
		Access:	RO
		Valid Bits per Entry.	

Valid Bit Vector 20 for L3

L3TLB_VLD_20 - Valid Bit Vector 20 for L3		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04D50h	
This register contains the valid bits for entries 0-31 of L3TLB.		

DWord	Bit	Description
0	31:0	**Valid Bit Vector 20 for L3**
		Default Value: 00000000h
		Access: RO
		Valid Bits per Entry.

Valid Bit Vector 21 for L3

L3TLB_VLD_21 - Valid Bit Vector 21 for L3		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04D54h	
This register contains the valid bits for entries 0-31 of L3TLB.		

DWord	**Bit**	**Description**	
0	31:0	**Valid Bit Vector 21 for L3**	
		Default Value:	00000000h
		Access:	RO
		Valid Bits per Entry.	

default

default

default

Valid Bit Vector 23 for L3

L3TLB_VLD_23 - Valid Bit Vector 23 for L3		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04D5Ch	
This register contains the valid bits for entries 0-31 of L3TLB.		

DWord	Bit	Description	
0	31:0	**Valid Bit Vector 23 for L3**	
		Default Value:	00000000h
		Access:	RO
		Valid Bits per Entry.	

Valid Bit Vector for VLF

VLFTLB_VLD - Valid Bit Vector for VLF		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04B30h	
This register contains the valid bits for entries 0-31 of VLFTLB.		

DWord	Bit	Description
0	31:0	**Valid Bit Vector for VLF**
		Default Value: 00000000h
		Access: RO
		Valid Bits per Entry.

Valid Bit Vector for VLFSL1

VLFSL1TLB_VLD - Valid Bit Vector for VLFSL1		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04B2Ch	
This register contains the valid bits for entries 0-31 of VLFSL1TLB.		
DWord	**Bit**	**Description**
0	31:0	**Valid Bit Vector for VLFSL1**
		Default Value: 00000000h
		Access: RO
		Valid Bits per Entry.

VC

<table>
<tr><th colspan="3">VC - VC</th></tr>
<tr><td>Register Space:</td><td colspan="2">PCI: 0/2/0</td></tr>
<tr><td>Project:</td><td colspan="2">CHV, BSW</td></tr>
<tr><td>Source:</td><td colspan="2">PRM</td></tr>
<tr><td>Default Value:</td><td colspan="2">0x00000000</td></tr>
<tr><td>Size (in bits):</td><td colspan="2">32</td></tr>
<tr><td>Address:</td><td colspan="2">000B4h</td></tr>
<tr><td colspan="3">Vendor Capabilities. Any SKU related fuses would be added here.</td></tr>
<tr><th>DWord</th><th>Bit</th><th>Description</th></tr>
<tr><td rowspan="2">0</td><td>31:1</td><td>

Reserved

Default Value:	0000000h
Access:	RO

Reserved

</td></tr>
<tr><td>0</td><td>

Spare_bit

Default Value:	0b
Access:	RO

Placeholder for SKU related fusing.

</td></tr>
</table>

VCES Idle Switch Delay

VECS_IDLEDLY - VCES Idle Switch Delay	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoEnhancementCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	1A23Ch

The IDLEDLY register contains an Idle Delay field which specifies the minimum number of microseconds allowed for command streamer to wait before a context is switched out leading to IDLE state in execlists mode, i.e following this context switch there is no active element available in HW to execute.
A default value of 0, means that by default, there is no restriction to wait on a context switch leading to IDLE. This register has no significance when execlists are not enabled.

DWord	Bit	Description	
0	31:21	**Reserved**	
		Project:	All
		Format:	MBZ
	20:0	**IDLE Delay**	
		Default Value:	0h
		Project:	All
		Format:	U21
		Minimum number of micro-seconds allowed.	

VCID

VCID - VCID		
Register Space:	PCI: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x01070009	
Size (in bits):	32	
Address:	000B0h	
Vendor Capability ID		

DWord	Bit	Description
0	31:24	**VERSION**
		Default Value: · 01h
		Access: · RO
		VS: Identifies this as the first revision of the CAPID register definition.
	23:16	**LENGTH**
		Default Value: · 07h
		Access: · RO
		LEN: This field has the value 07h to indicate structure length (8 bytes)
	15:8	**NEXT_CAPABILITY_POINTER**
		Default Value: · 00h
		Access: · R/W Once
		00 indicates capability list ends here. This register should be programmed by BIOS during boot-up. Once written, this register becomes Read_Only. This register can only be cleared by a Reset. Write-once allowing the capability list to be changed.
	7:0	**CAPABILITY_ID_CID**
		Default Value: · 09h
		Access: · RO
		Identifies this as a vendor dependent capability pointers.

VCS_PREEMPTION_HINT

VCS_PREEMPTION_HINT - VCS_PREEMPTION_HINT	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	124BCh
Valid Projects:	CHV, BSW

This register contains the Head pointer offset in to the Ring Buffer or the Dword aligned Graphics address in to the Batch Buffer corresponding to either MI_ARB_CHECK called Preemption Hint Address. When Preemption Hint Address is enabled, VCS will honor UHPTR only on parsing MI_ARB_CHK at Preemption Hint Address.

This register contains the Head pointer offset into the Ring Buffer or the Dword aligned Graphics address into the Batch Buffer corresponding to the below listed commands in execlist mode of operation

- MI_ARB_CHECK
- MI_WAIT_FOR_EVENT
- MI_SEMAPHORE_WAIT

Programming Notes
Programming Restriction: This register should NEVER be programmed in functional mode, this should be used only in validation mode to achieve deterministic behavior of UHPTR being sampled by a given MI_ARB_CHECK in command stream. Programmer has to ensure that VCS Preemption Hint register gets programmed before UHPTR is programmed and well before VCS crosses the corresponding execution point. Preemption hint for both RingBuffer and Batch Buffer can't be enabled simultaneously.

DWord	Bit	Description
0	31:2	**Preempted Hint Address**
		<table><tr><td>Format:</td><td>U30</td></tr><tr><td>Format:</td><td>GraphicsAddress[31:2]</td></tr></table>
		This field contains the Head offset in to the Ring Buffer when Preemption Hint is set to Ring Buffer and Dword aligned Graphics Address in to the batch buffer when Preemption Hint is set to Batch Buffer.
	1	**Batch Buffer Preemption Hint**
		<table><tr><td>Format:</td><td>Enable</td></tr></table>
		<table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>0h</td><td>Disabled</td><td>Preemption hint is disabled in batch buffer.</td></tr></table>

VCS_PREEMPTION_HINT - VCS_PREEMPTION_HINT

		1h	Enabled	Preemption hint is enabled in ring buffer and preemption hint address corresponds to the instruction in Batch Buffer.

	0	**Ring Preemption Hint**		
		Format:		Enable

Value	Name	Description
0h	Disable	Preemption hint is disabled in ring buffer.
1h	Enabled	Preemption hint is enabled in ring buffer and preemption hint address corresponds to the instruction in Ring Buffer.

VCS_PREEMPTION_HINT_UDW

VCS_PREEMPTION_HINT_UDW - VCS_PREEMPTION_HINT_UDW	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	124C8h
Valid Projects:	CHV, BSW

This register contains the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space of the Batch Buffer corresponding to MI_ARB_CHECK command called Preemption Hint Address.

Programming Notes
Programming Restriction:This register should NEVER be programmed in functional mode, this should be used only in validation mode to achieve deterministic behavior of UHPTR being sampled by a given MI_ARB_CHK in command stream.

DWord	Bit	Description
0	31:16	**Reserved**
		Format: MBZ
	15:0	**Preempted Hint Address Upper DWORD**
		Format: GraphicsAddress[47:32]
		This field contains the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space of the batch buffer when Preemption Hint is set to Batch Buffer. This field is not valid when Preemption Hint is set to Ring Buffer.

VCS Context ID Preemption Hint

VCS_CTXID_PREEMPTION_HINT - VCS Context ID Preemption Hint	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	124CCh
Valid Projects:	CHV, BSW

This register contains the Context ID of a context in execlist mode of operation. In execlist mode of operation VCS_PREEMPTION_HINT registers are looked at by Video Command Streamer on executing a context having Context ID that matches with the contents of this register. This register contents are valid and looked at only in execlist mode of operation.

Programming Notes
This register should NEVER be programmed in functional mode, this must be used only in validation mode to achieve deterministic preemption behavior in execlist mode of operation.

DWord	Bit	Description
0	31:0	**Context ID Preemption Hint**
		<table><tr><td>Format:</td><td>U32</td></tr></table> If 0 this field has no effect. If nonzero it indicates the only context ID that can be preempted when execlists are enabled. A preemption attempt when the context ID of the currently executing ring context does not match this field will be ignored.

VCS Context Sizes

<table>
<tr><th colspan="3">VCS_CXT_SIZE - VCS Context Sizes</th></tr>
<tr><td>Register Space:</td><td colspan="2">MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td colspan="2">CHV, BSW</td></tr>
<tr><td>Source:</td><td colspan="2">VideoCS</td></tr>
<tr><td>Default Value:</td><td colspan="2">0x000A1105 CHV, BSW</td></tr>
<tr><td>Access:</td><td colspan="2">Read/32 bit Write Only</td></tr>
<tr><td>Size (in bits):</td><td colspan="2">32</td></tr>
<tr><td>Address:</td><td colspan="2">121A8h</td></tr>
<tr><td>Valid Projects:</td><td colspan="2">CHV, BSW</td></tr>
</table>

DWord	Bit	Description
0	31:21	**Reserved**
		Format: MBZ
	20:16	**VCS Context Size**
		Format: U5
		Value / **Name** / **Project**
		Ah / **[Default]** / CHV, BSW
	15:13	**Reserved**
		Format: MBZ
	12:8	**VCR Context Size**
		Format: U5
		Value / **Name** / **Project**
		11h / **[Default]** / CHV, BSW
	7:5	**Reserved**
		Format: MBZ
	4:0	**Execlist Context Size**
		Format: U5
		Value / **Name** / **Project**
		5h / **[Default]** / CHV, BSW

VCS Context Timestamp Count

VCS_CTX_TIMESTAMP - VCS Context Timestamp Count	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	123A8h
Valid Projects:	CHV, BSW

This register provides a mechanism to obtain cumulative run time of a GPU context on HW. This register gets context save/restored on a context switch. SW must reset this register on very first submission of a context to HW, then afterwards gets context save/restored maintaining the cumulative run time of the corresponding context. This register (effectively) counts at a constant frequency by adjusting the increment amount according to the actual reference clock frequency. SW therefore does not need to know the reference clock frequency. This register gets reset on an engine reset.

This register is context save restore on a context switch.

DWord	Bit	Description
0	31:0	**Timestamp Value**
		Format: U32
		This register increments for every 80 ns of time.

VCS Counter for the bit stream decode engine

VCS_CNTR - VCS Counter for the bit stream decode engine		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	VideoCS	
Default Value:	0xFFFFFFFF	
Access:	R/W	
Size (in bits):	32	
Address:	12178h-1217Bh	
Valid Projects:	CHV, BSW	

DWord	Bit	Description
0	31:0	**Count Value**
		Default Value: ffffffffh
		Writing a Zero value to this register starts the counting.
		Writing a Value of FFFF FFFF to this counter stops the counter.

VCS Error Identity Register

VCS_EIR - VCS Error Identity Register	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoCS
Default Value:	0x00000000
Access:	R/WC
Size (in bits):	32
Address:	120B0h
Valid Projects:	CHV, BSW

The EIR register contains the persistent values of Hardware-Detected Error Condition bits. Any bit set in this register will cause the Master Error bit in the ISR to be set. The EIR register is also used by software to clear detected errors (by writing a 1 to the appropriate bit(s) except for the unrecoverable bits described).

DWord	Bit	Description
0	31:16	**Reserved**

Format:	MBZ

	15:0	**Error Identity Bits**

Format:	Array of Error condition bits ee the table titled Hardware-Detected Error Bits

This register contains the persistent values of ESR error status bits that are unmasked via the EMR register. The logical OR of all (defined) bits in this register is reported in the Master Error bit of the Interrupt Status Register. In order to clear an error condition, software must first clear the error by writing a 1 to the appropriate bit(s) in this field. If required, software should then proceed to clear the Master Error bit of the IIR.

Value	Name	Description
0h	**[Default]**	
1h	Error occurred	Error occurred

Programming Notes
Writing a 1 to a set bit will cause that error condition to be cleared. However, the Page Table Error bit (Bit 4) cannot be cleared except by reset (i.e., it is a fatal error).

VCS Error Mask Register

VCS_EMR - VCS Error Mask Register	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoCS
Default Value:	0xFFFFFFFF CHV, BSW
Access:	R/W
Size (in bits):	32
Address:	120B4h
Valid Projects:	CHV, BSW

The EMR register is used by software to control which Error Status Register bits are "masked" or "unmasked". "Unmasked" bits will be reported in the EIR, thus setting the Master Error ISR bit and possibly triggering a CPU interrupt, and will persist in the EIR until cleared by software. "Masked" bits will not be reported in the EIR and therefore cannot generate Master Error conditions or CPU interrupts.

Undefined or reserved bits in the Hardware Detected Error Bit Table will always return a read value of '1'

DWord	Bit	Description		
0	31:16	**Reserved**		
		Default Value:		FFFFh
		Project:		CHV, BSW
		Format:		Must Be One
	15:0	**Error Mask Bits**		
		Format:	Array of error condition mask bits See the table titled Hardware-Detected Error Bits.	
		This register contains a bit mask that selects which error condition bits (from the ESR) are reported in the EIR.		
		Value	Name	Description
		0000h	Not Masked	Will be reported in the EIR
		FFFFh	Masked **[Default]**	Will not be reported in the EIR

VCS Error Status Register

VCS_ESR - VCS Error Status Register		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	VideoCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Address:	120B8h	
Valid Projects:	CHV, BSW	

The ESR register contains the current values of all Hardware-Detected Error condition bits (these are all by definition persistent). The EMR register selects which of these error conditions are reported in the persistent EIR (i.e., set bits must be cleared by software) and thereby causing a Master Error interrupt condition to be reported in the ISR.

DWord	Bit	Description
0	31:16	**Reserved**
		Format: MBZ
	15:0	**Error Status Bits**
		Format: Array of error condition bits See the table titled Hardware-Detected Error Bits.
		This register contains the non-persistent values of all hardware-detected error condition bits.

Value	Name	Description
0h	**[Default]**	
1h	Error Condition Detected	Error Condition detected

VCS Execute Condition Code Register

VCS_EXCC - VCS Execute Condition Code Register	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoCS
Default Value:	0x00000000
Access:	R/W, RO
Size (in bits):	32
Trusted Type:	1
Address:	12028h
Valid Projects:	CHV, BSW

This register contains user defined and hardware generated conditions that are used by MI_WAIT_FOR_EVENT commands. An MI_WAIT_FOR_EVENT instruction excludes the executing ring from arbitration if the selected event evaluates to a 1, while instruction is discarded if the condition evaluates to a 0. Once excluded, a ring is enabled into arbitration when the selected condition evaluates to a 0.
This register also contains control for the invalidation of indirect state pointers on context restore.

DWord	Bit	Description
0	31:16	**Mask Bits**
		Format: Mask[15:0]
		These bits serve as a write enable for bits 15:0. If this register is written with any of these bits clear the corresponding bit in the field 15:0 will not be modified. Reading these bits always returns 0s.
	15:5	**Reserved**
		Format: MBZ
	4:0	**Reserved**
		Project: CHV, BSW
		Format: MBZ

VCS General Purpose Register

VCS_GPR - VCS General Purpose Register		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	VideoCS	
Default Value:	0x00000000, 0x00000000	
Access:	R/W	
Size (in bits):	64	
Address:	12600h-1267Fh	
Valid Projects:	CHV, BSW	
This is a general purpose register bank of sixteen 64-bit registers, used as temporary storage by the MI_MATH command to do ALU operations.		
Programming Notes		
Any operation that initiates a read to register 0x1266C will return the value of 0x1260c register. This does not include context save or MI_MATH command operation.		

DWord	**Bit**	**Description**	
0	63:0	**Reserved**	
		Format:	MBZ

VCS Hardware Status Mask Register

VCS_HWSTAM - VCS Hardware Status Mask Register	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoCS
Default Value:	0xFFFFFFFF
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	12098h
Valid Projects:	CHV, BSW

Access: RO for Reserved Control bits

The HWSTAM register has the same format as the Interrupt Control Registers. The bits in this register are "mask" bits that prevent the corresponding bits in the Interrupt Status Register from generating a "Hardware Status Write" (PCI write cycle). Any unmasked interrupt bit (HWSTAM bit set to 0) will allow the Interrupt Status Register to be written to the ISR location (within the memory page specified by the Hardware Status Page Address Register) when that Interrupt Status Register bit changes state.

Programming Notes

- To write the interrupt to the HWSP, the corresponding IMR bit must also be clear (enabled).
- At most 1 bit can be unmasked at any given time.

DWord	Bit	Description
0	31:0	**Hardware Status Mask Register**

		Default Value:	FFFFFFFFh
		Format:	Array of Masks

Refer to the table in the Interrupt Control Register section for bit definitions.

VCS IDLE Max Count

VCS_PWRCTX_MAXCNT - VCS IDLE Max Count	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoCS
Default Value:	0x00000040 CHV, BSW
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	12054h
Valid Projects:	CHV, BSW

This register contains the time in 0.64us to wait before telling power management hardware the render pipe is IDLE

DWord	Bit	Description
0	31:20	**Reserved**
		Format: ⟶ MBZ
	19:0	**MFX IDLE Wait Time**
		Format: ⟶ Max Count
		Specifies how long the command stream should wait before ensuring the pipe is IDLE and to let power management hardware know

Value	Name	Description
00040h	**[Default]**	0x00040 * 0.64us ~ 41us wait time

Programming Notes
• This is only useable if bit 0 of the PC_PSMI_CTRL is clear.
• The value in this field *must* be greater than 1.

VCS Idle Switch Delay

VCS_IDLEDLY - VCS Idle Switch Delay	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	1223Ch
Valid Projects:	CHV, BSW

The IDLEDLY register contains an Idle Delay field which specifies the minimum number of microseconds allowed for command streamer to wait before a context is switched out leading to IDLE state in Execlist mode, i.e following this context switch there is no active element available in HW to execute.
A default value of 0, means that by default, there is no restriction to wait on a context switch leading to IDLE. This register has no significance when Execlists are not enabled.

DWord	Bit	Description	
0	31:21	**Reserved**	
		Project:	All
		Format:	MBZ
	20:0	**IDLE Delay**	
		Project:	All
		Format:	U21
		Minimum number of micro-seconds allowed.	

VCS Instruction Parser Mode Register

VCS_INSTPM - VCS Instruction Parser Mode Register

Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32

Address:	120C0h-120C3h
Valid Projects:	CHV, BSW

The VCS_INSTPM register is used to control the operation of the VCS Instruction Parser. Certain classes of instructions can be disabled (ignored) - often useful for detecting performance bottlenecks. Also, "Synchronizing Flush" operations can be initiated - useful for ensuring the completion (vs. only parsing) of rendering instructions. DefaultValue=0000 0000h

Programming Notes
All reserved bits are implemented.

DWord	Bit	Description
0	31:16	**Masks** <table><tr><td>Format:</td><td>Mask[15:0]</td></tr></table> These bits serve as write enables for bits 15:0. If this register is written with any of these bits clear the corresponding bit in the field 15:0 will not be modified. Reading these bits always returns 0s.
	15:11	**Reserved** <table><tr><td>Project:</td><td>All</td></tr><tr><td>Format:</td><td>MBZ</td></tr></table>
	10	**Implied Atomic Fences To Write Fences** <table><tr><td>Project:</td><td>CHV, BSW</td></tr><tr><td>Format:</td><td>U1</td></tr></table> If set, all implied atomic fences generated by HW during various operations (Flushes, Context Switch) are converted to regular write fences. Setting this bit will affect data ordering functionality and must be only used in debug mode. When reset HW behaves as expected. <table><tr><td>Programming Notes</td></tr><tr><td>This bit is not context save and restored. SW must set this bit through the Work Around Batch buffer in to retain through standby and set this bit on each context submission.</td></tr></table>
	9	**Reserved** <table><tr><td>Project:</td><td>CHV, BSW</td></tr><tr><td>Format:</td><td>MBZ</td></tr></table>

VCS_INSTPM - VCS Instruction Parser Mode Register

	8:7	**Reserved**		
		Format:		MBZ
	6:5	**Reserved**		
		Project:	CHV, BSW	
		Format:	MBZ	
	4:0	**Reserved**		
		Access:		R/W
		Format:		MBZ

VCS Interrupt Mask Register

VCS_IMR - VCS Interrupt Mask Register	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoCS
Default Value:	0xFFFFFFFF
Access:	R/W
Size (in bits):	32
Address:	120A8h
Valid Projects:	CHV, BSW

The IMR register is used by software to control which Interrupt Status Register bits are masked or unmasked. Unmasked bits will be reported in the IIR, possibly triggering a CPU interrupt, and will persist in the IIR until cleared by software. Masked bits will not be reported in the IIR and therefore cannot generate CPU interrupts.

DWord	Bit	Description
0	31:0	**Interrupt Mask Bits**

Format:	Array of interrupt mask bits Refer to the Interrupt Control Register section for bit definitions.

This field contains a bit mask which selects which interrupt bits (from the ISR) are reported in the IIR.

Value	Name	Description
FFFF FFFFh	**[Default]**	
0h	Not Masked	Will be reported in the IIR
1h	Masked	Will not be reported in the IIR

VCS Mode Register for Software Interface

VCS_MI_MODE - VCS Mode Register for Software Interface	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoCS
Default Value:	0x00000200 CHV, BSW
Access:	R/W
Size (in bits):	32

Address:	1209Ch-1209Fh
Valid Projects:	CHV, BSW

The MI_MODE register contains information that controls software interface aspects of the command parser.

DWord	Bit	Description
0	31:16	**Masks** A 1 in a bit in this field allows the modification of the corresponding bit in Bits 15:0.
	15	**Suspend Flush** Mask: MMIO(0x209c)#31 Value / Name / Description: 0h — No Delay — HW will not delay flush, this bit will get cleared by MI_SUSPEND_FLUSH as well 1h — DelayFlush — Suspend flush is active
	14:12	**Reserved** Access: R/W
	11	**Invalidate UHPTR enable** If bit set H/W clears the valid bit of BCS_UHPTR (4134h, bit 0) when current active head pointer is equal to UHPTR.
	10	**Atomic Read Return for MI_COPY_MEM_MEM** Project: CHV, BSW Format: U1 Value / Name / Description: 0h — Disable **[Default]** — Hardware does a regular memory fence write to complete the write to the destination address before moving to the next instruction. 1h — Enable — Hardware does Atomic Move with Read Return to complete the write to the destination address before moving to the next instruction.

VCS_MI_MODE - VCS Mode Register for Software Interface

	9	**Ring Idle (Read Only Status bit)**

Access:	RO

Writes to this bit are not allowed.

Value	Name
0	Parser not idle
1	Parser idle **[Default]**

	8	**Stop Ring**

Software must set this bit to force the Ring and Command Parser to Idle. Software must read a "1" in Ring Idle bit after setting this bit to ensure that the hardware is idle.

Software must clear this bit for Ring to resume normal operation.

Value	Name
0	Normal Operation
1	Parser is turned off

	7:0	**Reserved**

Access:	R/W

VCS Reported Timestamp Count

VCS_TIMESTAMP - VCS Reported Timestamp Count	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoCS
Default Value:	0x00000000, 0x00000000
Access:	RO. This register is not set by the context restore.
Size (in bits):	64
Address:	12358h
Valid Projects:	CHV, BSW

This register provides an elapsed real-time value that can be used as a timestamp. This register is not reset by a graphics reset. It will maintain its value unless a full chipset reset is performed. Note: This timestamp register reflects the value of the PCU TSC. The PCU TSC counts 10ns increments; this timestamp reflects bits 38:3 of the TSC (i.e. 80ns granularity, rolling over every 1.5 hours).

DWord	Bit	Description
0	63:36	**Reserved** Format: MBZ
	35:0	**Timestamp Value** Format: U36 This register toggles every 80 ns. The upper 28 bits are zero.

VCS Reset Control Register

VCS_RESET_CTRL - VCS Reset Control Register		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	VideoCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	120D0h	
Valid Projects:	CHV, BSW	

This register is to be used to control soft reset.

DWord	Bit	Description
0	31:16	**Mask Bits** Format: Mask[15:0] Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)
	15:2	**Reserved** Format: MBZ
	1	**Ready for Reset** Format: U1 When set indicates video codec engine is ready for reset. This bit gets cleared on engine reset or when Soft Reset In progress is cleared.
	0	**Request Reset** Format: U1 When set indicates SW wishes to reset the video codec engine. On seeing this bit set Command Streamer will take appropriate action and set Ready For Reset status bit. This bit gets cleared on engine reset. This bit can also be cleared by writing "0" to this bit, this mode of clearing must be only used in debug and validation mode.

VCS Ring Buffer Next Context ID Register

VCS_RNCID - VCS Ring Buffer Next Context ID Register	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoCS
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Address:	12198h-1219Fh
Valid Projects:	CHV, BSW

This register contains the next ring context ID associated with the ring buffer.

Programming Notes
The current context (RCCID) register can be updated indirectly from this register on a context switch event. Note that this can only be triggered when arbitration is enabled or if the current context runs dry (head pointer becomes equal to tail pointer).

DWord	Bit	Description
0	63:0	**Context ID** See Context Descriptor for VCS.

VCS Semaphore Polling Interval on Wait

VCS_SEMA_WAIT_POLL - VCS Semaphore Polling Interval on Wait	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	1224Ch
Valid Projects:	CHV, BSW

The SEMA_WAIT_POLL register contains Poll Interval field which specifies the minimum number of microseconds allowed for command streamer to wait before re-fetching the data from the address mentioned in the MI_SEMAPHORE_WAIT command on WAIT Mode set to POLL until the condition is satisfied while the context is not switched out. When value of 0 is written the poll interval will be equal to the memory latency of the read completion.

DWord	Bit	Description	
0	31:21	**Reserved**	
		Format:	MBZ
	20:0	**Poll Interval** Minimum number of micro-seconds allowed	

VCS Threshold for the counter of bit stream decode engine

VCS_THRSH - VCS Threshold for the counter of bit stream decode engine	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoCS
Default Value:	0x00150000
Access:	R/W
Size (in bits):	32
Address:	1217Ch-1217Fh

DWord	Bit	Description
0	31:0	**Threshold Value**
		Default Value: 00150000h
		The value in this register reflects the number of clocks the bit stream decode engine is expected to run. If the value is exceeded the counter is reset and an interrupt may be enabled in the device.

VCW Clock Count

<table>
<tr><td colspan="2" align="center">**VCW_CLOCK_CNT - VCW Clock Count**</td></tr>
<tr><td>Register Space:</td><td>MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td>CHV, BSW</td></tr>
<tr><td>Source:</td><td>VideoEnhancementCS</td></tr>
<tr><td>Default Value:</td><td>0x00000000</td></tr>
<tr><td>Access:</td><td>RO</td></tr>
<tr><td>Size (in bits):</td><td>32</td></tr>
<tr><td>Trusted Type:</td><td>1</td></tr>
<tr><td>Address:</td><td>08820h</td></tr>
<tr><td>ShortName:</td><td>VCW0_CLOCK_CNT</td></tr>
<tr><td>Address:</td><td>08920h</td></tr>
<tr><td>ShortName:</td><td>VCW1_CLOCK_CNT</td></tr>
</table>

DWord	Bit	Description
0	31:24	**Reserved** Format: MBZ
	23:0	**Max clock count** Default Value: 0h Maximum number of clocks taken by VCW to process a column

VCW Internal Latency

VCW_INTERNAL_LAT - VCW Internal Latency	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoEnhancementCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	08824h
ShortName:	VCW0_INTERNAL_LAT
Address:	08924h
ShortName:	VCW1_INTERNAL_LAT

DWord	Bit	Description	
0	31:24	**Reserved**	
		Format:	MBZ
	23:0	**VCW internal data latency count**	
		Default Value:	0h

VCW Min Max Latency

VCW_MINMAX_LAT - VCW Min Max Latency		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	VideoEnhancementCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	08828h	
ShortName:	VCW0_MINMAX_LAT	
Address:	08928h	
ShortName:	VCW1_MINMAX_LAT	
DWord	**Bit**	**Description**
0	31:16	**Current request count**
		Default Value: 0h
	15:8	**Max latency**
		Default Value: 0h
		Maximum number of clocks taken for tag 200h
	7:0	**Min latency**
		Default Value: 0h
		Minimum number of clocks taken for tag 200h

VCW Total Latency

VCW_TOTAL_LAT - VCW Total Latency	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoEnhancementCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	0882Ch
ShortName:	VCW0_TOTAL_LAT
Address:	0892Ch
ShortName:	VCW1_TOTAL_LAT

DWord	Bit	Description	
0	31:0	**Total latency**	
		Default Value:	0h
		Accumumation of latency per frame for tag 200h	

VCW XY position

<table>
<tr><td colspan="4" align="center">**VCW_XY_POS - VCW XY position**</td></tr>
<tr><td>Register Space:</td><td colspan="3">MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td colspan="3">CHV, BSW</td></tr>
<tr><td>Source:</td><td colspan="3">VideoEnhancementCS</td></tr>
<tr><td>Default Value:</td><td colspan="3">0x00000000</td></tr>
<tr><td>Access:</td><td colspan="3">RO</td></tr>
<tr><td>Size (in bits):</td><td colspan="3">32</td></tr>
<tr><td>Trusted Type:</td><td colspan="3">1</td></tr>
<tr><td>Address:</td><td colspan="3">08830h</td></tr>
<tr><td>ShortName:</td><td colspan="3">VCW0_XY_POS</td></tr>
<tr><td>Address:</td><td colspan="3">08930h</td></tr>
<tr><td>ShortName:</td><td colspan="3">VCW1_XY_POS</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td colspan="2">**Description**</td></tr>
<tr><td rowspan="2">0</td><td>31:16</td><td colspan="2">**Current Y value**

Default Value: 0h

Current Y position of VCW walker</td></tr>
<tr><td>15:0</td><td colspan="2">**Current X value**

Default Value: 0h

Current X position of VCW walker</td></tr>
</table>

VEBOX TLB Control Register

<table>
<tr><td colspan="3" align="center">**VTCR - VEBOX TLB Control Register**</td></tr>
<tr><td colspan="3">Register Space: MMIO: 0/2/0</td></tr>
<tr><td colspan="3">Project: CHV, BSW</td></tr>
<tr><td colspan="3">Source: PRM</td></tr>
<tr><td colspan="3">Default Value: 0x00000000</td></tr>
<tr><td colspan="3">Size (in bits):   32</td></tr>
<tr><td colspan="3">Address: 04270h</td></tr>
</table>

DWord	Bit	Description
0	31:1	**Reserved**
		Default Value: 0000000000000000000000000000000b
		Access: RO
	0	**Invalidate TLBs on the corresponding Engine**
		Default Value: 0b
		Access: R/W
		SW writes 1 to invalidate the TLBs for the associated engine and HW clears the bit when invalidation is complete. To ensure proper invalidation of the TLBs, SW has to ensure the corresponding engine's HW pipeline is flushed and cleared from all its memory accesses. Otherwise HW cannot guarantee the proper invalidation for TLBs. This bit is self clear.

VEBX Context Element Descriptor (High Part)

VEBX_CTX_EDR_H - VEBX Context Element Descriptor (High Part)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	044C4h	

DWord	Bit	Description
0	31:0	**VEBX Context Element Descriptor (High Part)**
		Default Value: 00000000h
		Access: R/W

VEBX Context Element Descriptor (Low Part)

VEBX_CTX_EDR_L - VEBX Context Element Descriptor (Low Part)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000009	
Size (in bits):	32	
Address:	044C0h	

DWord	Bit	Description
0	31:0	**VEBX Context Element Descriptor (Low Part)**
		Default Value: · · · 00000009h
		Access: · · · R/W

VEBX Context Element Descriptor (Low Part)

VEBX_CTX_EDR_L - VEBX Context Element Descriptor (Low Part)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000009	
Size (in bits):	32	
Address:	044C0h	

DWord	Bit	Description	
0	31:0	**VEBX Context Element Descriptor**	
		Default Value:	00000009h
		Access:	R/W

VEBX Fault Counter

VEBX_FAULT_CNTR - VEBX Fault Counter	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	045C0h

DWord	Bit	Description	
0	31:0	**VEBX Fault Counter**	
		Default Value:	00000000h
		Access:	RO
		This counter only applies to advance context when fault and stream mode is selected.	

VEBX Fixed Counter

VEBX_FIXED_CNTR - VEBX Fixed Counter	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	045C4h

DWord	Bit	Description	
0	31:0	**VEBX Fixed Counter**	
		Default Value:	00000000h
		Access:	RO
		This counter only applies to advance context when fault and stream mode is selected.	

VEBX LRA 0

VEBX_LRA_0 - VEBX LRA 0		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x2F201F00	
Size (in bits):	32	
Address:	04A80h	

DWord	Bit	Description	
0	31:30	**Reserved**	
		Default Value:	00b
		Access:	RO
	29:24	**VEBX LRA1 Max**	
		Default Value:	101111b
		Access:	R/W
		Maximum value of programmable LRA1.	
	23:22	**Reserved**	
		Default Value:	00b
		Access:	RO
	21:16	**VEBX LRA1 Min**	
		Default Value:	100000b
		Access:	R/W
		Minimum value of programmable LRA1.	
	15:14	**Reserved**	
		Access:	RO
	13:8	**VEBX LRA0 Max**	
		Default Value:	011111b
		Access:	R/W
		Maximum value of programmable LRA0.	
	7:6	**Reserved**	
		Default Value:	00b
		Access:	RO
	5:0	**VEBXLRA0 Min**	
		Default Value:	000000b
		Access:	R/W
		Minimum value of programmable LRA0.	

VEBX LRA 1

VEBX_LRA_1 - VEBX LRA 1		

Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x06003F30
Size (in bits):	32
Address:	04A84h

DWord	Bit	Description		
0	31:30	**Reserved**		
		Default Value:		00b
		Access:		RO
	29:28	**VECS**		
		Default Value:		00b
		Access:		R/W
		Which LRA should VECS use.		
	27:26	**VFW**		
		Default Value:		01b
		Access:		R/W
		Which LRA should VFW use.		
	25:24	**VEO**		
		Default Value:		10b
		Access:		R/W
		Which LRA should VEO use.		
	23:14	**Reserved**		
		Default Value:	0000000000b	
		Access:	RO	
	13:8	**VEBXLRA2 Max**		
		Default Value:	111111b	
		Access:	R/W	
		Minimum value of programmable LRA2.		
	7:6	**Reserved**		
		Default Value:		00b
		Access:		RO

VEBX_LRA_1 - VEBX LRA 1

	5:0	**VEBXLRA2 Min**	
		Default Value:	110000b
		Access:	R/W
		Minimum value of programmable LRA2.	

VEBX PDP0/PML4/PASID Descriptor (High Part)

VEBX_CTX_PDP0_H - VEBX PDP0/PML4/PASID Descriptor (High Part)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	044CCh	

DWord	Bit	Description
0	31:0	**VEBX PDP0/PML4/PASID Descriptor (High Part)**
		Default Value: 00000000h
		Access: R/W

VEBX PDP0/PML4/PASID Descriptor (Low Part)

VEBX_CTX_PDP0_L - VEBX PDP0/PML4/PASID Descriptor (Low Part)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	044C8h	

DWord	Bit	Description
0	31:0	**VEBX PDP0/PML4/PASID Descriptor (Low Part)**
		Default Value: 00000000h
		Access: R/W

VEBX PDP1 Descriptor Register (High Part)

VEBX_CTX_PDP1_H - VEBX PDP1 Descriptor Register (High Part)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	044D4h	

DWord	Bit	Description
0	31:0	**VEBX PDP1 Descriptor Register (High Part)**
		Default Value: 00000000h
		Access: R/W

VEBX PDP1 Descriptor Register (Low Part)

VEBX_CTX_PDP1_L - VEBX PDP1 Descriptor Register (Low Part)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	044D0h	

DWord	Bit	Description
0	31:0	**VEBX PDP1 Descriptor Register (Low Part)**
		Default Value: 00000000h
		Access: R/W

VEBX PDP2 Descriptor Register (High Part)

VEBX_CTX_PDP2_H - VEBX PDP2 Descriptor Register (High Part)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	044DCh	

DWord	Bit	Description	
0	31:0	**VEBX PDP2 Descriptor Register (High Part)**	
		Default Value:	00000000h
		Access:	R/W

VEBX PDP2 Descriptor Register (Low Part)

VEBX_CTX_PDP2_L - VEBX PDP2 Descriptor Register (Low Part)			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	PRM		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	044D8h		

DWord	Bit	Description	
0	31:0	**VEBX PDP2 Descriptor Register (Low Part)**	
		Default Value:	00000000h
		Access:	R/W

VEBX PDP3 Descriptor Register (High Part)

VEBX_CTX_PDP3_H - VEBX PDP3 Descriptor Register (High Part)		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	044E4h	

DWord	Bit	Description		
0	31:0	**VEBX PDP3 Descriptor Register (High Part)**		
		Default Value:		00000000h
		Access:		R/W

VEBX PDP3 Descriptor Register (Low Part)

VEBX_CTX_PDP3_L - VEBX PDP3 Descriptor Register (Low Part)	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	044E0h

DWord	Bit	Description	
0	31:0	**VEBX PDP3 Descriptor Register (Low Part)**	
		Default Value:	00000000h
		Access:	R/W

VECS_PREEMPTION_HINT

VECS_PREEMPTION_HINT - VECS_PREEMPTION_HINT		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	VideoEnhancementCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	1A4BCh	

This register contains the Head pointer offset in to the Ring Buffer or the Dword aligned Graphics address in to the Batch Buffer corresponding to either MI_ARB_CHECK called Preemption Hint Address. When Preemption Hint Address is enabled, VECS will honor UHPTR only on parsing MI_ARB_CHK at Preemption Hint Address.

This register contains the Head pointer offset into the Ring Buffer or the Dword aligned Graphics address into the Batch Buffer corresponding to the below listed commands in execlist mode of operation

- MI_ARB_CHECK
- MI_WAIT_FOR_EVENT
- MI_SEMAPHORE_WAIT

Programming Notes
Programming Restriction:This register should NEVER be programmed in functional mode, this should be used only in validation mode to achieve deterministic behavior of UHPTR being sampled by a given MI_ARB_CHECK in command stream. Programmer has to ensure that VECS Preemption Hint register gets programmed before UHPTR is programmed and well before VECS crosses the corresponding execution point. Preemption hint for both RingBuffer and Batch Buffer can't be enabled simultaneously.

DWord	Bit	Description
0	31:2	**Preempted Hint Address**
		Format: U30
		Format: GraphicsAddress[31:2]
		This field contains the Head offset in to the Ring Buffer when Preemption Hint is set to Ring Buffer and Dword aligned Graphics Address in to the batch buffer when Preemption Hint is set to Batch Buffer.
	1	**Batch Buffer Preemption Hint**
		Format: Enable

Value	Name	Description
0h	Disabled	Preemption hint is disabled in batch buffer.
1h	Enabled	Preemption hint is enabled in ring buffer and preemption hint address corresponds to the instruction in Batch Buffer.

VECS_PREEMPTION_HINT - VECS_PREEMPTION_HINT		
0	**Ring Preemption Hint**	

Format:	Enable

Value	Name	Description
0h	Disable	Preemption hint is disabled in ring buffer.
1h	Enabled	Preemption hint is enabled in ring buffer and preemption hint address corresponds to the instruction in Ring Buffer.

VECS Context ID Preemption Hint

<table>
<tr><th colspan="2">VECS_CTXID_PREEMPTION_HINT - VECS Context ID Preemption Hint</th></tr>
<tr><td>Register Space:</td><td>MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td>CHV, BSW</td></tr>
<tr><td>Source:</td><td>VideoEnhancementCS</td></tr>
<tr><td>Default Value:</td><td>0x00000000</td></tr>
<tr><td>Access:</td><td>R/W</td></tr>
<tr><td>Size (in bits):</td><td>32</td></tr>
<tr><td>Address:</td><td>1A4CCh</td></tr>
</table>

This register contains the Context ID of a context in Execlist mode of operation. In execlist mode of operation VECS_PREEMPTION_HINT registers are looked at by Video Enhancement Command Streamer on executing a context having Context ID that matches with the contents of this register. This register contents are valid and looked at only in Execlist mode of operation.

Programming Notes
This register should NEVER be programmed in functional mode, this must be used only in validation mode to achieve deterministic preemption behavior in execlist mode of operation.

DWord	Bit	Description
0	31:0	**Context ID Preemption Hint**
		Format: U32
		If 0 this field has no effect. If nonzero it indicates the only context ID that can be preempted when execlists are enabled. A preemption attempt when the context ID of the currently executing ring context does not match this field will be ignored.

VECS Context Timestamp Count

VECS_CTX_TIMESTAMP - VECS Context Timestamp Count	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoEnhancementCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	1A3A8h

This register provides a mechanism to obtain cumulative run time of a GPU context on HW. This register gets context save/restored on a context switch. SW must reset this register on very first submission of a context to HW, then afterwards gets context save/restored maintaining the cumulative run time of the corresponding context. Note that the value of this register can be obtained in a 3D pipeline-synchronous fashion without a pipeline flush by using the PIPE_CONTROL command. See 3D Geometry Pipeline in the "3D and Media" volume. This register (effectively) counts at a constant frequency by adjusting the increment amount according to the actual reference clock frequency. SW therefore does not need to know the reference clock frequency. This register gets reset on an engine reset.

This register is context save restore on a context switch.

DWord	Bit	Description
0	31:0	**Timestamp Value**
		Format: U32
		This register increments for every 80 ns of time.

VECS Counter for the Video Enhancement Engine

VECS_CNTR - VECS Counter for the Video Enhancement Engine	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoEnhancementCS
Default Value:	0xFFFFFFFF
Access:	R/W
Size (in bits):	32
Address:	1A178h

DWord	Bit	Description
0	31:0	**Count Value**

Default Value:	ffffffffh

Writing a Zero value to this register starts the counting. Writing a Value of FFFF FFFF to this counter stops the counter.

VECS Error Identity Register

<table>
<tr><td colspan="4" align="center">**VECS_EIR - VECS Error Identity Register**</td></tr>
<tr><td colspan="4">Register Space: MMIO: 0/2/0</td></tr>
<tr><td colspan="4">Project: CHV, BSW</td></tr>
<tr><td colspan="4">Source: VideoEnhancementCS</td></tr>
<tr><td colspan="4">Default Value: 0x00000000</td></tr>
<tr><td colspan="4">Access: R/WC</td></tr>
<tr><td colspan="4">Size (in bits):   32</td></tr>
<tr><td colspan="4">Address: 1A0B0h</td></tr>
<tr><td colspan="4">The EIR register contains the persistent values of Hardware-Detected Error Condition bits. Any bit set in this register will cause the Master Error bit in the ISR to be set. The EIR register is also used by software to clear detected errors (by writing a '1' to the appropriate bit(s) except for the unrecoverable bits described).</td></tr>
</table>

DWord	Bit	Description
0	31:16	**Reserved** Project: All Format: MBZ
	15:0	**Error Identity Bits** Project: All Format: Array of Error condition bits See Table 1 5. Hardware-Detected Error Bits This register contains the persistent values of ESR error status bits that are unmasked via the EMR register. (See **Error! Reference source not found**.). The logical OR of all (defined) bits in this register is reported in the Master Error bit of the Interrupt Status Register. In order to clear an error condition, software must first clear the error by writing a '1' to the appropriate bit(s) in this field. If required, software should then proceed to clear the Master Error bit of the IIR.

Value	Name	Description	Project
0h	**[Default]**		
1h	Error occurred	Error occurred	All

Programming Notes
Writing a '1' to a set bit will cause that error condition to be cleared. However, the Page Table Error bit (Bit 4) can not be cleared except by reset (i.e., it is a fatal error).

VECS Error Mask Register

VECS_EMR - VECS Error Mask Register	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoEnhancementCS
Default Value:	0xFFFFFFFF CHV, BSW
Access:	R/W
Size (in bits):	32
Address:	1A0B4h

The EMR register is used by software to control which Error Status Register bits are "masked" or "unmasked". "Unmasked" bits will be reported in the EIR, thus setting the Master Error ISR bit and possibly triggering a CPU interrupt, and will persist in the EIR until cleared by software. "Masked" bits will not be reported in the EIR and therefore cannot generate Master Error conditions or CPU interrupts.

Undefined or reserved bits in the Hardware Detected Error Bit Table will always return a read value of '1'

DWord	Bit	Description
0	31:16	**Reserved**
		Default Value: FFFFh
		Project: CHV, BSW
		Format: Must Be One
	15:0	**Error Mask Bits**
		Project: All
		Format: Array of error condition mask bits See Table 1 5. Hardware-Detected Error Bits
		This register contains a bit mask that selects which error condition bits (from the ESR) are reported in the EIR.

Value	Name	Description
0000h	Not Masked	Will be reported in the EIR
FFFFh	Masked **[Default]**	Will not be reported in the EIR

VECS Error Status Register

VECS_ESR - VECS Error Status Register	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoEnhancementCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	1A0B8h

 The ESR register contains the current values of all Hardware-Detected Error condition bits (these are all by definition "persistent"). The EMR register selects which of these error conditions are reported in the persistent EIR (i.e., set bits must be cleared by software) and thereby causing a Master Error interrupt condition to be reported in the ISR.

DWord	Bit	Description
0	31:16	**Reserved**
		Project: All
		Format: MBZ
	15:0	**Error Status Bits**
		Project: All
		Format: Array of error condition bits See Table 1 5. Hardware-Detected Error Bits
		This register contains the non-persistent values of all hardware-detected error condition bits.

Value	Name	Description	Project
0h	**[Default]**		
1h	Error Condition Detected	Error Condition detected	All

VECS General Purpose Register

VECS_GPR - VECS General Purpose Register		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	VideoEnhancementCS	
Default Value:	0x00000000, 0x00000000	
Access:	R/W	
Size (in bits):	64	
Address:	1A600h-1A67Fh	

This is a general purpose register bank of sixteen 64-bit registers, used as temporary storage by the MI_MATH command to do ALU operations.

Programming Notes	Project
Any operation that initiates a read to register 0x1A66C will return the value of 0x1A60c register. This does not include context save or MI_MATH command operation.	CHV, BSW

DWord	Bit	Description	
0	63:0	**Reserved**	
		Format:	MBZ

VECS Hardware Status Mask Register

VECS_HWSTAM - VECS Hardware Status Mask Register	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoEnhancementCS
Default Value:	0xFFFFFFFF
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	1A098h

Access: RO for Reserved Control bits

The HWSTAM register has the same format as the Interrupt Control Registers. The bits in this register are "mask" bits that prevent the corresponding bits in the Interrupt Status Register from generating a "Hardware Status Write" (PCI write cycle). Any unmasked interrupt bit (HWSTAM bit set to 0) will allow the Interrupt Status Register to be written to the ISR location (within the memory page specified by the Hardware Status Page Address Register) when that Interrupt Status Register bit changes state.

Programming Notes
• To write the interrupt to the HWSP, the corresponding IMR bit must also be clear (enabled).
• At most 1 bit can be unmasked at any given time.

DWord	Bit	Description
0	31:0	**Hardware Status Mask Register**

Default Value:	FFFFFFFFh
Project:	All
Format:	Array of Masks

refer to Table 4-4 in Interrupt Control Register section for bit definitions

VECS IDLE Max Count

VECS_PWRCTX_MAXCNT - VECS IDLE Max Count		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	VideoEnhancementCS	
Default Value:	0x00000040	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	1A054h	
This register contains the time in 0.64us to wait before telling power management hardware the render pipe is IDLE		

DWord	Bit	Description
0	31:20	**Reserved**
		Project: All
		Format: MBZ
	19:0	**MFX IDLE Wait Time**
		Project: All
		Format: Max Count
		Specifies how long the command stream should wait before ensuring the pipe is IDLE and to let power management hardware know

Value	Name	Description
00040h	**[Default]**	0x00040 * 0.64us ~ 41us wait time

Programming Notes
This is only useable if bit 0 of the PC_PSMI_CTRL is clear

VECS Instruction Parser Mode Register

VECS_INSTPM - VECS Instruction Parser Mode Register	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoEnhancementCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	1A0C0h-1A0C3h

The VECS_INSTPM register is used to control the operation of the VECS Instruction Parser. Certain classes of instructions can be disabled (ignored) - often useful for detecting performance bottlenecks. Also, "Synchronizing Flush" operations can be initiated - useful for ensuring the completion (vs. only parsing) of rendering instructions.

Programming Notes
All reserved bits are implemented

DWord	Bit	Description
0	31:16	**Masks**

Format:	Mask[15:0]

These bits serve as write enables for bits 15:0. If this register is written with any of these bits clear the corresponding bit in the field 15:0 will not be modified. Reading these bits always returns 0s.

	15:11	**Reserved**

Project:	All
Format:	MBZ

	10	**Implied Atomic Fences To Write Fences**

Project:	CHV, BSW
Format:	U1

If set, all implied atomic fences generated by HW during various operations (Flushes, Context Switch) are converted to regular write fences. Setting this bit will affect data ordering functionality and must be only used in debug mode. When reset HW behaves as expected.

Programming Notes	Project
This bit is not context save and restored. SW must set this bit through the Work Around Batch buffer in to retain through standby and set this bit on each context submission.	CHV, BSW

	9	**Reserved**

Project:	CHV, BSW
Format:	MBZ

VECS_INSTPM - VECS Instruction Parser Mode Register

8:7	**Reserved**	
	Format:	MBZ
6:5	**Reserved**	
	Project:	CHV, BSW
	Format:	MBZ
4:0	**Reserved**	

VECS Interrupt Mask Register

VECS_IMR - VECS Interrupt Mask Register	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoEnhancementCS
Default Value:	0xFFFFFFFF
Access:	R/W
Size (in bits):	32
Address:	1A0A8h

The IMR register is used by software to control which Interrupt Status Register bits are "masked" or "unmasked". "Unmasked" bits will be reported in the IIR, possibly triggering a CPU interrupt, and will persist in the IIR until cleared by software. "Masked" bits will not be reported in the IIR and therefore cannot generate CPU interrupts.

DWord	Bit	Description			
0	31:0	**Interrupt Mask Bits**			
		Project:	All		
		Format:	Array of interrupt mask bits Refer to Table 4-4 in Interrupt Control Register section for bit definitions		
		This field contains a bit mask which selects which interrupt bits (from the ISR) are reported in the IIR.			
		Value	**Name**	**Description**	**Project**
		FFFF FFFFh	**[Default]**		
		0h	Not Masked	Will be reported in the IIR	All
		1h	Masked	Will not be reported in the IIR	All

VECS Mode Register for Software Interface

VECS_MI_MODE - VECS Mode Register for Software Interface	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoEnhancementCS
Default Value:	0x00000200 CHV, BSW
Access:	R/W
Size (in bits):	32

Address:	1A09Ch-1A09Fh

The MI_MODE register contains information that controls software interface aspects of the command parser

DWord	Bit	Description
0	31:16	**Masks** A "1" in a bit in this field allows the modification of the corresponding bit in Bits 15:0
	15	**Suspend Flush** 	Project:	All	 	Mask:	MMIO(0x209c)#31	 	Value	Name	Description	 	0h	No Delay	HW will not delay flush, this bit will get cleared by MI_SUSPEND_FLUSH as well	 	1h	Delay Flush	Suspend flush is active	
	14:12	**Reserved** 	Format:	MBZ	
	11	**Invalidate UHPTR Enable** If bit set H/W clears the valid bit of BCS_UHPTR (4134h, bit 0) when current active head pointer is equal to UHPTR.
	10	**Atomic Read Return for MI_COPY_MEM_MEM** 	Project:	CHV, BSW	 	Format:	U1	 	Value	Name	Description	 	0h	Disable **[Default]**	Hardware does a regular memory fence write to complete the write to the destination address before moving to the next instruction.	 	1h	Enable	Hardware does Atomic Move with Read Return to complete the write to the destination address before moving to the next instruction.	

VECS_MI_MODE - VECS Mode Register for Software Interface

	9	**Ring Idle (Read Only Status bit)** *Writes to this bit are not allowed.*

Value	Name
0	Parser not idle
1	Parser idle **[Default]**

	8	**Stop Ring** 0 = Normal Operation. 1 = Parser is turned off. Software must set this bit to force the Ring and Command Parser to Idle. Software must read a "1" in Ring Idle bit after setting this bit to ensure that the hardware is idle. *Software must clear this bit for Ring to resume normal operation.*
	7:0	**Reserved**

Format:	MBZ

VECS PREEMPTION HINT UDW

VECS_PREEMPTION_HINT_UDW - VECS PREEMPTION HINT UDW	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoEnhancementCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	1A4C8h

This register contains the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space of the Batch Buffer corresponding to MI_ARB_CHECK command called Preemption Hint Address.

Programming Notes
Programming Restriction:This register should NEVER be programmed in functional mode, this should be used only in validation mode to achieve deterministic behavior of UHPTR being sampled by a given MI_ARB_CHK in command stream.

DWord	Bit	Description
0	31:16	**Reserved**
		Format: MBZ
	15:0	**Preempted Hint Address Upper DWORD**
		Format: GraphicsAddress[47:32]
		This field contains the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space of the batch buffer when Preemption Hint is set to Batch Buffer. This field is not valid when Preemption Hint is set to Ring Buffer.

VECS Reported Timestamp Count

VECS_TIMESTAMP - VECS Reported Timestamp Count	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoEnhancementCS
Default Value:	0x00000000, 0x00000000
Access:	RO. This register is not set by the context restore.
Size (in bits):	64
Address:	1A358h

This register provides an elapsed real-time value that can be used as a timestamp. This register is *not* reset by a graphics reset. It will maintain its value unless a full chipset reset is performed. Note: This timestamp register reflects the value of the PCU TSC. The PCU TSC counts 10ns increments; this timestamp reflects bits 38:3 of the TSC (i.e. 80ns granularity, rolling over every 1.5 hours).

DWord	Bit	Description	
0	63:36	**Reserved**	
		Project:	All
		Format:	MBZ
	35:0	**TimeStampValue**	
		Project:	All
		Format:	U36
		This register toggles every 80 ns. The upper 28 bits are zero.	

VECS Reset Control Register

<table>
<tr><td colspan="3" align="center">**VECS_RESET_CTRL - VECS Reset Control Register**</td></tr>
<tr><td>Register Space:</td><td colspan="2">MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td colspan="2">CHV, BSW</td></tr>
<tr><td>Source:</td><td colspan="2">VideoEnhancementCS</td></tr>
<tr><td>Default Value:</td><td colspan="2">0x00000000</td></tr>
<tr><td>Access:</td><td colspan="2">R/W</td></tr>
<tr><td>Size (in bits):</td><td colspan="2">32</td></tr>
<tr><td>Address:</td><td colspan="2">1A0D0h</td></tr>
<tr><td colspan="3">This register is to be used to control soft reset.</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td>**Description**</td></tr>
<tr><td>0</td><td>31:16</td><td>**Mask Bits**

Format: Mask[15:0]

Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)</td></tr>
<tr><td></td><td>15:2</td><td>**Reserved**

Format: MBZ</td></tr>
<tr><td></td><td>1</td><td>**Ready for Reset**

Format: U1

When set indicates video enhancement engine is ready for reset. This bit gets cleared on engine reset or when Soft Reset In progress is cleared.</td></tr>
<tr><td></td><td>0</td><td>**Request Reset**

Format: U1

When set indicates SW wishes to reset the video enhancement engine. On seeing this bit set Command Streamer will take appropriate action and set Ready For Reset status bit. This bit gets cleared on engine reset. This bit can also be cleared by writing "0" to this bit, this mode of clearing must be only used in debug and validation mode.</td></tr>
</table>

VECS Semaphore Polling Interval on Wait

VECS_SEMA_WAIT_POLL - VECS Semaphore Polling Interval on Wait	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoEnhancementCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	1A24Ch

The SEMA_WAIT_POLL register contains Poll Interval field which specifies the minimum number of microseconds allowed for command streamer to wait before re-fetching the data from the address mentioned in the MI_SEMAPHORE_WAIT command on WAIT Mode set to POLL until the condition is satisfied while the context is not switched out. When value of 0 is written the poll interval will be equal to the memory latency of the read completion.

DWord	Bit	Description	
0	31:21	**Reserved**	
		Format:	MBZ
	20:0	**Poll Interval** Minimum number of micro-seconds allowed	

VECS Sleep State and PSMI Control

VECS_PSMI_CTRL - VECS Sleep State and PSMI Control	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoEnhancementCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	1A050h

This register is to be used to control all aspects of PSMI and power saving functions.

DWord	Bit	Description
0	31:16	**Mask Bits**
		<table><tr><td>Format:</td><td>Mask[15:0]</td></tr></table>
		Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)
	15:13	**Reserved**
		<table><tr><td>Project:</td><td>All</td></tr><tr><td>Format:</td><td>MBZ</td></tr></table>
	12	**Reserved**
		<table><tr><td>Project:</td><td>CHV, BSW</td></tr><tr><td>Format:</td><td>MBZ</td></tr></table>
	11:5	**Reserved**
		<table><tr><td>Format:</td><td>MBZ</td></tr></table>
	4	**GO Indicator**
		<table><tr><td>Project:</td><td>All</td></tr><tr><td>Access:</td><td>RO</td></tr><tr><td>Format:</td><td>GO</td></tr></table>
		This is a read only field. Writing to this bit is undefined. To simplify power saving and soft reset flows, the power management hardware has the ability to block all pending memory cycles of the render pipe. When GO=0, all cycles are blocked. All CPD enter/exit and RC6 enter/exit has this bit set to 0.
		<table><tr><th>Value</th><th>Name</th><th>Description</th><th>Project</th></tr><tr><td>0h</td><td>Disable **[Default]**</td><td>All pending memory read cycles are complete. No new cycles permitted except for power context or PSMI cycles</td><td>All</td></tr><tr><td>1h</td><td>Enable</td><td>Normal execution</td><td>All</td></tr></table>

　　　　　　　　　　　　　　　　Doc Ref # IHD-OS-CHV-BSW-Vol 2c-06.15

VECS_PSMI_CTRL - VECS Sleep State and PSMI Control

	3	**IDLE Indicator**	
		Default Value:	0h Render is assumed NOT IDLE coming out of reset
		Project:	All
		Access:	RO
		Format:	IDLE
		This is a read only field. Writing to this bit is undefined. This indicates what power management thinks what state the render pipe is in. That is, if set, the full handshake between render and power management has occured and most likely the render clocks are currently turned off.	
	2	**IDLE Flush Disable**	
		Default Value:	0h Flush Enabled
		Project:	All
		Format:	Disable
		For normal execution, before telling the power management hardware that the render pipe is IDLE, inserts a pipelined flush after the top of the pipe (command stream) is IDLE for MAXCNT (0x2054). Setting this bit disables the flush. After MAXCNT is reached, the command streamer will immediately send the IDLE indicator to power management.	
	1	**Reserved**	
		Project:	All
		Format:	MBZ
	0	**Reserved**	
		Project:	All

VECS Threshold for the Counter of Video Enhancement Engine

VECS_CTR_THRSH - VECS Threshold for the Counter of Video Enhancement Engine		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	VideoEnhancementCS	
Default Value:	0x00150000	
Access:	R/W	
Size (in bits):	32	
Address:	1A17Ch	

DWord	Bit	Description
0	31:0	**Threshold Value**
		Default Value: 00150000h
		The value in this register reflects the number of clocks the bit stream decode engine is expected to run. If the value is exceeded the counter is reset and an interrupt may be enabled in the device.

VEO Current Pipe 0 XY Register

VEO_CURRENT0_XY - VEO Current Pipe 0 XY Register	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoEnhancementCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	08854h
Address:	08954h

DWord	Bit	Description	
0	31:30	**Reserved**	
	29:16	**Current Input Pipe 0 X**	
		Default Value:	0h
	15	**Reserved**	
	14:0	**Current Input Pipe 0 Y**	
		Default Value:	0h

VEO DN Pipe 0 XY Register

VEO_DN0_XY - VEO DN Pipe 0 XY Register		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	VideoEnhancementCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	0884Ch	
Address:	0894Ch	

DWord	Bit	Description
0	31:30	**Reserved**
	29:16	**DN Pipe 0 X**
		Default Value: 0h
		dn_input_x[13:0]
	15	**Reserved**
	14:0	**DN Pipe 0 Y**
		Default Value: 0h
		dn_input_y[14:0]

VEO DN Pipe 1 XY Register

VEO_DN1_XY - VEO DN Pipe 1 XY Register		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	VideoEnhancementCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	08850h	
Address:	08950h	

DWord	Bit	Description
0	31:30	**Reserved**
	29:16	**DN Pipe 1 X**
		Default Value: 0h
	15	**Reserved**
	14:0	**DN Pipe 1 Y**
		Default Value: 0h

VEO DV Count Register

VEO_DV_COUNT - VEO DV Count Register		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	VideoEnhancementCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	08844h	
Address:	08944h	

DWord	Bit	Description
0	31:24	**Pipe1 Motion History DV/Hold Maxcount**
		Default Value: 0h
	23:16	**Pipe1 Pixel History DV/Hold Maxcount**
		Default Value: 0h
	15:8	**Pipe0 Motion History DV/Hold Maxcount**
		Default Value: 0h
	7:0	**Pipe0 Pixel History DV/Hold Maxcount**
		Default Value: 0h

VEO DV Hold Register

<table>
<tr><td colspan="3" align="center">**VEO_DVHOLD - VEO DV Hold Register**</td></tr>
<tr><td>Register Space:</td><td colspan="2">MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td colspan="2">CHV, BSW</td></tr>
<tr><td>Source:</td><td colspan="2">VideoEnhancementCS</td></tr>
<tr><td>Default Value:</td><td colspan="2">0x00000000</td></tr>
<tr><td>Access:</td><td colspan="2">RO</td></tr>
<tr><td>Size (in bits):</td><td colspan="2">32</td></tr>
<tr><td>Trusted Type:</td><td colspan="2">1</td></tr>
<tr><td>Address:</td><td colspan="2">0885Ch</td></tr>
<tr><td>Address:</td><td colspan="2">0895Ch</td></tr>
<tr><td colspan="3">Datavalid/Hold signals for VEO interface</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td>**Description**</td></tr>
<tr><td rowspan="11">0</td><td>31</td><td>**vdn_p0_veo_pixel_dv**
Default Value: 0h</td></tr>
<tr><td>30</td><td>**veo_vdn_p0_pixel_hold**
Default Value: 0h</td></tr>
<tr><td>29</td><td>**vdn_p0_veo_mh_dv**
Default Value: 0h</td></tr>
<tr><td>28</td><td>**veo_vdn_p0_mh_hold**
Default Value: 0h</td></tr>
<tr><td>27</td><td>**vdn_p0_veo_bne_luma_dv**
Default Value: 0h</td></tr>
<tr><td>26</td><td>**veo_vdn_p0_bne_luma_hold**
Default Value: 0h</td></tr>
<tr><td>25</td><td>**vdn_p0_veo_bne_chroma_dv**
Default Value: 0h</td></tr>
<tr><td>24</td><td>**veo_vdn_p0_bne_chroma_hold**
Default Value: 0h</td></tr>
<tr><td>23</td><td>**vdi_p0_veo_pixel_dv**
Default Value: 0h</td></tr>
<tr><td>22</td><td>**veo_vdi_p0_pixel_hold**
Default Value: 0h</td></tr>
<tr><td>21</td><td>**vdi_p0_veo_stmm_dv**
Default Value: 0h</td></tr>
</table>

VEO_DVHOLD - VEO DV Hold Register

	20	**veo_vdi_p0_stmm_hold**	
		Default Value:	0h
	19	**vdi_p0_veo_fmd_dv**	
		Default Value:	0h
	18	**veo_vdi_p0_fmd_hold**	
		Default Value:	0h
	17	**Reserved**	
		Default Value:	0h
	16	**Reserved**	
		Default Value:	0h
	15	**vdn_p1_veo_pixel_dv**	
		Default Value:	0h
	14	**veo_vdn_p1_pixel_hold**	
		Default Value:	0h
	13	**vdn_p1_veo_mh_dv**	
		Default Value:	0h
	12	**veo_vdn_p1_mh_hold**	
		Default Value:	0h
	11	**vdn_p1_veo_bne_luma_dv**	
		Default Value:	0h
	10	**veo_vdn_p1_bne_luma_hold**	
		Default Value:	0h
	9	**vdn_p1_veo_bne_chroma_dv**	
		Default Value:	0h
	8	**veo_vdn_p1_bne_chroma_hold**	
		Default Value:	0h
	7	**vdi_p1_veo_pixel_dv**	
		Default Value:	0h
	6	**veo_vdi_p1_pixel_hold**	
		Default Value:	0h
	5	**vdi_p1_veo_stmm_dv**	
		Default Value:	0h
	4	**veo_vdi_p1_stmm_hold**	
		Default Value:	0h
	3	**vdi_p1_veo_fmd_dv**	

VEO_DVHOLD - VEO DV Hold Register			
		Default Value:	0h
	2	**veo_vdi_p1_fmd_hold**	
		Default Value:	0h
	1	**Reserved**	
		Default Value:	0h
	0	**Reserved**	
		Default Value:	0h

VEO Previous Pipe 0 XY Register

VEO_PREVIOUS0_XY - VEO Previous Pipe 0 XY Register			
Register Space:	MMIO: 0/2/0		
Project:	CHV, BSW		
Source:	VideoEnhancementCS		
Default Value:	0x00000000		
Access:	RO		
Size (in bits):	32		
Trusted Type:	1		
Address:	08858h		
Address:	08958h		
DWord	**Bit**	**Description**	
0	31:30	**Reserved**	
	29:16	**Previous Input Pipe 0 X**	
		Default Value:	0h
	15	**Reserved**	
	14:0	**Previous Input Pipe 0 Y**	
		Default Value:	0h

VF Scratch Pad

VFSKPD - VF Scratch Pad		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	02470h	
Address:	083A8h-083ABh	
Valid Projects:	CHV, BSW	

DWord	Bit	Description
0	31:16	**Mask Bits** <table><tr><td>Format:</td><td>Mask[15:0]</td></tr></table> Must be set to modify corresponding bit in Bits 15:0. (All bits implemented)
	15	**Reserved**
	14:12	**Reserved**
	11	**Reserved**
	10	**Reserved**
	9	**Reserved**
	8	**End Offset Guardband Disable** <table><tr><td>Project:</td><td>CHV, BSW</td></tr><tr><td>Format:</td><td>U1</td></tr></table> <table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>0h</td><td>Enable **[Default]**</td><td>When 3DPRIMITIVE.End Offset Enable is set to 1, VF will use the guardband to determine when a draw call can be pre-empted. VF will not allow pre-emption in the guardband region.</td></tr><tr><td>1h</td><td>Disable</td><td>When set to Disable, there will not be any preemption or GB consideration for autodraw (3DPRIMITIVE.End Offset Enable set to 1).</td></tr></table>
	7	**Guardband Disable** <table><tr><td>Format:</td><td>U1</td></tr></table> <table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>0h</td><td>Enable **[Default]**</td><td>VF will use the guardband to determine when a draw call can be pre-empted. VF will not allow pre-emption in the guardband region.</td></tr><tr><td>1h</td><td>Disable</td><td>VF will not use the guardband to determine when a draw call can be pre-empted. VF will allow pre-emption on any vertex in the draw call.</td></tr></table>

VFSKPD - VF Scratch Pad

	6	Reserved	

	5	**TLB Prefectch Enable**	
		Project:	CHV, BSW
		Format:	U1

Value	Name	Description
0h	Disable **[Default]**	The VF will generate prefetch of TLB when it is fetching sequential vertex data and four or fewer vertex buffers are valid.
1h	Enable	VF will disable prefetch of TLB entries.

	4	Reserved
	3	Reserved

	2	**Vertex Cache Implicit Disable Inhibit**	
		Format:	U1

Value	Name	Description
0h	**[Default]**	Allow VF to disable VS0 when Sequential index or Prim ID is a valid Element.
1h		VF never implicitly disables the vertex cache. Software must disable the VS0 Cache when required.

	1	**Disable Over Fetch Cache**	
		Project:	CHV, BSW

Value	Name	Description
0h	**[Default]**	Cache will check for data in cache before making a request to memory
1h		Always re-fetch new data from memory.

Programming Notes
Note that the Disable Multiple Miss Read squash bit must be cleared for Disable Over Fetch Cache to be set.

	0	**Disable Multiple Miss Read squash**	
		Project:	CHV, BSW
		Format:	Disable

Value	Name	Description
0h	**[Default]**	Allow VF to squash reads that are to the same cacheline for vertex buffer requests.
1h		Disallow VF from squashing reads that are to the same cacheline for vertex buffer requests.

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VFW Credit Count Register

VFW_CREDIT_CNT - VFW Credit Count Register	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoEnhancementCS
Default Value:	0x00000002 CHV, BSW
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	08810h
Address:	08910h

DWord	Bit	Description
0	31:8	**Reserved**
	7:0	**Credit Count** The number of outstanding credits between VFW and GAV. If zero VEBOX cannot proceed due to GAV not releasing credits.

Value	Name	Project
2h	**[Default]**	CHV, BSW

VIC Virtual page Address Registers

VICTLB_VA - VIC Virtual page Address Registers	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	04900h-04903h

These registers are directly mapped to the current Virtual Addresses in the VICTLB (Vertex Fetch, Instruction Cache, and Command Streamer TLB.)

DWord	Bit	Description
0	31:12	**Address**
		Format: GraphicsAddress[31:12]
		Page virtual address.
	11:0	**Reserved**
		Format: MBZ

VIDEOBUSYCOUNTER

VIDEOBUSYCOUNTER - VIDEOBUSYCOUNTER		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	138124h	

SOXi Context Save/Restore : No
The 40-bit HW counter will wrap around. The only clear condition is CZ reset.
When 0x13_8104[15] is set to zero, bits 31:0 of the 40-bit counter are reported. When 0x13_8104[15] is set to one, its 39:8 of the 40-bit counter are reported.
The units are CZ clock cycles.
It is up to SW to periodically read this register and do a difference from the last time it was read. The primary usage for those registers for power characterization.
0x13_8104[7] controls if this register should count or if it should be gated: 0= clear, 1= count

DWord	Bit	Description	
0	31:0	**VIDEOBUSYTIME**	
		Default Value:	00000000h
		Access:	RO
		Render RC0 Residency Counter.	

Video Enhancement Mode Register

VEBOX_MODE - Video Enhancement Mode Register		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	VideoEnhancementCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	1A29Ch	

DWord	Bit	Description
0	31:16	**Mask Bits** Format: Mask[15:0] Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)
	15	**Execlist Enable** Default Value: 0h Project: CHV, BSW Mask: MMIO#31 When set, software can utilize the execlist registers to load a context into hardware. When this bit is clear the execlist mechanism cannot be used. The ring must be loaded via MMIO access. **Programming Notes** This bit is not intended to be changed dynamically. Changing the value of this bit while rendering is in progress will have UNDEFINED results. This bit should be changed only after a full reset and before submitting any commands to the device
	14	**Interrupt Steering Bit** Project: CHV, BSW Format: U1 When set, Command Streamer sends interrupt messages to the SHIM of the ON CHIP Micro Controller through message channel. When reset, Command Streamer sends the interrupt messages to Display Engine as config writes on GAM interface.
	13:10	**Reserved** Project: All Format: MBZ
	9	**Per-Process GTT Enable** Project: All Format: Enable Per-Process GTT BS Mode Enable

VEBOX_MODE - Video Enhancement Mode Register

Value	Name	Description
0h	PPGTT Disable **[Default]**	When clear, the Global GTT will be used to translate memory access from designated commands and for commands that select the PPGTT as their translation space in Basic Scheduler Mode.
1h	PPGTT Enable	When set, the PPGTT will be used to translate memory access from designated commands and for commands that select the PPGTT as their translation space.

Programming Notes	Project
This bit is used for enabling PPGTT access in Ring Buffer mode of scheduling. Privilege field in context descriptor states the same in Execlist mode of scheduling. This field should be set before programming PDP0/1/2/3 registers in order to set the PPGTT translation of memory access.	CHV, BSW

8 **Reserved**

Project:	CHV, BSW

7 **64Bit Virtual Addressing Enable**

Project:	CHV, BSW
Format:	Enable

Per-Process GTT Enable

Value	Name	Description	Project
0h	64Bit Virtual Addressing Disable **[Default]**	When clear indicates GFX operating in 32bit Virtual Addressing for PPGTT based memory access.	All

Programming Notes
This bit is only valid when PPGTT is enabled in ring buffer mode of scheduling. Context Descriptor has a similar bit to control 64bit virtual addressing in execlist mode of scheduling. Irrespective of this field set or clear virtual addresses translated through GGTT are always 32Bit. This field should be programmed before enabling PPGTT access. When this field is not set or for GGTT virtual addresses, Graphics Address [47:32] field of any commands or register exercised by SW should be programmed to 0x0.
64 Bit Virtual Addressing is not supported on CHV, BSW and must not be set.

6:5 **Reserved**

Project:	All
Format:	MBZ

4 **Reserved**

Project:	CHV, BSW

3:1 **Reserved**

Project:	CHV, BSW
Format:	MBZ

	VEBOX_MODE - Video Enhancement Mode Register	
	0	**Privilege Check Disable**
		Project: CHV, BSW
		Format: Enable
		This field when set, disables Privilege Violation checks on non-privileged batch buffers. When set Privileged commands are allowed to be executed from non-privileged batch buffers.

Video Mode Register

MFX_MODE - Video Mode Register	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	VideoCS, VideoCS2
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	1229Ch
Valid Projects:	CHV, BSW

DWord	Bit	Description
0	31:16	**Mask Bits** Format: Mask[15:0] Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)
	15	**Execlist Enable** Default Value: 0h Project: CHV, BSW Mask: MMIO#31 When set, software can utilize the execlist registers to load a context into hardware. When this bit is clear the Execution List mechanism cannot be used. The ring must be loaded via MMIO access. **Programming Notes** This bit is not intended to be changed dynamically. Changing the value of this bit while rendering is in progress will have UNDEFINED results. This bit should be changed only after a full reset and before submitting any commands to the device
	14	**Interrupt Steering Bit** Project: CHV, BSW Format: U1 When set, Command Streamer sends interrupt messages to the SHIM of the ON CHIP Micro Controller through message channel. When reset, Command Streamer sends the interrupt messages to Display Engine as config writes on GAM interface.
	13:10	**Reserved** Project: All Format: MBZ

MFX_MODE - Video Mode Register

	9	**Per-Process GTT Enable**	
		Format:	Enable Per-Process GTT BS Mode Enable

Value	Name	Description
0h	PPGTT Disable **[Default]**	When clear, the Global GTT will be used to translate memory access from designated commands and for commands that select the PPGTT as their translation space.
1h	PPGTT Enable	When set, the PPGTT will be used to translate memory access from designated commands and for commands that select the PPGTT as their translation space.

Programming Notes
This bit is used for enabling PPGTT access in Ring Buffer mode of scheduling. Privilege field in context descriptor states the same in Execlist Mode of scheduling. This field should be set before programming PDP0/1/2/3 registers in order to set the PPGTT translation of memory access.

	8	**Reserved**	
		Project:	CHV, BSW

	7	**64Bit Virtual Addressing Enable**	
		Project:	CHV, BSW
		Format:	Enable

Per-Process GTT Enable

Value	Name	Description
0h	64Bit Virtual Addressing Disable **[Default]**	When clear indicates GFX operating in 32bit Virtual Addressing for PPGTT based memory access.

Programming Notes
This bit is only valid when PPGTT is enabled in ring buffer mode of scheduling. Context Descriptor has a similar bit to control 64bit virtual addressing in execlist mode of scheduling. Irrespective of this field set or clear virtual addresses translated through GGTT are always 32Bit. This field should be programmed before enabling PPGTT access. When this field is not set or for GGTT virtual addresses, Graphics Address [47:32] field of any commands or register exercised by SW should be programmed to 0x0.
64 Bit Virtual Addressing is not supported on CHV, BSW and must not be set.

	6:5	**Reserved**	
		Project:	All
		Format:	MBZ

	4	**Reserved**	
		Project:	CHV, BSW

MFX_MODE - Video Mode Register			
	3:1	**Reserved**	
		Project:	CHV, BSW
		Format:	MBZ
	0	**Privilege Check Disable**	
		Project:	CHV, BSW
		Format:	Enable
		This field when set, disables Privilege Violation checks on non-privileged batch buffers. When set Privileged commands are allowed to be executed from non-privileged batch buffers.	

VS Invocation Counter

VS_INVOCATION_COUNT - VS Invocation Counter	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	RenderCS
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Trusted Type:	1
Address:	02320h
Valid Projects:	

This register stores the value of the vertex count shaded by VS. This register is part of the context save and restore.

DWord	Bit	Description
0	63:32	**VS Invocation Count Report UDW** Number of vertices that are dispatched as threads by the VS stage. Updated only when **Statistics Enable** is set in VS_STATE (see the Vertex Shader Chapter in the 3D Volume.)
	31:0	**VS Invocation Count Report LDW** Number of vertices that are dispatched as threads by the VS stage. Updated only when **Statistics Enable** is set in VS_STATE (see the Vertex Shader Chapter in the 3D Volume.)

Wait For Event and Display Flip Flags Register

<table>
<tr><td colspan="2" align="center">**SYNC_FLIP_STATUS - Wait For Event and Display Flip Flags Register**</td></tr>
<tr><td>Register Space:</td><td>MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td>CHV, BSW</td></tr>
<tr><td>Source:</td><td>PRM</td></tr>
<tr><td>Default Value:</td><td>0x00000000</td></tr>
<tr><td>Access:</td><td>R/W</td></tr>
<tr><td>Size (in bits):</td><td>32</td></tr>
<tr><td>Address:</td><td>022D0h</td></tr>
<tr><td>Name:</td><td>RCS Wait For Event and Display Flip Flags Register</td></tr>
<tr><td>ShortName:</td><td>RCS_SYNC_FLIP_STATUS</td></tr>
<tr><td>Valid Projects:</td><td>CHV, BSW</td></tr>
<tr><td>Address:</td><td>122D0h-122D3h</td></tr>
<tr><td>Name:</td><td>Wait For Event and Display Flip Flags Register</td></tr>
<tr><td>ShortName:</td><td>SYNC_FLIP_STATUS_VCSUNIT0</td></tr>
<tr><td>Address:</td><td>1A2D0h-1A2D3h</td></tr>
<tr><td>Name:</td><td>Wait For Event and Display Flip Flags Register</td></tr>
<tr><td>ShortName:</td><td>SYNC_FLIP_STATUS_VECSUNIT</td></tr>
<tr><td>Address:</td><td>1C2D0h-1C2D3h</td></tr>
<tr><td>Name:</td><td>Wait For Event and Display Flip Flags Register</td></tr>
<tr><td>ShortName:</td><td>SYNC_FLIP_STATUS_VCSUNIT1</td></tr>
<tr><td>Address:</td><td>222D0h</td></tr>
<tr><td>Name:</td><td>BCS Wait For Event and Display Flip Flags Register</td></tr>
<tr><td>ShortName:</td><td>BCS_SYNC_FLIP_STATUS</td></tr>
<tr><td>Valid Projects:</td><td>CHV, BSW</td></tr>
<tr><td colspan="2">This register is the saved value of what wait for events are still valid. This register is part of context save and restore for RC6 feature.</td></tr>
<tr><td colspan="2" align="center">**Programming Notes**</td></tr>
<tr><td colspan="2">**Programming Restriction:** This register should NEVER be programmed by SW, this is for HW internal use only.</td></tr>
</table>

DWord	Bit	Description
0	31	**Reserved**
		Format: MBZ
	30	**Display Plane A Asyncronous Display Flip Pending**
		Format: Enable

SYNC_FLIP_STATUS - Wait For Event and Display Flip Flags Register

		This field enables a wait for the duration of a Display Plane A "Flip Pending" condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.	
	29	**Display Plane A Syncronous Flip Display Pending**	
		Format:	Enable
		This field enables a wait for the duration of a Display Plane A "Flip Pending" condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.	
	28	**Display Sprite A Syncronous Flip Display Pending**	
		Format:	Enable
		This field enables a wait for the duration of a Display Sprite A "Flip Pending" condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.	
	27	**Reserved**	
		Format:	MBZ
	26	**Display Plane B Asyncronous Display Flip Pending**	
		Format:	Enable
		This field enables a wait for the duration of a Display Plane B "Flip Pending" condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.	
	25	**Display Plane B Syncronous Flip Display Pending**	
		Format:	Enable
		This field enables a wait for the duration of a Display Plane B Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.	
	24	**Display Sprite B Syncronous Flip Display Pending**	
		Format:	Enable
		This field enables a wait for the duration of a Display Sprite B Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.	

SYNC_FLIP_STATUS - Wait For Event and Display Flip Flags Register

23	**Reserved**	
	Source:	BlitterCS
	Format:	MBZ

23	**Display Plane A Asyncronous Performance Flip Pending Wait Enable**	
	Source:	RenderCS
	Format:	Enable
	This field enables a wait for the duration of a Display Plane A Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.	

22	**Display Plane A Asyncronous Flip Pending Wait Enable**	
	Format:	Enable
	This field enables a wait for the duration of a Display Plane A Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.	

21	**Display Plane A Syncronous Flip Pending Wait Enable**	
	Format:	Enable
	This field enables a wait for the duration of a Display Plane A Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.	

20	**Display Sprite A Syncronous Flip Pending Wait Enable**	
	Format:	Enable
	This field enables a wait for the duration of a Display Sprite A Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.	

19	**Reserved**	
	Format:	MBZ

18	**Display Pipe A Scan Line Wait Enable**	
	Format:	Enable
	This field enables a wait while a Display Pipe A Scan Line condition exists. This condition is defined as the the start of the scan line specified in the Pipe A Display Scan Line Count Range Compare Register. See Scan Line Event in the Device Programming Interface chapter of MI Functions.	

SYNC_FLIP_STATUS - Wait For Event and Display Flip Flags Register

17	**Display Pipe A Vertical Blank Wait Enable**	
	Format:	Enable
	This field enables a wait until the next Display Pipe A Vertical Blank event occurs. This event is defined as the start of the next Display Pipe A vertical blank period. Note that this can cause a wait for up to an entire refresh period. See Vertical Blank Event (See Programming Interface).	

16	**Reserved**	
	Project:	CHV, BSW
	Format:	MBZ

15	**Reserved**	
	Source:	BlitterCS
	Format:	MBZ

15	**Display Plane B Asyncronous Performance Flip Pending Wait Enable**	
	Source:	RenderCS
	Format:	Enable
	This field enables a wait for the duration of a Display Plane B Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.	

14	**Display Plane B Asyncronous Flip Pending Wait Enable**	
	Format:	Enable
	This field enables a wait for the duration of a Display Plane B Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.	

13	**Display Plane B Syncronous Flip Pending Wait Enable**	
	Format:	Enable
	This field enables a wait for the duration of a Display Plane B Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.	

12	**Display Sprite B Syncronous Flip Pending Wait Enable**	
	Format:	Enable

SYNC_FLIP_STATUS - Wait For Event and Display Flip Flags Register

		This field enables a wait for the duration of a Display Sprite B Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.

	11	**Reserved**

Format:	MBZ

	10	**Display Pipe B Scan Line Wait Enable**

Format:	Enable

This field enables a wait while a Display Pipe B Scan Line condition exists. This condition is defined as the the start of the scan line specified in the Pipe B Display Scan Line Count Range Compare Register. See Scan Line Event in the Device Programming Interface chapter of MI Functions.

	9	**Display Pipe B Vertical Blank Wait Enable**

Format:	Enable

This field enables a wait until the next Display Pipe B Vertical Blank event occurs. This event is defined as the start of the next Display Pipe B vertical blank period. Note that this can cause a wait for up to an entire refresh period. See Vertical Blank Event (See Programming Interface).

	8	**Reserved**

Project:	CHV, BSW
Format:	MBZ

	7:5	**Reserved**

Format:	MBZ

	4:0	**Reserved**

Project:	CHV, BSW
Format:	MBZ

Wait For Event and Display Flip Flags Register 1

<table>
<tr><td colspan="3" align="center">**SYNC_FLIP_STATUS_1 - Wait For Event and Display Flip Flags Register 1**</td></tr>
<tr><td>Register Space:</td><td colspan="2">MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td colspan="2">CHV, BSW</td></tr>
<tr><td>Source:</td><td colspan="2">PRM</td></tr>
<tr><td>Default Value:</td><td colspan="2">0x00000000</td></tr>
<tr><td>Access:</td><td colspan="2">R/W</td></tr>
<tr><td>Size (in bits):</td><td colspan="2">32</td></tr>
<tr><td>Address:</td><td colspan="2">022D4h</td></tr>
<tr><td>Name:</td><td colspan="2">RCS Wait For Event and Display Flip Flags Register 1</td></tr>
<tr><td>ShortName:</td><td colspan="2">RCS_SYNC_FLIP_STATUS_1</td></tr>
<tr><td>Address:</td><td colspan="2">122D4h-122D7h</td></tr>
<tr><td>Name:</td><td colspan="2">Wait For Event and Display Flip Flags Register 1</td></tr>
<tr><td>ShortName:</td><td colspan="2">SYNC_FLIP_STATUS_1_VCSUNIT0</td></tr>
<tr><td>Address:</td><td colspan="2">1A2D4h-1A2D7h</td></tr>
<tr><td>Name:</td><td colspan="2">Wait For Event and Display Flip Flags Register 1</td></tr>
<tr><td>ShortName:</td><td colspan="2">SYNC_FLIP_STATUS_1_VECSUNIT</td></tr>
<tr><td>Address:</td><td colspan="2">1C2D4h-1C2D7h</td></tr>
<tr><td>Name:</td><td colspan="2">Wait For Event and Display Flip Flags Register 1</td></tr>
<tr><td>ShortName:</td><td colspan="2">SYNC_FLIP_STATUS_1_VCSUNIT1</td></tr>
<tr><td>Address:</td><td colspan="2">222D4h</td></tr>
<tr><td>Name:</td><td colspan="2">BCS Wait For Event and Display Flip Flags Register 1</td></tr>
<tr><td>ShortName:</td><td colspan="2">BCS_SYNC_FLIP_STATUS_1</td></tr>
<tr><td>Valid Projects:</td><td colspan="2">CHV, BSW</td></tr>
<tr><td colspan="3">This register is the saved value of what wait for events are still valid. This register is part of context save and restore for RC6 feature.</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td>**Description**</td></tr>
<tr><td>0</td><td>31:27</td><td>**Reserved**</td></tr>
<tr><td></td><td>26</td><td>**Display Sprite C3 Synchronous Flip Pending Wait Enable**

<table><tr><td>Project:</td><td>CHV, BSW</td></tr><tr><td>Format:</td><td>Enable</td></tr></table>
This field enables a wait for the duration of a Display Sprite C3 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</td></tr>
</table>

SYNC_FLIP_STATUS_1 - Wait For Event and Display Flip Flags Register 1

25	**Display Sprite C3 Synchronous Flip Display Pending**	
	Project:	CHV, BSW
	Format:	Enable

This field enables a wait for the duration of a Display Sprite C3 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.

24	**Display Sprite B3 Synchronous Flip Pending Wait Enable**	
	Project:	CHV, BSW
	Format:	Enable

This field enables a wait for the duration of a Display Sprite B3 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.

23	**Display Sprite B3 Synchronous Flip Display Pending**	
	Project:	CHV, BSW
	Format:	Enable

This field enables a wait for the duration of a Display Sprite B3 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.

22	**Display Sprite A3 Synchronous Flip Pending Wait Enable**	
	Project:	CHV, BSW
	Format:	Enable

This field enables a wait for the duration of a Display Sprite A3 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.

21	**Display Sprite A3 Synchronous Flip Display Pending**	
	Project:	CHV, BSW
	Format:	Enable

This field enables a wait for the duration of a Display Sprite A3 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.

SYNC_FLIP_STATUS_1 - Wait For Event and Display Flip Flags Register 1

20	**Display Sprite C2 Synchronous Flip Pending Wait Enable**	
	Project:	CHV, BSW
	Format:	Enable

This field enables a wait for the duration of a Display Sprite C2 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.

19	**Display Sprite C2 Synchronous Flip Display Pending**	
	Project:	CHV, BSW
	Format:	Enable

This field enables a wait for the duration of a Display Sprite C2 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.

18	**Display Sprite B2 Synchronous Flip Pending Wait Enable**	
	Project:	CHV, BSW
	Format:	Enable

This field enables a wait for the duration of a Display Sprite B2 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.

17	**Display Sprite B2 Synchronous Flip Display Pending**	
	Project:	CHV, BSW
	Format:	Enable

This field enables a wait for the duration of a Display Sprite B2 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.

16	**Display Sprite A2 Synchronous Flip Pending Wait Enable**	
	Project:	CHV, BSW
	Format:	Enable

This field enables a wait for the duration of a Display Sprite A2 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.

SYNC_FLIP_STATUS_1 - Wait For Event and Display Flip Flags Register 1

15	**Display Sprite A2 Synchronous Flip Display Pending**	
	Project:	CHV, BSW
	Format:	Enable

This field enables a wait for the duration of a Display Sprite A2 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.

14	**Display Plane C Scan Line Event Pending**	
	Project:	CHV, BSW
	Format:	Enable

This field indicates scan line event operation is pending from Display Plane-C. This field gets set when MI_SCANLINE_INCL/EXCL command is parsed for Display Plane-C and gets reset on scan line event completion for Display Plane-C.

13	**Display Plane B Scan Line Event Pending**	
	Project:	CHV, BSW
	Format:	Enable

This field indicates scan line event operation is pending from Display Plane-B. This field gets set when MI_SCANLINE_INCL/EXCL command is parsed for Display Plane-B and gets reset on scan line event completion for Display Plane-B.

12	**Display Plane A Scan Line Event Pending**	
	Project:	CHV, BSW
	Format:	Enable

This field indicates scan line event operation is pending from Display Plane-A. This field gets set when MI_SCANLINE_INCL/EXCL command is parsed for Display Plane-A and gets reset on scan line event completion for Display Plane-A.

11	**Reserved**	
	Project:	CHV, BSW
	Format:	MBZ

10	**Display Plane C Asyncronous Display Flip Pending**	
	Format:	Enable

This field enables a wait for the duration of a Display Plane C Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.

SYNC_FLIP_STATUS_1 - Wait For Event and Display Flip Flags Register 1

9	**Display Plane C Syncronous Flip Display Pending**	
	Format:	Enable
	This field enables a wait for the duration of a Display Plane C Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.	

8	**Display Sprite C Syncronous Flip Display Pending**	
	Format:	Enable
	This field enables a wait for the duration of a Display Sprite C Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.	

7	**Reserved**	
	Source:	BlitterCS
	Format:	MBZ

7	**Display Plane C Asyncronous Performance Flip Pending Wait Enable**	
	Source:	RenderCS
	Format:	Enable
	This field enables a wait for the duration of a Display Plane C Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.	

6	**Display Plane C Asyncronous Flip Pending Wait Enable**	
	Format:	Enable
	This field enables a wait for the duration of a Display Plane C "Flip Pending" condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.	

5	**Display Plane C Syncronous Flip Pending Wait Enable**	
	Format:	Enable
	This field enables a wait for the duration of a Display Plane C Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.	

SYNC_FLIP_STATUS_1 - Wait For Event and Display Flip Flags Register 1

	4	**Display Sprite C Syncronous Flip Pending Wait Enable**	
		Format:	Enable
		This field enables a wait for the duration of a Display Sprite C Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.	
	3	**Reserved**	
		Format:	MBZ
	2	**Display Pipe C Scan Line Wait Enable**	
		Format:	Enable
		This field enables a wait while a Display Pipe C Scan Line condition exists. This condition is defined as the the start of the scan line specified in the Pipe C Display Scan Line Count Range Compare Register. See Scan Line Event in the Device Programming Interface chapter of MI Functions.	
	1	**Display Pipe C Vertical Blank Wait Enable**	
		Format:	Enable
		This field enables a wait until the next Display Pipe C Vertical Blank event occurs. This event is defined as the start of the next Display Pipe C vertical blank period. Note that this can cause a wait for up to an entire refresh period. See Vertical Blank Event (See Programming Interface).	
	0	**Reserved**	
		Project:	CHV, BSW
		Format:	MBZ

Walkers Fault Register

WF_REG - Walkers Fault Register		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04098h	
DWord	**Bit**	**Description**
0	31:1	**Walkers Fault Register**
		Default Value: 00000000000000000000000000000b
		Access: R/W
		All bits are only valid with bit[0]=1.
	0	**Valid Bit**
		Default Value: 0b
		Access: R/W
		This bit indicates that the first fault for this engine has been recorded. It can only be cleared by SW, which also clears the other fields.

WD_WNIC_MSG_ADDR

WD_WNIC_MSG_ADDR - WD_WNIC_MSG_ADDR		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	6E530h	
WNIC Message Address. This is a register within Gunit (CZ domain). Address uses the address as shown.		
DWord	**Bit**	**Description**
0	31:0	**Reserved**

WGBOX State Arbitration Priority Control

APC - WGBOX State Arbitration Priority Control		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
DWord	**Bit**	**Description**
0	31:9	**Reserved**
		Format: MBZ

WIDI LRA 0

WIDI_LRA_0 - WIDI LRA 0		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x37201F00	
Size (in bits):	32	
Address:	04A90h	

DWord	Bit	Description		
0	31:30	**Reserved**		
		Default Value:		00b
	29:24	**WIDI LRA1 Max**		
		Default Value:		110111b
		Access:		R/W
		Maximum value of programmable LRA1.		
	23:22	**Reserved**		
		Default Value:		00b
		Access:		RO
	21:16	**WIDI LRA1 Min**		
		Default Value:		100000b
		Access:		R/W
		Minimum value of programmable LRA1.		
	15:14	**Reserved**		
		Default Value:		00b
		Access:		RO
	13:8	**WIDI LRA0 Max**		
		Default Value:		011111b
		Access:		R/W
		Maximum value of programmable LRA0.		
	7:6	**Reserved**		
		Default Value:		00b
		Access:		RO
	5:0	**WIDILRA0 Min**		
		Default Value:		000000b
		Access:		R/W
		Minimum value of programmable LRA0.		

WIDI LRA 1

<table>
<tr><td colspan="3" align="center">**WIDI_LRA_1 - WIDI LRA 1**</td></tr>
<tr><td>Register Space:</td><td colspan="2">MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td colspan="2">CHV, BSW</td></tr>
<tr><td>Source:</td><td colspan="2">PRM</td></tr>
<tr><td>Default Value:</td><td colspan="2">0x01000000</td></tr>
<tr><td>Size (in bits):</td><td colspan="2">32</td></tr>
<tr><td>Address:</td><td colspan="2">04A94h</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td>**Description**</td></tr>
<tr><td rowspan="8">0</td><td>31:30</td><td>**Reserved**

Default Value: 00b
Access: RO</td></tr>
<tr><td>29:28</td><td>**VMX**

Default Value: 00b
Access: R/W
Which LRA should VMX use.</td></tr>
<tr><td>27:26</td><td>**BSP**

Default Value: 00b
Access: R/W
Which LRA should BSP use.</td></tr>
<tr><td>25:24</td><td>**IME**

Default Value: 01b
Access: R/W
Which LRA should IME/WRS use.</td></tr>
<tr><td>23:14</td><td>**Reserved**

Default Value: 0000000000b
Access: RO</td></tr>
<tr><td>13:8</td><td>**Reserved**</td></tr>
<tr><td>7:6</td><td>**Reserved**

Default Value: 00b
Access: RO</td></tr>
<tr><td>5:0</td><td>**Reserved**</td></tr>
</table>

WIDI TLB Control Register

WTCR - WIDI TLB Control Register		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04278h	

DWord	Bit	Description
0	31:1	**Reserved**
		Default Value: 00000000000000000000000000000b
		Access: RO
	0	**Invalidate TLBs on the corresponding Engine**
		Default Value: 0b
		Access: R/W
		SW writes 1 to invalidate the TLBs for the associated engine and HW clears the bit when invalidation is complete. To ensure proper invalidation of the TLBs, SW has to ensure the corresponding engine's HW pipeline is flushed and cleared from all its memory accesses. Otherwise HW cannot guarantee the proper invalidation for TLBs. This bit is self clear.

WRID_VALID_REG0

WRID_VALID_REG0 - WRID_VALID_REG0	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	04070h

DWord	Bit	Description
0	31:0	**WRID_VALID_REG0** <table><tr><td>Default Value:</td><td>00000000h</td></tr><tr><td>Access:</td><td>RO</td></tr></table> This register is for WRID Comparison usage. RO register with IA Access Type on DEV reset. wrdp_wrid_valid_vector[31:0] There are 96 write buffer. Each bit indicate the buffer is valid if set. Divide into 3 registers to accommodate all 96 deep

WRID_VALID_REG1

WRID_VALID_REG1 - WRID_VALID_REG1	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	04074h

DWord	Bit	Description	
0	31:0	**WRID_VALID_REG1**	
		Default Value:	00000000h
		Access:	RO
		This register is for WRID Comparison usage. RO register with IA Access Type on DEV reset. wrdp_wrid_valid_vector[63:32] There are 96 write buffer. Each bit indicate the buffer is valid if set. Divide into 3 registers to accommodate all 96 deep.	

WRID_VALID_REG2

WRID_VALID_REG2 - WRID_VALID_REG2	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x00000000
Size (in bits):	32
Address:	04078h

DWord	Bit	Description
0	31:0	**WRID_VALID_REG2**
		<table><tr><td>Default Value:</td><td>00000000h</td></tr><tr><td>Access:</td><td>RO</td></tr></table> This register is for WRID Comparison usage. RO register with IA Access Type on DEV reset. wrdp_wrid_valid_vector[95:64] There are 96 write buffer. Each bit indicate the buffer is valid if set. Divide into 3 registers to accommodate all 96 deep.

Write Watermark

WR_WATERMARK - Write Watermark	
Register Space:	MMIO: 0/2/0
Project:	CHV, BSW
Source:	PRM
Default Value:	0x000FFEA4
Size (in bits):	32
Address:	04028h

DWord	Bit	Description		
0	31:20	**Extra Bits**		
		Default Value:	000000000000b	
		Access:	R/W	
	19	**Watermark Timeout Enable**		
		Default Value:		1b
		Access:		R/W
	18:8	**Watermark Timeout**		
		Default Value:	11111111110b	
		Access:	R/W	
		Number of clocks that the write pipe queue is allowed to keep a ready write cycle, without reads or writes to the queue. Once this value is met, and if the feature is enabled, the watermark is considered reached, and all pending write requests are issued.		
	7	**Watermark Enable**		
		Default Value:		1b
		Access:		R/W
		Enable Write Request Grouping		
	6:0	**High Watermark**		
		Default Value:	0100100b	
		Access:	R/W	
		This is the number of write requests to be collected before initiating a write burst. Once a burst is initiated, it continues until all the available writes are requested.		

ZTLB LRA 0

ZTLB_LRA_0 - ZTLB LRA 0		
Register Space:	MMIO: 0/2/0	
Project:	CHV, BSW	
Source:	PRM	
Default Value:	0x01007E00	
Size (in bits):	32	
Address:	04A30h	

DWord	Bit	Description	
0	31:29	**Reserved**	
		Default Value:	000b
		Project:	CHV, BSW
		Access:	RO
	28:27	**STC LRA**	
		Default Value:	00b
		Access:	R/W
		Which LRA should STC use.	
	26:18	**ZTLB LRA1 Min**	
		Default Value:	001000000b
		Access:	R/W
		Minimum value of programmable LRA1.	
	17:9	**ZTLB LRA0 Max**	
		Default Value:	000111111b
		Access:	R/W
		Maximum value of programmable LRA0.	
	8:0	**ZTLB LRA0 Min**	
		Default Value:	000000000b
		Access:	R/W
		Minimum value of programmable LRA0.	

ZTLB LRA 1

<table>
<tr><td colspan="3" align="center">**ZTLB_LRA_1 - ZTLB LRA 1**</td></tr>
<tr><td>Register Space:</td><td colspan="2">MMIO: 0/2/0</td></tr>
<tr><td>Project:</td><td colspan="2">CHV, BSW</td></tr>
<tr><td>Source:</td><td colspan="2">PRM</td></tr>
<tr><td>Default Value:</td><td colspan="2">0x33FD80BF CHV, BSW</td></tr>
<tr><td>Size (in bits):</td><td colspan="2">32</td></tr>
<tr><td>Address:</td><td colspan="2">04A34h</td></tr>
<tr><td>**DWord**</td><td>**Bit**</td><td>**Description**</td></tr>
<tr><td rowspan="7">0</td><td>31</td><td>**Reserved**
Default Value: 0b
Access: RO</td></tr>
<tr><td>30:29</td><td>**HIZ LRA**
Default Value: 01b
Access: R/W
Which LRA should HIZ use.</td></tr>
<tr><td>28:27</td><td>**RCZ LRA**
Default Value: 10b
Access: R/W
Which LRA should RCZ use.</td></tr>
<tr><td>26:18</td><td>**ZTLB LRA2 Max**
Access: R/W
Maximum value of programmable LRA2.
Value: 011111111b Name: [Default] Project: CHV, BSW</td></tr>
<tr><td>17:9</td><td>**ZTLB LRA2 Min**
Default Value: 011000000b
Access: R/W
Minimum value of programmable LRA2.</td></tr>
<tr><td>8:0</td><td>**ZTLB LRA1 Max**
Default Value: 010111111b
Access: R/W
Maximum value of programmable LRA1.</td></tr>
</table>