



## **Intel® Open Source HD Graphics and Intel Iris™ Graphics**

### **Programmer's Reference Manual**

For the 2014-2015 Intel Core™ Processors, Celeron™ Processors  
and Pentium™ Processors based on the "Broadwell" Platform

Volume 2d: Command Reference: Structures

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## 3DSTATE\_CONSTANT(Body)

3DSTATE_CONSTANT(Body)						
DWord	Bit	Description				
0	31:16	<p><b>Constant Buffer 1 Read Length</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U16 read length</td> </tr> </table> <p>This field specifies the length of the constant data to be loaded from memory in 256-bit units.</p> <p><b>Programming Notes</b></p> <ul style="list-style-type: none"> <li>The sum of all four read length fields must be less than or equal to the size of 64</li> <li>Setting the value of the register to zero will disable buffer 1.</li> <li>If disabled, the <b>Pointer to Constant Buffer 1</b> must be programmed to zero.</li> </ul> <p>if gather constant are enabled, this field must be non-zero if a there was a preceding corresponding 3DSTATE_GATHER_CONSTANT_*, otherwise this field must be zero.</p>	Project:	All	Format:	U16 read length
Project:	All					
Format:	U16 read length					
<p><b>Constant Buffer 0 Read Length</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U16 read length</td> </tr> </table> <p>This field specifies the length of the constant data to be loaded from memory in 256-bit units.</p> <p><b>Programming Notes</b></p> <ul style="list-style-type: none"> <li>The sum of all four read length fields must be less than or equal to the size of 64</li> <li>Setting the value of the register to zero will disable buffer 0.</li> <li>If disabled, the <b>Pointer to Constant Buffer 0</b> must be programmed to zero.</li> </ul>	Project:	All	Format:	U16 read length		
Project:	All					
Format:	U16 read length					
1	31:16	<p><b>Constant Buffer 3 Read Length</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U16 read length</td> </tr> </table> <p>This field specifies the length of the constant data to be loaded from memory in 256-bit units.</p> <p><b>Programming Notes</b></p> <ul style="list-style-type: none"> <li>The sum of all four read length fields must be less than or equal to the size of 64</li> <li>Setting the value of the register to zero will disable buffer 3.</li> <li>If disabled, the <b>Pointer to Constant Buffer 3</b> must be programmed to zero.</li> </ul>	Project:	All	Format:	U16 read length
Project:	All					
Format:	U16 read length					

## 3DSTATE\_CONSTANT(Body)

	15:0	<b>Constant Buffer 2 Read Length</b>				
		<table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U16 read length</td></tr> </table>	Project:	All	Format:	U16 read length
Project:	All					
Format:	U16 read length					
		This field specifies the length of the constant data to be loaded from memory in 256-bit units.				
<b>Programming Notes</b>						
<ul style="list-style-type: none"> <li>The sum of all four read length fields must be less than or equal to the size of 64</li> <li>Setting the value of the register to zero will disable buffer 2.</li> <li>If disabled, the <b>Pointer to Constant Buffer 2</b> must be programmed to zero.</li> </ul>						
2..3 <b>Project:</b> BDW	63:5	<b>Pointer To Constant Buffer 0</b>				
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>GraphicsAddress[63:5]ConstantBuffer</td></tr> </table>	Project:	BDW	Format:	GraphicsAddress[63:5]ConstantBuffer
Project:	BDW					
Format:	GraphicsAddress[63:5]ConstantBuffer					
<b>Description</b>						
<p>When CONSTANT_BUFFER Address Offset Disable in INSTPM register is set, the value of this field is the virtual address of the location of the push constant buffer. GraphicsAddress [63:48] are ignored by the HW and assumed to be in correct canonical form [63:48] == [47]. When CONSTANT_BUFFER Address Offset Disable in INSTPM register is cleared, the value of this field is the offset into the Dynamic State Base Address. Only [47:5] of the field are added to the base address to generate the virtual address to be fetched from memory.</p>						
	4:0	<b>Reserved</b>				
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	BDW	Format:	MBZ
Project:	BDW					
Format:	MBZ					
4..5 <b>Project:</b> BDW	63:5	<b>Pointer To Constant Buffer 1</b>				
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>GraphicsAddress[63:5]ConstantBuffer</td></tr> </table>	Project:	BDW	Format:	GraphicsAddress[63:5]ConstantBuffer
Project:	BDW					
Format:	GraphicsAddress[63:5]ConstantBuffer					
<p>This field points to the location of Constant Buffer 1.</p>						
<p>If gather constants are enabled This field is an offset of constant Buffer1 from the Gather Pool BASE ADDRESS.</p> <p>If gather constants is disabled, the value of this field is the virtual address of the location of the push constant buffer. GraphicsAddress [63:48] are ignored by the HW and assumed to be in correct canonical form [63:48] == [47].</p>						
<b>Programming Notes</b>						
<p>Constant buffers must be allocated in linear (not tiled) graphics memory.</p>						
	4:0	<b>Reserved</b>				
		<table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	All	Format:	MBZ
Project:	All					
Format:	MBZ					

## 3DSTATE\_CONSTANT(Body)

<b>6..7</b> <b>Project:</b> BDW	<b>63:5</b>	<b>Pointer To Constant Buffer 2</b>		
		Project: BDW Format: GraphicsAddress[63:5]ConstantBuffer		
		The value of this field is the virtual address of the location of the push constant buffer 2. GraphicsAddress [63:48] are ignored by the HW and assumed to be in correct canonical form [63:48] == [47].		
<b>Programming Notes</b>				
Constant buffers must be allocated in linear (not tiled) graphics memory.				
<b>8..9</b> <b>Project:</b> BDW	<b>4:0</b>	<b>Reserved</b>		
		Project: BDW Format: MBZ		
<b>8..9</b> <b>Project:</b> BDW	<b>63:5</b>	<b>Pointer To Constant Buffer 3</b>		
		Project: BDW Format: GraphicsAddress[63:5]ConstantBuffer		
The value of this field is the virtual address of the location of the push constant buffer 3. GraphicsAddress [63:48] are ignored by the HW and assumed to be in correct canonical form [63:48] == [47].				
<b>Programming Notes</b>				
Constant buffers must be allocated in linear (not tiled) graphics memory.				
<b>8..9</b> <b>Project:</b> BDW	<b>4:0</b>	<b>Reserved</b>		
		Project: BDW Format: MBZ		

## A32 Buffer Base Address Message Header Control

<b>MHC_A32_BBA - A32 Buffer Base Address Message Header Control</b>						
<b>DWord</b>	<b>Bit</b>	<b>Description</b>				
0	31:0	<p><b>Buffer Base Address Offset</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>GeneralStateOffset[31:0]</td> </tr> </table> <p>Specifies the base address offset page [31:10] for A32 stateless messages.</p>	Project:	All	Format:	GeneralStateOffset[31:0]
Project:	All					
Format:	GeneralStateOffset[31:0]					

## A64 Data Size Message Descriptor Control Field

MDC_A64_DS - A64 Data Size Message Descriptor Control Field																					
DWord	Bit	Description																			
0	1:0	<p><b>Data Size</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Enumeration</td> </tr> </table> <p>Specifies the number of data elements to be read or written</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00h</td> <td>DE1</td> <td>1 data element (B, DW, QW)</td> </tr> <tr> <td>01h</td> <td>DE2</td> <td>2 data elements (B, DW, QW)</td> </tr> <tr> <td>02h</td> <td>DE4</td> <td>4 data elements (B, DW, QW)</td> </tr> <tr> <td>03h</td> <td>DE8</td> <td>8 data elements (B, DW, QW)</td> </tr> </tbody> </table> <p><b>Restriction</b></p> <p>The number of elements is constrained by SIMD Mode and Data Width. The max data payload limit is 256B: 2 elements SIMD16 QW, 4 elements SIMD16 DW, or 4 elements SIMD8 QW.</p>	Project:	All	Format:	Enumeration	Value	Name	Description	00h	DE1	1 data element (B, DW, QW)	01h	DE2	2 data elements (B, DW, QW)	02h	DE4	4 data elements (B, DW, QW)	03h	DE8	8 data elements (B, DW, QW)
Project:	All																				
Format:	Enumeration																				
Value	Name	Description																			
00h	DE1	1 data element (B, DW, QW)																			
01h	DE2	2 data elements (B, DW, QW)																			
02h	DE4	4 data elements (B, DW, QW)																			
03h	DE8	8 data elements (B, DW, QW)																			

## A64 Dual Oword Block Message Header

### MH\_A64\_OWDB - A64 Dual Oword Block Message Header

<p>Project: BDW</p> <p>Source: DataPort 1</p> <p>Size (in bits): 256</p> <p>Default Value: 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000</p>						
DWord	Bit	Description				
0-1	63:0	<p><b>BlockOffset0</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U64</td></tr> </table> <p>Specifies the U64 byte offset of Oword Block 0.</p> <p><b>Programming Notes</b></p> <p>If the BlockOffset is not in the 48-bit canonical address range, the access is Out-of-Bounds.</p> <p><b>Restriction</b></p> <p>The byte offset must be aligned to the message's data type. Dwords have [1:0] = 0, Qwords have [2:0] = 0, and Hwords have [4:0] = 0.</p>	Project:	All	Format:	U64
Project:	All					
Format:	U64					
2-3	63:0	<p><b>BlockOffset1</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U64</td></tr> </table> <p>Specifies the U64 byte offset of Oword Block 1.</p> <p><b>Programming Notes</b></p> <p>If the BlockOffset is not in the 48-bit canonical address range, the access is Out-of-Bounds.</p> <p><b>Restriction</b></p> <p>The byte offset must be aligned to the message's data type. Dwords have [1:0] = 0, Qwords have [2:0] = 0, and Hwords have [4:0] = 0.</p>	Project:	All	Format:	U64
Project:	All					
Format:	U64					
4-7	127:0	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>Ignore</td></tr> </table> <p>Ignored</p>	Project:	All	Format:	Ignore
Project:	All					
Format:	Ignore					

## A64 Hword Block Message Header

<b>MH_A64_HWB - A64 Hword Block Message Header</b>														
<b>DWord</b>	<b>Bit</b>	<b>Description</b>												
0-1	63:0	<p><b>BlockOffset</b></p> <table border="1"> <tr> <td>Format:</td> <td>U64</td> </tr> <tr> <td colspan="2">Specifies the U64 byte offset of Oword block.</td> </tr> <tr> <td align="center" colspan="2"><b>Programming Notes</b></td></tr> <tr> <td align="center" colspan="2">If the BlockOffset is not in the 48-bit canonical address range, the access is Out-of-Bounds.</td></tr> <tr> <td align="center" colspan="2"><b>Restriction</b></td></tr> <tr> <td align="center" colspan="2">The byte offset must be aligned to the message's data type. Dwords have [1:0] = 0, Qwords have [2:0] = 0, and Hwords have [4:0] = 0.</td></tr> </table>	Format:	U64	Specifies the U64 byte offset of Oword block.		<b>Programming Notes</b>		If the BlockOffset is not in the 48-bit canonical address range, the access is Out-of-Bounds.		<b>Restriction</b>		The byte offset must be aligned to the message's data type. Dwords have [1:0] = 0, Qwords have [2:0] = 0, and Hwords have [4:0] = 0.	
Format:	U64													
Specifies the U64 byte offset of Oword block.														
<b>Programming Notes</b>														
If the BlockOffset is not in the 48-bit canonical address range, the access is Out-of-Bounds.														
<b>Restriction</b>														
The byte offset must be aligned to the message's data type. Dwords have [1:0] = 0, Qwords have [2:0] = 0, and Hwords have [4:0] = 0.														
2-4	95:0	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>Ignore</td> </tr> <tr> <td colspan="2">Ignored</td> </tr> </table>	Format:	Ignore	Ignored									
Format:	Ignore													
Ignored														
5	31:0	<p><b>Hword Channel Mode</b></p> <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Format:</td> <td><b>MHC_A64_CMODE</b></td> </tr> <tr> <td colspan="2">Specifies the Hword Channel Mode</td> </tr> </table>	Project:	BDW	Format:	<b>MHC_A64_CMODE</b>	Specifies the Hword Channel Mode							
Project:	BDW													
Format:	<b>MHC_A64_CMODE</b>													
Specifies the Hword Channel Mode														
6-7	63:0	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>Ignore</td> </tr> <tr> <td colspan="2">Ignored</td> </tr> </table>	Format:	Ignore	Ignored									
Format:	Ignore													
Ignored														

## A64 Hword Data Blocks Message Descriptor Control Field

MDC_A64_DB_HW - A64 Hword Data Blocks Message Descriptor Control Field																								
DWord	Bit	Description																						
0	2:0	<p><b>Data Blocks</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Enumeration</td> </tr> </table> <p>Specifies the number of Hwords to be read or written</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>01h</td> <td>HW1 [Default]</td> <td>1 Hword block</td> </tr> <tr> <td>02h</td> <td>HW2</td> <td>2 Hword blocks</td> </tr> <tr> <td>03h</td> <td>HW4</td> <td>4 Hword blocks</td> </tr> <tr> <td>04h</td> <td>HW8</td> <td>8 Hword blocks</td> </tr> <tr> <td>Others</td> <td>Reserved</td> <td>Ignored</td> </tr> </tbody> </table>	Project:	All	Format:	Enumeration	Value	Name	Description	01h	HW1 [Default]	1 Hword block	02h	HW2	2 Hword blocks	03h	HW4	4 Hword blocks	04h	HW8	8 Hword blocks	Others	Reserved	Ignored
Project:	All																							
Format:	Enumeration																							
Value	Name	Description																						
01h	HW1 [Default]	1 Hword block																						
02h	HW2	2 Hword blocks																						
03h	HW4	4 Hword blocks																						
04h	HW8	8 Hword blocks																						
Others	Reserved	Ignored																						

## A64 Oword Block Message Header

<b>MH_A64_OWB - A64 Oword Block Message Header</b>						
<b>DWord</b>	<b>Bit</b>	<b>Description</b>				
0-1	63:0	<p><b>BlockOffset</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U64</td> </tr> </table> <p>Specifies the U64 byte offset of Oword block.</p> <p><b>Programming Notes</b></p> <p>If the BlockOffset is not in the 48-bit canonical address range, the access is Out-of-Bounds.</p> <p><b>Restriction</b></p> <p>The byte offset must be aligned to the message's data type. Dwords have [1:0] = 0, Qwords have [2:0] = 0, and Hwords have [4:0] = 0.</p>	Project:	All	Format:	U64
Project:	All					
Format:	U64					
2-7	191:0	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Ignore</td> </tr> </table> <p>Ignored</p>	Project:	All	Format:	Ignore
Project:	All					
Format:	Ignore					

## A64 Oword Data Blocks Message Descriptor Control Field

<b>MDC_A64_DB_OW - A64 Oword Data Blocks Message Descriptor Control Field</b>																											
<b>DWord</b>	<b>Bit</b>	<b>Description</b>																									
0	2:0	<p><b>Data Blocks</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Enumeration</td> </tr> </table> <p>Specifies the number of Oword blocks to be read or written</p> <table border="1"> <thead> <tr> <th><b>Value</b></th> <th><b>Name</b></th> <th><b>Description</b></th> </tr> </thead> <tbody> <tr> <td>00h</td> <td>OW1L</td> <td>1 Oword, read into or written from the low 128 bits of the destination register</td> </tr> <tr> <td>01h</td> <td>OW1U</td> <td>1 Oword, read into or written from the high 128 bits of the destination register</td> </tr> <tr> <td>02h</td> <td>OW2</td> <td>2 Owords</td> </tr> <tr> <td>03h</td> <td>OW4</td> <td>4 Owords</td> </tr> <tr> <td>04h</td> <td>OW8</td> <td>8 Owords</td> </tr> <tr> <td>Others</td> <td>Reserved</td> <td>Ignored</td> </tr> </tbody> </table>	Project:	All	Format:	Enumeration	<b>Value</b>	<b>Name</b>	<b>Description</b>	00h	OW1L	1 Oword, read into or written from the low 128 bits of the destination register	01h	OW1U	1 Oword, read into or written from the high 128 bits of the destination register	02h	OW2	2 Owords	03h	OW4	4 Owords	04h	OW8	8 Owords	Others	Reserved	Ignored
Project:	All																										
Format:	Enumeration																										
<b>Value</b>	<b>Name</b>	<b>Description</b>																									
00h	OW1L	1 Oword, read into or written from the low 128 bits of the destination register																									
01h	OW1U	1 Oword, read into or written from the high 128 bits of the destination register																									
02h	OW2	2 Owords																									
03h	OW4	4 Owords																									
04h	OW8	8 Owords																									
Others	Reserved	Ignored																									

## A64 Oword Dual Data Blocks Message Descriptor Control Field

<b>MDC_A64_DB_OWD - A64 Oword Dual Data Blocks Message Descriptor Control Field</b>																		
Project: BDW Size (in bits): 3 Default Value: 0x00000001																		
DWord	Bit	Description																
0	2:0	<b>Data Blocks</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>Enumeration</td></tr> </table> <p>Specifies the number of Oword blocks to be read or written</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>01h</td><td>OWD1 <b>[Default]</b></td><td>1 Hword register, 2 Owords</td></tr> <tr> <td>03h</td><td>OWD4</td><td>4 Hword registers, 8 Owords</td></tr> <tr> <td>Others</td><td>Reserved</td><td>Ignored</td></tr> </tbody> </table>	Project:	All	Format:	Enumeration	Value	Name	Description	01h	OWD1 <b>[Default]</b>	1 Hword register, 2 Owords	03h	OWD4	4 Hword registers, 8 Owords	Others	Reserved	Ignored
Project:	All																	
Format:	Enumeration																	
Value	Name	Description																
01h	OWD1 <b>[Default]</b>	1 Hword register, 2 Owords																
03h	OWD4	4 Hword registers, 8 Owords																
Others	Reserved	Ignored																

## AddrSubRegNum

AddrSubRegNum								
DWord	Bit	Description						
0	3:0	<p><b>Address Subregister Number</b></p> <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <th>Value</th> <th>Name</th> </tr> <tr> <td>0-15</td> <td>Address Subregister Number</td> </tr> </table>	Project:	BDW	Value	Name	0-15	Address Subregister Number
Project:	BDW							
Value	Name							
0-15	Address Subregister Number							

## Any Binding Table Index Message Descriptor Control Field

<b>MDC_BTS_SLM_A32 - Any Binding Table Index Message Descriptor Control Field</b>																											
<b>DWord</b>	<b>Bit</b>	<b>Description</b>																									
0	7:0	<p><b>Binding Table Index</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Enumeration</td> </tr> </table> <p>Specifies the surface for the message, which can be Surface State Model, SLM or Stateless.</p> <table border="1"> <thead> <tr> <th><b>Value</b></th> <th><b>Name</b></th> <th><b>Description</b></th> </tr> </thead> <tbody> <tr> <td>00h-0EFh</td> <td>BTS</td> <td>Index of Binding Table State Surfaces</td> </tr> <tr> <td>F0h-0FBh</td> <td>Reserved</td> <td>Reserved for future use</td> </tr> <tr> <td>0FCh</td> <td>Reserved</td> <td>Reserved for future use</td> </tr> <tr> <td>0FEh</td> <td>SLM</td> <td>Specifies an SLM access</td> </tr> <tr> <td>OFFh</td> <td>A32_A64</td> <td>Specifies a A32 or A64 Stateless access that is locally coherent (coherent within a thread group)</td> </tr> <tr> <td>0FDh</td> <td>A32_A64_NC</td> <td>Specifies a A32 or A64 Stateless access that is non-coherent (coherent within a thread).</td> </tr> </tbody> </table> <p><b>Restriction</b></p> <p>When using A32_A64_NC, SW must ensure that 2 threads do not both access the same cache line (64B)</p>	Project:	All	Format:	Enumeration	<b>Value</b>	<b>Name</b>	<b>Description</b>	00h-0EFh	BTS	Index of Binding Table State Surfaces	F0h-0FBh	Reserved	Reserved for future use	0FCh	Reserved	Reserved for future use	0FEh	SLM	Specifies an SLM access	OFFh	A32_A64	Specifies a A32 or A64 Stateless access that is locally coherent (coherent within a thread group)	0FDh	A32_A64_NC	Specifies a A32 or A64 Stateless access that is non-coherent (coherent within a thread).
Project:	All																										
Format:	Enumeration																										
<b>Value</b>	<b>Name</b>	<b>Description</b>																									
00h-0EFh	BTS	Index of Binding Table State Surfaces																									
F0h-0FBh	Reserved	Reserved for future use																									
0FCh	Reserved	Reserved for future use																									
0FEh	SLM	Specifies an SLM access																									
OFFh	A32_A64	Specifies a A32 or A64 Stateless access that is locally coherent (coherent within a thread group)																									
0FDh	A32_A64_NC	Specifies a A32 or A64 Stateless access that is non-coherent (coherent within a thread).																									

## Atomic Integer Binary Operation Message Descriptor Control Field

MDC_AOP2 - Atomic Integer Binary Operation Message Descriptor Control Field																																													
DWord	Bit	Description																																											
0	3:0	<p><b>Atomic Integer Operation Type</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Enumeration</td> </tr> </table> <p>Specifies the atomic integer binary operation to be performed</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>01h</td> <td>AOP_AND [Default]</td> <td>new_dst = old_dst AND src0</td> </tr> <tr> <td>02h</td> <td>AOP_OR</td> <td>new_dst = old_dst   src0</td> </tr> <tr> <td>03h</td> <td>AOP_XOR</td> <td>new_dst = old_dst ^ src0</td> </tr> <tr> <td>04h</td> <td>AOP_MOV</td> <td>new_dst = src0</td> </tr> <tr> <td>07h</td> <td>AOP_ADD</td> <td>new_dst = old_dst + src0</td> </tr> <tr> <td>08h</td> <td>AOP_SUB</td> <td>new_dst = old_dst - src0</td> </tr> <tr> <td>09h</td> <td>AOP_REVSUB</td> <td>new_dst = src0 - old_dst</td> </tr> <tr> <td>0Ah</td> <td>AOP_IMAX</td> <td>new_dst = imax(old_dst, src0)</td> </tr> <tr> <td>0Bh</td> <td>AOP_IMIN</td> <td>new_dst = imin(old_dst, src0)</td> </tr> <tr> <td>0Ch</td> <td>AOP_UMAX</td> <td>new_dst = umax(old_dst, src0)</td> </tr> <tr> <td>0Dh</td> <td>AOP_UMIN</td> <td>new_dst = umin(old_dst, src0)</td> </tr> <tr> <td>Others</td> <td>Reserved</td> <td>Ignored</td> </tr> </tbody> </table> <p><b>Programming Notes</b></p> <p>When Return Data Control is set, old_dst is returned.</p>	Project:	All	Format:	Enumeration	Value	Name	Description	01h	AOP_AND [Default]	new_dst = old_dst AND src0	02h	AOP_OR	new_dst = old_dst   src0	03h	AOP_XOR	new_dst = old_dst ^ src0	04h	AOP_MOV	new_dst = src0	07h	AOP_ADD	new_dst = old_dst + src0	08h	AOP_SUB	new_dst = old_dst - src0	09h	AOP_REVSUB	new_dst = src0 - old_dst	0Ah	AOP_IMAX	new_dst = imax(old_dst, src0)	0Bh	AOP_IMIN	new_dst = imin(old_dst, src0)	0Ch	AOP_UMAX	new_dst = umax(old_dst, src0)	0Dh	AOP_UMIN	new_dst = umin(old_dst, src0)	Others	Reserved	Ignored
Project:	All																																												
Format:	Enumeration																																												
Value	Name	Description																																											
01h	AOP_AND [Default]	new_dst = old_dst AND src0																																											
02h	AOP_OR	new_dst = old_dst   src0																																											
03h	AOP_XOR	new_dst = old_dst ^ src0																																											
04h	AOP_MOV	new_dst = src0																																											
07h	AOP_ADD	new_dst = old_dst + src0																																											
08h	AOP_SUB	new_dst = old_dst - src0																																											
09h	AOP_REVSUB	new_dst = src0 - old_dst																																											
0Ah	AOP_IMAX	new_dst = imax(old_dst, src0)																																											
0Bh	AOP_IMIN	new_dst = imin(old_dst, src0)																																											
0Ch	AOP_UMAX	new_dst = umax(old_dst, src0)																																											
0Dh	AOP_UMIN	new_dst = umin(old_dst, src0)																																											
Others	Reserved	Ignored																																											

## Atomic Integer Trinary Operation Message Descriptor Control Field

MDC_AOP3 - Atomic Integer Trinary Operation Message Descriptor Control Field																		
DWord	Bit	Description																
0	3:0	<p><b>Atomic Integer Operation Type</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Enumeration</td> </tr> </table> <p>Specifies the atomic integer trinary operation to be performed</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00h</td> <td>AOP_CMPWR_2W</td> <td><math>\text{new\_dst} = (\text{src0\_2W} == \text{old\_dst\_2W}) ? \text{src1\_2W} : \text{old\_dst\_2W}</math></td> </tr> <tr> <td>0Eh</td> <td>AOP_CMPWR [Default]</td> <td><math>\text{new\_dst} = (\text{src0} == \text{old\_dst}) ? \text{src1} : \text{old\_dst}</math></td> </tr> <tr> <td>Others</td> <td>Reserved</td> <td>Ignored</td> </tr> </tbody> </table> <p><b>Programming Notes</b></p> <p>When Return Data Control is set, old_dst is returned.</p>	Project:	All	Format:	Enumeration	Value	Name	Description	00h	AOP_CMPWR_2W	$\text{new\_dst} = (\text{src0\_2W} == \text{old\_dst\_2W}) ? \text{src1\_2W} : \text{old\_dst\_2W}$	0Eh	AOP_CMPWR [Default]	$\text{new\_dst} = (\text{src0} == \text{old\_dst}) ? \text{src1} : \text{old\_dst}$	Others	Reserved	Ignored
Project:	All																	
Format:	Enumeration																	
Value	Name	Description																
00h	AOP_CMPWR_2W	$\text{new\_dst} = (\text{src0\_2W} == \text{old\_dst\_2W}) ? \text{src1\_2W} : \text{old\_dst\_2W}$																
0Eh	AOP_CMPWR [Default]	$\text{new\_dst} = (\text{src0} == \text{old\_dst}) ? \text{src1} : \text{old\_dst}$																
Others	Reserved	Ignored																

## Atomic Integer Unary Operation Message Descriptor Control Field

<b>MDC_AOP1 - Atomic Integer Unary Operation Message Descriptor Control Field</b>																					
<b>DWord</b>	<b>Bit</b>	<b>Description</b>																			
0	3:0	<p><b>Atomic Integer Operation Type</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Enumeration</td> </tr> </table> <p>Specifies the atomic integer unary operation to be performed</p> <table border="1"> <thead> <tr> <th><b>Value</b></th> <th><b>Name</b></th> <th><b>Description</b></th> </tr> </thead> <tbody> <tr> <td>05h</td> <td>AOP_INC <b>[Default]</b></td> <td>new_dst = old_dst + 1</td> </tr> <tr> <td>06h</td> <td>AOP_DEC</td> <td>new_dst = old_dst - 1</td> </tr> <tr> <td>0Fh</td> <td>AOP_PREDEC</td> <td>new_dst = old_dst - 1</td> </tr> <tr> <td>Others</td> <td>Reserved</td> <td>Ignored</td> </tr> </tbody> </table> <p><b>Programming Notes</b></p> <p>When Return Data Control is set, new_dst is returned by AOP_PREDEC and otherwise old_dst is returned.</p>	Project:	All	Format:	Enumeration	<b>Value</b>	<b>Name</b>	<b>Description</b>	05h	AOP_INC <b>[Default]</b>	new_dst = old_dst + 1	06h	AOP_DEC	new_dst = old_dst - 1	0Fh	AOP_PREDEC	new_dst = old_dst - 1	Others	Reserved	Ignored
Project:	All																				
Format:	Enumeration																				
<b>Value</b>	<b>Name</b>	<b>Description</b>																			
05h	AOP_INC <b>[Default]</b>	new_dst = old_dst + 1																			
06h	AOP_DEC	new_dst = old_dst - 1																			
0Fh	AOP_PREDEC	new_dst = old_dst - 1																			
Others	Reserved	Ignored																			

## Audio Power State Format

Audio Power State Format														
DWord	Bit	Description												
0	1:0	<b>Power State</b> <table border="1"><thead><tr><th>Value</th><th>Name</th><th>Description</th></tr></thead><tbody><tr><td>00b</td><td>D0</td><td>D0</td></tr><tr><td>01b,10b</td><td>Unsupported</td><td>Unsupported</td></tr><tr><td>11b</td><td>D3 [Default]</td><td>D3</td></tr></tbody></table>	Value	Name	Description	00b	D0	D0	01b,10b	Unsupported	Unsupported	11b	D3 [Default]	D3
Value	Name	Description												
00b	D0	D0												
01b,10b	Unsupported	Unsupported												
11b	D3 [Default]	D3												

## AVC CABAC

AVC CABAC		
DWord	Bit	Description
0	15	<b>Reserved</b> Format: MBZ
	14	<b>Coefficient level out-of-bound Error</b> This flag indicates the coded coefficient level SEs in the bit-stream is out-of-bound.
	13	<b>Reserved</b> Format: MBZ
	12	<b>Reserved</b> Format: MBZ
	11	<b>Temporal Direction Motion Vector Out-of-Bound Error</b> This flag indicates motion vectors calculated from Temporal Direct Motion Vector is larger than the allowed range specified by the AVC spec.
	10	<b>Reserved</b> MBZ
	9	<b>Motion Vector Delta SE Out-of-Bound Error</b> This flag indicates inconsistent Motion Vector Delta SEs coded in the bit-stream.
	8	<b>Reference Index SE Out-of-Bound Error</b> This flag indicates inconsistent Reference Index SEs coded in the bit-stream.
	7	<b>MacroBlock QpDelta Error</b> This flag indicates out-of-bound MB QP delta SEs coded in the bit-stream.
	6	<b>Motion Vector Delta SE Error</b> This flag indicates out-of-bound motion vector delta SEs coded in the bit-stream.
	5	<b>Reference Index SE Error</b> This flag indicates out-of-bound Refidx SEs coded in the bit-stream.
	4	<b>Residual Error</b> This flag indicates out-of-bound absolute coefficient level SEs coded in the bit-stream.
	3	<b>Slice end Error</b> This flag indicates a pre-matured slice_end SE or inconsistent slice end on the last MB of a slice.
	2	<b>Chroma Intra prediction Mode Error</b> This flag indicates inconsistent Chroma Intra prediction mode SEs coded in the bit-stream.
	1	<b>Luma Intra prediction Mode Error</b> This flag indicates inconsistent luma Intra prediction mode SE coded in the bit-stream.
	0	<b>MB Concealment Flag</b> Each pulse from this flag indicates one MB is concealed by hardware.

## AVC CAVLC

AVC CAVLC		
DWord	Bit	Description
0	15	<b>Total Zero out-of-bound Error</b> This flag indicates the Total zero SE count exceed the max number of coeffs allowed in an intra16x16 AC block.
	14	<b>Coefficient level out-of-bound Error</b> This flag indicates the coded coefficient level SEs in the bit-stream is out-of-bound.
	13	<b>RunBefore out-of-bound Error</b> This flag indicates the coded RunBefore SE value is larger than the remaining zero block count.
	12	<b>Total coefficient Out-of-bound Error</b> This flag indicates the coded total coeff SE count exceed the max number of coeffs allowed in an intra16x16 AC block.
	11	<b>Temporal Direction Motion Vector Out-of-Bound Error</b> This flag indicates motion vectors calculated from Temporal Direct Motion Vector is larger than the allowed range specified by the AVC spec.
	10	<b>Reserved</b> Reserved
	9	<b>Motion Vector Delta SE Out-of-Bound Error</b> This flag indicates inconsistent Motion Vector Delta SEs coded in the bit-stream.
	8	<b>Reference Index SE Out-of-Bound Error</b> This flag indicates inconsistent Reference Index SEs coded in the bit-stream.
	7	<b>RunBefore/TotalZero Error</b> This flag indicates one or more inconsistent RunBefore or TotalZero SEs coded in the bit-stream.
	6	<b>Exponential Golomb Error</b> This flag indicates hardware detects more than 18 leadzero for skip and more than 19 for other SEs from the Exponential Golomb Logic
	5	<b>Total Coeff SE Error</b> This flag indicates one or more inconsistent total coeff SEs coded in the bit-stream.
	4	<b>Macroblock Coded Block Pattern Error</b> This flag indicates inconsistent CBP SEs coded in the bit-stream.
	3	<b>Mbtype/submbtype Error</b> This flag indicates inconsistent MBtype/SubMBtype SEs coded in the bit-stream.
	2	<b>Chroma Intra prediction Mode Error</b> This flag indicates inconsistent Chroma Intra prediction mode SEs coded in the bit-stream.
	1	<b>Luma Intra prediction Mode Error</b> This flag indicates inconsistent luma Intra prediction mode SE coded in the bit-stream.

## AVC CAVLC

0	<b>MB Concealment Flag</b> Each pulse from this flag indicates one MB is concealed by hardware.
---	--

## BCS Hardware-Detected Error Bit Definitions

BCS Hardware-Detected Error Bit Definitions							
DWord	Bit	Description					
0	15:3	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ			
Format:	MBZ						
2	<p><b>Command Privilege Violation Error</b></p> <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> </table> <p>This bit is set if a command classified as privileged is parsed in a non-privileged batch buffer. The command will be converted to a NOOP and parsing will continue.</p>	Project:	BDW				
Project:	BDW						
1	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ				
Format:	MBZ						
0	<p><b>Instruction Error</b></p> <p>This bit is set when the Renderer Instruction Parser detects an error while parsing an instruction. Instruction errors include:</p> <ul style="list-style-type: none"> <li>• Client ID value (Bits 31:29 of the Header) is not supported (only MI, 2D and 3D are supported).</li> <li>• Defeatured MI Instruction Opcodes:</li> </ul> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>1</td> <td></td> <td>Instruction Error detected</td> </tr> </tbody> </table> <p><b>Programming Notes</b></p> <p>This error indications cannot be cleared except by reset (i.e., it is a fatal error).</p>	Value	Name	Description	1		Instruction Error detected
Value	Name	Description					
1		Instruction Error detected					

## BINDING\_TABLE\_EDIT\_ENTRY

BINDING_TABLE_EDIT_ENTRY				
DWord	Bit	Description		
0	31:24	<b>Reserved</b> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ
Format:	MBZ			
23:16	<b>Binding Table Index</b> <table border="1"> <tr> <td>Format:</td> <td>U8</td> </tr> </table> <p>This field specifies the index of binding table entry that will be updated.</p>	Format:	U8	
Format:	U8			
15:0	<b>Surface State Pointer</b> <table border="1"> <tr> <td>Format:</td> <td>SurfaceStateOffset[21:6]RENDER_SURFACE_STATE [BDW]</td> </tr> </table> <p>Surface State Pointer. This address points to a surface state block. This pointer is relative to the Surface State Base Address.</p>	Format:	SurfaceStateOffset[21:6]RENDER_SURFACE_STATE [BDW]	
Format:	SurfaceStateOffset[21:6]RENDER_SURFACE_STATE [BDW]			

## BINDING\_TABLE\_STATE

<b>BINDING_TABLE_STATE</b>						
<b>DWord</b>	<b>Bit</b>	<b>Description</b>				
0	31:6	<p><b>Surface State Pointer</b></p> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>SurfaceStateOffset[31:6]</td></tr> </table> <p>This 64-byte aligned address points to a surface state block. This pointer is relative to the <b>Surface State Base Address</b>.</p>	Project:	BDW	Format:	SurfaceStateOffset[31:6]
Project:	BDW					
Format:	SurfaceStateOffset[31:6]					
	5:0	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	BDW	Format:	MBZ
Project:	BDW					
Format:	MBZ					

## Bit Definition for Interrupt Control Registers - Blitter

Bit Definition for Interrupt Control Registers - Blitter						
DWord	Bit	Description				
0	31:28	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table> <p>These bits may be assigned to interrupts on future products/steppings.</p>	Format:	MBZ		
Format:	MBZ					
	27	<p><b>Wait on Semaphore</b></p> <p>Exec-List Scheduling: Set when MI_SEMAPHORE_WAIT command is un-successful and when "Inhibit Synchronous Context Switch" is set. Scheduler can use this interrupt to preempt the context waiting on semaphore wait.</p>				
	26:25	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ		
Format:	MBZ					
	24	<p><b>Context Switch Interrupt</b></p> <p>Set when a context switch has just occurred. Exec-List Enable bit needs to be set for this interrupt to occur.</p>				
	23	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ		
Format:	MBZ					
	22	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	BDW	Format:	MBZ
Project:	BDW					
Format:	MBZ					
	21	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ		
Format:	MBZ					
	20	<p><b>MI_FLUSH_DW Notify Interrupt</b></p> <p>The Pipe Control packet (Fences) specified in 3D pipeline document may optionally generate an Interrupt. The Store QW associated with a fence is completed ahead of the interrupt.</p>				
	19	<p><b>Blitter Command Parser Master Error</b></p> <p>When this status bit is set, it indicates that the hardware has detected an error. It is set by the device upon an error condition and cleared by a CPU write of a one to the appropriate bit contained in the Error ID register followed by a write of a one to this bit in the IIR. Further information on the source of the error comes from the "Error Status Register" which along with the "Error Mask Register" determine which error conditions will cause the error status bit to be set and the interrupt to occur.</p> <p><b>Page Table Error:</b> Indicates a page table error.</p> <p><b>Instruction Parser Error:</b> The Blitter Instruction Parser encounters an error while parsing an instruction.</p>				

## Bit Definition for Interrupt Control Registers - Blitter

	18:17	<b>Reserved</b>	Format:	MBZ
	16	<b>Blitter Command Parser User Interrupt</b>	This status bit is set when an MI_USER_INTERRUPT instruction is executed on the Blitter Command Parser. Note that instruction execution is not halted and proceeds normally. A mechanism such as an MI_STORE_DATA instruction is required to associate a particular meaning to a user interrupt.	
	15:0	<b>Reserved</b>	Format:	MBZ

## Bit Definition for Interrupt Control Registers - Media#1

Bit Definition for Interrupt Control Registers - Media#1				
DWord	Bit	Description		
0	31:16	<b>Reserved</b> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ
Format:	MBZ			
	15:12	<b>Reserved</b> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table> <p>These bits may be assigned to interrupts on future products/steppings.</p>	Format:	MBZ
Format:	MBZ			
	11	<b>Wait on Semaphore</b> Exec-List Scheduling: Set when MI_SEMAPHORE_WAIT command is un-successful and when "Inhibit Synchronous Context Switch" is set. Scheduler can use this interrupt to preempt the context waiting on semaphore wait.		
	10	<b>Reserved</b> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ
Format:	MBZ			
	9	<b>Reserved</b>		
	8	<b>Context Switch Interrupt</b> Set when a context switch has just occurred. <b>Exelist Enable bit</b> needs to be set for this interrupt to occur.		
	7	<b>Reserved</b> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ
Format:	MBZ			
	6	<b>Timeout Counter Expired</b> Set when the VCS timeout counter has reached the timeout thresh-hold value.		
	5	<b>Reserved</b>		
	4	<b>MI_FLUSH_DW Notify Interrupt</b> The Pipe Control packet (Fences) specified in 3D pipeline document may optionally generate an Interrupt. The Store QW associated with a fence is completed ahead of the interrupt.		
	3	<b>Video Command Parser Master Error</b> When this status bit is set, it indicates that the hardware has detected an error. It is set by the device upon an error condition and cleared by a CPU write of a one to the appropriate bit contained in the Error ID register followed by a write of a one to this bit in the IIR. Further information on the source of the error comes from the "Error Status Register" which along with the "Error Mask Register" determine which error conditions will cause the error status bit to be set and the interrupt to occur. <b>Page Table Error:</b> Indicates a page table error. <b>Instruction Parser Error:</b> The Blitter Instruction Parser encounters an error while parsing an instruction.		

## Bit Definition for Interrupt Control Registers - Media#1

	2:1	<b>Reserved</b> Format:	MBZ
	0	<b>Video Command Parser User Interrupt</b> This status bit is set when an MI_USER_INTERRUPT instruction is executed on the Video Command Parser. Note that instruction execution is not halted and proceeds normally. A mechanism such as an MI_STORE_DATA instruction is required to associate a particular meaning to a user interrupt.	

## Bit Definition for Interrupt Control Registers - Media#2

Bit Definition for Interrupt Control Registers - Media#2				
DWord	Bit	Description		
0	31:28	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table> <p>These bits may be assigned to interrupts on future products/steppings.</p>	Format:	MBZ
Format:	MBZ			
	27	<p><b>Wait on Semaphore</b></p> <p>Exec-List Scheduling: Set when MI_SEMAPHORE_WAIT command is un-successful and when "Inhibit Synchronous Context Switch" is set. Scheduler can use this interrupt to preempt the context waiting on semaphore wait.</p>		
	26	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ
Format:	MBZ			
	25	<p><b>Reserved</b></p>		
	24	<p><b>Context Switch Interrupt</b></p> <p>Set when a context switch has just occurred. <b>Exelist Enable bit</b> needs to be set for this interrupt to occur.</p>		
	23	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ
Format:	MBZ			
	22	<p><b>Timeout Counter Expired</b></p> <p>Set when the VCS timeout counter has reached the timeout thresh-hold value.</p>		
	21	<p><b>Reserved</b></p>		
	20	<p><b>MI_FLUSH_DW Notify Interrupt</b></p> <p>The Pipe Control packet (Fences) specified in 3D pipeline document may optionally generate an Interrupt. The Store QW associated with a fence is completed ahead of the interrupt.</p>		
	19	<p><b>Video Command Parser Master Error</b></p> <p>When this status bit is set, it indicates that the hardware has detected an error. It is set by the device upon an error condition and cleared by a CPU write of a one to the appropriate bit contained in the Error ID register followed by a write of a one to this bit in the IIR. Further information on the source of the error comes from the "Error Status Register" which along with the "Error Mask Register" determine which error conditions will cause the error status bit to be set and the interrupt to occur.</p> <p><b>Page Table Error:</b> Indicates a page table error.</p> <p><b>Instruction Parser Error:</b> The Blitter Instruction Parser encounters an error while parsing an instruction.</p>		
	18:17	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ
Format:	MBZ			

## Bit Definition for Interrupt Control Registers - Media#2

	16	<b>Video Command Parser User Interrupt</b> This status bit is set when an MI_USER_INTERRUPT instruction is executed on the Video Command Parser. Note that instruction execution is not halted and proceeds normally. A mechanism such as an MI_STORE_DATA instruction is required to associate a particular meaning to a user interrupt.
	15:0	<b>Reserved</b> Format: <span style="border: 1px solid black; padding: 2px;"> </span> MBZ

## Bit Definition for Interrupt Control Registers - Render

Bit Definition for Interrupt Control Registers - Render								
DWord	Bit	Description						
0	31:16	<b>Reserved</b> <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table> <p>Reserved for other command streamers - cannot be allocated by main command streamer.</p>	Project:	BDW	Format:	MBZ		
Project:	BDW							
Format:	MBZ							
	15:12	<b>Reserved</b> <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	BDW	Format:	MBZ		
Project:	BDW							
Format:	MBZ							
	11	<b>Wait on Semaphore</b> <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> </table> <p>Exec-List Scheduling: Set when MI_SEMAPHORE_WAIT command is un-successful and when "Inhibit Synchronous Context Switch" is set. Scheduler can use this interrupt to preempt the context waiting on semaphore wait.</p>	Project:	BDW				
Project:	BDW							
	10	<b>L3 Counter Save Interrupt</b> <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> </table>	Project:	BDW				
Project:	BDW							
	9	<b>Reserved</b> <table border="1"> <tr> <td>Project:</td> <td>BDWx6</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	BDWx6	Format:	MBZ		
Project:	BDWx6							
Format:	MBZ							
	8	<b>Context Switch Interrupt</b> <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> </table> <p>Set when a context switch has just occurred. Execlist Enable bit needs to be set for this interrupt to occur.</p>	Project:	BDW				
Project:	BDW							
	7	<b>Page Fault</b> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <th>Description</th><th>Project</th></tr> <tr> <td>This interrupt is for handling Legacy Page Fault interface for all Command Streamers (BCS, RCS, VCS, VECS). When Fault Repair Mode is enabled, Interrupt mask register value is not looked at to generate interrupt due to page fault. Please refer to vol1c "Page Fault Support" section for more details.</td><td>BDW</td> </tr> </table>	Project:	All	Description	Project	This interrupt is for handling Legacy Page Fault interface for all Command Streamers (BCS, RCS, VCS, VECS). When Fault Repair Mode is enabled, Interrupt mask register value is not looked at to generate interrupt due to page fault. Please refer to vol1c "Page Fault Support" section for more details.	BDW
Project:	All							
Description	Project							
This interrupt is for handling Legacy Page Fault interface for all Command Streamers (BCS, RCS, VCS, VECS). When Fault Repair Mode is enabled, Interrupt mask register value is not looked at to generate interrupt due to page fault. Please refer to vol1c "Page Fault Support" section for more details.	BDW							
	6	<b>Timeout Counter Expired</b> <p>Set when the render pipe timeout counter (0x02190) has reached the timeout threshold value (0x0217c).</p>						

## Bit Definition for Interrupt Control Registers - Render

	5	<b>L3 Parity Error (Slice0)</b>				
		<table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> </table> <p>When this bit is set, L3 cache controller is indicating that it has encountered an parity error while checking the data.</p>	Project:	BDW		
Project:	BDW					
<b>PIPE_CONTROL Notify Interrupt</b>						
	4	The Pipe Control packet (Fences) specified in 3D pipeline document may optionally generate an Interrupt. The Store QW associated with a fence is completed ahead of the interrupt.				
<b>Render Command Parser Master Error</b>						
	3	<p>When this status bit is set, it indicates that the hardware has detected an error. It is set by the device upon an error condition and cleared by a CPU write of a one to the appropriate bit contained in the Error ID register followed by a write of a one to this bit in the IIR. Further information on the source of the error comes from the "Error Status Register" which along with the "Error Mask Register" determine which error conditions will cause the error status bit to be set and the interrupt to occur.</p> <p><b>Page Table Error:</b> Indicates a page table error.</p> <p><b>Instruction Parser Error:</b> The Render Instruction Parser encounters an error while parsing an instruction.</p>				
	2	<b>Reserved</b>				
		<table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	BDW	Format:	MBZ
Project:	BDW					
Format:	MBZ					
	1	<b>Reserved</b>				
	0	<b>Render Command Parser User Interrupt</b>				
		This status bit is set when an MI_USER_INTERRUPT instruction is executed on the Render Command Parser. Note that instruction execution is not halted and proceeds normally. A mechanism such as an MI_STORE_DATA instruction is required to associate a particular meaning to a user interrupt.				

## Bit Definition for Interrupt Control Registers - Video Enhancement

Bit Definition for Interrupt Control Registers - Video Enhancement						
DWord	Bit	Description				
0	31:12	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table> <p>These bits may be assigned to interrupts on future products/steppings.</p>	Format:	MBZ		
Format:	MBZ					
	11	<p><b>Wait on Semaphore</b></p> <p>Exec-List Scheduling: Set when MI_SEMAPHORE_WAIT command is un-successful and when "Inhibit Synchronous Context Switch" is set. Scheduler can use this interrupt to preempt the context waiting on semaphore wait.</p>				
	10	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ		
Format:	MBZ					
	9	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ		
Format:	MBZ					
	8	<p><b>Context Switch Interrupt</b></p> <p>Set when a context switch has just occurred. Exec-List Enable bit needs to be set for this interrupt to occur.</p>				
	7	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ		
Format:	MBZ					
	6	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	BDW	Format:	MBZ
Project:	BDW					
Format:	MBZ					
	5	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ		
Format:	MBZ					
	4	<p><b>MI_FLUSH_DW Notify Interrupt</b></p> <p>The Pipe Control packet (Fences) specified in 3D pipeline document may optionally generate an interrupt. The Store QW associated with a fence is completed ahead of the interrupt.</p>				

## Bit Definition for Interrupt Control Registers - Video Enhancement

	3	<b>Video Enhancement Command Parser Master Error</b> When this status bit is set, it indicates that the hardware has detected an error. It is set by the device upon an error condition and cleared by a CPU write of a one to the appropriate bit contained in the Error ID register followed by a write of a one to this bit in the IIR. Further information on the source of the error comes from the "Error Status Register" which along with the "Error Mask Register" determine which error conditions will cause the error status bit to be set and the interrupt to occur. <b>Page Table Error:</b> Indicates a page table error. <b>Instruction Parser Error:</b> The Blitter Instruction Parser encounters an error while parsing an instruction.		
	2:1	<b>Reserved</b> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ
Format:	MBZ			
	0	<b>Video Enhancement Command Parser User Interrupt</b> This status bit is set when an MI_USER_INTERRUPT instruction is executed on the Video Enhancement Command Parser. Note that instruction execution is not halted and proceeds normally. A mechanism such as an MI_STORE_DATA instruction is required to associate a particular meaning to a user interrupt.		

## Black Level Correction State - DW75..76

Black Level Correction State - DW75..76							
DWord	Bit	Description					
0	31:13	<b>Reserved</b> <table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ			
Format:	MBZ						
12:0	<b>Black Point Offset R</b> <table border="1"> <tr> <td>Default Value:</td><td>0</td></tr> <tr> <td>Format:</td><td>S12 2's complement</td></tr> <tr> <td colspan="2">Offset in for Y/R.</td></tr> </table>	Default Value:	0	Format:	S12 2's complement	Offset in for Y/R.	
Default Value:	0						
Format:	S12 2's complement						
Offset in for Y/R.							
1	31:26	<b>Reserved</b> <table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ			
Format:	MBZ						
25:13	<b>Black Point Offset G</b> <table border="1"> <tr> <td>Default Value:</td><td>0</td></tr> <tr> <td>Format:</td><td>S12 2's complement</td></tr> <tr> <td colspan="2">Offset in for U/G.</td></tr> </table>	Default Value:	0	Format:	S12 2's complement	Offset in for U/G.	
Default Value:	0						
Format:	S12 2's complement						
Offset in for U/G.							
12:0	<b>Black Point Offset B</b> <table border="1"> <tr> <td>Default Value:</td><td>0</td></tr> <tr> <td>Format:</td><td>S12 2's complement</td></tr> <tr> <td colspan="2">Offset in for V/B.</td></tr> </table>	Default Value:	0	Format:	S12 2's complement	Offset in for V/B.	
Default Value:	0						
Format:	S12 2's complement						
Offset in for V/B.							

## BLEND\_STATE

BLEND_STATE						
Project:	BDW					
Size (in bits):	544					
Default Value:	0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000					
<p>The blend state is stored as a structure containing a common DWORD that applies to all RTs and an array of up to 8 elements, each of which contains the two DWORDs for each. The start of each element is spaced 2 DWORDs apart. The blend state is aligned to a 64-byte boundary, which is pointed to by a field in 3DSTATE_BLEND_STATE_POINTERS. The 3-bit Render Target Index field in the Render Target Write data port message header is used to select which of the 8 elements from BLEND_STATE that is used on the current message.</p>						
DWord	Bit	Description				
0	31	<p><b>Alpha To Coverage Enable</b></p> <table border="1"> <tr> <td>Format:</td><td>Enable</td></tr> <tr> <td colspan="2">If set, Source0 Alpha is converted to a temporary 1/2/4-bit coverage mask and the mask bit corresponding to the sample# ANDed with the sample mask bit. If set, sample coverage is computed based on src0 alpha value. Value of 0 disables all samples and value of 1 enables all samples for that pixel. The same coverage needs to apply to all the RTs in MRT case. Further, any value of src0 alpha between 0 and 1 monotonically increases the number of enabled pixels. The field is applied to all the RTs in MRT case.</td></tr> </table>	Format:	Enable	If set, Source0 Alpha is converted to a temporary 1/2/4-bit coverage mask and the mask bit corresponding to the sample# ANDed with the sample mask bit. If set, sample coverage is computed based on src0 alpha value. Value of 0 disables all samples and value of 1 enables all samples for that pixel. The same coverage needs to apply to all the RTs in MRT case. Further, any value of src0 alpha between 0 and 1 monotonically increases the number of enabled pixels. The field is applied to all the RTs in MRT case.	
Format:	Enable					
If set, Source0 Alpha is converted to a temporary 1/2/4-bit coverage mask and the mask bit corresponding to the sample# ANDed with the sample mask bit. If set, sample coverage is computed based on src0 alpha value. Value of 0 disables all samples and value of 1 enables all samples for that pixel. The same coverage needs to apply to all the RTs in MRT case. Further, any value of src0 alpha between 0 and 1 monotonically increases the number of enabled pixels. The field is applied to all the RTs in MRT case.						
30	<p><b>Independent Alpha Blend Enable</b></p> <table border="1"> <tr> <td>Format:</td><td>Enable</td></tr> <tr> <td colspan="2">When enabled, the other fields in this instruction control the combination of the alpha components in the Color Buffer Blend stage. When disabled, the alpha components are combined in the same fashion as the color components. The field is applied to all the RTs in MRT case.</td></tr> </table>	Format:	Enable	When enabled, the other fields in this instruction control the combination of the alpha components in the Color Buffer Blend stage. When disabled, the alpha components are combined in the same fashion as the color components. The field is applied to all the RTs in MRT case.		
Format:	Enable					
When enabled, the other fields in this instruction control the combination of the alpha components in the Color Buffer Blend stage. When disabled, the alpha components are combined in the same fashion as the color components. The field is applied to all the RTs in MRT case.						
29	<p><b>Alpha To One Enable</b></p> <table border="1"> <tr> <td>Format:</td><td>Enable</td></tr> <tr> <td colspan="2">If set, Source0 Alpha is set to 1.0f after (possibly) being used to generate the AlphaToCoverage coverage mask. If Dual Source Blending is enabled, this bit must be disabled. The field is applied to all the RTs in MRT case.</td></tr> </table>	Format:	Enable	If set, Source0 Alpha is set to 1.0f after (possibly) being used to generate the AlphaToCoverage coverage mask. If Dual Source Blending is enabled, this bit must be disabled. The field is applied to all the RTs in MRT case.		
Format:	Enable					
If set, Source0 Alpha is set to 1.0f after (possibly) being used to generate the AlphaToCoverage coverage mask. If Dual Source Blending is enabled, this bit must be disabled. The field is applied to all the RTs in MRT case.						
28	<p><b>Alpha To Coverage Dither Enable</b></p> <table border="1"> <tr> <td>Format:</td><td>Enable</td></tr> <tr> <td colspan="2">If set, sample coverage is computed based on src0 alpha value and it modulates the sample coverage based on screen coordinates. Value of 0 disables all samples and value of 1 enables all samples for that pixel. The same coverage needs to apply to all the RTs in MRT case. Further, any value of src0 alpha between 0 and 1 monotonically increases the number of enabled pixels. If AlphaToCoverage is disabled, AlphaToCoverage Dither does not have any impact. The field is applied to all the RTs in MRT case.</td></tr> </table>	Format:	Enable	If set, sample coverage is computed based on src0 alpha value and it modulates the sample coverage based on screen coordinates. Value of 0 disables all samples and value of 1 enables all samples for that pixel. The same coverage needs to apply to all the RTs in MRT case. Further, any value of src0 alpha between 0 and 1 monotonically increases the number of enabled pixels. If AlphaToCoverage is disabled, AlphaToCoverage Dither does not have any impact. The field is applied to all the RTs in MRT case.		
Format:	Enable					
If set, sample coverage is computed based on src0 alpha value and it modulates the sample coverage based on screen coordinates. Value of 0 disables all samples and value of 1 enables all samples for that pixel. The same coverage needs to apply to all the RTs in MRT case. Further, any value of src0 alpha between 0 and 1 monotonically increases the number of enabled pixels. If AlphaToCoverage is disabled, AlphaToCoverage Dither does not have any impact. The field is applied to all the RTs in MRT case.						

BLEND_STATE		
27	<b>Alpha Test Enable</b>	<p>Format: <input type="text"/> Enable</p> <p>Enables the AlphaTest function of the Pixel Processing pipeline. The field is applied to all the RTs in MRT case.</p>
		<b>Programming Notes</b>
		Alpha Test can only be enabled if Pixel Shader outputs a float alpha value. Alpha Test is applied independently on each render target by comparing that render target's alpha value against the alpha reference value. If the alpha test fails, the corresponding pixel write will be suppressed only for that render target. The depth/stencil update will occur if alpha test passes for any render target.
26:24	<b>Alpha Test Function</b>	<p>Format: <input type="text"/> <b>3D_Compare_Function</b></p> <p>This field specifies the comparison function used in the AlphaTest function. The field is applied to all the RTs in MRT case.</p>
23	<b>Color Dither Enable</b>	<p>Format: <input type="text"/> Enable</p> <p>Enables dithering of colors (including any alpha component) before they are written to the Color Buffer. The field is applied to all the RTs in MRT case.</p>
		<b>Programming Notes</b>
		For YUV render target formats, this field must be programmed to 0.
22:21	<b>X Dither Offset</b>	<p>Format: <input type="text"/> U2</p> <p>Specifies offset to apply to pixel X coordinate LSBs when accessing dither table. The field is applied to all the RTs in MRT case.</p>
20:19	<b>Y Dither Offset</b>	<p>Format: <input type="text"/> U2</p> <p>Specifies offset to apply to pixel Y coordinate LSBs when accessing dither table. The field is applied to all the RTs in MRT case.</p>
18:0	<b>Reserved</b>	<p>Format: <input type="text"/> MBZ</p>
1..16	63:0	<b>Entry</b>
		<p>Format: <input type="text"/> <b>BLEND_STATE_ENTRY</b></p>

## BLEND\_STATE\_ENTRY

BLEND_STATE_ENTRY											
DWord	Bit	Description									
0..1	63	<p><b>Logic Op Enable</b></p> <table border="1"> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>Enables the LogicOp function of the Pixel Processing pipeline.</p> <p><b>Programming Notes</b></p> <p>Enabling LogicOp and Color Buffer Blending at the same time is UNDEFINED</p>	Format:	Enable							
Format:	Enable										
	62:59	<p><b>Logic Op Function</b></p> <table border="1"> <tr> <td>Format:</td> <td>3D.Logic.Op.Function</td> </tr> </table> <p>This field specifies the function to be performed (when enabled) in the Logic Op stage of the Pixel Processing pipeline. Note that the encoding of this field is one less than the corresponding "R2_" ROP code defined in WINGDI.H, and is a rather contorted mapping of the OpenGL LogicOp encodings. However, this field was defined such that, when the 4 bits are replicated to 8 bits, they coincide with the ROP codes used in the Blter. Note: if the Logic Op Function does not depend on "D", the dest buffer is not read.</p>	Format:	3D.Logic.Op.Function							
Format:	3D.Logic.Op.Function										
	58:37	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ							
Format:	MBZ										
	36	<p><b>Pre-Blend Source Only Clamp Enable</b></p> <p>This field specifies whether the source(s) are clamped prior to blending, regardless of whether blending is enabled. If DISABLED, no clamping is performed prior to blending. If ENABLED, only source0 and source 1, if dual source is enabled, are clamped prior to the blend to the range specified by Color Clamp Range.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Disabled</td> <td>No clamping is performed prior to blending.</td> </tr> <tr> <td>1</td> <td>Enabled</td> <td>Only Source(s) are clamped prior to blend function. Other inputs to blend must not be clamped.</td> </tr> </tbody> </table> <p><b>Programming Notes</b></p> <p>See table in Pre-Blending Color Clamp subsection for programming restrictions as a function of RT format. This field is ignored (treated as DISABLED) for UINT and SINT RT surface formats. Blending is not supported for those RT surface formats. <b>When this bit is enabled Pre-Blend Color Clamp Enable RT[0] must be disabled.</b></p>	Value	Name	Description	0	Disabled	No clamping is performed prior to blending.	1	Enabled	Only Source(s) are clamped prior to blend function. Other inputs to blend must not be clamped.
Value	Name	Description									
0	Disabled	No clamping is performed prior to blending.									
1	Enabled	Only Source(s) are clamped prior to blend function. Other inputs to blend must not be clamped.									

BLEND_STATE_ENTRY																	
	35:34	<p><b>Color Clamp Range</b>  Specifies the clamped range used in Pre-Blend and Post-Blend Color Clamp functions if one or both of those functions are enabled. Note that this range selection is shared between those functions. This field is ignored if both of the Color Clamp Enables are disabled</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0</td><td>COLORCLAMP_UNORM</td><td>Clamp Range [0,1]</td></tr> <tr> <td>1</td><td>COLORCLAMP_SNORM</td><td>Clamp Range [-1,1]</td></tr> <tr> <td>2</td><td>COLORCLAMP_RTFORMAT</td><td>Clamp to the range of the RT surface format (Note: The Alpha component is clamped to FLOAT16 for R11G11B10_FLOAT format).</td></tr> <tr> <td>3</td><td>Reserved</td><td>Reserved</td></tr> </tbody> </table>	Value	Name	Description	0	COLORCLAMP_UNORM	Clamp Range [0,1]	1	COLORCLAMP_SNORM	Clamp Range [-1,1]	2	COLORCLAMP_RTFORMAT	Clamp to the range of the RT surface format (Note: The Alpha component is clamped to FLOAT16 for R11G11B10_FLOAT format).	3	Reserved	Reserved
Value	Name	Description															
0	COLORCLAMP_UNORM	Clamp Range [0,1]															
1	COLORCLAMP_SNORM	Clamp Range [-1,1]															
2	COLORCLAMP_RTFORMAT	Clamp to the range of the RT surface format (Note: The Alpha component is clamped to FLOAT16 for R11G11B10_FLOAT format).															
3	Reserved	Reserved															
	33	<p><b>Pre-Blend Color Clamp Enable</b></p> <table border="1"> <tr> <td>Format:</td><td>Enable</td></tr> </table> <p>This field specifies whether the source, destination and constant color channels are clamped prior to blending, regardless of whether blending is enabled. If DISABLED, no clamping is performed prior to blending. If ENABLED, all inputs to the blend function are clamped prior to the blend to the range specified by Color Clamp Range.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0</td><td>Disabled</td><td>No clamping is performed prior to blending.</td></tr> <tr> <td>1</td><td>Enabled</td><td>All inputs to the blend function are clamped prior to the blend to the range specified by Color Clamp Range.</td></tr> </tbody> </table> <p><b>Programming Notes</b></p> <p>See table in Pre-Blending Color Clamp subsection for programming restrictions as a function of RT format. This field is ignored (treated as DISABLED) for UINT and SINT RT surface formats. Blending is not supported for those RT surface formats. The device will automatically clamp source color channels to the respective RT surface range.</p>	Format:	Enable	Value	Name	Description	0	Disabled	No clamping is performed prior to blending.	1	Enabled	All inputs to the blend function are clamped prior to the blend to the range specified by Color Clamp Range.				
Format:	Enable																
Value	Name	Description															
0	Disabled	No clamping is performed prior to blending.															
1	Enabled	All inputs to the blend function are clamped prior to the blend to the range specified by Color Clamp Range.															
	32	<p><b>Post-Blend Color Clamp Enable</b></p> <table border="1"> <tr> <td>Format:</td><td>Enable</td></tr> </table> <p>If blending is enabled, this field specifies whether the blending output channels are first clamped to the range specified by Color Clamp Range. Regardless of whether this clamping is enabled, the blending output channels will be clamped to the RT surface format just prior to being written.</p> <p><b>Programming Notes</b></p> <p>See table in Pre-Blending Color Clamp subsection for programming restrictions as a function of RT format. This field is ignored (treated as DISABLED) for UINT and SINT RT surface formats. Blending is not supported for those RT surface formats. The device will automatically clamp source color channels to the respective RT surface range. <b>When this bit is enabled Pre-Blend Source Only Clamp Enable RT[0] must be disabled.</b></p>	Format:	Enable													
Format:	Enable																

<b>BLEND_STATE_ENTRY</b>		
31	<b>Color Buffer Blend Enable</b>	
	Format:	Enable
	Enables the ColorBufferBlending (nee "alpha blending") function of the Pixel Processing Pipeline for this render target.	
	<b>Programming Notes</b>	
	Enabling LogicOp and ColorBufferBlending at the same time is UNDEFINED	
30:26	<b>Source Blend Factor</b>	
	Format:	<b>3D_Color_Buffer_Blend_Factor</b>
	Controls the "source factor" in the ColorBufferBlending function. Refer to Source Alpha Blend Factor for encodings.	
25:21	<b>Destination Blend Factor</b>	
	Format:	<b>3D_Color_Buffer_Blend_Factor</b>
	Controls the "destination factor" in the ColorBufferBlending function. Refer to Source Alpha Blend Factor for encodings.	
20:18	<b>Color Blend Function</b>	
	Format:	<b>3D_Color_Buffer_Blend_Function</b>
	This field specifies the function used to combine the color components in the ColorBufferBlending function of the Pixel Processing Pipeline. If Independent Alpha Blend Enable is disabled, this field will also control the blending of the alpha components in the ColorBufferBlending function.	
17:13	<b>Source Alpha Blend Factor</b>	
	Format:	<b>3D_Color_Buffer_Blend_Factor</b>
	Controls the "source factor" in alpha Color Buffer Blending stage. Note: For the source/destination alpha blend factors, the encodings indicating "COLOR" are the same as the encodings indicating "ALPHA", as the alpha component of the color is selected.	
12:8	<b>Destination Alpha Blend Factor</b>	
	Format:	<b>3D_Color_Buffer_Blend_Factor</b>
	Controls the "destination factor" in alpha Color Buffer Blending stage. Refer to Source Alpha Blend Factor for encodings.	
7:5	<b>Alpha Blend Function</b>	
	Format:	<b>3D_Color_Buffer_Blend_Function</b>
	This field specifies the function used to combine the alpha components in the Color Buffer blend stage of the Pixel Pipeline when the IndependentAlphaBlend state is enabled.	
4	<b>Reserved</b>	
	Format:	MBZ

BLEND_STATE_ENTRY													
	3	<b>Write Disable Alpha</b>											
		<table border="1"> <tr> <td>Format:</td><td>Disable</td><td></td></tr> </table>			Format:	Disable							
Format:	Disable												
		This field controls the writing of the alpha component into the Render Target.											
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Enabled</td><td>Alpha component can be overwritten</td></tr> <tr> <td>1b</td><td>Disabled</td><td>Writes to the color buffer will not modify Alpha.</td></tr> </tbody> </table>			Value	Name	Description	0b	Enabled	Alpha component can be overwritten	1b	Disabled	Writes to the color buffer will not modify Alpha.
Value	Name	Description											
0b	Enabled	Alpha component can be overwritten											
1b	Disabled	Writes to the color buffer will not modify Alpha.											
		<b>Programming Notes</b>											
		For YUV surfaces, this field must be set to 0B (enabled).											
	2	<b>Write Disable Red</b>											
		<table border="1"> <tr> <td>Format:</td><td>Disable</td><td></td></tr> </table>			Format:	Disable							
Format:	Disable												
		This field controls the writing of the red component into the Render Target.											
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Enabled</td><td>Red component can be overwritten</td></tr> <tr> <td>1b</td><td>Disabled</td><td>Writes to the color buffer will not modify Red.</td></tr> </tbody> </table>			Value	Name	Description	0b	Enabled	Red component can be overwritten	1b	Disabled	Writes to the color buffer will not modify Red.
Value	Name	Description											
0b	Enabled	Red component can be overwritten											
1b	Disabled	Writes to the color buffer will not modify Red.											
		<b>Programming Notes</b>											
		For YUV surfaces, this field must be set to 0B (enabled).											
	1	<b>Write Disable Green</b>											
		<table border="1"> <tr> <td>Format:</td><td>Disable</td><td></td></tr> </table>			Format:	Disable							
Format:	Disable												
		This field controls the writing of the green component into the Render Target.											
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Enabled</td><td>Green component can be overwritten</td></tr> <tr> <td>1b</td><td>Disabled</td><td>Writes to the color buffer will not modify Green.</td></tr> </tbody> </table>			Value	Name	Description	0b	Enabled	Green component can be overwritten	1b	Disabled	Writes to the color buffer will not modify Green.
Value	Name	Description											
0b	Enabled	Green component can be overwritten											
1b	Disabled	Writes to the color buffer will not modify Green.											
		<b>Programming Notes</b>											
		For YUV surfaces, this field must be set to 0B (enabled).											
	0	<b>Write Disable Blue</b>											
		<table border="1"> <tr> <td>Format:</td><td>Disable</td><td></td></tr> </table>			Format:	Disable							
Format:	Disable												
		This field controls the writing of the Blue component into the Render Target.											
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Enabled</td><td>Blue component can be overwritten</td></tr> <tr> <td>1b</td><td>Disabled</td><td>Writes to the color buffer will not modify Blue.</td></tr> </tbody> </table>			Value	Name	Description	0b	Enabled	Blue component can be overwritten	1b	Disabled	Writes to the color buffer will not modify Blue.
Value	Name	Description											
0b	Enabled	Blue component can be overwritten											
1b	Disabled	Writes to the color buffer will not modify Blue.											
		<b>Programming Notes</b>											
		For YUV surfaces, this field must be set to 0B (enabled).											

## Block Dimensions Message Header Control

MHC_BDIM - Block Dimensions Message Header Control																					
DWord	Bit	Description																			
0	31:22	<b>Reserved</b> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Ignore</td> </tr> <tr> <td colspan="2">Ignored</td></tr> </table>	Project:	All	Format:	Ignore	Ignored														
Project:	All																				
Format:	Ignore																				
Ignored																					
	21:20	<b>Block Height</b> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Enumeration</td> </tr> </table> <p>Height in rows of block being accessed. Range = [0,3] representing 1 to 8 rows.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>H1</td> <td>Block height = 1 row</td> </tr> <tr> <td>1h</td> <td>H2</td> <td>Block height = 2 rows</td> </tr> <tr> <td>2h</td> <td>H4</td> <td>Block height = 4 rows</td> </tr> <tr> <td>03h</td> <td>H8</td> <td>Block height = 8 rows</td> </tr> </tbody> </table>	Project:	All	Format:	Enumeration	Value	Name	Description	0h	H1	Block height = 1 row	1h	H2	Block height = 2 rows	2h	H4	Block height = 4 rows	03h	H8	Block height = 8 rows
Project:	All																				
Format:	Enumeration																				
Value	Name	Description																			
0h	H1	Block height = 1 row																			
1h	H2	Block height = 2 rows																			
2h	H4	Block height = 4 rows																			
03h	H8	Block height = 8 rows																			
	19:2	<b>Reserved</b> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Ignore</td> </tr> <tr> <td colspan="2">Ignored</td></tr> </table>	Project:	All	Format:	Ignore	Ignored														
Project:	All																				
Format:	Ignore																				
Ignored																					
	1:0	<b>Block Width</b> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Enumeration</td> </tr> </table> <p>Width in Dwords of block being accessed. Range = [0,3] representing 1 to 8 Dwords.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>W1</td> <td>Block width = 1 Dword</td> </tr> <tr> <td>1h</td> <td>W2</td> <td>Block width = 2 Dwords</td> </tr> <tr> <td>2h</td> <td>W4</td> <td>Block width = 4 Dwords</td> </tr> <tr> <td>03h</td> <td>W8</td> <td>Block width = 8 Dwords</td> </tr> </tbody> </table>	Project:	All	Format:	Enumeration	Value	Name	Description	0h	W1	Block width = 1 Dword	1h	W2	Block width = 2 Dwords	2h	W4	Block width = 4 Dwords	03h	W8	Block width = 8 Dwords
Project:	All																				
Format:	Enumeration																				
Value	Name	Description																			
0h	W1	Block width = 1 Dword																			
1h	W2	Block width = 2 Dwords																			
2h	W4	Block width = 4 Dwords																			
03h	W8	Block width = 8 Dwords																			

## Block Message Header

MH_BTS_GO - Block Message Header		
DWord	Bit	Description
0-1	63:0	<b>Reserved</b>
		Project:
		Format:
		Ignored
2	31:0	<b>Global Offset</b>
		Project:
		Format:
		Specifies the global element index into the buffer, in units of Owords, Dwords, or Bytes (depending on the message).
		<b>Programming Notes</b>
		The Global Offset for Oword Unaligned Block operations is specified as a Dword-aligned byte offset (offset bits [1:0] = 0).
		If the address offset calculated with the Global Offset is greater than the Surface Size, then the access is Out-of-Bounds.
3-7	159:0	<b>Reserved</b>
		Project:
		Format:
		Ignored

## BR00 - BLT Opcode and Control

BR00 - BLT Opcode and Control										
DWord	Bit	Description								
0	31	<p><b>BLT Engine Busy</b> This bit indicates whether the BLT Engine is busy (1) or idle (0). This bit is replicated in the SETUP BLT Opcode and Control register.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0</td><td>Idle <b>[Default]</b></td></tr> <tr> <td>1</td><td>Busy</td></tr> </tbody> </table>	Value	Name	0	Idle <b>[Default]</b>	1	Busy		
Value	Name									
0	Idle <b>[Default]</b>									
1	Busy									
	30	<p><b>Setup Instruction Instruction</b></p> <table border="1"> <tr> <td>Default Value:</td><td>0</td></tr> </table> <p>The current instruction performs clipping (1).</p>	Default Value:	0						
Default Value:	0									
	29	<p><b>Setup Monochrome Pattern</b> This bit is decoded from the Setup instruction opcode to identify whether a color (0) or monochrome (1) pattern is used with the SCANLINE_BLT instruction.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0</td><td>Color <b>[Default]</b></td></tr> <tr> <td>1</td><td>Monochrome</td></tr> </tbody> </table>	Value	Name	0	Color <b>[Default]</b>	1	Monochrome		
Value	Name									
0	Color <b>[Default]</b>									
1	Monochrome									
	28:22	<p><b>Instruction Target (Opcode)</b></p> <table border="1"> <tr> <td>Default Value:</td><td>0000000b</td></tr> </table> <p>This is the contents of the Instruction Target field from the last BLT instruction. This field is used by the BLT Engine state machine to identify the BLT instruction it is to perform. The opcode specifies whether the source and pattern operands are color or monochrome.</p>	Default Value:	0000000b						
Default Value:	0000000b									
	21:20	<p><b>32bpp Byte Mask</b> This field is only used for 32bpp.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>00b</td><td><b>[Default]</b></td></tr> <tr> <td>1xb</td><td>Write Alpha Channel</td></tr> <tr> <td>x1b</td><td>Write RGB Channel</td></tr> </tbody> </table>	Value	Name	00b	<b>[Default]</b>	1xb	Write Alpha Channel	x1b	Write RGB Channel
Value	Name									
00b	<b>[Default]</b>									
1xb	Write Alpha Channel									
x1b	Write RGB Channel									
	19:17	<p><b>Monochrome Source Start</b></p> <table border="1"> <tr> <td>Default Value:</td><td>000b</td></tr> </table> <p>This field indicates the starting monochrome pixel bit position within a byte per scan line of the source operand. The monochrome source is word aligned which means that at the end of the scan line all bits should be discarded until the next word boundary.</p>	Default Value:	000b						
Default Value:	000b									

## BR00 - BLT Opcode and Control

	16	<b>Bit/Byte Packed</b> Byte packed is for the NT driver.			
			<b>Value</b>		
			<b>Name</b>		
		0b	Bit <b>[Default]</b>		
		1b	Byte		
	15	<b>Src Tiling Enable</b>			
			<b>Value</b>		
			<b>Name</b>		
		0b	Tiling Disabled (Linear) <b>[Default]</b>		
		1b	Tiling enabled: Tile-X or Tile-Y		
	14:12	<b>Horizontal Pattern Seed</b>			
		Default Value:	0b		
		This field indicates the pattern pixel position which corresponds to X = 0.			
	11	<b>Dest Tiling Enable</b>			
		When set to '1', this means that Blitter is executing in Tiled mode. If '0' it means that Blitter is in Linear mode. Pre-Dev Blitter never executes in Tiled-Y mode, DevGT+ Blitter supports both Tile-X and Tile-Y modes. On reset, this bit will be '0'. This definition applies to only X, Y Blits.			
			<b>Value</b>	<b>Name</b>	
			0b	Tiling Disabled (Linear blit) <b>[Default]</b>	
			1b	Tiling enabled: Tile-X or Tile-Y	
	10:8	<b>Transparency Range Mode</b>			
		These bits control whether or not the byte(s) at the destination corresponding to a given pixel will be conditionally written, and what those conditions are. This feature can make it possible to perform various masking functions in order to selectively write or preserve graphics data already at the destination.			
			<b>Value</b>	<b>Name</b>	<b>Description</b>
			xx0b	<b>[Default]</b>	No color transparency mode enabled. This causes normal operation with regard to writing data to the destination.
			001b		[Source color transparency] The Transparency Color Low: (Pixel Greater or Equal) (source background register) and the Transparency Color High: (Pixel Less or Equal) (source foreground register) are compared to the source pixels. The range comparisons are done on each component (R, G, B) and then logically ANDed. If the source pixel components are not within the range defined by the Transparency Color registers, then the byte(s) at the destination corresponding to the current pixel are written with the result of the bit-wise operation.

## BR00 - BLT Opcode and Control

		011b		[Source and Alpha color transparency] The Transparency Color Low: (Pixel Greater or Equal) (source background register) and the Transparency Color High: (Pixel Less or Equal) (source foreground register) are compared to the source pixels. The range comparisons are done on each component (A, R, G, B) and then logically ANDed. If the source pixel components are not within the range defined by the Transparency Color registers, then the byte(s) at the destination corresponding to the current pixel are written with the result of the bit-wise operation."
		101b		[Destination and Alpha color transparency] The Transparency Color Low: (Pixel Greater or Equal) (source background register) and the Transparency Color High: (Pixel Less or Equal) (source foreground register) are compared to the destination pixels. The range comparisons are done on each component (A, R, G, B) and then logically ANDed. If the destination pixels are within the range, then the byte(s) at the destination corresponding to the current pixel are written with the result of the bit-wise operation.
		111b		[Destination color transparency] The Transparency Color Low: (Pixel Greater or Equal) (source background register) and the Transparency Color High: (Pixel Less or Equal) (source foreground register) are compared to the destination pixels. The range comparisons are done on each component (R, G, B) and then logically ANDed. If the destination pixels are within the range, then the byte(s) at the destination corresponding to the current pixel are written with the result of the bit-wise operation.
7:5	<b>Pattern Vertical Seed</b>	Default Value:		000b
		This field specifies the pattern scan line which corresponds to Y=0.		
4	<b>Destination Read Modify Write</b>	Default Value:		0b
		This bit is decoded from the last instruction's opcode field and Destination Transparency Mode to identify whether a Destination read is needed.		
3	<b>Color Source</b>	Default Value:		0b
		This bit is decoded from the last instructions opcode field to identify whether a color (1) source is used.		
2	<b>Monochrome Source</b>	Default Value:		0b
		This bit is decoded from the last instructions opcode field to identify whether a monochrome (1) source is used.		
1	<b>Color Pattern</b>	Default Value:		0b
		This bit is decoded from the last instructions opcode field to identify whether a color (1) pattern is used.		

## BR00 - BLT Opcode and Control

	0	<b>Monochrome Pattern</b>
		Default Value: 0b
This bit is decoded from the last instruction's opcode field to identify whether a monochrome (1) pattern is used.		

## BR01 - Setup BLT Raster OP, Control, and Destination Offset

BR01 - Setup BLT Raster OP, Control, and Destination Offset											
DWord	Bit	Description									
0	31	<p><b>Solid Pattern Select</b></p> <p>This bit applies only when the pattern data is monochrome. This bit determines whether or not the BLT Engine actually performs read operations from the frame buffer in order to load the pattern data. Use of this feature to prevent these read operations can increase BLT Engine performance, if use of the pattern data is indeed not necessary. The BLT Engine is configured to accept either monochrome or color pattern data via the opcode field.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>[Default]</td> <td>This causes normal operation with regard to the use of the pattern data. The BLT Engine proceeds with the process of reading the pattern data, and the pattern data is used as the pattern operand for all bit-wise operations.</td> </tr> <tr> <td>1b</td> <td></td> <td>The BLT Engine forgoes the process of reading the pattern data, the presumption is made that all of the bits of the pattern data are set to 0, and the pattern operand for all bit-wise operations is forced to the background color specified in the Color Expansion Background Color Register.</td> </tr> </tbody> </table>	Value	Name	Description	0b	[Default]	This causes normal operation with regard to the use of the pattern data. The BLT Engine proceeds with the process of reading the pattern data, and the pattern data is used as the pattern operand for all bit-wise operations.	1b		The BLT Engine forgoes the process of reading the pattern data, the presumption is made that all of the bits of the pattern data are set to 0, and the pattern operand for all bit-wise operations is forced to the background color specified in the Color Expansion Background Color Register.
Value	Name	Description									
0b	[Default]	This causes normal operation with regard to the use of the pattern data. The BLT Engine proceeds with the process of reading the pattern data, and the pattern data is used as the pattern operand for all bit-wise operations.									
1b		The BLT Engine forgoes the process of reading the pattern data, the presumption is made that all of the bits of the pattern data are set to 0, and the pattern operand for all bit-wise operations is forced to the background color specified in the Color Expansion Background Color Register.									
	30	<p><b>Clipping Enabled</b></p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>[Default]</td> </tr> <tr> <td>1b</td> <td></td> </tr> </tbody> </table>	Value	Name	0b	[Default]	1b				
Value	Name										
0b	[Default]										
1b											
	29	<p><b>Monochrome Source Transparency Mode</b></p> <p>This bit applies only when the source data is in monochrome. This bit determines whether or not the byte(s) at the destination corresponding to the pixel to which a given bit of the source data also corresponds will actually be written if that source data bit has the value of 0. This feature can make it possible to use the source as a transparency mask. The BLT Engine is configured to accept either monochrome or color source data via the opcode field.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>[Default]</td> <td>This causes normal operation with regard to the use of the source data. Wherever a bit in the source data has the value of 0, the color specified in the background color register is used as the source operand in the bit-wise operation for the pixel corresponding to the source data bit, and the bytes at the destination corresponding to that pixel are written with the result.</td> </tr> <tr> <td>1b</td> <td></td> <td>Wherever a bit in the source data has the value of 0, the byte(s) at the destination corresponding to the pixel to which the source data bit also corresponds are simply not written, and the data at those byte(s) at the destination are allowed to remain unchanged.</td> </tr> </tbody> </table>	Value	Name	Description	0b	[Default]	This causes normal operation with regard to the use of the source data. Wherever a bit in the source data has the value of 0, the color specified in the background color register is used as the source operand in the bit-wise operation for the pixel corresponding to the source data bit, and the bytes at the destination corresponding to that pixel are written with the result.	1b		Wherever a bit in the source data has the value of 0, the byte(s) at the destination corresponding to the pixel to which the source data bit also corresponds are simply not written, and the data at those byte(s) at the destination are allowed to remain unchanged.
Value	Name	Description									
0b	[Default]	This causes normal operation with regard to the use of the source data. Wherever a bit in the source data has the value of 0, the color specified in the background color register is used as the source operand in the bit-wise operation for the pixel corresponding to the source data bit, and the bytes at the destination corresponding to that pixel are written with the result.									
1b		Wherever a bit in the source data has the value of 0, the byte(s) at the destination corresponding to the pixel to which the source data bit also corresponds are simply not written, and the data at those byte(s) at the destination are allowed to remain unchanged.									

## BR01 - Setup BLT Raster OP, Control, and Destination Offset

	28	<p><b>Monochrome Pattern Transparency Mode</b></p> <p>This bit applies only when the pattern data is monochrome. This bit determines whether or not the byte(s) at the destination corresponding to the pixel to which a given bit of the pattern data also corresponds will actually be written if that pattern data bit has the value of 1. This feature can make it possible to use the pattern as a transparency mask. The BLT Engine is configured to accept either monochrome or color pattern data via the opcode field.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td><b>[Default]</b></td><td>This causes normal operation with regard to the use of the pattern data. Wherever a bit in the pattern data has the value of 0, the color specified in the background color register is used as the pattern operand in the bit-wise operation for the pixel corresponding to the pattern data bit, and the bytes at the destination corresponding to that pixel are written with the result.</td></tr> <tr> <td>1b</td><td></td><td>Wherever a bit in the pattern data has the value of 0, the byte(s) at the destination corresponding to the pixel to which the pattern data bit also corresponds are simply not written, and the data at those byte(s) at the destination are allowed to remain unchanged.</td></tr> </tbody> </table>	Value	Name	Description	0b	<b>[Default]</b>	This causes normal operation with regard to the use of the pattern data. Wherever a bit in the pattern data has the value of 0, the color specified in the background color register is used as the pattern operand in the bit-wise operation for the pixel corresponding to the pattern data bit, and the bytes at the destination corresponding to that pixel are written with the result.	1b		Wherever a bit in the pattern data has the value of 0, the byte(s) at the destination corresponding to the pixel to which the pattern data bit also corresponds are simply not written, and the data at those byte(s) at the destination are allowed to remain unchanged.	
Value	Name	Description										
0b	<b>[Default]</b>	This causes normal operation with regard to the use of the pattern data. Wherever a bit in the pattern data has the value of 0, the color specified in the background color register is used as the pattern operand in the bit-wise operation for the pixel corresponding to the pattern data bit, and the bytes at the destination corresponding to that pixel are written with the result.										
1b		Wherever a bit in the pattern data has the value of 0, the byte(s) at the destination corresponding to the pixel to which the pattern data bit also corresponds are simply not written, and the data at those byte(s) at the destination are allowed to remain unchanged.										
	27:26	<p><b>32bpp Byte Mask</b></p> <p>This bit applies only when the pattern data is monochrome. This bit determines whether or not the byte(s) at the destination corresponding to the pixel to which a given bit of the pattern data also corresponds will actually be written if that pattern data bit has the value of 1. This feature can make it possible to use the pattern as a transparency mask. The BLT Engine is configured to accept either monochrome or color pattern data via the opcode field.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>00b</td><td><b>[Default]</b></td></tr> <tr> <td>1xb</td><td>Write Alpha Channel</td></tr> <tr> <td>x1b</td><td>Write RGB Channel</td></tr> </tbody> </table>	Value	Name	00b	<b>[Default]</b>	1xb	Write Alpha Channel	x1b	Write RGB Channel		
Value	Name											
00b	<b>[Default]</b>											
1xb	Write Alpha Channel											
x1b	Write RGB Channel											
	25:24	<p><b>Color Depth</b></p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>00b</td><td>8 Bit Color Depth <b>[Default]</b></td></tr> <tr> <td>01b</td><td>16 Bit Color Depth</td></tr> <tr> <td>10b</td><td>Alternate 16 Bit Color Depth</td></tr> <tr> <td>11b</td><td>32 Bit Color Depth</td></tr> </tbody> </table>	Value	Name	00b	8 Bit Color Depth <b>[Default]</b>	01b	16 Bit Color Depth	10b	Alternate 16 Bit Color Depth	11b	32 Bit Color Depth
Value	Name											
00b	8 Bit Color Depth <b>[Default]</b>											
01b	16 Bit Color Depth											
10b	Alternate 16 Bit Color Depth											
11b	32 Bit Color Depth											
	23:16	<p><b>Raster Operation Select</b></p> <p>These 8 bits are used to select which one of 256 possible raster operations is to be performed by the BLT Engine.</p>										

## BR01 - Setup BLT Raster OP, Control, and Destination Offset

15:0	<b>Destination Pitch (Offset)</b> For non-XY Blits, the signed 16bit field allows for specifying upto + 32Kbytes signed pitches in bytes (same as before). For X, Y Blits with tiled-X surfaces, the pitch for Destination will be 512Byte aligned and should be programmable upto + 128Kbytes. For X, Y Blits with tiled-Y surfaces, the pitch for Destination will be 128Byte aligned and should be programmable upto + 128Kbytes. In this case, this 16bit signed pitch field is used to specify upto + 32KDWords. For X, Y blits with nontiled surfaces (linear surfaces), this 16bit field can be programmed to byte specification of upto + 32Kbytes (same as before). These 16 bits store the signed memory address offset value by which the destination address originally specified in the Destination Address Register is incremented or decremented as each scan line's worth of destination data is written into the frame buffer by the BLT Engine, so that the destination address will point to the next memory address to which the next scan line's worth of destination data is to be written. If the intended destination of a BLT operation is within on-screen frame buffer memory, this offset is normally set so that each subsequent scan line's worth of destination data lines up vertically with the destination data in the scan line, above. However, if the intended destination of a BLT operation is within off-screen memory, this offset can be set so that each subsequent scan line's worth of destination data is stored at a location immediately after the location where the destination data for the last scan line ended, in order to create a single contiguous block of bytes of destination data at the destination.
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## BR05 - Setup Expansion Background Color

BR05 - Setup Expansion Background Color		
DWord	Bit	Description
0	31:0	<p><b>Setup Expansion Background Color Bits</b></p> <p>These bits provide the one, two, or four bytes worth of color data that select the background color to be used in the color expansion of monochrome pattern or source data for either the SCANLINE_BLT or TEXT_BLT instructions. BR05 is also used as the solid pattern for the PIXEL_BLT instruction. Whether one, two, or three bytes worth of color data is needed depends upon the color depth to which the BLT Engine has been set. For a color depth of 32bpp, 16bpp and 8bpp, bits [31:0], [15:0] and [7:0], respectively, are used.</p>

## BR06 - Setup Expansion Foreground Color

BR06 - Setup Expansion Foreground Color		
DWord	Bit	Description
0	31:0	<p><b>Setup Expansion Foreground Color Bits</b></p> <p>These bits provide the one, two, or four bytes worth of color data that select the foreground color to be used in the color expansion of monochrome pattern or source data for either the SCANLINE_BLT or TEXT_BLT instructions. Whether one, two, or three bytes worth of color data is needed depends upon the color depth to which the BLT Engine has been set. For a color depth of 32bpp, 16bpp and 8bpp, bits [31:0], [15:0] and [7:0], respectively, are used.</p>

## BR07 - Setup Blit Color Pattern Address Lower Order Address bits

BR07 - Setup Blit Color Pattern Address Lower Order Address bits				
DWord	Bit	Description		
0	31:6	<p><b>Setup Blit Color Pattern Address</b></p> <table border="1"> <tr> <td>Format:</td> <td>GraphicsAddress[31:6]</td> </tr> </table> <p>Lower 32bits of the 48bit addressing.</p> <p>These 26 bits specify the starting address of the (8X8) pixel color <b>pattern from the SETUP_BLT instruction</b>. This register works identically to the Pattern Address register (BR15), but this version is <b>only used with the SCANLINE_BLT instruction execution</b> (the actual programming for this, is done in XY_SETUP_BLT command). The pattern data must be located in linear memory.</p> <p>The pattern data must be located on a pattern-size boundary. The pattern is always of 8x8 pixels, and therefore, its size is dependent upon its pixel depth. The pixel depth may be 8, 16, or 32 bits per pixel if the pattern is in color (the pixel depth of a color pattern must match the pixel depth to which the graphics system has been set). Monochrome patterns require 8 bytes and is supplied through the instruction. Color patterns of 8, 16, and 32 bits per pixel color depth must start on 64-byte, 128-byte and 256-byte boundaries, respectively.</p> <p>The Pattern Base Address programmed, must always be Cache Line (64byte) aligned.</p>	Format:	GraphicsAddress[31:6]
Format:	GraphicsAddress[31:6]			
5:0	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ	
Format:	MBZ			

## BR09 - Destination Address Lower Order Address Bits

BR09 - Destination Address Lower Order Address Bits				
DWord	Bit	Description		
0	31:0	<p><b>Destination Address Bits</b></p> <table border="1"> <tr> <td>Format:</td> <td>GraphicsAddress[31:0]</td> </tr> </table> <p>When tiling is enabled for XY-blits, this base address should be limited to 4KB. When tiling is disabled for XY-blits, this base address should be CL (64byte) aligned. These lower 32bits of the 48bit address, which specify the starting pixel address of the destination data. This register is also the working destination address register for the lower 32bits of the address, and changes as the BLT Engine performs the accesses. Used as the scan line address (Destination Y Address and Destination Y1 Address) for BLT instructions: PIXEL_BLT, SCANLINE_BLT, and TEXT_BLT. In this case the address points to the first pixel in a scan line and is compared with the ClipRect Y1 and Y2 address registers to determine whether the scan line should be written or not. The Destination Y1 address is the top scan line to be written for text. Note that for non-XY blits (COLOR_BLT, SRC_COPY_BLT), this address points to the first byte to be written. Note: Some instructions affect only one scan line (requiring only one coordinate); other instructions affect multiple scan lines and need both coordinates.</p>	Format:	GraphicsAddress[31:0]
Format:	GraphicsAddress[31:0]			

## BR11 - BLT Source Pitch (Offset)

BR11 - BLT Source Pitch (Offset)		
DWord	Bit	Description
0	31:16	<b>Reserved</b>
	15:0	<p><b>Source Pitch (Offset)</b></p> <p>For non-XY Blits with color source operand (SRC_COPY_BLT), the signed 16bit field allows for specifying upto + 32Kbytes signed pitch in bytes (same as before). For X, Y Blits with tiled-X surfaces, the pitch for Color Source will be 512Byte aligned and should be programmable upto + 128Kbytes. For X, Y Blits with tiled-Y surfaces, the pitch for Color Source will be 128Byte aligned and should be programmable upto + 128Kbytes. In this case, this 16bit signed pitch field is used to specify upto + 32KDWords. For X, Y blits with nontiled color source surfaces (linear surfaces), this 16bit field can be programmed to byte specification of upto + 32Kbytes (same as before). When the color source data is located within the frame buffer or AGP aperture, these signed 16 bits store the memory address offset (pitch) value by which the source address originally specified in the Source Address Register is incremented or decremented as each scan line's worth of source data is read from the frame buffer by the BLT Engine, so that the source address will point to the next memory address from which the next scan line's worth of source data is to be read. Note that if the intended source of a BLT operation is within on-screen frame buffer memory, this offset is normally set to accommodate the fact that each subsequent scan line's worth of source data lines up vertically with the source data in the scan line, above. However, if the intended source of a BLT operation is within off-screen memory, this offset can be set to accommodate a situation in which the source data exists as a single contiguous block of bytes where in each subsequent scan line's worth of source data is stored at a location immediately after the location where the source data for the last scan line ended.</p>

## BR12 - Source Address Lower order Address bits

BR12 - Source Address Lower order Address bits				
DWord	Bit	Description		
0	31:0	<p><b>Source Address Bits</b></p> <table border="1"> <tr> <td>Format:</td> <td>GraphicsAddress[31:0]</td> </tr> </table> <p>Lower 32bits of the 48bit addressing.  When tiling is enabled for XY-blits with Color source surfaces, this base address should be limited to 4KB. When tiling is disabled for XY-blits, this base address should be CL (64byte) aligned.  Note that for non-XY blit with Color Source (SRC_COPY_BLT), this address points to the first byte to be read.  These lower 32bits of the 48bit address, specify the starting pixel address of the color source data.  The lower 3 bits are used to indicate the position of the first valid byte within the first Quadword of the source data.  If this Source happens to be a Monosource surface, then this Monosource Base Address programmed, must always be Cache Line (64byte) aligned.</p>	Format:	GraphicsAddress[31:0]
Format:	GraphicsAddress[31:0]			

## BR13 - BLT Raster OP, Control, and Destination Pitch

BR13 - BLT Raster OP, Control, and Destination Pitch											
DWord	Bit	Description									
0	31	<p><b>Solid Pattern Select</b></p> <p>This bit applies only when the pattern data is monochrome. This bit determines whether or not the BLT Engine actually performs read operations from the frame buffer in order to load the pattern data. Use of this feature to prevent these read operations can increase BLT Engine performance, if use of the pattern data is indeed not necessary. The BLT Engine is configured to accept either monochrome or color pattern data via the opcode field.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>[Default]</td> <td>This causes normal operation with regard to the use of the pattern data. The BLT Engine proceeds with the process of reading the pattern data, and the pattern data is used as the pattern operand for all bit-wise operations.</td> </tr> <tr> <td>1</td> <td></td> <td>The BLT Engine forgoes the process of reading the pattern data, the presumption is made that all of the bits of the pattern data are set to 0, and the pattern operand for all bit-wise operations is forced to the background color specified in the Color Expansion Background Color Register.</td> </tr> </tbody> </table>	Value	Name	Description	0	[Default]	This causes normal operation with regard to the use of the pattern data. The BLT Engine proceeds with the process of reading the pattern data, and the pattern data is used as the pattern operand for all bit-wise operations.	1		The BLT Engine forgoes the process of reading the pattern data, the presumption is made that all of the bits of the pattern data are set to 0, and the pattern operand for all bit-wise operations is forced to the background color specified in the Color Expansion Background Color Register.
Value	Name	Description									
0	[Default]	This causes normal operation with regard to the use of the pattern data. The BLT Engine proceeds with the process of reading the pattern data, and the pattern data is used as the pattern operand for all bit-wise operations.									
1		The BLT Engine forgoes the process of reading the pattern data, the presumption is made that all of the bits of the pattern data are set to 0, and the pattern operand for all bit-wise operations is forced to the background color specified in the Color Expansion Background Color Register.									
30	Clipping Enabled	<p>Default Value:</p> <table border="1"> <tr> <td>0</td> </tr> </table>	0								
0											
29	<p><b>Monochrome Source Transparency Mode</b></p> <p>This bit applies only when the source data is in monochrome. This bit determines whether or not the byte(s) at the destination corresponding to the pixel to which a given bit of the source data also corresponds will actually be written if that source data bit has the value of 0. This feature can make it possible to use the source as a transparency mask. The BLT Engine is configured to accept either monochrome or color source data via the opcode field.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>[Default]</td> <td>This causes normal operation with regard to the use of the source data. Wherever a bit in the source data has the value of 0, the color specified in the background color register is used as the source operand in the bit-wise operation for the pixel corresponding to the source data bit, and the bytes at the destination corresponding to that pixel are written with the result.</td> </tr> <tr> <td>1</td> <td></td> <td>Where a bit in the source data has the value of 0, the byte(s) at the destination corresponding to the pixel to which the source data bit also corresponds are simply not written, and the data at those byte(s) at the destination are allowed to remain unchanged.</td> </tr> </tbody> </table>	Value	Name	Description	0	[Default]	This causes normal operation with regard to the use of the source data. Wherever a bit in the source data has the value of 0, the color specified in the background color register is used as the source operand in the bit-wise operation for the pixel corresponding to the source data bit, and the bytes at the destination corresponding to that pixel are written with the result.	1		Where a bit in the source data has the value of 0, the byte(s) at the destination corresponding to the pixel to which the source data bit also corresponds are simply not written, and the data at those byte(s) at the destination are allowed to remain unchanged.	
Value	Name	Description									
0	[Default]	This causes normal operation with regard to the use of the source data. Wherever a bit in the source data has the value of 0, the color specified in the background color register is used as the source operand in the bit-wise operation for the pixel corresponding to the source data bit, and the bytes at the destination corresponding to that pixel are written with the result.									
1		Where a bit in the source data has the value of 0, the byte(s) at the destination corresponding to the pixel to which the source data bit also corresponds are simply not written, and the data at those byte(s) at the destination are allowed to remain unchanged.									

## BR13 - BLT Raster OP, Control, and Destination Pitch

	28	<b>Monochrome Pattern Transparency Mode</b> This bit applies only when the pattern data is monochrome. This bit determines whether or not the byte(s) at the destination corresponding to the pixel to which a given bit of the pattern data also corresponds will actually be written if that pattern data bit has the value of 1. This feature can make it possible to use the pattern as a transparency mask. The BLT Engine is configured to accept either monochrome or color pattern data via the opcode in the Opcode and Control register.										
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>[Default]</td> <td>This causes normal operation with regard to the use of the pattern data. Where a bit in the pattern data has the value of 0, the color specified in the background color register is used as the pattern operand in the bit-wise operation for the pixel corresponding to the pattern data bit, and the bytes at the destination corresponding to that pixel are written with the result.</td> </tr> <tr> <td>1</td> <td></td> <td>Wherever a bit in the pattern data has the value of 0, the byte(s) at the destination corresponding to the pixel to which the pattern data bit also corresponds are simply not written, and the data at those byte(s) at the destination are allowed to remain unchanged.</td> </tr> </tbody> </table>	Value	Name	Description	0	[Default]	This causes normal operation with regard to the use of the pattern data. Where a bit in the pattern data has the value of 0, the color specified in the background color register is used as the pattern operand in the bit-wise operation for the pixel corresponding to the pattern data bit, and the bytes at the destination corresponding to that pixel are written with the result.	1		Wherever a bit in the pattern data has the value of 0, the byte(s) at the destination corresponding to the pixel to which the pattern data bit also corresponds are simply not written, and the data at those byte(s) at the destination are allowed to remain unchanged.	
Value	Name	Description										
0	[Default]	This causes normal operation with regard to the use of the pattern data. Where a bit in the pattern data has the value of 0, the color specified in the background color register is used as the pattern operand in the bit-wise operation for the pixel corresponding to the pattern data bit, and the bytes at the destination corresponding to that pixel are written with the result.										
1		Wherever a bit in the pattern data has the value of 0, the byte(s) at the destination corresponding to the pixel to which the pattern data bit also corresponds are simply not written, and the data at those byte(s) at the destination are allowed to remain unchanged.										
	27:26	<b>32bpp Byte Mask</b> This field is only used for 32bpp.										
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>[Default]</td> </tr> <tr> <td>1xb</td> <td>Write Alpha Channel</td> </tr> <tr> <td>x1b</td> <td>Write RGB Channel</td> </tr> </tbody> </table>	Value	Name	00b	[Default]	1xb	Write Alpha Channel	x1b	Write RGB Channel		
Value	Name											
00b	[Default]											
1xb	Write Alpha Channel											
x1b	Write RGB Channel											
	25:24	<b>Color Depth</b>										
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>8 Bit Color Depth [Default]</td> </tr> <tr> <td>01b</td> <td>16 Bit Color Depth</td> </tr> <tr> <td>10b</td> <td>24 Bit Color Depth</td> </tr> <tr> <td>11b</td> <td>Reserved</td> </tr> </tbody> </table>	Value	Name	00b	8 Bit Color Depth [Default]	01b	16 Bit Color Depth	10b	24 Bit Color Depth	11b	Reserved
Value	Name											
00b	8 Bit Color Depth [Default]											
01b	16 Bit Color Depth											
10b	24 Bit Color Depth											
11b	Reserved											
	23:16	<b>Raster Operation Select</b>										
		<table border="1"> <tr> <td>Default Value:</td> <td>00000000b</td> </tr> </table> <p>These 8 bits are used to select which one of 256 possible raster operations is to be performed by the BLT Engine.</p>	Default Value:	00000000b								
Default Value:	00000000b											

## BR13 - BLT Raster OP, Control, and Destination Pitch

15:0	<p><b>Destination Pitch(Offset)</b></p> <p>These 16 bits store the signed memory address offset value by which the destination address originally specified in the Destination Address Register is incremented or decremented as each scan line's worth of destination data is written into the frame buffer by the BLT Engine, so that the destination address will point to the next memory address to which the next scan line's worth of destination data is to be written. If the intended destination of a BLT operation is within on-screen frame buffer memory, this offset is normally set so that each subsequent scan line's worth of destination data lines up vertically with the destination data in the scan line, above. However, if the intended destination of a BLT operation is within off-screen memory, this offset can be set so that each subsequent scan line's worth of destination data is stored at a location immediately after the location where the destination data for the last scan line ended, in order to create a single contiguous block of bytes of destination data at the destination.</p>
------	--

## BR14 - Destination Width and Height

BR14 - Destination Width and Height		
DWord	Bit	Description
0	31:29	<b>Reserved</b>
	28:16	<b>Destination Height</b> These 13 bits specify the height of the destination data in terms of the number of scan lines. This is a working register.
	15:13	<b>Reserved</b>
	12:0	<b>Destination Byte Width</b> These 13 bits specify the width of the destination data in terms of the number of bytes per scan line. The number of pixels per scan line into which this value translates depends upon the color depth to which the graphics system has been set.

## BR15 - Color Pattern Address Lower order Address bits

BR15 - Color Pattern Address Lower order Address bits			
DWord	Bit	Description	
0	31:6	<b>Color Pattern Address</b>	
		Format:	GraphicsAddress[31:6]
	5:0	Lower 32bits of the 48bit addressing. There is no change to the Color Pattern address specification due to Non-Power-of-2 change. It remains the same as before. The pattern data must be located in linear memory. These 26 bits specify the starting address of the (8X8) pixel color pattern. The pattern data must be located on a pattern-size boundary. The pattern is always of 8x8 pixels, and therefore, its size is dependent upon its pixel depth. The pixel depth may be 8, 16, or 32 bits per pixel if the pattern is in color (the pixel depth of a color pattern must match the pixel depth to which the graphics system has been set). Monochrome patterns require 8 bytes and are applied through the instruction. Color patterns of 8, 16, and 32 bits per pixel color depth must start on 64-byte, 128-byte and 256-byte boundaries, respectively. The Pattern Base Address programmed, must always be Cache Line (64byte) aligned.	
		Reserved	Format: MBZ

## BR16 - Pattern Expansion Background and Solid Pattern Color

BR16 - Pattern Expansion Background and Solid Pattern Color		
Project:	BDW	
Source:	BlitterCS	
Size (in bits):	32	
Default Value:	0x00000000	
DWord	Bit	Description
0	31:0	<p><b>Pattern Expansion Background Color Bits</b></p> <p>These bits provide the one, two, or four bytes worth of color data that select the background color to be used in the color expansion of monochrome pattern data during BLT operations. Whether one, two, or four bytes worth of color data is needed depends upon the color depth to which the BLT Engine has been set. For a color depth of 32bpp, 16bpp and 8bpp, bits [31:0], [15:0] and [7:0], respectively, are used.</p>

## BR17 - Pattern Expansion Foreground Color

BR17 - Pattern Expansion Foreground Color		
DWord	Bit	Description
0	31:0	<p><b>Pattern Expansion Background Color Bits</b></p> <p>These bits provide the one, two, or four bytes worth of color data that select the foreground color to be used in the color expansion of monochrome pattern data during BLT operations. Whether one, two, or four bytes worth of color data is needed depends upon the color depth to which the BLT Engine has been set. For a color depth of 32bpp, 16bpp and 8bpp, bits [31:0], [15:0] and [7:0], respectively, are used.</p>

## BR18 - Source Expansion Background and Destination Color

BR18 - Source Expansion Background and Destination Color		
Project:	BDW	
Source:	BlitterCS	
Size (in bits):	32	
Default Value:	0x00000000	
DWord	Bit	Description
0	31:0	<p><b>Source Expansion Background Color Bits</b></p> <p>These bits provide the one, two, or four bytes worth of color data that select the background color to be used in the color expansion of monochrome source data during BLT operations. This register is also used to support destination transparency mode and Solid color fill. Whether one, two, three, or four bytes worth of color data is needed depends upon the color depth to which the BLT Engine has been set. For a color depth of 32bpp, 16bpp and 8bpp, bits [31:0], [15:0] and [7:0], respectively, are used.</p>

## BR19 - Source Expansion Foreground Color

BR19 - Source Expansion Foreground Color		
DWord	Bit	Description
0	31:0	<p><b>Pattern/Source Expansion Foreground Color Bits</b></p> <p>These bits provide the one, two, or four bytes worth of color data that select the foreground color to be used in the color expansion of monochrome source data during BLT operations. Whether one, two, or four bytes worth of color data is needed depends upon the color depth to which the BLT Engine has been set. For a color depth of 32bpp, 16bpp and 8bpp, bits [31:0], [15:0] and [7:0], respectively, are used.</p>

## BR27 - Destination Address Higher Order Address

BR27 - Destination Address Higher Order Address				
DWord	Bit	Description		
0	31:16	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ
Format:	MBZ			
	15:0	<p><b>Destination Address Upper DWORD</b></p> <table border="1"> <tr> <td>Format:</td> <td>GraphicsAddress[47:32]</td> </tr> </table> <p>When tiling is enabled for XY-blits, this base address should be limited to 4KB. Otherwise for XY blits, there is no restriction and it is same as before. These upper 16bits of the 48bit address, along with BR09 register, will specify the starting pixel address of the destination data. This register is also the working destination address register for the upper 16bits of the destination address, and changes as the BLT Engine performs the accesses. Used as the scan line address (Destination Y Address and Destination Y1 Address) for BLT instructions: PIXEL_BLT, SCANLINE_BLT, and TEXT_BLT. In this case the address points to the first pixel in a scan line and is compared with the ClipRect Y1 and Y2 address registers to determine whether the scan line should be written or not. The Destination Y1 address is the top scan line to be written for text. Note that for non-XY blits (COLOR_BLT, SRC_COPY_BLT), this 16bits of the 48bit address, along with BR09 register, points to the first byte to be written. This register is always the last register written for a BLT drawing instruction. Writing BR27 starts the BLT engine execution. Note: Some instructions affect only one scan line (requiring only one coordinate); other instructions affect multiple scan lines and need both coordinates.</p>	Format:	GraphicsAddress[47:32]
Format:	GraphicsAddress[47:32]			

## BR28 - Source Address Higher order Address

BR28 - Source Address Higher order Address				
Project:	BDW			
Source:	BlitterCS			
Size (in bits):	32			
Default Value:	0x00000000			
DWord	Bit	Description		
0	31:16	<b>Reserved</b> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ
Format:	MBZ			
15:0	<b>Source Address Upper DWORD</b> <table border="1"> <tr> <td>Format:</td> <td>GraphicsAddress[47:32]</td> </tr> </table> <p>These upper 16bits of the 48bit address, specify the starting pixel address of the color or mono source data. When tiling is enabled for XY-blits with Color source surfaces, this base address should be limited to 4KB. Otherwise for XY blits, there is no restriction and it is same as before, including for monosource and text blits. Note that for non-XY blit with Color Source (SRC_COPY_BLT), this address points to the first byte to be read.</p>	Format:	GraphicsAddress[47:32]	
Format:	GraphicsAddress[47:32]			

## BR29 - Color Pattern Address Higher order Address

BR29 - Color Pattern Address Higher order Address			
Project:	BDW		
Source:	BlitterCS		
Size (in bits):	32		
Default Value:	0x00000000		
DWord	Bit	Description	
0	31:16	<b>Reserved</b>	
		Format:	MBZ
	15:0	<b>Color Pattern Address Upper DWORD</b>	
		Format:	GraphicsAddress[47:32]
These upper 16bits of the 48bit address,specify the starting address of the (8X8) pixel pattern.			

## BR30 - Setup Blit Color Pattern Address Higher Order Address

BR30 - Setup Blit Color Pattern Address Higher Order Address				
Project:	BDW			
Source:	BlitterCS			
Size (in bits):	32			
Default Value:	0x00000000			
DWord	Bit	Description		
0	31:16	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ
Format:	MBZ			
15:0	<p><b>Setup Blit Color Pattern Address Upper DWORD</b></p> <table border="1"> <tr> <td>Format:</td> <td>GraphicsAddress[47:32]</td> </tr> </table> <p>These upper 16bits of the 48bit address,specify the starting address of the (8X8) pixel pattern.</p>	Format:	GraphicsAddress[47:32]	
Format:	GraphicsAddress[47:32]			

## Byte Masked Media Block Message Header

<b>MH_MBBM - Byte Masked Media Block Message Header</b>			
<b>DWord</b>	<b>Bit</b>	<b>Description</b>	
0	31:0	<b>X Offset</b>	
		Project:	All
		Format:	S31
		X offset (in bytes) of the upper left corner of the block into the surface.	
		<b>Programming Notes</b>	
1	31:0	<b>Y Offset</b>	
		Project:	All
		Format:	S31
		Y offset (in rows) of the upper left corner of the block into the surface.	
2	31:0	<b>Media Block Message Control</b>	
		Project:	All
		Format:	<b>MHC_MBBM_CONTROL</b>
		Specifies the Byte Masked message subtype and its additional input parameters.	
3	31:0	<b>Byte Mask</b>	
		Project:	All
		Format:	U32
		Specifies the Byte Mask for writes when Message Mode field is BYTE_MASK.	
		<b>Programming Notes</b>	
4	31:0	<b>FFTID</b>	
		Project:	All
		Format:	<b>MHC_FFTID</b>
		Fixed Function Thread ID	
5-7	95:0	<b>Reserved</b>	
		Project:	All
		Format:	Ignore
		Ignored	

## Byte Masked Media Block Message Header Control

### MHC\_MBBM\_CONTROL - Byte Masked Media Block Message Header Control

Project: BDW  
Size (in bits): 32  
Default Value: 0x00000000

DWord	Bit	Description													
0	31:30	<p><b>Message Mode</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Enumeration</td> </tr> </table> <p>Specifies the Media Block Write Message subtype is Byte Masked.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>02h</td> <td>BYTE_MASK</td> <td>The Block Height and Block Width fields are specified in this Dword. The Byte Mask qualifies which bytes are written.</td> </tr> <tr> <td>Others</td> <td>Reserved</td> <td>Reserved.</td> </tr> </tbody> </table>	Project:	All	Format:	Enumeration	Value	Name	Description	02h	BYTE_MASK	The Block Height and Block Width fields are specified in this Dword. The Byte Mask qualifies which bytes are written.	Others	Reserved	Reserved.
Project:	All														
Format:	Enumeration														
Value	Name	Description													
02h	BYTE_MASK	The Block Height and Block Width fields are specified in this Dword. The Byte Mask qualifies which bytes are written.													
Others	Reserved	Reserved.													
	29	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Ignore</td> </tr> </table> <p>Ignored</p>	Project:	All	Format:	Ignore									
Project:	All														
Format:	Ignore														
	28:24	<p><b>Sub-Register Offset</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U5</td> </tr> </table> <p>This field is ignored (reserved) for Media Block Write message.</p>	Project:	All	Format:	U5									
Project:	All														
Format:	U5														
	23:22	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Ignore</td> </tr> </table> <p>Ignored</p>	Project:	All	Format:	Ignore									
Project:	All														
Format:	Ignore														
	21:16	<p><b>Block Height</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U6</td> </tr> </table> <p>Height in rows of block being accessed. Range = [0,63] representing 1 to 64 rows</p> <table border="1"> <thead> <tr> <th>Restriction</th> </tr> </thead> <tbody> <tr> <td>If Block Width (bytes), then Maximum Block Height (rows) is constrained by (# Dwords width) * (# rows) &lt;= 64 Dwords.</td> </tr> </tbody> </table>	Project:	All	Format:	U6	Restriction	If Block Width (bytes), then Maximum Block Height (rows) is constrained by (# Dwords width) * (# rows) <= 64 Dwords.							
Project:	All														
Format:	U6														
Restriction															
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## MHC\_MBBM\_CONTROL - Byte Masked Media Block Message Header Control

	<b>15:10 Reserved</b>
	Project: All
	Format: Ignore
	Ignored
	<b>9:8 Register Pitch Control</b>
	Project: All
	Format: U2
	This field is ignored (reserved) for a Media Block Write message.
	<b>7:6 Reserved</b>
	Project: All
	Format: Ignore
	Ignored
	<b>5:0 Block Width</b>
	Project: All
	Format: U6
	Width in bytes of the block being accessed. Range = [0,31] representing 1 to 32 Bytes.
	<b>Programming Notes</b>
	Must be DWord aligned for Media Block Write message.

## CC\_VIEWPORT

CC_VIEWPORT						
DWord	Bit	Description				
0	31:0	<p><b>Minimum Depth</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>IEEE_Float</td></tr> </table> <p>Indicates the minimum depth. The interpolated or computed depth is clamped to this value prior to the depth test.</p> <p><b>Programming Notes</b></p> <p>The Minimum depth value must be less-than-or-equal to the Maximum depth value. The Minimum depth value cannot be NAN (Not-A-Number). The Minimum depth value must not be less than -1.0.</p>	Project:	All	Format:	IEEE_Float
Project:	All					
Format:	IEEE_Float					
1	31:0	<p><b>Maximum Depth</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>IEEE_Float</td></tr> </table> <p>Indicates the maximum depth. The interpolated or computed depth is clamped to this value prior to the depth test.</p> <p><b>Programming Notes</b></p> <p>The Maximum depth value cannot be NAN (Not-A-Number). The Maximum depth value must be less-than-or-equal to +1.0.</p>	Project:	All	Format:	IEEE_Float
Project:	All					
Format:	IEEE_Float					

## Channel Mask Message Descriptor Control Field

<b>MDC_CMASK - Channel Mask Message Descriptor Control Field</b>																																																									
<b>DWord</b>	<b>Bit</b>	<b>Description</b>																																																							
0	3:0	<b>Mask</b> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Enumeration</td> </tr> </table> <p>For the read message, indicates that which channels are read from the surface and included in the writeback message. For the write message, indicates which channels are included in the message payload and written to the surface.</p> <table border="1"> <thead> <tr> <th><b>Value</b></th> <th><b>Name</b></th> <th><b>Description</b></th> </tr> </thead> <tbody> <tr> <td>00h</td> <td>RGBA <b>[Default]</b></td> <td>Red, Green, Blue, and Alpha are included</td> </tr> <tr> <td>01h</td> <td>GBA</td> <td>Green, Blue, and Alpha are included</td> </tr> <tr> <td>02h</td> <td>RBA</td> <td>Red, Blue, and Alpha are included</td> </tr> <tr> <td>03h</td> <td>BA</td> <td>Blue and Alpha are included</td> </tr> <tr> <td>04h</td> <td>RGA</td> <td>Red, Green, and Alpha are included</td> </tr> <tr> <td>05h</td> <td>GA</td> <td>Green and Alpha are included</td> </tr> <tr> <td>06h</td> <td>RA</td> <td>Red and Alpha are included</td> </tr> <tr> <td>07h</td> <td>A</td> <td>Alpha is included</td> </tr> <tr> <td>08h</td> <td>RGB</td> <td>Red, Green, and Blue are included</td> </tr> <tr> <td>09h</td> <td>GB</td> <td>Green and Blue are included</td> </tr> <tr> <td>0Ah</td> <td>RB</td> <td>Red and Blue are included</td> </tr> <tr> <td>0Bh</td> <td>B</td> <td>Blue is included</td> </tr> <tr> <td>0Ch</td> <td>RG</td> <td>Red and Green are included</td> </tr> <tr> <td>0Dh</td> <td>G</td> <td>Green is included</td> </tr> <tr> <td>0Eh</td> <td>R</td> <td>Red is included</td> </tr> <tr> <td>0Fh</td> <td>Reserved</td> <td>Ignored</td> </tr> </tbody> </table>	Project:	All	Format:	Enumeration	<b>Value</b>	<b>Name</b>	<b>Description</b>	00h	RGBA <b>[Default]</b>	Red, Green, Blue, and Alpha are included	01h	GBA	Green, Blue, and Alpha are included	02h	RBA	Red, Blue, and Alpha are included	03h	BA	Blue and Alpha are included	04h	RGA	Red, Green, and Alpha are included	05h	GA	Green and Alpha are included	06h	RA	Red and Alpha are included	07h	A	Alpha is included	08h	RGB	Red, Green, and Blue are included	09h	GB	Green and Blue are included	0Ah	RB	Red and Blue are included	0Bh	B	Blue is included	0Ch	RG	Red and Green are included	0Dh	G	Green is included	0Eh	R	Red is included	0Fh	Reserved	Ignored
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0Dh	G	Green is included																																																							
0Eh	R	Red is included																																																							
0Fh	Reserved	Ignored																																																							

## Channel Mode Message Descriptor Control Field

<b>MDC_CMODE - Channel Mode Message Descriptor Control Field</b>															
<b>DWord</b>	<b>Bit</b>	<b>Description</b>													
0	0	<p><b>Channel Mode</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Enumeration</td> </tr> </table> <p>Two modes of channel-enable are provided: a SIMD8 or SIMD16 Dword channel serial view of a register, and a SIMD4x2 view of a register.</p> <table border="1"> <thead> <tr> <th><b>Value</b></th> <th><b>Name</b></th> <th><b>Description</b></th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Oword</td> <td>All 4 Dwords are read or written if one or more of these channels are enabled</td> </tr> <tr> <td>1</td> <td>Dword</td> <td>Each Dword is read or written only if its corresponding channel is enabled.</td> </tr> </tbody> </table>	Project:	All	Format:	Enumeration	<b>Value</b>	<b>Name</b>	<b>Description</b>	0	Oword	All 4 Dwords are read or written if one or more of these channels are enabled	1	Dword	Each Dword is read or written only if its corresponding channel is enabled.
Project:	All														
Format:	Enumeration														
<b>Value</b>	<b>Name</b>	<b>Description</b>													
0	Oword	All 4 Dwords are read or written if one or more of these channels are enabled													
1	Dword	Each Dword is read or written only if its corresponding channel is enabled.													

## Clock Gating Disable Format

Clock Gating Disable Format		
DWord	Bit	Description
0	0	<b>Clock_Gate_Disable</b>
Value	Name	Description
0b	Enable	Clock gating controlled by unit logic
1b	Disable	Disable clock gating function

## Clock Gating Disable Format

Clock Gating Disable Format		
DWord	Bit	Description
0	0	<b>Clock Gate Disable</b>
Value	Name	Description
0b	Enable	Clock gating controlled by unit enabling logic
1b	Disable	Disable clock gating function

## COLOR\_CALC\_STATE

<b>COLOR_CALC_STATE</b>											
<b>DWord</b>	<b>Bit</b>	<b>Description</b>									
0	31:24	<p><b>Stencil Reference Value</b></p> <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Format:</td> <td>U8.0</td> </tr> </table> <p>This field specifies the stencil reference value to compare against in the (front face) StencilTest function.</p>	Project:	BDW	Format:	U8.0					
Project:	BDW										
Format:	U8.0										
	23:16	<p><b>BackFace Stencil Reference Value</b></p> <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Format:</td> <td>U8.0</td> </tr> </table> <p>This field specifies the stencil reference value to compare against in the StencilTest function.</p>	Project:	BDW	Format:	U8.0					
Project:	BDW										
Format:	U8.0										
	15	<p><b>Round Disable Function Disable</b></p> <p>Disables the round-disable function of the color calculator.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Cancelled</td> <td>Dithering is cancelled based on the data used by blend to avoid drift.</td> </tr> <tr> <td>1</td> <td>Not Cancelled</td> <td>Dithering is NOT cancelled.</td> </tr> </tbody> </table>	Value	Name	Description	0	Cancelled	Dithering is cancelled based on the data used by blend to avoid drift.	1	Not Cancelled	Dithering is NOT cancelled.
Value	Name	Description									
0	Cancelled	Dithering is cancelled based on the data used by blend to avoid drift.									
1	Not Cancelled	Dithering is NOT cancelled.									
	14:1	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ							
Format:	MBZ										
	0	<p><b>Alpha Test Format</b></p> <p>This field selects the format for Alpha Reference Value and the format in which Alpha Test is performed.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>ALPHATEST_UNORM8</td> <td>UNorm8</td> </tr> <tr> <td>1h</td> <td>ALPHATEST_FLOAT32</td> <td>Float32</td> </tr> </tbody> </table> <p><b>Programming Notes</b></p> <p>Alpha-test format is independent of RT format. When PS outputs UNIT/SINT alpha-value, it will be treated as IEEE 32bit float number for the purpose of alpha-test.</p>	Value	Name	Description	0h	ALPHATEST_UNORM8	UNorm8	1h	ALPHATEST_FLOAT32	Float32
Value	Name	Description									
0h	ALPHATEST_UNORM8	UNorm8									
1h	ALPHATEST_FLOAT32	Float32									
1	31:0	<p><b>Alpha Reference Value As UNORM8</b></p> <table border="1"> <tr> <td>Exists If:</td> <td>[Alpha Test Format] == 'ALPHATEST_UNORM8'</td> </tr> <tr> <td>Format:</td> <td>UNORM8 Upper 24 bits MBZ</td> </tr> </table> <p>This field specifies the alpha reference value to compare against in the Alpha Test function.</p>	Exists If:	[Alpha Test Format] == 'ALPHATEST_UNORM8'	Format:	UNORM8 Upper 24 bits MBZ					
Exists If:	[Alpha Test Format] == 'ALPHATEST_UNORM8'										
Format:	UNORM8 Upper 24 bits MBZ										

<b>COLOR_CALC_STATE</b>						
	31:0	<b>Alpha Reference Value As FLOAT32</b>				
		<table border="1"> <tr> <td>Exists If:</td><td>[Alpha Test Format] = 'ALPHATEST_FLOAT32'</td></tr> <tr> <td>Format:</td><td>IEEE_Float</td></tr> </table> <p>This field specifies the alpha reference value to compare against in the Alpha Test function.</p>	Exists If:	[Alpha Test Format] = 'ALPHATEST_FLOAT32'	Format:	IEEE_Float
Exists If:	[Alpha Test Format] = 'ALPHATEST_FLOAT32'					
Format:	IEEE_Float					
2	31:0	<b>Blend Constant Color Red</b>				
		<table border="1"> <tr> <td>Format:</td><td>IEEE_Float</td></tr> </table> <p>This field specifies the Red channel of the Constant Color used in Color Buffer Blending.</p>	Format:	IEEE_Float		
Format:	IEEE_Float					
3	31:0	<b>Blend Constant Color Green</b>				
		<table border="1"> <tr> <td>Format:</td><td>IEEE_Float</td></tr> </table> <p>This field specifies the Green channel of the Constant Color used in Color Buffer Blending.</p>	Format:	IEEE_Float		
Format:	IEEE_Float					
4	31:0	<b>Blend Constant Color Blue</b>				
		<table border="1"> <tr> <td>Format:</td><td>IEEE_Float</td></tr> </table> <p>This field specifies the Blue channel of the Constant Color used in Color Buffer Blending.</p>	Format:	IEEE_Float		
Format:	IEEE_Float					
5	31:0	<b>Blend Constant Color Alpha</b>				
		<table border="1"> <tr> <td>Format:</td><td>IEEE_Float</td></tr> </table> <p>This field specifies the Alpha channel of the Constant Color used in Color Buffer Blending.</p>	Format:	IEEE_Float		
Format:	IEEE_Float					

## COLOR\_PROCESSING\_STATE - ACE State

<b>COLOR_PROCESSING_STATE - ACE State</b>										
<b>DWord</b>	<b>Bit</b>	<b>Description</b>								
0	31:7	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ						
Format:	MBZ									
	6:2	<p><b>Skin Threshold</b></p> <table border="1"> <tr> <td>Format:</td> <td>U5</td> </tr> </table> <p>Used for Y analysis (min/max) for pixels which are higher than skin threshold.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>1-31</td> <td></td> </tr> <tr> <td>26</td> <td>[Default]</td> </tr> </tbody> </table>	Format:	U5	Value	Name	1-31		26	[Default]
Format:	U5									
Value	Name									
1-31										
26	[Default]									
	1	<p><b>Full Image Histogram</b></p> <table border="1"> <tr> <td>Default Value:</td> <td>0</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>Used to ignore the area of interest for full image histogram.</p>	Default Value:	0	Format:	Enable				
Default Value:	0									
Format:	Enable									
	0	<p><b>ACE Enable</b></p> <table border="1"> <tr> <td>Format:</td> <td>Enable</td> </tr> </table>	Format:	Enable						
Format:	Enable									
1	31:24	<p><b>Y3</b></p> <table border="1"> <tr> <td>Default Value:</td> <td>76</td> </tr> <tr> <td>Format:</td> <td>U8</td> </tr> </table> <p>The value of the y_pixel for point 3 in PWL.</p>	Default Value:	76	Format:	U8				
Default Value:	76									
Format:	U8									
	23:16	<p><b>Y2</b></p> <table border="1"> <tr> <td>Default Value:</td> <td>56</td> </tr> <tr> <td>Format:</td> <td>U8</td> </tr> </table> <p>The value of the y_pixel for point 2 in PWL.</p>	Default Value:	56	Format:	U8				
Default Value:	56									
Format:	U8									
	15:8	<p><b>Y1</b></p> <table border="1"> <tr> <td>Default Value:</td> <td>36</td> </tr> <tr> <td>Format:</td> <td>U8</td> </tr> </table> <p>The value of the y_pixel for point 1 in PWL.</p>	Default Value:	36	Format:	U8				
Default Value:	36									
Format:	U8									

COLOR_PROCESSING_STATE - ACE State		
	7:0	<b>Ymin</b> Default Value: 16 Format: U8 The value of the y_pixel for point 0 in PWL.
2	31:24	<b>Y7</b> Default Value: 156 Format: U8 The value of the y_pixel for point 7 in PWL.
		<b>Y6</b> Default Value: 136 Format: U8 The value of the y_pixel for point 6 in PWL.
	15:8	<b>Y5</b> Default Value: 116 Format: U8 The value of the y_pixel for point 5 in PWL.
		<b>Y4</b> Default Value: 96 Format: U8 The value of the y_pixel for point 4 in PWL.
3	31:24	<b>Ymax</b> Default Value: 235 Format: U8 The value of the y_pixel for point 11 in PWL.
		<b>Y10</b> Default Value: 216 Format: U8 The value of the y_pixel for point 10 in PWL.
	15:8	<b>Y9</b> Default Value: 196 Format: U8 The value of the y_pixel for point 9 in PWL.

<b>COLOR_PROCESSING_STATE - ACE State</b>						
	7:0	<b>Y8</b> <table border="1"> <tr> <td>Default Value:</td><td>176</td></tr> <tr> <td>Format:</td><td>U8</td></tr> </table> <p>The value of the y_pixel for point 8 in PWL.</p>	Default Value:	176	Format:	U8
Default Value:	176					
Format:	U8					
4	31:24	<b>B4</b> <table border="1"> <tr> <td>Default Value:</td><td>96</td></tr> <tr> <td>Format:</td><td>U8</td></tr> </table> <p>The value of the bias for point 4 in PWL.</p>	Default Value:	96	Format:	U8
Default Value:	96					
Format:	U8					
23:16	<b>B3</b> <table border="1"> <tr> <td>Default Value:</td><td>76</td></tr> <tr> <td>Format:</td><td>U8</td></tr> </table> <p>The value of the bias for point 3 in PWL.</p>	Default Value:	76	Format:	U8	
Default Value:	76					
Format:	U8					
15:8	<b>B2</b> <table border="1"> <tr> <td>Default Value:</td><td>56</td></tr> <tr> <td>Format:</td><td>U8</td></tr> </table> <p>The value of the bias for point 2 in PWL.</p>	Default Value:	56	Format:	U8	
Default Value:	56					
Format:	U8					
7:0	<b>B1</b> <table border="1"> <tr> <td>Default Value:</td><td>36</td></tr> <tr> <td>Format:</td><td>U8</td></tr> </table> <p>The value of the bias for point 1 in PWL.</p>	Default Value:	36	Format:	U8	
Default Value:	36					
Format:	U8					
5	31:24	<b>B8</b> <table border="1"> <tr> <td>Default Value:</td><td>176</td></tr> <tr> <td>Format:</td><td>U8</td></tr> </table> <p>The value of the bias for point 8 in PWL.</p>	Default Value:	176	Format:	U8
Default Value:	176					
Format:	U8					
23:16	<b>B7</b> <table border="1"> <tr> <td>Default Value:</td><td>156</td></tr> <tr> <td>Format:</td><td>U8</td></tr> </table> <p>The value of the bias for point 7 in PWL.</p>	Default Value:	156	Format:	U8	
Default Value:	156					
Format:	U8					
15:8	<b>B6</b> <table border="1"> <tr> <td>Default Value:</td><td>136</td></tr> <tr> <td>Format:</td><td>U8</td></tr> </table> <p>The value of the bias for point 6 in PWL.</p>	Default Value:	136	Format:	U8	
Default Value:	136					
Format:	U8					

COLOR_PROCESSING_STATE - ACE State		
	7:0	<b>B5</b> Default Value: 116 Format: U8 The value of the bias for point 5 in PWL.
6	31:16	<b>Reserved</b> Format: MBZ
	15:8	<b>B10</b> Default Value: 216 Format: U8 The value of the bias for point 10 in PWL.
	7:0	<b>B9</b> Default Value: 196 Format: U8 The value of the bias for point 9 in PWL.
7	31:27	<b>Reserved</b> Format: MBZ
	26:16	<b>S1</b> Format: U1.10 The value of the slope for point 1 in PWL. The default is 1024/1024.
	15:11	<b>Reserved</b> Format: MBZ
	10:0	<b>S0</b> Format: U1.10 The value of the slope for point 0 in PWL. The default is 1024/1024.
8	31:27	<b>Reserved</b> Format: MBZ
	26:16	<b>S3</b> Format: U1.10 The value of the slope for point 3 in PWL. The default is 1024/1024.
	15:11	<b>Reserved</b> Format: MBZ
	10:0	<b>S2</b> Format: U1.10 The value of the slope for point 2 in PWL. The default is 1024/1024.

<b>COLOR_PROCESSING_STATE - ACE State</b>			
9	31:27	<b>Reserved</b>	Format: MBZ
	26:16	<b>S5</b>	Format: U1.10 The value of the slope for point 5 in PWL. The default is 1024/1024.
	15:11	<b>Reserved</b>	Format: MBZ
	10:0	<b>S4</b>	Format: U1.10 The value of the slope for point 4 in PWL. The default is 1024/1024.
10	31:27	<b>Reserved</b>	Format: MBZ
	26:16	<b>S7</b>	Format: U1.10 The value of the slope for point 7 in PWL. The default is 1024/1024.
	15:11	<b>Reserved</b>	Format: MBZ
	10:0	<b>S6</b>	Format: U1.10 The value of the slope for point 6 in PWL. The default is 1024/1024.
11	31:27	<b>Reserved</b>	Format: MBZ
	26:16	<b>S9</b>	Format: U1.10 The value of the slope for point 9 in PWL. The default is 1024/1024.
	15:11	<b>Reserved</b>	Format: MBZ
	10:0	<b>S8</b>	Format: U1.10 The value of the slope for point 8 in PWL. The default is 1024/1024.
12	31:11	<b>Reserved</b>	Format: MBZ
	10:0	<b>S10</b>	Format: U1.10 The value of the slope for point 10 in PWL. The default is 1024/1024.

## COLOR\_PROCESSING\_STATE - CSC State

COLOR_PROCESSING_STATE - CSC State		
DWord	Bit	Description
0	31:29	<b>Reserved</b> Format: MBZ
	28:16	<b>C1</b> Default Value: 0 Format: S2.10 2's complement Transform coefficient
	15:3	<b>C0</b> Default Value: 1024 Format: S2.10 2's complement Transform coefficient
	2	<b>YUV_IN</b> Default Value: 0 Format: YUV CSC input offset enable.
	1	<b>YUV_OUT</b> Default Value: 0 Format: RGB CSC output offset enable.
	0	<b>Transform Enable</b> Format: Enable
	31:26	<b>Reserved</b> Format: MBZ
	25:13	<b>C3</b> Default Value: 0 Format: S2.10 2's complement Transform coefficient.

<b>COLOR_PROCESSING_STATE - CSC State</b>		
	12:0	<b>C2</b> Default Value: 0 Format: S2.10 2's complement Transform coefficient.
2	31:26	<b>Reserved</b> Format: MBZ
	25:13	<b>C5</b> Default Value: 0 Format: S2.10 2's complement Transform coefficient.
	12:0	<b>C4</b> Default Value: 1024 Format: S2.10 2's complement Transform coefficient.
	31:26	<b>Reserved</b> Format: MBZ
3	25:13	<b>C7</b> Default Value: 0 Format: S2.10 2's complement Transform coefficient.
	12:0	<b>C6</b> Default Value: 0 Format: S2.10 2's complement Transform coefficient.
	31:13	<b>Reserved</b> Format: MBZ
4	12:0	<b>C8</b> Default Value: 1204 Format: S2.10 2's complement Transform coefficient.
	31:20	<b>Reserved</b> Format: MBZ
5	19:10	<b>Offset out 1</b> Default Value: 0 Format: S9 2's complement Offset Out for Y/R.

COLOR_PROCESSING_STATE - CSC State													
	9:0	<p><b>Offset In 1</b></p> <table border="1"> <tr> <td>Default Value:</td><td>0</td></tr> <tr> <td>Format:</td><td>S9 2's complement</td></tr> </table> <p>Offset in for Y/R.</p>	Default Value:	0	Format:	S9 2's complement							
Default Value:	0												
Format:	S9 2's complement												
6	31:20	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ									
Format:	MBZ												
	19:10	<p><b>Offset out 2</b></p> <table border="1"> <tr> <td>Default Value:</td><td>0</td></tr> <tr> <td>Format:</td><td>S9 2's complement</td></tr> </table> <p>Offset out for U/G.</p>	Default Value:	0	Format:	S9 2's complement							
Default Value:	0												
Format:	S9 2's complement												
	9:0	<p><b>Offset in 2</b></p> <table border="1"> <tr> <td>Default Value:</td><td>0</td></tr> <tr> <td>Format:</td><td>S9 2's complement</td></tr> </table> <p>Offset in for U/G.</p>	Default Value:	0	Format:	S9 2's complement							
Default Value:	0												
Format:	S9 2's complement												
7	31:20	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ									
Format:	MBZ												
	19:10	<p><b>Offset out 3</b></p> <table border="1"> <tr> <td>Default Value:</td><td>0</td></tr> <tr> <td>Format:</td><td>S9 2's complement</td></tr> </table> <p>Offset out for V/B.</p>	Default Value:	0	Format:	S9 2's complement							
Default Value:	0												
Format:	S9 2's complement												
	9:0	<p><b>Offset in 3</b></p> <table border="1"> <tr> <td>Default Value:</td><td>0</td></tr> <tr> <td>Format:</td><td>S9 2's complement</td></tr> </table> <p>Offset in for V/B.</p>	Default Value:	0	Format:	S9 2's complement							
Default Value:	0												
Format:	S9 2's complement												
8	31:17	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ									
Format:	MBZ												
	16	<p><b>Alpha from State Select</b></p> <table border="1"> <tr> <td>Format:</td><td>U1 Enumerated Type</td></tr> </table> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0</td><td></td><td>Alpha is taken from message</td></tr> <tr> <td>1</td><td></td><td>Alpha is taken from state</td></tr> </tbody> </table>	Format:	U1 Enumerated Type	Value	Name	Description	0		Alpha is taken from message	1		Alpha is taken from state
Format:	U1 Enumerated Type												
Value	Name	Description											
0		Alpha is taken from message											
1		Alpha is taken from state											
	15:0	<p><b>Color Pipe Alpha</b></p> <table border="1"> <tr> <td>Format:</td><td>U16</td></tr> </table>	Format:	U16									
Format:	U16												

## COLOR\_PROCESSING\_STATE - PROCAMP State

<b>COLOR_PROCESSING_STATE - PROCAMP State</b>								
<b>DWord</b>	<b>Bit</b>	<b>Description</b>						
0	31:28	<b>Reserved</b> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ				
Format:	MBZ							
27:17	<b>Contrast</b> <table border="1"> <tr> <td>Default Value:</td> <td>1</td> </tr> <tr> <td>Format:</td> <td>U4.7</td> </tr> <tr> <td colspan="2">Contrast magnitude.</td></tr> </table>	Default Value:	1	Format:	U4.7	Contrast magnitude.		
Default Value:	1							
Format:	U4.7							
Contrast magnitude.								
16:13	<b>Reserved</b> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ					
Format:	MBZ							
12:1	<b>Brightness</b> <table border="1"> <tr> <td>Default Value:</td> <td>0</td> </tr> <tr> <td>Format:</td> <td>S7.4 2's complement</td> </tr> <tr> <td colspan="2">Brightness magnitude.</td></tr> </table>	Default Value:	0	Format:	S7.4 2's complement	Brightness magnitude.		
Default Value:	0							
Format:	S7.4 2's complement							
Brightness magnitude.								
0	<b>PROCAMP Enable</b> <table border="1"> <tr> <td>Default Value:</td> <td>1</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table>	Default Value:	1	Format:	Enable			
Default Value:	1							
Format:	Enable							
31:16	<b>Cos_c_s</b> <table border="1"> <tr> <td>Default Value:</td> <td>256</td> </tr> <tr> <td>Format:</td> <td>S7.8 2's complement</td> </tr> <tr> <td colspan="2">UV multiplication cosine factor.</td></tr> </table>	Default Value:	256	Format:	S7.8 2's complement	UV multiplication cosine factor.		
Default Value:	256							
Format:	S7.8 2's complement							
UV multiplication cosine factor.								
1	15:0	<b>Sin_c_s</b> <table border="1"> <tr> <td>Default Value:</td> <td>0</td> </tr> <tr> <td>Format:</td> <td>S7.8 2's complement</td> </tr> <tr> <td colspan="2">UV multiplication sine factor.</td></tr> </table>	Default Value:	0	Format:	S7.8 2's complement	UV multiplication sine factor.	
Default Value:	0							
Format:	S7.8 2's complement							
UV multiplication sine factor.								

## COLOR\_PROCESSING\_STATE - STD/STE State

COLOR_PROCESSING_STATE - STD/STE State							
Project:	BDW						
Size (in bits):	928						
Default Value:	0x9A6E39F0, 0x400C0000, 0x00001180, 0xFE2F2E00, 0x000000FF, 0x00140000, 0xD82E0000, 0x8285ECEC, 0x00008282, 0x00000000, 0x02117000, 0xA38FEC96, 0x00008CC8, 0x00000000, 0x01478000, 0x0007C300, 0x00000000, 0x00000000, 0x1C180000, 0x00000000, 0x00000000, 0x00000000, 0x00007CF80, 0x00000000, 0x00000000, 0x1C080000, 0x00000000, 0x00000000, 0x00000000						
This state structure contains the STD/STE state used by the color processing function.							
DWord	Bit	Description					
0	31:24	<p><b>V_Mid</b></p> <table border="1"> <tr> <td>Default Value:</td> <td>154</td> </tr> <tr> <td>Format:</td> <td>U8</td> </tr> </table> <p>Rectangle middle-point V coordinate</p>	Default Value:	154	Format:	U8	
Default Value:	154						
Format:	U8						
23:16	<p><b>U_Mid</b></p> <table border="1"> <tr> <td>Default Value:</td> <td>110</td> </tr> <tr> <td>Format:</td> <td>U8</td> </tr> </table> <p>Rectangle middle-point U coordinate</p>	Default Value:	110	Format:	U8		
Default Value:	110						
Format:	U8						
15:10	<p><b>Hue Max</b></p> <table border="1"> <tr> <td>Default Value:</td> <td>14</td> </tr> <tr> <td>Format:</td> <td>U6</td> </tr> </table> <p>Rectangle half width</p>	Default Value:	14	Format:	U6		
Default Value:	14						
Format:	U6						
9:4	<p><b>Sat Max</b></p> <table border="1"> <tr> <td>Default Value:</td> <td>31</td> </tr> <tr> <td>Format:</td> <td>U6</td> </tr> </table> <p>Rectangle half length.</p>	Default Value:	31	Format:	U6		
Default Value:	31						
Format:	U6						
3	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ				
Format:	MBZ						
2	<p><b>Output Control</b></p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0</td><td>Output Pixels <b>[Default]</b></td></tr> <tr> <td>1</td><td>Output STD Decisions</td></tr> </tbody> </table>	Value	Name	0	Output Pixels <b>[Default]</b>	1	Output STD Decisions
Value	Name						
0	Output Pixels <b>[Default]</b>						
1	Output STD Decisions						
1	<p><b>STE Enable</b></p> <table border="1"> <tr> <td>Format:</td> <td>Enable</td> </tr> </table>	Format:	Enable				
Format:	Enable						
0	<p><b>STD Enable</b></p> <table border="1"> <tr> <td>Format:</td> <td>Enable</td> </tr> </table>	Format:	Enable				
Format:	Enable						

<b>COLOR_PROCESSING_STATE - STD/STE State</b>		
1	31	<b>Reserved</b> Format: MBZ
	30:28	<b>Diamond Margin</b> Default Value: 4 Format: U3
	27:21	<b>Diamond du</b> Default Value: 0 Format: S6 2's complement Rhombus center shift in the sat-direction, relative to the rectangle center.
	20:18	<b>HS Margin</b> Default Value: 3 Format: U3
	17:10	<b>Cos(α)</b> Format: S0.7 2's Compliment The default is 79/128
	9:8	<b>Reserved</b> Format: MBZ
	7:0	<b>Sin(α)</b> Format: S0.7 2's Compliment The default is 101/128
	31:21	<b>Reserved</b> Format: MBZ
	20:13	<b>Diamond Alpha</b> Format: U2.6 1 / tan(β) The default is 100/64
2	12:7	<b>Diamond Th</b> Default Value: 35 Format: U6 Half length of the rhombus axis in the sat-direction.
	6:0	<b>Diamond dv</b> Default Value: 0 Format: S6 2's complement
	31:24	<b>Y_point_3</b> Default Value: 254 Format: U8 Third point of the Y piecewise linear membership function.

## COLOR\_PROCESSING\_STATE - STD/STE State

	23:16	<b>Y_point_2</b>	Default Value:	47	
		Format:		U8	
Second point of the Y piecewise linear membership function.					
	15:8	<b>Y_point_1</b>	Default Value:	46	
		Format:		U8	
First point of the Y piecewise linear membership function.					
	7	<b>VY_STD_Enable</b>	Format:	Enable	
Enables STD in the VY subspace.					
	6:0	<b>Reserved</b>	Format:	MBZ	
4	31:18	<b>Reserved</b>	Format:	MBZ	
	17:13	<b>Y_Slope_2</b>	Format:	U2.3	
		Slope between points Y3 and Y4. The default is 31/8.			
	12:8	<b>Y_Slope_1</b>	Format:	U2.3	
Slope between points Y1 and Y2. The default is 31/8.					
5	7:0	<b>Y_point_4</b>	Default Value:	255	
		Format:		U8	
	Fourth point of the Y piecewise linear membership function				
	31:16	<b>INV_skin_types_margin</b>	Format:	U0.16	
1/(2* Skin_types_margin)					
		<b>Value</b>	<b>Name</b>	<b>Description</b>	
	20	[Default]		Skin_Type_margin	
	15:0	<b>Inverse Margin VYL</b>	Format:	U0.16	
		1 / Margin_VYL The default is 3300/65536			

<b>COLOR_PROCESSING_STATE - STD/STE State</b>			
6	31:24	<b>P1L</b>	
		Default Value:	216
	23:16	Format:	U8
Y Point 1 of the lower part of the detection PWLF.			
7	31:24	<b>POL</b>	
		Default Value:	46
	23:16	Format:	U8
Y Point 0 of the lower part of the detection PWLF.			
15:0	<b>Inverse Margin VYU</b>		
	Format:	U0.16	
1 / Margin_VYU The default is 1600/65536.			
8	31:24	<b>B1L</b>	
		Default Value:	130
	23:16	Format:	U8
V Bias 1 of the lower part of the detection PWLF.			
7	31:24	<b>B0L</b>	
		Default Value:	133
	23:16	Format:	U8
V Bias 0 of the lower part of the detection PWLF.			
15:8	<b>P3L</b>		
	Default Value:	236	
	Format:	U8	
Y Point 3 of the lower part of the detection PWLF.			
8	7:0	<b>P2L</b>	
		Default Value:	236
	7:0	Format:	U8
Y point 2 of the lower part of the detection PWLF.			
31:27	<b>Reserved</b>		
	Format:	MBZ	
26:16	<b>S0L</b>		
	Format:	S2.8 2's complement	
Slope 0 of the lower part of the detection PWLF. The default is -5/256.			

COLOR_PROCESSING_STATE - STD/STE State			
	15:8	<b>B3L</b>	
		Default Value:	130
		Format:	U8
		V Bias 3 of the lower part of the detection PWLF.	
	7:0	<b>B2L</b>	
		Default Value:	130
		Format:	U8
		V Bias 2 of the lower part of the detection PWLF.	
9	31:22	<b>Reserved</b>	
		Format:	MBZ
9	21:11	<b>S2L</b>	
		Format:	S2.8 2's complement
		Slope 2 of the lower part of the detection PWLF. The default is 0/256.	
9	10:0	<b>S1L</b>	
		Format:	S2.8 2's complement
		Slope 1 of the lower part of the detection PWLF. The default is 0/256.	
10	31:27	<b>Reserved</b>	
		Format:	MBZ
10	26:19	<b>P1U</b>	
		Default Value:	66
		Format:	U8
		Y Point 1 of the upper part of the detection PWLF.	
10	18:11	<b>P0U</b>	
		Default Value:	46
		Format:	U8
		Y Point 0 of the upper part of the detection PWLF.	
10	10:0	<b>S3L</b>	
		Format:	S2.8 2's complement
		Slope 3 of the lower part of the detection PWLF. The default is 0/256.	
11	31:24	<b>B1U</b>	
		Default Value:	163
		Format:	U8
		V Bias 1 of the upper part of the detection PWLF.	

<b>COLOR_PROCESSING_STATE - STD/STE State</b>			
	23:16	<b>B0U</b>	
		Default Value:	143
		Format:	U8
		V Bias 0 of the upper part of the detection PWLF.	
	15:8	<b>P3U</b>	
		Default Value:	236
		Format:	U8
		Y Point 3 of the upper part of the detection PWLF.	
	7:0	<b>P2U</b>	
		Default Value:	150
		Format:	U8
		Y Point 2 of the upper part of the detection PWLF.	
12	31:27	<b>Reserved</b>	
		Format:	MBZ
	26:16	<b>S0U</b>	
		Format:	S2.8 2's complement
		Slope 0 of the upper part of the detection PWLF. The default is 256/256.	
	15:8	<b>B3U</b>	
		Default Value:	140
		Format:	U8
		V Bias 3 of the upper part of the detection PWLF.	
	7:0	<b>B2U</b>	
		Default Value:	200
		Format:	U8
		V Bias 2 of the upper part of the detection PWLF.	
13	31:22	<b>Reserved</b>	
		Format:	MBZ
	21:11	<b>S2U</b>	
		Format:	S2.8 2's complement
		Slope 2 of the upper part of the detection PWLF. The default is -179/256.	
	10:0	<b>S1U</b>	
		Format:	S2.8 2's complement
		Slope 1 of the upper part of the detection PWLF. The default is -113/256.	

COLOR_PROCESSING_STATE - STD/STE State								
14	31:28	<b>Reserved</b>	Format: MBZ					
	27:20	<b>Skin Types Margin</b>	Default Value: 20 Format: U8 Skin types Y margin.					
	19:12	<b>Skin Types Thresh</b>	Default Value: 120 Format: U8 Skin types Y threshold.					
	11	<b>Skin Type Enable</b>	Format: Enable Treat differently bright and dark skin types. <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0</td><td>[Default]</td><td>Disable</td></tr> </tbody> </table>	Value	Name	Description	0	[Default]
Value	Name	Description						
0	[Default]	Disable						
10:0	<b>S3U</b>	Format: S2.8 2's complement Slope 3 of the upper part of the detection PWLF. The default is 0/256.						
31	<b>Reserved</b>	Format: MBZ						
30:21	<b>SATB1</b>	Format: S7.2 2's complement First bias for the saturation PWLF (bright skin). The default is -8/4.						
20:14	<b>SATP3</b>	Default Value: 31 Format: S6 2's complement Third point for the saturation PWLF (bright skin).						
13:7	<b>SATP2</b>	Default Value: 6 Format: S6 2's complement Second point for the saturation PWLF (bright skin).						
6:0	<b>SATP1</b>	Format: S6 2's complement First point for the saturation PWLF (bright skin). The default is -6.						

<b>COLOR_PROCESSING_STATE - STD/STE State</b>		
16	31	<b>Reserved</b> Format: MBZ
	30:20	<b>SATSO</b> Format: U3.8 Zeroth slope for the saturation PWLF (bright skin). The default is 297/256.
	19:10	<b>SATB3</b> Format: S7.2 2's complement Third bias for the saturation PWLF (bright skin). The default is 124/4.
	9:0	<b>SATB2</b> Format: S7.2 2's complement Second bias for the saturation PWLF (bright skin). The default is 8/4.
17	31:22	<b>Reserved</b> Format: MBZ
	21:11	<b>SATS2</b> Format: U3.8 Second slope for the saturation PWLF (bright skin). The default is 297/256.
	10:0	<b>SATS1</b> Format: U3.8 First slope for the saturation PWLF (bright skin). The default is 85/256.
18	31:25	<b>HUEP3</b> Default Value: 14 Format: S6 2's complement Third point for the hue PWLF (bright skin)
	24:18	<b>HUEP2</b> Default Value: 6 Format: S6 2's complement Second point for the hue PWLF (bright skin)
	17:11	<b>HUEP1</b> Format: S6 2's complement First point for the hue PWLF (bright skin). The default is -6.

COLOR_PROCESSING_STATE - STD/STE State			
	10:0	<b>SATS3</b>	
		Format:	U3.8
		Third slope for the saturation PWLF (bright skin). The default is 256/256.	
19	31:30	<b>Reserved</b>	
		Format:	MBZ
	29:20	<b>HUEB3</b>	
		Format:	S7.2 2's complement
		Third bias for the hue PWLF (bright skin). The default is 56/4.	
	19:10	<b>HUEB2</b>	
		Format:	S7.2 2's complement
		Second bias for the hue PWLF (bright skin). The default is 8/4.	
	9:0	<b>HUEB1</b>	
		Format:	S7.2 2's complement
		First bias for the hue PWLF (bright skin). The default is -8/4.	
20	31:22	<b>Reserved</b>	
		Format:	MBZ
	21:11	<b>HUES1</b>	
		Format:	U3.8
		First slope for the hue PWLF (bright skin) The default is 85/256.	
	10:0	<b>HUES0</b>	
		Format:	U3.8
		Zeroth slope for the hue PWLF (bright skin) The default is 384/256.	
21	31:22	<b>Reserved</b>	
		Format:	MBZ
	21:11	<b>HUES3</b>	
		Format:	U3.8
		Third slope for the hue PWLF (bright skin) The default is 256/256.	
	10:0	<b>HUES2</b>	
		Format:	U3.8
		Second slope for the hue PWLF (bright skin) The default is 384/256.	

<b>COLOR_PROCESSING_STATE - STD/STE State</b>		
22	31	<b>Reserved</b> Format: MBZ
	30:21	<b>SATB1_DARK</b> Format: S7.2 2's complement First bias for the saturation PWLF (dark skin) The default is 0/4.
	20:14	<b>SATP3_DARK</b> Default Value: 31 Format: S6 2's complement Third point for the saturation PWLF (dark skin)
	13:7	<b>SATP2_DARK</b> Default Value: 31 Format: S6 2's complement Second point for the saturation PWLF (dark skin)
	6:0	<b>SATP1_DARK</b> Format: S6 2's complement First point for the saturation PWLF (dark skin). The default is -11.
	31	<b>Reserved</b> Format: MBZ
23	30:20	<b>SATSO_DARK</b> Format: U3.8 Zeroth slope for the saturation PWLF (dark skin). The default is 397/256.
	19:10	<b>SATB3_DARK</b> Format: S7.2 2's complement Third bias for the saturation PWLF (dark skin). The default is 124/4.
	9:0	<b>SATB2_DARK</b> Format: S7.2 2's complement Second bias for the saturation PWLF (dark skin). The default is 124/4.
	31:22	<b>Reserved</b> Format: MBZ
24	21:11	<b>SATS2_DARK</b> Format: U3.8 Second slope for the saturation PWLF (dark skin). The default is 256/256.

<b>COLOR_PROCESSING_STATE - STD/STE State</b>			
	10:0	<b>SATS1_DARK</b>	
		Format:	U3.8
		First slope for the saturation PWLF (dark skin). The default is 189/256.	
25	31:25	<b>HUEP3_DARK</b>	
		Default Value:	14
		Format:	S6 2's complement
		Third point for the hue PWLF (dark skin).	
	24:18	<b>HUEP2_DARK</b>	
		Default Value:	2
		Format:	S6 2's complement
		Third point for the hue PWLF (dark skin).	
	17:11	<b>HUEP1_DARK</b>	
		Default Value:	0
		Format:	S6 2's complement
		Third point for the hue PWLF (dark skin).	
	10:0	<b>SATS3_DARK</b>	
		Format:	U3.8
		Third slope for the saturation PWLF (dark skin). The default is 256/256.	
26	31:30	<b>Reserved</b>	
		Format:	MBZ
	29:20	<b>HUEB3_DARK</b>	
		Format:	S7.2 2's complement
		Third bias for the hue PWLF (dark skin). The default is 56/4.	
	19:10	<b>HUEB2_DARK</b>	
		Format:	S7.2 2's complement
		Second bias for the hue PWLF (dark skin). The default is 0/4.	
	9:0	<b>HUEB1_DARK</b>	
		Format:	S7.2 2's complement
		First bias for the hue PWLF (dark skin). The default is 0/4.	
27	31:22	<b>Reserved</b>	
		Format:	MBZ

<b>COLOR_PROCESSING_STATE - STD/STE State</b>		
	21:11	<b>HUES1_DARK</b> Format: U3.8 First slope for the hue PWLF (dark skin). The default is 0/256.
	10:0	<b>HUES0_DARK</b> Format: U3.8 Zeroth slope for the hue PWLF (dark skin). The default is 256/256.
28	31:22	<b>Reserved</b> Format: MBZ
	21:11	<b>HUES3_DARK</b> Format: U3.8 Third slope for the hue PWLF (dark skin). The default is 256/256.
	10:0	<b>HUES2_DARK</b> Format: U3.8 Second slope for the hue PWLF (dark skin). The default is 299/256.

## COLOR\_PROCESSING\_STATE - TCC State

COLOR_PROCESSING_STATE - TCC State		
DWord	Bit	Description
0	31:24	<b>SatFactor3</b> Default Value: 220 Format: U1.7 The saturation factor for yellow.
	23:16	<b>SatFactor2</b> Default Value: 220 Format: U1.7 The saturation factor for red.
	15:8	<b>SatFactor1</b> Default Value: 220 Format: U1.7 The saturation factor for magenta.
	7	<b>TCC Enable</b> Format: Enable
	6:0	<b>Reserved</b> Format: MBZ
1	31:24	<b>SatFactor6</b> Default Value: 220 Format: U1.7 The saturation factor for blue.
	23:16	<b>SatFactor5</b> Default Value: 220 Format: U1.7 The saturation factor for cyan.

<b>COLOR_PROCESSING_STATE - TCC State</b>				
	15:8	<b>SatFactor4</b>		
		Default Value:	220	
	7:0	<b>Reserved</b>		
		Format:	MBZ	
	31:30	<b>Reserved</b>		
		Format:	MBZ	
	29:20	<b>Base Color 3</b>		
		Default Value:	483	
	19:10	<b>Base Color 2</b>		
		Default Value:	307	
		Format:	U10	
	9:0	<b>Base Color 1</b>		
		Default Value:	145	
		Format:	U10	
	31:30	<b>Reserved</b>		
		Format:	MBZ	
	29:20	<b>Base Color 6</b>		
		Default Value:	995	
		Format:	U10	
	19:10	<b>Base Color 5</b>		
		Default Value:	819	
		Format:	U10	
9:0	<b>Base Color 4</b>			
	Default Value:	657		
	Format:	U10		
	31:16	<b>Color Transit Slope 23</b>		
		Default Value:	744	
		Format:	U0.16	
		The calculation result of 1 / (BC3 - BC2) [1/62]		

COLOR_PROCESSING_STATE - TCC State						
	15:0	<p><b>Color Transit Slope 12</b></p> <table border="1"> <tr> <td>Default Value:</td><td>405</td></tr> <tr> <td>Format:</td><td>U0.16</td></tr> </table> <p>The calculation result of <math>1 / (\text{BC}2 - \text{BC}1)</math> [1/57]</p>	Default Value:	405	Format:	U0.16
Default Value:	405					
Format:	U0.16					
5	31:16	<p><b>Color Transit Slope 45</b></p> <table border="1"> <tr> <td>Default Value:</td><td>407</td></tr> <tr> <td>Format:</td><td>U0.16</td></tr> </table> <p>The calculation result of <math>1 / (\text{BC}5 - \text{BC}4)</math> [1/57]</p>	Default Value:	407	Format:	U0.16
Default Value:	407					
Format:	U0.16					
	15:0	<p><b>Color Transit Slope 34</b></p> <table border="1"> <tr> <td>Default Value:</td><td>1131</td></tr> <tr> <td>Format:</td><td>U0.16</td></tr> </table> <p>The calculation result of <math>1 / (\text{BC}4 - \text{BC}3)</math> [1/61]</p>	Default Value:	1131	Format:	U0.16
Default Value:	1131					
Format:	U0.16					
6	31:16	<p><b>Color Transit Slope 61</b></p> <table border="1"> <tr> <td>Default Value:</td><td>377</td></tr> <tr> <td>Format:</td><td>U0.16</td></tr> </table> <p>The calculation result of <math>1 / (\text{BC}1 - \text{BC}6)</math> [1/62]</p>	Default Value:	377	Format:	U0.16
Default Value:	377					
Format:	U0.16					
	15:0	<p><b>Color Transit Slope 56</b></p> <table border="1"> <tr> <td>Default Value:</td><td>372</td></tr> <tr> <td>Format:</td><td>U0.16</td></tr> </table> <p>The calculation result of <math>1 / (\text{BC}6 - \text{BC}5)</math> [1/62]</p>	Default Value:	372	Format:	U0.16
Default Value:	372					
Format:	U0.16					
7	31:22	<p><b>Color Bias 3</b></p> <table border="1"> <tr> <td>Default Value:</td><td>0</td></tr> <tr> <td>Format:</td><td>U2.8</td></tr> </table> <p>Color bias for BaseColor3.</p>	Default Value:	0	Format:	U2.8
Default Value:	0					
Format:	U2.8					
	21:12	<p><b>Color Bias 2</b></p> <table border="1"> <tr> <td>Default Value:</td><td>150</td></tr> <tr> <td>Format:</td><td>U2.8</td></tr> </table> <p>Color bias for BaseColor2.</p>	Default Value:	150	Format:	U2.8
Default Value:	150					
Format:	U2.8					
	11:2	<p><b>Color Bias 1</b></p> <table border="1"> <tr> <td>Default Value:</td><td>0</td></tr> <tr> <td>Format:</td><td>U2.8</td></tr> </table> <p>Color bias for BaseColor1.</p>	Default Value:	0	Format:	U2.8
Default Value:	0					
Format:	U2.8					

<b>COLOR_PROCESSING_STATE - TCC State</b>			
	1:0	<b>Reserved</b>	
		Format:	MBZ
8	31:22	<b>Color Bias 6</b>	
		Default Value:	0
		Format:	U2.8
		Color bias for BaseColor6.	
	21:12	<b>Color Bias 5</b>	
		Default Value:	0
		Format:	U2.8
		Color bias for BaseColor5.	
	11:2	<b>ColorBias4</b>	
		Default Value:	0
		Format:	U2.8
		Color bias for BaseColor4.	
	1:0	<b>Reserved</b>	
		Format:	MBZ
9	31	<b>Reserved</b>	
		Format:	MBZ
	30:24	<b>UV Threshold</b>	
		Default Value:	3
		Format:	U7
		Low UV threshold.	
	23:19	<b>Reserved</b>	
		Format:	MBZ
	18:16	<b>UV Threshold Bits</b>	
		Default Value:	3
		Format:	U3
		Low UV transition width bits.	
	15:13	<b>Reserved</b>	
		Format:	MBZ

COLOR_PROCESSING_STATE - TCC State			
	12:8	<b>STE Threshold</b>	
		Default Value:	0
		Format:	U5
Skin tone pixels enhancement threshold.			
	7:3	<b>Reserved</b>	
		Format:	MBZ
	2:0	<b>STE Slope Bits</b>	
		Default Value:	0
		Format:	U3
Skin tone pixels enhancement slope bits.			
	10	<b>Inverse UVMax Color</b>	
		Default Value:	146
		Format:	U0.16
1 / UVMaxColor. Used for the SFs2 calculation.			
	15:9	<b>Reserved</b>	
		Format:	MBZ
	8:0	<b>UVMax Color</b>	
		Default Value:	448
		Format:	U9
The maximum absolute value of the legal UV pixels. Used for the SFs2 calculation.			

## Color Calculator State Pointer Message Header Control

<b>MHC_RT_CCSP - Color Calculator State Pointer Message Header Control</b>						
<b>DWord</b>	<b>Bit</b>	<b>Description</b>				
0	31:6	<p><b>Color Calculator State Pointer</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>GeneralStateOffset[31:6]</td> </tr> </table> <p>Specifies the 64-byte aligned point to the color calculator state. This pointer is relative to the General State Base Address.</p>	Project:	All	Format:	GeneralStateOffset[31:6]
Project:	All					
Format:	GeneralStateOffset[31:6]					
	5:0	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Ignore</td> </tr> </table> <p>Ignored</p>	Project:	All	Format:	Ignore
Project:	All					
Format:	Ignore					

## Color Code Message Header Control

MHC_RT_CC - Color Code Message Header Control								
DWord	Bit	Description						
0	31:10	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Ignore</td> </tr> <tr> <td colspan="2">Ignored</td></tr> </table>	Project:	All	Format:	Ignore	Ignored	
Project:	All							
Format:	Ignore							
Ignored								
	9:8	<p><b>Color Code</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U2</td> </tr> </table> <p>This ID is assigned by the Windower unit and is used to track synchronizing events. Reserved for HW implementation use</p>	Project:	All	Format:	U2		
Project:	All							
Format:	U2							
	7:0	<p><b>FTTID</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U8</td> </tr> </table> <p>This ID is assigned by the fixed function unit and is a unique identifier for the thread. It is used to free up resources used by the thread upon thread completion.</p>	Project:	All	Format:	U8		
Project:	All							
Format:	U8							

## Context Descriptor Format

Context Descriptor Format												
DWord	Bit	Description										
0	63:32	<p><b>Context ID</b></p> <table border="1"> <thead> <tr> <th colspan="2">Description</th> </tr> </thead> <tbody> <tr> <td colspan="2">Context ID is a unique field assigned by GFX driver when a new context is created by which it is identified across all hierarchies of SW and HW.</td> </tr> <tr> <td colspan="2"> <ul style="list-style-type: none"> <li>• Context ID is used for semaphore signaling by hardware and software.</li> <li>• Context ID matching is used by hardware to detect Lite Restore.</li> <li>• Context ID is used by hardware for page fault reporting and response with IOMMU.</li> <li>• Context switch reason and the associated Context ID are reported to Context Switch Status Buffer by hardware on a context switch.</li> </ul> </td> </tr> </tbody> </table> <p>Context ID which is a 32 bit field is further divided in to three segments described below:</p> <ul style="list-style-type: none"> <li>• <b>Bits[63:55] (Bits 31:23 of Context ID)</b> is referred to as GroupID. GroupId+PASID combination of a context must be a unique identifier for contexts that are active in the system. The definition of active context is listed as:           <ul style="list-style-type: none"> <li>• Any Context that is already submitted to h/w or already running in h/w.</li> <li>• Any Context that hit page faults, was preempted (didn't run to context complete), and is waiting to be resubmitted pending IOMMU "last in group" response.</li> <li>• Any Context that has experienced reset but not all faults are responded to.</li> </ul> </li> <li>• <b>Bit[54] (Bit 22 of Context ID)</b> – MBZ for SW programming; this bit is used by hardware to distinguish between F&amp;H vs F&amp;S page requests and response messages to and from IOMMU. This bit is used by hardware on receiving page response to properly manage the page fault counters</li> <li>• <b>Bit[53] (Bit 21 of Context ID)</b> – MBZ from SW programming, is reserved for future hardware use.</li> <li>• <b>Bits[52:32] (Bits 20:0 of Context ID)</b> are for software use-only and must be unique field assigned by GFX driver when a new context is created.</li> </ul> <p><b>Logical Ring Context Address (LRCA)</b></p> <table border="1"> <thead> <tr> <th>Format:</th><th>GraphicsAddress[31:12]</th></tr> </thead> <tbody> <tr> <td colspan="2">This field contains the 4 KB-aligned address of the Logical Ring Context associated with this execlist element. LRCA must be always programmed in GGTT memory.</td></tr> </tbody> </table>	Description		Context ID is a unique field assigned by GFX driver when a new context is created by which it is identified across all hierarchies of SW and HW.		<ul style="list-style-type: none"> <li>• Context ID is used for semaphore signaling by hardware and software.</li> <li>• Context ID matching is used by hardware to detect Lite Restore.</li> <li>• Context ID is used by hardware for page fault reporting and response with IOMMU.</li> <li>• Context switch reason and the associated Context ID are reported to Context Switch Status Buffer by hardware on a context switch.</li> </ul>		Format:	GraphicsAddress[31:12]	This field contains the 4 KB-aligned address of the Logical Ring Context associated with this execlist element. LRCA must be always programmed in GGTT memory.	
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Format:	GraphicsAddress[31:12]											
This field contains the 4 KB-aligned address of the Logical Ring Context associated with this execlist element. LRCA must be always programmed in GGTT memory.												

Context Descriptor Format																	
11:9	<b>Reserved</b>																
	Format:																
8	<b>Privilege Access</b>																
	This field when set indicates PPGTT enabled in legacy context mode. In advanced context mode this field is reserved and must be zero.																
7:6	<b>Fault Handling</b>																
	Project:	BDW															
	Source:	RenderCS															
	<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0h</td><td>Fault and Hang</td><td>Fault model is not supported and fault occurrence is treated as catastrophic. GAM indicates Fault Error to Command streamer. Fault Error interrupt is reported to scheduler. Command Streamer will not initiate context switch on occurrence of Fault Error.</td></tr> <tr> <td>1h</td><td>Reserved</td><td>Reserved</td></tr> <tr> <td>2h</td><td>Reserved</td><td></td></tr> <tr> <td>3h</td><td>Reserved</td><td></td></tr> </tbody> </table>		Value	Name	Description	0h	Fault and Hang	Fault model is not supported and fault occurrence is treated as catastrophic. GAM indicates Fault Error to Command streamer. Fault Error interrupt is reported to scheduler. Command Streamer will not initiate context switch on occurrence of Fault Error.	1h	Reserved	Reserved	2h	Reserved		3h	Reserved	
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1h	Reserved	Reserved															
2h	Reserved																
3h	Reserved																
	<b>Programming Notes</b>																
	When execlist mode is set to "Legacy Context mode" Fault Handling mode must be set to "Fault and Hang."																
7:6	<b>Reserved</b>																
	Project:	BDW															
	Source:	BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS															
	Format:	MBZ															
5	<b>Reserved</b>																
	Project:	BDW															

## Context Descriptor Format

<b>Addressing Mode &amp; Legacy Context</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Project:</td><td style="padding: 2px;">BDW</td></tr> <tr> <td style="padding: 2px;">Format:</td><td style="padding: 2px;">U2</td></tr> </table> <p>Legacy context set indicates GPU is operating in legacy context mode of operation and doesn't support any SVM features. Legacy context reset indicates GPU is operating in advanced context mode of operation and support SVM features. Based on the Context mode set Addressing mode is interpreted appropriately. The table below summarizes the combinations supported.</p> <p>GFX engine always uses 32b virtual addressing mode when translated using GGTT irrespective of below options.</p>		Project:	BDW	Format:	U2											
Project:	BDW															
Format:	U2															
4:3	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 10%;">Value</th><th style="width: 10%;">Name</th><th style="width: 80%;">Description</th></tr> </thead> <tbody> <tr> <td style="padding: 2px;">00b</td><td style="padding: 2px;">Advanced Context with no A/D support</td><td style="padding: 2px;">GPU is enabled for advanced context mode and supports SVM features. GPU DOESN'T support Access and Dirty bit management in page tables. GPU supports 64b(48bit canonical) PPGTT graphics virtual addressing. PDP0_DESCRIPTOR contains the PASID (process address space identifier) and other PDP Descriptors are ignored.</td></tr> <tr> <td style="padding: 2px;">01b</td><td style="padding: 2px;">Legacy Context with no 64 bit VA support</td><td style="padding: 2px;">GPU is enabled for legacy context mode of operation and DOESN'T support any SVM features. GPU supports 32b PPGTT graphics virtual addressing. PDP*_descriptor contains the base address to 4GB of memory space supported.</td></tr> <tr> <td style="padding: 2px;">10b</td><td style="padding: 2px;">Advanced Context with A/D support</td><td style="padding: 2px;">GPU is enabled for advanced context mode and supports SVM features. GPU DOES support Access and Dirty bit management in page tables. GPU supports 64b (48bit canonical) PPGTT graphics virtual addressing. PDP0_DESCRIPTOR contains the PASID (process address space identifier) and other PDP Descriptors are ignored.</td></tr> <tr> <td style="padding: 2px;">11b</td><td style="padding: 2px;">Legacy Context with 64 bit VA support</td><td style="padding: 2px;">GPU is enabled for legacy context mode of operation and DOESN'T support any SVM features. GPU supports 64b (48bit canonical) PPGTT graphics virtual addressing and PDP0_DESCRIPTOR contains the base address to PML4 and other PDP Descriptors are ignored.</td></tr> </tbody> </table>	Value	Name	Description	00b	Advanced Context with no A/D support	GPU is enabled for advanced context mode and supports SVM features. GPU DOESN'T support Access and Dirty bit management in page tables. GPU supports 64b(48bit canonical) PPGTT graphics virtual addressing. PDP0_DESCRIPTOR contains the PASID (process address space identifier) and other PDP Descriptors are ignored.	01b	Legacy Context with no 64 bit VA support	GPU is enabled for legacy context mode of operation and DOESN'T support any SVM features. GPU supports 32b PPGTT graphics virtual addressing. PDP*_descriptor contains the base address to 4GB of memory space supported.	10b	Advanced Context with A/D support	GPU is enabled for advanced context mode and supports SVM features. GPU DOES support Access and Dirty bit management in page tables. GPU supports 64b (48bit canonical) PPGTT graphics virtual addressing. PDP0_DESCRIPTOR contains the PASID (process address space identifier) and other PDP Descriptors are ignored.	11b	Legacy Context with 64 bit VA support	GPU is enabled for legacy context mode of operation and DOESN'T support any SVM features. GPU supports 64b (48bit canonical) PPGTT graphics virtual addressing and PDP0_DESCRIPTOR contains the base address to PML4 and other PDP Descriptors are ignored.
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2	<p><b>Force Restore</b></p> <p>Setting this bit will force a context restore operation when switching to this context even if the LRCA in the CCID register (normally the LRCA of the last context from the prior execlist) matches this one.</p> <p>Note that it is legal (and likely desirable) for the <b>Render Context Restore Inhibit</b> bit (part of the CTXT_SR_CTL register) in the context image being restored to also be set. The "ring" context is being forced to be restored from a newly initialized context despite a possible LRCA match. However, the render context for such a newly initialized context will likely be uninitialized and so should not be restored.</p>															
1	<p><b>Force PD Restore</b></p> <p>Setting this bit will cause the on-chip page directory to be reloaded from the PD image in memory even on an LRCA match. No other operations of context restore will occur on an LRCA match, however. Software should set this bit if it has updated a context's page directory and wants the context to begin using the new page directory without having to switch away from it (to another context) and back again. Setting this bit will have no effect if <b>Force Restore</b> is also set; a complete context restore (including the PD) will be performed.</p>															

## Context Descriptor Format

	0	<b>Valid</b> Set if this register holds a valid context descriptor. SW should set this bit in the Element registers that it has set up to contain valid context descriptors. Any execlist elements that are not used in a submitted execlist must have this bit clear.
--	---	---

## Context Status

Context Status						
DWord	Bit	Description				
0	63:32	<b>Context ID</b> <table border="1"> <tr> <td>Format:</td> <td>U32</td> </tr> </table>	Format:	U32		
Format:	U32					
	31:30	<b>Reserved</b> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ		
Format:	MBZ					
	29	<b>Reserved</b> <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	BDW	Format:	MBZ
Project:	BDW					
Format:	MBZ					
	28	<b>Reserved</b> <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> </table>	Project:	BDW		
Project:	BDW					
	27:25	<b>Reserved</b> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ		
Format:	MBZ					
	24:20	<b>Reserved</b> <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	BDW	Format:	MBZ
Project:	BDW					
Format:	MBZ					
	19:16	<b>Reserved</b> <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	BDW	Format:	MBZ
Project:	BDW					
Format:	MBZ					
	15	<b>Lite Restore</b> <table border="1"> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>This bit is only valid only when Preempted bit is set. When set, this bit indicates that a given context got preempted with the same context resulting in Lite Restore in HW.</p>	Format:	Enable		
Format:	Enable					

Context Status																
14:12	<b>Display Plane</b>															
Project: BDW																
This indicates the display plane for which Wait on Scanline/V-Blank/Sync Flip has been executed leading to context switch. This field is only valid when one of the "Wait on Scanline" or "Wait on VBlank" or "Wait on sync Flip" is set.																
<table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0h</td><td>Display Plane-A</td></tr> <tr> <td>1h</td><td>Display Plane-B</td></tr> <tr> <td>2h</td><td>Display Plane-C</td></tr> <tr> <td>3h</td><td>Display Plane Sprite A</td></tr> <tr> <td>4h</td><td>Display Plane Sprite B</td></tr> <tr> <td>5h</td><td>Display Plane Sprite C</td></tr> </tbody> </table>			Value	Name	0h	Display Plane-A	1h	Display Plane-B	2h	Display Plane-C	3h	Display Plane Sprite A	4h	Display Plane Sprite B	5h	Display Plane Sprite C
Value	Name															
0h	Display Plane-A															
1h	Display Plane-B															
2h	Display Plane-C															
3h	Display Plane Sprite A															
4h	Display Plane Sprite B															
5h	Display Plane Sprite C															
11	<b>Semaphore Wait Mode</b>															
<table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0h</td><td>Signal Mode</td></tr> <tr> <td>1h</td><td>Poll Mode</td></tr> </tbody> </table>			Value	Name	0h	Signal Mode	1h	Poll Mode								
Value	Name															
0h	Signal Mode															
1h	Poll Mode															
10:9	<b>Reserved</b>															
Format: MBZ																
8	<b>Wait on Scanline</b>															
7	<b>Wait on Semaphore</b>															
6	<b>Wait on V-blank</b>															
5	<b>Wait on Sync Flip</b>															
4	<b>Context Complete</b> Element is completely processed (Head eqv to Tail) and resulted in a context switch.															
3	<b>ACTIVE to IDLE</b> Following this context switch there is no active element available in HW to execute															
2	<b>Element Switch</b> Context Switch happened from first element in the current exelist to the second element of the same exelist															
1	<b>Preempted</b> Submission of a new exelist has resulted in context switch. The switch is from element in current exelist to element in pending exelist															
0	<b>IDLE to ACTIVE</b> Exelist submitted when HW is IDLE. When this bit is set rest of the fields in CSQ are not valid.															

## CSC COEFFICIENT FORMAT

CSC COEFFICIENT FORMAT																										
DWord	Bit	Description																								
0	15	<b>Sign</b> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Positive</td> </tr> <tr> <td>1b</td> <td>Negative</td> </tr> </tbody> </table>	Value	Name	0b	Positive	1b	Negative																		
Value	Name																									
0b	Positive																									
1b	Negative																									
	14:12	<b>Exponent_bits</b> Represented as $2^{(-n)}$ <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>110b</td> <td>4</td> <td>4 or mantissa is bb.bbbbbbb</td> </tr> <tr> <td>111b</td> <td>2</td> <td>2 or mantissa is b.bbbbbbbb</td> </tr> <tr> <td>000b</td> <td>1</td> <td>1 or mantissa is 0.bbbbbbbb</td> </tr> <tr> <td>001b</td> <td>0.5</td> <td>0.5 or mantissa is 0.0bbbbbb</td> </tr> <tr> <td>010b</td> <td>0.25</td> <td>0.25 or mantissa is 0.00bbbbbb</td> </tr> <tr> <td>011b</td> <td>0.125</td> <td>0.125 or mantissa is 0.000bbbbbb</td> </tr> <tr> <td>Others</td> <td>Reserved</td> <td>Reserved</td> </tr> </tbody> </table>	Value	Name	Description	110b	4	4 or mantissa is bb.bbbbbbb	111b	2	2 or mantissa is b.bbbbbbbb	000b	1	1 or mantissa is 0.bbbbbbbb	001b	0.5	0.5 or mantissa is 0.0bbbbbb	010b	0.25	0.25 or mantissa is 0.00bbbbbb	011b	0.125	0.125 or mantissa is 0.000bbbbbb	Others	Reserved	Reserved
Value	Name	Description																								
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111b	2	2 or mantissa is b.bbbbbbbb																								
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001b	0.5	0.5 or mantissa is 0.0bbbbbb																								
010b	0.25	0.25 or mantissa is 0.00bbbbbb																								
011b	0.125	0.125 or mantissa is 0.000bbbbbb																								
Others	Reserved	Reserved																								
	11:3	<b>Mantissa</b>																								
	2:0	<b>Reserved</b>																								

## Data Port 0 Message Types

MT_DPO - Data Port 0 Message Types																																								
DWord	Bit	Description																																						
0	4	<p><b>Legacy DAP-DC Message</b></p> <table border="1"> <tr> <td>Format:</td> <td>Enumeration</td> </tr> </table> <p>Legacy Message</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>No [Default]</td> <td>Legacy DAP-DC Message</td> </tr> <tr> <td>1h</td> <td>Reserved</td> <td>Scratch Block Message, descriptor uses different Message Type encoding</td> </tr> </tbody> </table>	Format:	Enumeration	Value	Name	Description	0h	No [Default]	Legacy DAP-DC Message	1h	Reserved	Scratch Block Message, descriptor uses different Message Type encoding																											
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3:0																																								
<p><b>Message Type</b></p> <table border="1"> <tr> <td>Format:</td> <td>Enumeration</td> </tr> </table> <p>Specifies type of message</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00h</td> <td>MT0R_OWB [Default]</td> <td>Oword Block Read message</td> </tr> <tr> <td>01h</td> <td>MT0R_OWUB</td> <td>Unaligned Oword Block Read message</td> </tr> <tr> <td>02h</td> <td>MT0R_OWDB</td> <td>Oword Dual Block Read message</td> </tr> <tr> <td>03h</td> <td>MT0R_DWS</td> <td>Dword Scattered Read message</td> </tr> <tr> <td>04h</td> <td>MT0R_BS</td> <td>Byte Scattered Read message</td> </tr> <tr> <td>07h</td> <td>MT0_MEMFENCE</td> <td>Memory Fence message</td> </tr> <tr> <td>08h</td> <td>MT0W_OWB</td> <td>Oword Block Write message</td> </tr> <tr> <td>0Ah</td> <td>MT0W_OWDB</td> <td>Oword Dual Block Write message</td> </tr> <tr> <td>0Bh</td> <td>MT0W_DWS</td> <td>Dword Scattered Write message</td> </tr> <tr> <td>0Ch</td> <td>MT0W_BS</td> <td>Byte Scattered Write message</td> </tr> <tr> <td>Others</td> <td>Reserved</td> <td>Ignored</td> </tr> </tbody> </table>			Format:	Enumeration	Value	Name	Description	00h	MT0R_OWB [Default]	Oword Block Read message	01h	MT0R_OWUB	Unaligned Oword Block Read message	02h	MT0R_OWDB	Oword Dual Block Read message	03h	MT0R_DWS	Dword Scattered Read message	04h	MT0R_BS	Byte Scattered Read message	07h	MT0_MEMFENCE	Memory Fence message	08h	MT0W_OWB	Oword Block Write message	0Ah	MT0W_OWDB	Oword Dual Block Write message	0Bh	MT0W_DWS	Dword Scattered Write message	0Ch	MT0W_BS	Byte Scattered Write message	Others	Reserved	Ignored
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## Data Port 1 Message Types

MT_DP1 - Data Port 1 Message Types																																																																											
DWord	Bit	Description																																																																									
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## MT\_DP1 - Data Port 1 Message Types

		19h	MT1W_A64_US	A64 Untyped Surface Write message
		1Ah	MT1W_A64_SB	A64 Scattered Write message
		1Bh	MT1A_UF	Untyped Atomic Float Operation message
		1Ch	MT1A_UF4x2	Untyped Atomic Float Operation SIMD4x2 message
		1Dh	MT1A_A64_UF	A64 Untyped Atomic Float Operation message
		1Eh	MT1A_A64_UF4x2	A64 Untyped Atomic Float Operation SIMD4x2 message
		Others	Reserved	Ignored

## Data Size Message Descriptor Control Field

MDC_DS - Data Size Message Descriptor Control Field																					
DWord	Bit	Description																			
0	1:0	<p><b>Data Size</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Enumeration</td> </tr> </table> <p>Specifies the number of Bytes to be read or written</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00h</td> <td>B</td> <td>1 Byte</td> </tr> <tr> <td>01h</td> <td>W</td> <td>2 Bytes</td> </tr> <tr> <td>02h</td> <td>DW</td> <td>4 Bytes</td> </tr> <tr> <td>03h</td> <td>Reserved</td> <td>Reserved</td> </tr> </tbody> </table>	Project:	All	Format:	Enumeration	Value	Name	Description	00h	B	1 Byte	01h	W	2 Bytes	02h	DW	4 Bytes	03h	Reserved	Reserved
Project:	All																				
Format:	Enumeration																				
Value	Name	Description																			
00h	B	1 Byte																			
01h	W	2 Bytes																			
02h	DW	4 Bytes																			
03h	Reserved	Reserved																			

## Display Engine Render Response Message Definition

Display Engine Render Response Message Definition		
DWord	Bit	Description
0	29	<b>Reserved</b>
	28:23	<b>Reserved</b>
	22	<b>Reserved</b>
	21	<b>Pipe_C_Start_of_Vertical_Blank_Event</b> This event is reported on the start of the vertical blank of the transcoder attached to Pipe C.
	20	<b>Pipe_C_Sprite_Plane_Flip_Done_Event</b> This event is reported on the completion of a flip for the Pipe C Sprite Plane.
	19:16	<b>Reserved</b>
	15	<b>Pipe_C_Primary_Plane_Flip_Done_Event</b> This event is reported on the completion of a flip for the Pipe C Primary Plane.
	14	<b>Pipe_C_Scanline_Event</b> This event is reported on the start of the selected scan line for the transcoder attached to Pipe C.
	13	<b>Reserved</b>
	12	<b>Reserved</b>
	11	<b>Pipe_B_Start_of_Vertical_Blank_Event</b> This event is reported on the start of the vertical blank of the transcoder attached to Pipe B.
	10	<b>Pipe_B_Sprite_Plane_Flip_Done_Event</b> This event is reported on the completion of a flip for the Pipe B Sprite Plane.
	9	<b>Pipe_B_Primary_Plane_Flip_Done_Event</b> This event is reported on the completion of a flip for the Pipe B Primary Plane.
	8	<b>Pipe_B_Scanline_Event</b> This event is reported on the start of the selected scan line for the transcoder attached to Pipe B.
	7:6	<b>Reserved</b>
	5	<b>Reserved</b>

## Display Engine Render Response Message Definition

	4	<b>Reserved</b>
	3	<b>Pipe_A_Start_of_Vertical_Blank_Event</b> This event is reported on the start of the vertical blank of the transcoder attached to Pipe A.
	2	<b>Pipe_A_Sprite_Plane_Flip_Done_Event</b> This event is reported on the completion of a flip for the Pipe A Sprite Plane.
	1	<b>Pipe_A_Primary_Plane_Flip_Done_Event</b> This event is reported on the completion of a flip for the Pipe A Primary Plane.
	0	<b>Pipe_A_Scanline_Event</b> This event is reported on the start of the selected scan line for the transcoder attached to Pipe A.

## DstRegNum

DstRegNum									
<p><b>Description</b></p> <p>Register Number The register number for the operand. For a GRF register, is the part of a register address that aligns to a 256-bit (32-byte) boundary. For an ARF register, this field is encoded such that MSBs identify the architecture register type and LSBs provide the register number. An ARF register can only be dst or src0. Any src1 or src2 operands cannot be ARF registers. RegNum and SubRegNum together provide the byte-aligned address for the origin of a register region. RegNum provides bits 12:5 of that address. For one-source and two-source instructions, SubregNum provides bits 4:0. For three-source instructions, the address must be DWord-aligned; SubRegNum provides bits 4:2 of the address and bits 1:0 are zero. This field is present for the direct addressing mode and not present for indirect addressing. This field applies to both source and destination operands.</p>									
DWord	Bit	Description							
0	7:0	<b>Destination Register Number</b>							
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0-127</td> <td>If {Dst/Src0/Src1/Src2}.RegFile==GRF</td> <td></td> </tr> <tr> <td>0-0ffh</td> <td>If {Dst/Src0/Src1/Src2}.RegFile==ARF</td> <td>This field is used to encode the architecture register as well as providing the register number. See GEN Execution Environment chapter for details.</td> </tr> </tbody> </table>	Value	Name	Description	0-127	If {Dst/Src0/Src1/Src2}.RegFile==GRF		0-0ffh
Value	Name	Description							
0-127	If {Dst/Src0/Src1/Src2}.RegFile==GRF								
0-0ffh	If {Dst/Src0/Src1/Src2}.RegFile==ARF	This field is used to encode the architecture register as well as providing the register number. See GEN Execution Environment chapter for details.							

## DstSubRegNum

<b>DstSubRegNum</b>												
<p>Project: BDW</p> <p>Source: Eulsa</p> <p>Size (in bits): 5</p> <p>Default Value: 0x00000000</p>												
<p><b>Description</b></p> <p>Subregister Number The subregister number for the operand. For a GRF register, is the byte address within a 256-bit (32-byte) register. For an ARF register, determines the sub-register number according to the specified encoding for the given architecture register. RegNum and SubRegNum together provide the byte-aligned address for the origin of a GRF register region. RegNum provides bits 12:5 of that address. For one-source and two-source instructions, SubregNum provides bits 4:0. For three-source instructions, the address must be DWord-aligned; SubRegNum provides bits 4:2 of the address and bits 1:0 are zero.</p>												
<p><b>Programming Notes</b></p> <p>Note: The recommended instruction syntax uses subregister numbers within the GRF in units of actual data element size, corresponding to the data type used. For example for the F (Float) type, the assembler syntax uses subregister numbers 0 to 7, corresponding to subregister byte addresses of 0 to 28 in steps of 4, the element size.</p>												
<b>DWord</b>	<b>Bit</b>	<b>Description</b>										
0	4:0	<b>Destination Sub Register Number</b> <table border="1"> <thead> <tr> <th><b>Value</b></th><th><b>Name</b></th><th><b>Description</b></th></tr> </thead> <tbody> <tr> <td>0-31</td><td>If {Dst/Src0/Src1/Src2}.RegFile==GRF</td><td></td></tr> <tr> <td>0-0ffh</td><td>If {Dst/Src0/Src1/Src2}.RegFile==ARF</td><td>This field is used to encode the architecture register as well as providing the register number. See GEN Execution Environment chapter for details.</td></tr> </tbody> </table>		<b>Value</b>	<b>Name</b>	<b>Description</b>	0-31	If {Dst/Src0/Src1/Src2}.RegFile==GRF		0-0ffh	If {Dst/Src0/Src1/Src2}.RegFile==ARF	This field is used to encode the architecture register as well as providing the register number. See GEN Execution Environment chapter for details.
<b>Value</b>	<b>Name</b>	<b>Description</b>										
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0-0ffh	If {Dst/Src0/Src1/Src2}.RegFile==ARF	This field is used to encode the architecture register as well as providing the register number. See GEN Execution Environment chapter for details.										

## Dword Data Payload Register

MDCR_DW - Dword Data Payload Register						
DWord	Bit	Description				
0.0	31:0	<p><b>Dword0</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U32</td></tr> </table> <p>Specifies the slot 0 data in this payload register</p>	Project:	All	Format:	U32
Project:	All					
Format:	U32					
0.1	31:0	<p><b>Dword1</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U32</td></tr> </table> <p>Specifies the slot 1 data in this payload register</p>	Project:	All	Format:	U32
Project:	All					
Format:	U32					
0.2	31:0	<p><b>Dword2</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U32</td></tr> </table> <p>Specifies the slot 2 data in this payload register</p>	Project:	All	Format:	U32
Project:	All					
Format:	U32					
0.3	31:0	<p><b>Dword3</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U32</td></tr> </table> <p>Specifies the slot 3 data in this payload register</p>	Project:	All	Format:	U32
Project:	All					
Format:	U32					
0.4	31:0	<p><b>Dword4</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U32</td></tr> </table> <p>Specifies the slot 4 data in this payload register</p>	Project:	All	Format:	U32
Project:	All					
Format:	U32					
0.5	31:0	<p><b>Dword5</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U32</td></tr> </table> <p>Specifies the slot 5 data in this payload register</p>	Project:	All	Format:	U32
Project:	All					
Format:	U32					

## MDCR\_DW - Dword Data Payload Register

0.6	31:0	<b>Dword6</b> Project: All Format: U32 Specifies the slot 6 data in this payload register
0.7	31:0	<b>Dword7</b> Project: All Format: U32 Specifies the slot 7 data in this payload register

## Dword SIMD4x2 Atomic CMPWR Message Data Payload

<b>MDP_AOP4X2_DW2 - Dword SIMD4x2 Atomic CMPWR Message Data Payload</b>				
<b>DWord</b>	<b>Bit</b>	<b>Description</b>		
0	31:0	<p><b>Src0 Slot0</b></p> <table border="1"> <tr> <td>Format:</td> <td>U32 S31 F32</td> </tr> </table> <p>Specifies the Slot 0 Source 0 data</p>	Format:	U32 S31 F32
Format:	U32 S31 F32			
1	31:0	<p><b>Src1 Slot0</b></p> <table border="1"> <tr> <td>Format:</td> <td>U32 S31 F32</td> </tr> </table> <p>Specifies the Slot 0 Source 1 data</p>	Format:	U32 S31 F32
Format:	U32 S31 F32			
2-3	63:0	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>Ignore</td> </tr> </table> <p>Ignored</p>	Format:	Ignore
Format:	Ignore			
4	31:0	<p><b>Src0 Slot1</b></p> <table border="1"> <tr> <td>Format:</td> <td>U32 S31 F32</td> </tr> </table> <p>Specifies the Slot 1 Source 0 data</p>	Format:	U32 S31 F32
Format:	U32 S31 F32			
5	31:0	<p><b>Src1 Slot1</b></p> <table border="1"> <tr> <td>Format:</td> <td>U32 S31 F32</td> </tr> </table> <p>Specifies the Slot 1 Source 1 data</p>	Format:	U32 S31 F32
Format:	U32 S31 F32			
6-7	63:0	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>Ignore</td> </tr> </table> <p>Ignored</p>	Format:	Ignore
Format:	Ignore			

## Dword SIMD4x2 Atomic Operation Message Data Payload

<b>MDP_AOP4X2_DW1 - Dword SIMD4x2 Atomic Operation Message Data Payload</b>				
<b>DWord</b>	<b>Bit</b>	<b>Description</b>		
0	31:0	<p><b>Dword0</b></p> <table border="1"> <tr> <td>Format:</td> <td>U32 S31 F32</td> </tr> </table> <p>Specifies the Slot 0 Source or Return data</p>	Format:	U32 S31 F32
Format:	U32 S31 F32			
1-3	95:0	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>Ignore</td> </tr> </table> <p>Ignored</p>	Format:	Ignore
Format:	Ignore			
4	31:0	<p><b>Dword1</b></p> <table border="1"> <tr> <td>Format:</td> <td>U32 S31 F32</td> </tr> </table> <p>Specifies the Slot 1 Source or Return data</p>	Format:	U32 S31 F32
Format:	U32 S31 F32			
5-7	95:0	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>Ignore</td> </tr> </table> <p>Ignored</p>	Format:	Ignore
Format:	Ignore			

## Dword SIMD4x2 Data Payload

MDP_DW SIMD4X2 - Dword SIMD4x2 Data Payload						
DWord	Bit	Description				
0	31:0	<p><b>Red Slot0</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U32</td></tr> </table> <p>Specifies the Slot 0 red channel data</p>	Project:	All	Format:	U32
Project:	All					
Format:	U32					
1	31:0	<p><b>Green Slot0</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U32</td></tr> </table> <p>Specifies the Slot 0 green channel data</p>	Project:	All	Format:	U32
Project:	All					
Format:	U32					
2	31:0	<p><b>Blue Slot0</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U32</td></tr> </table> <p>Specifies the Slot 0 blue channel data</p>	Project:	All	Format:	U32
Project:	All					
Format:	U32					
3	31:0	<p><b>Alpha Slot0</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U32</td></tr> </table> <p>Specifies the Slot 0 alpha channel data</p>	Project:	All	Format:	U32
Project:	All					
Format:	U32					
4	31:0	<p><b>Red Slot1</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U32</td></tr> </table> <p>Specifies the Slot 1 red channel data</p>	Project:	All	Format:	U32
Project:	All					
Format:	U32					
5	31:0	<p><b>Green Slot1</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U32</td></tr> </table> <p>Specifies the Slot 1 green channel data</p>	Project:	All	Format:	U32
Project:	All					
Format:	U32					

**MDP\_DW SIMD4X2 - Dword SIMD4x2 Data Payload**

6	31:0	<b>Blue Slot1</b> <table border="1"><tr><td>Project:</td><td>All</td></tr><tr><td>Format:</td><td>U32</td></tr></table> <p>Specifies the Slot 1 blue channel data</p>	Project:	All	Format:	U32
Project:	All					
Format:	U32					
7	31:0	<b>Alpha Slot1</b> <table border="1"><tr><td>Project:</td><td>All</td></tr><tr><td>Format:</td><td>U32</td></tr></table> <p>Specifies the Slot 1 alpha channel data</p>	Project:	All	Format:	U32
Project:	All					
Format:	U32					

## Dword SIMD8 Atomic Operation CMPWR Message Data Payload

<b>MDP_AOP8_DW2 - Dword SIMD8 Atomic Operation CMPWR Message Data Payload</b>						
<b>DWord</b>	<b>Bit</b>	<b>Description</b>				
0.0-0.7	255:0	<p><b>Src0</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDCR_DW</b></td></tr> </table> <p>Specifies the Slot [7:0] Source 0 data</p>	Project:	All	Format:	<b>MDCR_DW</b>
Project:	All					
Format:	<b>MDCR_DW</b>					
1.0-1.7	255:0	<p><b>Src1</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDCR_DW</b></td></tr> </table> <p>Specifies the Slot [7:0] Source 1 data</p>	Project:	All	Format:	<b>MDCR_DW</b>
Project:	All					
Format:	<b>MDCR_DW</b>					

## Dword SIMD8 Data Payload

MDP_DW SIMD8 - Dword SIMD8 Data Payload						
DWord	Bit	Description				
0.0-0.7	255:0	<p><b>Data[7:0]</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDCR_DW</b></td></tr> </table> <p>Specifies the Slot [7:0] data</p>	Project:	All	Format:	<b>MDCR_DW</b>
Project:	All					
Format:	<b>MDCR_DW</b>					

## Dword SIMD16 Atomic Operation CMPWR Message Data Payload

<b>MDP_AOP16_DW2 - Dword SIMD16 Atomic Operation CMPWR Message Data Payload</b>						
<b>DWord</b>	<b>Bit</b>	<b>Description</b>				
0.0-0.7	255:0	<p><b>Src0[7:0]</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td><b>MDCR_DW</b></td> </tr> </table> <p>Specifies the Source 0 data for Slot [7:0]</p>	Project:	All	Format:	<b>MDCR_DW</b>
Project:	All					
Format:	<b>MDCR_DW</b>					
1.0-1.7	255:0	<p><b>Src0[15:8]</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td><b>MDCR_DW</b></td> </tr> </table> <p>Specifies the Source 0 data for Slot [15:8]</p>	Project:	All	Format:	<b>MDCR_DW</b>
Project:	All					
Format:	<b>MDCR_DW</b>					
2.0-2.7	255:0	<p><b>Src1[7:0]</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td><b>MDCR_DW</b></td> </tr> </table> <p>Specifies the Source 1 data for Slot [7:0]</p>	Project:	All	Format:	<b>MDCR_DW</b>
Project:	All					
Format:	<b>MDCR_DW</b>					
3.0-3.7	255:0	<p><b>Src1[15:8]</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td><b>MDCR_DW</b></td> </tr> </table> <p>Specifies the Source 1 data for Slot [15:8]</p>	Project:	All	Format:	<b>MDCR_DW</b>
Project:	All					
Format:	<b>MDCR_DW</b>					

## Dword SIMD16 Data Payload

<b>MDP_DW SIMD16 - Dword SIMD16 Data Payload</b>						
<b>DWord</b>	<b>Bit</b>	<b>Description</b>				
0.0-0.7	255:0	<p><b>Data[7:0]</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDCR_DW</b></td></tr> </table> <p>Specifies the Slot [7:0] data</p>	Project:	All	Format:	<b>MDCR_DW</b>
Project:	All					
Format:	<b>MDCR_DW</b>					
1.0-1.7	255:0	<p><b>Data[15:8]</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDCR_DW</b></td></tr> </table> <p>Specifies the Slot [15:8] data</p>	Project:	All	Format:	<b>MDCR_DW</b>
Project:	All					
Format:	<b>MDCR_DW</b>					

## DX9\_CONSTANTB\_ENTRY

DX9_CONSTANTB_ENTRY				
DWord	Bit	Description		
0	31:0	<p><b>Component</b></p> <table border="1"> <tr> <td>Format:</td> <td>U32</td> </tr> </table> <p>The boolean value to be stored.</p>	Format:	U32
Format:	U32			
This structure is the payload of the 3DSTATE_DX9_CONSTANTB_* commands. Each entry provides the values for the one boolean constant being updated.				

## DX9\_CONSTANTF\_ENTRY

DX9_CONSTANTF_ENTRY				
DWord	Bit	Description		
0	127:96	<p><b>Component 3</b></p> <table border="1"> <tr> <td>Format:</td> <td>IEEE_Float</td> </tr> </table> <p>The 4th component of the nth float to be stored.</p>	Format:	IEEE_Float
Format:	IEEE_Float			
95:64	<p><b>Component 2</b></p> <table border="1"> <tr> <td>Format:</td> <td>IEEE_Float</td> </tr> </table> <p>The 3rd component of the nth float to be stored.</p>	Format:	IEEE_Float	
Format:	IEEE_Float			
63:32	<p><b>Component 1</b></p> <table border="1"> <tr> <td>Format:</td> <td>IEEE_Float</td> </tr> </table> <p>The 2nd component of the nth float to be stored.</p>	Format:	IEEE_Float	
Format:	IEEE_Float			
31:0	<p><b>Component 0</b></p> <table border="1"> <tr> <td>Format:</td> <td>IEEE_Float</td> </tr> </table> <p>The 1st component of the nth float to be stored.</p>	Format:	IEEE_Float	
Format:	IEEE_Float			

## DX9\_CONSTANTI\_ENTRY

DX9_CONSTANTI_ENTRY				
DWord	Bit	Description		
0	31:0	<p><b>Component 0</b></p> <table border="1"> <tr> <td>Format:</td> <td>U32</td> </tr> </table> <p>The 1st component of the nth float to be stored.</p>	Format:	U32
Format:	U32			
1	31:0	<p><b>Component 1</b></p> <table border="1"> <tr> <td>Format:</td> <td>U32</td> </tr> </table> <p>The 2nd component of the nth float to be stored.</p>	Format:	U32
Format:	U32			
2	31:0	<p><b>Component 2</b></p> <table border="1"> <tr> <td>Format:</td> <td>U32</td> </tr> </table> <p>The 3rd component of the nth float to be stored.</p>	Format:	U32
Format:	U32			
3	31:0	<p><b>Component 3</b></p> <table border="1"> <tr> <td>Format:</td> <td>U32</td> </tr> </table> <p>The 4th component of the nth float to be stored.</p>	Format:	U32
Format:	U32			

## Encoder Statistics Format

Encoder Statistics Format			
DWord	Bit	Description	
0	31:24	<b>Tearing_Count 1 (FMD Variance[8])</b>	
		Format:	U8
		Number of pixels that have (diff_cTcB > diff_cTcT + diff_cBcB)	
	23:16	Value	Name
		0	DI is Disabled
	15:8	<b>Tearing_Count 2</b>	
		Format:	U8
		If the frame is Deinterlaced with Top First in the DN/DI state then this is (FMD Variance[9]) = Number of pixels that have (diff_cTpB > diff_cTcT + diff_pBpB)	
	7:0	If the frame is bottom first then this is (FMD Variance[10]) = Number of pixels that have (diff_cBpT > diff_pTpT + diff_cBcB)	
		Value	Name
		0	DI is Disabled
	1	<b>Motion_Count (FMD Variance[7])</b>	
		Format:	U8
		Number of pixels that are moving (different above a threshold)	
	31:28	Value	Name
		0	DI is Disabled
	31:28	<b>sSTAD</b>	
		Format:	U4
		Shift for the Sum in time of absolute differences for 16x4.	
		Value	Name
		0	DN is Disabled
		Project	
		BDW	

## Encoder Statistics Format

		<b>sSHCM</b>								
	27:24	Format: Shift for the Sum horizontally of absolute differences.								
		<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="background-color: #e0f2ff; text-align: center;"><b>Value</b></th><th style="background-color: #e0f2ff; text-align: center;"><b>Name</b></th><th style="background-color: #e0f2ff; text-align: center;"><b>Description</b></th></tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td><td></td><td>DN is Disabled</td></tr> </tbody> </table>			<b>Value</b>	<b>Name</b>	<b>Description</b>	0		DN is Disabled
<b>Value</b>	<b>Name</b>	<b>Description</b>								
0		DN is Disabled								
	23:20	<b>sSVCM</b>								
		Format: Shift for the Sum vertically of absolute differences.								
	19:16	<b>sDiff_cTpT</b>								
		Format: Shift for the sum of differences in top fields of current and previous frame.								
		<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="background-color: #e0f2ff; text-align: center;"><b>Value</b></th><th style="background-color: #e0f2ff; text-align: center;"><b>Name</b></th><th style="background-color: #e0f2ff; text-align: center;"><b>Description</b></th></tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td><td></td><td>DI is Disabled</td></tr> </tbody> </table>			<b>Value</b>	<b>Name</b>	<b>Description</b>	0		DI is Disabled
<b>Value</b>	<b>Name</b>	<b>Description</b>								
0		DI is Disabled								
	15:12	<b>sDiff_cBpB</b>								
		Format: Shift for the sum of differences in bottom field of current and previous frame.								
		<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="background-color: #e0f2ff; text-align: center;"><b>Value</b></th><th style="background-color: #e0f2ff; text-align: center;"><b>Name</b></th><th style="background-color: #e0f2ff; text-align: center;"><b>Description</b></th></tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td><td></td><td>DI is Disabled</td></tr> </tbody> </table>			<b>Value</b>	<b>Name</b>	<b>Description</b>	0		DI is Disabled
<b>Value</b>	<b>Name</b>	<b>Description</b>								
0		DI is Disabled								
	11:8	<b>sDiff_cTcB</b>								
		Format: Shift for the sum of differences between top and bottom field in current frame.								
		<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="background-color: #e0f2ff; text-align: center;"><b>Value</b></th><th style="background-color: #e0f2ff; text-align: center;"><b>Name</b></th><th style="background-color: #e0f2ff; text-align: center;"><b>Description</b></th></tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td><td></td><td>DI is Disabled</td></tr> </tbody> </table>			<b>Value</b>	<b>Name</b>	<b>Description</b>	0		DI is Disabled
<b>Value</b>	<b>Name</b>	<b>Description</b>								
0		DI is Disabled								
	7:4	<b>sDiff_cTpB</b>								
		Format: Shift for the sum of differences between current top and previous bottom.								
		<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="background-color: #e0f2ff; text-align: center;"><b>Value</b></th><th style="background-color: #e0f2ff; text-align: center;"><b>Name</b></th><th style="background-color: #e0f2ff; text-align: center;"><b>Description</b></th></tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td><td></td><td>DI is Disabled</td></tr> </tbody> </table>			<b>Value</b>	<b>Name</b>	<b>Description</b>	0		DI is Disabled
<b>Value</b>	<b>Name</b>	<b>Description</b>								
0		DI is Disabled								
	3:0	<b>sDiff_cBpT</b>								
		Format: Shift for the sum of differences between current bottom and previous top.								
		<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="background-color: #e0f2ff; text-align: center;"><b>Value</b></th><th style="background-color: #e0f2ff; text-align: center;"><b>Name</b></th><th style="background-color: #e0f2ff; text-align: center;"><b>Description</b></th></tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td><td></td><td>DI is Disabled</td></tr> </tbody> </table>			<b>Value</b>	<b>Name</b>	<b>Description</b>	0		DI is Disabled
<b>Value</b>	<b>Name</b>	<b>Description</b>								
0		DI is Disabled								

## Encoder Statistics Format

2	31:24	<b>mDiff_cBpB (FMD Variance[1])</b>	
		Format:	
		U8	
		Mantissa of sum of differences in bottom field of current and previous frame.	
	23:16	<b>mDiff_cTcB (FMD Variance[2])</b>	
		Format:	
		U8	
	15:8	Mantissa of sum of differences between top and bottom field in current frame.	
		<b>mDiff_cTpB (FMD Variance[3])</b>	
		Format:	
	7:0	U8	
		Mantissa of sum of differences between current top and previous bottom.	
		<b>mDiff_cBpT (FMD Variance[4])</b>	
	3	Format:	
		U8	
		Mantissa of sum of differences between current bottom and previous top.	
	31:24	<b>mSTAD</b>	
		Format:	
		U8	
	23:16	Mantissa of Sum in time of absolute differences for 16x4.	
		<b>mSHCM</b>	
		Format:	
	15:8	Mantissa of Sum horizontally of absolute differences.	
		<b>mSVCM</b>	
		Format:	

## Encoder Statistics Format

	7:0	<b>mDiff_cTpT (FMD Variance[0])</b>
		Format: U8
Mantissa of sum of differences in top fields of current and previous frame.		
Value	Name	Description
0		DI is Disabled

## EU\_INSTRUCTION\_BASIC\_ONE\_SRC

EU_INSTRUCTION_BASIC_ONE_SRC						
DWord	Bit	Description				
0..3	127:64	<b>RegSource</b> <table border="1"> <tr> <td>Exists If:</td><td>([Operand Controls][Src0.RegFile]!='IMM')</td></tr> <tr> <td>Format:</td><td><b>EU_INSTRUCTION_SOURCES_REG</b></td></tr> </table>	Exists If:	([Operand Controls][Src0.RegFile]!='IMM')	Format:	<b>EU_INSTRUCTION_SOURCES_REG</b>
Exists If:	([Operand Controls][Src0.RegFile]!='IMM')					
Format:	<b>EU_INSTRUCTION_SOURCES_REG</b>					
127:64	<b>ImmSource</b> <table border="1"> <tr> <td>Exists If:</td><td>([Operand Controls][Src0.RegFile]=='IMM')</td></tr> <tr> <td>Format:</td><td><b>EU_INSTRUCTION_SOURCES_IMM32</b></td></tr> </table>	Exists If:	([Operand Controls][Src0.RegFile]=='IMM')	Format:	<b>EU_INSTRUCTION_SOURCES_IMM32</b>	
Exists If:	([Operand Controls][Src0.RegFile]=='IMM')					
Format:	<b>EU_INSTRUCTION_SOURCES_IMM32</b>					
63:32	<b>Operand Controls</b> <table border="1"> <tr> <td>Format:</td><td><b>EU_INSTRUCTION_OPERAND_CONTROLS</b></td></tr> </table>	Format:	<b>EU_INSTRUCTION_OPERAND_CONTROLS</b>			
Format:	<b>EU_INSTRUCTION_OPERAND_CONTROLS</b>					
31:0	<b>Header</b> <table border="1"> <tr> <td>Format:</td><td><b>EU_INSTRUCTION_HEADER</b></td></tr> </table>	Format:	<b>EU_INSTRUCTION_HEADER</b>			
Format:	<b>EU_INSTRUCTION_HEADER</b>					

## EU\_INSTRUCTION\_BASIC\_THREE\_SRC

EU_INSTRUCTION_BASIC_THREE_SRC						
DWord	Bit	Description				
0..3	127	<b>Reserved</b> <table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ		
Format:	MBZ					
	126	<b>Reserved</b> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	BDW	Format:	MBZ
Project:	BDW					
Format:	MBZ					
125:106	Source 2	<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td><b>EU_INSTRUCTION_OPERAND_SRC_REG_THREE_SRC</b></td></tr> </table>	Project:	BDW	Format:	<b>EU_INSTRUCTION_OPERAND_SRC_REG_THREE_SRC</b>
Project:	BDW					
Format:	<b>EU_INSTRUCTION_OPERAND_SRC_REG_THREE_SRC</b>					
	105	<b>Reserved</b> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	BDW	Format:	MBZ
Project:	BDW					
Format:	MBZ					
104:85	Source 1	<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td><b>EU_INSTRUCTION_OPERAND_SRC_REG_THREE_SRC</b></td></tr> </table>	Project:	BDW	Format:	<b>EU_INSTRUCTION_OPERAND_SRC_REG_THREE_SRC</b>
Project:	BDW					
Format:	<b>EU_INSTRUCTION_OPERAND_SRC_REG_THREE_SRC</b>					
84	Reserved	<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	BDW	Format:	MBZ
Project:	BDW					
Format:	MBZ					
83:64	Source 0	<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td><b>EU_INSTRUCTION_OPERAND_SRC_REG_THREE_SRC</b></td></tr> </table>	Project:	BDW	Format:	<b>EU_INSTRUCTION_OPERAND_SRC_REG_THREE_SRC</b>
Project:	BDW					
Format:	<b>EU_INSTRUCTION_OPERAND_SRC_REG_THREE_SRC</b>					
63:56	Destination Register Number	<table border="1"> <tr> <td>Format:</td><td><b>DstRegNum</b></td></tr> </table>	Format:	<b>DstRegNum</b>		
Format:	<b>DstRegNum</b>					
55:53	Destination Subregister Number					

## EU\_INSTRUCTION\_BASIC\_THREE\_SRC

	52:49	<b>Destination Channel Enable</b>																					
		<table border="1"> <tr> <td>Format:</td><td style="background-color: #e0e0e0;"><b>ChanEn[4]</b></td></tr> </table>	Format:	<b>ChanEn[4]</b>																			
Format:	<b>ChanEn[4]</b>																						
<p>Four channel enables are defined for controlling which channels are written into the destination region. These channel mask bits are applied in a modulo-four manner to all ExecSize channels. There is 1-bit Channel Enable for each channel within the group of 4. If the bit is cleared, the write for the corresponding channel is disabled. If the bit is set, the write is enabled. Mnemonics for the bit being set for the group of 4 are <i>x</i>, <i>y</i>, <i>z</i>, and <i>w</i>, respectively, where <i>x</i> corresponds to Channel 0 in the group and <i>w</i> corresponds to channel 3 in the group</p>																							
	48:46	<b>Destination Data Type</b>																					
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>000b</td><td>:f</td><td>single precision Float (32-bit)</td></tr> <tr> <td>001b</td><td>:d</td><td>signed Doubleword integer</td></tr> <tr> <td>010b</td><td>:ud</td><td>Unsigned Doubleword integer</td></tr> <tr> <td>011b</td><td>:df</td><td>Double precision Float (64-bit)</td></tr> <tr> <td>100b</td><td>:hf</td><td>Half Float (16-bit)</td></tr> <tr> <td>101b-111b</td><td>Reserved</td><td></td></tr> </tbody> </table>	Value	Name	Description	000b	:f	single precision Float (32-bit)	001b	:d	signed Doubleword integer	010b	:ud	Unsigned Doubleword integer	011b	:df	Double precision Float (64-bit)	100b	:hf	Half Float (16-bit)	101b-111b	Reserved	
Value	Name	Description																					
000b	:f	single precision Float (32-bit)																					
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010b	:ud	Unsigned Doubleword integer																					
011b	:df	Double precision Float (64-bit)																					
100b	:hf	Half Float (16-bit)																					
101b-111b	Reserved																						
	45:43	<b>Source Data Type</b>																					
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>000b</td><td>:f</td><td>single precision Float (32-bit)</td></tr> <tr> <td>001b</td><td>:d</td><td>signed Doubleword integer</td></tr> <tr> <td>010b</td><td>:ud</td><td>Unsigned Doubleword integer</td></tr> <tr> <td>011b</td><td>:df</td><td>Double precision Float (64-bit)</td></tr> <tr> <td>100b</td><td>:hf</td><td>Half Float (16-bit)</td></tr> <tr> <td>101b-111b</td><td>Reserved</td><td></td></tr> </tbody> </table>	Value	Name	Description	000b	:f	single precision Float (32-bit)	001b	:d	signed Doubleword integer	010b	:ud	Unsigned Doubleword integer	011b	:df	Double precision Float (64-bit)	100b	:hf	Half Float (16-bit)	101b-111b	Reserved	
Value	Name	Description																					
000b	:f	single precision Float (32-bit)																					
001b	:d	signed Doubleword integer																					
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011b	:df	Double precision Float (64-bit)																					
100b	:hf	Half Float (16-bit)																					
101b-111b	Reserved																						
	42:41	<b>Source 2 Modifier</b>																					
		<table border="1"> <tr> <td>Exists If:</td><td>(Property[Source Modifier]=='true')</td></tr> <tr> <td>Format:</td><td style="background-color: #e0e0e0;"><b>SrcMod</b></td></tr> </table>	Exists If:	(Property[Source Modifier]=='true')	Format:	<b>SrcMod</b>																	
Exists If:	(Property[Source Modifier]=='true')																						
Format:	<b>SrcMod</b>																						
	40:39	<b>Source 1 Modifier</b>																					
		<table border="1"> <tr> <td>Exists If:</td><td>(Property[Source Modifier]=='true')</td></tr> <tr> <td>Format:</td><td style="background-color: #e0e0e0;"><b>SrcMod</b></td></tr> </table>	Exists If:	(Property[Source Modifier]=='true')	Format:	<b>SrcMod</b>																	
Exists If:	(Property[Source Modifier]=='true')																						
Format:	<b>SrcMod</b>																						
	42:37	<b>Reserved</b>																					
		<table border="1"> <tr> <td>Exists If:</td><td>(Property[Source Modifier]=='false')</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Exists If:	(Property[Source Modifier]=='false')	Format:	MBZ																	
Exists If:	(Property[Source Modifier]=='false')																						
Format:	MBZ																						
	38:37	<b>Source 0 Modifier</b>																					
		<table border="1"> <tr> <td>Exists If:</td><td>(Property[Source Modifier]=='true')</td></tr> <tr> <td>Format:</td><td style="background-color: #e0e0e0;"><b>SrcMod</b></td></tr> </table>	Exists If:	(Property[Source Modifier]=='true')	Format:	<b>SrcMod</b>																	
Exists If:	(Property[Source Modifier]=='true')																						
Format:	<b>SrcMod</b>																						

## EU\_INSTRUCTION\_BASIC\_THREE\_SRC

	36:35	<b>Reserved</b>											
		Project:	BDW										
		Format:	MBZ										
	34	<b>MaskCtrl</b>											
		Project:	BDW										
		(formerly WECtrl/Write Enable Control). This flag disables the normal write enables; it should normally be 0.											
		<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="background-color: #d9e1f2;">Value</th><th style="background-color: #d9e1f2;">Name</th><th style="background-color: #d9e1f2;">Description</th></tr> </thead> <tbody> <tr> <td>0</td><td>Normal</td><td>Use the normal write enables in Dst.ChanEn (normal setting).</td></tr> <tr> <td>1</td><td>NoMask</td><td>Write all channels except those disabled by predication or by other masks besides the write enables.</td></tr> </tbody> </table>			Value	Name	Description	0	Normal	Use the normal write enables in Dst.ChanEn (normal setting).	1	NoMask	Write all channels except those disabled by predication or by other masks besides the write enables.
Value	Name	Description											
0	Normal	Use the normal write enables in Dst.ChanEn (normal setting).											
1	NoMask	Write all channels except those disabled by predication or by other masks besides the write enables.											
		<b>Programming Notes</b>											
		MaskCtrl = NoMask also skips the check for PclP[n] == ExIP before enabling a channel, as described in the Evaluate Write Enable section.											
	33	<b>Flag Register Number</b>											
		This field contains the flag register number for instructions with a non-zero Conditional Modifier.											
	32	<b>Flag Subregister Number</b>											
		This field contains the flag subregister number for instructions with a non-zero Conditional Modifier.											
	31:0	<b>Header</b>											
		Format:	<b>EU_INSTRUCTION_HEADER</b>										

## EU\_INSTRUCTION\_BASIC\_TWO\_SRC

EU_INSTRUCTION_BASIC_TWO_SRC						
DWord	Bit	Description				
0..3	127:64	<b>RegSource</b> <table border="1"> <tr> <td>Exists If:</td><td>([RegSource][Src1.RegFile]!='IMM')</td></tr> <tr> <td>Format:</td><td><b>EU_INSTRUCTION_SOURCES_REG_REG</b></td></tr> </table>	Exists If:	([RegSource][Src1.RegFile]!='IMM')	Format:	<b>EU_INSTRUCTION_SOURCES_REG_REG</b>
Exists If:	([RegSource][Src1.RegFile]!='IMM')					
Format:	<b>EU_INSTRUCTION_SOURCES_REG_REG</b>					
127:64	<b>ImmSource</b> <table border="1"> <tr> <td>Exists If:</td><td>([ImmSource][Src1.RegFile]=='IMM')</td></tr> <tr> <td>Format:</td><td><b>EU_INSTRUCTION_SOURCES_REG_IMM</b></td></tr> </table>	Exists If:	([ImmSource][Src1.RegFile]=='IMM')	Format:	<b>EU_INSTRUCTION_SOURCES_REG_IMM</b>	
Exists If:	([ImmSource][Src1.RegFile]=='IMM')					
Format:	<b>EU_INSTRUCTION_SOURCES_REG_IMM</b>					
63:32	<b>Operand Controls</b> <table border="1"> <tr> <td>Format:</td><td><b>EU_INSTRUCTION_OPERAND_CONTROLS</b></td></tr> </table>	Format:	<b>EU_INSTRUCTION_OPERAND_CONTROLS</b>			
Format:	<b>EU_INSTRUCTION_OPERAND_CONTROLS</b>					
31:0	<b>Header</b> <table border="1"> <tr> <td>Format:</td><td><b>EU_INSTRUCTION_HEADER</b></td></tr> </table>	Format:	<b>EU_INSTRUCTION_HEADER</b>			
Format:	<b>EU_INSTRUCTION_HEADER</b>					

## EU\_INSTRUCTION\_BRANCH\_CONDITIONAL

EU_INSTRUCTION_BRANCH_CONDITIONAL			
DWord	Bit	Description	
0..3	127:64	<b>Sources</b>	
	Exists If:	([Src1.RegFile]!='IMM')	
	Format:	<b>EU_INSTRUCTION_SOURCES_REG_REG</b>	
	127:64	<b>Sources</b>	
	Exists If:	([Src1.RegFile]=='IMM')	
	Format:	<b>EU_INSTRUCTION_SOURCES_REG_IMM</b>	
	63:48	<b>JIP</b>	
	Format:	S15	
	Jump Target Offset. The jump distance in number of eight-byte units if a jump is taken for the instruction.		
47	47	<b>Reserved</b>	
	Format:	MBZ	
	46:44	<b>Src1.SrcType</b>	
	Format:	DataType	
	This field specifies the numeric data type of the source operand src1. The bits of a source operand are interpreted as the identified numeric data type, rather than coerced into a type implied by the operator. Depending on RegFile field of the source operand, there are two different encoding for this field. If a source is a register operand, this field follows the Source Register Type Encoding. If a source is an immediate operand, this field follows the Source Immediate Type Encoding.		
	<b>Programming Notes</b>		
	Both source operands, src0 and src1, support immediate types, but only one immediate is allowed for a given instruction and it must be the last operand.		
	Halfbyte integer vector (v) type can only be used in instructions in packed-word execution mode. Therefore, in a two-source instruction where src1 is of type :v, src0 must be of type :b, :ub, :w, or :uw.		
	43:42	<b>Src1.RegFile</b>	
41:39		Format:	<b>RegFile</b>
41:39	<b>Src0.SrcType</b>		
Format:	DataType		

## EU\_INSTRUCTION\_BRANCH\_CONDITIONAL

	38:37	<b>Src0.RegFile</b>						
		Format: <span style="border: 1px solid black; padding: 2px;"><b>RegFile</b></span>						
	36:34	<b>Destination Data Type</b>						
		Format: <span style="border: 1px solid black; padding: 2px;"><b>DataType</b></span>						
		This field specifies the numeric data type of the destination operand dst. The bits of the destination operand are interpreted as the identified numeric data type, rather than coerced into a type implied by the operator. For a send instruction, this field applies to the CurrDst ? the current destination operand.						
	33:32	<b>Destination Register File</b>						
		Format: <span style="border: 1px solid black; padding: 2px;"><b>RegFile</b></span>						
		<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="background-color: #d3d3d3; text-align: left; padding: 2px;"><b>Value</b></th> <th style="background-color: #d3d3d3; text-align: left; padding: 2px;"><b>Name</b></th> <th style="background-color: #d3d3d3; text-align: left; padding: 2px;"><b>Description</b></th> </tr> </thead> <tbody> <tr> <td style="padding: 2px;">11b</td> <td style="padding: 2px;">Reserved</td> <td style="padding: 2px;">Note that it is obvious that immediate cannot be a destination operand.</td></tr> </tbody> </table>	<b>Value</b>	<b>Name</b>	<b>Description</b>	11b	Reserved	Note that it is obvious that immediate cannot be a destination operand.
<b>Value</b>	<b>Name</b>	<b>Description</b>						
11b	Reserved	Note that it is obvious that immediate cannot be a destination operand.						
	31:0	<b>Header</b>						
		Format: <span style="color: red; border: 1px solid black; padding: 2px;"><b>EU_INSTRUCTION_HEADER</b></span>						

## EU\_INSTRUCTION\_BRANCH\_ONE\_SRC

EU_INSTRUCTION_BRANCH_ONE_SRC				
DWord	Bit	Description		
0..3	127:96	<b>JIP</b>		
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>S31</td></tr> </table> <p>Jump Target Offset. The relative offset in bytes if a jump is taken for the instruction.</p>	Project:	BDW
Project:	BDW			
Format:	S31			
95	<b>Source 0 Address Immediate [9] Sign Bit</b>			
95	<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> </table>	Project:	BDW	
Project:	BDW			
94:91	<b>Src1.SrcType</b>			
	<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>SrcType</td></tr> </table>	Project:	BDW	Format:
Project:	BDW			
Format:	SrcType			
90:89	<b>Src1.RegFile</b>			
	<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>RegFile</td></tr> </table>	Project:	BDW	Format:
Project:	BDW			
Format:	RegFile			
88:64	<b>Source 0</b>			
	<table border="1"> <tr> <td>Exists If:</td><td>(Structure[EU_INSTRUCTION_CONTROLS_A][AccessMode]=='Align16')</td></tr> <tr> <td>Format:</td><td>EU_INSTRUCTION_OPERAND_SRC_REG_ALIGN16</td></tr> </table>	Exists If:	(Structure[EU_INSTRUCTION_CONTROLS_A][AccessMode]=='Align16')	Format:
Exists If:	(Structure[EU_INSTRUCTION_CONTROLS_A][AccessMode]=='Align16')			
Format:	EU_INSTRUCTION_OPERAND_SRC_REG_ALIGN16			
88:64	<b>Source 0</b>			
	<table border="1"> <tr> <td>Exists If:</td><td>(Structure[EU_INSTRUCTION_CONTROLS_A][AccessMode]=='Align1')</td></tr> <tr> <td>Format:</td><td>EU_INSTRUCTION_OPERAND_SRC_REG_ALIGN1</td></tr> </table>	Exists If:	(Structure[EU_INSTRUCTION_CONTROLS_A][AccessMode]=='Align1')	Format:
Exists If:	(Structure[EU_INSTRUCTION_CONTROLS_A][AccessMode]=='Align1')			
Format:	EU_INSTRUCTION_OPERAND_SRC_REG_ALIGN1			
63:32	<b>Operand Control</b>			
63:32	<table border="1"> <tr> <td>Format:</td><td>EU_INSTRUCTION_OPERAND_CONTROLS</td></tr> </table>	Format:	EU_INSTRUCTION_OPERAND_CONTROLS	
Format:	EU_INSTRUCTION_OPERAND_CONTROLS			
31:0	<b>Header</b>			
31:0	<table border="1"> <tr> <td>Format:</td><td>EU_INSTRUCTION_HEADER</td></tr> </table>	Format:	EU_INSTRUCTION_HEADER	
Format:	EU_INSTRUCTION_HEADER			

## EU\_INSTRUCTION\_BRANCH\_TWO\_SRC

EU_INSTRUCTION_BRANCH_TWO_SRC						
DWord	Bit	Description				
0..3	127:96	<b>JIP</b> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>S31</td></tr> </table> <p>The byte-aligned jump distance if a jump is taken for the channel.</p>	Project:	BDW	Format:	S31
Project:	BDW					
Format:	S31					
	95:64	<b>UIP</b> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>S31</td></tr> </table> <p>The byte aligned jump distance if a jump is taken for the instruction.</p>	Project:	BDW	Format:	S31
Project:	BDW					
Format:	S31					
	63:32	<b>Operand Control</b> <table border="1"> <tr> <td>Format:</td><td>EU_INSTRUCTION_OPERAND_CONTROLS</td></tr> </table>	Format:	EU_INSTRUCTION_OPERAND_CONTROLS		
Format:	EU_INSTRUCTION_OPERAND_CONTROLS					
	31:0	<b>Header</b> <table border="1"> <tr> <td>Format:</td><td>EU_INSTRUCTION_HEADER</td></tr> </table>	Format:	EU_INSTRUCTION_HEADER		
Format:	EU_INSTRUCTION_HEADER					

## EU\_INSTRUCTION\_COMPACT\_THREE\_SRC

EU_INSTRUCTION_COMPACT_THREE_SRC				
DWord	Bit	Description		
0..1	63:57	<p><b>Src2.RegNum[6:0]</b></p> <table border="1"> <tr> <td>Format:</td> <td><b>SrcRegNum[6:0]</b></td> </tr> </table> <p>Src2.RegNum[6:0]. The SourceIndex field in the compact instruction determines Src2.RegNum[7].</p> <p>Maps to 124:118</p>	Format:	<b>SrcRegNum[6:0]</b>
Format:	<b>SrcRegNum[6:0]</b>			
	56:50	<p><b>Src1.RegNum[6:0]</b></p> <table border="1"> <tr> <td>Format:</td> <td><b>SrcRegNum[6:0]</b></td> </tr> </table> <p>Src1.RegNum[6:0]. The SourceIndex field in the compact instruction determines Src1.RegNum[7].</p> <p>Maps to 103:97</p>	Format:	<b>SrcRegNum[6:0]</b>
Format:	<b>SrcRegNum[6:0]</b>			
	49:43	<p><b>Src0.RegNum[6:0]</b></p> <table border="1"> <tr> <td>Format:</td> <td><b>SrcRegNum[6:0]</b></td> </tr> </table> <p>Src0.RegNum[6:0]. The SourceIndex field in the compact instruction determines Src0.RegNum[7].</p> <p>Maps to 82:76</p>	Format:	<b>SrcRegNum[6:0]</b>
Format:	<b>SrcRegNum[6:0]</b>			
	42:40	<p><b>Src2.SubRegNum</b></p> <table border="1"> <tr> <td>Format:</td> <td><b>SrcSubRegNum[4:2]</b></td> </tr> </table> <p>Maps to 117:115</p>	Format:	<b>SrcSubRegNum[4:2]</b>
Format:	<b>SrcSubRegNum[4:2]</b>			
	39:37	<p><b>Src1.SubRegNum</b></p> <table border="1"> <tr> <td>Format:</td> <td><b>SrcSubRegNum[4:2]</b></td> </tr> </table> <p>Maps to 96:94</p>	Format:	<b>SrcSubRegNum[4:2]</b>
Format:	<b>SrcSubRegNum[4:2]</b>			
	36:34	<p><b>Src0.SubRegNum</b></p> <table border="1"> <tr> <td>Format:</td> <td><b>SrcSubRegNum[4:2]</b></td> </tr> </table> <p>Maps to 75:73</p>	Format:	<b>SrcSubRegNum[4:2]</b>
Format:	<b>SrcSubRegNum[4:2]</b>			

## EU\_INSTRUCTION\_COMPACT\_THREE\_SRC

	<b>Src2.RepCtrl</b>																	
33	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Format:</td> <td style="padding: 2px; color: red;"><b>RepCtrl</b></td> </tr> </table> <p>Maps to 106</p>	Format:	<b>RepCtrl</b>															
Format:	<b>RepCtrl</b>																	
32	<b>Src1.RepCtrl</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Format:</td> <td style="padding: 2px; color: red;"><b>RepCtrl</b></td> </tr> </table> <p>Maps to 85</p>	Format:	<b>RepCtrl</b>															
Format:	<b>RepCtrl</b>																	
31	<b>Reserved</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Exists If:</td> <td style="padding: 2px;">(Property[Saturation]=='false')</td> </tr> <tr> <td style="padding: 2px;">Format:</td> <td style="padding: 2px;">MBZ</td> </tr> </table>	Exists If:	(Property[Saturation]=='false')	Format:	MBZ													
Exists If:	(Property[Saturation]=='false')																	
Format:	MBZ																	
30	<b>Reserved</b>																	
29	<b>Compaction Control</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Format:</td> <td style="padding: 2px; color: red;"><b>CmptCtrl</b></td> </tr> </table>	Format:	<b>CmptCtrl</b>															
Format:	<b>CmptCtrl</b>																	
28	<b>Src0.RepCtrl</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Format:</td> <td style="padding: 2px; color: red;"><b>RepCtrl</b></td> </tr> </table> <p>Maps to 64</p>	Format:	<b>RepCtrl</b>															
Format:	<b>RepCtrl</b>																	
27:19	<b>Reserved</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Format:</td> <td style="padding: 2px;">MBZ</td> </tr> </table>	Format:	MBZ															
Format:	MBZ																	
18:12	<b>Dst.RegNum[6:0]</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Format:</td> <td style="padding: 2px; color: red;"><b>DstRegNum[6:0]</b></td> </tr> </table> <p>Dst.RegNum[7:0] with MSB of zero and [6:0] from the compact instruction</p> <p>Maps to 63:56 (Dst.RegNum)</p>	Format:	<b>DstRegNum[6:0]</b>															
Format:	<b>DstRegNum[6:0]</b>																	
11:10	<b>SourceIndex</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Project:</td> <td style="padding: 2px;">BDW</td> </tr> </table> <p>Lookup one of four 46-bit values. That value is used (from MSB to LSB) for the Src2.RegNum[7], Src1.RegNum[7], Src0.RegNum[7], Src2.ChanSel, Src1.ChanSel, Src0.ChanSel, Dst.SubRegNum, Dst.ChanEnable, Dst.DstType, SrcType, Src2.Modifier, Src1.Modifier, and Src0.Modifier bit fields.</p> <p>Maps to 125, 104, 83, 114:107, 93:86, 72:65, 55:49, 48:43, 42:37</p> <table border="1" style="width: 100%; border-collapse: collapse; margin-top: 10px;"> <thead> <tr> <th style="background-color: #e0f2e0;">Value</th> <th style="background-color: #e0f2e0;">Name</th> <th style="background-color: #e0f2e0;">Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>00011100100111001001110010000011100000000000000</td> <td>No Negation</td> </tr> <tr> <td>1</td> <td>000111001001110010011100100000111000000000010</td> <td>Negate Src0</td> </tr> <tr> <td>2</td> <td>0001110010011100100111001000001110000000001000</td> <td>Negate Src1</td> </tr> <tr> <td>3</td> <td>0001110010011100100111001000001110000000100000</td> <td>Negate Src2</td> </tr> </tbody> </table>	Project:	BDW	Value	Name	Description	0	00011100100111001001110010000011100000000000000	No Negation	1	000111001001110010011100100000111000000000010	Negate Src0	2	0001110010011100100111001000001110000000001000	Negate Src1	3	0001110010011100100111001000001110000000100000	Negate Src2
Project:	BDW																	
Value	Name	Description																
0	00011100100111001001110010000011100000000000000	No Negation																
1	000111001001110010011100100000111000000000010	Negate Src0																
2	0001110010011100100111001000001110000000001000	Negate Src1																
3	0001110010011100100111001000001110000000100000	Negate Src2																
9:8	<b>ControlIndex</b>																	

## EU\_INSTRUCTION\_COMPACT\_THREE\_SRC

	Project:	BDW
Lookup one of four 24-bit values. That value is used (from MSB to LSB) for the MaskCtrl, FlagRegNum/FlagSubRegNum, AccWrCtrl, CondModifier, ExecSize, PredInv, PredCtrl, ThreadCtrl, QtrCtrl, NibCtrl, DepCtrl, and AccessMode bit fields.		
Maps to 34, 33:32, 28:8		
Value	Name	Description
0	1000000001100000000000001	(8) Q1 NoMask Align16
1	0000000001100000000000001	(8) Q1 Align16
2	0000000010000000000000001	(16) H1 Align16
3	000000001000000000100001	(16) H2 Align16
7	<b>Reserved</b>	
	Format:	MBZ
6:0	<b>Opcode</b>	

## EU\_INSTRUCTION\_COMPACT\_TWO\_SRC

EU_INSTRUCTION_COMPACT_TWO_SRC						
DWord	Bit	Description				
0..1	63:56	<p><b>Src1.RegNum</b></p> <table border="1"> <tr> <td>Exists If:</td><td>([DataTypeIndex][Src1.RegFile]!='IMM')</td></tr> <tr> <td>Format:</td><td><b>SrcRegNum</b></td></tr> </table> <p>Maps to 108:101 (Src1.RegNum)</p>	Exists If:	([DataTypeIndex][Src1.RegFile]!='IMM')	Format:	<b>SrcRegNum</b>
Exists If:	([DataTypeIndex][Src1.RegFile]!='IMM')					
Format:	<b>SrcRegNum</b>					
	63:56	<p><b>Src1.RegNum</b></p> <table border="1"> <tr> <td>Exists If:</td><td>([DataTypeIndex][Src1.RegFile]=='IMM')</td></tr> </table> <p>Maps to 103:96 (Imm32[7:0])</p>	Exists If:	([DataTypeIndex][Src1.RegFile]=='IMM')		
Exists If:	([DataTypeIndex][Src1.RegFile]=='IMM')					
	55:48	<p><b>Src0.RegNum</b></p> <table border="1"> <tr> <td>Format:</td><td><b>SrcRegNum</b></td></tr> </table> <p>Maps to 76:69 (Src0.RegNum)</p>	Format:	<b>SrcRegNum</b>		
Format:	<b>SrcRegNum</b>					
	47:40	<p><b>Dst.RegNum</b></p> <table border="1"> <tr> <td>Format:</td><td><b>DstRegNum</b></td></tr> </table> <p>Maps to 60:53 (Dst.RegNum)</p>	Format:	<b>DstRegNum</b>		
Format:	<b>DstRegNum</b>					
	39:35	<p><b>Src1Index</b></p> <table border="1"> <tr> <td>Exists If:</td><td>([DataTypeIndex][Src1.RegFile]!='IMM')</td></tr> <tr> <td>Format:</td><td><b>SrcIndex</b></td></tr> </table> <p>If not an immediate operand, lookup one of 32 12-bit values that maps to bits 120:109. That value is used (from MSB to LSB) for the Src1.VertStride, various Src1 bit fields based on AccessMode (Src1.ChanSel[7:4], Src1.Width, Src1.HorzStride), Src1.AddrMode, and Src1.SrcMod bit fields</p> <p>Maps to 120:109</p>	Exists If:	([DataTypeIndex][Src1.RegFile]!='IMM')	Format:	<b>SrcIndex</b>
Exists If:	([DataTypeIndex][Src1.RegFile]!='IMM')					
Format:	<b>SrcIndex</b>					

# EU INSTRUCTION COMPACT TWO SRC

39:35	<p><b>Src1Index</b></p> <table border="1"> <tr> <td>Exists If:</td><td>([DataTypeIndex][Src1.RegFile]=='IMM')</td></tr> </table> <p>If an immediate operand, there is no lookup. Determines bits 127:104 (Imm32[31:8]) as follows: map bits 39:35 directly to bits 108:104. Sign extend to fill bits 127:109. Compact format bit 39 is thus copied to all of bits 127:108 for an immediate operand.</p> <p>Maps to 127:104</p>	Exists If:	([DataTypeIndex][Src1.RegFile]=='IMM')		
Exists If:	([DataTypeIndex][Src1.RegFile]=='IMM')				
34:30	<p><b>Src0Index</b></p> <table border="1"> <tr> <td>Format:</td> <td><b>SrcIndex</b></td> </tr> </table> <p>Lookup one of 32 12-bit values. That value is used (from MSB to LSB) for the Src0.VertStride, various Src0 bit fields based on AccessMode (Src0.ChanSel[7:4], Src0.Width, Src0.HorzStride), Src0.AddrMode, and Src0.SrcMod bit fields. Note that this field spans a DWord boundary within the QWord compacted instruction.</p> <p>Maps to 88:77</p>	Format:	<b>SrcIndex</b>		
Format:	<b>SrcIndex</b>				
29	<p><b>Compaction Control</b></p> <table border="1"> <tr> <td>Format:</td> <td>CmptCtrl</td> </tr> </table>	Format:	CmptCtrl		
Format:	CmptCtrl				
28	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ		
Format:	MBZ				
27:24	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Exists If:</td> <td>(Property[Conditional Modifier]=='false')</td> </tr> </table> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Exists If:	(Property[Conditional Modifier]=='false')	Format:	MBZ
Exists If:	(Property[Conditional Modifier]=='false')				
Format:	MBZ				
27:24	<p><b>Conditional Modifier</b></p> <table border="1"> <tr> <td>Exists If:</td> <td>(Property[Conditional Modifier]=='true')</td> </tr> </table> <table border="1"> <tr> <td>Format:</td> <td><b>CondModifier</b></td> </tr> </table>	Exists If:	(Property[Conditional Modifier]=='true')	Format:	<b>CondModifier</b>
Exists If:	(Property[Conditional Modifier]=='true')				
Format:	<b>CondModifier</b>				
23	<p><b>Accumulator Write Control</b></p> <table border="1"> <tr> <td>Format:</td> <td>AccWrCtrl</td> </tr> </table>	Format:	AccWrCtrl		
Format:	AccWrCtrl				

## EU\_INSTRUCTION\_COMPACT\_TWO\_SRC

22:18	<b>SubRegIndex</b>																																																																																																		
	Lookup one of 32 15-bit values. That value is used (from MSB to LSB) for various fields for Src1, Src0, and Dst, including ChanEn/ChanSel, SubRegNum, and AddrImm[4] or AddrImm[4:0], depending on AddrMode and AccessMode.																																																																																																		
	Maps to 100:96, 68:64, 52:48																																																																																																		
	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #e0e0ff;"> <th style="text-align: center;"><b>Value</b></th><th style="text-align: center;"><b>Name</b></th><th style="text-align: center;"><b>Description</b></th></tr> </thead> <tbody> <tr><td style="text-align: center;">0</td><td>0000000000000000</td><td>0   0   0  </td></tr> <tr><td style="text-align: center;">1</td><td>0000000000000001</td><td>0.x   0.xx   0.xx</td></tr> <tr><td style="text-align: center;">2</td><td>0000000000001000</td><td>8   0   0  </td></tr> <tr><td style="text-align: center;">3</td><td>0000000000001111</td><td>0.xyzw   0.xx   0.xx</td></tr> <tr><td style="text-align: center;">4</td><td>0000000000010000</td><td>16   0   0  </td></tr> <tr><td style="text-align: center;">5</td><td>0000000100000000</td><td>0   4   0  </td></tr> <tr><td style="text-align: center;">6</td><td>0000001000000000</td><td>0   8   0  </td></tr> <tr><td style="text-align: center;">7</td><td>0000001100000000</td><td>0   12   0  </td></tr> <tr><td style="text-align: center;">8</td><td>0000010000000000</td><td>0   16   0  </td></tr> <tr><td style="text-align: center;">9</td><td>000001000010000</td><td>16   16   0  </td></tr> <tr><td style="text-align: center;">10</td><td>0000010100000000</td><td>0   20   0  </td></tr> <tr><td style="text-align: center;">11</td><td>0010000000000000</td><td>0   0   4  </td></tr> <tr><td style="text-align: center;">12</td><td>0010000000000001</td><td>0.x   0.xx   0.xy</td></tr> <tr><td style="text-align: center;">13</td><td>0010000100000001</td><td>0.x   0.xy   0.xy</td></tr> <tr><td style="text-align: center;">14</td><td>001000010000010</td><td>0.y   0.xy   0.xy</td></tr> <tr><td style="text-align: center;">15</td><td>001000010000011</td><td>0.xy   0.xy   0.xy</td></tr> <tr><td style="text-align: center;">16</td><td>001000010000100</td><td>0.z   0.xy   0.xy</td></tr> <tr><td style="text-align: center;">17</td><td>001000010000111</td><td>0.xyz   0.xy   0.xy</td></tr> <tr><td style="text-align: center;">18</td><td>001000010001000</td><td>0.w   0.xy   0.xy</td></tr> <tr><td style="text-align: center;">19</td><td>001000010001110</td><td>0.yzw   0.xy   0.xy</td></tr> <tr><td style="text-align: center;">20</td><td>001000010001111</td><td>0.xyzw   0.xy   0.xy</td></tr> <tr><td style="text-align: center;">21</td><td>001000110000000</td><td>0   12   4  </td></tr> <tr><td style="text-align: center;">22</td><td>001000111101000</td><td>0.w   0.ww   0.xy</td></tr> <tr><td style="text-align: center;">23</td><td>0100000000000000</td><td>0   0   8  </td></tr> <tr><td style="text-align: center;">24</td><td>0100001100000000</td><td>0   12   8  </td></tr> <tr><td style="text-align: center;">25</td><td>0110000000000000</td><td>0   0   12  </td></tr> <tr><td style="text-align: center;">26</td><td>011110010000111</td><td>0.xyz   0.xy   0.ww</td></tr> <tr><td style="text-align: center;">27</td><td>1000000000000000</td><td>0   0   16  </td></tr> <tr><td style="text-align: center;">28</td><td>1010000000000000</td><td>0   0   20  </td></tr> <tr><td style="text-align: center;">29</td><td>1100000000000000</td><td>0   0   24  </td></tr> <tr><td style="text-align: center;">30</td><td>1110000000000000</td><td>0   0   28  </td></tr> <tr><td style="text-align: center;">31</td><td>111000000011100</td><td>28   0   28  </td></tr> </tbody> </table>	<b>Value</b>	<b>Name</b>	<b>Description</b>	0	0000000000000000	0   0   0	1	0000000000000001	0.x   0.xx   0.xx	2	0000000000001000	8   0   0	3	0000000000001111	0.xyzw   0.xx   0.xx	4	0000000000010000	16   0   0	5	0000000100000000	0   4   0	6	0000001000000000	0   8   0	7	0000001100000000	0   12   0	8	0000010000000000	0   16   0	9	000001000010000	16   16   0	10	0000010100000000	0   20   0	11	0010000000000000	0   0   4	12	0010000000000001	0.x   0.xx   0.xy	13	0010000100000001	0.x   0.xy   0.xy	14	001000010000010	0.y   0.xy   0.xy	15	001000010000011	0.xy   0.xy   0.xy	16	001000010000100	0.z   0.xy   0.xy	17	001000010000111	0.xyz   0.xy   0.xy	18	001000010001000	0.w   0.xy   0.xy	19	001000010001110	0.yzw   0.xy   0.xy	20	001000010001111	0.xyzw   0.xy   0.xy	21	001000110000000	0   12   4	22	001000111101000	0.w   0.ww   0.xy	23	0100000000000000	0   0   8	24	0100001100000000	0   12   8	25	0110000000000000	0   0   12	26	011110010000111	0.xyz   0.xy   0.ww	27	1000000000000000	0   0   16	28	1010000000000000	0   0   20	29	1100000000000000	0   0   24	30	1110000000000000	0   0   28	31	111000000011100
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3	0000000000001111	0.xyzw   0.xx   0.xx																																																																																																	
4	0000000000010000	16   0   0																																																																																																	
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31	111000000011100	28   0   28																																																																																																	

## EU\_INSTRUCTION\_COMPACT\_TWO\_SRC

17:13	<b>DataTypeIDex</b>		
	Lookup one of 32 21-bit values. That value is used (from MSB to LSB) for the Dst.AddrMode, Dst.HorzStride, Src1.SrcType, Src1.RegFile, Src0.SrcType, Src0.RegFile, Dst.DstType, and Dst.RegFile bit fields.		
	Maps to 63:61, 94:89, 46:35		
Value	Name	Description	
0	00100000000000000000000000000000	r:ud   a:ud   a:ud   <1>   dir	
1	001000000000000010000000	a:ud   r:ud   a:ud   <1>   dir	
2	001000000000000010000001	r:ud   r:ud   a:ud   <1>   dir	
3	001000000000000011000001	r:ud   i:ud   a:ud   <1>   dir	
4	001000000000101011101	r:f   r:d   a:ud   <1>   dir	
5	001000000010111011101	r:f   i:vf   a:ud   <1>   dir	
6	0010000000111010000001	r:ud   r:f   a:ud   <1>   dir	
7	0010000000111010000101	r:d   r:f   a:ud   <1>   dir	
8	001000000011101011101	r:f   r:f   a:ud   <1>   dir	
9	0010000010000010000001	r:ud   r:ud   r:ud   <1>   dir	
10	0010000110000010000000	a:ud   r:ud   i:ud   <1>   dir	
11	0010000110000010000001	r:ud   r:ud   i:ud   <1>   dir	
12	001000101000101000101	r:d   r:d   r:d   <1>   dir	
13	001000111000101000100	a:d   r:d   i:d   <1>   dir	
14	001000111000101000101	r:d   r:d   i:d   <1>   dir	
15	001011100011101011101	r:f   r:f   a:f   <1>   dir	
16	001011101011100011101	r:f   a:f   r:f   <1>   dir	
17	001011101011101011100	a:f   r:f   r:f   <1>   dir	
18	001011101011101011101	r:f   r:f   r:f   <1>   dir	
19	001011111011101011100	a:f   r:f   i:f   <1>   dir	
20	000000000010000001100	a:w   a:ub   a:ud   <0>   dir	
21	0010000000000001011101	r:f   r:ud   a:ud   <1>   dir	
22	0010000000000101000101	r:d   r:d   a:ud   <1>   dir	
23	0010000010000010000000	a:ud   r:ud   r:ud   <1>   dir	
24	001000101000101000100	a:d   r:d   r:d   <1>   dir	
25	001000111000100000100	a:d   a:d   i:d   <1>   dir	
26	001001001001000001001	r:uw   a:uw   r:uw   <1>   dir	
27	001010111011101011101	r:f   r:f   i:vf   <1>   dir	
28	001011111011101011101	r:f   r:f   i:f   <1>   dir	
29	001001111001101001100	a:w   r:w   i:w   <1>   dir	

## EU\_INSTRUCTION\_COMPACT\_TWO\_SRC

		30	001001001001001001000	a:uw   r:uw   r:uw   <1>   dir
		31	001001011001001001000	a:uw   r:uw   i:uw   <1>   dir
12:8	<b>ControlIndex</b>			
	Lookup one of 32 19-bit values. That value is used (from MSB to LSB) for the FlagRegNum, FlagSubRegNum, Saturate, ExecSize, PredInv, PredCtrl, ThreadCtrl, QtrCtrl, DepCtrl, MaskCtrl, and AccessMode bit fields.			
	Maps to 33:32, 31, 23:12, 10:9, 34, 8			
Value	Name	Description		
0	0000000000000000000010	Align1   We   (1)   f0.0		
1	0000100000000000000000	Align1   (4)   f0.0		
2	0000100000000000000001	Align16   (4)   f0.0		
3	0000100000000000000010	Align1   We   (4)   f0.0		
4	0000100000000000000011	Align16   We   (4)   f0.0		
5	00001000000000000000100	Align1   NoDDClr   (4)   f0.0		
6	00001000000000000000101	Align16   NoDDClr   (4)   f0.0		
7	00001000000000000000111	Align16   We   NoDDClr   (4)   f0.0		
8	00001000000000001000	Align1   NoDDChk   (4)   f0.0		
9	00001000000000001001	Align16   NoDDChk   (4)   f0.0		
10	00001000000000001101	Align16   NoDDClr, NoDDChk   (4)   f0.0		
11	00001100000000000000	Align1   Q1   (8)   f0.0		
12	00001100000000000001	Align16   Q1   (8)   f0.0		
13	0000110000000000000010	Align1   We   Q1   (8)   f0.0		
14	0000110000000000000011	Align16   We   Q1   (8)   f0.0		
15	00001100000000000000100	Align1   NoDDClr   Q1   (8)   f0.0		
16	00001100000000000000101	Align16   NoDDClr   Q1   (8)   f0.0		
17	00001100000000000000111	Align16   We   NoDDClr   Q1   (8)   f0.0		
18	00001100000000001001	Align16   NoDDChk   Q1   (8)   f0.0		
19	00001100000000001101	Align16   NoDDClr, NoDDChk   Q1   (8)   f0.0		
20	000011000000000010000	Align1   Q2   (8)   f0.0		
21	000011000010000000	Align1   Q1   +f.xyzw   (8)   f0.0		
22	00010000000000000000	Align1   H1   (16)   f0.0		
23	0001000000000000000010	Align1   We   H1   (16)   f0.0		
24	00010000000000000000100	Align1   NoDDClr   H1   (16)   f0.0		
25	000100000010000000	Align1   H1   +f.xyzw   (16)   f0.0		
26	00101100000000000000	Align1   Q1   (8)   .sat   f0.0		
27	001011000000000010000	Align1   Q2   (8)   .sat   f0.0		

EU_INSTRUCTION_COMPACT_TWO_SRC				
	28	00110000000000000000	Align1   H1   (16)   .sat   f0.0	
	29	001100000010000000	Align1   H1   +f.xyzw   (16)   .sat   f0.0	
	30	01010000000000000000	Align1   H1   (16)   f0.1	
	31	010100000010000000	Align1   H1   +f.xyzw   (16)   f0.1	
	7	<b>Reserved</b>		
	6:0	<b>Opcode</b>		

## EU\_INSTRUCTION\_CONTROLS\_A

EU_INSTRUCTION_CONTROLS_A														
DWord	Bit	Description												
0	15:13	<b>ExecSize</b> <table border="1"> <tr> <td>Format:</td> <td><b>ExecSize</b></td> </tr> </table> <p>This field determines the number of channels operating in parallel for this instruction. The size cannot exceed the maximum number of channels allowed for the given data type.</p>		Format:	<b>ExecSize</b>									
Format:	<b>ExecSize</b>													
	12	<b>Reserved</b> <table border="1"> <tr> <td>Exists If:</td> <td>(Property[Predication]=='false')</td> </tr> </table>		Exists If:	(Property[Predication]=='false')									
Exists If:	(Property[Predication]=='false')													
	12	<b>PredInv</b> <table border="1"> <tr> <td>Exists If:</td> <td>(Property[Predication]=='true')</td> </tr> </table> <p>This field, together with PredCtrl, enables and controls the generation of the predication mask for the instruction. When it is set, the predication uses the inverse of the predication bits generated according to setting of Predicate Control. In other words, effect of PredInv happens after PredCtrl. This field is ignored by hardware if Predicate Control is set to 0000 - there is no predication. PMask is the final predication mask produced by the effects of both fields.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Positive <b>[Default]</b></td> <td>Positive polarity of predication. Use the predication mask produced by PredCtrl</td> </tr> <tr> <td>1</td> <td>Negative</td> <td>Negative polarity of predication. If PredCtrl is nonzero, invert the predication mask.</td> </tr> </tbody> </table>		Exists If:	(Property[Predication]=='true')	Value	Name	Description	0	Positive <b>[Default]</b>	Positive polarity of predication. Use the predication mask produced by PredCtrl	1	Negative	Negative polarity of predication. If PredCtrl is nonzero, invert the predication mask.
Exists If:	(Property[Predication]=='true')													
Value	Name	Description												
0	Positive <b>[Default]</b>	Positive polarity of predication. Use the predication mask produced by PredCtrl												
1	Negative	Negative polarity of predication. If PredCtrl is nonzero, invert the predication mask.												
	11:8	<b>Reserved</b> <table border="1"> <tr> <td>Exists If:</td> <td>(Property[Predication]=='false')</td> </tr> <tr> <td>Format:</td> <td><b>PredCtrl</b></td> </tr> </table>		Exists If:	(Property[Predication]=='false')	Format:	<b>PredCtrl</b>							
Exists If:	(Property[Predication]=='false')													
Format:	<b>PredCtrl</b>													
	11:8	<b>PredCtrl</b> <table border="1"> <tr> <td>Exists If:</td> <td>(Property[Predication]=='true')</td> </tr> <tr> <td>Format:</td> <td><b>PredCtrl</b></td> </tr> </table> <p>This field, together with PredInv, enables and controls the generation of the predication mask for the instruction. It allows per-channel conditional execution of the instruction based on the content of the selected flag register. Encoding depends on the access mode. In Align16 access mode, there are eight encodings (including no predication). All encodings are based on group-of-4 predicate bits, including channel sequential, replication swizzles and horizontal any all operations. The same configuration is repeated for each group-of-4 execution channels.</p>		Exists If:	(Property[Predication]=='true')	Format:	<b>PredCtrl</b>							
Exists If:	(Property[Predication]=='true')													
Format:	<b>PredCtrl</b>													

## EU\_INSTRUCTION\_CONTROLS\_A

	7:6	<b>Thread Control</b>									
		<table border="1" style="width: 100%;"> <tr> <td style="padding: 2px;">Format:</td> <td style="padding: 2px; text-align: right;"><b>ThreadCtrl</b></td> </tr> </table>	Format:	<b>ThreadCtrl</b>							
Format:	<b>ThreadCtrl</b>										
<p>Thread Control. This field provides explicit control for thread switching. If this field is set to 00b, it is up to the GEN execution units to manage thread switching. This is the normal (and unnamed) mode. In this mode, for example, if the current instruction cannot proceed due to operand dependencies, the EU switches to the next available thread to fill the compute pipe. In another example, if the current instruction is ready to go, however, there is another thread with higher priority that also has an instruction ready, the EU switches to that thread. If this field is set to Switch, a forced thread switch occurs after the current instruction is executed and before the next instruction. In addition, a long delay (longer than the execution pipe latency) is introduced for the current thread. Particularly, the instruction queue of the current thread is flushed after the current instruction is dispatched for execution. Switch is designed primarily as a safety feature in case there are race conditions for certain instructions.</p>											
	5:4	<b>QtrCtrl</b>									
		<table border="1" style="width: 100%;"> <tr> <td style="padding: 2px;">Format:</td> <td style="padding: 2px; text-align: right;"><b>QtrCtrl</b></td> </tr> </table>	Format:	<b>QtrCtrl</b>							
Format:	<b>QtrCtrl</b>										
<p><b>Quarter Control.</b></p> <p>This field provides explicit control for ARF selection. This field combined with NibCtrl and ExecSize determines which channels are used for the ARF registers.</p>											
	3	<b>NibCtrl</b>									
<p>Nibble Control. This field is used in some instructions along with QtrCtrl. See the description of QtrCtrl below. NibCtrl is only used for SIMD4 instructions with a DF (Double Float) source or destination.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #d9e1f2;"> <th style="width: 10%;">Value</th> <th style="width: 10%;">Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">Odd</td> <td>Use an odd 1/8th for DMask/VMask and ARF (first, third, fifth, or seventh depending on QtrCtrl).</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">Even</td> <td>Use an even 1/8th for DMask/VMask and ARF (second, fourth, sixth, or eighth depending on QtrCtrl).</td> </tr> </tbody> </table> <p style="text-align: center;"><b>Programming Notes</b></p> <p>Note that if eighths are given zero-based indices from 0 to 7, then NibCtrl = 0 indicates even indices and NibCtrl = 1 indicates odd indices.</p>			Value	Name	Description	0	Odd	Use an odd 1/8th for DMask/VMask and ARF (first, third, fifth, or seventh depending on QtrCtrl).	1	Even	Use an even 1/8th for DMask/VMask and ARF (second, fourth, sixth, or eighth depending on QtrCtrl).
Value	Name	Description									
0	Odd	Use an odd 1/8th for DMask/VMask and ARF (first, third, fifth, or seventh depending on QtrCtrl).									
1	Even	Use an even 1/8th for DMask/VMask and ARF (second, fourth, sixth, or eighth depending on QtrCtrl).									

## EU\_INSTRUCTION\_CONTROLS\_A

2:1	<p><b>DepCtrl</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Format:</td><td style="padding: 2px;"><b>DepCtrl</b></td></tr> </table> <p>Destination Dependency Control. This field selectively disables destination dependency check and clear for this instruction. When it is set to 00, normal destination dependency control is performed for the instruction - hardware checks for destination hazards to ensure data integrity. Specifically, destination register dependency check is conducted before the instruction is made ready for execution. After the instruction is executed, the destination register scoreboard will be cleared when the destination operands retire. When bit 10 is set (NoDDCir), the destination register scoreboard will NOT be cleared when the destination operands retire. When bit 11 is set (NoDDChk), hardware does not check for destination register dependency before the instruction is made ready for execution. NoDDCir and NoDDChk are not mutual exclusive. When this field is not all-zero, hardware does not protect against destination hazards for the instruction. This is typically used to assemble data in a fine grained fashion (e.g. matrix-vector compute with dot-product instructions), where the data integrity is guaranteed by software based on the intended usage of instruction sequences.</p>	Format:	<b>DepCtrl</b>				
Format:	<b>DepCtrl</b>						
0	<p><b>AccessMode</b></p> <p>Access Mode. This field determines the operand access for the instruction. It applies to all source and destination operands. When it is cleared (Align1), the instruction uses byte-aligned addressing for source and destination operands. Source swizzle control and destination mask control are not supported. When it is set (Align16), the instruction uses 16-byte-aligned addressing for all source and destination operands. Source swizzle control and destination mask control are supported in this mode.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="background-color: #d9e1f2; text-align: center; padding: 2px;">Value</th><th style="background-color: #d9e1f2; text-align: center; padding: 2px;">Name</th></tr> </thead> <tbody> <tr> <td style="text-align: center; padding: 2px;">0</td><td style="text-align: center; padding: 2px;">Align1 <b>[Default]</b></td></tr> <tr> <td style="text-align: center; padding: 2px;">1</td><td style="text-align: center; padding: 2px;">Align16</td></tr> </tbody> </table>	Value	Name	0	Align1 <b>[Default]</b>	1	Align16
Value	Name						
0	Align1 <b>[Default]</b>						
1	Align16						

## EU\_INSTRUCTION\_CONTROLS\_B

EU_INSTRUCTION_CONTROLS_B											
DWord	Bit	Description									
0	3	<b>Reserved</b>									
		Exists If:	(Property[Saturation]=='false')								
	3	Format:	MBZ								
0	2	<b>Saturate</b>									
	3	Exists If:	(Property[Saturation]=='true')								
	2	Enables or disables destination saturation. When it is set, output values to the destination register are saturated. The saturation operation depends on the destination data type. Saturation is the operation that converts any value outside the saturation target range for the data type to the closest value in the target range. For a floating-point destination type, the saturation target range is [0.0, 1.0]. For a floating-point NaN, there is no <i>closest value</i> ; any NaN saturates to 0.0. Note that enabling Saturate overrides all of the NaN propagation behaviors described for various numeric instructions. Any floating-point number greater than 1.0, including +INF, saturates to 1.0. Any negative floating-point number, including -INF, saturates to 0.0. Any floating-point number in the range 0.0 to 1.0 is not changed by saturation. For an integer destination type, the maximum range for that type is the saturation target range. For example, the saturation range for B (Signed Byte Integer) is [-128, 127]. When Saturate is clear, destination values are not saturated. For example, a wrapped result (modulo) is output to the destination for an overflowed integer value. See the Numeric Data Types section for information about data types and their ranges.									
	1	<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>No destination modification <b>[Default]</b></td> <td></td> </tr> <tr> <td>1</td> <td>sat</td> <td>Saturate the output</td> </tr> </tbody> </table>		Value	Name	Description	0	No destination modification <b>[Default]</b>		1	sat
Value	Name	Description									
0	No destination modification <b>[Default]</b>										
1	sat	Saturate the output									
2 Reserved											

## EU\_INSTRUCTION\_CONTROLS\_B

	<b>CmptCtrl</b>	Compaction Control Indicates whether the instruction is compacted to the 64-bit compact instruction format. When this bit is set, the 64-bit compact instruction format is used. The EU decodes the compact format using lookup tables internal to the hardware, but documented for use by software tools. Only some instruction variations can be compacted, the variations supported by those lookup tables and the compact format. See EU Compact Instruction Format [BDW] for more information.	
1	<b>Value</b>	<b>Name</b>	<b>Description</b>
	0	NoCompaction	No compaction. 128-bit native instruction supporting all instruction options.
0	<b>Value</b>	<b>Name</b>	<b>Description</b>
	1	Compacted	Compaction is enabled. 64-bit compact instruction supporting only some instruction variations.
0	<b>AccWrCtrl</b>	AccWrCtrl. This field allows per instruction accumulator write control.	
	<b>Value</b>	<b>Name</b>	<b>Description</b>
0	0	Don't write to ACC <b>[Default]</b>	
	1	Update ACC	Write result to the ACC, and destination

## EU\_INSTRUCTION\_CONTROLS

EU_INSTRUCTION_CONTROLS					
DWord	Bit	Description			
0	23:20	<b>Controls B</b> <table border="1"> <tr> <td>Format:</td> <td><b>EU_INSTRUCTION_CONTROLS_B</b></td> </tr> </table>	Format:	<b>EU_INSTRUCTION_CONTROLS_B</b>	
Format:	<b>EU_INSTRUCTION_CONTROLS_B</b>				
19:16	<b>Reserved</b> <table border="1"> <tr> <td>Exists If:</td> <td>(Property[Conditional Modifier]=='false')</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Exists If:	(Property[Conditional Modifier]=='false')	Format:	MBZ
Exists If:	(Property[Conditional Modifier]=='false')				
Format:	MBZ				
19:16	<b>CondModifier</b> <table border="1"> <tr> <td>Exists If:</td> <td>(Property[Conditional Modifier]=='true')</td> </tr> <tr> <td>Format:</td> <td><b>CondModifier</b></td> </tr> </table> <p>Does not exist for send/sendc/math/branch/break-continue opcodes</p>	Exists If:	(Property[Conditional Modifier]=='true')	Format:	<b>CondModifier</b>
Exists If:	(Property[Conditional Modifier]=='true')				
Format:	<b>CondModifier</b>				
15:0	<b>Controls A</b> <table border="1"> <tr> <td>Format:</td> <td><b>EU_INSTRUCTION_CONTROLS_A</b></td> </tr> </table>	Format:	<b>EU_INSTRUCTION_CONTROLS_A</b>		
Format:	<b>EU_INSTRUCTION_CONTROLS_A</b>				

## EU\_INSTRUCTION\_HEADER

EU_INSTRUCTION_HEADER				
DWord	Bit	Description		
0	31:8	<b>Control</b> <table border="1"> <tr> <td>Format:</td> <td>EU_INSTRUCTION_CONTROLS</td> </tr> </table>	Format:	EU_INSTRUCTION_CONTROLS
Format:	EU_INSTRUCTION_CONTROLS			
7	<b>Reserved</b> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ	
Format:	MBZ			
6:0	<b>Opcode</b> <table border="1"> <tr> <td>Format:</td> <td>EU_OPCODE</td> </tr> </table>	Format:	EU_OPCODE	
Format:	EU_OPCODE			

## EU\_INSTRUCTION\_ILLEGAL

EU_INSTRUCTION_ILLEGAL				
DWord	Bit	Description		
0..3	127:7	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ
Format:	MBZ			
6:0	<p><b>Opcode</b></p> <table border="1"> <tr> <td>Format:</td> <td>EU_OPCODE</td> </tr> </table>	Format:	EU_OPCODE	
Format:	EU_OPCODE			

## EU\_INSTRUCTION\_MATH

EU_INSTRUCTION_MATH		
DWord	Bit	Description
0..3	127:64	<b>RegSource</b> Format: EU_INSTRUCTION_SOURCES_REG_REG
	63:32	<b>Operand Control</b> Format: EU_INSTRUCTION_OPERAND_CONTROLS
	31:28	<b>Controls B</b> Format: EU_INSTRUCTION_CONTROLS_B
	27:24	<b>Function Control (FC)</b> Format: FC
	23:8	<b>Controls A</b> Format: EU_INSTRUCTION_CONTROLS_A
	7	<b>Reserved</b> Format: MBZ
	6:0	<b>Opcode</b> Format: EU_OPCODE

## EU\_INSTRUCTION\_NOP

EU_INSTRUCTION_NOP				
Project:	BDW			
Source:	Eulsa			
Size (in bits):	128			
Default Value:	0x00000000, 0x00000000, 0x00000000, 0x00000000			
DWord	Bit	Description		
0..3	127:31	<b>Reserved</b> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ
Format:	MBZ			
30	<b>Reserved</b>			
29:7	<b>Reserved</b> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ	
Format:	MBZ			
6:0	<b>Opcode</b> <table border="1"> <tr> <td>Format:</td> <td>EU_OPCODE</td> </tr> </table>	Format:	EU_OPCODE	
Format:	EU_OPCODE			

## EU\_INSTRUCTION\_OPERAND\_CONTROLS

EU_INSTRUCTION_OPERAND_CONTROLS		
DWord	Bit	Description
0	31:16	<b>Destination Register Region</b>
		Exists If: (Structure[EU_INSTRUCTION_CONTROLS_A][AccessMode]=='Align16')
	31:16	Format: EU_INSTRUCTION_OPERAND_DST_ALIGN16
		Exists If: (Structure[EU_INSTRUCTION_CONTROLS_A][AccessMode]=='Align1')
		Format: EU_INSTRUCTION_OPERAND_DST_ALIGN1
	15	<b>Reserved</b>
		Exists If: ([Destination Register Region][Destination Addressing Mode]=='Direct')
	15	<b>Destination Address Immediate[9:9]</b>
		Exists If: ([Destination Register Region][Destination Addressing Mode]=='Indirect')
		Format: U1
	14:11	<b>Src0.SrcType</b>
		Exists If: ([Src0.RegFile]!='IMM')
	14:11	Format: SrcType
		Exists If: ([Src0.RegFile]=='IMM')
		Format: SrcImmType
	10:9	<b>Src0.RegFile</b>
	Format: RegFile	
	8:5	<b>Destination Data Type</b>
	Format: DstType	
	This field specifies the numeric data type of the destination operand dst. The bits of the destination operand are interpreted as the identified numeric data type, rather than coerced into a type implied by the operator. For a send instruction, this field applies to the CurrDst - the current destination operand.	

## EU\_INSTRUCTION\_OPERAND\_CONTROLS

	4:3	<b>Destination Register File</b>								
		Format:		<b>RegFile</b>						
	2	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="background-color: #d9e1f2;">Value</th><th style="background-color: #d9e1f2;">Name</th><th style="background-color: #d9e1f2;">Description</th></tr> </thead> <tbody> <tr> <td>11b</td><td>Reserved</td><td>Note that it is obvious that immediate cannot be a destination operand.</td></tr> </tbody> </table>		Value	Name	Description	11b	Reserved	Note that it is obvious that immediate cannot be a destination operand.	
Value	Name	Description								
11b	Reserved	Note that it is obvious that immediate cannot be a destination operand.								
<b>MaskCtrl</b> Mask Control (formerly Write Enable Control). This field determines if the per channel write enables are used to generate the final write enable. This field should be normally "0". <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="background-color: #d9e1f2;">Value</th><th style="background-color: #d9e1f2;">Name</th><th style="background-color: #d9e1f2;">Description</th></tr> </thead> <tbody> <tr> <td>0</td><td>Normal <b>[Default]</b></td><td></td></tr> <tr> <td>1</td><td>Write all channels</td><td>Except channels killed with predication control</td></tr> </tbody> </table>		Value	Name	Description	0	Normal <b>[Default]</b>		1	Write all channels	Except channels killed with predication control
Value	Name	Description								
0	Normal <b>[Default]</b>									
1	Write all channels	Except channels killed with predication control								
<b>Programming Notes</b>										
MaskCtrl = NoMask skips the check for PclP[n] == ExIP before enabling a channel, as described in the Evaluate Write Enable section.										
1:0 <b>Flag Register Number/Subregister Number</b>										

## EU\_INSTRUCTION\_OPERAND\_DST\_ALIGN1

EU_INSTRUCTION_OPERAND_DST_ALIGN1								
DWord	Bit	Description						
0	15	<p><b>Destination Addressing Mode</b></p> <table border="1"> <tr> <td>Format:</td> <td><b>AddrMode</b></td> </tr> </table> <p>For a send instruction, this field applies to PostDst - the post destination operand. Addressing mode for CurrDst (current destination operand) is fixed as Direct. (See Instruction Reference chapter for CurrDst and PostDst.)</p>	Format:	<b>AddrMode</b>				
Format:	<b>AddrMode</b>							
	14:13	<p><b>Destination Horizontal Stride</b></p> <table border="1"> <tr> <td>Format:</td> <td><b>HorzStride</b></td> </tr> </table> <p>For a send instruction, this field applies to CurrDst. PostDst only uses the register number.</p>	Format:	<b>HorzStride</b>				
Format:	<b>HorzStride</b>							
	12:9	<p><b>Destination Address Subregister Number</b></p> <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Exists If:</td> <td>([Destination Addressing Mode]=='Indirect')</td> </tr> <tr> <td>Format:</td> <td><b>AddrSubRegNum</b></td> </tr> </table> <p>For a send instruction, this field applies to PostDst</p>	Project:	BDW	Exists If:	([Destination Addressing Mode]=='Indirect')	Format:	<b>AddrSubRegNum</b>
Project:	BDW							
Exists If:	([Destination Addressing Mode]=='Indirect')							
Format:	<b>AddrSubRegNum</b>							
	12:5	<p><b>Destination Register Number</b></p> <table border="1"> <tr> <td>Exists If:</td> <td>([Destination Addressing Mode]=='Direct')</td> </tr> <tr> <td>Format:</td> <td><b>DstRegNum</b></td> </tr> </table> <p>For a send instruction, this field applies to PostDst.</p>	Exists If:	([Destination Addressing Mode]=='Direct')	Format:	<b>DstRegNum</b>		
Exists If:	([Destination Addressing Mode]=='Direct')							
Format:	<b>DstRegNum</b>							
	8:0	<p><b>Destination Address Immediate</b></p> <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Exists If:</td> <td>([Destination Addressing Mode]=='Indirect')</td> </tr> <tr> <td>Format:</td> <td>S8</td> </tr> </table> <p>For a send instruction, this field applies to PostDst.</p>	Project:	BDW	Exists If:	([Destination Addressing Mode]=='Indirect')	Format:	S8
Project:	BDW							
Exists If:	([Destination Addressing Mode]=='Indirect')							
Format:	S8							
	4:0	<p><b>Destination Subregister Number</b></p> <table border="1"> <tr> <td>Exists If:</td> <td>([Destination Addressing Mode]=='Direct')</td> </tr> <tr> <td>Format:</td> <td><b>DstSubRegNum</b></td> </tr> </table> <p>For a send instruction, this field applies to CurrDst.</p>	Exists If:	([Destination Addressing Mode]=='Direct')	Format:	<b>DstSubRegNum</b>		
Exists If:	([Destination Addressing Mode]=='Direct')							
Format:	<b>DstSubRegNum</b>							

## EU\_INSTRUCTION\_OPERAND\_DST\_ALIGN16

EU_INSTRUCTION_OPERAND_DST_ALIGN16								
DWord	Bit	Description						
0	15	<p><b>Destination Addressing Mode</b></p> <table border="1"> <tr> <td>Format:</td> <td><b>AddrMode</b></td> </tr> </table> <p>For a send instruction, this field applies to PostDst - the post destination operand. Addressing mode for CurrDst (current destination operand) is fixed as Direct. (See Instruction Reference chapter for CurrDst and PostDst.)</p>	Format:	<b>AddrMode</b>				
Format:	<b>AddrMode</b>							
	14:13	<p><b>Reserved</b></p> <table border="1"> <tr> <th>Value</th> <th>Name</th> </tr> <tr> <td>01b</td> <td>See Programming Note</td> </tr> </table> <p><b>Programming Notes</b></p> <p>Although Dst.HorzStride is a don't care for Align16, HW needs this to be programmed as ?01?.</p>	Value	Name	01b	See Programming Note		
Value	Name							
01b	See Programming Note							
	12:9	<p><b>Destination Address Subregister Number</b></p> <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Exists If:</td> <td>([Destination Addressing Mode]=='Indirect')</td> </tr> <tr> <td>Format:</td> <td><b>AddrSubRegNum</b></td> </tr> </table> <p>For a send instruction, this field applies to PostDst</p>	Project:	BDW	Exists If:	([Destination Addressing Mode]=='Indirect')	Format:	<b>AddrSubRegNum</b>
Project:	BDW							
Exists If:	([Destination Addressing Mode]=='Indirect')							
Format:	<b>AddrSubRegNum</b>							
	12:5	<p><b>Destination Register Number</b></p> <table border="1"> <tr> <td>Exists If:</td> <td>([Destination Addressing Mode]=='Direct')</td> </tr> <tr> <td>Format:</td> <td><b>DstRegNum</b></td> </tr> </table> <p>For a send instruction, this field applies to PostDst.</p>	Exists If:	([Destination Addressing Mode]=='Direct')	Format:	<b>DstRegNum</b>		
Exists If:	([Destination Addressing Mode]=='Direct')							
Format:	<b>DstRegNum</b>							
	8:4	<p><b>Destination Address Immediate[8:4]</b></p> <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Exists If:</td> <td>([Destination Addressing Mode]=='Indirect')</td> </tr> <tr> <td>Format:</td> <td>S8[8:4]</td> </tr> </table> <p>For a send instruction, this field applies to PostDst</p>	Project:	BDW	Exists If:	([Destination Addressing Mode]=='Indirect')	Format:	S8[8:4]
Project:	BDW							
Exists If:	([Destination Addressing Mode]=='Indirect')							
Format:	S8[8:4]							

EU_INSTRUCTION_OPERAND_DST_ALIGN16						
	4	<b>Destination Subregister Number</b> <table border="1"> <tr> <td>Exists If:</td><td>([Destination Addressing Mode] == 'Direct')</td></tr> <tr> <td>Format:</td><td><b>DstSubRegNum[4:4]</b></td></tr> </table> <p>For a send instruction, this field applies to CurrDst.</p>	Exists If:	([Destination Addressing Mode] == 'Direct')	Format:	<b>DstSubRegNum[4:4]</b>
Exists If:	([Destination Addressing Mode] == 'Direct')					
Format:	<b>DstSubRegNum[4:4]</b>					
	3:0	<b>Destination Channel Enable</b> <table border="1"> <tr> <td>Format:</td><td><b>ChanEn[4]</b></td></tr> </table> <p>For a send instruction, this field applies to the CurrDst</p>	Format:	<b>ChanEn[4]</b>		
Format:	<b>ChanEn[4]</b>					

## EU\_INSTRUCTION\_OPERAND\_SEND\_MSG

EU_INSTRUCTION_OPERAND_SEND_MSG												
DWord	Bit	Description										
0	31	<p><b>EOT</b></p> <table border="1"> <thead> <tr> <th colspan="2">Description</th> </tr> </thead> <tbody> <tr> <td colspan="2">This field controls the termination of the thread. For a send instruction, if this field is set, EU will terminate the thread and also set the EOT bit in the message sideband. This field only applies to the send instruction. It is not present for other instructions.</td></tr> <tr> <th>Value</th><th>Name</th></tr> <tr> <td>0</td><td>Thread is not terminated</td></tr> <tr> <td>1</td><td>EOT</td></tr> </tbody> </table>	Description		This field controls the termination of the thread. For a send instruction, if this field is set, EU will terminate the thread and also set the EOT bit in the message sideband. This field only applies to the send instruction. It is not present for other instructions.		Value	Name	0	Thread is not terminated	1	EOT
Description												
This field controls the termination of the thread. For a send instruction, if this field is set, EU will terminate the thread and also set the EOT bit in the message sideband. This field only applies to the send instruction. It is not present for other instructions.												
Value	Name											
0	Thread is not terminated											
1	EOT											

## EU\_INSTRUCTION\_OPERAND\_SRC\_REG\_ALIGN1

EU_INSTRUCTION_OPERAND_SRC_REG_ALIGN1		
DWord	Bit	Description
0	24:21	<b>Source Vertical Stride</b> Format: <span style="border: 1px solid black; padding: 2px;">VertStride</span>
	20:18	<b>Source Width</b> Format: <span style="border: 1px solid black; padding: 2px;">Width</span>
	17:16	<b>Source Horizontal Stride</b> Format: <span style="border: 1px solid black; padding: 2px;">HorzStride</span>
	15	<b>Source Addressing Mode</b> Format: <span style="border: 1px solid black; padding: 2px;">AddrMode</span>
	14:13	<b>Reserved</b> Exists If: (Property[Source Modifier]=='false') Format: MBZ
	14:13	<b>Source Modifier</b> Exists If: (Property[Source Modifier]=='true') Format: <span style="border: 1px solid black; padding: 2px;">SrcMod</span>
	12:9	<b>Source Address Subregister Number</b> Project: BDW Exists If: ([Source Addressing Mode]=='Indirect') Format: <span style="border: 1px solid black; padding: 2px;">AddrSubRegNum</span>
	12:5	<b>Source Register Number</b> Exists If: ([Source Addressing Mode]=='Direct') Format: <span style="border: 1px solid black; padding: 2px;">SrcRegNum</span>
	8:0	<b>Source Address Immediate [8:0]</b> Project: BDW Exists If: ([Source Addressing Mode]=='Indirect') Format: S9[8:0]
	4:0	<b>Source Subregister Number</b> Exists If: ([Source Addressing Mode]=='Direct') Format: <span style="border: 1px solid black; padding: 2px;">SrcSubRegNum</span>

## EU\_INSTRUCTION\_OPERAND\_SRC\_REG\_ALIGN16

EU_INSTRUCTION_OPERAND_SRC_REG_ALIGN16		
DWord	Bit	Description
0	24:21	<b>Source Vertical Stride</b> Format: <b>VertStride</b>
	20	<b>Reserved</b> Format: MBZ
	19:16	<b>Source Channel Select[7:4]</b> Format: <b>ChanSel[4][7:4]</b>
	15	<b>Source Addressing Mode</b> Format: <b>AddrMode</b>
	14:13	<b>Reserved</b> Exists If: (Property[Source Modifier]=='false') Format: MBZ
	14:13	<b>Source Modifier</b> Exists If: (Property[Source Modifier]=='true') Format: <b>SrcMod</b>
	12:9	<b>Source Address Subregister Number</b> Project: BDW Exists If: ([Source Addressing Mode]=='Indirect') Format: <b>AddrSubRegNum</b>
	12:5	<b>Source Register Number</b> Exists If: ([Source Addressing Mode]=='Direct') Format: <b>SrcRegNum</b>
	8:4	<b>Source Address Immediate[8:4]</b> Project: BDW Exists If: ([Source Addressing Mode]=='Indirect') Format: S9[8:4]
	4	<b>Source Subregister Number[4:4]</b> Exists If: ([Source Addressing Mode]=='Direct') Format: <b>SrcSubRegNum[4:4]</b>

**EU\_INSTRUCTION\_OPERAND\_SRC\_REG\_ALIGN16**

	3:0	<b>Source Channel Select[3:0]</b>
		Format: <b>ChanSel[4][3:0]</b>

## EU\_INSTRUCTION\_OPERAND\_SRC\_REG\_THREE\_SRC

EU_INSTRUCTION_OPERAND_SRC_REG_THREE_SRC		
DWord	Bit	Description
0	19:12	<b>Source Register Number</b> Format: <span style="border: 1px solid black; padding: 2px;">SrcRegNum</span>
	11:9	<b>Source Subregister Number [4:2]</b> Format: <span style="border: 1px solid black; padding: 2px;">SrcSubRegNum[4:2]</span>
	8:1	<b>Source Swizzle</b> Format: <span style="border: 1px solid black; padding: 2px;">ChanSel[4]</span>
	0	<b>Source Replicate Control</b> Format: <span style="border: 1px solid black; padding: 2px;">RepCtrl</span>

## EU\_INSTRUCTION\_SEND

EU_INSTRUCTION_SEND									
DWord	Bit	Description							
0..3	127:96	<b>Message</b> <table border="1"> <tr> <td>Format:</td> <td><b>EU_INSTRUCTION_OPERAND_SEND_MSG</b></td> </tr> </table>	Format:	<b>EU_INSTRUCTION_OPERAND_SEND_MSG</b>					
Format:	<b>EU_INSTRUCTION_OPERAND_SEND_MSG</b>								
95	<b>Reserved</b> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ						
Format:	MBZ								
94:91	<b>Src1.SrcType</b> <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Format:</td> <td><b>SrcType</b></td> </tr> <tr> <th>Value</th><th>Name</th></tr> <tr> <td>11b</td> <td>Reserved</td> </tr> </table>	Project:	BDW	Format:	<b>SrcType</b>	Value	Name	11b	Reserved
Project:	BDW								
Format:	<b>SrcType</b>								
Value	Name								
11b	Reserved								
90:89	<b>Src1.RegFile</b> <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Format:</td> <td><b>RegFile</b></td> </tr> </table>	Project:	BDW	Format:	<b>RegFile</b>				
Project:	BDW								
Format:	<b>RegFile</b>								
88:64	<b>Source 0</b> <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Exists If:</td> <td>(Structure[EU_INSTRUCTION_CONTROLS_A][AccessMode]=='Align16')</td> </tr> <tr> <td>Format:</td> <td><b>EU_INSTRUCTION_OPERAND_SRC_REG_ALIGN16</b></td> </tr> </table>	Project:	BDW	Exists If:	(Structure[EU_INSTRUCTION_CONTROLS_A][AccessMode]=='Align16')	Format:	<b>EU_INSTRUCTION_OPERAND_SRC_REG_ALIGN16</b>		
Project:	BDW								
Exists If:	(Structure[EU_INSTRUCTION_CONTROLS_A][AccessMode]=='Align16')								
Format:	<b>EU_INSTRUCTION_OPERAND_SRC_REG_ALIGN16</b>								
88:64	<b>Source 0</b> <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Exists If:</td> <td>(Structure[EU_INSTRUCTION_CONTROLS_A][AccessMode]=='Align1')</td> </tr> <tr> <td>Format:</td> <td><b>EU_INSTRUCTION_OPERAND_SRC_REG_ALIGN1</b></td> </tr> </table>	Project:	BDW	Exists If:	(Structure[EU_INSTRUCTION_CONTROLS_A][AccessMode]=='Align1')	Format:	<b>EU_INSTRUCTION_OPERAND_SRC_REG_ALIGN1</b>		
Project:	BDW								
Exists If:	(Structure[EU_INSTRUCTION_CONTROLS_A][AccessMode]=='Align1')								
Format:	<b>EU_INSTRUCTION_OPERAND_SRC_REG_ALIGN1</b>								
63:32	<b>Operand Control</b> <table border="1"> <tr> <td>Format:</td> <td><b>EU_INSTRUCTION_OPERAND_CONTROLS</b></td> </tr> </table>	Format:	<b>EU_INSTRUCTION_OPERAND_CONTROLS</b>						
Format:	<b>EU_INSTRUCTION_OPERAND_CONTROLS</b>								
31:28	<b>Controls B</b> <table border="1"> <tr> <td>Format:</td> <td><b>EU_INSTRUCTION_CONTROLS_B</b></td> </tr> </table>	Format:	<b>EU_INSTRUCTION_CONTROLS_B</b>						
Format:	<b>EU_INSTRUCTION_CONTROLS_B</b>								
27:24	<b>Shared Function ID (SFID)</b> <table border="1"> <tr> <td>Format:</td> <td><b>SFID</b></td> </tr> </table>	Format:	<b>SFID</b>						
Format:	<b>SFID</b>								
23:8	<b>Controls A</b> <table border="1"> <tr> <td>Format:</td> <td><b>EU_INSTRUCTION_CONTROLS_A</b></td> </tr> </table>	Format:	<b>EU_INSTRUCTION_CONTROLS_A</b>						
Format:	<b>EU_INSTRUCTION_CONTROLS_A</b>								

## EU\_INSTRUCTION\_SEND

	7	<b>Reserved</b>	Format:	MBZ
	6:0	<b>Opcode</b>	Format:	EU_OPCODE

## EU\_INSTRUCTION\_SOURCES\_IMM32

EU_INSTRUCTION_SOURCES_IMM32			
Project: BDW Source: Eulsa Size (in bits): 64 Default Value: 0x00000000, 0x00000000			
Single source, immediate			
DWord	Bit	Description	
0..1	63:32	<b>Source 0 Immediate</b>	
	31:25	<b>Reserved</b>	
		Format:	MBZ
	24:0	<b>Source 0</b> Exists   (Structure[EU_INSTRUCTION_CONTROLS_A][AccessMode]=='Align16') AND If:   (Structure[EU_INSTRUCTION_OPERAND_CONTROLS][Src0.RegFile]!='IMM') Format: <b>EU_INSTRUCTION_OPERAND_SRC_REG_ALIGN16</b>	
	24:0	<b>Source 0</b> Exists   (Structure[EU_INSTRUCTION_CONTROLS_A][AccessMode]=='Align1') AND If:   (Structure[EU_INSTRUCTION_OPERAND_CONTROLS][Src0.RegFile]!='IMM') Format: <b>EU_INSTRUCTION_OPERAND_SRC_REG_ALIGN1</b>	

## EU\_INSTRUCTION\_SOURCES\_REG

EU_INSTRUCTION_SOURCES_REG			
Project: BDW Source: Eulsa Size (in bits): 64 Default Value: 0x00000000, 0x00000000			
Single source, register			
DWord	Bit	Description	
0..1	63:25	<b>Reserved</b>	
		Format:	MBZ
	24:0	<b>Source 0</b>	
	24:0	Exists	(Structure[EU_INSTRUCTION_CONTROLS_A][AccessMode]=='Align16') AND (Structure[EU_INSTRUCTION_OPERAND_CONTROLS][Src0.RegFile]!='IMM')
		If:	(Structure[EU_INSTRUCTION_OPERAND_CONTROLS][Src0.RegFile]!='IMM')
		Format:	<b>EU_INSTRUCTION_OPERAND_SRC_REG_ALIGN16</b>
	24:0	<b>Source 0</b>	
		Exists	(Structure[EU_INSTRUCTION_CONTROLS_A][AccessMode]=='Align1') AND (Structure[EU_INSTRUCTION_OPERAND_CONTROLS][Src0.RegFile]!='IMM')
		If:	(Structure[EU_INSTRUCTION_OPERAND_CONTROLS][Src0.RegFile]!='IMM')
		Format:	<b>EU_INSTRUCTION_OPERAND_SRC_REG_ALIGN1</b>

## EU\_INSTRUCTION\_SOURCES\_REG\_IMM

EU_INSTRUCTION_SOURCES_REG_IMM								
DWord	Bit	Description						
0..1	63:32	<b>Source 1 Immediate</b>						
	31	<b>Reserved</b>						
		Exists If: ([Source 0][Source Addressing Mode]=='Direct') Format: MBZ						
	31	<b>Source 0 Address Immediate [9] (Sign Bit)</b>						
		Exists If: ([Source 0][Source Addressing Mode]=='Indirect') Format: S9[9]						
	30:27	<b>Src1.SrcType</b>						
		Format: <b>SrcImmType</b>						
	26:25	<b>Src1.RegFile</b>						
		Format: <b>RegFile</b>						
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>Reserved</td> </tr> <tr> <td>01b</td> <td>Reserved</td> </tr> </tbody> </table>	Value	Name	00b	Reserved	01b	Reserved
Value	Name							
00b	Reserved							
01b	Reserved							
	24:0	<b>Source 0</b>						
		Exists If: (Structure[EU_INSTRUCTION_CONTROLS_A][AccessMode]=='Align16') AND (Structure[EU_INSTRUCTION_OPERAND_CONTROLS][Src0.RegFile]!='IMM') Format: <b>EU_INSTRUCTION_OPERAND_SRC_REG_ALIGN16</b>						
	24:0	<b>Source 0</b>						
		Exists If: (Structure[EU_INSTRUCTION_CONTROLS_A][AccessMode]=='Align1') AND (Structure[EU_INSTRUCTION_OPERAND_CONTROLS][Src0.RegFile]!='IMM') Format: <b>EU_INSTRUCTION_OPERAND_SRC_REG_ALIGN1</b>						

## EU\_INSTRUCTION\_SOURCES\_REG\_REG

EU_INSTRUCTION_SOURCES_REG_REG			
Project: BDW Source: Eulsa Size (in bits): 64 Default Value: 0x00000000, 0x00000000			
Dual source, both registers			
DWord	Bit	Description	
0..1	63:58	<b>Reserved</b>	Format: MBZ
	57	<b>Reserved</b>	Exists If: ([Source 1][Source Addressing Mode]=='Direct') Format: MBZ
	57	<b>Source 1 Address Immediate [9] (Sign Bit)</b>	Exists If: ([Source 1][Source Addressing Mode]=='Indirect') Format: S9[9]
	56:32	<b>Source 1</b>	Exists If: (Structure[EU_INSTRUCTION_CONTROLS_A][AccessMode]=='Align16') Format: EU_INSTRUCTION_OPERAND_SRC_REG_ALIGN16
	56:32	<b>Source 1</b>	Exists If: (Structure[EU_INSTRUCTION_CONTROLS_A][AccessMode]=='Align1') Format: EU_INSTRUCTION_OPERAND_SRC_REG_ALIGN1
	31	<b>Reserved</b>	Exists If: ([Source 0][Source Addressing Mode]=='Direct') Format: MBZ
	31	<b>Source 0 Address Immediate [9] (Sign Bit)</b>	Exists If: ([Source 0][Source Addressing Mode]=='Indirect') Format: S9[9]

## EU\_INSTRUCTION\_SOURCES\_REG\_REG

	<b>Src1.SrcType</b>						
	<table border="1"> <tr> <td>Format:</td><td><b>SrcType</b></td></tr> </table>	Format:	<b>SrcType</b>				
Format:	<b>SrcType</b>						
<p>This field specifies the numeric data type of the source operand src1. The bits of a source operand are interpreted as the identified numeric data type, rather than coerced into a type implied by the operator. Depending on RegFile field of the source operand, there are two different encoding for this field. If a source is a register operand, this field follows the Source Register Type Encoding. If a source is an immediate operand, this field follows the Source Immediate Type Encoding.</p> <table border="1"> <thead> <tr> <th style="text-align: center;"><b>Value</b></th><th style="text-align: center;"><b>Name</b></th></tr> </thead> <tbody> <tr> <td style="text-align: center;">11b</td><td>Reserved</td></tr> </tbody> </table>		<b>Value</b>	<b>Name</b>	11b	Reserved		
<b>Value</b>	<b>Name</b>						
11b	Reserved						
<b>Programming Notes</b>							
<p>Both source operands, src0 and src1, support immediate types, but only one immediate is allowed for a given instruction and it must be the last operand.</p> <p>Halfbyte integer vector (v) type can only be used in instructions in packed-word execution mode. Therefore, in a two-source instruction where src1 is of type :v, src0 must be of type :b, :ub, :w, or :uw.</p>							
26:25	<b>Src1.RegFile</b>						
	<table border="1"> <tr> <td>Format:</td><td><b>RegFile</b></td></tr> </table>	Format:	<b>RegFile</b>				
Format:	<b>RegFile</b>						
24:0	<b>Source 0</b>						
	<table border="1"> <tr> <td>Exists</td><td>(Structure[EU_INSTRUCTION_CONTROLS_A][AccessMode]=='Align16') AND</td></tr> <tr> <td>If:</td><td>(Structure[EU_INSTRUCTION_OPERAND_CONTROLS][Src0.RegFile]!='IMM')</td></tr> <tr> <td>Format:</td><td><b>EU_INSTRUCTION_OPERAND_SRC_REG_ALIGN16</b></td></tr> </table>	Exists	(Structure[EU_INSTRUCTION_CONTROLS_A][AccessMode]=='Align16') AND	If:	(Structure[EU_INSTRUCTION_OPERAND_CONTROLS][Src0.RegFile]!='IMM')	Format:	<b>EU_INSTRUCTION_OPERAND_SRC_REG_ALIGN16</b>
Exists	(Structure[EU_INSTRUCTION_CONTROLS_A][AccessMode]=='Align16') AND						
If:	(Structure[EU_INSTRUCTION_OPERAND_CONTROLS][Src0.RegFile]!='IMM')						
Format:	<b>EU_INSTRUCTION_OPERAND_SRC_REG_ALIGN16</b>						
24:0	<b>Source 0</b>						
	<table border="1"> <tr> <td>Exists</td><td>(Structure[EU_INSTRUCTION_CONTROLS_A][AccessMode]=='Align1') AND</td></tr> <tr> <td>If:</td><td>(Structure[EU_INSTRUCTION_OPERAND_CONTROLS][Src0.RegFile]!='IMM')</td></tr> <tr> <td>Format:</td><td><b>EU_INSTRUCTION_OPERAND_SRC_REG_ALIGN1</b></td></tr> </table>	Exists	(Structure[EU_INSTRUCTION_CONTROLS_A][AccessMode]=='Align1') AND	If:	(Structure[EU_INSTRUCTION_OPERAND_CONTROLS][Src0.RegFile]!='IMM')	Format:	<b>EU_INSTRUCTION_OPERAND_SRC_REG_ALIGN1</b>
Exists	(Structure[EU_INSTRUCTION_CONTROLS_A][AccessMode]=='Align1') AND						
If:	(Structure[EU_INSTRUCTION_OPERAND_CONTROLS][Src0.RegFile]!='IMM')						
Format:	<b>EU_INSTRUCTION_OPERAND_SRC_REG_ALIGN1</b>						

## ExtMsgDescpt

ExtMsgDescpt								
DWord	Bit	Description						
Extended Message Descriptor Definition for SendS (Immediate)	0	<b>Extended Function Control</b> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>U16</td></tr> </table> <p>This field is intended to control the target function unit. Refer to the section on the specific target function unit for details on the contents of this field.</p>	Project:	BDW	Format:	U16		
Project:	BDW							
Format:	U16							
<b>Reserved</b> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	BDW	Format:	MBZ				
Project:	BDW							
Format:	MBZ							
11	<b>Reserved</b> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	BDW	Format:	MBZ			
Project:	BDW							
Format:	MBZ							
<b>Reserved</b> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	BDW	Format:	MBZ				
Project:	BDW							
Format:	MBZ							
10:6	<b>Reserved</b> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	BDW	Format:	MBZ			
Project:	BDW							
Format:	MBZ							
<b>EOT</b> <table border="1"> <tr> <td>Format:</td><td>U1</td></tr> </table> <p>This field, if set, indicates that this is the final message of the thread and the thread's resources can be reclaimed.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0</td><td>No Termination</td></tr> <tr> <td>1</td><td>EOT</td></tr> </tbody> </table>	Format:	U1	Value	Name	0	No Termination	1	EOT
Format:	U1							
Value	Name							
0	No Termination							
1	EOT							
4	<b>Reserved</b> <table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ					
Format:	MBZ							

## ExtMsgDescpt

	3:0	<b>Target Function ID</b>
		Format: U4
<p>If set, indicates that the message includes a header. Depending on the target shared function, this field may be restricted to either enabled or disabled. Refer to the specific shared function section for details.</p>		
Value	Name	
0000b	Null	
0001b	Reserved	
0010b	SamplingEngine	
0011b	MessageGateway	
0100b	DataPortSamplerCache	
0101b	DataPortRenderCache	
0110b	URB	
0111b	ThreadSpawner	
1000b	VideoMotionEstimation	
1001b	ConstantCache	
1010b-1111b	Reserved	

## ExtMsgDescptImmediate

ExtMsgDescptImmediate													
DWord	Bit	Description											
Extended Message Descriptor Definition for SendS (Immediate)	0	<table border="1"> <tr> <td><b>Extended Function Control</b></td> <td></td> </tr> <tr> <td>Format:</td> <td>U16</td> </tr> <tr> <td colspan="2">This field is intended to control the target function unit. Refer to the section on the specific target function unit for details on the contents of this field.</td></tr> </table>	<b>Extended Function Control</b>		Format:	U16	This field is intended to control the target function unit. Refer to the section on the specific target function unit for details on the contents of this field.						
<b>Extended Function Control</b>													
Format:	U16												
This field is intended to control the target function unit. Refer to the section on the specific target function unit for details on the contents of this field.													
15:12	<table border="1"> <tr> <td><b>Reserved</b></td> <td></td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	<b>Reserved</b>		Format:	MBZ								
<b>Reserved</b>													
Format:	MBZ												
11	<table border="1"> <tr> <td><b>Reserved</b></td> <td></td> </tr> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	<b>Reserved</b>		Project:	BDW	Format:	MBZ						
<b>Reserved</b>													
Project:	BDW												
Format:	MBZ												
10	<table border="1"> <tr> <td><b>Reserved</b></td> <td></td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	<b>Reserved</b>		Format:	MBZ								
<b>Reserved</b>													
Format:	MBZ												
9:6	<table border="1"> <tr> <td><b>Reserved</b></td> <td></td> </tr> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	<b>Reserved</b>		Project:	BDW	Format:	MBZ						
<b>Reserved</b>													
Project:	BDW												
Format:	MBZ												
5	<table border="1"> <tr> <td><b>EOT</b></td> <td></td> </tr> <tr> <td>Format:</td> <td>U1</td> </tr> <tr> <td colspan="2">This field, if set, indicates that this is the final message of the thread and the thread's resources can be reclaimed.</td></tr> <tr> <th>Value</th><th>Name</th></tr> <tr> <td>0</td><td>No Termination</td></tr> <tr> <td>1</td><td>EOT</td></tr> </table>	<b>EOT</b>		Format:	U1	This field, if set, indicates that this is the final message of the thread and the thread's resources can be reclaimed.		Value	Name	0	No Termination	1	EOT
<b>EOT</b>													
Format:	U1												
This field, if set, indicates that this is the final message of the thread and the thread's resources can be reclaimed.													
Value	Name												
0	No Termination												
1	EOT												
4	<table border="1"> <tr> <td><b>Reserved</b></td> <td></td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	<b>Reserved</b>		Format:	MBZ								
<b>Reserved</b>													
Format:	MBZ												

## ExtMsgDescptImmediate

	3:0	<b>Target Function ID</b>
		Format: U4
<p>If set, indicates that the message includes a header. Depending on the target shared function, this field may be restricted to either enabled or disabled. Refer to the specific shared function section for details.</p>		
Value	Name	
0000b	Null	
0001b	Reserved	
0010b	SamplingEngine	
0011b	MessageGateway	
0100b	DataPortSamplerCache	
0101b	DataPortRenderCache	
0110b	URB	
0111b	ThreadSpawner	
1000b	VideoMotionEstimation	
1001b	ConstantCache	
1010b-1111b	Reserved	

## FFTID Message Header Control

MHC_FFTID - FFTID Message Header Control								
DWord	Bit	Description						
0	31:8	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Ignore</td> </tr> <tr> <td colspan="2">Ignored</td></tr> </table>	Project:	All	Format:	Ignore	Ignored	
Project:	All							
Format:	Ignore							
Ignored								
	7:0	<p><b>FFTID</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U8</td> </tr> </table> <p>Fixed function thread ID, used to free up resources by the thread on thread completion.</p>	Project:	All	Format:	U8		
Project:	All							
Format:	U8							

## Filter\_Coefficient

Filter_Coefficient		
DWord	Bit	Description
0	7:0	<b>Filter Coefficient</b> Format: S1.6 2's Complement Range : [-1 63/64, +1 63/64]

## Filter\_Coefficients

Filter_Coefficients		
DWord	Bit	Description
0	63:56	<b>Filter Coefficient Offset 7</b>
		Format: <input type="text"/> Filter_Coefficient
	55:48	<b>Filter Coefficient Offset 6</b>
		Format: <input type="text"/> Filter_Coefficient
	47:40	<b>Filter Coefficient Offset 5</b>
		Format: <input type="text"/> Filter_Coefficient
	39:32	<b>Filter Coefficient Offset 4</b>
		Format: <input type="text"/> Filter_Coefficient
31:24	31:24	<b>Filter Coefficient Offset 3</b>
		Format: <input type="text"/> Filter_Coefficient
	23:16	<b>Filter Coefficient Offset 2</b>
		Format: <input type="text"/> Filter_Coefficient
	15:8	<b>Filter Coefficient Offset 1</b>
		Format: <input type="text"/> Filter_Coefficient
	7:0	<b>Filter Coefficient Offset 0</b>
		Format: <input type="text"/> Filter_Coefficient

## FrameDeltaQp

FrameDeltaQp		
DWord	Bit	Description
0..1	63:56	<b>FrameDeltaQp[7]</b> Format: S7
	55:48	<b>FrameDeltaQp[6]</b> Format: S7
	47:40	<b>FrameDeltaQp[5]</b> Format: S7
	39:32	<b>FrameDeltaQp[4]</b> Format: S7
	31:24	<b>FrameDeltaQp[3]</b> Format: S7
	23:16	<b>FrameDeltaQp[2]</b> Format: S7
	15:8	<b>FrameDeltaQp[1]</b> Format: S7
	7:0	<b>FrameDeltaQp[0]</b> Format: S7

## FrameDeltaQpRange

FrameDeltaQpRange		
DWord	Bit	Description
0..1	63:56	<b>FrameDeltaQpRange[7]</b> Format: U8
	55:48	<b>FrameDeltaQpRange[6]</b> Format: U8
	47:40	<b>FrameDeltaQpRange[5]</b> Format: U8
	39:32	<b>FrameDeltaQpRange[4]</b> Format: U8
	31:24	<b>FrameDeltaQpRange[3]</b> Format: U8
	23:16	<b>FrameDeltaQpRange[2]</b> Format: U8
	15:8	<b>FrameDeltaQpRange[1]</b> Format: U8
	7:0	<b>FrameDeltaQpRange[0]</b> Format: U8

## FunctionControl

# FunctionControl

Project: BDW  
Source: Eulsa  
Size (in bits): 6  
Default Value: 0x00000000

DWord	Bit	Description
0	5:4	<b>Reserved</b>
	3:0	<b>Target Function ID</b>
Value	Name	
0000b	Reserved	
0001b	INV (Reciprocal)	
0010b	LOG	
0011b	EXP	
0100b	SQRT	
0101b	RSQ	
0110b	SIN	
0111b	COS	
1000b	Reserved	
1001b	FDIV	
1010b	POW	
1011b	INT DIV Quotient and remainder	
1100b	INT DIV Quotient only	
1101b	INT DIV Remainder only	
1110b	INVM	
1111b	RSQRTM	

## GATHER\_CONSTANT\_ENTRY

GATHER_CONSTANT_ENTRY					
DWord	Bit	Description			
0	15:8	<p><b>Constant Buffer Offset</b></p> <table border="1"> <tr> <td>Format:</td> <td>Offset[7:0]ConstantBuffer</td> </tr> </table> <p>This field specifies the Offset in 128-bit units of the 128b entry fetched from the constant buffer for this entry (including when <b>On-Die Table Read Enable</b> is set).</p>	Format:	Offset[7:0]ConstantBuffer	
Format:	Offset[7:0]ConstantBuffer				
7:4	<p><b>Channel Mask</b></p> <table border="1"> <tr> <td>Mask:</td> <td>Mask[3:0]</td> </tr> <tr> <td>Format:</td> <td>ConstantBuffer</td> </tr> </table> <p>Each bit of this field correspond to the 4 channels of each entry fetched from memory. When the bit is a 1, the corresponding 32-bit value is loaded in FF's push constant buffer. When the bit is a 0, the corresponding 32-bit value is not loaded. If this field is zero it means the entry is not used.</p>	Mask:	Mask[3:0]	Format:	ConstantBuffer
Mask:	Mask[3:0]				
Format:	ConstantBuffer				
3:0	<p><b>Binding Table Index Offset</b></p> <table border="1"> <tr> <td>Format:</td> <td>Constant Buffer Index offset [3:0]Surface State for ConstantBuffer</td> </tr> </table> <p>This field specifies the Binding Table index offset from the <b>Constant Buffer Binding Table Block</b> starting point in the Binding Table. This value is added to the <b>Constant Buffer Binding Table Block</b> will result in the Binding Table Index pointing to the surface state containing the constant buffer to be referenced. If <b>VS Constant Buffer Dx9 Enable</b> is set then a value of '1' specifies that the fetch to the constant buffer should be offset by 4KB in order to address the upper 4K of the constant buffer. Any value greater than '1' is invalid when <b>VS Constant Buffer Dx9 Enable</b> is set.</p>	Format:	Constant Buffer Index offset [3:0]Surface State for ConstantBuffer		
Format:	Constant Buffer Index offset [3:0]Surface State for ConstantBuffer				

## GTC CPU Interrupt Bit Definition

GTC CPU Interrupt Bit Definition		
DWord	Bit	Description
0	31:7	<b>Reserved</b>
	6:3	<b>Unused_Int_6_3</b> These interrupts are currently unused.
	2	<b>GTC_Lock_Timeout</b> CPU GTC has lost lock with PCH GTC. The difference between the local and remote GTC has exceeded the programmed threshold.
	1	<b>GTC_Update_Message_Rx_Error</b> An error occurred during reception of the PCH to CPU GTC update message.
	0	<b>GTC_Update_Received</b> A GTC update message has been received from the PCH GTC controller and the register updates are ready to read.

## GT Interrupt Bit Definition

GT Interrupt Bit Definition		
DWord	Bit	Description
0	31:30	<b>Unused_Int_31_30</b> These interrupts are currently unused.
	29	<b>Blitter_Page_Directory_Faults</b> This is a write of logic1 via GT interrupt message bit 29
	28:27	<b>Unused_Int_28_27</b> These interrupts are currently unused.
	26	<b>Blitter_MI_FLUSH_DW_Notify</b> This is a write of logic1 via GT interrupt message bit 26
	25	<b>Blitter_Command_Parser_Master_Error</b> This is a write of logic1 via GT interrupt message bit 25
	24	<b>Blitter_MMIO_Sync_Flush_Status</b> This is a write of logic1 via GT interrupt message bit 24
	23	<b>Unused_Int_23</b> These interrupts are currently unused.
	22	<b>Blitter_Command_Parser_User_Interrupt</b> This is a write of logic1 via GT interrupt message bit 22
	21:20	<b>Unused_Int_21_20</b> These interrupts are currently unused.
	19	<b>VideoCodec_Page_Directory_Faults</b> This is a write of logic1 via GT interrupt message bit 19
	18	<b>VideoCodec_Timeout_Counter_Expired</b> This is a write of logic1 via GT interrupt message bit 18
	17	<b>Reserved</b>
	16	<b>VideoCodec_MI_FLUSH_DW_Notify</b> This is a write of logic1 via GT interrupt message bit 16
	15	<b>VideoCodec_Command_Parser_Master_Error</b> This is a write of logic1 via GT interrupt message bit 15
	14	<b>VideoCodec_MMIO_Sync_Flush_Status</b> This is a write of logic1 via GT interrupt message bit 14
	13	<b>Reserved</b>

## GT Interrupt Bit Definition

	12	<b>VideoCodec_Command_Parser_User_Interrupt</b> This is a write of logic1 via GT interrupt message bit 12
	11	<b>L3_Parity_Error_Interrupt</b> This is a write of logic1 via GT interrupt message bit 11
	10	<b>L3_Counter_Save</b> This is a write of logic1 via GT interrupt message bit 10
	9	<b>Render_Perf_Monitor_Buffer_Half_Full_Interrupt</b> This is a write of logic1 via GT interrupt message bit 9
	8	<b>Preemption_Complete_Interrupt</b> This is a write of logic1 via GT interrupt message bit 8
	7	<b>Render_Page_Directoy_Faults</b> This is a write of logic1 via GT interrupt message bit 7
	6	<b>Render_Timeout_Counter_Expired</b> This is a write of logic1 via GT interrupt message bit 6
	5	<b>Render_L3_Parity_Error</b> This is a write of logic1 via GT interrupt message bit 5
	4	<b>Render_PIPE_CONTROL_Notify</b> This is a write of logic1 via GT interrupt message bit 4
	3	<b>Render_Command_Parser_Master_Error</b> This is a write of logic1 via GT interrupt message bit 3
	2	<b>Render_MMIO_Sync_Flush_Status</b> This is a write of logic1 via GT interrupt message bit 2
	1	<b>Reserved</b>
	0	<b>Render_Command_Parser_User_Interrupt</b> This is a write of logic1 via GT interrupt message bit 0

## Hardware-Detected Error Bit Definitions

Hardware-Detected Error Bit Definitions							
DWord	Bit	Description					
0	31:3	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ			
Format:	MBZ						
2	<p><b>Command Privilege Violation Error</b></p> <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> </table> <p>This bit is set if a command classified as privileged is parsed in a non-privileged batch buffer. The command will be converted to a NOOP and parsing will continue.</p>	Project:	BDW				
Project:	BDW						
1	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ				
Format:	MBZ						
0	<p><b>Instruction Error</b></p> <p>This bit is set when the Renderer Instruction Parser detects an error while parsing an instruction. Instruction errors include:</p> <ul style="list-style-type: none"> <li>• Client ID value (Bits 31:29 of the Header) is not supported (only MI, 2D and 3D are supported).</li> <li>• Defeatured MI Instruction Opcodes:</li> </ul> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>1</td> <td></td> <td>Instruction Error detected</td> </tr> </tbody> </table> <p><b>Programming Notes</b></p> <p>This error indications cannot be cleared except by reset (i.e., it is a fatal error).</p>	Value	Name	Description	1		Instruction Error detected
Value	Name	Description					
1		Instruction Error detected					

## Hardware Status Page Layout

DWord	Bit	Description		
0	31:0	<p><b>Interrupt Status Register Storage</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 5px;">Project:</td> <td style="padding: 5px;">All</td> </tr> </table> <p>The content of the ISR register is written to this location whenever an "unmasked" bit of the ISR (as determined by the HWSTAM register) changes state.</p>	Project:	All
Project:	All			

## Hardware Status Page Layout

<b>Hardware Status Page Layout</b>						
1..3	31:0	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="padding: 2px;">Project:</td> <td style="padding: 2px; text-align: right;">All</td> </tr> <tr> <td colspan="2" style="padding: 2px;">Must not be used.</td> </tr> </table>	Project:	All	Must not be used.	
Project:	All					
Must not be used.						
4	31:0	<p><b>Ring Head Pointer Storage</b></p> <table border="1" style="width: 100%;"> <tr> <td style="padding: 2px;">Project:</td> <td style="padding: 2px; text-align: right;">All</td> </tr> <tr> <td colspan="2" style="padding: 2px;">The contents of the Ring Buffer Head Pointer register (register DWord 1) are written to this location either as result of an MI_REPORT_HEAD instruction or as the result of an "automatic report" (see RINGBUF registers).</td> </tr> </table>	Project:	All	The contents of the Ring Buffer Head Pointer register (register DWord 1) are written to this location either as result of an MI_REPORT_HEAD instruction or as the result of an "automatic report" (see RINGBUF registers).	
Project:	All					
The contents of the Ring Buffer Head Pointer register (register DWord 1) are written to this location either as result of an MI_REPORT_HEAD instruction or as the result of an "automatic report" (see RINGBUF registers).						
5..15	31:0	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="padding: 2px;">Project:</td> <td style="padding: 2px; text-align: right;">All</td> </tr> <tr> <td colspan="2" style="padding: 2px;">Must not be used.</td> </tr> </table>	Project:	All	Must not be used.	
Project:	All					
Must not be used.						
16..27	31:0	<p><b>Context Status DWords</b></p> <table border="1" style="width: 100%;"> <tr> <td style="padding: 2px;">Project:</td> <td style="padding: 2px; text-align: right;">BDW</td> </tr> </table>	Project:	BDW		
Project:	BDW					
28..30 <b>Project:</b> BDW	31:0	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="padding: 2px;">Project:</td> <td style="padding: 2px; text-align: right;">BDW</td> </tr> <tr> <td colspan="2" style="padding: 2px;">Must not be used.</td> </tr> </table>	Project:	BDW	Must not be used.	
Project:	BDW					
Must not be used.						
31 <b>Project:</b> BDW	31:0	<p><b>Last Written Status Offset</b></p> <table border="1" style="width: 100%;"> <tr> <td style="padding: 2px;">Project:</td> <td style="padding: 2px; text-align: right;">BDW</td> </tr> </table>	Project:	BDW		
Project:	BDW					
32..39 <b>Project:</b> BDW	31:0	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="padding: 2px;">Project:</td> <td style="padding: 2px; text-align: right;">BDW</td> </tr> </table>	Project:	BDW		
Project:	BDW					
40..46	31:0	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="padding: 2px;">Project:</td> <td style="padding: 2px; text-align: right;">All</td> </tr> </table>	Project:	All		
Project:	All					
47	31:0	<p><b>Reserved</b></p> <table border="1" style="width: 100%;"> <tr> <td style="padding: 2px;">Project:</td> <td style="padding: 2px; text-align: right;">BDW</td> </tr> </table>	Project:	BDW		
Project:	BDW					
48..1023	31:0	<p><b>General Purpose</b></p> <table border="1" style="width: 100%;"> <tr> <td style="padding: 2px;">Project:</td> <td style="padding: 2px; text-align: right;">All</td> </tr> <tr> <td colspan="2" style="padding: 2px;">These locations can be used for general purpose via the MI_STORE_DATA_INDEX or MI_STORE_DATA_IMM instructions.</td> </tr> </table>	Project:	All	These locations can be used for general purpose via the MI_STORE_DATA_INDEX or MI_STORE_DATA_IMM instructions.	
Project:	All					
These locations can be used for general purpose via the MI_STORE_DATA_INDEX or MI_STORE_DATA_IMM instructions.						

## Header Forbidden Message Descriptor Control Field

MDC_MHF - Header Forbidden Message Descriptor Control Field															
DWord	Bit	Description													
0	0	<p><b>Message Header Present</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Enumeration</td> </tr> </table> <p>Indicates the message forbids a message header.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>No [Default]</td> <td>Message header is not present</td> </tr> <tr> <td>1h</td> <td>Reserved</td> <td>Not used</td> </tr> </tbody> </table>	Project:	All	Format:	Enumeration	Value	Name	Description	0h	No [Default]	Message header is not present	1h	Reserved	Not used
Project:	All														
Format:	Enumeration														
Value	Name	Description													
0h	No [Default]	Message header is not present													
1h	Reserved	Not used													

## Header Present Message Descriptor Control Field

<b>MDC_MHP - Header Present Message Descriptor Control Field</b>																	
Project: BDW Size (in bits): 1 Default Value: 0x00000000																	
DWord	Bit	Description															
0	0	<b>Message Header Present</b> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Enumeration</td> </tr> <tr> <td colspan="2">Specifies if the message uses the optional message header.</td></tr> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> <tr> <td>0h</td><td>No</td><td>Message header is not present</td></tr> <tr> <td>1h</td><td>Yes</td><td>Message header is present</td></tr> </table>	Project:	All	Format:	Enumeration	Specifies if the message uses the optional message header.		Value	Name	Description	0h	No	Message header is not present	1h	Yes	Message header is present
Project:	All																
Format:	Enumeration																
Specifies if the message uses the optional message header.																	
Value	Name	Description															
0h	No	Message header is not present															
1h	Yes	Message header is present															

## Header Required Message Descriptor Control Field

<b>MDC_MHR - Header Required Message Descriptor Control Field</b>															
<b>DWord</b>	<b>Bit</b>	<b>Description</b>													
0	0	<p><b>Message Header Present</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Enumeration</td> </tr> </table> <p>Indicates the message requires a message header.</p> <table border="1"> <thead> <tr> <th><b>Value</b></th> <th><b>Name</b></th> <th><b>Description</b></th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Reserved</td> <td>Not used</td> </tr> <tr> <td>1h</td> <td>Yes <b>[Default]</b></td> <td>Message header is present</td> </tr> </tbody> </table>	Project:	All	Format:	Enumeration	<b>Value</b>	<b>Name</b>	<b>Description</b>	0h	Reserved	Not used	1h	Yes <b>[Default]</b>	Message header is present
Project:	All														
Format:	Enumeration														
<b>Value</b>	<b>Name</b>	<b>Description</b>													
0h	Reserved	Not used													
1h	Yes <b>[Default]</b>	Message header is present													

## HW Generated BINDING\_TABLE\_STATE

HW Generated BINDING_TABLE_STATE			
<b>DWord</b>			
<b>Bit</b>			
0	15:0	<b>Surface State Pointer</b>	
		Format:	SurfaceStateOffset[21:6] [BDW]

## Hword 1 Block Data Payload

MDP_HW1 - Hword 1 Block Data Payload						
DWord	Bit	Description				
0.0-0.7	255:0	<p><b>Hword</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U256</td></tr> </table> <p>Specifies the Hword data</p>	Project:	All	Format:	U256
Project:	All					
Format:	U256					

## Hword 2 Block Data Payload

MDP_HW2 - Hword 2 Block Data Payload						
DWord	Bit	Description				
0.0-0.7	255:0	<p><b>Hword0</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U256</td></tr> </table> <p>Specifies the Hword data for element 0</p>	Project:	All	Format:	U256
Project:	All					
Format:	U256					
1.0-1.7	255:0	<p><b>Hword1</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U256</td></tr> </table> <p>Specifies the Hword data for element 1</p>	Project:	All	Format:	U256
Project:	All					
Format:	U256					

## Hword 4 Block Data Payload

MDP_HW4 - Hword 4 Block Data Payload						
DWord	Bit	Description				
0.0-0.7	255:0	<p><b>Hword0</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U256</td></tr> </table> <p>Specifies the Hword data for element 0</p>	Project:	All	Format:	U256
Project:	All					
Format:	U256					
1.0-1.7	255:0	<p><b>Hword1</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U256</td></tr> </table> <p>Specifies the Hword data for element 1</p>	Project:	All	Format:	U256
Project:	All					
Format:	U256					
2.0-2.7	255:0	<p><b>Hword2</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U256</td></tr> </table> <p>Specifies the Hword data for element 2</p>	Project:	All	Format:	U256
Project:	All					
Format:	U256					
3.0-3.7	255:0	<p><b>Hword3</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U256</td></tr> </table> <p>Specifies the Hword data for element 3</p>	Project:	All	Format:	U256
Project:	All					
Format:	U256					

## Hword 8 Block Data Payload

MDP_HW8 - Hword 8 Block Data Payload						
DWord	Bit	Description				
0.0-0.7	255:0	<p><b>Hword0</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U256</td></tr> </table> <p>Specifies the Hword data for element 0</p>	Project:	All	Format:	U256
Project:	All					
Format:	U256					
1.0-1.7	255:0	<p><b>Hword1</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U256</td></tr> </table> <p>Specifies the Hword data for element 1</p>	Project:	All	Format:	U256
Project:	All					
Format:	U256					
2.0-2.7	255:0	<p><b>Hword2</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U256</td></tr> </table> <p>Specifies the Hword data for element 2</p>	Project:	All	Format:	U256
Project:	All					
Format:	U256					
3.0-3.7	255:0	<p><b>Hword3</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U256</td></tr> </table> <p>Specifies the Hword data for element 3</p>	Project:	All	Format:	U256
Project:	All					
Format:	U256					
4.0-4.7	255:0	<p><b>Hword4</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U256</td></tr> </table> <p>Specifies the Hword data for element 4</p>	Project:	All	Format:	U256
Project:	All					
Format:	U256					

MDP_HW8 - Hword 8 Block Data Payload						
5.0-5.7	255:0	<p><b>Hword5</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U256</td></tr> </table> <p>Specifies the Hword data for element 5</p>	Project:	All	Format:	U256
Project:	All					
Format:	U256					
6.0-6.7	255:0	<p><b>Hword6</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U256</td></tr> </table> <p>Specifies the Hword data for element 6</p>	Project:	All	Format:	U256
Project:	All					
Format:	U256					
7.0-7.7	255:0	<p><b>Hword7</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U256</td></tr> </table> <p>Specifies the Hword data for element 7</p>	Project:	All	Format:	U256
Project:	All					
Format:	U256					

## Hword Channel Mode Message Header Control

<b>MHC_A64_CMODE - Hword Channel Mode Message Header Control</b>						
<b>DWord</b>	<b>Bit</b>	<b>Description</b>				
0	31	<b>Reserved</b> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td><b>MDC_CMODE</b></td> </tr> </table> <p>Specifies whether the read or write operation occurs on all 4 Dwords if any of those channel enables are set, or else only on the dwords whose corresponding channel enable is set.</p>	Project:	All	Format:	<b>MDC_CMODE</b>
Project:	All					
Format:	<b>MDC_CMODE</b>					
<b>Reserved</b> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Ignore</td> </tr> </table> <p>Ignored</p>	Project:	All	Format:	Ignore		
Project:	All					
Format:	Ignore					

## Hword Register Blocks Message Descriptor Control Field

<b>MDC_DB_HW - Hword Register Blocks Message Descriptor Control Field</b>																					
Project:	BDW																				
Size (in bits):	2																				
Default Value:	0x00000000																				
DWord	Bit	Description																			
0	1:0	<p><b>Register Blocks</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Enumeration</td> </tr> </table> <p>Specifies the number of Hword blocks to be read or written</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00h</td> <td>HW1</td> <td>1 Hword register</td> </tr> <tr> <td>01h</td> <td>HW2</td> <td>2 Hword registers</td> </tr> <tr> <td>02h</td> <td>HW4</td> <td>4 Hword registers</td> </tr> <tr> <td>03h</td> <td>HW8</td> <td>8 Hword registers</td> </tr> </tbody> </table>	Project:	All	Format:	Enumeration	Value	Name	Description	00h	HW1	1 Hword register	01h	HW2	2 Hword registers	02h	HW4	4 Hword registers	03h	HW8	8 Hword registers
Project:	All																				
Format:	Enumeration																				
Value	Name	Description																			
00h	HW1	1 Hword register																			
01h	HW2	2 Hword registers																			
02h	HW4	4 Hword registers																			
03h	HW8	8 Hword registers																			

## Ignored Message Header

<b>MH_IGNORE - Ignored Message Header</b>								
Project: BDW Source: DataPort 0 Size (in bits): 256 Default Value: 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000								
Some messages require a message header or have an optional message header, but do not use any information in the header.								
DWord	Bit	Description						
0-7	255:0	<b>Reserved</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>Ignore</td></tr> <tr> <td colspan="2">Ignored</td></tr> </table>	Project:	All	Format:	Ignore	Ignored	
Project:	All							
Format:	Ignore							
Ignored								

## Inline Data Description for MFD\_AVC\_BSD\_Object

Inline Data Description for MFD_AVC_BSD_Object																	
DWord	Bit	Description															
0	31	<p><b>Concealment Method</b></p> <p>This field specifies the method used for concealment when error is detected. If set, a copy from collocated macroblock location is performed from the concealment reference indicated by the ConCeal_Pic_Id field. If it is not set, a copy from the current picture is performed using Intra 16x16 Prediction method.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td></td> <td>Intra 16x16 Prediction</td> </tr> <tr> <td>1</td> <td></td> <td>Inter P Copy</td> </tr> </tbody> </table>	Value	Name	Description	0		Intra 16x16 Prediction	1		Inter P Copy						
Value	Name	Description															
0		Intra 16x16 Prediction															
1		Inter P Copy															
	30	<p><b>Init Current MB Number</b></p> <p>When set, the current Slice_Start_MB_Num, Slice_MB_Start_Hor_Pos and Slice_MB_Start_Vert_Pos fields will be used to initialize the Current_MB_Number register. This effectively disables the concealment capability.</p>															
	29	<p><b>Intra PredMode (4x4/8x8 Luma) Error Control Bit</b></p> <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> </table> <p>This field controls if AVC decoder will fix Intra Prediction Mode if the decoded value is incorrect according to MB position</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td></td> <td>AVC decoder will detect and fix IntraPredMode (4x4/8x8 Luma) Errors.</td> </tr> <tr> <td>1</td> <td></td> <td>AVC decoder will NOT detect IntraPredMode (4x4/8x8 Luma) Errors. The wrong IntraPredMode value will be retaind.</td> </tr> </tbody> </table>	Project:	BDW	Value	Name	Description	0		AVC decoder will detect and fix IntraPredMode (4x4/8x8 Luma) Errors.	1		AVC decoder will NOT detect IntraPredMode (4x4/8x8 Luma) Errors. The wrong IntraPredMode value will be retaind.				
Project:	BDW																
Value	Name	Description															
0		AVC decoder will detect and fix IntraPredMode (4x4/8x8 Luma) Errors.															
1		AVC decoder will NOT detect IntraPredMode (4x4/8x8 Luma) Errors. The wrong IntraPredMode value will be retaind.															
	28:27	<p><b>MB Error Concealment B Temporal Prediction mode</b></p> <p>These two bits control how the reference L0/L1 are overridden in B temporal slice.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>[Default]</td> <td>Both Reference Indexes L0/L1 are forced to 0 during Concealment</td> </tr> <tr> <td>01b</td> <td></td> <td>Only Reference Index L1 is forced to 0; Reference Index L0 is forced to -1</td> </tr> <tr> <td>10b</td> <td></td> <td>Only Reference Index L0 is forced to 0; Reference Index L1 is forced to -1</td> </tr> <tr> <td>11b</td> <td>Reserved</td> <td>Invalid</td> </tr> </tbody> </table>	Value	Name	Description	00b	[Default]	Both Reference Indexes L0/L1 are forced to 0 during Concealment	01b		Only Reference Index L1 is forced to 0; Reference Index L0 is forced to -1	10b		Only Reference Index L0 is forced to 0; Reference Index L1 is forced to -1	11b	Reserved	Invalid
Value	Name	Description															
00b	[Default]	Both Reference Indexes L0/L1 are forced to 0 during Concealment															
01b		Only Reference Index L1 is forced to 0; Reference Index L0 is forced to -1															
10b		Only Reference Index L0 is forced to 0; Reference Index L1 is forced to -1															
11b	Reserved	Invalid															

## Inline Data Description for MFD\_AVC\_BSD\_Object

	26	<b>Reserved</b>													
		Project:	BDW												
		Format:	MBZ												
	25	<b>MB Error Concealment B Temporal Motion Vectors Override Enable Flag</b>	During MB Error Concealment on B slice with Temporal Direct Prediction, motion vectors are forced to 0 to improve image quality. This bit can be set to preserve the original weight prediction.												
			<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0</td><td>[Default]</td><td>Predicted Motion Vectors are used during MB Concealment</td></tr> <tr> <td>1</td><td></td><td>Motion Vectors are Overridden to 0 during MB Concealment</td></tr> </tbody> </table>	Value	Name	Description	0	[Default]	Predicted Motion Vectors are used during MB Concealment	1		Motion Vectors are Overridden to 0 during MB Concealment			
Value	Name	Description													
0	[Default]	Predicted Motion Vectors are used during MB Concealment													
1		Motion Vectors are Overridden to 0 during MB Concealment													
	24	<b>MB Error Concealment B Temporal Weight Prediction Disable Flag</b>	During MB Error Concealment on B slice with Temporal Direct Prediction, weight prediction is disabled to improve image quality. This bit can be set to preserve the original weight prediction.												
			<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0</td><td>[Default]</td><td>Weight Prediction is Disabled during MB Concealment</td></tr> <tr> <td>1</td><td></td><td>Weight Prediction will not be overridden during MB Concealment</td></tr> </tbody> </table>	Value	Name	Description	0	[Default]	Weight Prediction is Disabled during MB Concealment	1		Weight Prediction will not be overridden during MB Concealment			
Value	Name	Description													
0	[Default]	Weight Prediction is Disabled during MB Concealment													
1		Weight Prediction will not be overridden during MB Concealment													
	23:22	<b>Reserved</b>													
		Format:	MBZ												
	21:16	<b>Concealment Picture ID</b>	This field identifies the picture in the reference list to be used for concealment. This field is only valid if <b>Concealment Method</b> is Inter P Copy.												
			<table border="1"> <thead> <tr> <th>Bit Filed</th><th>Value</th><th>Defenition</th></tr> </thead> <tbody> <tr> <td>21</td><td>0</td><td>Frame Picture</td></tr> <tr> <td>21</td><td>1</td><td>Field picture</td></tr> <tr> <td>20:16</td><td>All</td><td>Frame Store Index[4:0]</td></tr> </tbody> </table>	Bit Filed	Value	Defenition	21	0	Frame Picture	21	1	Field picture	20:16	All	Frame Store Index[4:0]
Bit Filed	Value	Defenition													
21	0	Frame Picture													
21	1	Field picture													
20:16	All	Frame Store Index[4:0]													
	15	<b>Reserved</b>													
		Format:	MBZ												
	14	<b>BSD Premature Complete Error Handling</b>	BSD Premature Complete Error occurs in situation where the Slice decode is completed but there are still data in the bitstream.												
			<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>1</td><td></td><td>Set the interrupt to the driver (provide MMIO registers for MB address R/W)</td></tr> <tr> <td>0</td><td></td><td>Ignore the error and continue (masked the interrupt), assume the hardware automatically performs the error handling</td></tr> </tbody> </table>	Value	Name	Description	1		Set the interrupt to the driver (provide MMIO registers for MB address R/W)	0		Ignore the error and continue (masked the interrupt), assume the hardware automatically performs the error handling			
Value	Name	Description													
1		Set the interrupt to the driver (provide MMIO registers for MB address R/W)													
0		Ignore the error and continue (masked the interrupt), assume the hardware automatically performs the error handling													
	13	<b>Reserved</b>													
		Format:	MBZ												

## Inline Data Description for MFD\_AVC\_BSD\_Object

	12	<b>MPR Error (MV out of range) Handling</b> Software must follow the action for each Value as follow:															
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>1</td><td></td><td>Set the interrupt to the driver (provide MMIO registers for MB address R/W)</td></tr> <tr> <td>0</td><td></td><td>Ignore the error and continue (masked the interrupt), assume the hardware automatically performs the error handling</td></tr> </tbody> </table>	Value	Name	Description	1		Set the interrupt to the driver (provide MMIO registers for MB address R/W)	0		Ignore the error and continue (masked the interrupt), assume the hardware automatically performs the error handling						
Value	Name	Description															
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0		Ignore the error and continue (masked the interrupt), assume the hardware automatically performs the error handling															
	11	<b>Reserved</b>															
		<table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ													
Format:	MBZ																
	10	<b>Entropy Error Handling</b> Software must follow the action for each Value as follow:															
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>1</td><td></td><td>Set the interrupt to the driver (provide MMIO registers for MB address R/W).</td></tr> <tr> <td>0</td><td></td><td>Ignore the error and continue (masked the interrupt), assume the hardware automatically perform the error handling.</td></tr> </tbody> </table>	Value	Name	Description	1		Set the interrupt to the driver (provide MMIO registers for MB address R/W).	0		Ignore the error and continue (masked the interrupt), assume the hardware automatically perform the error handling.						
Value	Name	Description															
1		Set the interrupt to the driver (provide MMIO registers for MB address R/W).															
0		Ignore the error and continue (masked the interrupt), assume the hardware automatically perform the error handling.															
	9	<b>Reserved</b>															
		<table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ													
Format:	MBZ																
	8	<b>MB Header Error Handling</b> Software must follow the action for each Value as follow:															
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>1</td><td></td><td>Set the interrupt to the driver (provide MMIO registers for MB address R/W).</td></tr> <tr> <td>0</td><td></td><td>Ignore the error and continue (masked the interrupt), assume the hardware automatically perform the error concealment.</td></tr> </tbody> </table>	Value	Name	Description	1		Set the interrupt to the driver (provide MMIO registers for MB address R/W).	0		Ignore the error and continue (masked the interrupt), assume the hardware automatically perform the error concealment.						
Value	Name	Description															
1		Set the interrupt to the driver (provide MMIO registers for MB address R/W).															
0		Ignore the error and continue (masked the interrupt), assume the hardware automatically perform the error concealment.															
	7:6	<b>MB Error Concealment B Spatial Prediction mode</b> These two bits control how the reference L0/L1 are overridden in B spatial slice.															
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>00b</td><td><b>[Default]</b></td><td>Both Reference Indexes L0/L1 are forced to 0 during Concealment</td></tr> <tr> <td>01b</td><td></td><td>Only Reference Index L1 is forced to 0; Reference Index L0 is forced to -1</td></tr> <tr> <td>10b</td><td></td><td>Only Reference Index L0 is forced to 0; Reference Index L1 is forced to -1</td></tr> <tr> <td>11b</td><td>Reserved</td><td>Invalid</td></tr> </tbody> </table>	Value	Name	Description	00b	<b>[Default]</b>	Both Reference Indexes L0/L1 are forced to 0 during Concealment	01b		Only Reference Index L1 is forced to 0; Reference Index L0 is forced to -1	10b		Only Reference Index L0 is forced to 0; Reference Index L1 is forced to -1	11b	Reserved	Invalid
Value	Name	Description															
00b	<b>[Default]</b>	Both Reference Indexes L0/L1 are forced to 0 during Concealment															
01b		Only Reference Index L1 is forced to 0; Reference Index L0 is forced to -1															
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11b	Reserved	Invalid															
	5	<b>Reserved</b>															
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> </table>	Project:	BDW													
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Format:	MBZ																

## Inline Data Description for MFD\_AVC\_BSD\_Object

		<b>4 MB Error Concealment B Spatial Motion Vectors Override Disable Flag</b> During MB Error Concealment on B slice with Spatial Direct Prediction, motion vectors are forced to 0 to improve image quality. This bit can be set to use the predicted motion vectors instead. This bit does not affect normal decoded MB.									
	4	<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0</td><td>[Default]</td><td>Motion Vectors are Overridden to 0 during MB Concealment</td></tr> <tr> <td>1</td><td></td><td>Predicted Motion Vectors are used during MB Concealment</td></tr> </tbody> </table>	Value	Name	Description	0	[Default]	Motion Vectors are Overridden to 0 during MB Concealment	1		Predicted Motion Vectors are used during MB Concealment
Value	Name	Description									
0	[Default]	Motion Vectors are Overridden to 0 during MB Concealment									
1		Predicted Motion Vectors are used during MB Concealment									
	3	<b>MB Error Concealment B Spatial Weight Prediction Disable Flag</b> During MB Error Concealment on B slice with Spatial Direct Prediction, weight prediction is disabled to improve image quality. This bit can be set to preserve the original weight prediction. This bit does not affect normal decoded MB.									
	3	<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0</td><td>[Default]</td><td>Weight Prediction is Disabled during MB Concealment.</td></tr> <tr> <td>1</td><td></td><td>Weight Prediction will not be overridden during MB Concealment.</td></tr> </tbody> </table>	Value	Name	Description	0	[Default]	Weight Prediction is Disabled during MB Concealment.	1		Weight Prediction will not be overridden during MB Concealment.
Value	Name	Description									
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1		Weight Prediction will not be overridden during MB Concealment.									
	2	<b>Reserved</b>									
	2	<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	BDW	Format:	MBZ					
Project:	BDW										
Format:	MBZ										
	1	<b>MB Error Concealment P Slice Motion Vectors Override Disable Flag</b> During MB Error Concealment on P slice, motion vectors are forced to 0 to improve image quality. This bit can be set to use the predicted motion vectors instead. This bit does not affect normal decoded MB.									
	1	<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0</td><td>[Default]</td><td>Motion Vectors are Overridden to 0 during MB Concealment</td></tr> <tr> <td>1</td><td></td><td>Predicted Motion Vectors are used during MB Concealment</td></tr> </tbody> </table>	Value	Name	Description	0	[Default]	Motion Vectors are Overridden to 0 during MB Concealment	1		Predicted Motion Vectors are used during MB Concealment
Value	Name	Description									
0	[Default]	Motion Vectors are Overridden to 0 during MB Concealment									
1		Predicted Motion Vectors are used during MB Concealment									
	0	<b>MB Error Concealment P Slice Weight Prediction Disable Flag</b> During MB Error Concealment on P slice, weight prediction is disabled to improve image quality. This bit can be set to preserve the original weight prediction. This bit does not affect normal decoded MB.									
	0	<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0</td><td>[Default]</td><td>Weight Prediction is Disabled during MB Concealment.</td></tr> <tr> <td>1</td><td></td><td>Weight Prediction will not be overridden during MB Concealment.</td></tr> </tbody> </table>	Value	Name	Description	0	[Default]	Weight Prediction is Disabled during MB Concealment.	1		Weight Prediction will not be overridden during MB Concealment.
Value	Name	Description									
0	[Default]	Weight Prediction is Disabled during MB Concealment.									
1		Weight Prediction will not be overridden during MB Concealment.									
1	31:16	<b>First MB Byte Offset of Slice Data or Slice Header</b>									
1	31:16	<table border="1"> <thead> <tr> <th>Programming Notes</th><th>Project</th></tr> </thead> <tbody> <tr> <td>MFX supports only DXVA2 Long and Short Format.</td><td>BDW</td></tr> </tbody> </table>	Programming Notes	Project	MFX supports only DXVA2 Long and Short Format.	BDW					
Programming Notes	Project										
MFX supports only DXVA2 Long and Short Format.	BDW										
1	15:8	<b>Reserved</b>									
1	15:8	<table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ							
Format:	MBZ										
1	7	<b>Fix Prev Mb Skipped</b> Enables an alternative method for decoding mb_skipped, to cope with an encoder that codes a skipped MB as a direct MB with no coefficient.									

## Inline Data Description for MFD\_AVC\_BSD\_Object

	6:5	<b>Reserved</b>									
		Format: <span style="float: right;">MBZ</span>									
<b>Programming Notes</b>											
Please note that the field MUST be set to '0' at this time.											
	4	<b>Emulation Prevention Byte Present</b>									
		<table border="1" style="width: 100%;"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td></td> <td>H/W needs to perform Emulation Byte Removal</td> </tr> <tr> <td>1</td> <td></td> <td>H/W does not need to perform Emulation Byte Removal</td> </tr> </tbody> </table>	Value	Name	Description	0		H/W needs to perform Emulation Byte Removal	1		H/W does not need to perform Emulation Byte Removal
Value	Name	Description									
0		H/W needs to perform Emulation Byte Removal									
1		H/W does not need to perform Emulation Byte Removal									
	3	<b>LastSlice Flag</b> It is needed for both error concealment at the end of a picture (so, no more phantom slice). It is also needed to know to set the last MB in a picture correctly.									
		<table border="1" style="width: 100%;"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>1</td> <td></td> <td>If the current Slice to be decoded is the very last slice of the current picture.</td> </tr> <tr> <td>0</td> <td></td> <td>If the current Slice to be decoded is any slice other than the very last slice of the current picture</td> </tr> </tbody> </table>	Value	Name	Description	1		If the current Slice to be decoded is the very last slice of the current picture.	0		If the current Slice to be decoded is any slice other than the very last slice of the current picture
Value	Name	Description									
1		If the current Slice to be decoded is the very last slice of the current picture.									
0		If the current Slice to be decoded is any slice other than the very last slice of the current picture									
	2:0	<b>First Macroblock (MB)Bit Offset</b> Exists If: //AVC Long Format Only Format: U3  This field provides the bit offset of the first macroblock of the Slice in the first byte of the input compressed bitstream.									
<b>Project:</b> BDW	31	<b>I Slice Concealment Mode</b> Project: <span style="float: right;">BDW</span> This field controls how AVC decoder handle MB concealment in I Slice									
		<table border="1" style="width: 100%;"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Intra Concealment</td> </tr> <tr> <td>1</td> <td>Inter Concealment</td> </tr> </tbody> </table>	Value	Name	0	Intra Concealment	1	Inter Concealment			
Value	Name										
0	Intra Concealment										
1	Inter Concealment										
<b>Programming Notes</b>											
If this field is set to "1" (Inter Concealment), driver must provide a valid reference picture (programmed using "Concealment Reference Picture" field) for concealment reference picture. In this mode, weight prediction is disabled and motion vectors are forced to 0 as well.											
	30	<b>Reserved</b>									
		Project: <span style="float: right;">BDW</span>									
		Format: <span style="float: right;">MBZ</span>									

## Inline Data Description for MFD\_AVC\_BSD\_Object

	29:24	<b>Concealment Reference Picture + Field Bit</b>																							
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>U6</td></tr> </table>	Project:	BDW	Format:	U6																			
Project:	BDW																								
Format:	U6																								
		This field provides the concealment reference picture for hardware to conceal in case driver wants to specify one concealment picture. This field matches with the DPB order sent to hardware. This field applies to all I/P/B slices																							
		<table border="1"> <thead> <tr> <th>Bit Filed</th><th>Value</th><th>Defenition</th></tr> </thead> <tbody> <tr> <td>29</td><td>MBZ</td><td>is reserved for future expansion</td></tr> <tr> <td>28:25</td><td>All</td><td>Reference Picture Number</td></tr> <tr> <td>24</td><td>All</td><td>Field Bit(if the current picture is a field picture [Frame picture must be 0])</td></tr> </tbody> </table>	Bit Filed	Value	Defenition	29	MBZ	is reserved for future expansion	28:25	All	Reference Picture Number	24	All	Field Bit(if the current picture is a field picture [Frame picture must be 0])											
Bit Filed	Value	Defenition																							
29	MBZ	is reserved for future expansion																							
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	23	<b>P Slice Concealment Mode</b>																							
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> </table> <p>This field controls how AVC decoder handle MB concealment in P Slice</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>1</td><td>Intra Concealment</td></tr> <tr> <td>0</td><td>Inter Concealment</td></tr> </tbody> </table>	Project:	BDW	Value	Name	1	Intra Concealment	0	Inter Concealment															
Project:	BDW																								
Value	Name																								
1	Intra Concealment																								
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	22:19	<b>Reserved</b>																							
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	BDW	Format:	MBZ																			
Project:	BDW																								
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	18:16	<b>P Slice Inter Concealment Mode</b>																							
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> </table> <p>This field controls how AVC decoder select reference picture for Concealment in P Slice.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>000b</td><td></td><td>Top of Reference List L0 (Use top entry of Reference List L0)</td></tr> <tr> <td>001b</td><td></td><td>Driver Specified Concealment Reference</td></tr> <tr> <td>010b</td><td></td><td>Predicted Reference (Use reference picture predicted using P-Skip Algorithm)</td></tr> <tr> <td>011b</td><td></td><td>Temporal Closest (Using POC to select the closest forward picture) [For L0: Closest POC smaller than current POC]</td></tr> <tr> <td>100b</td><td></td><td>First Long Term Picture in Reference List L0 (If no long term picture available, use Temporal Closest Picture)</td></tr> <tr> <td>101b-111b</td><td>Reserved</td><td></td></tr> </tbody> </table>	Project:	BDW	Value	Name	Description	000b		Top of Reference List L0 (Use top entry of Reference List L0)	001b		Driver Specified Concealment Reference	010b		Predicted Reference (Use reference picture predicted using P-Skip Algorithm)	011b		Temporal Closest (Using POC to select the closest forward picture) [For L0: Closest POC smaller than current POC]	100b		First Long Term Picture in Reference List L0 (If no long term picture available, use Temporal Closest Picture)	101b-111b	Reserved	
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## Inline Data Description for MFD\_AVC\_BSD\_Object

	15	<b>B Slice Concealment Mode</b>																				
		<table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> </table> <p>This field controls how AVC decoder handle MB concealment in B Slice</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>Intra Concealment</td> </tr> <tr> <td>0</td> <td>Inter Concealment</td> </tr> </tbody> </table>	Project:	BDW	Value	Name	1	Intra Concealment	0	Inter Concealment												
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Value	Name																					
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	13:12	<b>B Slice Inter Direct Type Concealment Mode</b>																				
		<table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> </table> <p>AVC decoder can use Spatial or Temporal Direct for B Skip/Direct. This field determine can override the mode on how AVC decoder handles MB concealment in B slice.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td></td> <td>Use Default Direct Type (slice programmed direct type)</td> </tr> <tr> <td>01b</td> <td></td> <td>Forced to Spatial Direct Only</td> </tr> <tr> <td>10b</td> <td></td> <td>Forced to Temporal Direct Only</td> </tr> <tr> <td>11b</td> <td></td> <td>Spatial Direct without Temporal Componenet (MovingBlock information)</td> </tr> </tbody> </table>	Project:	BDW	Value	Name	Description	00b		Use Default Direct Type (slice programmed direct type)	01b		Forced to Spatial Direct Only	10b		Forced to Temporal Direct Only	11b		Spatial Direct without Temporal Componenet (MovingBlock information)			
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	10:8	<b>B Slice Spatial Inter Concealment Mode</b>																				
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000b		Top of Reference List L0/L1 (Use top entry of Reference List L0/L1).																				
001b		Driver Specified Concealment Reference																				
011b		Temporal Closest (Using POC to select the closest forward picture) [For L0: Closest POC smaller than current POC] [For L1: Closest POC larger than current POC]																				
100b		" First Long Term Picture in Reference List L0/L1 (If no long term picture available, use Temporal Closest Picture)																				
101b-111b	Reserved																					
	7	<b>Reserved</b>																				
		<table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> </table> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	BDW	Format:	MBZ																
Project:	BDW																					
Format:	MBZ																					

## Inline Data Description for MFD\_AVC\_BSD\_Object

	6:4	<b>B Slice Temporal Inter Concealment Mode</b>																							
		<table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td><td style="width: 50%;">BDW</td></tr> </table> <p>This field controls how AVC decoder select reference picture for Temporal Inter Concealment in B Slice</p>	Project:	BDW																					
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		<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="background-color: #d9e1f2; width: 10%;">Value</th><th style="background-color: #d9e1f2; width: 10%;">Name</th><th style="background-color: #d9e1f2; width: 80%;">Description</th></tr> </thead> <tbody> <tr> <td>000b</td><td></td><td>Top of Reference List L0/L1 (Use top entry of Reference List L0/L1)</td></tr> <tr> <td>001b</td><td></td><td>Driver Specified Concealment Reference</td></tr> <tr> <td>010b</td><td></td><td>Predicted Reference (Use reference picture predicted using B-Skip Algorithm)</td></tr> <tr> <td>011b</td><td></td><td>" Temporal Closest (Using POC to select the closest forward picture) [For L0: Closest POC smaller than current POC] [For L1: Closest POC larger than current POC]</td></tr> <tr> <td>100b</td><td></td><td>First Long Term Picture in Reference List L0/L1 (If no long term picture available, use Temporal Closest Picture)</td></tr> <tr> <td>101b-111b</td><td>Reserved</td><td></td></tr> </tbody> </table>			Value	Name	Description	000b		Top of Reference List L0/L1 (Use top entry of Reference List L0/L1)	001b		Driver Specified Concealment Reference	010b		Predicted Reference (Use reference picture predicted using B-Skip Algorithm)	011b		" Temporal Closest (Using POC to select the closest forward picture) [For L0: Closest POC smaller than current POC] [For L1: Closest POC larger than current POC]	100b		First Long Term Picture in Reference List L0/L1 (If no long term picture available, use Temporal Closest Picture)	101b-111b	Reserved	
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	3:2	<b>Reserved</b>																							
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Format:	MBZ																								
	1	<b>Intra 8x8/4x4 Prediction Error Concealment Control Bit</b>																							
		<table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td><td style="width: 50%;">BDW</td></tr> </table> <p>This field controls if AVC goes into MB concealment mode (next MB) when an error is detected on Intra8x8/4x4 Prediction Mode (these 2 modes have fixed coding so it may not affect the bitstream.</p>	Project:	BDW																					
Project:	BDW																								
		<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="background-color: #d9e1f2; width: 10%;">Value</th><th style="background-color: #d9e1f2; width: 10%;">Name</th><th style="background-color: #d9e1f2; width: 80%;">Description</th></tr> </thead> <tbody> <tr> <td>0</td><td></td><td>AVC decoder will NOT go into MB concealment when Intra8x8/4x4 Prediction mode is incorrect.</td></tr> <tr> <td>1</td><td></td><td>AVC decoder will go into MB concealment when Intra8x8/4x4 Prediction mode is incorrect.</td></tr> </tbody> </table>	Value	Name	Description	0		AVC decoder will NOT go into MB concealment when Intra8x8/4x4 Prediction mode is incorrect.	1		AVC decoder will go into MB concealment when Intra8x8/4x4 Prediction mode is incorrect.														
Value	Name	Description																							
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1		AVC decoder will go into MB concealment when Intra8x8/4x4 Prediction mode is incorrect.																							
	0	<b>Intra Prediction Error Control Bit (applied to Intra16x16/Intra8x8/Intra4x4 Luma and Chroma)</b>																							
		<table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td><td style="width: 50%;">BDW</td></tr> </table> <p>This field controls if AVC decoder will fix Intra Prediction Mode if the decoded value is incorrect according to MB position.</p>	Project:	BDW																					
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		<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="background-color: #d9e1f2; width: 10%;">Value</th><th style="background-color: #d9e1f2; width: 10%;">Name</th><th style="background-color: #d9e1f2; width: 80%;">Description</th></tr> </thead> <tbody> <tr> <td>0</td><td></td><td>AVC decoder will detect and fix Intra Prediction Mode Errors.</td></tr> <tr> <td>1</td><td></td><td>AVC decoder will retain the Intra Prediction value decoded from bitstream.</td></tr> </tbody> </table>	Value	Name	Description	0		AVC decoder will detect and fix Intra Prediction Mode Errors.	1		AVC decoder will retain the Intra Prediction value decoded from bitstream.														
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## Inline Data Description - VP8 PAK OBJECT

Inline Data Description - VP8 PAK OBJECT														
DWord	Bit	Description												
0	31:23	<b>Reserved</b>												
		Format:	MBZ											
	22:20	<b>MV Format(Motion Vector Size)</b>												
		Exists If:	//IntraMbFlag = 0											
		This field specifies the size and format of the output motion vectors.												
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>Intra MB</td> <td>No Motion vectors</td> </tr> <tr> <td>100b</td> <td>Inter Predict MB (Unpacked Motion Vector Mode)</td> <td>Sixteen Motion Vectors Per MacroBlock</td> </tr> <tr> <td>Others</td> <td>Reserved</td> <td></td> </tr> </tbody> </table>		Value	Name	Description	000b	Intra MB	No Motion vectors	100b	Inter Predict MB (Unpacked Motion Vector Mode)	Sixteen Motion Vectors Per MacroBlock	Others	Reserved
Value	Name	Description												
000b	Intra MB	No Motion vectors												
100b	Inter Predict MB (Unpacked Motion Vector Mode)	Sixteen Motion Vectors Per MacroBlock												
Others	Reserved													
	<b>Programming Notes</b>													
	This field MBZ, when the <b>IntraMbFlag = 1</b> .													
19:18	<b>SegmentID</b>													
	Format:	U2												
	Segment number 0-3													
17			<b>Enable Coeff Clamp</b>											
			<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>1</td> <td></td> <td>Magnitude of coefficients of the current MB is clamped based on the clamping matrix after quantization</td> </tr> <tr> <td>0</td> <td></td> <td>No Clamping</td> </tr> </tbody> </table>			Value	Name	Description	1		Magnitude of coefficients of the current MB is clamped based on the clamping matrix after quantization	0		No Clamping
Value	Name	Description												
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0		No Clamping												
16:14	<b>Reserved</b>													
		Format:	MBZ											

## Inline Data Description - VP8 PAK OBJECT

	13	<p><b>Intra MB Flag</b> This field specifies whether the current macroblock is an Intra (I) Macroblock. For Key pictures (IsKeyFrameFlag DW2, bit[5] of MFX_VP8_PIC_STATE), this field must be set to 1.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center; padding: 2px;">Value</th><th style="text-align: center; padding: 2px;">Name</th></tr> </thead> <tbody> <tr> <td style="padding: 2px;">0h</td><td style="padding: 2px;">INTER (Inter MacroBlock)</td></tr> <tr> <td style="padding: 2px;">1h</td><td style="padding: 2px;">INTRA (Intra MacroBlock)</td></tr> </tbody> </table> <p style="text-align: center;"><b>Programming Notes</b></p> <p>For I-picture MB (Intra MB Flag = 1), this field must be set to 1.</p>	Value	Name	0h	INTER (Inter MacroBlock)	1h	INTRA (Intra MacroBlock)																		
Value	Name																									
0h	INTER (Inter MacroBlock)																									
1h	INTRA (Intra MacroBlock)																									
	12:11	<p><b>RefPicSelect</b> This field specifies which reference pic (among Last Frame, Golden Frame and Alt Frame) is selected for the current macroblock when Intra MB Flag = 0 .</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center; padding: 2px;">Value</th><th style="text-align: center; padding: 2px;">Name</th></tr> </thead> <tbody> <tr> <td style="padding: 2px;">00b</td><td style="padding: 2px;">Last Frame</td></tr> <tr> <td style="padding: 2px;">01b</td><td style="padding: 2px;">Golden Frame</td></tr> <tr> <td style="padding: 2px;">10b</td><td style="padding: 2px;">Alt Frame</td></tr> </tbody> </table>	Value	Name	00b	Last Frame	01b	Golden Frame	10b	Alt Frame																
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00b	Last Frame																									
01b	Golden Frame																									
10b	Alt Frame																									
	10:8	<p><b>MB Type 3-Bits - Inter/Intra MB</b> MB Type 3 Bits [10:8] specifies InterMB MV mode configurations: 16x16 or 2 16x8 or 4 8x8 or 16x4 when Intra MB Flag = 0 and bit [8] = IntraMB mode configurations: 4x4 or 16x16 when Intra MB Flag = 1</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center; padding: 2px;">Value</th><th style="text-align: center; padding: 2px;">Name</th><th style="text-align: center; padding: 2px;">Description</th></tr> </thead> <tbody> <tr> <td style="padding: 2px;">000b</td><td style="padding: 2px;">16x16</td><td style="padding: 2px;"><b>Inter MB</b> Only DW 6 bits 3:0 are used to indicate MVMode, MVMode can't be split</td></tr> <tr> <td style="padding: 2px;">001b</td><td style="padding: 2px;">2 16x8 (mv_Top Bottom)</td><td style="padding: 2px;"><b>Inter MB [10:8]</b> Split MV is inferred. DW5 bits[3:0] are used for MVMode for first 16x8 partition, DW6 bits[3:0] are used for MVMode for second 16x8 partition.</td></tr> <tr> <td style="padding: 2px;">010b</td><td style="padding: 2px;">2 8 x16 (mv_left_right)</td><td style="padding: 2px;"><b>Inter MB [10:8]</b> Split MV is inferred. DW5 bits[3:0] are used for MVMode for first 8x16 partition, DW5 bits[11:8] are used for MVMode for second 8x16 partition.</td></tr> <tr> <td style="padding: 2px;">011b</td><td style="padding: 2px;">4 8x8 (mv_quarters)</td><td style="padding: 2px;"><b>Inter MB [10:8]</b> Split MV is inferred. DW5 bits[3:0] are used for MVMode for first 8x8 partition. DW5 bits[11:8] are used for MVMode for second 8x8 partition. DW6 bits[3:0] are used for MVMode for third 8x8 partition. DW6 bits[11:8] are used for MVMode for fourth 8x8 partition.</td></tr> <tr> <td style="padding: 2px;">100b</td><td style="padding: 2px;">16 4x4 (mv_16)</td><td style="padding: 2px;"><b>Inter MB [10:8]</b> Split MV is inferred. There are 16 partitions. Each Sub-block uses 4 bits in DW6 and DW7.</td></tr> <tr> <td style="padding: 2px;">0b</td><td style="padding: 2px;">16x16</td><td style="padding: 2px;"><b>Intra MB [8]</b> Only DW5, bits[3:0] are used for Y mode. For B_PRED, "16 4x4" should be used which implies B_PRED mode.</td></tr> <tr> <td style="padding: 2px;">1b</td><td style="padding: 2px;">16 4x4</td><td style="padding: 2px;"><b>Intra MB [8]</b> All bits in DW5 and DW6 are used to represent B_PRED modes (Bmodes) in each sub-blocks.</td></tr> </tbody> </table>	Value	Name	Description	000b	16x16	<b>Inter MB</b> Only DW 6 bits 3:0 are used to indicate MVMode, MVMode can't be split	001b	2 16x8 (mv_Top Bottom)	<b>Inter MB [10:8]</b> Split MV is inferred. DW5 bits[3:0] are used for MVMode for first 16x8 partition, DW6 bits[3:0] are used for MVMode for second 16x8 partition.	010b	2 8 x16 (mv_left_right)	<b>Inter MB [10:8]</b> Split MV is inferred. DW5 bits[3:0] are used for MVMode for first 8x16 partition, DW5 bits[11:8] are used for MVMode for second 8x16 partition.	011b	4 8x8 (mv_quarters)	<b>Inter MB [10:8]</b> Split MV is inferred. DW5 bits[3:0] are used for MVMode for first 8x8 partition. DW5 bits[11:8] are used for MVMode for second 8x8 partition. DW6 bits[3:0] are used for MVMode for third 8x8 partition. DW6 bits[11:8] are used for MVMode for fourth 8x8 partition.	100b	16 4x4 (mv_16)	<b>Inter MB [10:8]</b> Split MV is inferred. There are 16 partitions. Each Sub-block uses 4 bits in DW6 and DW7.	0b	16x16	<b>Intra MB [8]</b> Only DW5, bits[3:0] are used for Y mode. For B_PRED, "16 4x4" should be used which implies B_PRED mode.	1b	16 4x4	<b>Intra MB [8]</b> All bits in DW5 and DW6 are used to represent B_PRED modes (Bmodes) in each sub-blocks.
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## Inline Data Description - VP8 PAK OBJECT

	7:6	<b>Reserved</b>	Format:	MBZ
	5:4	<b>MB UV Mode</b>		
			<b>Value</b>	<b>Name</b>
			0	DC_PRED
			1	V_PRED
			2	H_PRED
			3	TM_PRED
	3	<b>Reserved</b>	Format:	MBZ
	2	<b>Skip MB Flag</b> This field is equivalent to mb_skip_flag in VP8 spec.		
			<b>Programming Notes</b>	
			By setting this field to 1, it forces an Inter MacroBlock to be encoded as a skipped MacroBlock	
	1:0	<b>Reserved</b>	Format:	MBZ
1	31:24	<b>Reserved</b>	Format:	MBZ
	23:16	<b>MbYCnt (Vertical Origin)</b> Format: U8 Unit of MacroBlock This field specifies the vertical origin of current macroblock in the destination picture in units of macroblocks.		
	15:8	<b>Reserved</b>	Format:	MBZ
	7:0	<b>MbXCnt (Horizontal Origin)</b> Format: U8 Unit of MacroBlock This field specifies the horizontal origin of current macroblock in the destination picture in units of macroblocks.		
2	31:28	<b>B Mode for SubBlock7 (Y mode for the macroblock in non-B mode)</b> For Y-Mode and B-Mode Assignments refer to the assignment lists below this table.		
	27:24	<b>B Mode for SubBlock6 (Y mode for the macroblock in non-B mode)</b> For Y-Mode and B-Mode Assignments refer to the assignment lists below this table.		
	23:20	<b>B Mode for SubBlock5 (Y mode for the macroblock in non-B mode)</b> For Y-Mode and B-Mode Assignments refer to the assignment lists below this table.		
	19:16	<b>B Mode for SubBlock4 (Y mode for the macroblock in non-B mode)</b> For Y-Mode and B-Mode Assignments refer to the assignment lists below this table.		

## Inline Data Description - VP8 PAK OBJECT

	15:12	<b>B Mode for SubBlock3 (Y mode for the macroblock in non-B mode)</b> For Y-Mode and B-Mode Assignments refer to the assignment lists below this table.
	11:8	<b>B Mode for SubBlock2 (Y mode for the macroblock in non-B mode)</b> For Y-Mode and B-Mode Assignments refer to the assignment lists below this table.
	7:4	<b>B Mode for SubBlock1 (Y mode for the macroblock in non-B mode)</b> For Y-Mode and B-Mode Assignments refer to the assignment lists below this table.
	3:0	<b>B Mode for SubBlock0 (Y mode for the macroblock in non-B mode)</b> For Y-Mode and B-Mode Assignments refer to the assignment lists below this table.
3	31:28	<b>B Mode for SubBlock15 (Y mode for the macroblock in non-B mode)</b> For Y-Mode and B-Mode Assignments refer to the assignment lists below this table.
	27:24	<b>B Mode for SubBlock14(Y mode for the macroblock in non-B mode)</b> For Y-Mode and B-Mode Assignments refer to the assignment lists below this table.
	23:20	<b>B Mode for SubBlock13(Y mode for the macroblock in non-B mode)</b> For Y-Mode and B-Mode Assignments refer to the assignment lists below this table.
	19:16	<b>B Mode for SubBlock12(Y mode for the macroblock in non-B mode)</b> For Y-Mode and B-Mode Assignments refer to the assignment lists below this table.
	15:12	<b>B Mode for SubBlock11(Y mode for the macroblock in non-B mode)</b> For Y-Mode and B-Mode Assignments refer to the assignment lists below this table.
	11:8	<b>B Mode for SubBlock10 (Y mode for the macroblock in non-B mode)</b> For Y-Mode and B-Mode Assignments refer to the assignment lists below this table.
	7:4	<b>B Mode for SubBlock9 (Y mode for the macroblock in non-B mode)</b> For Y-Mode and B-Mode Assignments refer to the assignment lists below this table.
	3:0	<b>B Mode for SubBlock8 (Y mode for the macroblock in non-B mode)</b> For Y-Mode and B-Mode Assignments refer to the assignment lists below this table.

## INTERFACE\_DESCRIPTOR\_DATA

INTERFACE_DESCRIPTOR_DATA										
DWord	Bit	Description								
0	31:6	<p><b>Kernel Start Pointer</b></p> <table border="1"> <tr> <td>Format:</td> <td>InstructionBaseOffset[31:6]Kernel</td> </tr> </table> <p>Specifies the 64-byte aligned address offset of the first instruction in the kernel. This pointer is relative to the <b>Instruction Base Address</b>.</p>	Format:	InstructionBaseOffset[31:6]Kernel						
Format:	InstructionBaseOffset[31:6]Kernel									
5:0	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ							
Format:	MBZ									
1	31:16	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ						
Format:	MBZ									
15:0	<p><b>Kernel Start Pointer High</b></p> <table border="1"> <tr> <td>Format:</td> <td>InstructionBaseOffset[47:32]Kernel</td> </tr> </table> <p>This field specifies the high 16 bits of starting address of the Kernel Pointer.</p>	Format:	InstructionBaseOffset[47:32]Kernel							
Format:	InstructionBaseOffset[47:32]Kernel									
2	31:20	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	BDW	Format:	MBZ				
Project:	BDW									
Format:	MBZ									
19	<p><b>Denorm Mode</b></p> <p>This field specifies how Float denormalized numbers are handles in the dispatched thread.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Ftz</td> <td>Float denorms will be flushed to zero when appearing as inputs, denorms will never come out of instructions. Double precision float and half precision float numbers are not flushed to zero.</td> </tr> <tr> <td>1h</td> <td>SetByKernel</td> <td>Denorms will be handled in by kernel.</td> </tr> </tbody> </table>	Value	Name	Description	0h	Ftz	Float denorms will be flushed to zero when appearing as inputs, denorms will never come out of instructions. Double precision float and half precision float numbers are not flushed to zero.	1h	SetByKernel	Denorms will be handled in by kernel.
Value	Name	Description								
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1h	SetByKernel	Denorms will be handled in by kernel.								
18	Single Program Flow	<p>Specifies whether the kernel program has a single program flow (SIMDnxm with m = 1) or multiple program flows (SIMDnxm with m &gt; 1).</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Multiple</td> </tr> <tr> <td>1h</td> <td>Single</td> </tr> </tbody> </table>	Value	Name	0h	Multiple	1h	Single		
Value	Name									
0h	Multiple									
1h	Single									

## INTERFACE\_DESCRIPTOR\_DATA

	17	<b>Thread Priority</b> Specifies the priority of the thread for dispatch.							
		<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center; padding: 2px;">Value</th><th style="text-align: center; padding: 2px;">Name</th></tr> </thead> <tbody> <tr> <td style="padding: 2px;">0h</td><td style="padding: 2px;">Normal Priority</td></tr> <tr> <td style="padding: 2px;">1h</td><td style="padding: 2px;">High Priority</td></tr> </tbody> </table>		Value	Name	0h	Normal Priority	1h	High Priority
Value	Name								
0h	Normal Priority								
1h	High Priority								
	16	<b>Floating Point Mode</b> Specifies the floating point mode used by the dispatched thread.							
		<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center; padding: 2px;">Value</th><th style="text-align: center; padding: 2px;">Name</th></tr> </thead> <tbody> <tr> <td style="padding: 2px;">0h</td><td style="padding: 2px;">IEEE-754</td></tr> <tr> <td style="padding: 2px;">1h</td><td style="padding: 2px;">Alternate</td></tr> </tbody> </table>		Value	Name	0h	IEEE-754	1h	Alternate
Value	Name								
0h	IEEE-754								
1h	Alternate								
	15:14	<b>Reserved</b>							
		Format:	MBZ						
	13	<b>Illegal Opcode Exception Enable</b>							
		Format:	Enable						
		This bit gets loaded into EU CR0.1[12] (note the bit # difference). See <i>Exceptions and ISA Execution Environment</i> .							
	12	<b>Reserved</b>							
		Format:	MBZ						
	11	<b>Mask Stack Exception Enable</b>							
		Format:	Enable						
		This bit gets loaded into EU CR0.1[11]. See <i>Exceptions and ISA Execution Environment</i> .							
	10:8	<b>Reserved</b>							
		Format:	MBZ						
	7	<b>Software Exception Enable</b>							
		Format:	Enable						
		This bit gets loaded into EU CR0.1[13] (note the bit # difference). See <i>Exceptions and ISA Execution Environment</i> .							
	6:0	<b>Reserved</b>							
		Format:	MBZ						
	3	<b>Sampler State Pointer</b>							
		Format:	DynamicStateOffset[31:5]SAMPLER_STATE						
		Specifies the 32-byte aligned address offset of the sampler state table. This pointer is relative to the <b>Dynamic State Base Address</b> . <i>This field is ignored for child threads.</i>							

INTERFACE_DESCRIPTOR_DATA																									
	4:2	<b>Sampler Count</b>																							
		<table border="1"> <tr> <td>Format:</td><td colspan="2">U3</td></tr> </table>			Format:	U3																			
Format:	U3																								
		<p>Specifies how many samplers (in multiples of 4) the kernel uses. Used only for prefetching the associated sampler state entries. <i>This field is ignored for child threads.</i> If this field is not zero, sampler state is prefetched for the first instance of a root thread upon the startup of the media pipeline.</p>																							
		<table border="1"> <thead> <tr> <th>Value</th><th colspan="2">Name</th></tr> </thead> <tbody> <tr> <td>[0,4]</td><td colspan="2"></td></tr> <tr> <td>0h</td><td colspan="2">No samplers used</td></tr> <tr> <td>1h</td><td colspan="2">Between 1 and 4 samplers used</td></tr> <tr> <td>2h</td><td colspan="2">Between 5 and 8 samplers used</td></tr> <tr> <td>3h</td><td colspan="2">Between 9 and 12 samplers used</td></tr> <tr> <td>4h</td><td colspan="2">Between 13 and 16 samplers used</td></tr> </tbody> </table>			Value	Name		[0,4]			0h	No samplers used		1h	Between 1 and 4 samplers used		2h	Between 5 and 8 samplers used		3h	Between 9 and 12 samplers used		4h	Between 13 and 16 samplers used	
Value	Name																								
[0,4]																									
0h	No samplers used																								
1h	Between 1 and 4 samplers used																								
2h	Between 5 and 8 samplers used																								
3h	Between 9 and 12 samplers used																								
4h	Between 13 and 16 samplers used																								
	1:0	<b>Reserved</b>																							
		<table border="1"> <tr> <td>Format:</td><td colspan="2">MBZ</td></tr> </table>			Format:	MBZ																			
Format:	MBZ																								
4	31:16	<b>Reserved</b>																							
		<table border="1"> <tr> <td>Format:</td><td colspan="2">MBZ</td></tr> </table>			Format:	MBZ																			
Format:	MBZ																								
	15:5	<b>Binding Table Pointer</b>																							
		<table border="1"> <tr> <td>Format:</td><td colspan="2">SurfaceStateOffset[15:5]BINDING_TABLE_STATE*256</td></tr> </table>			Format:	SurfaceStateOffset[15:5]BINDING_TABLE_STATE*256																			
Format:	SurfaceStateOffset[15:5]BINDING_TABLE_STATE*256																								
		<p>Specifies the 32-byte aligned address of the binding table. This pointer is relative to the <b>Surface State Base Address</b>. <i>This field is ignored for child threads.</i></p>																							
	4:0	<b>Binding Table Entry Count</b>																							
		<table border="1"> <tr> <td>Project:</td><td colspan="2">BDW</td></tr> <tr> <td>Format:</td><td colspan="2">U5</td></tr> </table>			Project:	BDW		Format:	U5																
Project:	BDW																								
Format:	U5																								
		<p>Specifies how many binding table entries the kernel uses. Used only for prefetching of the binding table entries and associated surface state. <i>This field is ignored for child threads.</i> If this field is not zero, binding table and surface state are prefetched for the first instance of a root thread upon the startup of the media pipeline.</p>																							
		<table border="1"> <thead> <tr> <th>Value</th><th colspan="2">Name</th></tr> </thead> <tbody> <tr> <td>[0,31]</td><td colspan="2"></td></tr> </tbody> </table>			Value	Name		[0,31]																	
Value	Name																								
[0,31]																									
		<b>Programming Notes</b>																							
		<p>The maximum number of prefetched binding table entries is limited to 31. For kernels using a large number of binding table entries, it may be wise to set this field to zero to avoid prefetching too many entries and thrashing the state cache.</p>																							

## INTERFACE\_DESCRIPTOR\_DATA

5	31:16	<b>Constant/Indirect URB Entry Read Length</b>															
		<table border="1" style="width: 100%;"> <tr> <td style="padding: 2px;">Format:</td><td style="padding: 2px; text-align: right;">U16</td></tr> </table>	Format:	U16													
Format:	U16																
<p>Specifies the amount of URB data read and passed in the thread payload for the Constant or Indirect URB entry, in 8-DW register increments. A value 0 means that no Constant or Indirect URB Entry will be loaded. The Constant URB Entry Read Offset field will then be ignored. In GPGPU mode this describes how much data is delivered in a single dispatch. Multiple dispatches in a thread group will deliver constant data offset by this value. The total amount of constant data is (Constant URB Read Length * Number of Threads in GPGPU Thread Group + Cross-Thread Constant Data Read Length).</p>																	
<p>If <b>Cross-Thread Constant Data Read Length</b> for Indirect is greater than 0, then this field must also be greater than 0. The allowed combinations are:</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%;">Constant/Indirect URB Entry Read Length <b>Entry Read Length</b></th><th style="width: 50%;">Cross-Thread Constant <b>Data Read Length</b></th><th style="width: 5%;">Notes</th></tr> </thead> <tbody> <tr> <td>=0</td><td>=0</td><td>No Payload</td></tr> <tr> <td>&gt;0</td><td>=0</td><td>Per-thread payload only</td></tr> <tr> <td>&gt;0</td><td>&gt;0</td><td>Both kinds of payload</td></tr> <tr> <td>=0</td><td>&gt;0</td><td>Only for CURBE payloads</td></tr> </tbody> </table>			Constant/Indirect URB Entry Read Length <b>Entry Read Length</b>	Cross-Thread Constant <b>Data Read Length</b>	Notes	=0	=0	No Payload	>0	=0	Per-thread payload only	>0	>0	Both kinds of payload	=0	>0	Only for CURBE payloads
Constant/Indirect URB Entry Read Length <b>Entry Read Length</b>	Cross-Thread Constant <b>Data Read Length</b>	Notes															
=0	=0	No Payload															
>0	=0	Per-thread payload only															
>0	>0	Both kinds of payload															
=0	>0	Only for CURBE payloads															
<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%;">Value</th><th style="width: 50%;">Name</th></tr> </thead> <tbody> <tr> <td style="text-align: center;">[0,63]</td><td></td></tr> </tbody> </table>			Value	Name	[0,63]												
Value	Name																
[0,63]																	
15:0		<b>Constant URB Entry Read Offset</b>															
		<table border="1" style="width: 100%;"> <tr> <td style="padding: 2px;">Format:</td><td style="padding: 2px; text-align: right;">U16</td></tr> </table>	Format:	U16													
Format:	U16																
<p>Specifies the offset (in 8-DW units) at which Constant URB data is to be read from the URB before being included in the thread payload.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 15%;">Value</th><th style="width: 15%;">Name</th><th style="width: 70%;">Description</th></tr> </thead> <tbody> <tr> <td style="text-align: center;">[0,1983]</td><td></td><td>Indicating [0,1983] 256-bit register increments. ROB has 64KB of storage; 2048 entries. However, lowest 64 entries are reserved for VFE/TS to store interface descriptor data. Hence, (URB Entry Read Offset + Read Length) shall not exceed 1984.</td></tr> </tbody> </table>			Value	Name	Description	[0,1983]		Indicating [0,1983] 256-bit register increments. ROB has 64KB of storage; 2048 entries. However, lowest 64 entries are reserved for VFE/TS to store interface descriptor data. Hence, (URB Entry Read Offset + Read Length) shall not exceed 1984.									
Value	Name	Description															
[0,1983]		Indicating [0,1983] 256-bit register increments. ROB has 64KB of storage; 2048 entries. However, lowest 64 entries are reserved for VFE/TS to store interface descriptor data. Hence, (URB Entry Read Offset + Read Length) shall not exceed 1984.															
6	31:24	<b>Reserved</b>															
		<table border="1" style="width: 100%;"> <tr> <td style="padding: 2px;">Format:</td><td style="padding: 2px; text-align: right;">MBZ</td></tr> </table>	Format:	MBZ													
Format:	MBZ																

## INTERFACE\_DESCRIPTOR\_DATA

23:22	<p><b>Rounding Mode</b></p> <table border="1"> <tr> <td>Format:</td><td>U2</td></tr> </table> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>00b</td><td>RTNE [Default]</td><td>Round to Nearest Even</td></tr> <tr> <td>01b</td><td>RU</td><td>Round toward +Infinity</td></tr> <tr> <td>10b</td><td>RD</td><td>Round toward -Infinity</td></tr> <tr> <td>11b</td><td>RTZ</td><td>Round toward Zero</td></tr> </tbody> </table>	Format:	U2	Value	Name	Description	00b	RTNE [Default]	Round to Nearest Even	01b	RU	Round toward +Infinity	10b	RD	Round toward -Infinity	11b	RTZ	Round toward Zero					
Format:	U2																						
Value	Name	Description																					
00b	RTNE [Default]	Round to Nearest Even																					
01b	RU	Round toward +Infinity																					
10b	RD	Round toward -Infinity																					
11b	RTZ	Round toward Zero																					
21	<p><b>Barrier Enable</b></p> <table border="1"> <tr> <td>Format:</td><td>Enable</td></tr> </table> <p>This field specifies whether the thread group requires a barrier. If not, it can be dispatched without allocating one.</p>	Format:	Enable																				
Format:	Enable																						
20:16	<p><b>Shared Local Memory Size</b></p> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>U5</td></tr> </table> <p>This field indicates how much shared local memory the thread group requires. The amount is specified in 4k blocks, but only powers of 2 are allowed: 0, 4k, 8k, 16k, 32k and 64k per half-slice.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0</td><td>Encodes 0k</td></tr> <tr> <td>1</td><td>Encodes 4k</td></tr> <tr> <td>2</td><td>Encodes 8k</td></tr> <tr> <td>4</td><td>Encodes 16k</td></tr> <tr> <td>8</td><td>Encodes 32k</td></tr> <tr> <td>16</td><td>Encodes 64k</td></tr> </tbody> </table> <table border="1"> <thead> <tr> <th>Programming Notes</th><th>Project</th></tr> </thead> <tbody> <tr> <td>If SLMSize &gt; 0, then a barrier must also be allocated.</td><td>BDW</td></tr> </tbody> </table>	Project:	BDW	Format:	U5	Value	Name	0	Encodes 0k	1	Encodes 4k	2	Encodes 8k	4	Encodes 16k	8	Encodes 32k	16	Encodes 64k	Programming Notes	Project	If SLMSize > 0, then a barrier must also be allocated.	BDW
Project:	BDW																						
Format:	U5																						
Value	Name																						
0	Encodes 0k																						
1	Encodes 4k																						
2	Encodes 8k																						
4	Encodes 16k																						
8	Encodes 32k																						
16	Encodes 64k																						
Programming Notes	Project																						
If SLMSize > 0, then a barrier must also be allocated.	BDW																						
15	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	BDW	Format:	MBZ																		
Project:	BDW																						
Format:	MBZ																						
14:10	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ																				
Format:	MBZ																						

<b>INTERFACE_DESCRIPTOR_DATA</b>							
	9:0	<b>Number of Threads in GPGPU Thread Group</b>					
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>U10</td></tr> </table>	Project:	BDW	Format:	U10	
Project:	BDW						
Format:	U10						
		Specifies the number of threads that are in this thread group. The minimum value is 1, while the maximum value is the number of threads in a subslice for local barriers. See vol1b Configurations for the number of threads per subslice for different products. The maximum value for global barriers is limited by the number of threads in the system, or by 511, whichever is lower. This field should not be set to 0 even if the barrier is disabled, since an accurate value is needed for proper pre-emption.					
7	31:8	<b>Reserved</b>					
		<table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ			
Format:	MBZ						
	7:0	<b>Cross-Thread Constant Data Read Length</b>					
		<table border="1"> <tr> <td>Format:</td><td>U8</td></tr> </table>	Format:	U8			
Format:	U8						
		Specifies the amount of constant data in CURBE in 8-DW register increments which will be sent to every thread in the thread group in addition to the per thread ids specified by <b>Constant URB Entry Read Length</b> .					
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>[0,127]</td><td></td></tr> </tbody> </table>	Value	Name	[0,127]		
Value	Name						
[0,127]							

## INTERRUPT

INTERRUPT												
DWord	Bit	Description										
0	31:0	<p><b>ISR</b></p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>These are the Interrupt Status Register Bits. This field contains the non-persistent values of the interrupt status bits. The IMR selects which of these interrupt conditions are reported in the persistent IIR</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Condition Doesn't exist</td> </tr> <tr> <td>1b</td> <td>Condition Exists</td> </tr> </tbody> </table> <p><b>Restriction</b></p> <p>Some inputs to this register are short pulses. Do not use this register to sample these conditions.</p>	Access:	RO	Value	Name	0b	Condition Doesn't exist	1b	Condition Exists		
Access:	RO											
Value	Name											
0b	Condition Doesn't exist											
1b	Condition Exists											
1	31:0	<p><b>IMR</b></p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>These are the Interrupt Mask Register Bits. This field contains a bit mask which selects which interrupt bits from the ISR are reported in the IIR.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>FFFFFFFFFFh</td> <td>All interrupts masked <b>[Default]</b></td> </tr> <tr> <td>0b</td> <td>Not Masked</td> </tr> <tr> <td>1b</td> <td>Masked</td> </tr> </tbody> </table> <p><b>Restriction</b></p> <p>For GT interrupts DO NOT use this register to mask interrupt events. Instead program this IMR to all 0s and use the individual GT command streamer MASK bits in the GT register space. This prevents unneeded messaging to DE.</p>	Access:	R/W	Value	Name	FFFFFFFFFFh	All interrupts masked <b>[Default]</b>	0b	Not Masked	1b	Masked
Access:	R/W											
Value	Name											
FFFFFFFFFFh	All interrupts masked <b>[Default]</b>											
0b	Not Masked											
1b	Masked											

## INTERRUPT

2	31:0	<b>IIR</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td><td style="padding: 2px; text-align: right;">R/WC</td></tr> </table> <p>These are the Interrupt Identity Register Bits. This field holds the persistent values of the interrupt bits from the ISR which are unmasked by the IMR. The IER enables an interrupt to be generated when the corresponding bit in the IIR becomes set. A disabled interrupt will still appear in the IIR. Bits set in this register will remain set (persist) until the interrupt condition is cleared by writing a '1' to the appropriate bits.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 30%;">Value</th><th style="width: 70%;">Name</th></tr> </thead> <tbody> <tr> <td style="padding: 2px;">0b</td><td style="padding: 2px;">Condition Not Detected</td></tr> <tr> <td style="padding: 2px;">1b</td><td style="padding: 2px;">Condition Detected</td></tr> </tbody> </table> <p><b>Programming Notes</b></p> <p>For each bit, the IIR can store a second pending interrupt if two or more of the same interrupt conditions occur before the first condition is cleared. Upon clearing the first interrupt, the IIR bit will momentarily go low, then return high to indicate there is second interrupt pending.</p>	Access:	R/WC	Value	Name	0b	Condition Not Detected	1b	Condition Detected
Access:	R/WC									
Value	Name									
0b	Condition Not Detected									
1b	Condition Detected									
3	31:0	<b>IER</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td><td style="padding: 2px; text-align: right;">R/W</td></tr> </table> <p>These are the Interrupt Enable Register Bits. The field enables an interrupt to be generated when the corresponding bit in the IIR becomes set. A disabled interrupt will still appear in the IIR.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 30%;">Value</th><th style="width: 70%;">Name</th></tr> </thead> <tbody> <tr> <td style="padding: 2px;">0b</td><td style="padding: 2px;">Disabled</td></tr> <tr> <td style="padding: 2px;">1b</td><td style="padding: 2px;">Enabled</td></tr> </tbody> </table> <p><b>Programming Notes</b></p> <p>The master interrupt enable must be set to 1b for any of these enabled interrupts to propagate to PCI device 2 interrupt processing.</p>	Access:	R/W	Value	Name	0b	Disabled	1b	Enabled
Access:	R/W									
Value	Name									
0b	Disabled									
1b	Enabled									

## Invalidate After Read Message Descriptor Control Field

<b>MDC_IAR - Invalidate After Read Message Descriptor Control Field</b>						
<b>DWord</b>	<b>Bit</b>	<b>Description</b>				
0	0	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table> <p>Previously, this Enable field was intended to optimize scratch and spill/fill read messages, where the memory was only used by a single thread and did not need to be maintained after the thread completed. If enabled, it caused all lines in the L3 cache accessed by the message to be invalidated after the read occurred, regardless of whether the line contained modified data. It was intended as a performance hint indicating that the data would no longer be used to avoid writing back data to memory.</p>	Project:	All	Format:	MBZ
Project:	All					
Format:	MBZ					

## JPEG

JPEG		
DWord	Bit	Description
0	15:5	<b>Reserved</b> Format: MBZ
	4	<b>Inconsistent VLD SE Error</b> This flag indicates an inconsistent SE coded in the bit-stream. Bit-stream does not match any entries in the hauffman table.
	3	<b>Extra Block Error</b> This flag indicates extra block coded within an ECS data boundary.
	2	<b>Missing block Error</b> This flag indicates one or more blocks are missing within an ECS data boundary.
	1	<b>Extra ECS Error</b> This flag indicates extra ECS' coded in the bit-stream SCAN payload data.
	0	<b>Missing ECS Error</b> This flag indicates one or more ECS' are missing from the bit-stream SCAN payload data.

## LOD Message Address Payload Control

MACD_LOD - LOD Message Address Payload Control								
DWord	Bit	Description						
0	31:4	<b>Reserved</b>						
		<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> <tr> <td colspan="2">Ignored</td></tr> </table>	Project:	All	Format:	MBZ	Ignored	
Project:	All							
Format:	MBZ							
Ignored								
	3:0	<b>LOD</b>						
		<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U4</td> </tr> <tr> <td colspan="2">Specifies the LOD for this slot.</td></tr> </table>	Project:	All	Format:	U4	Specifies the LOD for this slot.	
Project:	All							
Format:	U4							
Specifies the LOD for this slot.								
<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>[0,14]</td> <td></td> <td>representing LOD</td> </tr> </tbody> </table>			Value	Name	Description	[0,14]		representing LOD
Value	Name	Description						
[0,14]		representing LOD						

## Lower Oword Block Data Payload

MDP_OW1L - Lower Oword Block Data Payload						
DWord	Bit	Description				
0.0-0.3	127:0	<p><b>Oword</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U128</td></tr> </table> <p>Specifies the upper Oword data element</p>	Project:	All	Format:	U128
Project:	All					
Format:	U128					
0.4-0.7	127:0	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>Ignore</td></tr> </table> <p>Ignored</p>	Project:	All	Format:	Ignore
Project:	All					
Format:	Ignore					

## MEDIA\_SURFACE\_STATE

MEDIA_SURFACE_STATE											
DWord	Bit	Description									
0	31:0	<b>Reserved</b>									
		Project:	BDW								
		Format:	MBZ								
1	31:18	<b>Height</b>									
		Format:	U14-1								
		This field specifies the height of the surface in units of pixels. For PLANAR surface formats, this field indicates the height of the Y (luma) plane.									
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> <th>Exists If</th> </tr> </thead> <tbody> <tr> <td>[0,16383]</td> <td></td> <td>representing heights [1,16384]</td> <td>[Surface Type] != FM_STRBUF_*</td> </tr> </tbody> </table>		Value	Name	Description	Exists If	[0,16383]		representing heights [1,16384]	[Surface Type] != FM_STRBUF_*
Value	Name	Description	Exists If								
[0,16383]		representing heights [1,16384]	[Surface Type] != FM_STRBUF_*								
		<b>Programming Notes</b>									
		Height (field value + 1) must be a multiple of 2 for PLANAR_420 surfaces. If Vertical Line Stride is 1, this field indicates the height of the field, not the height of the frame.									
17:4	Width										
		Format:	U14-1								
		This field specifies the width of the surface in units of pixels. For PLANAR surface formats, this field indicates the width of the Y (luma) plane.									
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> <th>Exists If</th> </tr> </thead> <tbody> <tr> <td>[0,16383]</td> <td></td> <td>representing widths [1,16384]</td> <td>[Surface Type] != FM_STRBUF_*</td> </tr> </tbody> </table>		Value	Name	Description	Exists If	[0,16383]		representing widths [1,16384]	[Surface Type] != FM_STRBUF_*
Value	Name	Description	Exists If								
[0,16383]		representing widths [1,16384]	[Surface Type] != FM_STRBUF_*								
		<b>Programming Notes</b>									
		<ul style="list-style-type: none"> <li>The Width specified by this field multiplied by the pixel size in bytes must be less than or equal to the surface pitch (specified in bytes via the Surface Pitch field).</li> <li>Width (field value + 1) must be a multiple of 2 for PLANAR_420, PLANAR_422, and all YCRCB_* and Y16_UNORM surfaces, and must be a multiple of 4 for PLANAR_411 and Y8_UNORM_VA surfaces.</li> <li>For deinterlace messages, the Width (field value + 1) must be a multiple of 8.</li> <li>For Y8_UNORM_VA format width should be in multiple of 4, for Y16_UNORM_VA format width should be in multiple of 2, for Y1_UNORM format width should be in multiple of</li> </ul>									

## MEDIA\_SURFACE\_STATE

		<p>32</p> <ul style="list-style-type: none"> <li>When Address Control = Mirror, the total width should be in multiple of 4bytes.</li> </ul> <p>Width (field value + 1) must be a multiple of 2 for PLANAR_420_16</p>										
	3:2	<p><b>Picture Structure</b></p> <p>Specifies the encoding of the current picture.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>00b</td><td>Frame Picture</td></tr> <tr> <td>01b</td><td>Top Field Picture</td></tr> <tr> <td>10b</td><td>Bottom Field Picture</td></tr> <tr> <td>11b</td><td>Invalid, not allowed</td></tr> </tbody> </table>	Value	Name	00b	Frame Picture	01b	Top Field Picture	10b	Bottom Field Picture	11b	Invalid, not allowed
Value	Name											
00b	Frame Picture											
01b	Top Field Picture											
10b	Bottom Field Picture											
11b	Invalid, not allowed											
	1:0	<p><b>Cr(V)/Cb(U) Pixel Offset V Direction</b></p> <table border="1"> <tr> <td>Default Value:</td><td>0</td></tr> <tr> <td>Format:</td><td>U0.2</td></tr> </table> <p><b>Description</b></p> <p>Specifies the distance to the U/V values with respect to the even numbered Y channels in the V direction</p> <p><b>Programming Notes</b></p> <p>This field is ignored for all formats except PLANAR_420_8</p>	Default Value:	0	Format:	U0.2						
Default Value:	0											
Format:	U0.2											

## MEDIA\_SURFACE\_STATE

2	31:27	<b>Surface Format</b>																																																									
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> </table>	Project:	BDW																																																							
Project:	BDW																																																										
Specifies the format of the surface. All of the Y and G channels will use table 0 and all of the Cr/Cb/R/B channels will use table 1.																																																											
Note: Y8_UNORM_VA, Y16_UNORM and Y16_SNORM are used for all functions of sample_8x8 except AVS where rest of the formats are not used. These two formats are packed as 32bits in L1 though the individual pixels are either 8bpp or 16bpp respectively.																																																											
<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr><td>0</td><td>YCRCB_NORMAL</td><td></td></tr> <tr><td>1</td><td>YCRCB_SWAPUVY</td><td></td></tr> <tr><td>2</td><td>YCRCB_SWAPUV</td><td></td></tr> <tr><td>3</td><td>YCRCB_SWAPY</td><td></td></tr> <tr><td>4</td><td>PLANAR_420_8</td><td></td></tr> <tr><td>5</td><td>Y8_UNORM_VA</td><td>Sample_8x8 only except AVS</td></tr> <tr><td>6</td><td>Y16_SNORM</td><td>Sample_8x8 only except AVS</td></tr> <tr><td>7</td><td>Y16_UNORM_VA</td><td>Sample_8x8 only except AVS</td></tr> <tr><td>8</td><td>R10G10B10A2_UNORM</td><td>Sample_8x8 only</td></tr> <tr><td>9</td><td>R8G8B8A8_UNORM</td><td>Sample_8x8 AVS only</td></tr> <tr><td>10</td><td>R8B8_UNORM (CrCb)</td><td>Sample_8x8 AVS only</td></tr> <tr><td>11</td><td>R8_UNORM (Cr/Cb)</td><td>Sample_8x8 AVS only</td></tr> <tr><td>12</td><td>Y8_UNORM</td><td>Sample_8x8 AVS only</td></tr> <tr><td>13</td><td>A8Y8U8V8_UNORM</td><td>Sample_8x8 AVS only</td></tr> <tr><td>14</td><td>B8G8R8A8_UNORM</td><td>Sample_8x8 AVS only</td></tr> <tr><td>15</td><td>R16G16B16A16</td><td>Sample_8x8 AVS only</td></tr> <tr><td>16</td><td>Y1_UNORM</td><td>Sample_8x8 only for boolean surfaces (1bit/pixel)</td></tr> <tr><td>Others</td><td>Reserved</td><td></td></tr> </tbody> </table>			Value	Name	Description	0	YCRCB_NORMAL		1	YCRCB_SWAPUVY		2	YCRCB_SWAPUV		3	YCRCB_SWAPY		4	PLANAR_420_8		5	Y8_UNORM_VA	Sample_8x8 only except AVS	6	Y16_SNORM	Sample_8x8 only except AVS	7	Y16_UNORM_VA	Sample_8x8 only except AVS	8	R10G10B10A2_UNORM	Sample_8x8 only	9	R8G8B8A8_UNORM	Sample_8x8 AVS only	10	R8B8_UNORM (CrCb)	Sample_8x8 AVS only	11	R8_UNORM (Cr/Cb)	Sample_8x8 AVS only	12	Y8_UNORM	Sample_8x8 AVS only	13	A8Y8U8V8_UNORM	Sample_8x8 AVS only	14	B8G8R8A8_UNORM	Sample_8x8 AVS only	15	R16G16B16A16	Sample_8x8 AVS only	16	Y1_UNORM	Sample_8x8 only for boolean surfaces (1bit/pixel)	Others	Reserved	
Value	Name	Description																																																									
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26	<b>Interleave Chroma</b>																																																										
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<table border="1"> <thead> <tr> <th>Description</th></tr> </thead> <tbody> <tr> <td>This field indicates that the chroma fields are interleaved in a single plane rather than stored as two separate planes. This field is only used for PLANAR surface formats.</td></tr> </tbody> </table>			Description	This field indicates that the chroma fields are interleaved in a single plane rather than stored as two separate planes. This field is only used for PLANAR surface formats.																																																							
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25:22	<b>Reserved</b>																																																										
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	BDW	Format:	MBZ																																																					
Project:	BDW																																																										
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<b>MEDIA_SURFACE_STATE</b>													
21	<b>Address Control</b>												
	Project:		BDW										
	<b>Surface Pitch</b>												
	Format:		U18-1 pitch in Bytes										
	This field specifies the surface pitch in (#Bytes - 1).												
	<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>[0,262143]</td><td></td><td>For other linear surfaces: representing [1B, 256KB]</td></tr> <tr> <td>[511, 262143]</td><td></td><td>For X-tiled surface: representing [512B, 256KB] = [1 tile, 512 tiles]</td></tr> <tr> <td>[127, 262143]</td><td></td><td>For Y-tiled surfaces: representing [128B, 256KB] = [1 tile, 2048 tiles]</td></tr> </tbody> </table>		Value	Name	Description	[0,262143]		For other linear surfaces: representing [1B, 256KB]	[511, 262143]		For X-tiled surface: representing [512B, 256KB] = [1 tile, 512 tiles]	[127, 262143]	
Value	Name	Description											
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[511, 262143]		For X-tiled surface: representing [512B, 256KB] = [1 tile, 512 tiles]											
[127, 262143]		For Y-tiled surfaces: representing [128B, 256KB] = [1 tile, 2048 tiles]											
<b>Programming Notes</b>													
For tiled surfaces, the pitch must be a multiple of the tile widthIf Half Pitch for Chroma is set, this field must be a multiple of two tile widths for tiled surfaces, or a multiple of 2 bytes for linear surfaces.The Surface Pitches of current picture and reference picture should be declared as the identical type in VDI mode with identical Height, Width and Format.													
2	<b>Half Pitch for Chroma</b>												
	Format:		Enable										
	This field indicates that the chroma plane(s) will use a pitch equal to half the value specified in the Surface Pitch field. This field is only used for PLANAR surface formats.												
	<b>Programming Notes</b>												
	Must be Zero as this field is not used.												

## MEDIA SURFACE STATE

1:0	<p><b>Tile Mode</b></p> <table border="1"> <tr> <td>Format:</td><td>U2 Enumerated Type</td></tr> </table> <p>This field specifies the type of memory tiling (Linear, WMajor, XMajor, or YMajor) employed to tile this surface. See Memory Interface Functions for details on memory tiling and restrictions.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0h</td><td>TILEMODE_LINEAR</td><td>Linear mode (no tiling)</td></tr> <tr> <td>1h</td><td>Reserved</td><td>Reserved</td></tr> <tr> <td>2h</td><td>TILEMODE_XMAJOR</td><td>X major tiling</td></tr> <tr> <td>3h</td><td>TILEMODE_YMAJOR</td><td>Y major tiling</td></tr> </tbody> </table>	Format:	U2 Enumerated Type	Value	Name	Description	0h	TILEMODE_LINEAR	Linear mode (no tiling)	1h	Reserved	Reserved	2h	TILEMODE_XMAJOR	X major tiling	3h	TILEMODE_YMAJOR	Y major tiling
Format:	U2 Enumerated Type																	
Value	Name	Description																
0h	TILEMODE_LINEAR	Linear mode (no tiling)																
1h	Reserved	Reserved																
2h	TILEMODE_XMAJOR	X major tiling																
3h	TILEMODE_YMAJOR	Y major tiling																
<b>Programming Notes</b>																		
<ul style="list-style-type: none"> <li>Refer to <i>Memory Data Formats</i> for restrictions on TileMode direction for the various buffer types. (Of particular interest is the fact that YMAJOR tiling is not supported for display/overlay buffers).</li> </ul>																		
<ul style="list-style-type: none"> <li>The corresponding cache(s) must be invalidated before a previously accessed surface is accessed again with an altered state of this field.</li> </ul>																		
<ul style="list-style-type: none"> <li>Linear surfaces can be mapped to Main Memory (uncached) or System Memory (cacheable, snooped). Tiled (X/Y/W) surfaces can only be mapped to Main Memory.</li> </ul>																		
3	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> </table> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	All	Format:	MBZ													
Project:	All																	
Format:	MBZ																	
29:16	<p><b>X Offset for U(Cb)</b></p> <table border="1"> <tr> <td>Format:</td> <td>U14 Pixel Offset</td> </tr> </table>	Format:	U14 Pixel Offset															
Format:	U14 Pixel Offset																	
<b>Description</b>																		
<p>For non planar surfaces this field specifies the horizontal offset in pixels from the Surface Base Address to the start (origin) of the surface.</p>																		
<p>For Planar surfaces this field specifies the horizontal offset in pixels from the Surface Base Address to the start (origin) of the U(Cb) plane or the interleaved UV plane if Interleave Chroma is enabled.</p>																		
<b>Programming Notes</b>																		
<p>For PLANAR_420 and PLANAR_422 surface formats, this field must indicate an even number of pixels.</p>																		
15:14	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ															
Format:	MBZ																	

<b>MEDIA_SURFACE_STATE</b>				
13:0		<b>Y Offset for U(Cb)</b>		
		Format:	U14 Row Offset	
<b>Description</b>				
For non planar surfaces this field specifies the vertical offset in pixels from the Surface Base Address to the start (origin) of the surface.				
For Planar surfaces this field specifies the vertical offset in rows from the Surface Base Address to the start (origin) of the U(Cb) plane or the interleaved UV plane if Interleave Chroma is enabled.				
4	31:30	<b>Reserved</b>		
		Project:	All	
29:16		<b>X Offset for V(Cr)</b>		
		Exists If:	//([Surface Format] is one of planar) AND ([Interleave Chroma] == '0')	
		Format:	U14 Pixel Offset	
		<b>Description</b>		
		This field specifies the horizontal offset in pixels from the Surface Base Address to the start (origin) of the V(Cr) plane.		
		<b>Programming Notes</b>		
15		<b>Reserved</b>		
		Format:	MBZ	
14:0		<b>Y Offset for V(Cr)</b>		
		Exists If:	//([Surface Format] is one of planar) AND ([Interleave Chroma] == '0')	
		Format:	U15 Row Offset	
		<b>Description</b>		
		This field specifies the vertical offset in rows from the Surface Base Address to the start (origin) of the V(Cr) plane.		
		<b>Programming Notes</b>		
		This field must indicate a multiple of 4 (bit 0 & 1 = 00).		

## MEDIA\_SURFACE\_STATE

5	31	<b>Vertical Line Stride</b>						
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>U1 in lines to skip between logically adjacent lines</td></tr> </table>	Project:	BDW	Format:	U1 in lines to skip between logically adjacent lines		
Project:	BDW							
Format:	U1 in lines to skip between logically adjacent lines							
For Surfaces accessed via the sample_8x8 message: Specifies number of lines (0 or 1) to skip between logically adjacent lines - provides support of interleaved (field) surfaces as textures. For Other Surfaces: Vertical Line Stride must be zero.								
<b>Workaround</b>								
Workaround (BDW bug# 1909178) : All surfaces used by the sampler between sampler cache invalidates must have the same setting of this field in both RENDER_SURFACE_STATE and MEDIA_SURFACE_STATE.								
<b>Vertical Line Stride Offset</b>								
<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>U1 in lines of initial offset (when Vertical Line Stride == 1)</td></tr> </table>	Project:	BDW	Format:	U1 in lines of initial offset (when Vertical Line Stride == 1)				
Project:	BDW							
Format:	U1 in lines of initial offset (when Vertical Line Stride == 1)							
For Surfaces accessed via the sample_8x8 message: Specifies the offset of the initial line from the beginning of the buffer. For Other Surfaces: Vertical Line Stride Offset must be zero.								
30		<b>Programming Notes</b>						
		This field must be set to 0 if Vertical Line Stride is 0.						
29:24	<b>Reserved</b>	<table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ				
Format:	MBZ							
23:20	<b>Reserved</b>	<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	BDW	Format:	MBZ		
Project:	BDW							
Format:	MBZ							
19:18	<b>Reserved</b>	<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	BDW	Format:	MBZ		
Project:	BDW							
Format:	MBZ							
17:7	<b>Reserved</b>	<table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ				
Format:	MBZ							
6:0	<b>Surface Memory Object Control State</b>	<table border="1"> <tr> <td>Default Value:</td><td>0h DefaultValueDesc</td></tr> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td><b>MEMORY_OBJECT_CONTROL_STATE</b></td></tr> </table> <p>This 7-bit field is used in various state commands and indirect state objects to define cacheability and other attributes related to memory objects.</p>	Default Value:	0h DefaultValueDesc	Project:	BDW	Format:	<b>MEMORY_OBJECT_CONTROL_STATE</b>
Default Value:	0h DefaultValueDesc							
Project:	BDW							
Format:	<b>MEMORY_OBJECT_CONTROL_STATE</b>							

<b>MEDIA_SURFACE_STATE</b>						
6	31:0	<p><b>Surface Base Address</b></p> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>GraphicsAddress[31:0]</td></tr> </table> <p>Specifies the low 32 bits of the byte-aligned base address of the surface.</p> <p><b>Programming Notes</b></p> <p>For SURFTYPE_BUFFER render targets, this field specifies the base address of first element of the surface. The surface is interpreted as a simple array of that single element type. The address must be naturally-aligned to the element size (e.g., a buffer containing R32G32B32A32_FLOAT elements must be 16-byte aligned). For SURFTYPE_BUFFER non-rendertarget surfaces, this field specifies the base address of the first element of the surface, computed in software by adding the surface base address to the byte offset of the element in the buffer. Mipmapped, cube and 3D sampling engine surfaces are stored in a 'monolithic' (fixed) format, and only require a single address for the base texture. Linear render target surface base addresses must be element-size aligned, for non-YUV surface formats, or a multiple of 2 element-sizes for YUV surface formats. Other linear surfaces have no alignment requirements (byte alignment is sufficient.) Linear depth buffer surface base addresses must be 64-byte aligned. Note that while render targets (color) can be SURFTYPE_BUFFER, depth buffers cannot. Tiled surface base addresses must be 4KB-aligned. Note that only the offsets from Surface Base Address are tiled, Surface Base Address itself is not transformed using the tiling algorithm. For tiled surfaces, the actual start of the surface can be offset from the Surface Base Address by the X Offset and Y Offset fields. Certain message types used to access surfaces have more stringent alignment requirements. Please refer to the specific message documentation for additional restrictions.</p>	Project:	BDW	Format:	GraphicsAddress[31:0]
Project:	BDW					
Format:	GraphicsAddress[31:0]					
7	31:16	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ		
Format:	MBZ					
	15:0	<p><b>Surface Base Address High</b></p> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>GraphicsAddress[47:32]</td></tr> </table> <p>Specifies the high 16 bits of the byte-aligned base address of the surface. Refer to Surface Base Address [31:0] for programming notes applying to this field.</p>	Project:	BDW	Format:	GraphicsAddress[47:32]
Project:	BDW					
Format:	GraphicsAddress[47:32]					

## MEMORY\_OBJECT\_CONTROL\_STATE

MEMORY_OBJECT_CONTROL_STATE																	
DWord	Bit	Description															
0	6:5	<p><b>Memory Type:LLC/eLLC Cacheability Control</b>  This is the field used in the GT interface block to determine what type of access is generated to Uncore. For the cases where LELLCCC is set, cacheable transactions are generated to enable LLC usage for particular streams.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>UC with Fence (if coherent cycle)</td> <td>Use Cacheability Controls from page table</td> </tr> <tr> <td>01b</td> <td>UC (Uncacheable)</td> <td>non-cacheable</td> </tr> <tr> <td>10b</td> <td>WT</td> <td>Writethrough</td> </tr> <tr> <td>11b</td> <td>WB</td> <td>Writeback</td> </tr> </tbody> </table>	Value	Name	Description	00b	UC with Fence (if coherent cycle)	Use Cacheability Controls from page table	01b	UC (Uncacheable)	non-cacheable	10b	WT	Writethrough	11b	WB	Writeback
Value	Name	Description															
00b	UC with Fence (if coherent cycle)	Use Cacheability Controls from page table															
01b	UC (Uncacheable)	non-cacheable															
10b	WT	Writethrough															
11b	WB	Writeback															
	4:3	<p><b>Target Cache</b>  This field controls the L3\$, LLC and eLLC (eDRAM) cacheability for a given surface. Setting of "00" points to PTE settings which defaults to eDRAM (when present). If no eDRAM, the access will be allocated to LLC. Setting of "01", allocates into LLC and victimizes the line to eDRAM. Setting of "10" allows the line to be allocated in either LLC or eDRAM. Setting of "11" is the only option for a memory access to be allocated in L3\$ as well as LLC/eLLC. Errata BDW:A-E (FIXED BY:G0 Stepping): For all system that does NOT use SVM (i.e. coherent L3\$ surfaces), back snoops from LLC has to be disabled (Dis_GtCvUpdtOnRd = "1"). Than target Cache settings can be programmed as POR requirements of L3/LLC/eDRAM caching. For all systems that does use SVM (i.e. coherent L3\$ surfaces), the recommended setting would be "00" in target cache settings. In case of L3 surfaces, the performance has to be tuned between "00" and "11" setting based on the benefits of L3 caching outweighing the degradation of backsnoops.  Post G0-stepping, the above w/a for coherent L3\$ surfaces is not needed.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>eLLC Only (when eDRAM is present, else gets allocated in LLC)</td> <td></td> </tr> <tr> <td>01b</td> <td>LLC Only</td> <td></td> </tr> <tr> <td>10b</td> <td>LLC/eLLC Allowed</td> <td></td> </tr> <tr> <td>11b</td> <td>L3 + Defer to PAT for LLC/eLLC selection</td> <td>Post G0 stepping this field has been changed to allow L3 caching without the need to cache in LLC. L3 Caching will be enabled for TC="11", however LLC and eLLC selection will be based on the PAT value programmed.</td> </tr> </tbody> </table>	Value	Name	Description	00b	eLLC Only (when eDRAM is present, else gets allocated in LLC)		01b	LLC Only		10b	LLC/eLLC Allowed		11b	L3 + Defer to PAT for LLC/eLLC selection	Post G0 stepping this field has been changed to allow L3 caching without the need to cache in LLC. L3 Caching will be enabled for TC="11", however LLC and eLLC selection will be based on the PAT value programmed.
Value	Name	Description															
00b	eLLC Only (when eDRAM is present, else gets allocated in LLC)																
01b	LLC Only																
10b	LLC/eLLC Allowed																
11b	L3 + Defer to PAT for LLC/eLLC selection	Post G0 stepping this field has been changed to allow L3 caching without the need to cache in LLC. L3 Caching will be enabled for TC="11", however LLC and eLLC selection will be based on the PAT value programmed.															
	2	<b>Reserved</b>															

## MEMORY\_OBJECT\_CONTROL\_STATE

1:0	<b>Age for QUADLRU</b> This field allows the selection of AGE parameter for a given surface in LLC or eLLC. If a particular allocation is done at youngest age ("0,1,2") it tends to stay longer in the cache. This option is given to GFX software to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches.															
<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="background-color: #e0e0ff; text-align: left; padding: 2px;">Value</th> <th style="background-color: #e0e0ff; text-align: left; padding: 2px;">Name</th> <th style="background-color: #e0e0ff; text-align: left; padding: 2px;">Description</th> </tr> </thead> <tbody> <tr> <td style="padding: 2px;">00b</td> <td style="padding: 2px;"></td> <td style="padding: 2px;">MRU - allocated with a higher age (default is 2) which needs to be decremented to 0 before it can be considered for victimization.</td> </tr> <tr> <td style="padding: 2px;">01b</td> <td style="padding: 2px;"></td> <td style="padding: 2px;">MRU - allocated with a higher age (default is 2) which needs to be decremented to 0 before it can be considered for victimization.</td> </tr> <tr> <td style="padding: 2px;">10b</td> <td style="padding: 2px;"></td> <td style="padding: 2px;">MRU - allocated with a higher age (default is 2) which needs to be decremented to 0 before it can be considered for victimization.</td> </tr> <tr> <td style="padding: 2px;">11b</td> <td style="padding: 2px;"></td> <td style="padding: 2px;">LRU - allocated with lower age (default is 0) which makes it likely to be victimized during next victimization.</td> </tr> </tbody> </table>		Value	Name	Description	00b		MRU - allocated with a higher age (default is 2) which needs to be decremented to 0 before it can be considered for victimization.	01b		MRU - allocated with a higher age (default is 2) which needs to be decremented to 0 before it can be considered for victimization.	10b		MRU - allocated with a higher age (default is 2) which needs to be decremented to 0 before it can be considered for victimization.	11b		LRU - allocated with lower age (default is 0) which makes it likely to be victimized during next victimization.
Value	Name	Description														
00b		MRU - allocated with a higher age (default is 2) which needs to be decremented to 0 before it can be considered for victimization.														
01b		MRU - allocated with a higher age (default is 2) which needs to be decremented to 0 before it can be considered for victimization.														
10b		MRU - allocated with a higher age (default is 2) which needs to be decremented to 0 before it can be considered for victimization.														
11b		LRU - allocated with lower age (default is 0) which makes it likely to be victimized during next victimization.														

## MemoryAddressAttributes

MemoryAddressAttributes		
DWord	Bit	Description
<b>Project:</b> BDW	0	<b>Reserved</b>
	31:9	Project: Format:
	8:7	<b>Base Address - Arbitration Priority Control</b>
	8:7	Project: Format:
	6:5	<b>Reserved</b>
	6:5	Project:
	4:3	<b>Base Address - Target Cache (TC)</b>
	4:3	Project: Format:
	2	This field allows the choice of LLC vs. eLLC for caching.
	2	<b>Reserved</b>
	2	Project:

## MemoryAddressAttributes

1:0	<b>Base Address - Age for QUADLRU (AGE)</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Project:</td><td style="padding: 2px;">BDW</td></tr> <tr> <td style="padding: 2px;">Format:</td><td style="padding: 2px;">U2</td></tr> </table> <p>This field allows the selection of AGE parameter for a given surface in LLC. If a particular allocation is done at youngest age ("3") it tends to stay longer in the cache as compared to older age allocations ("2", "1", or "0"). This option is given to the driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches.</p> <p>This field is also used for eLLC.</p> <table border="1" style="width: 100%; border-collapse: collapse; margin-top: 10px;"> <thead> <tr style="background-color: #d9e1f2;"> <th style="width: 15%;">Value</th><th style="width: 85%;">Name</th></tr> </thead> <tbody> <tr> <td style="padding: 2px;">00b</td><td style="padding: 2px;">Good chance of generating hits</td></tr> <tr> <td style="padding: 2px;">01b</td><td style="padding: 2px;">Next good chance of generating hits</td></tr> <tr> <td style="padding: 2px;">10b</td><td style="padding: 2px;">Decent chance of generating hits</td></tr> <tr> <td style="padding: 2px;">11b</td><td style="padding: 2px;">Poor chance of generating hits</td></tr> </tbody> </table>	Project:	BDW	Format:	U2	Value	Name	00b	Good chance of generating hits	01b	Next good chance of generating hits	10b	Decent chance of generating hits	11b	Poor chance of generating hits
Project:	BDW														
Format:	U2														
Value	Name														
00b	Good chance of generating hits														
01b	Next good chance of generating hits														
10b	Decent chance of generating hits														
11b	Poor chance of generating hits														

## Merged Media Block Message Header

<b>MH_MBM - Merged Media Block Message Header</b>						
<b>DWord</b>	<b>Bit</b>	<b>Description</b>				
0	31:0	<p><b>X Offset</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>S31</td> </tr> </table> <p>X offset (in bytes) of the upper left corner of the block into the surface.</p>	Project:	All	Format:	S31
Project:	All					
Format:	S31					
1	31:0	<p><b>Y Offset</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>S31</td> </tr> </table> <p>Y offset (in rows) of the upper left corner of the block into the surface.</p>	Project:	All	Format:	S31
Project:	All					
Format:	S31					
2	31:0	<p><b>Merged Media Block Message Control</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td><b>MHC_MBM_CONTROL</b></td> </tr> </table> <p>Specifies the Merged message subtype and additional input parameters.</p>	Project:	All	Format:	<b>MHC_MBM_CONTROL</b>
Project:	All					
Format:	<b>MHC_MBM_CONTROL</b>					
3	31:0	<p><b>Mask</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U32</td> </tr> </table> <p>The Mask is ignored by the Merged Media Block message: all Dwords are always returned on reads, and always enabled to be written on writes.</p>	Project:	All	Format:	U32
Project:	All					
Format:	U32					
4	31:0	<p><b>FFTID</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td><b>MHC_FFTID</b></td> </tr> </table> <p>Fixed Function Thread ID</p>	Project:	All	Format:	<b>MHC_FFTID</b>
Project:	All					
Format:	<b>MHC_FFTID</b>					
5-7	95:0	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Ignore</td> </tr> </table> <p>Ignored</p>	Project:	All	Format:	Ignore
Project:	All					
Format:	Ignore					

## Merged Media Block Message Header Control

### MHC\_MBM\_CONTROL - Merged Media Block Message Header Control

Project: BDW  
 Size (in bits): 32  
 Default Value: 0x00000000

DWord	Bit	Description									
0	31:30	<b>Message Mode</b>									
		Project:	All	Format:	Enumeration						
Specifies the Media Block Read message is Normal subtype.											
29		Value	Name	Description	Project						
		00h	Normal	The Block Height and Block Width fields are specified in this Dword. The Mask is ignored by a media block read message.	All						
28:24		Others	Reserved	Reserved.	All						
		<b>Reserved</b>									
<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Ignore</td> </tr> <tr> <td colspan="2">Ignored</td></tr> </table>						Project:	All	Format:	Ignore	Ignored	
Project:	All										
Format:	Ignore										
Ignored											
		<b>Sub-Register Offset</b>									
		Project:	All	Format:	U5						
Provides the sub-register offset in unit of bytes of a Merged Media Block Read message. This field is ignored (reserved) for a media block write message. Range = [0, 28]. Only a multiple of BasePitch, including 0, is valid.											
		<b>Programming Notes</b>									
		Sub-Register Offset and Register Pitch Control allow software to assemble multiple media block reads directly into a shared GRF register set. For example, if both are set to zero, the read data are written to GRF registers, aligning to the least significant bits of the first register, and the register pitch is equal to the next power-of-2 that is greater than or equal to the Block Width. If Register Pitch Control is non-zero, multiple media block read messages sharing the same Register Pitch Control but with different Sub-Register Offset can fill in the same set of GRF registers with media block data line interleaved.									
		<b>Restriction</b>									
		For the Sampler Cache Data, this field must be zero.									
BasePitch is defined as the next power-of-2 that is greater than or equal to the Block Width. Minimum BasePitch is 1 DWord.											
Sub-Register Offset must be aligned to BasePitch (therefore will be a multiple of DWords as											

## MHC\_MBM\_CONTROL - Merged Media Block Message Header Control

	<p>well). When Register Pitch Control = 0, Sub-Register Offset must align to BasePitch*Block Height, ensuring the output fits in a single GRF register. In general (and specifically when Sub-Register Offset is greater than 0), when the resulting data will cross a GRF register boundary, the data must be placed symmetrically between GRF registers.</p>						
23:22	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>Ignore</td></tr> <tr> <td colspan="2">Ignored</td></tr> </table>	Project:	All	Format:	Ignore	Ignored	
Project:	All						
Format:	Ignore						
Ignored							
21:16	<p><b>Block Height</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U6</td></tr> <tr> <td colspan="2">Height in rows of block being accessed. Range = [0,63] representing 1 to 64 rows</td></tr> </table> <p style="text-align: center;"><b>Restriction</b></p> <p>If Block Width (bytes), then Maximum Block Height (rows) is constrained by (# Dwords width) * (# rows) &lt;= 64 Dwords.</p>	Project:	All	Format:	U6	Height in rows of block being accessed. Range = [0,63] representing 1 to 64 rows	
Project:	All						
Format:	U6						
Height in rows of block being accessed. Range = [0,63] representing 1 to 64 rows							
15:10	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>Ignore</td></tr> <tr> <td colspan="2">Ignored</td></tr> </table>	Project:	All	Format:	Ignore	Ignored	
Project:	All						
Format:	Ignore						
Ignored							
9:8	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td><td>BDW*:A0</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> <tr> <td colspan="2">Restriction : Must be zero.</td></tr> </table>	Project:	BDW*:A0	Format:	MBZ	Restriction : Must be zero.	
Project:	BDW*:A0						
Format:	MBZ						
Restriction : Must be zero.							
7:6	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>Ignore</td></tr> <tr> <td colspan="2">Ignored</td></tr> </table>	Project:	All	Format:	Ignore	Ignored	
Project:	All						
Format:	Ignore						
Ignored							
5:0	<p><b>Block Width</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U6</td></tr> <tr> <td colspan="2">Width in bytes of the block being accessed. Range = [0,31] representing 1 to 32 Bytes.</td></tr> </table>	Project:	All	Format:	U6	Width in bytes of the block being accessed. Range = [0,31] representing 1 to 32 Bytes.	
Project:	All						
Format:	U6						
Width in bytes of the block being accessed. Range = [0,31] representing 1 to 32 Bytes.							

## Message Descriptor - Render Target Write

Message Descriptor - Render Target Write															
DWord	Bit	Description													
0	31	<b>Reserved</b> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ											
Format:	MBZ														
	30	<b>Reserved</b> <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	BDW	Format:	MBZ									
Project:	BDW														
Format:	MBZ														
	29:14	<b>Reserved</b> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ											
Format:	MBZ														
	13	<b>Reserved</b> <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	BDW	Format:	MBZ									
Project:	BDW														
Format:	MBZ														
	12	<b>Last Render Target Select</b> This bit must be set on the last render target write message sent for each group of pixels. For single render target pixel shaders, this bit is set on all render target write messages. For multiple render target pixel shaders, this bit is set only on messages sent to the last render target. This bit must be zero for SIMD8 Image Write message. <table border="1"> <tr> <td align="center" colspan="2"><b>Programming Notes</b></td></tr> <tr> <td align="center" colspan="2">In general, when threads are not launched by 3D FF, this bit must be zero.</td></tr> </table>	<b>Programming Notes</b>		In general, when threads are not launched by 3D FF, this bit must be zero.										
<b>Programming Notes</b>															
In general, when threads are not launched by 3D FF, this bit must be zero.															
	11	<b>Slot Group Select</b> This field selects whether slots 15:0 or slots 31:16 are used for bypassed data. Bypassed data includes the antialias alpha, multisample coverage mask, and if the header is not present also includes the X/Y addresses and pixel enables. For 8- and 16-pixel dispatches, SLOTGRP_LO must be selected on every message. For 32-pixel dispatches, this field must be set correctly for each message based on which slots are currently being processed. <table border="1"> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> <tr> <td>0</td> <td>SLOTGRP_LO</td> <td>choose bypassed data for slots 15:0</td> </tr> <tr> <td>1</td> <td>SLOTGRP_HI</td> <td>choose bypassed data for slots 31:16</td> </tr> </table> <table border="1"> <tr> <td align="center" colspan="2"><b>Programming Notes</b></td></tr> <tr> <td align="center" colspan="2">For SIMD8 Image Write message this field MBZ.</td></tr> </table>	Value	Name	Description	0	SLOTGRP_LO	choose bypassed data for slots 15:0	1	SLOTGRP_HI	choose bypassed data for slots 31:16	<b>Programming Notes</b>		For SIMD8 Image Write message this field MBZ.	
Value	Name	Description													
0	SLOTGRP_LO	choose bypassed data for slots 15:0													
1	SLOTGRP_HI	choose bypassed data for slots 31:16													
<b>Programming Notes</b>															
For SIMD8 Image Write message this field MBZ.															

## Message Descriptor - Render Target Write

10:8	<b>Message Type</b>		
	This field specifies the type of render target message. For the SIMD8_DUALSRC_xx messages, the low bit indicates which slots to use for the pixel enables, X/Y addresses, and oMask.		
	<b>Value</b>	<b>Name</b>	<b>Description</b>
	000b	SIMD16	SIMD16 single source message
	001b	SIMD16_REPDATA	SIMD16 single source message with replicated data
	010b	SIMD8_DUALSRC_LO	SIMD8 dual source message, use slots 7:0
	011b	SIMD8_DUALSRC_HI	SIMD8 dual source message, use slots 15:8
7:0	100b	SIMD8_LO	SIMD8 single source message, use slots 7:0
	111b	SIMD16_REPDATA	It's only supported when accessing <i>Tiled Memory</i> . Using this Message Type to access linear ( <i>Untiled</i> ) memory is UNDEFINED.
	<b>Programming Notes</b>		
	the above slots indicated are within the 16 slots selected by <b>Slot Group Select</b> . If SLOTGRP_HI is selected, the SIMD8 message types above reference slots 23:16 or 31:24 instead of 7:0 or 15:8, respectively.		
	SIMD16_REPDATA message must not be used in SIMD8 pixel-shaders.		
7:0	<b>Reserved</b>		
	Format:	MBZ	

## Message Descriptor - Sampling Engine

Message Descriptor - Sampling Engine								
DWord	Bit	Description						
0	31	<p><b>EOT</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> </table>	Project:	All				
Project:	All							
	30	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	BDW	Format:	MBZ		
Project:	BDW							
Format:	MBZ							
	29	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	BDW	Format:	MBZ		
Project:	BDW							
Format:	MBZ							
	28:25	<p><b>Message Length</b></p> <table border="1"> <tr> <td>Format:</td> <td>U4</td> </tr> </table> <p>This field specifies the number of 256-bit GRF registers starting from (src) to be sent out on the request message payload.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>[1,15]</td> <td></td> </tr> </tbody> </table> <p><b>Programming Notes</b></p> <p>A value of 0 is considered erroneous.</p>	Format:	U4	Value	Name	[1,15]	
Format:	U4							
Value	Name							
[1,15]								
	24:20	<p><b>Response Length</b></p> <table border="1"> <tr> <td>Format:</td> <td>U5</td> </tr> </table> <p>This field indicates the number of 256-bit registers expected in the message response.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>[0,16]</td> <td></td> </tr> </tbody> </table> <p><b>Programming Notes</b></p> <p>A value 0 indicates that the request message does not expect any response. The largest response supported is 16 GRF registers.</p>	Format:	U5	Value	Name	[0,16]	
Format:	U5							
Value	Name							
[0,16]								
	19	<p><b>Header Present</b></p> <table border="1"> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>Specifies whether the message includes a header phase. If the header is not present (this field is zero), all of the fields normally contained in the header are assumed to be 0.</p>	Format:	Enable				
Format:	Enable							

## Message Descriptor - Sampling Engine

	18:17	<b>SIMD Mode[1:0]</b>						
		<table border="1"> <tr> <td>Format:</td><td>U2</td></tr> </table> <p>Specifies the SIMD mode of the message being sent.</p>	Format:	U2				
Format:	U2							
	16:12	<b>Message Type</b>						
		<table border="1"> <tr> <td>Format:</td><td>U5</td></tr> </table> <p>Specifies the type of message being sent. For more details, please refer to <b>Message Format</b> section for the definition of these 5 bits..</p>	Format:	U5				
Format:	U5							
	11:8	<b>Sampler Index</b>						
		<table border="1"> <tr> <td>Format:</td><td>U4</td></tr> </table> <p>Specifies the index into the sampler state table. Ignored for Id, resinfo, sampleinfo, and cache_flush type messages.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>[0,15]</td><td></td></tr> </tbody> </table>	Format:	U4	Value	Name	[0,15]	
Format:	U4							
Value	Name							
[0,15]								
		<b>Programming Notes</b>						
		<ul style="list-style-type: none"> <li>For the deinterlace message, this field must be a multiple of 2 (even).</li> <li>For the sample_8x8 message, this field must be a multiple of 4.</li> </ul>						
	7:0	<b>Binding Table Index</b>						
		<table border="1"> <tr> <td>Format:</td><td>U8</td></tr> </table> <p>Specifies the index into the <b>binding table</b>. Ignored for cache_flush type messages. Values of 255 and 253 indicate stateless. 254 indicates SLM. 252 indicates bindless.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>[0,255]</td><td></td></tr> </tbody> </table>	Format:	U8	Value	Name	[0,255]	
Format:	U8							
Value	Name							
[0,255]								

## MFD\_MPEG2\_BSD\_OBJECT Inline Data Description

MFD_MPEG2_BSD_OBJECT Inline Data Description											
DWord	Bit	Description									
0	31:24	<p><b>Slice Horizontal Position</b></p> <table border="1"> <tr> <td>Format:</td> <td>U8 in Macroblocks</td> </tr> </table> <p>This field indicates the horizontal position of the first macroblock in the slice.</p>	Format:	U8 in Macroblocks							
Format:	U8 in Macroblocks										
	23:16	<p><b>Slice Vertical Position</b></p> <table border="1"> <tr> <td>Format:</td> <td>U8 in Macroblocks</td> </tr> </table> <p>This field indicates the vertical position of the first macroblock in the slice.</p>	Format:	U8 in Macroblocks							
Format:	U8 in Macroblocks										
	15:8	<p><b>Macroblock Count</b></p> <table border="1"> <tr> <td>Format:</td> <td>U8 in Macroblocks</td> </tr> </table> <p>This field indicates the number of macroblocks in the slice, including skipped macroblocks.</p>	Format:	U8 in Macroblocks							
Format:	U8 in Macroblocks										
	7	<p><b>Slice Concealment Override Bit</b></p> <p>This bit forces hardware to handle the current slice in Conceal or Deocde Mode. If this bit is set to one, VIN will force the current slice to do concealment or to decode from bitstream regardless if the slice boundary has errors or not.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>1h</td> <td></td> <td>VIN will use driver-provided "Slice Concealment Type" regardless of valid slice boundary</td> </tr> <tr> <td>0h</td> <td></td> <td>Driver must program "Slice Concealment Type" to '0'. VIN will set "Slice Concealment Type" depending if the slice boundary has error or not</td> </tr> </tbody> </table>	Value	Name	Description	1h		VIN will use driver-provided "Slice Concealment Type" regardless of valid slice boundary	0h		Driver must program "Slice Concealment Type" to '0'. VIN will set "Slice Concealment Type" depending if the slice boundary has error or not
Value	Name	Description									
1h		VIN will use driver-provided "Slice Concealment Type" regardless of valid slice boundary									
0h		Driver must program "Slice Concealment Type" to '0'. VIN will set "Slice Concealment Type" depending if the slice boundary has error or not									
	6	<p><b>Slice Concealment Type Bit</b></p> <p>This bit can be forced by driver ("Slice Concealment Override Bit") or set by VINunit depending on slice boundary errors.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>1h</td> <td></td> <td>VMD will conceal all MBs of the slice regardless of bitstream. (If driver does not force the value of this bit, VIN will set this bit depending on slice boundary error. If the next slice position of the current slice is out-of-bound or the same or earlier than the current slice start position, VIN will set this bit for the next slice)</td> </tr> <tr> <td>0h</td> <td></td> <td>VMD will decode MBs from the bitstream until the bitstream is run-out. Then VMD will conceal the remaining MBs.</td> </tr> </tbody> </table> <p><b>Programming Notes</b></p> <p>VIN can turn this bit from 0 to 1 internally if "Slice Concealment Disable Bit" is "0" and VIN</p>	Value	Name	Description	1h		VMD will conceal all MBs of the slice regardless of bitstream. (If driver does not force the value of this bit, VIN will set this bit depending on slice boundary error. If the next slice position of the current slice is out-of-bound or the same or earlier than the current slice start position, VIN will set this bit for the next slice)	0h		VMD will decode MBs from the bitstream until the bitstream is run-out. Then VMD will conceal the remaining MBs.
Value	Name	Description									
1h		VMD will conceal all MBs of the slice regardless of bitstream. (If driver does not force the value of this bit, VIN will set this bit depending on slice boundary error. If the next slice position of the current slice is out-of-bound or the same or earlier than the current slice start position, VIN will set this bit for the next slice)									
0h		VMD will decode MBs from the bitstream until the bitstream is run-out. Then VMD will conceal the remaining MBs.									

## MFD\_MPEG2\_BSD\_OBJECT Inline Data Description

		detects slice boundary errors.									
5	<b>Last Pic Slice</b>	This bit is added to support error concealment at the end of a picture.									
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>1h</td><td></td><td>The current Slice is the last Slice of the entire picture</td></tr> <tr> <td>0h</td><td></td><td>The current Slice is not the last Slice of current picture</td></tr> </tbody> </table>	Value	Name	Description	1h		The current Slice is the last Slice of the entire picture	0h		The current Slice is not the last Slice of current picture
Value	Name	Description									
1h		The current Slice is the last Slice of the entire picture									
0h		The current Slice is not the last Slice of current picture									
4	<b>Reserved</b>										
3	<b>Is Last MB</b>	<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>1h</td><td></td><td>The current MB is the last MB in the current Slice</td></tr> <tr> <td>0h</td><td></td><td>The current MB is not the last MB in the current Slice</td></tr> </tbody> </table>	Value	Name	Description	1h		The current MB is the last MB in the current Slice	0h		The current MB is not the last MB in the current Slice
Value	Name	Description									
1h		The current MB is the last MB in the current Slice									
0h		The current MB is not the last MB in the current Slice									
2:0	<b>First Macroblock Bit Offset</b>	<table border="1"> <tr> <td>Format:</td><td>U3</td></tr> </table> <p>This field provides the bit offset of the first macroblock in the first byte of the input bitstream.</p>	Format:	U3							
Format:	U3										
1	31:29	<b>Reserved</b> <table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ							
Format:	MBZ										
	28:24	<b>Quantizer Scale Code</b> <table border="1"> <tr> <td>Format:</td><td>U5</td></tr> </table> <p>This field sets the quantizer scale code of the inverse quantizer. It remains in effect until changed by a decoded quantizer scale code in a macroblock. This field is decoded from the slice header by host software.</p>	Format:	U5							
Format:	U5										
	23:17	<b>Reserved</b> <table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ							
Format:	MBZ										
	16:8	<b>Next Slice Vertical Position</b> <table border="1"> <tr> <td>Format:</td><td>U9 in macroblocks</td></tr> </table> <p>This field indicates the vertical position (in macroblock units) of the first macroblock in the next slice.</p> <table border="1"> <tr> <td align="center"><b>Programming Notes</b></td></tr> </table> <p>This field is primarily used for error concealment. In the case that current slice is the last slice, this field should set to the height of the picture (field picture will be in height of field) (since y-direction is zero-based numbering).</p>	Format:	U9 in macroblocks	<b>Programming Notes</b>						
Format:	U9 in macroblocks										
<b>Programming Notes</b>											
	7:0	<b>Next Slice Horizontal Position</b> <table border="1"> <tr> <td>Format:</td><td>U8 in macroblocks</td></tr> </table> <p>This field indicates the horizontal position (in macroblock units) of the first macroblock in the next slice.</p> <table border="1"> <tr> <td align="center"><b>Programming Notes</b></td></tr> </table> <p>This field is primarily used for error concealment. In the case that current slice is the last slice, this field should set 0.</p>	Format:	U8 in macroblocks	<b>Programming Notes</b>						
Format:	U8 in macroblocks										
<b>Programming Notes</b>											

## MPEG2

MPEG2		
DWord	Bit	Description
0	15:6	<b>Reserved</b> Format: <input type="text"/> MBZ
	5	<b>Missing EOB Error</b> This flag indicates missing EOB SEs coded in the bit-stream. Missing EOBs are concealed to match CBP of the error MB.
	4	<b>Inconsistent starting position Error - overlapping MBs</b> This flag indicates two slices overlapping one another by one or more MBs. Duplicate MBs decoded off the second slice shall be discarded.
	3	<b>Slice out-of-bound Error</b> This flag indicates a slice is running beyond the width of the picture. Out-of-bound MBs shall be discarded.
	2	<b>Premature frame end Error</b> This flag indicates missing slices/MBs coded in the bit-stream of a frame. One or more MBs are concealed to reach end of picture.
	1	<b>Inconsistent starting position Error - Missing MBs</b> This flag indicates one or more MBs are being concealed due to inconsistent MB starting and ending positions between slices.
	0	<b>MB Concealment Flag</b> . Each pulse from this flag indicates one MB is concealed by hardware.

## MsgDescpt31

MsgDescpt31						
DWord	Bit	Description				
0	28:25	<p><b>Message Length</b></p> <p>This field specifies the number of 256-bit MRF registers starting from &lt;curr_dest&gt; to be sent out on the request message payload. Valid value ranges from 1 to 15. A value of 0 is considered erroneous.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>1-15</td> <td>Number of MRF Registers</td> </tr> </tbody> </table>	Value	Name	1-15	Number of MRF Registers
Value	Name					
1-15	Number of MRF Registers					
	24:20	<p><b>Response Length</b></p> <p>This field indicates the number of 256-bit registers expected in the message response. The valid value ranges from 0 to 16. A value 0 indicates that the request message does not expect any response. The largest response supported is 16 GRF registers.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0-16</td> <td>Number of Registers</td> </tr> </tbody> </table>	Value	Name	0-16	Number of Registers
Value	Name					
0-16	Number of Registers					
	19	<p><b>Header Present</b></p> <table border="1"> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>If set, indicates that the message includes a header. Depending on the target shared function, this field may be restricted to either enabled or disabled. Refer to the specific shared function section for details.</p>	Format:	Enable		
Format:	Enable					
	18:0	<p><b>Function Control</b></p> <p>This field is intended to control the target function unit. Refer to the section on the specific target function unit for details on the contents of this field.</p>				

## Normal Media Block Message Header

<b>MH_MB - Normal Media Block Message Header</b>						
<b>DWord</b>	<b>Bit</b>	<b>Description</b>				
0	31:0	<p><b>X Offset</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>S31</td> </tr> </table> <p>X offset (in bytes) of the upper left corner of the block into the surface.</p> <p><b>Programming Notes</b></p> <p>Must be DWord aligned (Bits 1:0 MBZ) for the write form of the message.</p>	Project:	All	Format:	S31
Project:	All					
Format:	S31					
1	31:0	<p><b>Y Offset</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>S31</td> </tr> </table> <p>Y offset (in rows) of the upper left corner of the block into the surface.</p>	Project:	All	Format:	S31
Project:	All					
Format:	S31					
2	31:0	<p><b>Normal Media Block Message Control</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td><b>MHC_MB_CONTROL</b></td> </tr> </table> <p>Specifies the Normal message subtype and additional input parameters.</p>	Project:	All	Format:	<b>MHC_MB_CONTROL</b>
Project:	All					
Format:	<b>MHC_MB_CONTROL</b>					
3	31:0	<p><b>Mask</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U32</td> </tr> </table> <p>The Mask is ignored by the Normal Media Block message: all Dwords are always returned on reads, and always enabled to be written on writes.</p>	Project:	All	Format:	U32
Project:	All					
Format:	U32					
4	31:0	<p><b>FFTID</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td><b>MHC_FFTID</b></td> </tr> </table> <p>Fixed Function Thread ID</p>	Project:	All	Format:	<b>MHC_FFTID</b>
Project:	All					
Format:	<b>MHC_FFTID</b>					
5-7	95:0	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Ignore</td> </tr> </table> <p>Ignored</p>	Project:	All	Format:	Ignore
Project:	All					
Format:	Ignore					

## Normal Media Block Message Header Control

### MHC\_MB\_CONTROL - Normal Media Block Message Header Control

Project: BDW  
Size (in bits): 32  
Default Value: 0x00000000

DWord	Bit	Description			
0	31:30	<b>Message Mode</b>			
		Project:	All		
		Format:	Enumeration		
		Specifies the interpretation of M0.3 (Pixel or Byte Mask). For the Sampler Cache Data Port, this field is ignored, behaving as if always set to NORMAL.			
Value					
00h	Normal	The Block Height and Block Width fields are specified in this Dword. The Mask is ignored by a media block read message and behaves as if it is set to all ones for a media block write message.			
Others	Reserved	Reserved.			
Programming Notes					
The Media Block Read message is Normal subtype when both Sub-Register Offset and Register Pitch Control are zero. The Media Block Read message is Merged subtype when either Sub-Register Offset or Register Pitch Control are non-zero.					
29	29	<b>Reserved</b>			
		Project:	All		
		Format:	Ignore		
		Ignored			
28:24	28:24	<b>Sub-Register Offset</b>			
		Project:	All		
		Format:	MBZ		
		The sub-register offset must be 0 for Normal Media Block Read message subtype. This field is ignored (reserved) for a media block write message.			
23:22	23:22	<b>Reserved</b>			
		Project:	All		
		Format:	Ignore		
		Ignored			

## MHC\_MB\_CONTROL - Normal Media Block Message Header Control

		<p><b>21:16 Block Height</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U6</td> </tr> </table> <p>Height in rows of block being accessed. Range = [0,63] representing 1 to 64 rows</p> <p style="text-align: center;"><b>Restriction</b></p> <p>If Block Width (bytes), then Maximum Block Height (rows) is constrained by (# Dwords width) * (# rows) &lt;= 64 Dwords.</p> <p><b>15:10 Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Ignore</td> </tr> </table> <p>Ignored</p> <p><b>9:8 Register Pitch Control</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table> <p>The register pitch must be 0 for a Normal Media Block Read message. This field is ignored (reserved) for a media block write message.</p> <p><b>7:6 Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Ignore</td> </tr> </table> <p>Ignored</p> <p><b>5:0 Block Width</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U6</td> </tr> </table> <p>Width in bytes of the block being accessed. For normal Media Block Writes, Range = [0,63] representing 1 to 64 Bytes. For normal Media Block Reads and for masked and merged Media Block messages, Range = [0,31] representing 1 to 32 Bytes.</p> <p style="text-align: center;"><b>Programming Notes</b></p> <p>Must be DWord aligned for the write form of the message.</p>	Project:	All	Format:	U6	Project:	All	Format:	Ignore	Project:	All	Format:	MBZ	Project:	All	Format:	Ignore	Project:	All	Format:	U6
Project:	All																					
Format:	U6																					
Project:	All																					
Format:	Ignore																					
Project:	All																					
Format:	MBZ																					
Project:	All																					
Format:	Ignore																					
Project:	All																					
Format:	U6																					

## oMask Message Data Payload Register

MDPR_OMASK - oMask Message Data Payload Register						
DWord	Bit	Description				
0	31:16	<p><b>oMask1</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U16</td> </tr> </table> <p>oMask for Pixels [15:0] of Slot 1. Not used for Slot Group HI.</p>	Project:	All	Format:	U16
Project:	All					
Format:	U16					
15:0	<p><b>oMask0</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U16</td> </tr> </table> <p>oMask for Pixels [15:0] of Slot 0. Not used for Slot Group HI.</p>	Project:	All	Format:	U16	
Project:	All					
Format:	U16					
1	31:16	<p><b>oMask3</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U16</td> </tr> </table> <p>oMask for Pixels [15:0] of Slot 3. Not used for Slot Group HI.</p>	Project:	All	Format:	U16
Project:	All					
Format:	U16					
15:0	<p><b>oMask2</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U16</td> </tr> </table> <p>oMask for Pixels [15:0] of Slot 2. Not used for Slot Group HI.</p>	Project:	All	Format:	U16	
Project:	All					
Format:	U16					
2	31:16	<p><b>oMask5</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U16</td> </tr> </table> <p>oMask for Pixels [15:0] of Slot 5. Not used for Slot Group HI.</p>	Project:	All	Format:	U16
Project:	All					
Format:	U16					
15:0	<p><b>oMask4</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U16</td> </tr> </table> <p>oMask for Pixels [15:0] of Slot 4. Not used for Slot Group HI.</p>	Project:	All	Format:	U16	
Project:	All					
Format:	U16					
3	31:16	<p><b>oMask7</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U16</td> </tr> </table> <p>oMask for Pixels [15:0] of Slot 7. Not used for Slot Group HI.</p>	Project:	All	Format:	U16
Project:	All					
Format:	U16					

MDPR_OMASK - oMask Message Data Payload Register						
	15:0	<b>oMask6</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U16</td></tr> </table> oMask for Pixels [15:0] of Slot 6. Not used for Slot Group HI.	Project:	All	Format:	U16
Project:	All					
Format:	U16					
4	31:16	<b>oMask9</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U16</td></tr> </table> oMask for Pixels [15:0] of Slot 9. Used only if Slot Group HI or SIMD16.	Project:	All	Format:	U16
Project:	All					
Format:	U16					
	15:0	<b>oMask8</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U16</td></tr> </table> oMask for Pixels [15:0] of Slot 8. Used only if Slot Group HI or SIMD16.	Project:	All	Format:	U16
Project:	All					
Format:	U16					
5	31:16	<b>oMask11</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U16</td></tr> </table> oMask for Pixels [15:0] of Slot 11. Used only if Slot Group HI or SIMD16.	Project:	All	Format:	U16
Project:	All					
Format:	U16					
	15:0	<b>oMask10</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U16</td></tr> </table> oMask for Pixels [15:0] of Slot 10. Used only if Slot Group HI or SIMD16.	Project:	All	Format:	U16
Project:	All					
Format:	U16					
6	31:16	<b>oMask13</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U16</td></tr> </table> oMask for Pixels [15:0] of Slot 13. Used only if Slot Group HI or SIMD16.	Project:	All	Format:	U16
Project:	All					
Format:	U16					
	15:0	<b>oMask12</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U16</td></tr> </table> oMask for Pixels [15:0] of Slot 12. Used only if Slot Group HI or SIMD16.	Project:	All	Format:	U16
Project:	All					
Format:	U16					
7	31:16	<b>oMask15</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U16</td></tr> </table> oMask for Pixels [15:0] of Slot 15. Used only if Slot Group HI or SIMD16.	Project:	All	Format:	U16
Project:	All					
Format:	U16					
	15:0	<b>oMask14</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U16</td></tr> </table> oMask for Pixels [15:0] of Slot 14. Used only if Slot Group HI or SIMD16.	Project:	All	Format:	U16
Project:	All					
Format:	U16					

## OM Replicated SIMD16 Render Target Data Payload

<b>MDP_RTW_M16REP - OM Replicated SIMD16 Render Target Data Payload</b>						
<b>DWord</b>	<b>Bit</b>	<b>Description</b>				
0.0-0.7	255:0	<p><b>oMask</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDPR_OMASK</b></td></tr> </table> <p>Slots [15:0] oMask</p>	Project:	All	Format:	<b>MDPR_OMASK</b>
Project:	All					
Format:	<b>MDPR_OMASK</b>					
1.0-1.7	255:0	<p><b>RGBA</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDPR_RGBA</b></td></tr> </table> <p>RGBA for all slots [15:0]</p>	Project:	All	Format:	<b>MDPR_RGBA</b>
Project:	All					
Format:	<b>MDPR_RGBA</b>					

## OM SOA SIMD8 Render Target Data Payload

<b>MDP_RTW_MA8 - OM SOA SIMD8 Render Target Data Payload</b>						
<b>DWord</b>	<b>Bit</b>	<b>Description</b>				
0.0-0.7	255:0	<p><b>Source 0 Alpha</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW_SIMD8</b></td></tr> </table> <p>Slots [7:0] Source 0 Alpha</p>	Project:	All	Format:	<b>MDP_DW_SIMD8</b>
Project:	All					
Format:	<b>MDP_DW_SIMD8</b>					
1.0-1.7	255:0	<p><b>oMask</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDPR_OMASK</b></td></tr> </table> <p>Slots [7:0] oMask. Upper half ignored.</p>	Project:	All	Format:	<b>MDPR_OMASK</b>
Project:	All					
Format:	<b>MDPR_OMASK</b>					
2.0-2.7	255:0	<p><b>Red</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW_SIMD8</b></td></tr> </table> <p>Slots [7:0] Red</p>	Project:	All	Format:	<b>MDP_DW_SIMD8</b>
Project:	All					
Format:	<b>MDP_DW_SIMD8</b>					
3.0-3.7	255:0	<p><b>Green</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW_SIMD8</b></td></tr> </table> <p>Slots [7:0] Green</p>	Project:	All	Format:	<b>MDP_DW_SIMD8</b>
Project:	All					
Format:	<b>MDP_DW_SIMD8</b>					
4.0-4.7	255:0	<p><b>Blue</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW_SIMD8</b></td></tr> </table> <p>Slots [7:0] Blue</p>	Project:	All	Format:	<b>MDP_DW_SIMD8</b>
Project:	All					
Format:	<b>MDP_DW_SIMD8</b>					
5.0-5.7	255:0	<p><b>Alpha</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW_SIMD8</b></td></tr> </table> <p>Slots [7:0] Alpha</p>	Project:	All	Format:	<b>MDP_DW_SIMD8</b>
Project:	All					
Format:	<b>MDP_DW_SIMD8</b>					

## OM SOA SIMD16 Render Target Data Payload

<b>MDP_RTW_MA16 - OM SOA SIMD16 Render Target Data Payload</b>						
<b>DWord</b>	<b>Bit</b>	<b>Description</b>				
0.0-0.7	255:0	<p><b>Source 0 Alpha[7:0]</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW SIMD8</b></td></tr> </table> <p>Slots [7:0] Source 0 Alpha</p>	Project:	All	Format:	<b>MDP_DW SIMD8</b>
Project:	All					
Format:	<b>MDP_DW SIMD8</b>					
1.0-1.7	255:0	<p><b>Source 0 Alpha[15:8]</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW SIMD8</b></td></tr> </table> <p>Slots [15:8] Source 0 Alpha</p>	Project:	All	Format:	<b>MDP_DW SIMD8</b>
Project:	All					
Format:	<b>MDP_DW SIMD8</b>					
2.0-2.7	255:0	<p><b>oMask</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDPR_OMASK</b></td></tr> </table> <p>Slots [15:0] oMask</p>	Project:	All	Format:	<b>MDPR_OMASK</b>
Project:	All					
Format:	<b>MDPR_OMASK</b>					
3.0-3.7	255:0	<p><b>Red[7:0]</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW SIMD8</b></td></tr> </table> <p>Slots [7:0] Red</p>	Project:	All	Format:	<b>MDP_DW SIMD8</b>
Project:	All					
Format:	<b>MDP_DW SIMD8</b>					
4.0-4.7	255:0	<p><b>Red[15:8]</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW SIMD8</b></td></tr> </table> <p>Slots [15:8] Red</p>	Project:	All	Format:	<b>MDP_DW SIMD8</b>
Project:	All					
Format:	<b>MDP_DW SIMD8</b>					

<b>MDP_RTW_MA16 - OM SOA SIMD16 Render Target Data Payload</b>						
5.0-5.7	255:0	<b>Green[7:0]</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW_SIMD8</b></td></tr> </table> Slots [7:0] Green	Project:	All	Format:	<b>MDP_DW_SIMD8</b>
Project:	All					
Format:	<b>MDP_DW_SIMD8</b>					
6.0-6.7	255:0	<b>Green[15:8]</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW_SIMD8</b></td></tr> </table> Slots [15:8] Green	Project:	All	Format:	<b>MDP_DW_SIMD8</b>
Project:	All					
Format:	<b>MDP_DW_SIMD8</b>					
7.0-7.7	255:0	<b>Blue[7:0]</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW_SIMD8</b></td></tr> </table> Slots [7:0] Blue	Project:	All	Format:	<b>MDP_DW_SIMD8</b>
Project:	All					
Format:	<b>MDP_DW_SIMD8</b>					
8.0-8.7	255:0	<b>Blue[15:8]</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW_SIMD8</b></td></tr> </table> Slots [15:8] Blue	Project:	All	Format:	<b>MDP_DW_SIMD8</b>
Project:	All					
Format:	<b>MDP_DW_SIMD8</b>					
9.0-9.7	255:0	<b>Alpha[7:0]</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW_SIMD8</b></td></tr> </table> Slots [7:0] Alpha	Project:	All	Format:	<b>MDP_DW_SIMD8</b>
Project:	All					
Format:	<b>MDP_DW_SIMD8</b>					
10.0-10.7	255:0	<b>Alpha[15:8]</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW_SIMD8</b></td></tr> </table> Slots [15:8] Alpha	Project:	All	Format:	<b>MDP_DW_SIMD8</b>
Project:	All					
Format:	<b>MDP_DW_SIMD8</b>					

## OM SIMD8 Dual Source Render Target Data Payload

MDP_RTW_M8DS - OM SIMD8 Dual Source Render Target Data Payload						
DWord	Bit	Description				
0.0-0.7	255:0	<p><b>oMask</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDPR_OMASK</b></td></tr> </table> <p>oMask for slots [7:0] and [15:8]. Operation selects upper or lower half.</p>	Project:	All	Format:	<b>MDPR_OMASK</b>
Project:	All					
Format:	<b>MDPR_OMASK</b>					
1.0-1.7	255:0	<p><b>Src0 Red</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW_SIMD8</b></td></tr> </table> <p>Slots[7:0] or [15:8] of Src0 Red</p>	Project:	All	Format:	<b>MDP_DW_SIMD8</b>
Project:	All					
Format:	<b>MDP_DW_SIMD8</b>					
2.0-2.7	255:0	<p><b>Src0 Green</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW_SIMD8</b></td></tr> </table> <p>Slots[7:0] or [15:8] of Src0 Green</p>	Project:	All	Format:	<b>MDP_DW_SIMD8</b>
Project:	All					
Format:	<b>MDP_DW_SIMD8</b>					
3.0-3.7	255:0	<p><b>Src0 Blue</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW_SIMD8</b></td></tr> </table> <p>Slots[7:0] or [15:8] of Src0 Blue</p>	Project:	All	Format:	<b>MDP_DW_SIMD8</b>
Project:	All					
Format:	<b>MDP_DW_SIMD8</b>					
4.0-4.7	255:0	<p><b>Src0 Alpha</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW_SIMD8</b></td></tr> </table> <p>Slots[7:0] or [15:8] of Src0 Alpha</p>	Project:	All	Format:	<b>MDP_DW_SIMD8</b>
Project:	All					
Format:	<b>MDP_DW_SIMD8</b>					

## MDP\_RTW\_M8DS - OM SIMD8 Dual Source Render Target Data Payload

5.0-5.7	255:0	<b>Src1 Red</b>		
		<table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW SIMD8</b></td></tr> </table> Slots[7:0] or [15:8] of Src1 Red	Project:	All
Project:	All			
Format:	<b>MDP_DW SIMD8</b>			
6.0-6.7	255:0	<b>Src1 Green</b>		
		<table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW SIMD8</b></td></tr> </table> Slots[7:0] or [15:8] of Src1 Green	Project:	All
Project:	All			
Format:	<b>MDP_DW SIMD8</b>			
7.0-7.7	255:0	<b>Src1 Blue</b>		
		<table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW SIMD8</b></td></tr> </table> Slots[7:0] or [15:8] of Src1 Blue	Project:	All
Project:	All			
Format:	<b>MDP_DW SIMD8</b>			
8.0-8.7	255:0	<b>Src1 Alpha</b>		
		<table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW SIMD8</b></td></tr> </table> Slots[7:0] or [15:8] of Src1 Alpha	Project:	All
Project:	All			
Format:	<b>MDP_DW SIMD8</b>			

## OM SIMD8 Render Target Data Payload

<b>MDP_RTW_M8 - OM SIMD8 Render Target Data Payload</b>						
<b>DWord</b>	<b>Bit</b>	<b>Description</b>				
0.0-0.7	255:0	<p><b>oMask</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td><b>MDPR_OMASK</b></td> </tr> </table> <p>Slots [7:0] oMask. Upper half ignored.</p>	Project:	All	Format:	<b>MDPR_OMASK</b>
Project:	All					
Format:	<b>MDPR_OMASK</b>					
1.0-1.7	255:0	<p><b>Red</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td><b>MDP_DW_SIMD8</b></td> </tr> </table> <p>Slots [7:0] Red</p>	Project:	All	Format:	<b>MDP_DW_SIMD8</b>
Project:	All					
Format:	<b>MDP_DW_SIMD8</b>					
2.0-2.7	255:0	<p><b>Green</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td><b>MDP_DW_SIMD8</b></td> </tr> </table> <p>Slots [7:0] Green</p>	Project:	All	Format:	<b>MDP_DW_SIMD8</b>
Project:	All					
Format:	<b>MDP_DW_SIMD8</b>					
3.0-3.7	255:0	<p><b>Blue</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td><b>MDP_DW_SIMD8</b></td> </tr> </table> <p>Slots [7:0] Blue</p>	Project:	All	Format:	<b>MDP_DW_SIMD8</b>
Project:	All					
Format:	<b>MDP_DW_SIMD8</b>					
4.0-4.7	255:0	<p><b>Alpha</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td><b>MDP_DW_SIMD8</b></td> </tr> </table> <p>Slots [7:0] Alpha</p>	Project:	All	Format:	<b>MDP_DW_SIMD8</b>
Project:	All					
Format:	<b>MDP_DW_SIMD8</b>					

## OM SIMD16 Render Target Data Payload

<b>MDP_RTW_M16 - OM SIMD16 Render Target Data Payload</b>						
<b>DWord</b>	<b>Bit</b>	<b>Description</b>				
0.0-0.7	255:0	<b>oMask</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDPR_OMASK</b></td></tr> </table> Slots [15:0] oMask	Project:	All	Format:	<b>MDPR_OMASK</b>
Project:	All					
Format:	<b>MDPR_OMASK</b>					
1.0-1.7	255:0	<b>Red[7:0]</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW SIMD8</b></td></tr> </table> Slots [7:0] Red	Project:	All	Format:	<b>MDP_DW SIMD8</b>
Project:	All					
Format:	<b>MDP_DW SIMD8</b>					
2.0-2.7	255:0	<b>Red[15:8]</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW SIMD8</b></td></tr> </table> Slots [15:8] Red	Project:	All	Format:	<b>MDP_DW SIMD8</b>
Project:	All					
Format:	<b>MDP_DW SIMD8</b>					
3.0-3.7	255:0	<b>Green[7:0]</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW SIMD8</b></td></tr> </table> Slots [7:0] Green	Project:	All	Format:	<b>MDP_DW SIMD8</b>
Project:	All					
Format:	<b>MDP_DW SIMD8</b>					
4.0-4.7	255:0	<b>Green[15:8]</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW SIMD8</b></td></tr> </table> Slots [15:8] Green	Project:	All	Format:	<b>MDP_DW SIMD8</b>
Project:	All					
Format:	<b>MDP_DW SIMD8</b>					

MDP_RTW_M16 - OM SIMD16 Render Target Data Payload							
5.0-5.7	255:0	<b>Blue[7:0]</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW SIMD8</b></td></tr> </table> Slots [7:0] Blue	Project:	All	Format:	<b>MDP_DW SIMD8</b>	
Project:	All						
Format:	<b>MDP_DW SIMD8</b>						
6.0-6.7	255:0	<b>Blue[15:8]</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW SIMD8</b></td></tr> </table> Slots [15:8] Blue	Project:	All	Format:	<b>MDP_DW SIMD8</b>	
Project:	All						
Format:	<b>MDP_DW SIMD8</b>						
7.0-7.7	255:0	<b>Alpha[7:0]</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW SIMD8</b></td></tr> </table> Slots [7:0] Alpha	Project:	All	Format:	<b>MDP_DW SIMD8</b>	
Project:	All						
Format:	<b>MDP_DW SIMD8</b>						
8.0-8.7	255:0	<b>Alpha[15:8]</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW SIMD8</b></td></tr> </table> Slots [15:8] Alpha	Project:	All	Format:	<b>MDP_DW SIMD8</b>	
Project:	All						
Format:	<b>MDP_DW SIMD8</b>						

## Oword 1 Dual Block Data Payload

MDP_OWD1 - Oword 1 Dual Block Data Payload						
DWord	Bit	Description				
0.0-0.3	127:0	<b>Oword Slot0</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U128</td></tr> </table> Specifies the Slot 0 data	Project:	All	Format:	U128
Project:	All					
Format:	U128					
0.4-0.7	127:0	<b>Oword Slot1</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U128</td></tr> </table> Specifies the Slot 1 data	Project:	All	Format:	U128
Project:	All					
Format:	U128					

## Oword 2 Block Data Payload

MDP_OW2 - Oword 2 Block Data Payload						
DWord	Bit	Description				
0.0-0.3	127:0	<p><b>Oword0</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U128</td></tr> </table> <p>Specifies the Oword data for block element 0</p>	Project:	All	Format:	U128
Project:	All					
Format:	U128					
0.4-0.7	127:0	<p><b>Oword1</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U128</td></tr> </table> <p>Specifies the Oword data for block element 1</p>	Project:	All	Format:	U128
Project:	All					
Format:	U128					

## Oword 4 Block Data Payload

MDP_OW4 - Oword 4 Block Data Payload						
DWord	Bit	Description				
0.0-0.7	255:0	<b>Data[1:0]</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDCR_OW</b></td></tr> </table> <p>Specifies the Oword data for block elements [1:0]</p>	Project:	All	Format:	<b>MDCR_OW</b>
Project:	All					
Format:	<b>MDCR_OW</b>					
1.0-1.7	255:0	<b>Data[3:2]</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDCR_OW</b></td></tr> </table> <p>Specifies the Oword data for block elements [3:2]</p>	Project:	All	Format:	<b>MDCR_OW</b>
Project:	All					
Format:	<b>MDCR_OW</b>					

## Oword 4 Dual Block Data Payload

MDP_OWD4 - Oword 4 Dual Block Data Payload						
DWord	Bit	Description				
0.0-0.3	127:0	<p><b>Oword0 Slot0</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U128</td></tr> </table> <p>Specifies the Slot 0 data for block element 0</p>	Project:	All	Format:	U128
Project:	All					
Format:	U128					
0.4-0.7	127:0	<p><b>Oword0 Slot1</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U128</td></tr> </table> <p>Specifies the Slot 1 data for block element 0</p>	Project:	All	Format:	U128
Project:	All					
Format:	U128					
1.0-1.3	127:0	<p><b>Oword1 Slot0</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U128</td></tr> </table> <p>Specifies the Slot 0 data for block element 1</p>	Project:	All	Format:	U128
Project:	All					
Format:	U128					
1.4-1.7	127:0	<p><b>Oword1 Slot1</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U128</td></tr> </table> <p>Specifies the Slot 1 data for block element 1</p>	Project:	All	Format:	U128
Project:	All					
Format:	U128					
2.0-2.3	127:0	<p><b>Oword2 Slot0</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U128</td></tr> </table> <p>Specifies the Slot 0 data for block element 2</p>	Project:	All	Format:	U128
Project:	All					
Format:	U128					
2.4-2.7	127:0	<p><b>Oword2 Slot1</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U128</td></tr> </table> <p>Specifies the Slot 1 data for block element 2</p>	Project:	All	Format:	U128
Project:	All					
Format:	U128					

<b>MDP_OWD4 - Oword 4 Dual Block Data Payload</b>						
3.0-3.3	127:0	<b>Oword3 Slot0</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U128</td></tr> </table> <p>Specifies the Slot 0 data for block element 3</p>	Project:	All	Format:	U128
Project:	All					
Format:	U128					
3.4-3.7	127:0	<b>Oword3 Slot1</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U128</td></tr> </table> <p>Specifies the Slot 1 data for block element 3</p>	Project:	All	Format:	U128
Project:	All					
Format:	U128					

## Oword 8 Block Data Payload

MDP_OW8 - Oword 8 Block Data Payload						
DWord	Bit	Description				
0.0-0.7	255:0	<p><b>Data[1:0]</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDCR_OW</b></td></tr> </table> <p>Specifies the Oword data for block elements [1:0]</p>	Project:	All	Format:	<b>MDCR_OW</b>
Project:	All					
Format:	<b>MDCR_OW</b>					
1.0-1.7	255:0	<p><b>Data[3:2]</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDCR_OW</b></td></tr> </table> <p>Specifies the Oword data for block elements [3:2]</p>	Project:	All	Format:	<b>MDCR_OW</b>
Project:	All					
Format:	<b>MDCR_OW</b>					
2.0-2.7	255:0	<p><b>Data[5:4]</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDCR_OW</b></td></tr> </table> <p>Specifies the Oword data for block elements [5:4]</p>	Project:	All	Format:	<b>MDCR_OW</b>
Project:	All					
Format:	<b>MDCR_OW</b>					
3.0-3.7	255:0	<p><b>Data[7:6]</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDCR_OW</b></td></tr> </table> <p>Specifies the Oword data for block elements [7:6]</p>	Project:	All	Format:	<b>MDCR_OW</b>
Project:	All					
Format:	<b>MDCR_OW</b>					

## Oword A64 SIMD4x2 Atomic CMPWR16B Message Data Payload

<b>MDP_A64_AOP4X2_OW2 - Oword A64 SIMD4x2 Atomic CMPWR16B Message Data Payload</b>				
<b>DWord</b>	<b>Bit</b>	<b>Description</b>		
0.0-0.3	127:0	<p><b>Src0 Slot0</b></p> <table border="1"> <tr> <td>Format:</td> <td>U128</td> </tr> </table> <p>Specifies the Slot 0 Source 0 data</p>	Format:	U128
Format:	U128			
0.4-0.7	127:0	<p><b>Src0 Slot1</b></p> <table border="1"> <tr> <td>Format:</td> <td>U128</td> </tr> </table> <p>Specifies the Slot 1 Source 0 data</p>	Format:	U128
Format:	U128			
1.0-1.3	127:0	<p><b>Src1 Slot0</b></p> <table border="1"> <tr> <td>Format:</td> <td>U128</td> </tr> </table> <p>Specifies the Slot 0 Source 1 data</p>	Format:	U128
Format:	U128			
1.4-1.7	127:0	<p><b>Src1 Slot1</b></p> <table border="1"> <tr> <td>Format:</td> <td>U128</td> </tr> </table> <p>Specifies the Slot 1 Source 1 data</p>	Format:	U128
Format:	U128			

## Oword A64 SIMD4x2 Atomic Operation Return Data Message Data Payload

<b>MDP_A64_AOP4X2_OW1 - Oword A64 SIMD4x2 Atomic Operation Return Data Message Data Payload</b>				
<b>DWord</b>	<b>Bit</b>	<b>Description</b>		
0.0-0.3	127:0	<p><b>Oword0</b></p> <table border="1"> <tr> <td>Format:</td> <td>U128</td> </tr> </table> <p>Specifies the Slot 0 Return data</p>	Format:	U128
Format:	U128			
0.4-0.7	127:0	<p><b>Oword1</b></p> <table border="1"> <tr> <td>Format:</td> <td>U128</td> </tr> </table> <p>Specifies the Slot1 Return data</p>	Format:	U128
Format:	U128			

## Oword A64 SIMD8 Atomic Operation CMPWR16B Message Data Payload

<b>MDP_A64_AOP8_OW2 - Oword A64 SIMD8 Atomic Operation CMPWR16B Message Data Payload</b>						
<b>DWord</b>	<b>Bit</b>	<b>Description</b>				
0.0-0.7	255:0	<p><b>Slot[1:0] Src0</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDCR_OW</b></td></tr> </table> <p>Specifies the Slot [1:0] Source 0 data</p>	Project:	All	Format:	<b>MDCR_OW</b>
Project:	All					
Format:	<b>MDCR_OW</b>					
1.0-1.7	255:0	<p><b>Slot[3:2] Src0</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDCR_OW</b></td></tr> </table> <p>Specifies the Slot [3:2] Source 0 data</p>	Project:	All	Format:	<b>MDCR_OW</b>
Project:	All					
Format:	<b>MDCR_OW</b>					
2.0-2.7	255:0	<p><b>Slot[5:4] Src0</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDCR_OW</b></td></tr> </table> <p>Specifies the Slot [5:4] Source 0 data</p>	Project:	All	Format:	<b>MDCR_OW</b>
Project:	All					
Format:	<b>MDCR_OW</b>					
3.0-3.7	255:0	<p><b>Slot[7:6] Src0</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDCR_OW</b></td></tr> </table> <p>Specifies the Slot [7:6] Source 0 data</p>	Project:	All	Format:	<b>MDCR_OW</b>
Project:	All					
Format:	<b>MDCR_OW</b>					
4.0-4.7	255:0	<p><b>Slot[1:0] Src1</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDCR_OW</b></td></tr> </table> <p>Specifies the Slot [1:0] Source 1 data</p>	Project:	All	Format:	<b>MDCR_OW</b>
Project:	All					
Format:	<b>MDCR_OW</b>					

## **MDP\_A64\_AOP8\_OW2 - Oword A64 SIMD8 Atomic Operation CMPWR16B Message Data Payload**

5.0-5.7	255:0	<p><b>Slot[3:2] Src1</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDCR_OW</b></td></tr> </table> <p>Specifies the Slot [3:2] Source 1 data</p>	Project:	All	Format:	<b>MDCR_OW</b>
Project:	All					
Format:	<b>MDCR_OW</b>					
6.0-6.7	255:0	<p><b>Slot[5:4] Src1</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDCR_OW</b></td></tr> </table> <p>Specifies the Slot [5:4] Source 1 data</p>	Project:	All	Format:	<b>MDCR_OW</b>
Project:	All					
Format:	<b>MDCR_OW</b>					
7.0-7.7	255:0	<p><b>Slot[7:6] Src1</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDCR_OW</b></td></tr> </table> <p>Specifies the Slot [7:6] Source 1 data</p>	Project:	All	Format:	<b>MDCR_OW</b>
Project:	All					
Format:	<b>MDCR_OW</b>					

## Oword Data Blocks Message Descriptor Control Field

<b>MDC_DB_OW - Oword Data Blocks Message Descriptor Control Field</b>																											
<b>DWord</b>	<b>Bit</b>	<b>Description</b>																									
0	2:0	<b>Data Blocks</b> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Enumeration</td> </tr> </table> <p>Specifies the number of Oword blocks to be read or written</p> <table border="1"> <thead> <tr> <th><b>Value</b></th> <th><b>Name</b></th> <th><b>Description</b></th> </tr> </thead> <tbody> <tr> <td>00h</td> <td>OW1L</td> <td>1 Oword, read into or written from the low 128 bits of the destination register</td> </tr> <tr> <td>01h</td> <td>OW1U</td> <td>1 Oword, read into or written from the high 128 bits of the destination register</td> </tr> <tr> <td>02h</td> <td>OW2</td> <td>2 Owords</td> </tr> <tr> <td>03h</td> <td>OW4</td> <td>4 Owords</td> </tr> <tr> <td>04h</td> <td>OW8</td> <td>8 Owords</td> </tr> <tr> <td>Others</td> <td>Reserved</td> <td>Ignored</td> </tr> </tbody> </table>	Project:	All	Format:	Enumeration	<b>Value</b>	<b>Name</b>	<b>Description</b>	00h	OW1L	1 Oword, read into or written from the low 128 bits of the destination register	01h	OW1U	1 Oword, read into or written from the high 128 bits of the destination register	02h	OW2	2 Owords	03h	OW4	4 Owords	04h	OW8	8 Owords	Others	Reserved	Ignored
Project:	All																										
Format:	Enumeration																										
<b>Value</b>	<b>Name</b>	<b>Description</b>																									
00h	OW1L	1 Oword, read into or written from the low 128 bits of the destination register																									
01h	OW1U	1 Oword, read into or written from the high 128 bits of the destination register																									
02h	OW2	2 Owords																									
03h	OW4	4 Owords																									
04h	OW8	8 Owords																									
Others	Reserved	Ignored																									

## Oword Data Payload Register

MDCR_OW - Oword Data Payload Register						
DWord	Bit	Description				
0.0-0.3	127:0	<p><b>Oword0</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U128</td></tr> </table> <p>Specifies the slot 0 data in this payload register</p>	Project:	All	Format:	U128
Project:	All					
Format:	U128					
0.4-0.7	127:0	<p><b>Oword1</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U128</td></tr> </table> <p>Specifies the slot 1 data in this payload register</p>	Project:	All	Format:	U128
Project:	All					
Format:	U128					

## Oword Dual Data Blocks Message Descriptor Control Field

<b>MDC_DB_OWD - Oword Dual Data Blocks Message Descriptor Control Field</b>																				
Project: BDW Size (in bits): 2 Default Value: 0x00000000																				
DWord	Bit	Description																		
0	1:0	<b>OW Dual Data Blocks</b> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Enumeration</td> </tr> <tr> <td colspan="2">Specifies the number of Oword Blocks to be read or written</td></tr> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> <tr> <td>00h</td><td>OWD1</td><td>1 Hword register, 2 Owords</td></tr> <tr> <td>02h</td><td>OWD4</td><td>4 Hword registers, 8 Owords</td></tr> <tr> <td>Others</td><td>Reserved</td><td>Ignored</td></tr> </table>	Project:	All	Format:	Enumeration	Specifies the number of Oword Blocks to be read or written		Value	Name	Description	00h	OWD1	1 Hword register, 2 Owords	02h	OWD4	4 Hword registers, 8 Owords	Others	Reserved	Ignored
Project:	All																			
Format:	Enumeration																			
Specifies the number of Oword Blocks to be read or written																				
Value	Name	Description																		
00h	OWD1	1 Hword register, 2 Owords																		
02h	OWD4	4 Hword registers, 8 Owords																		
Others	Reserved	Ignored																		

## PALETTE\_ENTRY

PALETTE_ENTRY				
DWord	Bit	Description		
0	31:24	<p><b>Alpha</b></p> <table border="1"> <tr> <td>Format:</td> <td>U8</td> </tr> </table> <p>Alpha channel value for this entry in the texture color palette.</p>	Format:	U8
Format:	U8			
23:16	<p><b>Red</b></p> <table border="1"> <tr> <td>Format:</td> <td>U8</td> </tr> </table> <p>Red channel value for this entry in the texture color palette.</p>	Format:	U8	
Format:	U8			
15:8	<p><b>Green</b></p> <table border="1"> <tr> <td>Format:</td> <td>U8</td> </tr> </table> <p>Green channel value for this entry in the texture color palette.</p>	Format:	U8	
Format:	U8			
7:0	<p><b>Blue</b></p> <table border="1"> <tr> <td>Format:</td> <td>U8</td> </tr> </table> <p>Blue channel value for this entry in the texture color palette.</p>	Format:	U8	
Format:	U8			

## Performance Counter Report Format 101b

Performance Counter Report Format 101b		
DWord	Bit	Description
0	31:0	<b>RPT_ID</b>
1	31:0	<b>TIME_STAMP</b>
2	31:0	<b>CTX_ID</b>
3	31:0	<b>GPU_TICKS</b>
4	31:0	<b>A-Cntr 0 (low dword)</b>
5	31:0	<b>A-Cntr 1 (low dword)</b>
6	31:0	<b>A-Cntr 2 (low dword)</b>
7	31:0	<b>A-Cntr 3 (low dword)</b>
8	31:0	<b>A-Cntr 4 (low dword)</b>
9	31:0	<b>A-Cntr 5 (low dword)</b>
10	31:0	<b>A-Cntr 6 (low dword)</b>
11	31:0	<b>A-Cntr 7 (low dword)</b>
12	31:0	<b>A-Cntr 8 (low dword)</b>
13	31:0	<b>A-Cntr 9 (low dword)</b>
14	31:0	<b>A-Cntr 10 (low dword)</b>
15	31:0	<b>A-Cntr 11 (low dword)</b>
16	31:0	<b>A-Cntr 12 (low dword)</b>
17	31:0	<b>A-Cntr 13 (low dword)</b>
18	31:0	<b>A-Cntr 14 (low dword)</b>
19	31:0	<b>A-Cntr 15 (low dword)</b>
20	31:0	<b>A-Cntr 16 (low dword)</b>
21	31:0	<b>A-Cntr 17 (low dword)</b>

Performance Counter Report Format 101b		
22	31:0	<b>A-Cntr 18 (low dword)</b>
23	31:0	<b>A-Cntr 19 (low dword)</b>
24	31:0	<b>A-Cntr 20 (low dword)</b>
25	31:0	<b>A-Cntr 21 (low dword)</b>
26	31:0	<b>A-Cntr 22 (low dword)</b>
27	31:0	<b>A-Cntr 23 (low dword)</b>
28	31:0	<b>A-Cntr 24 (low dword)</b>
29	31:0	<b>A-Cntr 25 (low dword)</b>
30	31:0	<b>A-Cntr 26 (low dword)</b>
31	31:0	<b>A-Cntr 27 (low dword)</b>
32	31:0	<b>A-Cntr 28 (low dword)</b>
33	31:0	<b>A-Cntr 29 (low dword)</b>
34	31:0	<b>A-Cntr 30 (low dword)</b>
35	31:0	<b>A-Cntr 31 (low dword)</b>
36	31:0	<b>A-Cntr 32 (low dword)</b>
37	31:0	<b>A-Cntr 33 (low dword)</b>
38	31:0	<b>A-Cntr 34 (low dword)</b>
39	31:0	<b>A-Cntr 35 (low dword)</b>
40	31:24	<b>High byte of A3</b>
	23:16	<b>High byte of A2</b>
	15:8	<b>High byte of A1</b>
	7:0	<b>High byte of A0</b>
41	31:24	<b>High byte of A7</b>
	23:16	<b>High byte of A6</b>
	15:8	<b>High byte of A5</b>
	7:0	<b>High byte of A4</b>
42	31:24	<b>High byte of A11</b>
	23:16	<b>High byte of A10</b>
	15:8	<b>High byte of A9</b>
	7:0	<b>High byte of A8</b>
43	31:24	<b>High byte of A15</b>
	23:16	<b>High byte of A14</b>
	15:8	<b>High byte of A13</b>
	7:0	<b>High byte of A12</b>
44	31:24	<b>High byte of A19</b>
	23:16	<b>High byte of A18</b>

Performance Counter Report Format 101b		
	15:8	<b>High byte of A17</b>
	7:0	<b>High byte of A16</b>
45	31:24	<b>High byte of A23</b>
	23:16	<b>High byte of A22</b>
	15:8	<b>High byte of A21</b>
	7:0	<b>High byte of A20</b>
46	31:24	<b>High byte of A27</b>
	23:16	<b>High byte of A26</b>
	15:8	<b>High byte of A25</b>
	7:0	<b>High byte of A24</b>
47	31:24	<b>High byte of A31</b>
	23:16	<b>High byte of A30</b>
	15:8	<b>High byte of A29</b>
	7:0	<b>High byte of A28</b>
48	31:0	<b>B-Cntr 0</b>
49	31:0	<b>B-Cntr 1</b>
50	31:0	<b>B-Cntr 2</b>
51	31:0	<b>B-Cntr 3</b>
52	31:0	<b>B-Cntr 4</b>
53	31:0	<b>B-Cntr 5</b>
54	31:0	<b>B-Cntr 6</b>
55	31:0	<b>B-Cntr 7</b>
56	31:0	<b>C-Cntr 0</b>
57	31:0	<b>C-Cntr 1</b>
58	31:0	<b>C-Cntr 2</b>
59	31:0	<b>C-Cntr 3</b>
60	31:0	<b>C-Cntr 4</b>
61	31:0	<b>C-Cntr 5</b>
62	31:0	<b>C-Cntr 6</b>
63	31:0	<b>C-Cntr 7</b>

## Per Thread Scratch Space Message Header Control

MHC_PTSS - Per Thread Scratch Space Message Header Control						
DWord	Bit	Description				
0	31:4	<b>Reserved</b>				
		<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Ignore</td> </tr> <tr> <td colspan="2">Ignored</td></tr> </table>	Project:	All	Format:	Ignore
Project:	All					
Format:	Ignore					
Ignored						
	3:0	<b>Per Thread Scratch Space</b>				
		<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U4</td> </tr> </table> <p>Specifies the amount of scratch space allowed to be used by this thread for messages in which the Binding Table Index is Stateless model, otherwise this field is ignored. The data port will use this to bounds check scratch space messages. Value range = [0,11] represents [1KB, 2MB] in powers of two.</p>	Project:	All	Format:	U4
Project:	All					
Format:	U4					
<b>Programming Notes</b>						
Writes out of bounds will be ignored. Reads out of bounds will return 0.						

## Pixel Masked Media Block Message Header

<b>MH_MBPM - Pixel Masked Media Block Message Header</b>						
<b>DWord</b>	<b>Bit</b>	<b>Description</b>				
0	31:0	<p><b>X Offset</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>S31</td> </tr> </table> <p>X offset (in bytes) of the upper left corner of the block into the surface.</p> <p><b>Programming Notes</b></p> <p>When Message Mode is set to PIXEL_MASK, this field must be a multiple of 32.</p>	Project:	All	Format:	S31
Project:	All					
Format:	S31					
1	31:0	<p><b>Y Offset</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>S31</td> </tr> </table> <p>Y offset (in rows) of the upper left corner of the block into the surface.</p> <p><b>Programming Notes</b></p> <p>When Message Mode is set to PIXEL_MASK, this field must be a multiple of 4.</p>	Project:	All	Format:	S31
Project:	All					
Format:	S31					
2	31:0	<p><b>Media Block Message Control</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td><b>MHC_MBPM_CONTROL</b></td> </tr> </table> <p>Specifies the message subtype is Pixel Masked.</p>	Project:	All	Format:	<b>MHC_MBPM_CONTROL</b>
Project:	All					
Format:	<b>MHC_MBPM_CONTROL</b>					
3	31:0	<p><b>Pixel Mask</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U32</td> </tr> </table> <p>Specifies the Pixel Mask for writes when Message Mode field is PIXEL_MASK.</p> <p><b>Programming Notes</b></p> <p>The Pixel Mask applies to the 2x2 square tiles (UL, UR, LL, LR), which themselves tiled (UL, UR, LL, LR) and then repeated on the right for the remaining 16-bits to cover a 4 row 8 column area.</p>	Project:	All	Format:	U32
Project:	All					
Format:	U32					
4	31:0	<p><b>FFTID</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td><b>MHC_FFTID</b></td> </tr> </table> <p>Fixed Function Thread ID</p>	Project:	All	Format:	<b>MHC_FFTID</b>
Project:	All					
Format:	<b>MHC_FFTID</b>					

## MH\_MBPM - Pixel Masked Media Block Message Header

5-7	95:0	<b>Reserved</b>
		Project:
		Format:
		Ignored

## Pixel Masked Media Block Message Header Control

<b>MHC_MBPM_CONTROL - Pixel Masked Media Block Message Header Control</b>															
<b>DWord</b>	<b>Bit</b>	<b>Description</b>													
0	31:30	<p><b>Message Mode</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Enumeration</td> </tr> </table> <p>Specifies the Media Block Write Message subtype is Pixel Masked.</p> <table border="1"> <thead> <tr> <th><b>Value</b></th> <th><b>Name</b></th> <th><b>Description</b></th> </tr> </thead> <tbody> <tr> <td>01h</td> <td>PIXEL_MASK</td> <td>Use the Pixel Mask in the Message Header. The Block Height and Block Width are ignored and behave as if they are set to 4 rows and 32 bytes, respectively.</td> </tr> <tr> <td>Others</td> <td>Reserved</td> <td>Reserved.</td> </tr> </tbody> </table>	Project:	All	Format:	Enumeration	<b>Value</b>	<b>Name</b>	<b>Description</b>	01h	PIXEL_MASK	Use the Pixel Mask in the Message Header. The Block Height and Block Width are ignored and behave as if they are set to 4 rows and 32 bytes, respectively.	Others	Reserved	Reserved.
Project:	All														
Format:	Enumeration														
<b>Value</b>	<b>Name</b>	<b>Description</b>													
01h	PIXEL_MASK	Use the Pixel Mask in the Message Header. The Block Height and Block Width are ignored and behave as if they are set to 4 rows and 32 bytes, respectively.													
Others	Reserved	Reserved.													
	29	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Ignore</td> </tr> </table> <p>Ignored</p>	Project:	All	Format:	Ignore									
Project:	All														
Format:	Ignore														
	28:24	<p><b>Sub-Register Offset</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U5</td> </tr> </table> <p>This field is ignored (reserved) for a media block write message.</p>	Project:	All	Format:	U5									
Project:	All														
Format:	U5														
	23:22	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Ignore</td> </tr> </table> <p>Ignored</p>	Project:	All	Format:	Ignore									
Project:	All														
Format:	Ignore														
	21:16	<p><b>Block Height</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U6</td> </tr> </table> <p>This field is ignored (reserved) for a Pixel Masked media block write message.</p>	Project:	All	Format:	U6									
Project:	All														
Format:	U6														

## MHC\_MBPM\_CONTROL - Pixel Masked Media Block Message Header Control

	15:10	<b>Reserved</b>				
		<table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>Ignore</td></tr> </table> <p>Ignored</p>	Project:	All	Format:	Ignore
Project:	All					
Format:	Ignore					
	9:8	<b>Register Pitch Control</b>				
		<table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U2</td></tr> </table> <p>This field is ignored (reserved) for a media block write message.</p>	Project:	All	Format:	U2
Project:	All					
Format:	U2					
	7:6	<b>Reserved</b>				
		<table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>Ignore</td></tr> </table> <p>Ignored</p>	Project:	All	Format:	Ignore
Project:	All					
Format:	Ignore					
	5:0	<b>Block Width</b>				
		<table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U6</td></tr> </table> <p>This field is ignored (reserved) for a Pixel Masked media block write message.</p>	Project:	All	Format:	U6
Project:	All					
Format:	U6					

## Pixel Sample Mask Message Header Control

<b>MHC_PSM - Pixel Sample Mask Message Header Control</b>						
<b>DWord</b>	<b>Bit</b>	<b>Description</b>				
0	31:16	<b>Reserved</b> <table border="1"> <tr> <td>Format:</td> <td>Ignore</td> </tr> <tr> <td colspan="2">Ignored</td></tr> </table>	Format:	Ignore	Ignored	
Format:	Ignore					
Ignored						
15:0	<b>Pixel Sample Mask</b> <table border="1"> <tr> <td>Default Value:</td> <td>0FFFFh Default</td> </tr> <tr> <td>Format:</td> <td>U16</td> </tr> </table> <p>SIMD16 and SIMD8 messages. All 16 bits are used for SIMD16. For untyped SIMD8 messages, the low 8 bits of field are used. If the header is not delivered, this field defaults to all ones. This field is ignored for SIMD4x2 messages.</p>	Default Value:	0FFFFh Default	Format:	U16	
Default Value:	0FFFFh Default					
Format:	U16					

## Pixel Sample Mask Render Target Message Header Control

<b>MHC_RT_PSM - Pixel Sample Mask Render Target Message Header Control</b>						
<b>DWord</b>	<b>Bit</b>	<b>Description</b>				
0	31:16	<p><b>Dispatched Pixel/Sample Enables</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U16</td> </tr> </table> <p>One bit per pixel (or sample within pixel) indicating which pixels/samples were originally enabled when the thread was dispatched. The Dispatched Pixel/Sample Enables must be unmodified from the ones sent when the pixel shader thread was initiated. If the Dispatched Pixel/Sample Enables are modified, behavior is undefined.</p> <p><b>Programming Notes</b></p> <p>When operating in PER_SAMPLE mode these bits correspond to samples, not pixels. Each subspan slot (4 bits) corresponds to a specific sample location for the subspan. Note that in NUMSAMPLES_1 mode, a pixel and sample are synonymous. When operating in PER_PIXEL mode, this field is ignored, and instead the SampleEnableMask (obtained via bypass) are used to clear the Depth Scoreboard.</p>	Project:	All	Format:	U16
Project:	All					
Format:	U16					
	15:0	<p><b>Pixel/Sample Enables</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U16</td> </tr> </table> <p>Specifies which pixels/samples are still lit based on kill instruction activity in the pixel shader. This mask is AND'd with the Dispatched Pixel/Sample Enables mask, and that is used to control actual accesses to the color buffer. Pixels/samples will be dropped on masked writes, and the GRF is not modified for masked reads.</p> <p><b>Programming Notes</b></p> <p>When operating in PER_SAMPLE mode these bits correspond to samples, not pixels, as the PS is run per-sample. Each subspan slot (4 bits) corresponds to a specific sample location for the subspan. When operating in PER_PIXEL mode, these bits still correspond to pixels, as the PS is run per-pixel. Each pixel's mask bit is replicated according to Number of Multisamples and combined with other masks to control writes to the multisample locations.</p>	Project:	All	Format:	U16
Project:	All					
Format:	U16					

## Power Clock State Format

Power Clock State Format																											
DWord	Bit	Description																									
0 <b>Project:</b> BDW	30:19	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	BDW	Access:	RO	Format:	MBZ																			
Project:	BDW																										
Access:	RO																										
Format:	MBZ																										
	18	<p><b>Enable Slice Count Request</b></p> <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Enable Slice Count Request. This field is for Broadwell.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Disable</td> <td>Use async PMunit slice count request.</td> </tr> <tr> <td>1h</td> <td>Enable</td> <td>Use SliceCount from this register.</td> </tr> </tbody> </table>	Project:	BDW	Access:	R/W	Value	Name	Description	0h	Disable	Use async PMunit slice count request.	1h	Enable	Use SliceCount from this register.												
Project:	BDW																										
Access:	R/W																										
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1h	Enable	Use SliceCount from this register.																									
	17:15	<p><b>Slice Count Request</b></p> <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Slice Count Request. This field is for Broadwell.</p> <p>This is further limited to the number of slices in a given SKU</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>001b</td> <td></td> <td>1 slice.</td> </tr> <tr> <td>010b</td> <td></td> <td>2 slices.</td> </tr> <tr> <td>011b</td> <td></td> <td>3 slices.</td> </tr> <tr> <td>100b</td> <td></td> <td>4 slices.</td> </tr> <tr> <td>101b</td> <td></td> <td>5 slices. Hardware will revert to 4 slices</td> </tr> <tr> <td>110b</td> <td></td> <td>6 slices.</td> </tr> </tbody> </table>	Project:	BDW	Access:	R/W	Value	Name	Description	001b		1 slice.	010b		2 slices.	011b		3 slices.	100b		4 slices.	101b		5 slices. Hardware will revert to 4 slices	110b		6 slices.
Project:	BDW																										
Access:	R/W																										
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Power Clock State Format															
	8	<p><b>NON-SLM Indication</b></p> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Non-SLM Indication.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0h</td><td></td><td>Workload may use SLM, requiring higher Vmin.</td></tr> <tr> <td>1h</td><td></td><td>Workload must not use SLM, allowing lower Vmin</td></tr> </tbody> </table>	Project:	BDW	Access:	R/W	Value	Name	Description	0h		Workload may use SLM, requiring higher Vmin.	1h		Workload must not use SLM, allowing lower Vmin
Project:	BDW														
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Value	Name	Description													
0h		Workload may use SLM, requiring higher Vmin.													
1h		Workload must not use SLM, allowing lower Vmin													
	7:0	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>RO</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	BDW	Access:	RO	Format:	MBZ							
Project:	BDW														
Access:	RO														
Format:	MBZ														

## PPHWSP\_LAYOUT

PPHWSP_LAYOUT - PPHWSP_LAYOUT		
DWord	Bit	Description
0..3	31:0	<b>Reserved</b>
4	31:0	<b>Ring Head Pointer Storage</b> The contents of the Ring Buffer Head Pointer register (register DWord 1) are written to this location either as result of an MI_REPORT_HEAD instruction or as the result of an "automatic report" (see RINGBUF registers).
5..15	31:0	<b>Reserved</b>
16	0	<b>Cumulative Context Run Time</b> This has the cumulative run time of the context on HW. HW reports CTX_TIMESTAMP to this location on a context switch.
17	31:1	<b>Reserved</b>
	0	<b>Reserved</b> Project: BDW
18..19	63:0	<b>Preempt Request Received Timestamp</b> TIMESTAMP register sampled on preemption request is reported.
20..21	63:0	<b>Context Restore Complete Timestamp</b> TIMESTAMP register sampled on context restore complete is reported.
22..23	63:0	<b>Context Save Finished Timestamp</b> TIMESTAMP register sampled on context save completion is reported.
24..27	127:0	<b>MI_SEMAPHORE_WAIT</b> MI_SEMAPHORE_WAIT command on which the context got switched out due to semaphore wait. This field is only valid and must be looked at when the context switch reason in context status buffer is stated as "Wait on Semaphore".
28..31	127:0	<b>Reserved</b>
<b>Project:</b> BDW	63:0	<b>Reserved</b> Project: BDW
	31:0	<b>Reserved</b>

## Qword A64 SIMD4x2 Atomic CMPWR Message Data Payload

MDP_A64_AOP4X2_QW2 - Qword A64 SIMD4x2 Atomic CMPWR Message Data Payload				
DWord	Bit	Description		
0.0-0.1	63:0	<p><b>Src0 Slot0</b></p> <table border="1"> <tr> <td>Format:</td> <td>U64</td> </tr> </table> <p>Specifies the Slot 0 Source 0 data</p>	Format:	U64
Format:	U64			
0.2-0.3	63:0	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>Ignore</td> </tr> </table> <p>Ignored</p>	Format:	Ignore
Format:	Ignore			
0.4-0.5	63:0	<p><b>Src0 Slot1</b></p> <table border="1"> <tr> <td>Format:</td> <td>U64</td> </tr> </table> <p>Specifies the Slot 1 Source 0 data</p>	Format:	U64
Format:	U64			
0.6-0.7	63:0	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>Ignore</td> </tr> </table> <p>Ignored</p>	Format:	Ignore
Format:	Ignore			
1.0-1.1	63:0	<p><b>Src1 Slot0</b></p> <table border="1"> <tr> <td>Format:</td> <td>U64</td> </tr> </table> <p>Specifies the Slot 0 Source 1 data</p>	Format:	U64
Format:	U64			
1.2-1.3	63:0	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>Ignore</td> </tr> </table> <p>Ignored</p>	Format:	Ignore
Format:	Ignore			
1.4-1.5	63:0	<p><b>Src1 Slot1</b></p> <table border="1"> <tr> <td>Format:</td> <td>U64</td> </tr> </table> <p>Specifies the Slot 1 Source 1 data</p>	Format:	U64
Format:	U64			

## MDP\_A64\_AOP4X2\_QW2 - Qword A64 SIMD4x2 Atomic CMPWR Message Data Payload

1.6-1.7	63:0	<b>Reserved</b>
		Format: <input type="text"/> Ignore
		Ignored

## Qword Data Payload Register

MDCR_QW - Qword Data Payload Register						
DWord	Bit	Description				
0.0-0.1	63:0	<p><b>Qword0</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U64</td></tr> </table> <p>Specifies the slot 0 data in this payload register</p>	Project:	All	Format:	U64
Project:	All					
Format:	U64					
0.2-0.3	63:0	<p><b>Qword1</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U64</td></tr> </table> <p>Specifies the slot 1 data in this payload register</p>	Project:	All	Format:	U64
Project:	All					
Format:	U64					
0.4-0.5	63:0	<p><b>Qword2</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U64</td></tr> </table> <p>Specifies the slot 2 data in this payload register</p>	Project:	All	Format:	U64
Project:	All					
Format:	U64					
0.6-0.7	63:0	<p><b>Qword3</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U64</td></tr> </table> <p>Specifies the slot 3 data in this payload register</p>	Project:	All	Format:	U64
Project:	All					
Format:	U64					

## Qword SIMD4x2 Atomic CMPWR8B Message Data Payload

<b>MDP_AOP4X2_QW2 - Qword SIMD4x2 Atomic CMPWR8B Message Data Payload</b>				
<b>DWord</b>	<b>Bit</b>	<b>Description</b>		
0-1	63:0	<p><b>Src0 Slot0</b></p> <table border="1"> <tr> <td>Format:</td> <td>U64</td> </tr> </table> <p>Specifies the Slot 0 Source 0 data</p>	Format:	U64
Format:	U64			
2-3	63:0	<p><b>Src1 Slot0</b></p> <table border="1"> <tr> <td>Format:</td> <td>U64</td> </tr> </table> <p>Specifies the Slot 0 Source 1 data</p>	Format:	U64
Format:	U64			
4-5	63:0	<p><b>Src0 Slot1</b></p> <table border="1"> <tr> <td>Format:</td> <td>U64</td> </tr> </table> <p>Specifies the Slot 1 Source 0 data</p>	Format:	U64
Format:	U64			
6-7	63:0	<p><b>Src1 Slot1</b></p> <table border="1"> <tr> <td>Format:</td> <td>U64</td> </tr> </table> <p>Specifies the Slot 1 Source 1 data</p>	Format:	U64
Format:	U64			

## Qword SIMD4x2 Atomic Operation Message Data Payload

<b>MDP_AOP4X2_QW1 - Qword SIMD4x2 Atomic Operation Message Data Payload</b>				
<b>DWord</b>	<b>Bit</b>	<b>Description</b>		
0-1	63:0	<p><b>Qword0</b></p> <table border="1"> <tr> <td>Format:</td> <td>U64 S63</td> </tr> </table> <p>Specifies the Slot 0 Source or Return data</p>	Format:	U64 S63
Format:	U64 S63			
2-3	63:0	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>Ignore</td> </tr> </table> <p>Ignored</p>	Format:	Ignore
Format:	Ignore			
4-5	63:0	<p><b>Qword1</b></p> <table border="1"> <tr> <td>Format:</td> <td>U64 S63</td> </tr> </table> <p>Specifies the Slot 1 Source or Return data</p>	Format:	U64 S63
Format:	U64 S63			
6-7	63:0	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>Ignore</td> </tr> </table> <p>Ignored</p>	Format:	Ignore
Format:	Ignore			

## Qword SIMD8 Atomic Operation CMPWR8B Message Data Payload

<b>MDP_AOP8_QW2 - Qword SIMD8 Atomic Operation CMPWR8B Message Data Payload</b>						
<b>DWord</b>	<b>Bit</b>	<b>Description</b>				
0.0-0.7	255:0	<p><b>Slot[7:0] Src0[31:0]</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td><b>MDCR_DW</b></td> </tr> </table> <p>Specifies the lower 32-bits of Slot [7:0] Source 0 data</p>	Project:	All	Format:	<b>MDCR_DW</b>
Project:	All					
Format:	<b>MDCR_DW</b>					
1.0-1.7	255:0	<p><b>Slot[7:0] Src0[63:32]</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td><b>MDCR_DW</b></td> </tr> </table> <p>Specifies the upper 32-bits of Slot [7:0] Source 0 data</p>	Project:	All	Format:	<b>MDCR_DW</b>
Project:	All					
Format:	<b>MDCR_DW</b>					
2.0-2.7	255:0	<p><b>Slot[7:0] Src1[31:0]</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td><b>MDCR_DW</b></td> </tr> </table> <p>Specifies the lower 32-bits of Slot [7:0] Source 1 data</p>	Project:	All	Format:	<b>MDCR_DW</b>
Project:	All					
Format:	<b>MDCR_DW</b>					
3.0-3.7	255:0	<p><b>Slot[7:0] Src1[63:32]</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td><b>MDCR_DW</b></td> </tr> </table> <p>Specifies the upper 32-bits of Slot [7:0] Source 1 data</p>	Project:	All	Format:	<b>MDCR_DW</b>
Project:	All					
Format:	<b>MDCR_DW</b>					

## Qword SIMD8 Atomic Operation CMPWR Message Data Payload

<b>MDP_A64_AOP8_QW2 - Qword SIMD8 Atomic Operation CMPWR Message Data Payload</b>						
<b>DWord</b>	<b>Bit</b>	<b>Description</b>				
0.0-0.7	255:0	<p><b>Slot[3:0] Src0</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td><b>MDCR_QW</b></td> </tr> </table> <p>Specifies the Slot [3:0] Source 0 data</p>	Project:	All	Format:	<b>MDCR_QW</b>
Project:	All					
Format:	<b>MDCR_QW</b>					
1.0-1.7	255:0	<p><b>Slot[7:4] Src0</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td><b>MDCR_QW</b></td> </tr> </table> <p>Specifies the Slot [7:4] Source 0 data</p>	Project:	All	Format:	<b>MDCR_QW</b>
Project:	All					
Format:	<b>MDCR_QW</b>					
2.0-2.7	255:0	<p><b>Slot[3:0] Src1</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td><b>MDCR_QW</b></td> </tr> </table> <p>Specifies the Slot [3:0] Source 1 data</p>	Project:	All	Format:	<b>MDCR_QW</b>
Project:	All					
Format:	<b>MDCR_QW</b>					
3.0-3.7	255:0	<p><b>Slot[7:4] Src1</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td><b>MDCR_QW</b></td> </tr> </table> <p>Specifies the Slot [7:4] Source 1 data</p>	Project:	All	Format:	<b>MDCR_QW</b>
Project:	All					
Format:	<b>MDCR_QW</b>					

## Qword SIMD8 Atomic Operation Return Data Message Data Payload

<b>MDP_AOP8_QW1 - Qword SIMD8 Atomic Operation Return Data Message Data Payload</b>						
<b>DWord</b>	<b>Bit</b>	<b>Description</b>				
0.0-0.7	255:0	<p><b>Slot[7:0] Qword[31:0]</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDCR_DW</b></td></tr> </table> <p>Specifies the lower 32-bits of Slot [7:0] Return data</p>	Project:	All	Format:	<b>MDCR_DW</b>
Project:	All					
Format:	<b>MDCR_DW</b>					
1.0-1.7	255:0	<p><b>Slot[7:0] Qword[63:32]</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDCR_DW</b></td></tr> </table> <p>Specifies the upper 32-bits of Slot [7:0] Return data</p>	Project:	All	Format:	<b>MDCR_DW</b>
Project:	All					
Format:	<b>MDCR_DW</b>					

## Qword SIMD8 Data Payload

MDP_QW SIMD8 - Qword SIMD8 Data Payload						
DWord	Bit	Description				
0.0-0.7	255:0	<p><b>Data[3:0]</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDCR_QW</b></td></tr> </table> <p>Specifies the Slot [3:0] data</p>	Project:	All	Format:	<b>MDCR_QW</b>
Project:	All					
Format:	<b>MDCR_QW</b>					
1.0-1.7	255:0	<p><b>Data[7:4]</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDCR_QW</b></td></tr> </table> <p>Specifies the Slot [7:4] data</p>	Project:	All	Format:	<b>MDCR_QW</b>
Project:	All					
Format:	<b>MDCR_QW</b>					

## Qword SIMD16 Atomic Operation CMPWR8B Message Data Payload

<b>MDP_AOP16_QW2 - Qword SIMD16 Atomic Operation CMPWR8B Message Data Payload</b>						
<b>DWord</b>	<b>Bit</b>	<b>Description</b>				
0.0-0.7	255:0	<b>Slot[7:0] Src0[31:0]</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDCR_DW</b></td></tr> </table> Specifies the lower 32-bits of Source 0 data for Slot [7:0]	Project:	All	Format:	<b>MDCR_DW</b>
Project:	All					
Format:	<b>MDCR_DW</b>					
1.0-1.7	255:0	<b>Slot[15:8] Src0[31:0]</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDCR_DW</b></td></tr> </table> Specifies the lower 32-bits Source 0 data for Slot [15:8]	Project:	All	Format:	<b>MDCR_DW</b>
Project:	All					
Format:	<b>MDCR_DW</b>					
2.0-2.7	255:0	<b>Slot[7:0] Src0[63:32]</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDCR_DW</b></td></tr> </table> Specifies the upper 32-bits of Source 0 data for Slot [7:0]	Project:	All	Format:	<b>MDCR_DW</b>
Project:	All					
Format:	<b>MDCR_DW</b>					
3.0-3.7	255:0	<b>Slot[15:8] Src0[63:32]</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDCR_DW</b></td></tr> </table> Specifies the upper 32-bits Source 0 data for Slot [15:8]	Project:	All	Format:	<b>MDCR_DW</b>
Project:	All					
Format:	<b>MDCR_DW</b>					
4.0-4.7	255:0	<b>Slot[7:0] Src1[31:0]</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDCR_DW</b></td></tr> </table> Specifies the lower 32-bits of Source 1 data for Slot [7:0]	Project:	All	Format:	<b>MDCR_DW</b>
Project:	All					
Format:	<b>MDCR_DW</b>					

## MDP\_AOP16\_QW2 - Qword SIMD16 Atomic Operation CMPWR8B Message Data Payload

5.0-5.7	255:0	<b>Slot[15:8] Src1[31:0]</b>				
		<table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDCR_DW</b></td></tr> </table> <p>Specifies the lower 32-bits Source 1 data for Slot [15:8]</p>	Project:	All	Format:	<b>MDCR_DW</b>
Project:	All					
Format:	<b>MDCR_DW</b>					
6.0-6.7	255:0	<b>Slot[7:0] Src1[63:32]</b>				
		<table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDCR_DW</b></td></tr> </table> <p>Specifies the upper 32-bits of Source 1 data for Slot [7:0]</p>	Project:	All	Format:	<b>MDCR_DW</b>
Project:	All					
Format:	<b>MDCR_DW</b>					
7.0-7.7	255:0	<b>Slot[15:8] Src1[63:32]</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDCR_DW</b></td></tr> </table> <p>Specifies the upper 32-bits Source 1 data for Slot [15:8]</p>	Project:	All	Format:	<b>MDCR_DW</b>
Project:	All					
Format:	<b>MDCR_DW</b>					

## Qword SIMD16 Atomic Operation Return Data Message Data Payload

### MDP\_AOP16\_QW1 - Qword SIMD16 Atomic Operation Return Data Message Data Payload

Project:	BDW					
Size (in bits):	1024					
Default Value:	0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000					
DWord	Bit	Description				
0.0-0.7	255:0	<p><b>Slot[7:0] Qword[31:0]</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDCR_DW</b></td></tr> </table> <p>Specifies the lower 32-bits of Return data for Slot [7:0]</p>	Project:	All	Format:	<b>MDCR_DW</b>
Project:	All					
Format:	<b>MDCR_DW</b>					
1.0-1.7	255:0	<p><b>Slot[15:8] Qword[31:0]</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDCR_DW</b></td></tr> </table> <p>Specifies the lower 32-bits of Return data for Slot [15:8]</p>	Project:	All	Format:	<b>MDCR_DW</b>
Project:	All					
Format:	<b>MDCR_DW</b>					
2.0-2.7	255:0	<p><b>Slot[7:0] Qword[63:32]</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDCR_DW</b></td></tr> </table> <p>Specifies the upper 32-bits of Return data for Slot [7:0]</p>	Project:	All	Format:	<b>MDCR_DW</b>
Project:	All					
Format:	<b>MDCR_DW</b>					
3.0-3.7	255:0	<p><b>Slot[15:8] Qword[63:32]</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDCR_DW</b></td></tr> </table> <p>Specifies the upper 32-bits of Return data for Slot [15:8]</p>	Project:	All	Format:	<b>MDCR_DW</b>
Project:	All					
Format:	<b>MDCR_DW</b>					

## Qword SIMD16 Data Payload

### MDP\_QW SIMD16 - Qword SIMD16 Data Payload

Project:	BDW					
Size (in bits):	1024					
Default Value:	0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000					
<b>Description</b>						
0.0-0.7	255:0	<p><b>Data[3:0]</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td><b>MDCR_QW</b></td> </tr> </table> <p>Specifies the Slot [3:0] data</p>	Project:	All	Format:	<b>MDCR_QW</b>
Project:	All					
Format:	<b>MDCR_QW</b>					
1.0-1.7	255:0	<p><b>Data[7:4]</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td><b>MDCR_QW</b></td> </tr> </table> <p>Specifies the Slot [7:4] data</p>	Project:	All	Format:	<b>MDCR_QW</b>
Project:	All					
Format:	<b>MDCR_QW</b>					
2.0-2.7	255:0	<p><b>qw11_qw8</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td><b>MDCR_QW</b></td> </tr> </table> <p>Specifies the Slot [11:8] data</p>	Project:	All	Format:	<b>MDCR_QW</b>
Project:	All					
Format:	<b>MDCR_QW</b>					
3.0-3.7	255:0	<p><b>qw15_qw12</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td><b>MDCR_QW</b></td> </tr> </table> <p>Specifies the Slot [15:12] data</p>	Project:	All	Format:	<b>MDCR_QW</b>
Project:	All					
Format:	<b>MDCR_QW</b>					

## Read-Only Data Port Message Types

MT_DP_RO - Read-Only Data Port Message Types																																	
DWord	Bit	Description																															
0	4	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> <tr> <td>Ignored</td> <td></td> </tr> </table>	Format:	MBZ	Ignored																												
Format:	MBZ																																
Ignored																																	
	3:0	<p><b>Message Type</b></p> <table border="1"> <tr> <td>Format:</td> <td>Enumeration</td> </tr> <tr> <td colspan="2">Specifies type of message</td></tr> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> <tr> <td>00h</td><td>MT_CC_OWB [Default]</td><td>Oword Block Read Constant Cache message</td></tr> <tr> <td>01h</td><td>MT_CC_OWUB</td><td>Unaligned Oword Block Read Constant Cache message</td></tr> <tr> <td>02h</td><td>MT_CC_OWDB</td><td>Oword Dual Block Read Constant Cache message</td></tr> <tr> <td>03h</td><td>MT_CC_DWS</td><td>Dword Scattered Read Constant Cache message</td></tr> <tr> <td>04h</td><td>MT_SC_OWUB</td><td>Unaligned Oword Block Read Sampler Cache message</td></tr> <tr> <td>05h</td><td>MT_SC_MB</td><td>Media Block Read Sampler Cache message</td></tr> <tr> <td>06h</td><td>MT_RSI</td><td>Read Surface Info message</td></tr> <tr> <td>Others</td><td>Reserved</td><td>Ignored</td></tr> </table>	Format:	Enumeration	Specifies type of message		Value	Name	Description	00h	MT_CC_OWB [Default]	Oword Block Read Constant Cache message	01h	MT_CC_OWUB	Unaligned Oword Block Read Constant Cache message	02h	MT_CC_OWDB	Oword Dual Block Read Constant Cache message	03h	MT_CC_DWS	Dword Scattered Read Constant Cache message	04h	MT_SC_OWUB	Unaligned Oword Block Read Sampler Cache message	05h	MT_SC_MB	Media Block Read Sampler Cache message	06h	MT_RSI	Read Surface Info message	Others	Reserved	Ignored
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06h	MT_RSI	Read Surface Info message																															
Others	Reserved	Ignored																															

## Read Surface Info 32-Bit Address Payload

<b>MAP32B_RSI - Read Surface Info 32-Bit Address Payload</b>						
<b>DWord</b>	<b>Bit</b>	<b>Description</b>				
0.0	31:0	<p><b>U</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U32</td></tr> </table> <p>Specifies the U channel address offset.</p>	Project:	All	Format:	U32
Project:	All					
Format:	U32					
0.1	31:0	<p><b>V</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U32</td></tr> </table> <p>Specifies the V channel address offset.</p>	Project:	All	Format:	U32
Project:	All					
Format:	U32					
0.2	31:0	<p><b>R</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U32</td></tr> </table> <p>Specifies the R channel address offset.</p>	Project:	All	Format:	U32
Project:	All					
Format:	U32					
0.3	31:0	<p><b>LOD</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MACD_LOD</b></td></tr> </table> <p>Specifies the LOD.</p>	Project:	All	Format:	<b>MACD_LOD</b>
Project:	All					
Format:	<b>MACD_LOD</b>					
0.4-0.7	127:0	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>Ignore</td></tr> </table> <p>Ignored</p>	Project:	All	Format:	Ignore
Project:	All					
Format:	Ignore					

## Read Surface Info Data Payload

<b>MDP_RSI - Read Surface Info Data Payload</b>								
<b>DWord</b>	<b>Bit</b>	<b>Description</b>						
0.0-0.5	191:0	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Ignore</td> </tr> <tr> <td colspan="2">Ignored</td></tr> </table>	Project:	All	Format:	Ignore	Ignored	
Project:	All							
Format:	Ignore							
Ignored								
0.6-0.7	63:0	<p><b>Instruction Base Address</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>GraphicsAddress[63:0]</td> </tr> </table> <p>Instruction Base Address from STATE_BASE_ADDRESS, extended to 64-bit format.</p> <p><b>Programming Notes</b></p> <p>The 48-bit address is returned in a 64-bit address in canonical form.</p>	Project:	All	Format:	GraphicsAddress[63:0]		
Project:	All							
Format:	GraphicsAddress[63:0]							
1.0	31:0	<p><b>Width</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U32</td> </tr> </table> <p>Surface Width generally computed from RENDER_SURFACE_STATE Width (stored as width minus 1). The value is 0 for NULL surface, and in all other cases (Width+1) » LOD. Surface Width from RENDER_SURFACE_STATE (U14), zero extended to 32 bits.</p>	Project:	All	Format:	U32		
Project:	All							
Format:	U32							
1.1	31:0	<p><b>Height</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U32</td> </tr> </table> <p>Surface Height, generally computed from RENDER_SURFACE_STATE Height (stored as height minus 1). The value for a 1D array is RENDER_SURFACE_STATE's (Depth + 1). The value for 1D non-array, BUFFER, and NULL surface is 0. In all other case, the value is (Height + 1) » LOD.</p>	Project:	All	Format:	U32		
Project:	All							
Format:	U32							
1.2	31:0	<p><b>Depth</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U32</td> </tr> </table> <p>Surface Depth, generally computed from RENDER_SURFACE_STATE Depth (which is stored depth minus 1). If 2D Array or Cube Array surface, value is the (Depth+1). If 3D surface, value is (Depth+1) » LOD. In all other case, the value is 0.</p>	Project:	All	Format:	U32		
Project:	All							
Format:	U32							

## MDP\_RSI - Read Surface Info Data Payload

		<b>MDP_RSI - Read Surface Info Data Payload</b>																																															
1.3	31:0	<b>MIP Count</b>																																															
<table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U32</td></tr> </table>			Project:	All	Format:	U32	MIP Count from RENDER_SURFACE_STATE, range [0, 14], zero extended to 32 bits.																																										
Project:	All																																																
Format:	U32																																																
1.4	31:0	<b>Surface Type</b>																																															
<table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U32</td></tr> </table>			Project:	All	Format:	U32	Surface Type from RENDER_SURFACE_STATE, zero extended to 32 bits																																										
Project:	All																																																
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Others	Reserved	Reserved																																															
1.5	31:0	<b>Surface Format</b>																																															
<table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U32</td></tr> </table>			Project:	All	Format:	U32	Surface Format from RENDER_SURFACE_STATE (U9), zero extended to 32 bits.																																										
Project:	All																																																
Format:	U32																																																
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## RENDER\_SURFACE\_STATE

RENDER_SURFACE_STATE																													
DWord	Bit	Description																											
0	31:29	<p><b>Surface Type</b> This field defines the type of the surface.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>SURFTYPE_1D</td> <td>Defines a 1-dimensional map or array of maps</td> </tr> <tr> <td>1h</td> <td>SURFTYPE_2D</td> <td>Defines a 2-dimensional map or array of maps</td> </tr> <tr> <td>2h</td> <td>SURFTYPE_3D</td> <td>Defines a 3-dimensional (volumetric) map</td> </tr> <tr> <td>3h</td> <td>SURFTYPE_CUBE</td> <td>Defines a cube map or array of cube maps</td> </tr> <tr> <td>4h</td> <td>SURFTYPE_BUFFER</td> <td>Defines an element in a buffer</td> </tr> <tr> <td>5h</td> <td>SURFTYPE_STRBUF</td> <td>Defines a structured buffer surface</td> </tr> <tr> <td>6h</td> <td>Reserved</td> <td></td> </tr> <tr> <td>7h</td> <td>SURFTYPE_NULL</td> <td>Defines a null surface</td> </tr> </tbody> </table>	Value	Name	Description	0h	SURFTYPE_1D	Defines a 1-dimensional map or array of maps	1h	SURFTYPE_2D	Defines a 2-dimensional map or array of maps	2h	SURFTYPE_3D	Defines a 3-dimensional (volumetric) map	3h	SURFTYPE_CUBE	Defines a cube map or array of cube maps	4h	SURFTYPE_BUFFER	Defines an element in a buffer	5h	SURFTYPE_STRBUF	Defines a structured buffer surface	6h	Reserved		7h	SURFTYPE_NULL	Defines a null surface
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6h	Reserved																												
7h	SURFTYPE_NULL	Defines a null surface																											
<b>Programming Notes</b>																													
<p>A null surface is used in instances where an actual surface is not bound. When a write message is generated to a null surface, no actual surface is written to. When a read message (including any sampling engine message) is generated to a null surface, the result is all zeros. Note that a null surface type is allowed to be used with all messages, even if it is not specifically indicated as supported. All of the remaining fields in surface state are ignored for null surfaces, with the following exceptions:</p> <ul style="list-style-type: none"> <li>• <b>Width, Height, Depth, LOD, and Render Target View Extent</b> fields must match the depth buffer's corresponding state for all render target surfaces, including null.</li> </ul> <p>All sampling engine and data port messages support null surfaces with the above behavior, even if not mentioned as specifically supported, except for the following:</p> <ul style="list-style-type: none"> <li>• Data Port Media Block Read/Write messages</li> <li>• Data Port Transpose Read message</li> <li>• The <b>Surface Type</b> of a surface used as a render target (accessed via the Data Port's Render Target Write message) must be the same as the <b>Surface Type</b> of all other render targets and of the depth buffer (defined in 3DSTATE_DEPTH_BUFFER), unless either the</li> </ul>																													

RENDER_SURFACE_STATE																
		<p>depth buffer or render targets are SURFTYPE_NULL.</p> <p>For sampling using the 3D sampler, if the Surface Type is programmed to SURFTYPE_NULL, the Surface Format must be a supported surface format for the 3D sampler.</p>														
28	<b>Surface Array</b>	<table border="1"> <tr> <td>Format:</td><td>Enable</td></tr> <tr> <td colspan="2">This field, if enabled, indicates that the surface is an array.</td></tr> <tr> <td colspan="2" style="text-align: center;"><b>Programming Notes</b></td></tr> <tr> <td colspan="2">If this field is <i>enabled</i>, the <b>Surface Type</b> must be SURFTYPE_1D, SURFTYPE_2D, or SURFTYPE_CUBE.</td></tr> <tr> <td colspan="2">If this field is <i>disabled</i> and <b>Surface Type</b> is SURFTYPE_1D, SURFTYPE_2D, or SURFTYPE_CUBE, the <b>Depth</b> field must be set to zero.</td></tr> </table>	Format:	Enable	This field, if enabled, indicates that the surface is an array.		<b>Programming Notes</b>		If this field is <i>enabled</i> , the <b>Surface Type</b> must be SURFTYPE_1D, SURFTYPE_2D, or SURFTYPE_CUBE.		If this field is <i>disabled</i> and <b>Surface Type</b> is SURFTYPE_1D, SURFTYPE_2D, or SURFTYPE_CUBE, the <b>Depth</b> field must be set to zero.					
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27	<b>Reserved</b>	<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	BDW	Format:	MBZ										
Project:	BDW															
Format:	MBZ															
26:18	<b>Surface Format</b>	<table border="1"> <tr> <td>Format:</td><td><b>SURFACE_FORMAT</b></td></tr> <tr> <td colspan="2">This field specifies the format of the surface or element within this surface. This field is ignored for all data port messages other than the render target message and streamed vertex buffer write message. Some forms of the media block messages use the surface format.</td></tr> <tr> <td colspan="2" style="text-align: center;"><b>Programming Notes</b></td></tr> <tr> <td colspan="2">If <b>Number of Multisamples</b> is set to a value other than MULTISAMPLECOUNT_1, this field cannot be set to the following formats:</td></tr> <tr> <td colspan="2"> <ul style="list-style-type: none"> <li>Any compressed texture format (BC*, DXT*, FXT*, ETC*, EAC*)</li> <li>Any YCRCB* format</li> </ul> </td></tr> <tr> <td colspan="2">This field cannot be a YUV (YCRCB*) or compressed (BC*, DXT*, FXT*, ETC*, EAC*) format if the <b>Surface Type</b> is SURFTYPE_BUFFER or SURFTYPE_STRBUF</td></tr> <tr> <td colspan="2">This field cannot be a compressed (BC*, DXT*, FXT*, ETC*, EAC*) format if the <b>Surface Type</b> is SURFTYPE_1D.</td></tr> </table>	Format:	<b>SURFACE_FORMAT</b>	This field specifies the format of the surface or element within this surface. This field is ignored for all data port messages other than the render target message and streamed vertex buffer write message. Some forms of the media block messages use the surface format.		<b>Programming Notes</b>		If <b>Number of Multisamples</b> is set to a value other than MULTISAMPLECOUNT_1, this field cannot be set to the following formats:		<ul style="list-style-type: none"> <li>Any compressed texture format (BC*, DXT*, FXT*, ETC*, EAC*)</li> <li>Any YCRCB* format</li> </ul>		This field cannot be a YUV (YCRCB*) or compressed (BC*, DXT*, FXT*, ETC*, EAC*) format if the <b>Surface Type</b> is SURFTYPE_BUFFER or SURFTYPE_STRBUF		This field cannot be a compressed (BC*, DXT*, FXT*, ETC*, EAC*) format if the <b>Surface Type</b> is SURFTYPE_1D.	
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## RENDER\_SURFACE\_STATE

17:16

**Surface Vertical Alignment**
**Description**

**For Sampling Engine and Render Target Surfaces:** This field specifies the vertical alignment requirement in elements for the surface. Refer to the "Memory Data Formats" chapter for details on how this field changes the layout of the surface in memory. An *element* is defined as a pixel in uncompressed surface formats, and as a compression block in compressed surface formats. For MSFMT\_DEPTH\_STENCIL type multisampled surfaces, an element is a sample.

This field applies to surface formats other than compressed formats.

**For other surfaces:** This field is ignored.

Value	Name	Description
0h	Reserved	Reserved
1h	VALIGN_4	Vertical alignment factor j = 4
2h	VALIGN_8	Vertical alignment factor j = 8
3h	VALIGN_16	Vertical alignment factor j = 16

**Programming Notes**

This field is intended to be set to VALIGN\_4 if the surface was rendered as a depth buffer, for a multisampled (4x) render target, or for a multisampled (8x) render target, since these surfaces support only alignment of 4. Use of VALIGN\_4 for other surfaces is supported, but increases memory usage.

This field is intended to be set to VALIGN\_8 only if the surface was rendered as a stencil buffer, since stencil buffer surfaces support only alignment of 8. If set to VALIGN\_8, Surface Format must be R8\_UINT.

For uncompressed surfaces, the units of "j" are rows of pixels on the physical surface. For compressed texture formats, the units of "j" are in compression blocks, thus each increment in "j" is equal to h pixels, where h is the height of the compression block in pixels.

## RENDER\_SURFACE\_STATE

15:14	<b>Surface Horizontal Alignment</b>																
	<b>Description</b>																
	For Sampling Engine and Render Target Surfaces: This field specifies the horizontal alignment requirement for the surface.																
	This field applies to surface formats other than compressed formats.																
	<b>For other surfaces:</b> This field is ignored.																
<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center; background-color: #e0e0ff;">Value</th><th style="text-align: center; background-color: #e0e0ff;">Name</th><th style="text-align: center; background-color: #e0e0ff;">Description</th></tr> </thead> <tbody> <tr><td style="text-align: center;">0h</td><td style="text-align: center;">Reserved</td><td>Reserved</td></tr> <tr><td style="text-align: center;">1h</td><td style="text-align: center;">HALIGN 4</td><td>Horizontal alignment factor j = 4</td></tr> <tr><td style="text-align: center;">2h</td><td style="text-align: center;">HALIGN 8</td><td>Horizontal alignment factor j = 8</td></tr> <tr><td style="text-align: center;">3h</td><td style="text-align: center;">HALIGN 16</td><td>Horizontal alignment factor j = 16</td></tr> </tbody> </table>			Value	Name	Description	0h	Reserved	Reserved	1h	HALIGN 4	Horizontal alignment factor j = 4	2h	HALIGN 8	Horizontal alignment factor j = 8	3h	HALIGN 16	Horizontal alignment factor j = 16
Value	Name	Description															
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1h	HALIGN 4	Horizontal alignment factor j = 4															
2h	HALIGN 8	Horizontal alignment factor j = 8															
3h	HALIGN 16	Horizontal alignment factor j = 16															
<b>Programming Notes</b> <p>This field is intended to be set to HALIGN_8 only if the surface was rendered as a depth buffer with Z16 format or a stencil buffer. In this case it must be set to HALIGN_8 since these surfaces support only alignment of 8. For Z32 formats it must be set to HALIGN_4. Use of HALIGN_8 for other surfaces is supported, but increases memory usage.</p> <p>For uncompressed surfaces, the units of "i" are pixels on the physical surface. For compressed texture formats, the units of "i" are in compression blocks, thus each increment in "i" is equal to w pixels, where w is the width of the compression block in pixels.</p> <p>When Auxiliary Surface Mode is set to AUX_CCS_D or AUX_CCS_E, HALIGN 16 must be used.</p>																	

## RENDER\_SURFACE\_STATE

13:12	<p><b>Tile Mode</b></p> <p>This field specifies the type of memory tiling (Linear, WMajor, XMajor, or YMajor) employed to tile this surface. See <i>Memory Interface Functions</i> for details on memory tiling and restrictions.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th><th style="text-align: center;">Name</th><th style="text-align: center;">Description</th></tr> </thead> <tbody> <tr> <td style="text-align: center;">0h</td><td style="text-align: center;">LINEAR</td><td>Linear mode (no tiling)</td></tr> <tr> <td style="text-align: center;">1h</td><td style="text-align: center;">WMAJOR</td><td>W major tiling</td></tr> <tr> <td style="text-align: center;">2h</td><td style="text-align: center;">XMAJOR</td><td>X major tiling</td></tr> <tr> <td style="text-align: center;">3h</td><td style="text-align: center;">YMAJOR</td><td>Y major tiling</td></tr> </tbody> </table> <p style="text-align: center;"><b>Programming Notes</b></p> <ul style="list-style-type: none"> <li>• Refer to <i>Memory Data Formats</i> for restrictions on <i>TileMode</i> direction for the various buffer types. (Of particular interest is the fact that YMAJOR tiling is not supported for display/overlay buffers).</li> <li>• The corresponding cache(s) must be invalidated before a previously accessed surface is accessed again with an altered state of this field.</li> <li>• Use of WMAJOR is valid only for sampling engine, Data Cache Data Port and render target surfaces and <b>Surface Format</b> must be R8_UINT. Vertical Line Stride must be zero. In addition to W tiling, this mode implies that the surface is stored as a stencil buffer. Refer to <i>Memory Data Formats</i> section for details on stencil buffer surface layout.</li> <li>• Linear surfaces can be mapped to Main Memory (uncached) or System Memory (cacheable, snooped). Tiled (X/Y/W) surfaces can only be mapped to Main Memory.</li> <li>• If <b>Surface Type</b> is SURFTYPE_BUFFER, this field must be TILEMODE_LINEAR</li> <li>• If <b>Number of Multisamples</b> is not MULTISAMPLECOUNT_1, this field must be YMAJOR.</li> </ul>	Value	Name	Description	0h	LINEAR	Linear mode (no tiling)	1h	WMAJOR	W major tiling	2h	XMAJOR	X major tiling	3h	YMAJOR	Y major tiling
Value	Name	Description														
0h	LINEAR	Linear mode (no tiling)														
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3h	YMAJOR	Y major tiling														
11	<p><b>Vertical Line Stride</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 10%;">Format:</td><td>U1</td><td>In lines to skip between logically adjacent lines</td></tr> </table> <p><b>For 2D Non-Array Surfaces accessed via the Sampling Engine or Data Cache Data Port:</b> Specifies number of lines (0 or 1) to skip between logically adjacent lines - provides support of interleaved (field) surfaces as textures.</p> <p><b>For Other Surfaces:</b> Vertical Line Stride must be zero.</p> <p style="text-align: center;"><b>Programming Notes</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td>This bit must not be set if the surface format is a compressed type (BCn*, FXT1, ETC*, EAC*).</td></tr> <tr> <td>This bit must not be set if the <b>Auxiliary Surface Mode</b> is not AUX_NONE.</td></tr> <tr> <td>If this bit is set on a sampling engine surface, the mip mode filter must be set to MIPFILTER_NONE and the min and mag mode filter cannot be set to MAPFILTER_FLEXIBLE.</td></tr> </table> <p style="text-align: center;"><b>Workaround</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td>Workaround (BDW bug# 1909178) : All surfaces used by the sampler between sampler cache invalidates must have the same setting of this field in both RENDER_SURFACE_STATE and MEDIA_SURFACE_STATE.</td></tr> </table>	Format:	U1	In lines to skip between logically adjacent lines	This bit must not be set if the surface format is a compressed type (BCn*, FXT1, ETC*, EAC*).	This bit must not be set if the <b>Auxiliary Surface Mode</b> is not AUX_NONE.	If this bit is set on a sampling engine surface, the mip mode filter must be set to MIPFILTER_NONE and the min and mag mode filter cannot be set to MAPFILTER_FLEXIBLE.	Workaround (BDW bug# 1909178) : All surfaces used by the sampler between sampler cache invalidates must have the same setting of this field in both RENDER_SURFACE_STATE and MEDIA_SURFACE_STATE.								
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## RENDER\_SURFACE\_STATE

	<b>Vertical Line Stride Offset</b>									
	<table border="1" style="width: 100%;"> <tr> <td style="padding: 2px;">Format:</td> <td style="padding: 2px;">U1 In lines of initial offset (when Vertical Line Stride == 1)</td> </tr> </table>	Format:	U1 In lines of initial offset (when Vertical Line Stride == 1)							
Format:	U1 In lines of initial offset (when Vertical Line Stride == 1)									
<b>For 2D Non-Array Surfaces accessed via the Sampling Engine or Data Cache Data Port:</b>										
Specifies the offset of the initial line from the beginning of the buffer. Ignored when Vertical Line Stride is 0.										
<b>For Other Surfaces:</b>										
Vertical Line Stride Offset must be zero.										
	<b>Sampler L2 Bypass Mode Disable</b>									
	<table border="1" style="width: 100%;"> <tr> <td style="padding: 2px;">Format:</td> <td style="padding: 2px;">Disable</td> </tr> </table>	Format:	Disable							
Format:	Disable									
This field allows the Sampler L2 bypass mode to be disabled for the surface. If enabled, Sampler can still disable the L2 bypass as needed.										
	<b>Render Cache Read Write Mode</b>									
<b>For Surfaces accessed via the Data Port to Render Cache:</b>										
This field specifies the way Render Cache treats a write request. If unset, Render Cache allocates a write-only cache line for a write miss. If set, Render Cache allocates a read-write cache line for a write miss.										
<b>For Surfaces accessed via the Sampling Engine or Data Port to Texture Cache or Data Cache:</b>										
This field is reserved : MBZ										
<table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th style="background-color: #e0e0ff; width: 15%;">Value</th> <th style="background-color: #e0e0ff; width: 15%;">Name</th> <th style="background-color: #e0e0ff; width: 70%;">Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Write-Only Cache</td> <td>Allocating write-only cache for a write miss</td> </tr> <tr> <td>1h</td> <td>Read-Write Cache</td> <td>Allocating read-write cache for a write miss</td> </tr> </tbody> </table>		Value	Name	Description	0h	Write-Only Cache	Allocating write-only cache for a write miss	1h	Read-Write Cache	Allocating read-write cache for a write miss
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0h	Write-Only Cache	Allocating write-only cache for a write miss								
1h	Read-Write Cache	Allocating read-write cache for a write miss								
<b>Programming Notes</b>										
This field is provided for performance optimization for Render Cache read/write accesses (from Gen4 EU's point of view).										

## RENDER\_SURFACE\_STATE

7:6	<p><b>Media Boundary Pixel Mode</b></p> <p><b>For 2D Non-Array Surfaces accessed via the Data Port Media Block Read Message or Data Port Transpose Read message:</b></p> <p>This field enables control of which rows are returned on vertical out-of-bounds reads using the Data Port Media Block Read Message or Data Port Transpose Read message. In the description below, frame mode refers to <b>Vertical Line Stride</b> = 0, field mode is <b>Vertical Line Stride</b> = 1 in which only the even or odd rows are addressable. The frame refers to the entire surface, while the field refers only to the even or odd rows within the surface.</p> <p><b>For Other Surfaces:</b></p> <p>Reserved : MBZ</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center; padding: 2px;"><b>Value</b></th><th style="text-align: center; padding: 2px;"><b>Name</b></th><th style="text-align: center; padding: 2px;"><b>Description</b></th></tr> </thead> <tbody> <tr> <td style="text-align: center; padding: 2px;">0h</td><td style="text-align: center; padding: 2px;">NORMAL_MODE</td><td style="padding: 2px;">The row returned on an out-of-bound access is the closest row in the frame or field. Rows from the opposite field are never returned.</td></tr> <tr> <td style="text-align: center; padding: 2px;">1h</td><td style="text-align: center; padding: 2px;">Reserved</td><td style="padding: 2px;"></td></tr> <tr> <td style="text-align: center; padding: 2px;">2h</td><td style="text-align: center; padding: 2px;">PROGRESSIVE_FRAME</td><td style="padding: 2px;">The row returned on an out-of-bound access is the closest row in the frame, even if in field mode.</td></tr> <tr> <td style="text-align: center; padding: 2px;">3h</td><td style="text-align: center; padding: 2px;">INTERLACED_FRAME</td><td style="padding: 2px;">In field mode, the row returned on an out-of-bound access is the closest row in the field. In frame mode, even out-of-bound rows return the nearest even row while odd out-of-bound rows return the nearest odd row.</td></tr> </tbody> </table>	<b>Value</b>	<b>Name</b>	<b>Description</b>	0h	NORMAL_MODE	The row returned on an out-of-bound access is the closest row in the frame or field. Rows from the opposite field are never returned.	1h	Reserved		2h	PROGRESSIVE_FRAME	The row returned on an out-of-bound access is the closest row in the frame, even if in field mode.	3h	INTERLACED_FRAME	In field mode, the row returned on an out-of-bound access is the closest row in the field. In frame mode, even out-of-bound rows return the nearest even row while odd out-of-bound rows return the nearest odd row.
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5	<p><b>Cube Face Enable - Negative X</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 20%;">Exists If:</td><td style="width: 80%;">[Surface Type] == 'SURFTYPE_CUBE'</td></tr> <tr> <td>Format:</td><td>Enable</td></tr> </table> <p><b>For SURFTYPE_CUBE Surfaces accessed via the Sampling Engine:</b> This field enable the individual face of a cube map. Enabling a face indicates that the face is present in the cube map, while disabling it indicates that that face is represented by the texture map's border color. Refer to Memory Data Formats for the correlation between faces and the cube map memory layout. Note that storage for disabled faces must be provided.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="text-align: center; padding: 2px;"><b>Programming Notes</b></td></tr> <tr> <td style="padding: 2px;">When TEXCOORDMODE_CLAMP is used when accessing a cube map, this field must be programmed to 1b (face enabled).</td></tr> </table>	Exists If:	[Surface Type] == 'SURFTYPE_CUBE'	Format:	Enable	<b>Programming Notes</b>	When TEXCOORDMODE_CLAMP is used when accessing a cube map, this field must be programmed to 1b (face enabled).									
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## RENDER\_SURFACE\_STATE

		<b>Cube Face Enable - Positive X</b>				
	4	<table border="1" style="width: 100%;"> <tr> <td>Exists If:</td><td>[Surface Type] == 'SURFTYPE_CUBE'</td></tr> <tr> <td>Format:</td><td>Enable</td></tr> </table> <p><b>For SURFTYPE_CUBE Surfaces accessed via the Sampling Engine:</b> This field enable the individual face of a cube map. Enabling a face indicates that the face is present in the cube map, while disabling it indicates that that face is represented by the texture map's border color. Refer to Memory Data Formats for the correlation between faces and the cube map memory layout. Note that storage for disabled faces must be provided.</p>	Exists If:	[Surface Type] == 'SURFTYPE_CUBE'	Format:	Enable
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		<table border="1" style="width: 100%;"> <tr> <td>Exists If:</td><td>[Surface Type] == 'SURFTYPE_CUBE'</td></tr> <tr> <td>Format:</td><td>Enable</td></tr> </table> <p><b>For SURFTYPE_CUBE Surfaces accessed via the Sampling Engine:</b> This field enable the individual face of a cube map. Enabling a face indicates that the face is present in the cube map, while disabling it indicates that that face is represented by the texture map's border color. Refer to Memory Data Formats for the correlation between faces and the cube map memory layout. Note that storage for disabled faces must be provided.</p>	Exists If:	[Surface Type] == 'SURFTYPE_CUBE'	Format:	Enable
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## RENDER\_SURFACE\_STATE

		<b>Cube Face Enable - Negative Z</b>				
	1	<table border="1"> <tr> <td>Exists If:</td><td>[Surface Type] == 'SURFTYPE_CUBE'</td></tr> <tr> <td>Format:</td><td>Enable</td></tr> </table>	Exists If:	[Surface Type] == 'SURFTYPE_CUBE'	Format:	Enable
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		<b>Programming Notes</b>				
		When TEXCOORDMODE_CLAMP is used when accessing a cube map, this field must be programmed to 1b (face enabled).				
	5:0	<b>Reserved</b> <table border="1"> <tr> <td>Exists If:</td><td>[Surface Type] != 'SURFTYPE_CUBE'</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Exists If:	[Surface Type] != 'SURFTYPE_CUBE'	Format:	MBZ
Exists If:	[Surface Type] != 'SURFTYPE_CUBE'					
Format:	MBZ					
	0	<b>Cube Face Enable - Positive Z</b> <table border="1"> <tr> <td>Exists If:</td><td>[Surface Type] == 'SURFTYPE_CUBE'</td></tr> <tr> <td>Format:</td><td>Enable</td></tr> </table> <p><b>For SURFTYPE_CUBE Surfaces accessed via the Sampling Engine:</b> This field enable the individual face of a cube map. Enabling a face indicates that the face is present in the cube map, while disabling it indicates that that face is represented by the texture map's border color. Refer to Memory Data Formats for the correlation between faces and the cube map memory layout. Note that storage for disabled faces must be provided.</p>	Exists If:	[Surface Type] == 'SURFTYPE_CUBE'	Format:	Enable
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	1	<b>Reserved</b> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	BDW	Format:	MBZ
Project:	BDW					
Format:	MBZ					
	30:24	<b>Memory Object Control State</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MEMORY_OBJECT_CONTROL_STATE</b></td></tr> </table> <p>Specifies the memory object control state for this surface and the associated Auxiliary surface (if any).</p>	Project:	All	Format:	<b>MEMORY_OBJECT_CONTROL_STATE</b>
Project:	All					
Format:	<b>MEMORY_OBJECT_CONTROL_STATE</b>					

## RENDER SURFACE STATE

23:19	<b>Base Mip Level</b>
	Project: All
	Format: U4.1
Range: [0.0, 14.0]	
Specifies which mip level is considered the "base" level when determining mag-vs-min filter and selecting the "base" mip level.	
<b>Programming Notes</b>	
This field also exists in SAMPLER_STATE. If both fields are zero, the Base Mip Level is zero. If one is nonzero, Base Mip Level is the nonzero field. It is illegal to have both Base Mip Level fields nonzero.	
18	<b>Reserved</b>
	Project: BDW
	Format: MBZ
17	<b>Reserved</b>
	Project: BDW
	Format: MBZ
16:15	<b>Reserved</b>
	Format: MBZ

<b>RENDER_SURFACE_STATE</b>								
14:0	<b>Surface QPitch</b>							
	Format:	QPitch[16:2]						
	<b>Description</b>							
	<p>This field specifies the distance in rows between array slices. It is used only in the following cases:</p> <ul style="list-style-type: none"> <li>• <b>Surface Array</b> is enabled OR</li> <li>• <b>Number of Multisamples</b> is not NUMSAMPLES_1 and <b>Multisampled Surface Storage Format</b> set to MSFMT_MSS OR</li> <li>• <b>Surface Type</b> is SURFTYPE_CUBE</li> </ul>							
	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="background-color: #d9e1f2;">Value</th><th style="background-color: #d9e1f2;">Name</th><th style="background-color: #d9e1f2;">Description</th></tr> </thead> <tbody> <tr> <td>[4h,1FFFCh]</td><td></td><td>in multiples of 4 (low 2 bits missing)</td></tr> </tbody> </table>		Value	Name	Description	[4h,1FFFCh]		in multiples of 4 (low 2 bits missing)
Value	Name	Description						
[4h,1FFFCh]		in multiples of 4 (low 2 bits missing)						
	<b>Programming Notes</b>							
	<p>This field must be set to an integer multiple of the <b>Surface Vertical Alignment</b>. For compressed textures (BC*, FXT1, ETC*, EAC*, ASTC Surface Formats), this field is in units of rows in the uncompressed surface, and must be set to an integer multiple of the vertical alignment parameter "j" defined in the <i>Common Surface Formats</i> section.</p>							
	<p>Software must ensure that this field is set to a value sufficiently large such that the array slices in the surface do not overlap. Refer to the Memory Data Formats section for information on how surfaces are stored in memory.</p>							
2	<b>Reserved</b>							
	Format:	MBZ						

## **RENDER\_SURFACE\_STATE**

29:16	<b>Height</b>																								
	Format: U14-1																								
	<b>Description</b>																								
	This field specifies the height of the surface, minus 1. If the surface is MIP-mapped, this field contains the height of the base MIP level. For buffers, this field specifies a portion of the buffer size.																								
	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: left; padding: 2px;"><b>Value</b></th><th style="text-align: left; padding: 2px;"><b>Name</b></th><th style="text-align: left; padding: 2px;"><b>Description</b></th><th style="text-align: left; padding: 2px;"><b>Exists If</b></th></tr> </thead> <tbody> <tr> <td style="padding: 2px;">[0,0]</td><td style="padding: 2px;"></td><td style="padding: 2px;">must be zero</td><td style="padding: 2px;">[Surface Type] == 'SURFTYPE_1D'</td></tr> <tr> <td style="padding: 2px;">[0,16383]</td><td style="padding: 2px;"></td><td style="padding: 2px;">height of surface - 1 (y/v dimension)</td><td style="padding: 2px;">[SurfaceType] == 'SURFTYPE_2D'</td></tr> <tr> <td style="padding: 2px;">[0,2047]</td><td style="padding: 2px;"></td><td style="padding: 2px;">height of surface - 1 (y/v dimension)</td><td style="padding: 2px;">[SurfaceType] == 'SURFTYPE_3D'</td></tr> <tr> <td style="padding: 2px;">[0,16383]</td><td style="padding: 2px;"></td><td style="padding: 2px;">height of surface - 1 (y/v dimension)</td><td style="padding: 2px;">[SurfaceType] == 'SURFTYPE_CUBE'</td></tr> <tr> <td style="padding: 2px;">[0,16383]</td><td style="padding: 2px;"></td><td style="padding: 2px;">contains bits [20:7] of the number of entries in the buffer - 1</td><td style="padding: 2px;">([SurfaceType] == 'SURFTYPE_BUFFER')    ([SurfaceType] == 'SURFTYPE_STRBUF')</td></tr> </tbody> </table>		<b>Value</b>	<b>Name</b>	<b>Description</b>	<b>Exists If</b>	[0,0]		must be zero	[Surface Type] == 'SURFTYPE_1D'	[0,16383]		height of surface - 1 (y/v dimension)	[SurfaceType] == 'SURFTYPE_2D'	[0,2047]		height of surface - 1 (y/v dimension)	[SurfaceType] == 'SURFTYPE_3D'	[0,16383]		height of surface - 1 (y/v dimension)	[SurfaceType] == 'SURFTYPE_CUBE'	[0,16383]		contains bits [20:7] of the number of entries in the buffer - 1
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[0,16383]		height of surface - 1 (y/v dimension)	[SurfaceType] == 'SURFTYPE_CUBE'																						
[0,16383]		contains bits [20:7] of the number of entries in the buffer - 1	([SurfaceType] == 'SURFTYPE_BUFFER')    ([SurfaceType] == 'SURFTYPE_STRBUF')																						
<b>Programming Notes</b>																									
For typed buffer and structured buffer surfaces, the number of entries in the buffer ranges from 1 to $2^{27}$ . For raw buffer surfaces, the number of entries in the buffer is the number of bytes which can range from 1 to $2^{30}$ . After subtracting one from the number of entries, software must place the fields of the resulting 27-bit value into the <b>Height</b> , <b>Width</b> , and <b>Depth</b> fields as indicated, right-justified in each field. Unused upper bits must be set to zero.																									
If <b>Vertical Line Stride</b> is 1, this field indicates the height of the field, not the height of the frame																									
The <b>Height</b> of a render target must be the same as the <b>Height</b> of the other render targets and the depth buffer (defined in 3DSTATE_DEPTH_BUFFER), unless <b>Surface Type</b> is SURFTYPE_1D or SURFTYPE_2D with <b>Depth</b> = 0 (non-array) and <b>LOD</b> = 0 (non-mip mapped).																									
If this surface in memory is accessed with Vertical Line Stride set to both 0 and 1, this field must be an even value when Vertical Line Stride is 0.																									
If Media Pixel Boundary Mode is not set to NORMAL_MODE, this field must be an even value.																									
If Surface Format is PLANAR*, this field must be a multiple of 4																									
<b>Reserved</b>																									
Format:	MBZ																								

## RENDER\_SURFACE\_STATE

13:0	<b>Width</b>																										
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Format:</td><td style="padding: 2px;">U14-1</td></tr> </table>			Format:	U14-1																						
Format:	U14-1																										
<b>Description</b>																											
<p>This field specifies the width of the surface, minus 1. If the surface is MIP-mapped, this field specifies the width of the base MIP level. The width is specified in units of pixels or texels. For buffers, this field specifies a portion of the buffer size.</p>																											
<p>For surfaces accessed with the Media Block Read/Write message, this field is in units of DWords.</p>																											
<p>For surfaces accessed with the Transpose Read Message, this field is in units of DWords.</p>																											
<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="background-color: #e0e0ff; text-align: left; padding: 2px;">Value</th><th style="background-color: #e0e0ff; text-align: left; padding: 2px;">Name</th><th style="background-color: #e0e0ff; text-align: left; padding: 2px;">Description</th><th style="background-color: #e0e0ff; text-align: left; padding: 2px;">Exists If</th></tr> </thead> <tbody> <tr> <td style="padding: 2px;">[0,16383]</td><td style="padding: 2px;"></td><td style="padding: 2px;">width of surface - 1 (x/u dimension)</td><td style="padding: 2px;">[SurfaceType] == 'SURFTYPE_1D'</td></tr> <tr> <td style="padding: 2px;">[0,16383]</td><td style="padding: 2px;"></td><td style="padding: 2px;">width of surface - 1 (x/u dimension)</td><td style="padding: 2px;">[SurfaceType] == 'SURFTYPE_2D'</td></tr> <tr> <td style="padding: 2px;">[0,2047]</td><td style="padding: 2px;"></td><td style="padding: 2px;">width of surface - 1 (x/u dimension)</td><td style="padding: 2px;">[SurfaceType] == 'SURFTYPE_3D'</td></tr> <tr> <td style="padding: 2px;">[0,16383]</td><td style="padding: 2px;"></td><td style="padding: 2px;">width of surface - 1 (x/u dimension)</td><td style="padding: 2px;">[SurfaceType] == 'SURFTYPE_CUBE'</td></tr> <tr> <td style="padding: 2px;">[0,127]</td><td style="padding: 2px;"></td><td style="padding: 2px;">contains bits [6:0] of the number of entries in the buffer - 1</td><td style="padding: 2px;">([SurfaceType] == 'SURFTYPE_BUFFER')    ([SurfaceType] == 'SURFTYPE_STRBUF')</td></tr> </tbody> </table>				Value	Name	Description	Exists If	[0,16383]		width of surface - 1 (x/u dimension)	[SurfaceType] == 'SURFTYPE_1D'	[0,16383]		width of surface - 1 (x/u dimension)	[SurfaceType] == 'SURFTYPE_2D'	[0,2047]		width of surface - 1 (x/u dimension)	[SurfaceType] == 'SURFTYPE_3D'	[0,16383]		width of surface - 1 (x/u dimension)	[SurfaceType] == 'SURFTYPE_CUBE'	[0,127]		contains bits [6:0] of the number of entries in the buffer - 1	([SurfaceType] == 'SURFTYPE_BUFFER')    ([SurfaceType] == 'SURFTYPE_STRBUF')
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[0,16383]		width of surface - 1 (x/u dimension)	[SurfaceType] == 'SURFTYPE_1D'																								
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[0,127]		contains bits [6:0] of the number of entries in the buffer - 1	([SurfaceType] == 'SURFTYPE_BUFFER')    ([SurfaceType] == 'SURFTYPE_STRBUF')																								
<b>Programming Notes</b>																											
<ul style="list-style-type: none"> <li>• For surface types other than SURFTYPE_BUFFER or STRBUF The Width specified by this field must be less than or equal to the surface pitch (specified in bytes via the Surface Pitch field).</li> <li>• For cube maps, Width must be set equal to the Height.</li> <li>• For MONO8 textures, Width must be a multiple of 32 texels.</li> <li>• The <b>Width</b> of a render target must be the same as the <b>Width</b> of the other render target(s) and the depth buffer (defined in 3DSTATE_DEPTH_BUFFER), unless <b>Surface Type</b> is SURFTYPE_1D or SURFTYPE_2D with <b>Depth</b> = 0 (non-array) and <b>LOD</b> = 0 (non-mip mapped).</li> <li>• The <b>Width</b> of a render target with YUV surface format must be a multiple of 2.</li> <li>• For SURFTYPE_BUFFER: The low two bits of this field must be 11 if the Surface Format is RAW (the size of the buffer must be a multiple of 4 bytes).</li> </ul>																											
<p>If <b>Surface Format</b> is PLANAR*, this field must be a multiple of 4</p>																											
<p>If any geometry is drawn inside this square it will be copied to column X=2 and X=3 (arrangement on Y position will stay the same). If any geometry exceeds the boundaries of this 2x2 region it will be drawn normally. The issue also only occurs if the surface has TileMode != Linear</p>																											

RENDER_SURFACE_STATE			
3	31:21	<b>Depth</b>	
		Format:	U11-1
This field specifies the total number of levels, minus 1, for a volume texture or the number of array elements, minus 1, allowed to be accessed starting at the <b>Minimum Array Element</b> for arrayed surfaces. If the volume texture is MIP-mapped, this field specifies the depth of the base MIP level. For buffers, this field specifies a portion of the buffer size.			
Value	Name	Description	Exists If
[0,2047]		number of array elements - 1	[SurfaceType] == 'SURFTYPE_1D'
[0,2047]		number of array elements - 1	[SurfaceType] == 'SURFTYPE_2D'
[0,2047]		depth of surface - 1 (z/r dimension)	[SurfaceType] == 'SURFTYPE_3D'
[0,340]		number of array elements - 1 [see programming notes for range]	[SurfaceType] == 'SURFTYPE_CUBE'
[0,1023]		contains bits [30:21] of the number of entries in the buffer - 1	([SurfaceType] == 'SURFTYPE_BUFFER') AND ([SurfaceFormat] == 'RAW')
[0,63]		contains bits [26:21] of the number of entries in the buffer - 1	([SurfaceType] == 'SURFTYPE_BUFFER') AND ([SurfaceFormat] != 'RAW')
[0,63]		contains bits [26:21] of the number of entries in the buffer - 1	[SurfaceType] == 'SURFTYPE_STRBUF'
Programming Notes			
The <b>Depth</b> of a render target must be the same as the <b>Depth</b> of the other render target(s) and of the depth buffer (defined in 3DSTATE_DEPTH_BUFFER).			
For SURFTYPE_CUBE: For Sampling Engine Surfaces, the range of this field is [0,340], indicating the number of cube array elements (equal to the number of underlying 2D array elements divided by 6). For other surfaces, this field must be zero.			
For SURFTYPE_BUFFER: The range of this field is [0,63] unless the Surface Format is RAW and Surface Ptich is 1 byte.			
For SURFTYPE_1D, 2D, and CUBE: The range of this field is reduced by one for each increase from zero of <b>Minimum Array Element</b> . For example, if <b>Minimum Array Element</b> is set to 1024 on a 2D surface, the range of this field is reduced to [0,1023].			
20		<b>Reserved</b>	
		Project:	BDW
		Format:	MBZ
19		<b>Reserved</b>	
		Project:	BDW
		Format:	MBZ
18		<b>Reserved</b>	
		Project:	BDW
		Format:	MBZ

		<b>RENDER_SURFACE_STATE</b>	
17:0	<b>Surface Pitch</b>	Format:	U18-1 Pitch in #Bytes
Surface Pitch Range:			
<ul style="list-style-type: none"> <li>• For surfaces of type SURFTYPE_BUFFER: [0,2047] -&gt; [1B, 2048B]</li> <li>• For surfaces of type SURFTYPE_STRBUF: [0,2047] -&gt; [1B, 2048B]</li> <li>• For other linear surfaces: [0, 262143] -&gt; [1B, 256KB]</li> <li>• For X-tiled surface: [511, 262143] -&gt; [512B, 256KB] = [1 tile, 512 tiles]</li> <li>• For Y-tiled surfaces: [127, 262143]-&gt;[128B, 256KB] = [1 tile, 2048 tiles]</li> <li>• For W-tiled surfaces: [127, 262143]-&gt;[128B, 256KB] = [1 tile, 2048 tiles]</li> <li>• For TileYF and TileYS surfaces, the range is dependent on the Cu parameter (refer to <i>Memory Data Formats</i> section for the definition of the Cu parameter depending on the case). The range in bytes is <math>[2^{Cu}-1,262143]</math> -&gt; <math>[(2^{Cu})B,256KB]</math> = [1 tile, 256KB/(2<sup>Cu</sup>) tiles]</li> </ul>			
<p>This field specifies the surface pitch in (#Bytes - 1).</p> <p>For surfaces of type SURFTYPE_BUFFER and SURFTYPE_STRBUF, this field indicates the size of the structure.</p>			
<b>Programming Notes</b>			
<ul style="list-style-type: none"> <li>• For linear <i>render target</i> surfaces and surfaces accessed with the typed data port messages, the pitch must be a multiple of the element size for non-YUV surface formats. Pitch must be a multiple of 2 * element size for YUV surface formats.</li> <li>• For untyped data port messages, which are only supported with <b>Surface Type</b> SURFTYPE_BUFFER, the pitch is ignored and assumed to be 1 byte.</li> <li>• For linear surfaces with <b>Surface Type</b> of SURFTYPE_STRBUF, the pitch must be a multiple of 4 bytes.</li> <li>• For linear surfaces with <b>Surface Type</b> of SURFTYPE_BUFFER and <b>Surface Format</b> RAW, the pitch must be 1 byte.</li> <li>• For other linear surfaces, the pitch can be any multiple of bytes.</li> <li>• For tiled surfaces, the pitch must be a multiple of the tile width.</li> </ul>			
<p>If the surface is a stencil buffer (and thus has <b>Tile Mode</b> set to TILEMODE_WMAJOR), the pitch must be set to 2x the value computed based on width, as the stencil buffer is stored with two rows interleaved. For details on the separate stencil buffer storage format in memory, see GPU Overview (vol1a), Memory Data Formats, Surface Layout, 2D Surfaces, Stencil Buffer Layout (section 8.20.4.8).</p>			
4	31	<b>Reserved</b>	
Project:	BDW		
Exists If:	[Surface Type] != 'SURFTYPE_STRBUF'		
Format:	MBZ		

## RENDER\_SURFACE\_STATE

30:29

### Render Target And Sample Unorm Rotation

Exists If:	[Surface Type] != 'SURFTYPE_STRBUF'
------------	-------------------------------------

**For Render Target Surfaces:** This field specifies the rotation of this render target surface when being written to memory.

**For Other Surfaces:** This field is ignored.

Value	Name	Description
0h	0DEG	No rotation (0 degrees)
1h	90DEG	Rotate by 90 degrees
3h	270DEG	Rotate by 270 degrees

### Programming Notes

#### Programming Notes for Render Target Surfaces only

- Rotation is not supported for render targets of any type other than simple, non-mipmapped, non-array 2D surfaces. The surface must be using tiled with X major.
- Width** and **Height** fields apply to the dimensions of the surface before rotation.
- For 90 and 270 degree rotated surfaces, the **Height** (rather than the **Width**) must be less than or equal to the **Surface Pitch** (specified in bytes).
- For 90 and 270 degree rotated surfaces, the actual **Height** and **Width** of the surface in pixels (not the field value which is decremented) must both be even.

Rotation is supported only for surfaces with the following surface formats: B5G6R5\_UNORM, B5G6R5\_UNORM\_SRGB, R8G8B8A8\_UNORM, R8G8B8A8\_UNORM\_SRGB, B8G8R8[A|X]8\_UNORM, B8G8R8[A|X]8\_UNORM\_SRGB, B10G10R10[A|X]2\_UNORM, B10G10R10A2\_UNORM\_SRGB, R10G10B10A2\_UNORM, R10G10B10A2\_UNORM\_SRGB, R16G16B16A16\_FLOAT, R16G16B16X16\_FLOAT

28:18

### Minimum Array Element

Exists If:	[Surface Type] != 'SURFTYPE_STRBUF'
Format:	U11

17:7

### Render Target View Extent

Exists If:	[Surface Type] != 'SURFTYPE_STRBUF'
Format:	U11-1

Range [0,2047] to indicate extent of [1,2048]

**For Render Target and Typed Dataport 3D Surfaces:**

This field indicates the extent of the accessible 'R' coordinates minus 1 on the LOD currently being rendered to.

**For Render Target and Typed Dataport 1D and 2D Surfaces:**

This field must be set to the same value as the Depth field.

**For Other Surfaces:**

This field is ignored.

## RENDER\_SURFACE\_STATE

		<b>Multisampled Surface Storage Format</b>																
	6	<table border="1"> <tr> <td>Exists If:</td> <td>[Surface Type] != 'SURFTYPE_STRBUF'</td> </tr> </table> <p>This field indicates the storage format of the multisampled surface.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>MSS</td> <td>Multisampled surface was/is rendered as a render target</td> </tr> <tr> <td>1h</td> <td>DEPTH_STENCIL</td> <td>Multisampled surface was rendered as a depth or stencil buffer</td> </tr> </tbody> </table>	Exists If:	[Surface Type] != 'SURFTYPE_STRBUF'	Value	Name	Description	0h	MSS	Multisampled surface was/is rendered as a render target	1h	DEPTH_STENCIL	Multisampled surface was rendered as a depth or stencil buffer					
Exists If:	[Surface Type] != 'SURFTYPE_STRBUF'																	
Value	Name	Description																
0h	MSS	Multisampled surface was/is rendered as a render target																
1h	DEPTH_STENCIL	Multisampled surface was rendered as a depth or stencil buffer																
		<b>Programming Notes</b>																
		<ul style="list-style-type: none"> <li>• All multisampled render target surfaces must have this field set to MSFMT_MSS</li> <li>• IF this field is MSFMT_DEPTH_STENCIL, the only sampling engine messages allowed are "ld2dms", "resinfo", and "sampleinfo".</li> <li>• This field is ignored if <b>Number of Multisamples</b> is MULTISAMPLECOUNT_1</li> </ul>																
	5:3	<b>Number of Multisamples</b>																
		<table border="1"> <tr> <td>Exists If:</td> <td>[Surface Type] != 'SURFTYPE_STRBUF'</td> </tr> </table> <p>This field indicates the number of multisamples on the surface.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>MULTISAMPLECOUNT_1</td> </tr> <tr> <td>1h</td> <td>MULTISAMPLECOUNT_2</td> </tr> <tr> <td>2h</td> <td>MULTISAMPLECOUNT_4</td> </tr> <tr> <td>3h</td> <td>MULTISAMPLECOUNT_8</td> </tr> <tr> <td>4h</td> <td>Reserved</td> </tr> <tr> <td>5h-7h</td> <td>Reserved</td> </tr> </tbody> </table>	Exists If:	[Surface Type] != 'SURFTYPE_STRBUF'	Value	Name	0h	MULTISAMPLECOUNT_1	1h	MULTISAMPLECOUNT_2	2h	MULTISAMPLECOUNT_4	3h	MULTISAMPLECOUNT_8	4h	Reserved	5h-7h	Reserved
Exists If:	[Surface Type] != 'SURFTYPE_STRBUF'																	
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2h	MULTISAMPLECOUNT_4																	
3h	MULTISAMPLECOUNT_8																	
4h	Reserved																	
5h-7h	Reserved																	
		<b>Programming Notes</b>																
		<p>If this field is any value other than MULTISAMPLECOUNT_1, the <b>Surface Type</b> must be SURFTYPE_2D. This field must be set to MULTISAMPLECOUNT_1 unless the surface is a Sampling Engine surface or Render Target surface.</p> <p>If this field is any value other than MULTISAMPLECOUNT_1, Surface Min LOD, Mip Count / LOD, and Resource Min LOD must be set to zero.</p>																
	31:0	<b>Reserved</b>																
		<table border="1"> <tr> <td>Exists If:</td> <td>[Surface Type] == 'SURFTYPE_STRBUF'</td> </tr> </table>	Exists If:	[Surface Type] == 'SURFTYPE_STRBUF'														
Exists If:	[Surface Type] == 'SURFTYPE_STRBUF'																	
		Format: MBZ																

RENDER_SURFACE_STATE											
	2:0	<b>Multisample Position Palette Index</b>									
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Exists If:</td><td>[Surface Type] != 'SURFTYPE_STRBUF'</td></tr> </table> <p>This field indicates the index into the sample position palette that the multisampled surface is using. This field is only used as a return value for the sampleinfo message, and is otherwise not used by hardware.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>[0,7]</td><td></td></tr> </tbody> </table>	Project:	BDW	Exists If:	[Surface Type] != 'SURFTYPE_STRBUF'	Value	Name	[0,7]		
Project:	BDW										
Exists If:	[Surface Type] != 'SURFTYPE_STRBUF'										
Value	Name										
[0,7]											
5	31:25	<b>X Offset</b>									
		<table border="1"> <tr> <td>Format:</td><td>PixelFormat[8:2]</td></tr> </table> <p>This field specifies the horizontal offset in pixels from the <b>Surface Base Address</b> to the start (origin) of the surface.</p> <p>This field effectively loosens the alignment restrictions on the origin of tiled surfaces. Previously, tiled surface origin was (by definition) located at the base address, and thus needed to satisfy the 4KB base address alignment restriction. Now the origin can be specified at a finer (4-wide x 4-high pixel) resolution.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>[0,508]</td><td></td><td>In multiples of 4 (low 2 bits missing)</td></tr> </tbody> </table>	Format:	PixelFormat[8:2]	Value	Name	Description	[0,508]		In multiples of 4 (low 2 bits missing)	
Format:	PixelFormat[8:2]										
Value	Name	Description									
[0,508]		In multiples of 4 (low 2 bits missing)									
		<b>Programming Notes</b>									
		<ul style="list-style-type: none"> <li>For linear surfaces, this field must be zero.</li> <li>For surfaces accessed with the <i>Data Port Media Block Read/Write</i> message, the pixel size is assumed to be 32 bits in width.</li> <li>For surfaces accessed with the <b>Data Port Transpose Read message</b>, the pixel size is assumed to be 32 bits in width.</li> <li>For <b>Surface Format</b> with other than 8, 16, 32, 64, or 128 bits per pixel, this field must be zero.</li> <li>If <b>Render Target Rotation</b> is set to other than RTROTATE_0DEG, this field must be zero.</li> <li>If <b>Surface Type</b> not SURFTYPE_2D, this field must be zero.</li> <li>If <b>MIP Count</b> is not zero, this field must be zero.</li> <li>If <b>Number of Multisamples</b> is not MULTISAMPLECOUNT_1, this field must be zero.</li> <li>If <b>Surface Array</b> is enabled, this field must be zero.</li> <li>If <b>Auxiliary Surface Mode</b> is not AUX_NONE, this field must be zero.</li> <li>If <b>Surface Vertical Alignment</b> is VALIGN_8, this field must be a multiple of 8.</li> <li>For <b>Surface Format</b> with 8 bits per element, this field must be a multiple of 16.</li> <li>For <b>Surface Format</b> with 16 bits per element, this field must be a multiple of 8.</li> </ul>									
		This field must be zero if Surface Format is PLANAR*.									
	24	<b>Reserved</b>									
		<table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ							
Format:	MBZ										

<b>RENDER_SURFACE_STATE</b>											
		23:21									
<b>Y Offset</b> <table border="1"> <tr> <td>Format:</td><td>RowOffset[4:2]</td></tr> </table> <p>This field specifies the vertical offset in rows from the <b>Surface Base Address</b> to the start of the surface. (See additional description in the <b>X Offset</b> field.)</p>		Format:	RowOffset[4:2]								
Format:	RowOffset[4:2]										
<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>[0,28]</td><td></td><td>In multiples of 4 (low two bits missing)</td></tr> </tbody> </table>			Value	Name	Description	[0,28]		In multiples of 4 (low two bits missing)			
Value	Name	Description									
[0,28]		In multiples of 4 (low two bits missing)									
<b>Programming Notes</b> <ul style="list-style-type: none"> <li>For linear surfaces, this field must be zero.</li> <li>For render targets in which the <b>Render Target Array Index</b> is not zero, this field must be zero.</li> <li>For <b>Surface Format</b> with other than 8, 16, 32, 64, or 128 bits per pixel, this field must be zero.</li> <li>If <b>Render Target Rotation</b> is set to other than RTROTATE_0DEG, this field must be zero.</li> <li>If <b>Surface Type</b> not SURFTYPE_2D, this field must be zero.</li> <li>If <b>MIP Count</b> is not zero, this field must be zero.</li> <li>If <b>Number of Multisamples</b> is not MULTISAMPLECOUNT_1, this field must be zero.</li> <li>If <b>Surface Array</b> is enabled, this field must be zero.</li> <li>If <b>Auxiliary Surface Mode</b> is not AUX_NONE, this field must be zero.</li> </ul>											
This field must be zero if <b>Surface Format</b> is PLANAR*.											
		20									
<b>EWA Disable For Cube</b> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>Disable</td></tr> </table> <p>Specifies if EWA mode for LOD quality improvement needs to be disabled for cube maps.</p>		Project:	BDW	Format:	Disable						
Project:	BDW										
Format:	Disable										
<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0h</td><td>Enable [<b>Default</b>]</td><td>EWA is enabled for cube maps</td></tr> <tr> <td>1h</td><td>Disable</td><td>EWA is disabled for cube maps</td></tr> </tbody> </table>			Value	Name	Description	0h	Enable [ <b>Default</b> ]	EWA is enabled for cube maps	1h	Disable	EWA is disabled for cube maps
Value	Name	Description									
0h	Enable [ <b>Default</b> ]	EWA is enabled for cube maps									
1h	Disable	EWA is disabled for cube maps									
<b>Programming Notes</b> <p>This field indicates if EWA mode for LOD quality improvement needs to be disabled for cube maps. By default EWA would be on for cube maps hence this field must be 0. If there is any spec violation seen with EWA on cube maps then this field must be set to 1 to disable EWA for cubes.</p>											
		19:18									
<b>Reserved</b> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>		Project:	BDW	Format:	MBZ						
Project:	BDW										
Format:	MBZ										

RENDER_SURFACE_STATE													
	17:16	<b>Reserved</b>											
		<table border="1"> <tr> <td>Project:</td><td colspan="2">BDW</td></tr> <tr> <td>Format:</td><td colspan="2">MBZ</td></tr> </table>			Project:	BDW		Format:	MBZ				
Project:	BDW												
Format:	MBZ												
	15	<b>Reserved</b>											
		<table border="1"> <tr> <td>Project:</td><td colspan="2">BDW</td></tr> <tr> <td>Format:</td><td colspan="2">MBZ</td></tr> </table>			Project:	BDW		Format:	MBZ				
Project:	BDW												
Format:	MBZ												
	14	<b>Coherency Type</b> Specifies the type of coherency maintained for this surface.											
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0h</td><td>GPU coherent</td><td>Surface memory is kept coherent with GPU threads using GPU read/write ordering rules. Surface memory is backed by system memory but is not kept coherent with CPU (LLC).</td></tr> <tr> <td>1h</td><td>IA coherent</td><td>Surface memory is kept coherent with CPU (LLC).</td></tr> </tbody> </table>			Value	Name	Description	0h	GPU coherent	Surface memory is kept coherent with GPU threads using GPU read/write ordering rules. Surface memory is backed by system memory but is not kept coherent with CPU (LLC).	1h	IA coherent	Surface memory is kept coherent with CPU (LLC).
Value	Name	Description											
0h	GPU coherent	Surface memory is kept coherent with GPU threads using GPU read/write ordering rules. Surface memory is backed by system memory but is not kept coherent with CPU (LLC).											
1h	IA coherent	Surface memory is kept coherent with CPU (LLC).											
		<b>Programming Notes</b>											
		This field may optionally be 1 (IA coherent) for messages sent to SFID_DP_DC0 or SFID_DP_DC1 or SFID_DP_DC2. This field is typically set to 0 (GPU coherent) if the context is operating in a non-SVM legacy mode (for example, Ring Buffer or a Execlist using 32-bit Virtual Address Legacy Context PPGTT32).											
	13:12	<b>Reserved</b>											
		<table border="1"> <tr> <td>Format:</td><td colspan="2">MBZ</td></tr> </table>			Format:	MBZ							
Format:	MBZ												
	11:8	<b>Reserved</b>											
		<table border="1"> <tr> <td>Project:</td><td colspan="2">BDW</td></tr> <tr> <td>Format:</td><td colspan="2">MBZ</td></tr> </table>			Project:	BDW		Format:	MBZ				
Project:	BDW												
Format:	MBZ												
	7:4	<b>Surface Min LOD</b> <table border="1"> <tr> <td>Format:</td><td colspan="2">U4 In LOD Units</td></tr> </table>			Format:	U4 In LOD Units							
Format:	U4 In LOD Units												
		<b>For Sampling Engine and Typed Surfaces:</b> This field indicates the most detailed LOD that can be accessed as part of this surface. This field is added to the delivered LOD ( <i>sample_l</i> , <i>ld</i> , or <i>resinfo</i> message types) before it is used to address the surface.											
		<b>For Other Surfaces:</b> This field is ignored.											
		<b>Programming Notes</b>											
		This field must be zero if the <b>Surface Format</b> is MONO8											

## RENDER\_SURFACE\_STATE

	3:0	<p><b>MIP Count / LOD</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 15%;">Format:</td><td><b>Sampling Engine and Typed Surfaces:</b> U4 in (LOD units - 1) <b>Render Target Surfaces:</b> U4 in LOD units</td></tr> <tr> <td>Range</td><td><b>Sampling Engine and Typed Surfaces:</b> [0,14] representing [1,15] MIP levels <b>Render Target Surfaces:</b> [0,14] representing LOD <b>Other Surfaces:</b> [0]</td></tr> </table> <p><b>For Sampling Engine and Typed Surfaces:</b> This field indicates the number of MIP levels allowed to be accessed starting at <b>Surface Min LOD</b>, which must be less than or equal to the number of MIP levels actually stored in memory for this surface. For sample* messages, the mip map access is clamped to be between the mipmap specified by the integer bits of the Min LOD and the ceiling of the value specified here. For Id* messages, out-of-bounds behavior results for LODs outside of the range specified in this field.</p> <p><b>For Render Target Surfaces:</b> This field defines the MIP level that is currently being rendered into. This is the absolute MIP level on the surface and is not relative to the <b>Surface Min LOD</b> field, which is ignored for render target surfaces.</p> <p><b>For Other Surfaces:</b> This field is reserved : MBZ</p>	Format:	<b>Sampling Engine and Typed Surfaces:</b> U4 in (LOD units - 1) <b>Render Target Surfaces:</b> U4 in LOD units	Range	<b>Sampling Engine and Typed Surfaces:</b> [0,14] representing [1,15] MIP levels <b>Render Target Surfaces:</b> [0,14] representing LOD <b>Other Surfaces:</b> [0]		
Format:	<b>Sampling Engine and Typed Surfaces:</b> U4 in (LOD units - 1) <b>Render Target Surfaces:</b> U4 in LOD units							
Range	<b>Sampling Engine and Typed Surfaces:</b> [0,14] representing [1,15] MIP levels <b>Render Target Surfaces:</b> [0,14] representing LOD <b>Other Surfaces:</b> [0]							
		<p style="text-align: center;"><b>Programming Notes</b></p> <p>The <b>LOD</b> of a render target must be the same as the <b>LOD</b> of the other render target(s) and of the depth buffer (defined in 3DSTATE_DEPTH_BUFFER).</p> <p>For render targets with YUV surface formats, the <b>LOD</b> must be zero.</p> <p>For sampling engine surfaces with YCRCB* or PLANAR* surface format, <b>MIP Count</b> must be zero.</p>						
6	31	<p><b>Reserved</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 15%;">Exists If:</td><td>([Surface Format] != 'PLANAR')</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Exists If:	([Surface Format] != 'PLANAR')	Format:	MBZ		
Exists If:	([Surface Format] != 'PLANAR')							
Format:	MBZ							
	31	<p><b>Separate UV Plane Enable</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 15%;">Exists If:</td><td>([Surface Format] == 'PLANAR')</td></tr> <tr> <td>Format:</td><td>Enable</td></tr> </table> <p>If enabled, this field indicates that the U and V are present as separate planes. If disabled, the UV data is interleaved on a single plane.</p> <p style="text-align: center;"><b>Programming Notes</b></p> <p>This field must be disabled (separate UV planes are not supported).</p>	Exists If:	([Surface Format] == 'PLANAR')	Format:	Enable		
Exists If:	([Surface Format] == 'PLANAR')							
Format:	Enable							
	30	<p><b>Reserved</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 15%;">Project:</td><td>BDW</td></tr> <tr> <td>Exists If:</td><td>([Surface Format] == 'PLANAR')</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	BDW	Exists If:	([Surface Format] == 'PLANAR')	Format:	MBZ
Project:	BDW							
Exists If:	([Surface Format] == 'PLANAR')							
Format:	MBZ							

## RENDER SURFACE STATE

30:16	<p><b>Auxiliary Surface QPitch</b></p> <table border="1"> <tr> <td>Exists If:</td><td>([Surface Format] != 'PLANAR')</td></tr> <tr> <td>Format:</td><td>QPitch[16:2]</td></tr> </table> <p>This field specifies the distance in rows between array slices on the auxiliary surface.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>[4h,1FFFCh]</td><td></td><td>in multiples of 4 (low 2 bits missing)</td></tr> </tbody> </table> <p><b>Programming Notes</b></p> <p>This field must be set to an integer multiple of the <b>Surface Vertical Alignment</b></p> <p>Software must ensure that this field is set to a value sufficiently large such that the array slices in the auxiliary surface do not overlap. Refer to the Memory Data Formats section for information on how surfaces are stored in memory.</p> <p>For non-multisampled render target's auxiliary surface, MCS, QPitch must be computed with Horizontal Alignment = 256 and Surface Vertical Alignment = 128. These alignments are only for MCS buffer and not for associated render target.</p>	Exists If:	([Surface Format] != 'PLANAR')	Format:	QPitch[16:2]	Value	Name	Description	[4h,1FFFCh]		in multiples of 4 (low 2 bits missing)
Exists If:	([Surface Format] != 'PLANAR')										
Format:	QPitch[16:2]										
Value	Name	Description									
[4h,1FFFCh]		in multiples of 4 (low 2 bits missing)									
29:16	<p><b>X Offset for U or UV Plane</b></p> <table border="1"> <tr> <td>Exists If:</td><td>([Surface Format] == 'PLANAR')</td></tr> <tr> <td>Format:</td><td>U14</td></tr> </table> <p>This field specifies the horizontal offset in pixels from the <b>Surface Base Address</b> to the start (origin) of the U plane or interleaved UV plane, depending on the setting of <b>Separate UV Plane Enable</b>.</p> <p><b>Programming Notes</b></p> <p>This field must be a multiple of 4 (bits 1:0 MBZ).</p> <p><b>Auxiliary Surface Mode</b> is forced to AUX_NONE.</p>	Exists If:	([Surface Format] == 'PLANAR')	Format:	U14						
Exists If:	([Surface Format] == 'PLANAR')										
Format:	U14										
15	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table> <p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Exists If:</td><td>([Surface Format] == 'PLANAR')</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	BDW	Format:	MBZ	Project:	All	Exists If:	([Surface Format] == 'PLANAR')	Format:	MBZ
Project:	BDW										
Format:	MBZ										
Project:	All										
Exists If:	([Surface Format] == 'PLANAR')										
Format:	MBZ										
14:12	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Exists If:</td><td>([Surface Format] != 'PLANAR')</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Exists If:	([Surface Format] != 'PLANAR')	Format:	MBZ						
Exists If:	([Surface Format] != 'PLANAR')										
Format:	MBZ										

## RENDER\_SURFACE\_STATE

		<b>Auxiliary Surface Pitch</b>																																
	11:3	<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Exists If:</td><td>([Surface Format] != 'PLANAR')</td></tr> <tr> <td>Format:</td><td>U9-1 Pitch in #Tiles</td></tr> </table> <p>This field specifies the Auxiliary surface pitch in (#Tiles - 1).</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>[0, 511]</td><td></td><td>-&gt; [1 tile, 512 tiles]</td></tr> </tbody> </table>	Project:	BDW	Exists If:	([Surface Format] != 'PLANAR')	Format:	U9-1 Pitch in #Tiles	Value	Name	Description	[0, 511]		-> [1 tile, 512 tiles]																				
Project:	BDW																																	
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Format:	U9-1 Pitch in #Tiles																																	
Value	Name	Description																																
[0, 511]		-> [1 tile, 512 tiles]																																
	13:0	<b>Y Offset for U or UV Plane</b> <table border="1"> <tr> <td>Exists If:</td><td>([Surface Format] == 'PLANAR')</td></tr> <tr> <td>Format:</td><td>U14</td></tr> </table> <p>This field specifies the vertical offset in rows from the <b>Surface Base Address</b> to the start (origin) of the U plane or interleaved UV plane, depending on the setting of <b>Separate UV Plane Enable</b>.</p> <table border="1"> <tr> <td align="center" colspan="2"><b>Programming Notes</b></td></tr> </table> <p><b>Auxiliary Surface Mode</b> is forced to AUX_NONE.</p>	Exists If:	([Surface Format] == 'PLANAR')	Format:	U14	<b>Programming Notes</b>																											
Exists If:	([Surface Format] == 'PLANAR')																																	
Format:	U14																																	
<b>Programming Notes</b>																																		
	2:0	<b>Auxiliary Surface Mode</b> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Exists If:</td><td>([Surface Format] != 'PLANAR')</td></tr> <tr> <td>Format:</td><td>U3</td></tr> </table> <p>Specifies what type of surface the Auxiliary surface is. The Auxiliary surface has its own base address and pitch, but otherwise shares or overrides other fields set for the primary surface, detailed in the programming notes below.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0h</td><td>AUX_NONE</td><td>No Auxiliary surface is used</td></tr> <tr> <td>1h</td><td>AUX_MCS</td><td>The Auxiliary surfaces is an MCS (Multisample Control Surface)</td></tr> <tr> <td>2h</td><td>AUX_APPEND</td><td>The Auxiliary surface is an append buffer</td></tr> <tr> <td>3h</td><td>AUX_HIZ</td><td>The Auxiliary surface is a hierarchical depth buffer</td></tr> <tr> <td>4h</td><td>Reserved</td><td></td></tr> <tr> <td>5h</td><td>Reserved</td><td></td></tr> <tr> <td>6h-7h</td><td>Reserved</td><td></td></tr> </tbody> </table> <table border="1"> <tr> <td align="center" colspan="2"><b>Programming Notes</b></td></tr> </table> <p>The CCS and hierarchical depth Auxiliary surface shares <b>Height</b>, <b>Width</b>, <b>Depth</b>, <b>Surface Type</b>, <b>Surface Array</b>, <b>Surface Min LOD</b>, <b>MIP Count / LOD</b>, <b>Surface Object Control State</b>, <b>Resource Min LOD</b>, and <b>Minimum Array Element</b> with the primary surface. The hierarchical depth Auxiliary surface uses <b>Surface Horizontal Alignment</b> of 16, <b>Surface Vertical Alignment</b> of 8, regardless of the primary surface's values for these fields. <b>X &amp; Y Offset</b> are set to zero for the purpose of accessing the Auxiliary surface. If this field is set to AUX_HIZ, <b>Surface Format</b> must be one of the following: R32_FLOAT, R24_UNORM_X8_TYPELESS, or R16_UNORM, and the format must match the format used when the surface was used as a depth buffer (with R channel corresponding to D channel).</p>	Project:	BDW	Exists If:	([Surface Format] != 'PLANAR')	Format:	U3	Value	Name	Description	0h	AUX_NONE	No Auxiliary surface is used	1h	AUX_MCS	The Auxiliary surfaces is an MCS (Multisample Control Surface)	2h	AUX_APPEND	The Auxiliary surface is an append buffer	3h	AUX_HIZ	The Auxiliary surface is a hierarchical depth buffer	4h	Reserved		5h	Reserved		6h-7h	Reserved		<b>Programming Notes</b>	
Project:	BDW																																	
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4h	Reserved																																	
5h	Reserved																																	
6h-7h	Reserved																																	
<b>Programming Notes</b>																																		

## RENDER\_SURFACE\_STATE

		The CCS Auxiliary surface for non-multisampled render targets has Horizontal Alignment = 256 and Vertical alignment = 128.  If this field is set to AUX_HIZ, <b>Number of Multisamples</b> must be MULTISAMPLECOUNT_1, and Surface Type cannot be SURFTYPE_3D.				
7	31	<p><b>Red Clear Color</b></p> <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Format:</td> <td><b>Clear Color [BDW]</b> Enumerated Type</td> </tr> </table> <p><b>For Sampling Engine Multisampled Surfaces and Render Targets:</b> Specifies the clear value for the red channel.</p> <p><b>For Other Surfaces:</b> This field is ignored.</p>	Project:	BDW	Format:	<b>Clear Color [BDW]</b> Enumerated Type
Project:	BDW					
Format:	<b>Clear Color [BDW]</b> Enumerated Type					
	30	<p><b>Green Clear Color</b></p> <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Format:</td> <td><b>Clear Color [BDW]</b> Enumerated Type</td> </tr> </table> <p><b>For Sampling Engine Multisampled Surfaces and Render Targets:</b> Specifies the clear value for the green channel.</p> <p><b>For Other Surfaces:</b> This field is ignored.</p>	Project:	BDW	Format:	<b>Clear Color [BDW]</b> Enumerated Type
Project:	BDW					
Format:	<b>Clear Color [BDW]</b> Enumerated Type					
	29	<p><b>Blue Clear Color</b></p> <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Format:</td> <td><b>Clear Color [BDW]</b> Enumerated Type</td> </tr> </table> <p><b>For Sampling Engine Multisampled Surfaces and Render Targets:</b> Specifies the clear value for the blue channel.</p> <p><b>For Other Surfaces:</b> This field is ignored.</p>	Project:	BDW	Format:	<b>Clear Color [BDW]</b> Enumerated Type
Project:	BDW					
Format:	<b>Clear Color [BDW]</b> Enumerated Type					
	28	<p><b>Alpha Clear Color</b></p> <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Format:</td> <td><b>Clear Color [BDW]</b> Enumerated Type</td> </tr> </table> <p><b>For Sampling Engine Multisampled Surfaces and Render Targets:</b> Specifies the clear value for the alpha channel.</p> <p><b>For Other Surfaces:</b> This field is ignored.</p>	Project:	BDW	Format:	<b>Clear Color [BDW]</b> Enumerated Type
Project:	BDW					
Format:	<b>Clear Color [BDW]</b> Enumerated Type					
	27:25	<p><b>Shader Channel Select Red</b></p> <table border="1"> <tr> <td>Format:</td> <td><b>Shader Channel Select [BDW]</b> Enumerated Type</td> </tr> </table> <p>Specifies which surface channel is read or written in the Red shader channel.</p> <p><b>Programming Notes</b></p> <p>The Shader channel selects also define which shader channels are written to which surface</p>	Format:	<b>Shader Channel Select [BDW]</b> Enumerated Type		
Format:	<b>Shader Channel Select [BDW]</b> Enumerated Type					

## RENDER\_SURFACE\_STATE

		<p>channel. If the Shader channel select is SCS_ZERO or SCS_ONE then it is not written to the surface. If the shader channel select is SCS_RED it is written to the surface red channel and so on. If more than one shader channel select is set to the same surface channel only the first shader channel in RGBA order will be written. Each shader channel select must be set to the same surface channel (R = SCS_RED, G = SCS_GREEN, B = SCS_BLUE, A = SCS_ALPHA) if the surface is accessed via the sampler's sample_unorm* or sample_8x8 messages.</p> <p>The Shader Channel Select fields do not affect the following sampling engine message types: resinfo, sampleinfo, LOD, and ld_mcs. These messages behave as if each Shader Channel Select is set to the same color surface channel.</p> <p>For the sampling engine <i>gather4*</i> messages, the Gather4 Source Channel Select field in the message header defines which channel's Shader Channel Select is used to select the surface channel to be sampled. Other Shader Channel Select fields are ignored.</p> <p>For the sampling engine <i>sample*_c</i> and <i>gather4*_c</i> messages, the compare operation always occurs on the red channel from the surface regardless of the setting of the Shader Channel Select fields.</p> <p>For Render Target, Red, Green and Blue Shader Channel Selects MUST be such that only valid components can be swapped i.e. only change the order of components in the pixel. Any other values for these Shader Channel Select fields are not valid for Render Targets. This also means that there MUST not be multiple shader channels mapped to the same RT channel.</p> <p>When multiple Channel selects have the same value and shader channel is disabled, disable channel writes 0s to memory. This behavior does not match with Data Port message via HDC.</p>		
24:22	<b>Shader Channel Select Green</b>	<table border="1" style="width: 100%;"> <tr> <td style="width: 10%;">Format:</td> <td><b>Shader Channel Select [BDW]</b> Enumerated Type</td> </tr> </table> <p>See <b>Shader Channel Select Red</b> for details.</p>	Format:	<b>Shader Channel Select [BDW]</b> Enumerated Type
Format:	<b>Shader Channel Select [BDW]</b> Enumerated Type			
21:19	<b>Shader Channel Select Blue</b>	<table border="1" style="width: 100%;"> <tr> <td style="width: 10%;">Format:</td> <td><b>Shader Channel Select [BDW]</b> Enumerated Type</td> </tr> </table> <p>See <b>Shader Channel Select Red</b> for details.</p>	Format:	<b>Shader Channel Select [BDW]</b> Enumerated Type
Format:	<b>Shader Channel Select [BDW]</b> Enumerated Type			

RENDER_SURFACE_STATE			
18:16	<p><b>Shader Channel Select Alpha</b></p> <table border="1"> <tr> <td>Format:</td><td><b>Shader Channel Select [BDW]</b> Enumerated Type</td></tr> </table> <p>See <b>Shader Channel Select Red</b> for details.</p>	Format:	<b>Shader Channel Select [BDW]</b> Enumerated Type
Format:	<b>Shader Channel Select [BDW]</b> Enumerated Type		
	<p align="center"><b>Programming Notes</b></p> <p><b>Shader Channel Select Alpha</b> must be set to SCS_ONE for the following formats when sampling (not reading via data port):</p> <p>BC6H_SF16  BC6H_UF16  R32G32B32_FLOAT  R11G11B10_FLOAT  L32X32_FLOAT  PLANAR_420_8  ETC1_RGB8  ETC2_RGB8  EAC_R11  EAC_RG11  EAC_SIGNED_R11  EAC_SIGNED_RG11  ETC2_SRGB8  R8G8B8_UNORM_SRGB  R8G8B8_UNORM  R8G8B8_SNORM  R8G8B8_UINT  R8G8B8_SINT  R16G16B16_FLOAT  R16G16B16_UNORM  R16G16B16_SNORM  R16G16B16_UINT  R16G16B16_SINT</p>		
	For Render Target, this field MUST be programmed to value = SCS_ALPHA.		
15:12	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ
Format:	MBZ		

## RENDER\_SURFACE\_STATE

		<b>Resource Min LOD</b>				
		<table border="1"> <tr> <td>Format:</td><td>U4.8 in LOD units</td></tr> </table>	Format:	U4.8 in LOD units		
Format:	U4.8 in LOD units					
<b>For Sampling Engine Surfaces:</b>						
This field indicates the most detailed LOD that is present in the resource underlying the surface. Refer to the "LOD Computation Pseudocode" section for the use of this field.						
<b>For Other Surfaces:</b>						
This field is ignored.						
<table border="1"> <thead> <tr> <th style="text-align: center;">Value</th><th style="text-align: center;">Name</th></tr> </thead> <tbody> <tr> <td>[0,14]</td><td></td></tr> </tbody> </table>			Value	Name	[0,14]	
Value	Name					
[0,14]						
<b>Programming Notes</b>						
This field must be zero if the <b>Surface Format</b> is MONO8						
This field must be zero if the <b>ChromaKey Enable</b> is enabled in the associated sampler.						
8..9	63:0	<b>Surface Base Address</b> <table border="1"> <tr> <td>Format:</td><td>GraphicsAddress[63:0]SurfaceBase</td></tr> </table> <p>Specifies the byte-aligned base address of the surface.</p>	Format:	GraphicsAddress[63:0]SurfaceBase		
Format:	GraphicsAddress[63:0]SurfaceBase					
<b>Programming Notes</b>						
<ul style="list-style-type: none"> <li>For SURFTYPE_BUFFER render targets, this field specifies the base address of first element of the surface. The surface is interpreted as a simple array of that single element type. The address must be naturally-aligned to the element size (e.g., a buffer containing R32G32B32A32_FLOAT elements must be 16-byte aligned).</li> <li>For SURFTYPE_BUFFER non-rendertarget surfaces, this field specifies the base address of the first element of the surface, computed in software by adding the surface base address to the byte offset of the element in the buffer. The base address must be aligned to element size.</li> <li>Linear depth buffer surface base addresses must be 64-byte aligned. Note that while render targets (color) can be SURFTYPE_BUFFER, depth buffers cannot.</li> <li>Mipmapped surfaces are stored in a "monolithic" (fixed) format, and only require a single address for the base MIP. All other MIPs are positioned relative to the base MIP.</li> <li>The Base Address for linear (non-tiled) render target surfaces and surfaces accessed with the typed surface read/write data port messages must be element-size aligned for Non-YUV surface formats, or a multiple of 2 element-sizes for YUV surface formats.</li> <li>Other linear (non-tiled) surfaces have no alignment requirements (byte alignment is sufficient).</li> <li>For tiled surfaces, the actual start of the surface can be offset from the Surface Base Address by the X Offset and Y Offset fields. Tiles are inherently page-aligned (4K or 64K).</li> </ul>						

RENDER_SURFACE_STATE							
<ul style="list-style-type: none"> <li>Certain message types used to access surfaces have more stringent alignment requirements. Please refer to the specific data-port message documentation for additional restrictions.</li> </ul>							
10..11	63:62	<b>Reserved</b>	<table border="1"> <tr> <td>Exists If:</td><td>([Surface Format] == 'PLANAR')</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Exists If:	([Surface Format] == 'PLANAR')	Format:	MBZ
Exists If:	([Surface Format] == 'PLANAR')						
Format:	MBZ						
61:48	<b>X Offset for V Plane</b>	<table border="1"> <tr> <td>Exists If:</td><td>([Surface Format] == 'PLANAR')</td></tr> <tr> <td>Format:</td><td>U14</td></tr> </table> <p>This field specifies the horizontal offset in pixels from the <b>Surface Base Address</b> to the start (origin) of the V plane.</p>	Exists If:	([Surface Format] == 'PLANAR')	Format:	U14	
Exists If:	([Surface Format] == 'PLANAR')						
Format:	U14						
<p style="text-align: center;"><b>Programming Notes</b></p> <p>This field must be a multiple of 4 (bits 1:0 MBZ).</p> <p>This field is ignored if <b>Separate UV Plane Enable</b> is disabled.</p>							
47:46	<b>Reserved</b>	<table border="1"> <tr> <td>Exists If:</td><td>([Surface Format] == 'PLANAR')</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Exists If:	([Surface Format] == 'PLANAR')	Format:	MBZ	
Exists If:	([Surface Format] == 'PLANAR')						
Format:	MBZ						
45:32	<b>Y Offset for V Plane</b>	<table border="1"> <tr> <td>Exists If:</td><td>([Surface Format] == 'PLANAR')</td></tr> <tr> <td>Format:</td><td>U14</td></tr> </table> <p>This field specifies the vertical offset in rows from the <b>Surface Base Address</b> to the start (origin) of the V plane.</p>	Exists If:	([Surface Format] == 'PLANAR')	Format:	U14	
Exists If:	([Surface Format] == 'PLANAR')						
Format:	U14						
<p style="text-align: center;"><b>Programming Notes</b></p> <p>This field is ignored if <b>Separate UV Plane Enable</b> is disabled.</p>							
31:21	<b>Auxiliary Table Index for Media Compressed Surface</b>	Exists If:	[Memory Compression Enable] == 1				
	<p>This field is valid only if Media Memory Compression is on for the surface (Memory Compression Enable == 1). In that case, the Auxiliary Surface Base address is never expected to be used and hence can be overloaded. This represents the 11 bit index into the table in memory which maps the surface to the auxiliary base address.</p>						
63:12	<b>Auxiliary Surface Base Address</b>	Exists If:	([Surface Format] != 'PLANAR') AND [Memory Compression Enable] == 0				
	<table border="1"> <tr> <td>Format:</td><td>GraphicsAddress[63:12]</td></tr> </table> <p>Specifies the 4kbyte-aligned base address of the Auxiliary surface associated with the primary surface specified in other SURFACE_STATE fields.</p>			Format:	GraphicsAddress[63:12]		
Format:	GraphicsAddress[63:12]						

<b>RENDER_SURFACE_STATE</b>			
	11	<b>Reserved</b>	
		Project:	BDW
		Format:	MBZ
	10	<b>Reserved</b>	
		Project:	BDW
		Format:	MBZ
	9:0	<b>Reserved</b>	
		Project:	BDW
		Format:	MBZ
	12		
	13	31:0	<b>Reserved</b>
			Project: BDW
			Exists If: [Auxiliary Surface Mode] == 'AUX_HIZ'
			Format: MBZ
	14	31:0	<b>Reserved</b>
			Exists If: [Auxiliary Surface Mode] == 'AUX_HIZ'
			Format: MBZ
	15	31:0	<b>Reserved</b>
			Project: BDW
			Exists If: [Auxiliary Surface Mode] == 'AUX_HIZ'
			Format: MBZ

## Render Data Port Message Types

MT_DP_RT - Render Data Port Message Types																			
Project: BDW Source: Render Cache DataPort Size (in bits): 5 Default Value: 0x0000000C																			
Lists all the Message Types in a Render Data Port Message Descriptor [18:14].																			
DWord	Bit	Description																	
0	4	<b>Reserved</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> <tr> <td colspan="2">Ignored</td></tr> </table>	Project:	All	Format:	MBZ	Ignored												
Project:	All																		
Format:	MBZ																		
Ignored																			
3:0	<b>Message Type</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>Enumeration</td></tr> <tr> <td colspan="2">Specifies type of message</td></tr> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> <tr> <td>0Ch</td><td>MT_RTW <b>[Default]</b></td><td>Render Target Write message</td></tr> <tr> <td>0Dh</td><td>MT_RTR</td><td>Render Target Read message</td></tr> <tr> <td>Others</td><td>Reserved</td><td>Ignored</td></tr> </table>	Project:	All	Format:	Enumeration	Specifies type of message		Value	Name	Description	0Ch	MT_RTW <b>[Default]</b>	Render Target Write message	0Dh	MT_RTR	Render Target Read message	Others	Reserved	Ignored
Project:	All																		
Format:	Enumeration																		
Specifies type of message																			
Value	Name	Description																	
0Ch	MT_RTW <b>[Default]</b>	Render Target Write message																	
0Dh	MT_RTR	Render Target Read message																	
Others	Reserved	Ignored																	

## RenderTargetIndex Message Header Control

<b>MHC_RT_RTI - Render Target Index Message Header Control</b>						
<b>DWord</b>	<b>Bit</b>	<b>Description</b>				
0	31:3	<b>Reserved</b>				
		<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Ignore</td> </tr> <tr> <td colspan="2">Ignored</td></tr> </table>	Project:	All	Format:	Ignore
Project:	All					
Format:	Ignore					
Ignored						
	2:0	<b>RenderTarget Index</b>				
		<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U3</td> </tr> </table> <p>Specifies the render target index that will be used to select blend state from BLEND_STATE.</p>	Project:	All	Format:	U3
Project:	All					
Format:	U3					

## Render Target Message Header

MH_RT - Render Target Message Header						
DWord	Bit	Description				
0.0	31:0	<p><b>RenderTarget Controls 0</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MHC_RT_C0</b></td></tr> </table> <p>Specifies controls for Render Target Write and Read messages.</p>	Project:	All	Format:	<b>MHC_RT_C0</b>
Project:	All					
Format:	<b>MHC_RT_C0</b>					
0.1	31:0	<p><b>Color Calculator State Pointer</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MHC_RT_CCSP</b></td></tr> </table> <p>For Render Target Write message, specifies the HWORD-aligned GeneralStateOffset for Color State. Ignored by Render Target Read message.</p>	Project:	All	Format:	<b>MHC_RT_CCSP</b>
Project:	All					
Format:	<b>MHC_RT_CCSP</b>					
0.2	31:0	<p><b>RenderTarget Index</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MHC_RT_RTI</b></td></tr> </table> <p>For Render Target Write message, specifies the render target index used to select blend state from BLEND_STATE. Ignored by Render Target Read message.</p>	Project:	All	Format:	<b>MHC_RT_RTI</b>
Project:	All					
Format:	<b>MHC_RT_RTI</b>					
0.3-0.4	63:0	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>Ignore</td></tr> </table> <p>Ignored</p>	Project:	All	Format:	Ignore
Project:	All					
Format:	Ignore					
0.5	31:0	<p><b>Color Code</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MHC_RT_CC</b></td></tr> </table> <p>Hardware uses to track synchronizing events and free resources on thread completion.</p>	Project:	All	Format:	<b>MHC_RT_CC</b>
Project:	All					
Format:	<b>MHC_RT_CC</b>					
0.6-0.7	63:0	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>Ignore</td></tr> </table> <p>Ignored</p>	Project:	All	Format:	Ignore
Project:	All					
Format:	Ignore					

## MH\_RT - Render Target Message Header

1.0-1.1	63:0	<b>Reserved</b>				
		<table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>Ignore</td></tr> </table> <p>Ignored</p>	Project:	All	Format:	Ignore
Project:	All					
Format:	Ignore					
1.2	31:0	<b>Subspan 0</b>				
		<table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MHC_RT_SUBSPAN</b></td></tr> </table> <p>Upper left corner of subspan 0</p>	Project:	All	Format:	<b>MHC_RT_SUBSPAN</b>
Project:	All					
Format:	<b>MHC_RT_SUBSPAN</b>					
1.3	31:0	<b>Subspan 1</b>				
		<table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MHC_RT_SUBSPAN</b></td></tr> </table> <p>Upper left corner of subspan 1</p>	Project:	All	Format:	<b>MHC_RT_SUBSPAN</b>
Project:	All					
Format:	<b>MHC_RT_SUBSPAN</b>					
1.4	31:0	<b>Subspan 2</b>				
		<table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MHC_RT_SUBSPAN</b></td></tr> </table> <p>Upper left corner of subspan 2</p>	Project:	All	Format:	<b>MHC_RT_SUBSPAN</b>
Project:	All					
Format:	<b>MHC_RT_SUBSPAN</b>					
1.5	31:0	<b>Subspan 3</b>				
		<table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MHC_RT_SUBSPAN</b></td></tr> </table> <p>Upper left corner of subspan 3</p>	Project:	All	Format:	<b>MHC_RT_SUBSPAN</b>
Project:	All					
Format:	<b>MHC_RT_SUBSPAN</b>					
1.6	31:0	<b>Reserved</b>				
		<table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>Ignore</td></tr> </table> <p>Ignored</p>	Project:	All	Format:	Ignore
Project:	All					
Format:	Ignore					
1.7	31:0	<b>Pixel Sample Enables</b>				
		<table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MHC_RT_PSM</b></td></tr> </table> <p>Pixel Sample Enables</p>	Project:	All	Format:	<b>MHC_RT_PSM</b>
Project:	All					
Format:	<b>MHC_RT_PSM</b>					

## RenderTarget Message Header Control

### MHC\_RT\_C0 - Render Target Message Header Control

Project: BDW Size (in bits): 32 Default Value: 0x00000000															
DWord	Bit	Description													
0	31	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Ignore</td> </tr> <tr> <td colspan="2">Ignored</td></tr> </table>	Project:	All	Format:	Ignore	Ignored								
Project:	All														
Format:	Ignore														
Ignored															
	30:27	<p><b>Viewport Index</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U4</td> </tr> </table> <p>For Render Target Write message, specifies the index of the viewport currently being used. Range = [0,15] Ignored by Render Target Read message.</p>	Project:	All	Format:	U4									
Project:	All														
Format:	U4														
	26:16	<p><b>Render Target Array Index</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U11</td> </tr> </table> <p>Specifies the array index to be used for the following surface types: SURFTYPE_1D: specifies the array index. Range = [0,511] SURFTYPE_2D: specifies the array index. Range = [0,511] SURFTYPE_3D: specifies the Z or R coordinate. Range = [0,2047] SURFTYPE_BUFFER: must be zero. SURFTYPE_CUBE: specifies the face identifier. Mapping (0,+x) (1,-x) (2,+y) (3,-y) (4,+z) (5,-z).</p> <p><b>Programming Notes</b></p> <p>The Render Target Array Index used by hardware for access to the Render Target is overridden with the Minimum Array Element defined in SURFACE_STATE if it is out of the range between Minimum Array Element and Depth. For cube surfaces, a depth value of 5 is used for this determination.</p>	Project:	All	Format:	U11									
Project:	All														
Format:	U11														
	15	<p><b>Front/Back Facing Polygon</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U1</td> </tr> </table> <p>Determines whether the polygon is front or back facing. Used by the render cache to determine which stencil test state to use.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Front facing</td> <td>All</td> </tr> <tr> <td>1h</td> <td>Back facing</td> <td>All</td> </tr> </tbody> </table>	Project:	All	Format:	U1	Value	Name	Description	0h	Front facing	All	1h	Back facing	All
Project:	All														
Format:	U1														
Value	Name	Description													
0h	Front facing	All													
1h	Back facing	All													

## MHC\_RT\_C0 - Render Target Message Header Control

	14	<b>Stencil Present to Render Target</b>				
		<table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>Enable</td></tr> </table>	Project:	All	Format:	Enable
Project:	All					
Format:	Enable					
		For Render Target Write message, indicates that computed stencil is included in the message. Must be zero for Render Target Read message.				
	13	<b>Source Depth Present to Render Target</b>				
		<table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>Enable</td></tr> </table>	Project:	All	Format:	Enable
Project:	All					
Format:	Enable					
		For Render Target Write Message, indicates that source depth data is included in the message. Must be zero for Render Target Read message.				
	12	<b>oMask to Render Target</b>				
		<table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>Enable</td></tr> </table>	Project:	All	Format:	Enable
Project:	All					
Format:	Enable					
		For Render Target Write message, indicates that oMask data is present in the message and is to be used to mask off samples. Must be zero for Render Target Read message.				
	11	<b>Source0 Alpha Present to Render Target</b>				
		<table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>Enable</td></tr> </table>	Project:	All	Format:	Enable
Project:	All					
Format:	Enable					
		For Render Target Write message, indicates that Source0 Alpha (aka o0.a) data is included in RTWrite message. If present, these alpha values are used as inputs to AlphaTest and AlphaToCoverage functions. This is required to meet the API rules when writing to multiple render targets (MRTs). Must be zero for Render Target Read message.				
		<b>Programming Notes</b>				
		This bit should not be set when write to RT0, though sending and using redundant alpha will provide the correct results (at lower performance). This bit is not supported on Dual-Source Blend message types, as source0 alpha is already included in those messages. This bit is not supported on replicated data message types.				
	10	<b>Reserved</b>				
		<table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>Ignore</td></tr> </table>	Project:	All	Format:	Ignore
Project:	All					
Format:	Ignore					
		Ignored				
	9	<b>Reserved</b>				
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>Ignore</td></tr> </table>	Project:	BDW	Format:	Ignore
Project:	BDW					
Format:	Ignore					
		Ignored				
	8:6	<b>Starting Sample Pair Index</b>				
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>U3</td></tr> </table>	Project:	BDW	Format:	U3
Project:	BDW					
Format:	U3					
		Indicates the index of the first sample pair of the dispatch. Range = [0,3]				

## MHC\_RT\_C0 - Render Target Message Header Control

	5:0	<b>Reserved</b>
		Project:
		Format:
		Ignored

## Replicated Pixel Render Target Data Payload Register

MDPR_RGBA - Replicated Pixel Render Target Data Payload Register						
DWord	Bit	Description				
0	31:0	<p><b>Red</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U32</td></tr> </table> <p>Specifies the value of all slots' red channel.</p>	Project:	All	Format:	U32
Project:	All					
Format:	U32					
1	31:0	<p><b>Green</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U32</td></tr> </table> <p>Specifies the value of all slots' green channel.</p>	Project:	All	Format:	U32
Project:	All					
Format:	U32					
2	31:0	<p><b>Blue</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U32</td></tr> </table> <p>Specifies the value of all slots' blue channel.</p>	Project:	All	Format:	U32
Project:	All					
Format:	U32					
3	31:0	<p><b>Alpha</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U32</td></tr> </table> <p>Specifies the value of all slots' alpha channel.</p>	Project:	All	Format:	U32
Project:	All					
Format:	U32					
4-7	127:0	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>Ignore</td></tr> </table> <p>Ignored</p>	Project:	All	Format:	Ignore
Project:	All					
Format:	Ignore					

## Replicated SIMD16 Render Target Data Payload

MDP_RTW_16REP - Replicated SIMD16 Render Target Data Payload						
DWord	Bit	Description				
0.0-0.7	255:0	<p><b>RGBA</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDPR_RGBA</b></td></tr> </table> <p>RGBA for all slots [15:0]</p>	Project:	All	Format:	<b>MDPR_RGBA</b>
Project:	All					
Format:	<b>MDPR_RGBA</b>					

## Reversed SIMD Mode 2 Message Descriptor Control Field

<b>MDC_SM2R - Reversed SIMD Mode 2 Message Descriptor Control Field</b>															
<b>DWord</b>	<b>Bit</b>	<b>Description</b>													
0	0	<b>SIMD Mode</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>Enumeration</td></tr> </table> <p>Specifies the SIMD mode of the message (number of slots processed)</p> <table border="1"> <thead> <tr> <th><b>Value</b></th><th><b>Name</b></th><th><b>Description</b></th></tr> </thead> <tbody> <tr> <td>00h</td><td>SIMD16</td><td>SIMD16</td></tr> <tr> <td>01h</td><td>SIMD8</td><td>SIMD8</td></tr> </tbody> </table>	Project:	All	Format:	Enumeration	<b>Value</b>	<b>Name</b>	<b>Description</b>	00h	SIMD16	SIMD16	01h	SIMD8	SIMD8
Project:	All														
Format:	Enumeration														
<b>Value</b>	<b>Name</b>	<b>Description</b>													
00h	SIMD16	SIMD16													
01h	SIMD8	SIMD8													

## RoundingPrecisionTable\_3\_Bits

RoundingPrecisionTable_3_Bits																						
DWord	Bit	Description																				
0	2:0	<p><b>Rounding Precision</b></p> <table border="1"> <tr> <td>Format:</td> <td>U3</td> </tr> <tr> <th>Value</th><th>Name</th></tr> <tr> <td>000b</td><td>+1/16</td></tr> <tr> <td>001b</td><td>+2/16</td></tr> <tr> <td>010b</td><td>+3/16</td></tr> <tr> <td>011b</td><td>+4/16</td></tr> <tr> <td>100b</td><td>+5/16</td></tr> <tr> <td>101b</td><td>+6/16</td></tr> <tr> <td>110b</td><td>+7/16</td></tr> <tr> <td>111b</td><td>+8/16</td></tr> </table>	Format:	U3	Value	Name	000b	+1/16	001b	+2/16	010b	+3/16	011b	+4/16	100b	+5/16	101b	+6/16	110b	+7/16	111b	+8/16
Format:	U3																					
Value	Name																					
000b	+1/16																					
001b	+2/16																					
010b	+3/16																					
011b	+4/16																					
100b	+5/16																					
101b	+6/16																					
110b	+7/16																					
111b	+8/16																					

## SOA SIMD8 Render Target Data Payload

<b>MDP_RTW_A8 - SOA SIMD8 Render Target Data Payload</b>						
<b>DWord</b>	<b>Bit</b>	<b>Description</b>				
0.0-0.7	255:0	<p><b>Source 0 Alpha</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW_SIMD8</b></td></tr> </table> <p>Slots [7:0] Source 0 Alpha</p>	Project:	All	Format:	<b>MDP_DW_SIMD8</b>
Project:	All					
Format:	<b>MDP_DW_SIMD8</b>					
1.0-1.7	255:0	<p><b>Red</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW_SIMD8</b></td></tr> </table> <p>Slots [7:0] Red</p>	Project:	All	Format:	<b>MDP_DW_SIMD8</b>
Project:	All					
Format:	<b>MDP_DW_SIMD8</b>					
2.0-2.7	255:0	<p><b>Green</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW_SIMD8</b></td></tr> </table> <p>Slots [7:0] Green</p>	Project:	All	Format:	<b>MDP_DW_SIMD8</b>
Project:	All					
Format:	<b>MDP_DW_SIMD8</b>					
3.0-3.7	255:0	<p><b>Blue</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW_SIMD8</b></td></tr> </table> <p>Slots [7:0] Blue</p>	Project:	All	Format:	<b>MDP_DW_SIMD8</b>
Project:	All					
Format:	<b>MDP_DW_SIMD8</b>					
4.0-4.7	255:0	<p><b>Alpha</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW_SIMD8</b></td></tr> </table> <p>Slots [7:0] Alpha</p>	Project:	All	Format:	<b>MDP_DW_SIMD8</b>
Project:	All					
Format:	<b>MDP_DW_SIMD8</b>					

## SOA SIMD16 Render Target Data Payload

<b>MDP_RTW_A16 - SOA SIMD16 Render Target Data Payload</b>						
<b>DWord</b>	<b>Bit</b>	<b>Description</b>				
0.0-0.7	255:0	<p><b>Source 0 Alpha[7:0]</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW SIMD8</b></td></tr> </table> <p>Slots [7:0] Source 0 Alpha</p>	Project:	All	Format:	<b>MDP_DW SIMD8</b>
Project:	All					
Format:	<b>MDP_DW SIMD8</b>					
1.0-1.7	255:0	<p><b>Source 0 Alpha[15:7]</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW SIMD8</b></td></tr> </table> <p>Slots [15:8] Source 0 Alpha</p>	Project:	All	Format:	<b>MDP_DW SIMD8</b>
Project:	All					
Format:	<b>MDP_DW SIMD8</b>					
2.0-2.7	255:0	<p><b>Red[7:0]</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW SIMD8</b></td></tr> </table> <p>Slots [7:0] Red</p>	Project:	All	Format:	<b>MDP_DW SIMD8</b>
Project:	All					
Format:	<b>MDP_DW SIMD8</b>					
3.0-3.7	255:0	<p><b>Red[15:8]</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW SIMD8</b></td></tr> </table> <p>Slots [15:8] Red</p>	Project:	All	Format:	<b>MDP_DW SIMD8</b>
Project:	All					
Format:	<b>MDP_DW SIMD8</b>					
4.0-4.7	255:0	<p><b>Green[7:0]</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW SIMD8</b></td></tr> </table> <p>Slots [7:0] Green</p>	Project:	All	Format:	<b>MDP_DW SIMD8</b>
Project:	All					
Format:	<b>MDP_DW SIMD8</b>					

<b>MDP_RTW_A16 - SOA SIMD16 Render Target Data Payload</b>						
5.0-5.7	255:0	<b>Green[15:8]</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW SIMD8</b></td></tr> </table> Slots [15:8] Green	Project:	All	Format:	<b>MDP_DW SIMD8</b>
Project:	All					
Format:	<b>MDP_DW SIMD8</b>					
6.0-6.7	255:0	<b>Blue[7:0]</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW SIMD8</b></td></tr> </table> Slots [7:0] Blue	Project:	All	Format:	<b>MDP_DW SIMD8</b>
Project:	All					
Format:	<b>MDP_DW SIMD8</b>					
7.0-7.7	255:0	<b>Blue[15:8]</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW SIMD8</b></td></tr> </table> Slots [15:8] Blue	Project:	All	Format:	<b>MDP_DW SIMD8</b>
Project:	All					
Format:	<b>MDP_DW SIMD8</b>					
8.0-8.7	255:0	<b>Alpha[7:0]</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW SIMD8</b></td></tr> </table> Slots [7:0] Alpha	Project:	All	Format:	<b>MDP_DW SIMD8</b>
Project:	All					
Format:	<b>MDP_DW SIMD8</b>					
9.0-9.7	255:0	<b>Alpha[15:8]</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW SIMD8</b></td></tr> </table> Slots [15:8] Alpha	Project:	All	Format:	<b>MDP_DW SIMD8</b>
Project:	All					
Format:	<b>MDP_DW SIMD8</b>					

## SAMPLER\_BORDER\_COLOR\_STATE

<b>SAMPLER_BORDER_COLOR_STATE</b>								
Project:	Pre-BDW							
Size (in bits):	128							
Default Value:	0x00000000, 0x00000000, 0x00000000, 0x00000000							
<b>Description</b>								
<p>The interpretation of the border color depends on the Texture Border Color Mode field in SAMPLER_STATE as follows:</p> <ul style="list-style-type: none"> <li>DX9 mode: The border color is 8-bit UNORM format, regardless of the surface format chosen. For surface formats with one or more channels missing (i.e. R5G6R5_UNORM is missing the alpha channel), the value from the border color, if selected, will be used even for the missing channels.</li> <li>DX10/OGL mode: the format of the border color depends on the format of the surface being sampled. If the map format is UINT, then the border color format is R32G32B32A32_UINT. If the map format is SINT, then the border color format is R32G32B32A32_SINT. Otherwise, the border color format is R32G32B32A32_FLOAT. For surface formats with one or more channels missing, the value from the border color is not used for the missing channels, resulting in these channels resulting in the overall default value (0 for colors and 1 for alpha) regardless of whether border color is chosen. The surface formats with "L" and "I" have special behavior with respect to the border color. The border color value used for the replicated channels (RGB for "L" formats and RGBA for "I" formats) comes from the red channel of border color. In these cases, the green and blue channels, and also alpha for "I", of the border color are ignored. The format of this state depends on the Texture Border Color Mode field.</li> </ul>								
<b>Programming Notes</b>								
<ul style="list-style-type: none"> <li>DX9 mode is not supported for surfaces with more than 16 bits in any channel, other than 32-bit float formats which are supported.</li> <li>The conditions under which this color is used depend on the <b>Surface Type</b> - 1D/2D/3D surfaces use the border color when the coordinates extend beyond the surface extent; cube surfaces use the border color for "empty" (disabled) faces.</li> <li>The border color itself is accessed through the texture cache hierarchy rather than the state cache hierarchy. Thus, if the border color is changed in memory, the texture cache must be invalidated and the state cache does not need to be invalidated.</li> <li>MAPFILTER_MONO: The border color is ignored. Border color is fixed at a value of 0 by hardware.</li> </ul>								
DWord	Bit	Description						
0	31:24	<p><b>Border Color Alpha</b></p> <table border="1"> <tr> <td>Exists If:</td><td>Structure[SAMPLER_STATE][Texture Border Color Mode] == 'DX9'</td></tr> <tr> <td>Format:</td><td>UNORM8</td></tr> <tr> <td colspan="2">Texture Border Color Mode = DX9</td></tr> </table>	Exists If:	Structure[SAMPLER_STATE][Texture Border Color Mode] == 'DX9'	Format:	UNORM8	Texture Border Color Mode = DX9	
Exists If:	Structure[SAMPLER_STATE][Texture Border Color Mode] == 'DX9'							
Format:	UNORM8							
Texture Border Color Mode = DX9								

<b>SAMPLER_BORDER_COLOR_STATE</b>						
	23:16	<b>Border Color Blue</b> <table border="1"> <tr> <td>Exists If:</td><td>Structure[SAMPLER_STATE][Texture Border Color Mode] == 'DX9'</td></tr> <tr> <td>Format:</td><td>UNORM8</td></tr> </table> <p>Texture Border Color Mode = DX9</p>	Exists If:	Structure[SAMPLER_STATE][Texture Border Color Mode] == 'DX9'	Format:	UNORM8
Exists If:	Structure[SAMPLER_STATE][Texture Border Color Mode] == 'DX9'					
Format:	UNORM8					
	15:8	<b>Border Color Green</b> <table border="1"> <tr> <td>Exists If:</td><td>Structure[SAMPLER_STATE][Texture Border Color Mode] == 'DX9'</td></tr> <tr> <td>Format:</td><td>UNORM8</td></tr> </table> <p>Texture Border Color Mode = DX9</p>	Exists If:	Structure[SAMPLER_STATE][Texture Border Color Mode] == 'DX9'	Format:	UNORM8
Exists If:	Structure[SAMPLER_STATE][Texture Border Color Mode] == 'DX9'					
Format:	UNORM8					
	31:0	<b>Border Color Red - (DX10/OGL)</b> <table border="1"> <tr> <td>Exists If:</td><td>Structure[SAMPLER_STATE][Texture Border Color Mode] == 'DX10/OGL'</td></tr> <tr> <td>Format:</td><td>IEEE_FP</td></tr> </table> <p>Texture Border Color Mode = DX10/OGL</p>	Exists If:	Structure[SAMPLER_STATE][Texture Border Color Mode] == 'DX10/OGL'	Format:	IEEE_FP
Exists If:	Structure[SAMPLER_STATE][Texture Border Color Mode] == 'DX10/OGL'					
Format:	IEEE_FP					
	7:0	<b>Border Color Red - (DX9)</b> <table border="1"> <tr> <td>Exists If:</td><td>Structure[SAMPLER_STATE][Texture Border Color Mode] == 'DX9'</td></tr> <tr> <td>Format:</td><td>UNORM8</td></tr> </table> <p>Texture Border Color Mode = DX9</p>	Exists If:	Structure[SAMPLER_STATE][Texture Border Color Mode] == 'DX9'	Format:	UNORM8
Exists If:	Structure[SAMPLER_STATE][Texture Border Color Mode] == 'DX9'					
Format:	UNORM8					
1	31:0	<b>Border Color Green</b> <table border="1"> <tr> <td>Format:</td><td>IEEE_FP</td></tr> </table> <p>Texture Border Color Mode = DX10/OGL</p>	Format:	IEEE_FP		
Format:	IEEE_FP					
2	31:0	<b>Border Color Blue</b> <table border="1"> <tr> <td>Format:</td><td>IEEE_FP</td></tr> </table> <p>Texture Border Color Mode = DX10/OGL</p>	Format:	IEEE_FP		
Format:	IEEE_FP					
3	31:0	<b>Border Color Alpha</b> <table border="1"> <tr> <td>Format:</td><td>IEEE_FP</td></tr> </table> <p>Texture Border Color Mode = DX10/OGL</p>	Format:	IEEE_FP		
Format:	IEEE_FP					

## SAMPLER\_INDIRECT\_STATE\_BORDER\_COLOR

### SAMPLER\_INDIRECT\_STATE\_BORDER\_COLOR

Project:	BDW
Size (in bits):	128
Default Value:	0x00000000, 0x00000000, 0x00000000, 0x00000000

This structure is a one version of the SAMPLER\_INDIRECT\_STATE structure, suitable for many needs.

An instance of this structure is pointed to by the **Indirect State Pointer** field in SAMPLER\_STATE.

The interpretation of the border color depends on the **Texture Border Color Mode** field in SAMPLER\_STATE as follows:

- In **DX9** mode, the border color is 8-bit UNORM format, regardless of the surface format chosen. For surface formats with one or more channels missing (i.e. R5G6R5\_UNORM is missing the alpha channel), the value from the border color, if selected, will be used even for the missing channels.
- In **DX10/OGL** mode, the format of the border color is R32G32B32A32\_FLOAT, R32G32B32A32\_SINT, or R32G32B32A32\_UINT, depending on the surface format chosen. For surface formats with one or more channels missing, the value from the border color is not used for the missing channels, resulting in these channels resulting in the overall default value (0 for colors and 1 for alpha) regardless of whether border color is chosen. The surface formats with "L" and "I" have special behavior with respect to the border color. The border color value used for the replicated channels (RGB for "L" formats and RGBA for "I" formats) comes from the *red* channel of border color. In these cases, the green and blue channels, and also alpha for "I", of the border color are ignored.

#### Programming Notes

- DX9 mode is not supported for surfaces with more than 16 bits in any channel, other than 32-bit float formats which are supported.
- The conditions under which this color is used depend on the **Surface Type** - 1D/2D/3D surfaces use the border color when the coordinates extend beyond the surface extent; cube surfaces use the border color for "empty" (disabled) faces.
- The border color itself is accessed through the texture cache hierarchy rather than the state cache hierarchy. Thus, if the border color is changed in memory, the texture cache must be invalidated and the state cache does not need to be invalidated.
- MAPFILTER\_MONO: The border color is ignored. Border color is fixed at a value of 0 by hardware.

DWord	Bit	Description
0	31:24	<b>Border Color Alpha As U8</b>
		Exists If: //Structure[SAMPLER_STATE][Texture Border Color Mode] == 'DX9' Format: U8
	23:16	<b>Border Color Blue As U8</b>
		Exists If: //Structure[SAMPLER_STATE][Texture Border Color Mode] == 'DX9' Format: U8

<b>SAMPLER_INDIRECT_STATE_BORDER_COLOR</b>			
	15:8	<b>Border Color Green As U8</b>	
		Exists If:	//Structure[SAMPLER_STATE][Texture Border Color Mode] == 'DX9'
		Format:	U8
	31:0	<b>Border Color Red As Float</b>	
		Exists If:	//Structure[SAMPLER_STATE][Texture Border Color Mode] == 'DX10/OGL' AND (Structure[RENDER_SURFACE_STATE][Surface Format]Property[IsFloat]==true'
		Format:	IEEE_Float
	31:0	<b>Border Color Red As U32</b>	
		Exists If:	//Structure[SAMPLER_STATE][Texture Border Color Mode] == 'DX10/OGL' AND (Structure[RENDER_SURFACE_STATE][Surface Format]Property[IsUnsigned]==true'
		Format:	U32
	31:0	<b>Border Color Red As S31</b>	
		Exists If:	//Structure[SAMPLER_STATE][Texture Border Color Mode] == 'DX10/OGL' AND (Structure[RENDER_SURFACE_STATE][Surface Format]Property[IsSigned]==true'
		Format:	S31
	7:0	<b>Border Color Red As U8</b>	
		Exists If:	//Structure[SAMPLER_STATE][Texture Border Color Mode] == 'DX9'
		Format:	U8
1	31:0	<b>Reserved</b>	
		Exists If:	//Structure[SAMPLER_STATE][Texture Border Color Mode] == 'DX9'
		Format:	MBZ
	31:0	<b>Border Color Green As S31</b>	
		Exists If:	//Structure[SAMPLER_STATE][Texture Border Color Mode] == 'DX10/OGL' AND (Structure[RENDER_SURFACE_STATE][Surface Format]Property[IsSigned]==true'
		Format:	S31
	31:0	<b>Border Color Green As U32</b>	
		Exists If:	//Structure[SAMPLER_STATE][Texture Border Color Mode] == 'DX10/OGL' AND (Structure[RENDER_SURFACE_STATE][Surface Format]Property[IsUnsigned]==true'
		Format:	U32
	31:0	<b>Border Color Green As Float</b>	
		Exists If:	//Structure[SAMPLER_STATE][Texture Border Color Mode] == 'DX10/OGL' AND (Structure[RENDER_SURFACE_STATE][Surface Format]Property[IsFloat]==true'
		Format:	IEEE_Float
2	31:0	<b>Reserved</b>	
		Exists If:	//Structure[SAMPLER_STATE][Texture Border Color Mode] == 'DX9'
		Format:	MBZ

<b>SAMPLER_INDIRECT_STATE_BORDER_COLOR</b>				
	31:0	<b>Border Color Blue As S31</b>		
		Exists If:	//Structure[SAMPLER_STATE][Texture Border Color Mode] == 'DX10/OGL' AND (Structure[RENDER_SURFACE_STATE][Surface Format]Property[IsSigned]=='true'	
		Format:	S31	
	31:0	<b>Border Color Blue As U32</b>		
		Exists If:	//Structure[SAMPLER_STATE][Texture Border Color Mode] == 'DX10/OGL' AND (Structure[RENDER_SURFACE_STATE][Surface Format]Property[IsUnsigned]=='true'	
		Format:	U32	
	31:0	<b>Border Color Blue As Float</b>		
		Exists If:	//Structure[SAMPLER_STATE][Texture Border Color Mode] == 'DX10/OGL' AND (Structure[RENDER_SURFACE_STATE][Surface Format]Property[IsFloat]=='true'	
		Format:	IEEE_Float	
3	31:0	<b>Reserved</b>		
		Exists If:	//Structure[SAMPLER_STATE][Texture Border Color Mode] == 'DX9'	
		Format:	MBZ	
	31:0	<b>Border Color Alpha As S31</b>		
		Exists If:	//Structure[SAMPLER_STATE][Texture Border Color Mode] == 'DX10/OGL' AND (Structure[RENDER_SURFACE_STATE][Surface Format]Property[IsSigned]=='true'	
		Format:	S31	
	31:0	<b>Border Color Alpha As U32</b>		
		Exists If:	//Structure[SAMPLER_STATE][Texture Border Color Mode] == 'DX10/OGL' AND (Structure[RENDER_SURFACE_STATE][Surface Format]Property[IsUnsigned]=='true'	
		Format:	U32	
	31:0	<b>Border Color Alpha As Float</b>		
		Exists If:	//Structure[SAMPLER_STATE][Texture Border Color Mode] == 'DX10/OGL' AND (Structure[RENDER_SURFACE_STATE][Surface Format]Property[IsFloat]=='true'	
		Format:	IEEE_Float	

## SAMPLER\_INDIRECT\_STATE

### SAMPLER\_INDIRECT\_STATE

Project:	BDW
Size (in bits):	512
Default Value:	0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000

Note: There are three variations of this structure, defined separately because their payloads have different lengths. Currently only SAMPLER\_INDIRECT\_STATE\_BORDER\_COLOR is fully defined.

This structure is pointed to by **Indirect State Pointer** (SAMPLER\_STATE).

The interpretation of the border color depends on the **Texture Border Color Mode** field in SAMPLER\_STATE as follows:

- In **DX9** mode, the border color is 8-bit UNORM format, regardless of the surface format chosen. For surface formats with one or more channels missing (i.e. R5G6R5\_UNORM is missing the alpha channel), the value from the border color, if selected, will be used *even for the missing channels*.
- In **DX10/OGL** mode, the format of the border color is R32G32B32A32\_FLOAT, R32G32B32A32\_SINT, or R32G32B32A32\_UINT, depending on the surface format chosen. For surface formats with one or more channels missing, the value from the border color is not used for the missing channels, resulting in these channels resulting in the overall default value (0 for colors and 1 for alpha) regardless of whether border color is chosen. The surface formats with "L" and "I" have special behavior with respect to the border color. The border color value used for the replicated channels (RGB for "L" formats and RGBA for "I" formats) comes from the *red* channel of border color. In these cases, the green and blue channels, and also alpha for "I", of the border color are ignored.

The format of this state depends on the **Texture Border Color Mode** field.

#### Programming Notes

- DX9 mode is not supported for surfaces with more than 16 bits in any channel, other than 32-bit float formats which are supported.
- The conditions under which this color is used depend on the **Surface Type** - 1D/2D/3D surfaces use the border color when the coordinates extend beyond the surface extent; cube surfaces use the border color for "empty" (disabled) faces.
- The border color itself is accessed through the texture cache hierarchy rather than the state cache hierarchy. Thus, if the border color is changed in memory, the texture cache must be invalidated and the state cache does not need to be invalidated.
- MAPFILTER\_MONO: The border color is ignored. Border color is fixed at a value of 0 by hardware.

DWord	Bit	Description						
0	31:24	<b>Border Color Alpha</b> <table border="1"> <tr> <td>Exists If:</td><td>//Structure[SAMPLER_STATE][Texture Border Color Mode] == 'DX9'</td></tr> <tr> <td>Format:</td><td>UNORM8</td></tr> <tr> <td colspan="2">Texture Border Color Mode = DX9</td></tr> </table>	Exists If:	//Structure[SAMPLER_STATE][Texture Border Color Mode] == 'DX9'	Format:	UNORM8	Texture Border Color Mode = DX9	
Exists If:	//Structure[SAMPLER_STATE][Texture Border Color Mode] == 'DX9'							
Format:	UNORM8							
Texture Border Color Mode = DX9								

SAMPLER_INDIRECT_STATE										
	23:16	<p><b>Border Color Blue</b></p> <table border="1"> <tr> <td>Exists If:</td><td>//Structure[SAMPLER_STATE][Texture Border Color Mode] == 'DX9'</td></tr> <tr> <td>Format:</td><td>UNORM8</td></tr> </table> <p>Texture Border Color Mode = DX9</p>	Exists If:	//Structure[SAMPLER_STATE][Texture Border Color Mode] == 'DX9'	Format:	UNORM8				
Exists If:	//Structure[SAMPLER_STATE][Texture Border Color Mode] == 'DX9'									
Format:	UNORM8									
	15:8	<p><b>Border Color Green</b></p> <table border="1"> <tr> <td>Exists If:</td><td>//Structure[SAMPLER_STATE][Texture Border Color Mode] == 'DX9'</td></tr> <tr> <td>Format:</td><td>UNORM8</td></tr> </table> <p>Texture Border Color Mode = DX9</p>	Exists If:	//Structure[SAMPLER_STATE][Texture Border Color Mode] == 'DX9'	Format:	UNORM8				
Exists If:	//Structure[SAMPLER_STATE][Texture Border Color Mode] == 'DX9'									
Format:	UNORM8									
	31:0	<p><b>Border Color Red</b></p> <table border="1"> <tr> <td>Exists If:</td><td>//Structure[SAMPLER_STATE][Texture Border Color Mode] == 'DX10/OGL'</td></tr> <tr> <td>Format:</td><td>SINT32 (2's complement) for all SINT surface formats</td></tr> <tr> <td>Format:</td><td>UINT32 for all UINT surface formats</td></tr> <tr> <td>Format:</td><td>IEEE_FP for all other surface formats</td></tr> </table> <p>Texture Border Color Mode = DX10/OGL</p>	Exists If:	//Structure[SAMPLER_STATE][Texture Border Color Mode] == 'DX10/OGL'	Format:	SINT32 (2's complement) for all SINT surface formats	Format:	UINT32 for all UINT surface formats	Format:	IEEE_FP for all other surface formats
Exists If:	//Structure[SAMPLER_STATE][Texture Border Color Mode] == 'DX10/OGL'									
Format:	SINT32 (2's complement) for all SINT surface formats									
Format:	UINT32 for all UINT surface formats									
Format:	IEEE_FP for all other surface formats									
	7:0	<p><b>Border Color Red</b></p> <table border="1"> <tr> <td>Exists If:</td><td>//Structure[SAMPLER_STATE][Texture Border Color Mode] == 'DX9'</td></tr> <tr> <td>Format:</td><td>UNORM8</td></tr> </table> <p>Texture Border Color Mode = DX9</p>	Exists If:	//Structure[SAMPLER_STATE][Texture Border Color Mode] == 'DX9'	Format:	UNORM8				
Exists If:	//Structure[SAMPLER_STATE][Texture Border Color Mode] == 'DX9'									
Format:	UNORM8									
1	31:0	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Exists If:</td><td>//Structure[SAMPLER_STATE][Texture Border Color Mode] == 'DX9'</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Exists If:	//Structure[SAMPLER_STATE][Texture Border Color Mode] == 'DX9'	Format:	MBZ				
Exists If:	//Structure[SAMPLER_STATE][Texture Border Color Mode] == 'DX9'									
Format:	MBZ									
	31:0	<p><b>Border Color Green</b></p> <table border="1"> <tr> <td>Exists If:</td><td>//Structure[SAMPLER_STATE][Texture Border Color Mode] == 'DX10/OGL'</td></tr> <tr> <td>Format:</td><td>IEEE_FP</td></tr> <tr> <td>Format:</td><td>S31</td></tr> <tr> <td>Format:</td><td>U32</td></tr> </table> <p>Texture Border Color Mode = DX10/OGL</p>	Exists If:	//Structure[SAMPLER_STATE][Texture Border Color Mode] == 'DX10/OGL'	Format:	IEEE_FP	Format:	S31	Format:	U32
Exists If:	//Structure[SAMPLER_STATE][Texture Border Color Mode] == 'DX10/OGL'									
Format:	IEEE_FP									
Format:	S31									
Format:	U32									
2	31:0	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Exists If:</td><td>//Structure[SAMPLER_STATE][Texture Border Color Mode] == 'DX9'</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Exists If:	//Structure[SAMPLER_STATE][Texture Border Color Mode] == 'DX9'	Format:	MBZ				
Exists If:	//Structure[SAMPLER_STATE][Texture Border Color Mode] == 'DX9'									
Format:	MBZ									

## SAMPLER\_INDIRECT\_STATE

	31:0	<b>Border Color Blue</b>
		Exists If: //Structure[SAMPLER_STATE][Texture Border Color Mode] == 'DX10/OGL'
		Format: IEEE_FP
		Format: S31
		Format: U32
		Texture Border Color Mode = DX10/OGL
3	31:0	<b>Reserved</b>
		Exists If: //Structure[SAMPLER_STATE][Texture Border Color Mode] == 'DX9'
		Format: MBZ
	31:0	<b>Border Color Alpha</b>
		Exists If: //Structure[SAMPLER_STATE][Texture Border Color Mode] == 'DX10/OGL'
		Format: IEEE_FP
		Format: S31
		Format: U32
		Texture Border Color Mode = DX10/OGL
4..15	31:0	<b>Reserved</b>

## SAMPLER\_STATE\_8x8\_AVs\_COEFFICIENTS

<b>SAMPLER_STATE_8x8_AVs_COEFFICIENTS</b>								
<table border="1"> <thead> <tr> <th colspan="2"><b>Description</b></th><th><b>Project</b></th></tr> </thead> <tbody> <tr> <td colspan="2">ExistsIf = AVs</td><td>BDW</td></tr> </tbody> </table>			<b>Description</b>		<b>Project</b>	ExistsIf = AVs		BDW
<b>Description</b>		<b>Project</b>						
ExistsIf = AVs		BDW						
<b>DWord</b>	<b>Bit</b>	<b>Description</b>						
0	31:24	<b>Table 0Y Filter Coefficient[n,1]</b>						
		<table border="1"> <tr> <td>Format:</td> <td>S1.6 2's Complement</td> </tr> </table> <b>Range:</b> [-2, +2)	Format:	S1.6 2's Complement				
Format:	S1.6 2's Complement							
23:16	<b>Table 0X Filter Coefficient[n,1]</b>							
	<table border="1"> <tr> <td>Format:</td> <td>S1.6 2's Complement</td> </tr> </table> <b>Range:</b> [-2, +2)	Format:	S1.6 2's Complement					
Format:	S1.6 2's Complement							
15:8	<b>Table 0Y Filter Coefficient[n,0]</b>							
	<table border="1"> <tr> <td>Format:</td> <td>S1.6 2's Complement</td> </tr> </table> <b>Range:</b> [-2, +2)	Format:	S1.6 2's Complement					
Format:	S1.6 2's Complement							
<table border="1"> <tr> <td align="center" colspan="2"><b>Programming Notes</b></td></tr> <tr> <td align="center" colspan="2">If the format is R10G10B10A2_UNORM or R8G8B8A8_UNORM, this field MBZ.</td></tr> </table>	<b>Programming Notes</b>		If the format is R10G10B10A2_UNORM or R8G8B8A8_UNORM, this field MBZ.					
<b>Programming Notes</b>								
If the format is R10G10B10A2_UNORM or R8G8B8A8_UNORM, this field MBZ.								
7:0	<b>Table 0X Filter Coefficient[n,0]</b>							
	<table border="1"> <tr> <td>Format:</td> <td>S1.6 2's Complement</td> </tr> </table> <b>Range:</b> [-2, +2)	Format:	S1.6 2's Complement					
Format:	S1.6 2's Complement							
<table border="1"> <tr> <td align="center" colspan="2"><b>Programming Notes</b></td></tr> <tr> <td align="center" colspan="2">If the format is R10G10B10A2_UNORM or R8G8B8A8_UNORM, this field MBZ.</td></tr> </table>	<b>Programming Notes</b>		If the format is R10G10B10A2_UNORM or R8G8B8A8_UNORM, this field MBZ.					
<b>Programming Notes</b>								
If the format is R10G10B10A2_UNORM or R8G8B8A8_UNORM, this field MBZ.								
1	31:24	<b>Table 0Y Filter Coefficient[n,3]</b>						
		<table border="1"> <tr> <td>Format:</td> <td>S1.6 2's Complement</td> </tr> </table> <b>Range:</b> [-2.0, +2.0)	Format:	S1.6 2's Complement				
Format:	S1.6 2's Complement							
23:16	<b>Table 0X Filter Coefficient[n,3]</b>							
	<table border="1"> <tr> <td>Format:</td> <td>S1.6 2's Complement</td> </tr> </table> <b>Range:</b> [-2.0, +2.0)	Format:	S1.6 2's Complement					
Format:	S1.6 2's Complement							
15:8	<b>Table 0Y Filter Coefficient[n,2]</b>							
	<table border="1"> <tr> <td>Format:</td> <td>S1.6 2's Complement</td> </tr> </table> <b>Range:</b> [-2.0, +2.0)	Format:	S1.6 2's Complement					
Format:	S1.6 2's Complement							

<b>SAMPLER_STATE_8x8_AV_S_COEFFICIENTS</b>			
	7:0	<b>Table 0X Filter Coefficient[n,2]</b>	
		Format:	S1.6 2's Complement
		<b>Range:</b>	[-2.0, +2.0)
2	31:24	<b>Table 0Y Filter Coefficient[n,5]</b>	
		Format:	S1.6 2's Complement
		<b>Range:</b>	[-2.0, +2.0)
	23:16	<b>Table 0X Filter Coefficient[n,5]</b>	
		Format:	S1.6 2's Complement
		<b>Range:</b>	[-2.0, +2.0)
	15:8	<b>Table 0Y Filter Coefficient[n,4]</b>	
		Format:	S1.6 2's Complement
		<b>Range:</b>	[-2.0, +2.0)
		<b>Programming Notes</b>	
		If the format is R10G10B10A2_UNORM or R8G8B8A8_UNORM, this field MBZ.	
	7:0	<b>Table 0X Filter Coefficient[n,4]</b>	
		Format:	S1.6 2's Complement
		<b>Range:</b>	[-2.0, +2.0)
		<b>Programming Notes</b>	
		If the format is R10G10B10A2_UNORM or R8G8B8A8_UNORM, this field MBZ.	
3	31:24	<b>Table 0Y Filter Coefficient[n,7]</b>	
		Format:	S1.6 2's Complement
		<b>Range:</b>	[-2, +2)
	23:16	<b>Table 0X Filter Coefficient[n,7]</b>	
		Format:	S1.6 2's Complement
		<b>Range:</b>	[-2, +2)
	15:8	<b>Table 0Y Filter Coefficient[n,6]</b>	
		Format:	S1.6 2's Complement
		<b>Range:</b>	[-2, +2)
	7:0	<b>Table 0X Filter Coefficient[n,6]</b>	
		Format:	S1.6 2's Complement
		<b>Range:</b>	[-2, +2)

## SAMPLER\_STATE\_8x8\_AV\_S\_COEFFICIENTS

4	31:24	<b>Table 1X Filter Coefficient[n,3]</b>		
		<table border="1"> <tr> <td>Format:</td><td>S1.6 2's Complement</td></tr> </table> <p><b>Range:</b> [-2.0, +2.0)</p>	Format:	S1.6 2's Complement
Format:	S1.6 2's Complement			
<b>Table 1X Filter Coefficient[n,2]</b>				
5	23:16	<table border="1"> <tr> <td>Format:</td><td>S1.6 2's Complement</td></tr> </table>	Format:	S1.6 2's Complement
Format:	S1.6 2's Complement			
<table border="1"> <thead> <tr> <th>Description</th><th>Project</th></tr> </thead> <tbody> <tr> <td><b>Range:</b> [-1.0, +1.0)</td><td>BDW</td></tr> </tbody> </table>	Description	Project	<b>Range:</b> [-1.0, +1.0)	BDW
Description	Project			
<b>Range:</b> [-1.0, +1.0)	BDW			
<b>Reserved</b>				
6	15:0	<table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ
Format:	MBZ			
<b>Reserved</b>				
<table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ		
Format:	MBZ			
7	31:16	<b>Table 1X Filter Coefficient[n,5]</b>		
		<table border="1"> <tr> <td>Format:</td><td>S1.6 2's Complement</td></tr> </table>	Format:	S1.6 2's Complement
Format:	S1.6 2's Complement			
<table border="1"> <thead> <tr> <th>Description</th><th>Project</th></tr> </thead> <tbody> <tr> <td><b>Range:</b> [-1.0, +1.0)</td><td>BDW</td></tr> </tbody> </table>	Description	Project	<b>Range:</b> [-1.0, +1.0)	BDW
Description	Project			
<b>Range:</b> [-1.0, +1.0)	BDW			
7	15:8	<b>Table 1X Filter Coefficient[n,4]</b>		
		<table border="1"> <tr> <td>Format:</td><td>S1.6 2's Complement</td></tr> </table>	Format:	S1.6 2's Complement
Format:	S1.6 2's Complement			
<b>Range:</b> [-2.0, +2.0)				
6	31:24	<b>Table 1Y Filter Coefficient[n,3]</b>		
		<table border="1"> <tr> <td>Format:</td><td>S1.6 2's Complement</td></tr> </table>	Format:	S1.6 2's Complement
Format:	S1.6 2's Complement			
<b>Range:</b> [-2.0, +2.0)				
6	23:16	<b>Table 1Y Filter Coefficient[n,2]</b>		
		<table border="1"> <tr> <td>Format:</td><td>S1.6 2's Complement</td></tr> </table>	Format:	S1.6 2's Complement
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Description	Project			
<b>Range:</b> [-1.0, +1.0)	BDW			
7	15:0	<b>Reserved</b>		
		<table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ
Format:	MBZ			
<b>Reserved</b>				
7	31:16	<table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ
Format:	MBZ			

## SAMPLER\_STATE\_8x8\_AV\_S\_COEFFICIENTS

	15:8	<b>Table 1Y Filter Coefficient[n,5]</b>				
		Format: S1.6 2's Complement				
		<table border="1"> <thead> <tr> <th>Description</th><th>Project</th></tr> </thead> <tbody> <tr> <td><b>Range:</b> [-1.0, +1.0)</td><td>BDW</td></tr> </tbody> </table>	Description	Project	<b>Range:</b> [-1.0, +1.0)	BDW
Description	Project					
<b>Range:</b> [-1.0, +1.0)	BDW					
	7:0	<b>Table 1Y Filter Coefficient[n,4]</b>				
		Format: S1.6 2's Complement				
		<b>Range:</b> [-2.0, +2.0)				



## SAMPLER STATE 8x8 AVS

## SAMPLER\_STATE\_8x8\_AVs

	17:12	<b>Strong Edge Threshold</b>			
		Default Value:	8		
		Format:	U6		
		If EM > <b>Strong Edge Threshold</b> , the basic VSA detects a strong edge.			
	11:6	<b>Weak Edge Threshold</b>			
		Default Value:	1		
		Format:	U6		
		If <b>Strong Edge Threshold</b> > EM > <b>Weak Edge Threshold</b> , the basic VSA detects a weak edge.			
	5:0	<b>Gain Factor</b>			
		Default Value:	44		
		Format:	U6		
		User control sharpening strength			
1	31:0	<b>Reserved</b>			
		Project:	BDW		
		Format:	MBZ		
2	31:27	<b>Reserved</b>			
	26:22	Reserved			
	21:17	Reserved			
	16:14	<b>Strong Edge Weight</b>			
		Default Value:	7		
		Format:	U3		
		Sharpening strength when a strong edge is found in basic VSA.			
	13:11	<b>Regular Weight</b>			
		Default Value:	2		
		Format:	U3		
		Sharpening strength when a weak edge is found in basic VSA.			
	10:8	<b>Non Edge Weight</b>			
		Default Value:	1		
		Format:	U3		
		Sharpening strength when no edge is found in basic VSA.			

<b>SAMPLER_STATE_8x8_AVs</b>																
	7:0	<p><b>Global Noise Estimation</b></p> <table border="1"> <tr> <td>Default Value:</td><td>255</td></tr> <tr> <td>Format:</td><td>U8</td></tr> </table> <p>Global noise estimation of previous frame.</p>	Default Value:	255	Format:	U8										
Default Value:	255															
Format:	U8															
3	31	<p><b>Skin Tone Tuned IEF_Enable</b></p> <table border="1"> <tr> <td>Default Value:</td><td>1</td></tr> <tr> <td>Format:</td><td>U1</td></tr> </table> <p>Control bit to enable the skin tone tuned IEF.</p>	Default Value:	1	Format:	U1										
Default Value:	1															
Format:	U1															
30	<p><b>IEF4Smooth_Enable</b></p> <table border="1"> <tr> <td>Format:</td><td>U1</td></tr> </table> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0</td><td>[Default]</td><td>IEF is operating as a content adaptive detail filter based on 5x5 region</td></tr> <tr> <td>1</td><td></td><td>IEF is operating as a content adaptive smooth filter based on 3x3 region</td></tr> </tbody> </table>	Format:	U1	Value	Name	Description	0	[Default]	IEF is operating as a content adaptive detail filter based on 5x5 region	1		IEF is operating as a content adaptive smooth filter based on 3x3 region				
Format:	U1															
Value	Name	Description														
0	[Default]	IEF is operating as a content adaptive detail filter based on 5x5 region														
1		IEF is operating as a content adaptive smooth filter based on 3x3 region														
29:28	<p><b>Enable 8-tap filter</b></p> <p><b>Adaptive Filtering (Mode = 11) ExistsIf:</b> R10G10B10A2_UNORM R8G8B8A8_UNORM (AYUV also) R8B8G8A8_UNORM B8G8R8A8_UNORM R16G16B16A16</p> <p><b>Enable 8-tap Filtering on UV channel (Mode = 10) ExistsIf:</b> R10G10B10A2_UNORM R8G8B8A8_UNORM (AYUV also) R8B8_UNORM (CrCb) R8_UNORM R8B8G8A8_UNORM B8G8R8A8_UNORM R16G16B16A16 Y8_UNORM</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>00b</td><td></td><td>4-tap filter is only done on all channels.</td></tr> <tr> <td>01b</td><td></td><td>Enable 8-tap Adaptive filter on G-channel. 4-tap filter on other channels.</td></tr> <tr> <td>10b</td><td></td><td>8-tap filter is done on all channels (UV-ch uses the Y-coefficients)</td></tr> <tr> <td>11b</td><td></td><td>Enable 8-tap Adaptive filter all channels (UV-ch uses the Y-coefficients).</td></tr> </tbody> </table> <p><b>Programming Notes</b></p> <p>For 00 and 10, are applicable for RGB surfaces only or surface without Y-ch. In case it is a YUV surface it will default to adaptive mode automatically which is 01 and 11 respectively. Alpha channel is always bi-linear filter irrespective of the above modes.</p> <p>Mode 01 and 00 are legacy support and are supported on all surface formats.</p> <p>When Mode is 10 and Surface format is Y8_UNORM, Bypass X/Y Adaptive Filtering must be 1, and Default Sharp Level must be 255</p>	Value	Name	Description	00b		4-tap filter is only done on all channels.	01b		Enable 8-tap Adaptive filter on G-channel. 4-tap filter on other channels.	10b		8-tap filter is done on all channels (UV-ch uses the Y-coefficients)	11b		Enable 8-tap Adaptive filter all channels (UV-ch uses the Y-coefficients).
Value	Name	Description														
00b		4-tap filter is only done on all channels.														
01b		Enable 8-tap Adaptive filter on G-channel. 4-tap filter on other channels.														
10b		8-tap filter is done on all channels (UV-ch uses the Y-coefficients)														
11b		Enable 8-tap Adaptive filter all channels (UV-ch uses the Y-coefficients).														

## SAMPLER\_STATE\_8x8\_AVs

	27:22	<b>Hue_Max</b>				
		<table border="1"> <tr> <td>Default Value:</td><td>14</td></tr> <tr> <td>Format:</td><td>U6</td></tr> </table> <p>Rectangle half width.</p>	Default Value:	14	Format:	U6
Default Value:	14					
Format:	U6					
	21:16	<b>Sat_Max</b>				
		<table border="1"> <tr> <td>Default Value:</td><td>31</td></tr> <tr> <td>Format:</td><td>U6</td></tr> </table> <p>Rectangle half length</p>	Default Value:	31	Format:	U6
Default Value:	31					
Format:	U6					
	15:8	<b>Cos(alpha)</b>				
		<table border="1"> <tr> <td>Format:</td><td>S0.7 2's Complement</td></tr> </table> <p>Deafult Value: 79/128</p>	Format:	S0.7 2's Complement		
Format:	S0.7 2's Complement					
	7:0	<b>Sin(alpha)</b>				
		<table border="1"> <tr> <td>Format:</td><td>S0.7 2's Complement</td></tr> </table> <p>Deafult Value: 101/128</p>	Format:	S0.7 2's Complement		
Format:	S0.7 2's Complement					
4	31:24	<b>V_Mid</b>				
		<table border="1"> <tr> <td>Default Value:</td><td>154</td></tr> <tr> <td>Format:</td><td>U8</td></tr> </table> <p>Rectangle middle-point V coordinate.</p>	Default Value:	154	Format:	U8
Default Value:	154					
Format:	U8					
	23:16	<b>U_Mid</b>				
		<table border="1"> <tr> <td>Default Value:</td><td>110</td></tr> <tr> <td>Format:</td><td>U8</td></tr> </table> <p>Rectangle middle-point U coordinate.</p>	Default Value:	110	Format:	U8
Default Value:	110					
Format:	U8					
	15	<b>VY_STD_Enable</b>				
		<table border="1"> <tr> <td>Format:</td><td>Enable</td></tr> </table> <p>Enables STD in the VY subspace.</p>	Format:	Enable		
Format:	Enable					
	14:12	<b>Diamond Margin</b>				
		<table border="1"> <tr> <td>Default Value:</td><td>4</td></tr> <tr> <td>Format:</td><td>U3</td></tr> </table>	Default Value:	4	Format:	U3
Default Value:	4					
Format:	U3					
	11	<b>Reserved</b>				
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	BDW	Format:	MBZ
Project:	BDW					
Format:	MBZ					

SAMPLER_STATE_8x8_AVs			
	10:0	<b>S3U</b>	
		Format:	S2.8 2's Complement
		Deafult Value:	0/256
5	31	<b>SkinDetailFactor</b>	
		Format:	S0
		This flag bit is in operation only when the control bit <b>Skin Tone TunedIEF_Enable</b> is on.	
		<b>Value</b>	<b>Name</b>
		1	sign(SkinDetailFactor) is equal to +1, and the content of the detected skin tone area is not detail revealed.
		0	sign(SkinDetailFactor) is equal to -1, and the content of the detected skin tone area is detail revealed.
	30:24	<b>Diamond_du</b>	
		Default Value:	2
		Format:	S6 2's Complement
		Rhombus center shift in the sat-direction, relative to the rectangle center.	
	23:21	<b>HS_margin</b>	
		Default Value:	3
		Format:	U3
		Defines rectangle margin	
	20:13	<b>Diamond_alpha</b>	
		Format:	U2.6
		Deafault Value:	100/64
		$1 / \tan(\beta)$	
	12:7	<b>Diamond_Th</b>	
		Default Value:	35
		Format:	U6
		Half length of the rhombus axis in the sat-direction.	
	6:0	<b>Diamond_dv</b>	
		Default Value:	0
		Format:	S6 2's Complement
		Rhombus center shift in the hue-direction, relative to the rectangle center.	

## SAMPLER\_STATE\_8x8\_AVs

6	31:24	<b>Y_point_4</b>		
		<table border="1"> <tr> <td>Default Value:</td><td>255</td></tr> <tr> <td>Format:</td><td>U8</td></tr> </table> <p>Fourth point of the Y piecewise linear membership function.</p>	Default Value:	255
Default Value:	255			
Format:	U8			
<table border="1"> <tr> <td>Default Value:</td><td>254</td></tr> <tr> <td>Format:</td><td>U8</td></tr> </table> <p>Third point of the Y piecewise linear membership function.</p>	Default Value:	254	Format:	U8
Default Value:	254			
Format:	U8			
<table border="1"> <tr> <td>Default Value:</td><td>47</td></tr> <tr> <td>Format:</td><td>U8</td></tr> </table> <p>Second point of the Y piecewise linear membership function.</p>	Default Value:	47	Format:	U8
Default Value:	47			
Format:	U8			
7	7:0	<b>Y_point_1</b>		
		<table border="1"> <tr> <td>Default Value:</td><td>46</td></tr> <tr> <td>Format:</td><td>U8</td></tr> </table> <p>First point of the Y piecewise linear membership function.</p>	Default Value:	46
Default Value:	46			
Format:	U8			
<b>Reserved</b> <table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ		
Format:	MBZ			
<b>INV_Margin_VYL</b> <table border="1"> <tr> <td>Format:</td><td>U0.16</td></tr> </table> <p>1/Margin_VYL = 3300/65536</p>	Format:	U0.16		
Format:	U0.16			
8	31:24	<b>P1L</b>		
		<table border="1"> <tr> <td>Default Value:</td><td>216</td></tr> <tr> <td>Format:</td><td>U8</td></tr> </table> <p>Y Point 1 of the lower part of the detection PWLF.</p>	Default Value:	216
Default Value:	216			
Format:	U8			
23:16	<b>POL</b>			
	<table border="1"> <tr> <td>Default Value:</td><td>46</td></tr> <tr> <td>Format:</td><td>U8</td></tr> </table> <p>Y Point 0 of the lower part of the detection PWLF.</p>	Default Value:	46	Format:
Default Value:	46			
Format:	U8			
15:0	<b>INV_Margin_VYU</b> 1/Margin_VYU = 1600/65536			

## **SAMPLER\_STATE\_8x8\_AVs**

9	31:24	<b>B1L</b>
		Default Value:
		Format:
		V Bias 1 of the lower part of the detection PWLF.
10	23:16	<b>B0L</b>
		Default Value:
		Format:
		V Bias 0 of the lower part of the detection PWLF.
10	15:8	<b>P3L</b>
		Default Value:
		Format:
		Y Point 3 of the lower part of the detection PWLF.
10	7:0	<b>P2L</b>
		Default Value:
		Format:
		Y Point 2 of the lower part of the detection PWLF.
10	31:27	<b>Y_Slope_2</b>
		Format:
		Default Value: 31/8
		Slope between points Y3 and Y4.
10	26:16	<b>S0L</b>
		Format:
		Default Value: -5/256
		Slope 0 of the lower part of the detection PWLF.
10	15:8	<b>B3L</b>
		Default Value:
		Format:
		V Bias 3 of the lower part of the detection PWLF.
10	7:0	<b>B2L</b>
		Default Value:
		Format:
		130

## SAMPLER\_STATE\_8x8\_AVs

11	31:22	<b>Reserved</b>
		Format: MBZ
		<b>S2L</b>
		Format: S2.8 2's Complement
		Default Value: 0/256
		Slope 2 of the lower part of the detection PWLF.
		<b>S1L</b>
		Format: S2.8 2's Complement
		Default Value: 0/256
		Slope 1 of the lower part of the detection PWLF.
12	31:27	<b>Y_Slope1</b>
		Format: U2.3
		Default Value: 31/8
		Slope between points Y1 and Y2.
		<b>P1U</b>
		Default Value: 66
		Format: U8
		Y Point 1 of the upper part of the detection PWLF.
		<b>P0U</b>
		Default Value: 46
13	31:24	Format: U8
		Default Value: 0/256
		Slope 0 of the upper part of the detection PWLF.
		<b>S3L</b>
		Format: S2.8 2's Complement
		Default Value: 0/256
		Slope 3 of the lower part of the detection PWLF.
		<b>B1U</b>
		Default Value: 163
		Format: U8
		V Bias 1 of the upper part of the detection PWLF.

## **SAMPLER\_STATE\_8x8\_AVs**

	23:16	<b>BOU</b>				
		<table border="1"> <tr> <td>Default Value:</td> <td>143</td> </tr> <tr> <td>Format:</td> <td>U8</td> </tr> </table> <p>V Bias 0 of the upper part of the detection PWLF.</p>	Default Value:	143	Format:	U8
Default Value:	143					
Format:	U8					
	15:8	<b>P3U</b>				
		<table border="1"> <tr> <td>Default Value:</td> <td>236</td> </tr> <tr> <td>Format:</td> <td>U8</td> </tr> </table> <p>Y Point 3 of the upper part of the detection PWLF.</p>	Default Value:	236	Format:	U8
Default Value:	236					
Format:	U8					
	7:0	<b>P2U</b>				
		<table border="1"> <tr> <td>Default Value:</td> <td>150</td> </tr> <tr> <td>Format:</td> <td>U8</td> </tr> </table> <p>Y Point 2 of the upper part of the detection PWLF.</p>	Default Value:	150	Format:	U8
Default Value:	150					
Format:	U8					
14	31:27	<b>Reserved</b>				
		<table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ		
Format:	MBZ					
	26:16	<b>S0U</b>				
		<table border="1"> <tr> <td>Format:</td> <td>S2.8 2's Complement</td> </tr> </table>	Format:	S2.8 2's Complement		
Format:	S2.8 2's Complement					
		<table border="1"> <tr> <td>Default Value: 256/256</td> <td></td> </tr> </table>	Default Value: 256/256			
Default Value: 256/256						
		<table border="1"> <tr> <td>Slope 0 of the upper part of the detection PWLF.</td> <td></td> </tr> </table>	Slope 0 of the upper part of the detection PWLF.			
Slope 0 of the upper part of the detection PWLF.						
	15:8	<b>B3U</b>				
		<table border="1"> <tr> <td>Default Value:</td> <td>140</td> </tr> <tr> <td>Format:</td> <td>U8</td> </tr> </table>	Default Value:	140	Format:	U8
Default Value:	140					
Format:	U8					
		<table border="1"> <tr> <td>V Bias 3 of the upper part of the detection PWLF.</td> <td></td> </tr> </table>	V Bias 3 of the upper part of the detection PWLF.			
V Bias 3 of the upper part of the detection PWLF.						
	7:0	<b>B2U</b>				
		<table border="1"> <tr> <td>Default Value:</td> <td>200</td> </tr> <tr> <td>Format:</td> <td>U8</td> </tr> </table>	Default Value:	200	Format:	U8
Default Value:	200					
Format:	U8					
		<table border="1"> <tr> <td>V Bias 2 of the upper part of the detection PWLF.</td> <td></td> </tr> </table>	V Bias 2 of the upper part of the detection PWLF.			
V Bias 2 of the upper part of the detection PWLF.						
15	31:22	<b>Reserved</b>				
		<table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ		
Format:	MBZ					
	21:11	<b>S2U</b>				
		<table border="1"> <tr> <td>Format:</td> <td>S2.8 2's Complement</td> </tr> </table>	Format:	S2.8 2's Complement		
Format:	S2.8 2's Complement					
		<table border="1"> <tr> <td>Default Value: -179/256</td> <td></td> </tr> </table>	Default Value: -179/256			
Default Value: -179/256						
		<table border="1"> <tr> <td>Slope 2 of the upper part of the detection PWLF.</td> <td></td> </tr> </table>	Slope 2 of the upper part of the detection PWLF.			
Slope 2 of the upper part of the detection PWLF.						

<b>SAMPLER_STATE_8x8_AVs</b>				
	10:0	<b>S1U</b>		
		Format:	S2.8 2's Complement	
		Default Value: 113/256		
		Slope 1 of the upper part of the detection PWLF.		
16..23	255:0	<b>Filter Coefficient[0]</b>		
		Format:	<b>SAMPLER_STATE_8x8_AVs_COEFFICIENTS</b>	
24..31	255:0	<b>Filter Coefficient[1]</b>		
		Format:	<b>SAMPLER_STATE_8x8_AVs_COEFFICIENTS</b>	
32..39	255:0	<b>Filter Coefficient[2]</b>		
		Format:	<b>SAMPLER_STATE_8x8_AVs_COEFFICIENTS</b>	
40..47	255:0	<b>Filter Coefficient[3]</b>		
		Format:	<b>SAMPLER_STATE_8x8_AVs_COEFFICIENTS</b>	
48..55	255:0	<b>Filter Coefficient[4]</b>		
		Format:	<b>SAMPLER_STATE_8x8_AVs_COEFFICIENTS</b>	
56..63	255:0	<b>Filter Coefficient[5]</b>		
		Format:	<b>SAMPLER_STATE_8x8_AVs_COEFFICIENTS</b>	
64..71	255:0	<b>Filter Coefficient[6]</b>		
		Format:	<b>SAMPLER_STATE_8x8_AVs_COEFFICIENTS</b>	
72..79	255:0	<b>Filter Coefficient[7]</b>		
		Format:	<b>SAMPLER_STATE_8x8_AVs_COEFFICIENTS</b>	
80..87	255:0	<b>Filter Coefficient[8]</b>		
		Format:	<b>SAMPLER_STATE_8x8_AVs_COEFFICIENTS</b>	
88..95	255:0	<b>Filter Coefficient[9]</b>		
		Format:	<b>SAMPLER_STATE_8x8_AVs_COEFFICIENTS</b>	
96..103	255:0	<b>Filter Coefficient[10]</b>		
		Format:	<b>SAMPLER_STATE_8x8_AVs_COEFFICIENTS</b>	
104..111	255:0	<b>Filter Coefficient[11]</b>		
		Format:	<b>SAMPLER_STATE_8x8_AVs_COEFFICIENTS</b>	
112..119	255:0	<b>Filter Coefficient[12]</b>		
		Format:	<b>SAMPLER_STATE_8x8_AVs_COEFFICIENTS</b>	
120..127	255:0	<b>Filter Coefficient[13]</b>		
		Format:	<b>SAMPLER_STATE_8x8_AVs_COEFFICIENTS</b>	
128..135	255:0	<b>Filter Coefficient[14]</b>		
		Format:	<b>SAMPLER_STATE_8x8_AVs_COEFFICIENTS</b>	

<b>SAMPLER_STATE_8x8_AVs</b>										
136..143	255:0	<b>Filter Coefficient[15]</b>	Format: <b>SAMPLER_STATE_8x8_AVs_COEFFICIENTS</b>							
144..151	255:0	<b>Filter Coefficient[16]</b>	Format: <b>SAMPLER_STATE_8x8_AVs_COEFFICIENTS</b>							
152	31:24	<b>Default Sharpness Level</b>	Format: U8 When adaptive scaling is off, determines the balance between sharp and smooth scalers.							
			<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0</td><td>[Default]</td><td>Contribute 1 from the smooth scalar</td></tr> <tr> <td>255</td><td></td><td>Contribute 1 from the sharp scalar</td></tr> </tbody> </table>	Value	Name	Description	0	[Default]	Contribute 1 from the smooth scalar	255
Value	Name	Description								
0	[Default]	Contribute 1 from the smooth scalar								
255		Contribute 1 from the sharp scalar								
<b>Max Derivative 4 Pixels</b>	Format: U8 Used in adaptive filtering to specify the lower boundary of the smooth 4 pixel area.									
<b>Max Derivative 8 Pixels</b>	Format: U8 Used in adaptive filtering to specify the lower boundary of the smooth 8 pixel area.									
<b>Reserved</b>	Format: MBZ									
<b>Transition Area with 4 Pixels</b>	Format: U3 Used in adaptive filtering to specify the width of the transition area for the 4 pixel calculation.									
<b>Reserved</b>	Format: MBZ									
<b>Transition Area with 8 Pixels</b>	Format: U3 Used in adaptive filtering to specify the width of the transition area for the 8 pixel calculation.									
<b>Reserved</b>	Format: MBZ									

## SAMPLER\_STATE\_8x8\_AVs

	22	<b>Bypass X Adaptive Filtering</b>									
		Format: <input type="text"/> Disable									
When disabled, the X direction will use <b>Default Sharpness Level</b> to blend between the smooth and sharp filters rather than the calculated value.											
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>1</td><td>Disable</td><td>Disable X Adaptive Filtering</td></tr> <tr> <td>0</td><td>Enable</td><td>Enable X Adaptive Filtering</td></tr> </tbody> </table>	Value	Name	Description	1	Disable	Disable X Adaptive Filtering	0	Enable	Enable X Adaptive Filtering
Value	Name	Description									
1	Disable	Disable X Adaptive Filtering									
0	Enable	Enable X Adaptive Filtering									
	21	<b>Bypass Y Adaptive Filtering</b>									
		Format: <input type="text"/> Disable									
When disabled, the Y direction will use <b>Default Sharpness Level</b> to blend between the smooth and sharp filters rather than the calculated value.											
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>1</td><td>Disable</td><td>Disable Y Adaptive Filtering</td></tr> <tr> <td>0</td><td>Enable</td><td>Enable Y Adaptive Filtering</td></tr> </tbody> </table>	Value	Name	Description	1	Disable	Disable Y Adaptive Filtering	0	Enable	Enable Y Adaptive Filtering
Value	Name	Description									
1	Disable	Disable Y Adaptive Filtering									
0	Enable	Enable Y Adaptive Filtering									
	20:2	<b>Reserved</b>									
		Format: <input type="text"/> MBZ									
	1	<b>Adaptive Filter for all channels</b>									
		Format: <input type="text"/> Enable									
Only to be enabled if 8-tap Adaptive filter mode is on, else it should be disabled.											
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>1</td><td>Enable</td><td>Enable Adaptive Filter on UV/RB Channels</td></tr> <tr> <td>0</td><td>Disable</td><td>Disable Adaptive Filter on UV/RB Channels</td></tr> </tbody> </table>	Value	Name	Description	1	Enable	Enable Adaptive Filter on UV/RB Channels	0	Disable	Disable Adaptive Filter on UV/RB Channels
Value	Name	Description									
1	Enable	Enable Adaptive Filter on UV/RB Channels									
0	Disable	Disable Adaptive Filter on UV/RB Channels									
	0	<b>RGB Adaptive</b>									
		Format: <input type="text"/> Enable									
This should be always set to 0 for YUV input and can be enabled/disabled for RGB input. This should be enabled only if we enable 8-tap adaptive filter for RGB input.											
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>1</td><td>Enable</td><td>Enable the RGB Adaptive filter using the equation <math>(Y = (R + 2G + B) \gg 2)</math></td></tr> <tr> <td>0</td><td>Disable</td><td>Disable the RGB Adaptive equation and use G-Ch directly for adaptive filter</td></tr> </tbody> </table>	Value	Name	Description	1	Enable	Enable the RGB Adaptive filter using the equation $(Y = (R + 2G + B) \gg 2)$	0	Disable	Disable the RGB Adaptive equation and use G-Ch directly for adaptive filter
Value	Name	Description									
1	Enable	Enable the RGB Adaptive filter using the equation $(Y = (R + 2G + B) \gg 2)$									
0	Disable	Disable the RGB Adaptive equation and use G-Ch directly for adaptive filter									

# SAMPLER STATE 8x8 CONVOLVE

## SAMPLER\_STATE\_8x8\_CONVOLVE

## SAMPLER\_STATE\_8x8\_CONVOLVE

### Description

Function: 0001b ExistsIf: [Convolve] && [(Kernel Size) = < (15x15)]

DWord	Bit	Description										
0	31:21	<b>Reserved</b>										
		Format:	MBZ									
	20	<b>Reserved</b>										
		Project:	BDW									
		Format:	MBZ									
	19:17	<b>Reserved</b>										
		Format:	MBZ									
	16	<b>Reserved</b>										
		Project:	BDW									
		Format:	MBZ									
	15:13	<b>Reserved</b>										
		Format:	MBZ									
	12	<b>Size of the Coefficient</b>										
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>8bit</td> <td>The lower 8 bits of the accumulator is forced to zero or ignored during the accumulation operation.</td> </tr> <tr> <td>1</td> <td>16bit</td> <td>The lower 8 bits are also included for the operation. The final result of the accumulator is shifted before clamping the result as specified by the Scale down value.: Result[15:0] = Clamp(Accum[40:12] » scale_down)</td> </tr> </tbody> </table>		Value	Name	Description	0	8bit	The lower 8 bits of the accumulator is forced to zero or ignored during the accumulation operation.	1	16bit	The lower 8 bits are also included for the operation. The final result of the accumulator is shifted before clamping the result as specified by the Scale down value.: Result[15:0] = Clamp(Accum[40:12] » scale_down)
Value	Name	Description										
0	8bit	The lower 8 bits of the accumulator is forced to zero or ignored during the accumulation operation.										
1	16bit	The lower 8 bits are also included for the operation. The final result of the accumulator is shifted before clamping the result as specified by the Scale down value.: Result[15:0] = Clamp(Accum[40:12] » scale_down)										
	11:8	<b>Scale down value</b>										
		Exists If:	//[Convolve] Only									
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>[0,10]</td> <td></td> <td>The final result is shifted by this value before clamp is done.</td> </tr> </tbody> </table>		Value	Name	Description	[0,10]		The final result is shifted by this value before clamp is done.			
Value	Name	Description										
[0,10]		The final result is shifted by this value before clamp is done.										
	7:4	<b>WIDTH</b>										
		Exists If:	//[Convolve] Only									
		It contains the WIDTH of the kernel.										
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>[2-15]</td> <td></td> </tr> </tbody> </table>		Value	Name	[2-15]						
Value	Name											
[2-15]												
	3:0	<b>HEIGHT</b>										
		Exists If:	//[Convolve] Only									
		It contains the HEIGHT of the kernel.										
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>[2-15]</td> <td></td> </tr> </tbody> </table>		Value	Name	[2-15]						
Value	Name											
[2-15]												

## SAMPLER\_STATE\_8x8\_CONVOLVE

1..15	31:0	<b>Reserved</b>
		Format: MBZ
16	31:16	<b>Filter Coefficient[0,1]</b> Exists If: ///[Filtering] Operation Format: S3.4(8bit)/S3.12(16bit) in 2's Complement <b>Range:</b> [-8.0, +8.0) <b>Programming Notes</b> Please note that this field is MBZ if not used in the Filtering Mode.
	15:0	<b>Filter Coefficient[0,0]</b> Exists If: ///[Filtering] Operation Format: S3.4(8bit)/S3.12(16bit) in 2's Complement <b>Range:</b> [-8.0, +8.0) <b>Programming Notes</b> Please note that this field is MBZ if not used in the Filtering Mode.
17	31:16	<b>Filter Coefficient[0,3]</b> Exists If: ///[Filtering] Operation Format: S3.4(8bit)/S3.12(16bit) in 2's Complement <b>Range:</b> [-8.0, +8.0) <b>Programming Notes</b> Please note that this field is MBZ if not used in the Filtering Mode.
	15:0	<b>Filter Coefficient[0,2]</b> Exists If: ///[Filtering] Operation Format: S3.4(8bit)/S3.12(16bit) in 2's Complement <b>Range:</b> [-8.0, +8.0) <b>Programming Notes</b> Please note that this field is MBZ if not used in the Filtering Mode.
18..19	31:0	<b>Filter Coefficient[0,7:4]</b> This table has the same layout as shown above.
20..23	31:0	<b>Filter Coefficient[0,15:8]</b> This table has the same layout as shown above.
24..143	31:0	<b>Filter Coefficient[15:1,15:0]</b> Columns [15:1] of the coefficient containing 16 coefficients for [15:0] rows. This table has the same layout as shown above.
144..263	31:0	<b>Reserved</b> Project: BDW Format: MBZ

## SAMPLER\_STATE\_8x8\_CONVOLVE

264..391	31:0	<b>Reserved</b>	
		Project:	BDW
		Format:	MBZ
392..511	31:0	<b>Reserved</b>	
		Project:	BDW
		Format:	MBZ

## SAMPLER\_STATE\_8x8\_ERODE\_DILATE\_MINMAXFILTER

<b>SAMPLER_STATE_8x8_ERODE_DILATE_MINMAXFILTER</b>		
Project: BDW Size (in bits): 256 Default Value: 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000		
<b>Description</b>		<b>Project</b>
The table is valid for the following funstions: 0100 - Erode 0101 - Dilate 0011 - MinMaxFilter		BDW
<b>Programming Notes</b>		
Max kernel size is 15x15. For sizes less than 15x15 the coefficients not used should be zeroed out.		
<b>DWord</b>	<b>Bit</b>	<b>Description</b>
0	31:16	<b>16bit Mask for Row0 [15:0]</b>
	15:8	<b>Reserved</b>
		Format: MBZ
	7:4	<b>Width Of The Kernel</b>
	3:0	<b>Value</b>
		<b>Name</b>
	2-15	
1	31:16	<b>16bit Mask for Row2 [15:0]</b>
	15:0	<b>16bit Mask for Row1 [15:0]</b>
2	31:16	<b>16bit Mask for Row4 [15:0]</b>
	15:0	<b>16bit Mask for Row3 [15:0]</b>
3	31:16	<b>16bit Mask for Row6 [15:0]</b>
	15:0	<b>16bit Mask for Row5 [15:0]</b>
4	31:16	<b>16bit Mask for Row8 [15:0]</b>
	15:0	<b>16bit Mask for Row7 [15:0]</b>
5	31:16	<b>16bit Mask for Row10 [15:0]</b>
	15:0	<b>16bit Mask for Row9 [15:0]</b>
6	31:16	<b>16bit Mask for Row12 [15:0]</b>
	15:0	<b>16bit Mask for Row11 [15:0]</b>
7	31:16	<b>16bit Mask for Row14 [15:0]</b>
	15:0	<b>16bit Mask for Row13 [15:0]</b>

## SAMPLER\_STATE

<b>SAMPLER_STATE</b>											
<b>DWord</b>	<b>Bit</b>	<b>Description</b>									
0	31	<p><b>Sampler Disable</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Disable</td> </tr> </table> <p>This field allows the sampler to be disabled. If disabled, all output channels will return 0.</p>	Project:	All	Format:	Disable					
Project:	All										
Format:	Disable										
	30	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> </table>	Project:	BDW							
Project:	BDW										
	29	<p><b>Texture Border Color Mode</b></p> <p>For some surface formats, the 32 bit border color is decoded differently based on the border color mode. In addition, the default value of channels not included in the surface may be affected by this field. Refer to the "Sampler Output Channel Mapping" table for the values of these channels, and for surface formats that may only support one of these modes. Also refer to the definition of SAMPLER_BORDER_COLOR_STATE for more details on the behavior of the two modes defined by this field.</p> <table border="1"> <thead> <tr> <th><b>Value</b></th> <th><b>Name</b></th> <th><b>Description</b></th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>DX10/OGL</td> <td>DX10/OGL mode for interpreting the border color</td> </tr> <tr> <td>1h</td> <td>DX9</td> <td>DX9 and earlier mode for interpreting the border color</td> </tr> </tbody> </table> <p><b>Programming Notes</b></p> <p>This field is required to be the same for every message over a period of time. A flush of the sampler cache must occur before a message with the opposite state of this field is delivered.</p> <p>This field must be set to DX9 mode when used with surfaces that have Surface Format P4A4_UNORM or A4P4_UNORM.</p> <p>This field must be set to DX10/OGL mode when used with surfaces that have Surface Format YCRCB_SWAPUV or YCRCB_SWAPY.</p> <p>This field must be set to DX10/OGL mode if <b>Surface Format</b> for the associated surface is UINT OR SINT.</p> <p>This field must be set to DX10/OGL mode if REDUCTION_MINIMUM or REDUCTION_MAXIMUM or message type is sample_min or sample_max.</p>	<b>Value</b>	<b>Name</b>	<b>Description</b>	0h	DX10/OGL	DX10/OGL mode for interpreting the border color	1h	DX9	DX9 and earlier mode for interpreting the border color
<b>Value</b>	<b>Name</b>	<b>Description</b>									
0h	DX10/OGL	DX10/OGL mode for interpreting the border color									
1h	DX9	DX9 and earlier mode for interpreting the border color									

## SAMPLER\_STATE

	<b>LOD PreClamp Mode</b>																																																															
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## SAMPLER\_STATE

19:17

**Mag Mode Filter**

Project:	All
Format:	U3 Enumerated Type

This field determines how texels are sampled/filtered when a texture is being "magnified" (enlarged). For volume maps, this filter mode selection also applies to the 3rd (inter-layer) dimension.

Value	Name	Description
0h	NEAREST	Sample the nearest texel
1h	LINEAR	Bilinearly filter the 4 nearest texels
2h	ANISOTROPIC	Perform an "anisotropic" filter on the chosen mip level
4h-5h	Reserved	
6h	MONO	Perform a monochrome convolution filter
7h	Reserved	

### Programming Notes

Only MAPFILTER\_NEAREST and MAPFILTER\_LINEAR are supported for surfaces of type SURFTYPE\_3D.

Only MAPFILTER\_NEAREST is supported for surface formats that do not support "Sampling Engine Filtering" as indicated in the Surface Formats table unless using the sample\_c message type or minimum/maximum operation.

MAPFILTER\_MONO: Only CLAMP\_BORDER texture addressing mode is supported. Both Mag Mode Filter and Min Mode Filter must be programmed to MAPFILTER\_MONO. Mip Mode Filter must be MIPFILTER\_NONE. Only valid on surfaces with Surface Format MONO8 and with Surface Type SURFTYPE\_2D.

MAPFILTER\_ANISOTROPIC may cause artifacts at cube edges if enabled for cube maps with the TEXCOORDMODE\_CUBE addressing mode.

MAPFILTER\_ANISOTROPIC will be overridden to MAPFILTER\_LINEAR when using a sample\_l or sample\_l\_c message type or when Force LOD to Zero is set in the message header.

Both Mag Mode Filter and Min Mode Filter must be set to MAPFILTER\_NEAREST if Surface Format for the associated surface is UINT or SINT. However, all settings of this field other than MAPFILTER\_MONO are allowed with UINT/SINT if a minimum or maximum operation is being performed.

MAPFILTER\_FLEXIBLE might have data corruption when sampled from surface with float32 format with exponent value exceeded 248

MAPFILTER\_FLEXIBLE operates on float16 or float32 surfaces could have erroneous signed for infinity output i.e. 0x7f800000 <-> 0xff800000

MAPFILTER\_FLEXIBLE when float16 +/-inf apply to coefficient that are absolutely larger than 1.0 output result could be nan instead of +/-inf MAPFILTER\_FLEXIBLE: A Null Tile reference will be reported back even if the associated texel has a coefficient of 0.0.

## SAMPLER\_STATE

		<b>Min Mode Filter</b>																									
	16:14	<table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U3 Enumerated Type</td></tr> </table> <p>This field determines how texels are sampled/filtered when a texture is being "minified" (shrunk). For volume maps, this filter mode selection also applies to the 3rd (inter-layer) dimension. See Mag Mode Filter</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0h</td><td>NEAREST</td><td>Sample the nearest texel</td></tr> <tr> <td>1h</td><td>LINEAR</td><td>Bilinearly filter the 4 nearest texels</td></tr> <tr> <td>2h</td><td>ANISOTROPIC</td><td>Perform an "anisotropic" filter on the chosen mip level</td></tr> <tr> <td>4h-5h</td><td>Reserved</td><td></td></tr> <tr> <td>6h</td><td>MONO</td><td>Perform a monochrome convolution filter</td></tr> <tr> <td>7h</td><td>Reserved</td><td></td></tr> </tbody> </table>	Project:	All	Format:	U3 Enumerated Type	Value	Name	Description	0h	NEAREST	Sample the nearest texel	1h	LINEAR	Bilinearly filter the 4 nearest texels	2h	ANISOTROPIC	Perform an "anisotropic" filter on the chosen mip level	4h-5h	Reserved		6h	MONO	Perform a monochrome convolution filter	7h	Reserved	
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	13:1	<b>Texture LOD Bias</b>																									
		<table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>S4.8 2's complement</td></tr> </table> <p>Range: [-16.0, 16.0)</p> <p>This field specifies the signed bias value added to the calculated texture map LOD prior to min-vs-mag determination and mip-level clamping. Assuming mipmapping is enabled, a positive LOD bias will result in a somewhat blurrier image (using less-detailed mip levels) and possibly higher performance, while a negative bias will result in a somewhat crisper image (using more-detailed mip levels) and may lower performance.</p>	Project:	All	Format:	S4.8 2's complement																					
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		There is no requirement or need to offset the LOD Bias in order to produce a correct LOD for texture filtering (as was required for correct bilinear and anisotropic filtering in some legacy devices).																									
	0	<b>Anisotropic Algorithm</b>																									
		<table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U1 Enumerated Type</td></tr> </table> <p>Controls which algorithm is used for anisotropic filtering. Generally, the EWA approximation algorithm results in higher image quality than the legacy algorithm.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0h</td><td>LEGACY</td><td>Use the legacy algorithm for anisotropic filtering</td></tr> <tr> <td>1h</td><td>EWA Approximation</td><td>Use the new EWA approximation algorithm for anisotropic filtering</td></tr> </tbody> </table>	Project:	All	Format:	U1 Enumerated Type	Value	Name	Description	0h	LEGACY	Use the legacy algorithm for anisotropic filtering	1h	EWA Approximation	Use the new EWA approximation algorithm for anisotropic filtering												
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1	31:20	<b>Min LOD</b>		
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Project:	All			
Format:	U4.8 in LOD units			
Range: [0.0, 14.0], where the upper limit is also bounded by the Max LOD.				
This field specifies the minimum value used to clamp the computed LOD after LOD bias is applied. Note that the minification-vs.-magnification status is determined after LOD bias and before this maximum (resolution) mip clamping is applied. The integer bits of this field are used to control the "maximum" (highest resolution) mipmap level that may be accessed (where LOD 0 is the highest resolution map). The fractional bits of this value effectively clamp the inter-level trilinear blend factor when trilinear filtering is in use.				
<b>Programming Notes</b>				
If Min LOD is greater than Max LOD, Min LOD takes precedence, i.e. the resulting LOD will always be Min LOD.				
This field must be zero if the Min or Mag Mode Filter is set to MAPFILTER_MONO				
19:8		<b>Max LOD</b>		
		<table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U4.8 in LOD units</td></tr> </table>	Project:	All
Project:	All			
Format:	U4.8 in LOD units			
Range: [0.0, 14.0]				
This field specifies the maximum value used to clamp the computed LOD after LOD bias is applied. Note that the minification-vs.-magnification status is determined after LOD bias and before this minimum (resolution) mip clamping is applied. The integer bits of this field are used to control the "minimum" (lowest resolution) mipmap level that may be accessed. The fractional bits of this value effectively clamp the inter-level trilinear blend factor when trilinear filtering is in use. Force the mip map access to be between the mipmap specified by the integer bits of the Min LOD and the ceiling of the value specified here.				
7		<b>ChromaKey Enable</b>		
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>Enable This field enables the chroma key function.</td></tr> </table>	Project:	BDW
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Format:	Enable This field enables the chroma key function.			
<b>Programming Notes</b>				
Supported only on a specific subset of surface formats. See section titled: "Surface Formats" in this volume for supported formats. This field must be disabled if min or mag filter is MAPFILTER_MONO or MAPFILTER_ANISOTROPIC. This field must be disabled if used with a surface of type SURFTYPE_3D.				

## SAMPLER\_STATE

		<b>ChromaKey Index</b>				
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>U2</td></tr> </table>	Project:	BDW	Format:	U2
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Format:	U2					
		Range: [0, 3]				
		<p>This field specifies the index of the ChromaKey Table entry associated with this Sampler. This field is a "don't care" unless <b>ChromaKey Enable</b> is ENABLED.</p>				
		<b>ChromaKey Mode</b>				
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Project:	BDW					
Format:	U1 Enumerated Type					
		<p>This field specifies the behavior of the device in the event of a ChromaKey match. This field is ignored if ChromaKey is disabled.</p> <p>KEYFILTER_REPLACE_BLACK: In this mode, each texel that matches the chroma key is replaced with (0,0,0,0) (black with alpha=0) prior to filtering. For YCrCb surface formats, the black value is A=0, R(Cr)=0x80, G(Y)=0x10, B(Cb)=0x80. This will tend to darken/fade edges of keyed regions. Note that the pixel pipeline must be programmed to use the resulting filtered texel value to gain the intended effect, e.g., handle the case of a totally keyed-out region (filtered texel alpha==0) through use of alpha test, etc.</p>				
Value	Name	Description				
0h	KEYFILTER_KILL_ON_ANY_MATCH	In this mode, if any contributing texel matches the chroma key, the corresponding pixel mask bit for that pixel is cleared. The result of this operation is observable only if the Killed Pixel Mask Return flag is set on the input message.				
1h	KEYFILTER_REPLACE_BLACK	In this mode, each texel that matches the chroma key is replaced with (0,0,0,0) (black with alpha=0) prior to filtering. For YCrCb surface formats, the black value is A=0, R(Cr)=0x80, G(Y)=0x10, B(Cb)=0x80. This will tend to darken/fade edges of keyed regions. Note that the pixel pipeline must be programmed to use the resulting filtered texel value to gain the intended effect, e.g., handle the case of a totally keyed-out region (filtered texel alpha==0) through use of alpha test, etc.				

## SAMPLER\_STATE

		<b>Shadow Function</b>																						
	3:1	<table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U3 Enumerated Type</td></tr> </table> <p>This field is used for shadow mapping support via the sample_c message type, and specifies the specific comparison operation to be used. The comparison is between the texture sample red channel (except for alpha-only formats which use the alpha channel), and the "ref" value provided in the input message.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0h</td><td>PREFILTEROP_ALWAYS</td></tr> <tr> <td>1h</td><td>PREFILTEROP_NEVER</td></tr> <tr> <td>2h</td><td>PREFILTEROP_LESS</td></tr> <tr> <td>3h</td><td>PREFILTEROP_EQUAL</td></tr> <tr> <td>4h</td><td>PREFILTEROP_LEQUAL</td></tr> <tr> <td>5h</td><td>PREFILTEROP_GREATER</td></tr> <tr> <td>6h</td><td>PREFILTEROP_NOTEQUAL</td></tr> <tr> <td>7h</td><td>PREFILTEROP_GEQUAL</td></tr> </tbody> </table>	Project:	All	Format:	U3 Enumerated Type	Value	Name	0h	PREFILTEROP_ALWAYS	1h	PREFILTEROP_NEVER	2h	PREFILTEROP_LESS	3h	PREFILTEROP_EQUAL	4h	PREFILTEROP_LEQUAL	5h	PREFILTEROP_GREATER	6h	PREFILTEROP_NOTEQUAL	7h	PREFILTEROP_GEQUAL
Project:	All																							
Format:	U3 Enumerated Type																							
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	0	<b>Cube Surface Control Mode</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U1 Enumerated Type</td></tr> </table> <p>When sampling from a SURFTYPE_CUBE surface, this field controls whether the TC* Address Control Mode fields are interpreted as programmed or overridden to TEXCOORDMODE_CUBE.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0h</td><td>PROGRAMMED</td></tr> <tr> <td>1h</td><td>OVERRIDE</td></tr> </tbody> </table> <p><b>Programming Notes</b></p> <p>This field must be set to CUBECTRLMODE_PROGRAMMED</p>	Project:	All	Format:	U1 Enumerated Type	Value	Name	0h	PROGRAMMED	1h	OVERRIDE												
Project:	All																							
Format:	U1 Enumerated Type																							
Value	Name																							
0h	PROGRAMMED																							
1h	OVERRIDE																							
2	31:30	<b>Reserved</b>																						
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> </table>	Project:	BDW																				
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	29:28	<b>Reserved</b>																						
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> </table>	Project:	BDW																				
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	27:26	<b>Reserved</b>																						
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	31:24	<b>Reserved</b>																						
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Project:	BDW																							
	25:24	<b>Reserved</b>																						
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> </table>	Project:	BDW																				
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## SAMPLER\_STATE

	23:6	<b>Indirect State Pointer</b>											
		Project:	BDW										
		<b>Description</b>											
		This pointer is relative to the Dynamic State Base Address.											
	5	<b>Reserved</b>											
		Project:	BDW										
		Format:	MBZ										
	4	<b>Reserved</b>											
		Project:	BDW										
	3	<b>Reserved</b>											
		Project:	BDW										
	2	<b>Reserved</b>											
		Project:	BDW										
	1	<b>Reserved</b>											
		Project:	BDW										
	0	<b>LOD Clamp Magnification Mode</b>											
		Project:	BDW										
		Format:	U1 Enumerated Type										
		This field allows the flexibility to control how LOD clamping is handled when in magnification mode.											
		<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: left; padding: 2px;">Value</th> <th style="text-align: left; padding: 2px;">Name</th> <th style="text-align: left; padding: 2px;">Description</th> </tr> </thead> <tbody> <tr> <td style="padding: 2px;">0h</td> <td style="padding: 2px;">MIPNONE</td> <td style="padding: 2px;">When in magnification mode, Sampler will clamp LOD as if the <b>Mip Mode Filter</b> is MIPFILTER_NONE. This is how OpenGL defines magnification, and therefore it is expected that those drivers would not set this bit.</td> </tr> <tr> <td style="padding: 2px;">1h</td> <td style="padding: 2px;">MIPFILTER</td> <td style="padding: 2px;">When in magnification mode, Sampler will clamp LOD based on the value of <b>Mip Mode Filter</b>.</td> </tr> </tbody> </table>			Value	Name	Description	0h	MIPNONE	When in magnification mode, Sampler will clamp LOD as if the <b>Mip Mode Filter</b> is MIPFILTER_NONE. This is how OpenGL defines magnification, and therefore it is expected that those drivers would not set this bit.	1h	MIPFILTER	When in magnification mode, Sampler will clamp LOD based on the value of <b>Mip Mode Filter</b> .
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	3	<b>Reserved</b>											
		Project:	BDW										
	23:22	<b>Reserved</b>											
		Project:	BDW										
		Format:	MBZ										

<b>SAMPLER_STATE</b>																																	
21:19	<b>Maximum Anisotropy</b>																																
<table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U3 Enumerated Type</td></tr> </table> <p>This field clamps the maximum value of the anisotropy ratio used by the MAPFILTER_ANISOTROPIC filter (Min or Mag Mode Filter).</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0h</td><td>RATIO 2:1</td><td>At most a 2:1 aspect ratio filter is used</td></tr> <tr> <td>1h</td><td>RATIO 4:1</td><td>At most a 4:1 aspect ratio filter is used</td></tr> <tr> <td>2h</td><td>RATIO 6:1</td><td>At most a 6:1 aspect ratio filter is used</td></tr> <tr> <td>3h</td><td>RATIO 8:1</td><td>At most a 8:1 aspect ratio filter is used</td></tr> <tr> <td>4h</td><td>RATIO 10:1</td><td>At most a 10:1 aspect ratio filter is used</td></tr> <tr> <td>5h</td><td>RATIO 12:1</td><td>At most a 12:1 aspect ratio filter is used</td></tr> <tr> <td>6h</td><td>RATIO 14:1</td><td>At most a 14:1 aspect ratio filter is used</td></tr> <tr> <td>7h</td><td>RATIO 16:1</td><td>At most a 16:1 aspect ratio filter is used</td></tr> </tbody> </table>			Project:	All	Format:	U3 Enumerated Type	Value	Name	Description	0h	RATIO 2:1	At most a 2:1 aspect ratio filter is used	1h	RATIO 4:1	At most a 4:1 aspect ratio filter is used	2h	RATIO 6:1	At most a 6:1 aspect ratio filter is used	3h	RATIO 8:1	At most a 8:1 aspect ratio filter is used	4h	RATIO 10:1	At most a 10:1 aspect ratio filter is used	5h	RATIO 12:1	At most a 12:1 aspect ratio filter is used	6h	RATIO 14:1	At most a 14:1 aspect ratio filter is used	7h	RATIO 16:1	At most a 16:1 aspect ratio filter is used
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18	<b>U Address Mag Filter Rounding Enable</b>																																
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17	<b>U Address Min Filter Rounding Enable</b>																																
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16	<b>V Address Mag Filter Rounding Enable</b>																																
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## SAMPLER\_STATE

		<b>V Address Min Filter Rounding Enable</b>															
	15	<table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>Enable</td></tr> </table> <p>Controls whether the texture address is rounded or truncated before being used to select texels to sample. Provides independent control of rounding on one texture address dimension (U/V/R) in either mag or min filter mode.</p>	Project:	All	Format:	Enable											
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Format:	Enable																
		<b>Programming Notes</b>															
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	14	<b>R Address Mag Filter Rounding Enable</b>															
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	13	<b>R Address Min Filter Rounding Enable</b>															
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Format:	Enable																
		<b>Programming Notes</b>															
		Hardware will <b>not</b> force rounding enable.															
	12:11	<b>Trilinear Filter Quality</b>															
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>U2 Enumerated Type</td></tr> </table> <p>Selects the quality level for the trilinear filter.</p>	Project:	BDW	Format:	U2 Enumerated Type											
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Format:	U2 Enumerated Type																
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0</td><td>FULL</td><td>Full Quality. Both mip maps are sampled under all circumstances.</td></tr> <tr> <td>1</td><td>HIGH</td><td>High Quality. Same as full quality.</td></tr> <tr> <td>2</td><td>MED</td><td>Medium Quality. If the contribution of one mip map is less than 25%, only the other mip map contributes.</td></tr> <tr> <td>3</td><td>LOW</td><td>Low Quality. If the contribution of one mip map is less than 37.5%, only the other mip map contributes.</td></tr> </tbody> </table>	Value	Name	Description	0	FULL	Full Quality. Both mip maps are sampled under all circumstances.	1	HIGH	High Quality. Same as full quality.	2	MED	Medium Quality. If the contribution of one mip map is less than 25%, only the other mip map contributes.	3	LOW	Low Quality. If the contribution of one mip map is less than 37.5%, only the other mip map contributes.
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## SAMPLER\_STATE

		<b>Non-normalized Coordinate Enable</b>				
	10	<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>Enable</td></tr> </table> <p>This field, if enabled, specifies that the input coordinates (U/V/R) are in non-normalized space, where each integer increment is one texel on LOD 0. If disabled, coordinates are normalized, where the range 0 to 1 spans the entire surface.</p>	Project:	BDW	Format:	Enable
Project:	BDW					
Format:	Enable					
		<b>Programming Notes</b> <p>The following state must be set as indicated if this field is <i>enabled</i>:</p> <ul style="list-style-type: none"> <li>TCX/Y/Z Address Control Mode must be TEXCOORDMODE_CLAMP, TEXCOORDMODE_HALF_BORDER, or TEXCOORDMODE_CLAMP_BORDER.</li> <li>Surface Type must be SURFTYPE_2D or SURFTYPE_3D.</li> <li>Mag Mode Filter must be MAPFILTER_NEAREST or MAPFILTER_LINEAR.</li> <li>Min Mode Filter must be MAPFILTER_NEAREST or MAPFILTER_LINEAR.</li> <li>Mip Mode Filter must be MIPFILTER_NONE.</li> <li>Min LOD must be 0.</li> <li>Max LOD must be 0.</li> <li>MIP Count must be 0.</li> <li>Surface Min LOD must be 0.</li> <li>Texture LOD Bias must be 0.</li> </ul>				
	9	<b>Reserved</b>				
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	BDW	Format:	MBZ
Project:	BDW					
Format:	MBZ					
	8:6	<b>TCX Address Control Mode</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>Texture Coordinate Mode [BDW]</b> Enumerated Type</td></tr> </table> <p>Controls how the 1st (TCX, aka U) component of input texture coordinates are mapped to texture map addresses - specifically, how coordinates "outside" the texture are handled (wrap/clamp/mirror). The setting of this field is subject to being overridden by the Cube Surface Control Mode field when sampling from a SURFTYPE_CUBE surface.</p>	Project:	All	Format:	<b>Texture Coordinate Mode [BDW]</b> Enumerated Type
Project:	All					
Format:	<b>Texture Coordinate Mode [BDW]</b> Enumerated Type					
		<b>Programming Notes</b> <p>When using cube map texture coordinates, each TC component must have the same Address Control Mode.</p>				
		<p>When TEXCOORDMODE_CUBE is not used accessing a cube map, the map's Cube Face Enable field must be programmed to 111111b (all faces enabled).</p>				
		<p>MAPFILTER_MONO: Texture addressing modes must all be set to TEXCOORDMODE_CLAMP_BORDER. The <b>Border Color</b> is ignored in this mode, a constant value of 0 is used for border color. Software must pad the border texels within the map itself with 0.</p>				
		<p>If <b>Surface Format</b> is PLANAR*, this field must be set to TEXCOORDMODE_CLAMP.</p>				

## SAMPLER\_STATE

		<b>TCY Address Control Mode</b>				
		<table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>Texture Coordinate Mode [BDW]</b> Enumerated Type</td></tr> </table>	Project:	All	Format:	<b>Texture Coordinate Mode [BDW]</b> Enumerated Type
Project:	All					
Format:	<b>Texture Coordinate Mode [BDW]</b> Enumerated Type					
		Controls how the 2nd (TCY, aka V) component of input texture coordinates are mapped to texture map addresses - specifically, how coordinates "outside" the texture are handled (wrap/clamp/mirror). See Address TCX Control Mode above for details				
		<b>Programming Notes</b>				
		If this field is set to TEXCOORDMODE_CLAMP_BORDER or TEXCOORDMODE_HALF_BORDER and a 1D surface is sampled, incorrect blending with the border color in the vertical direction may occur.				
		<b>TCZ Address Control Mode</b>				
		<table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>Texture Coordinate Mode [BDW]</b> Enumerated Type</td></tr> </table>	Project:	All	Format:	<b>Texture Coordinate Mode [BDW]</b> Enumerated Type
Project:	All					
Format:	<b>Texture Coordinate Mode [BDW]</b> Enumerated Type					
		<b>Description</b>				
		Controls how the 3rd (TCZ) component of input texture coordinates are mapped to texture map addresses - specifically, how coordinates "outside" the texture are handled (wrap/clamp/mirror). See Address TCX Control Mode above for details				
		If this field is set to TEXCOORDMODE_CLAMP_BORDER or TEXCOORDMODE_HALF_BORDER and a 3D surface is sampled, incorrect blending with the border color in the Q direction may occur.				

## SCISSOR\_RECT

SCISSOR_RECT										
DWord	Bit	Description								
0	31:16	<p><b>Scissor Rectangle Y Min</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U16 Pixels from Drawing Rectangle origin (upper left corner)</td> </tr> </table> <p>Specifies Y Min coordinate of (inclusive) Scissor Rectangle used for scissor test. Pixels with (Draw Rectangle-relative) Y coordinates less than Y Min will be clipped out if Scissor Rectangle is enabled. NOTE: If Y Min is set to a value greater than Y Max, all primitives will be discarded for this viewport.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>[0,16383]</td> <td></td> </tr> </tbody> </table>	Project:	All	Format:	U16 Pixels from Drawing Rectangle origin (upper left corner)	Value	Name	[0,16383]	
Project:	All									
Format:	U16 Pixels from Drawing Rectangle origin (upper left corner)									
Value	Name									
[0,16383]										
0	15:0	<p><b>Scissor Rectangle X Min</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U16 Pixels from Drawing Rectangle origin (upper left corner)</td> </tr> </table> <p>Specifies X Min coordinate of (inclusive) Scissor Rectangle used for scissor test. Pixels with (Draw Rectangle-relative) X coordinates less than X Min will be clipped out if Scissor Rectangle is enabled. NOTE: If X Min is set to a value greater than X Max, all primitives will be discarded for this viewport.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>[0,16383]</td> <td></td> </tr> </tbody> </table>	Project:	All	Format:	U16 Pixels from Drawing Rectangle origin (upper left corner)	Value	Name	[0,16383]	
Project:	All									
Format:	U16 Pixels from Drawing Rectangle origin (upper left corner)									
Value	Name									
[0,16383]										
1	31:16	<p><b>Scissor Rectangle Y Max</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U16 Pixels from Drawing Rectangle origin (upper left corner)</td> </tr> </table> <p>Specifies Y Max coordinate of (inclusive) Scissor Rectangle used for scissor test. Pixels with (Draw Rectangle-relative) Y coordinates greater than Y Max will be clipped out if Scissor Rectangle is enabled.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>[0,16383]</td> <td></td> </tr> </tbody> </table>	Project:	All	Format:	U16 Pixels from Drawing Rectangle origin (upper left corner)	Value	Name	[0,16383]	
Project:	All									
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Value	Name									
[0,16383]										

## SCISSOR\_RECT

15:0	<b>Scissor Rectangle X Max</b> <table border="1"><tr><td>Project:</td><td>All</td></tr><tr><td>Format:</td><td>U16 Pixels from Drawing Rectangle origin (upper left corner)</td></tr></table> <p>Specifies X Max coordinate of (inclusive) Scissor Rectangle used for scissor test. Pixels with (Draw Rectangle-relative) Y coordinates greater than X Max will be clipped out if Scissor Rectangle is enabled.</p> <table border="1"><thead><tr><th>Value</th><th>Name</th><th>Project</th></tr></thead><tbody><tr><td>0-16383</td><td></td><td>BDW</td></tr></tbody></table>	Project:	All	Format:	U16 Pixels from Drawing Rectangle origin (upper left corner)	Value	Name	Project	0-16383		BDW
Project:	All										
Format:	U16 Pixels from Drawing Rectangle origin (upper left corner)										
Value	Name	Project									
0-16383		BDW									

## Scratch Hword Block Message Header

<b>MH_A32_HWB - Scratch Hword Block Message Header</b>								
<b>DWord</b>	<b>Bit</b>	<b>Description</b>						
0-2	95:0	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Ignore</td> </tr> <tr> <td colspan="2">Ignored</td></tr> </table>	Project:	All	Format:	Ignore	Ignored	
Project:	All							
Format:	Ignore							
Ignored								
3	31:0	<p><b>Per Thread Scratch Space</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td><b>MHC_PTSS</b></td> </tr> <tr> <td colspan="2">Specifies amount of scratch space used by this thread, for Stateless bounds checking.</td></tr> </table>	Project:	All	Format:	<b>MHC_PTSS</b>	Specifies amount of scratch space used by this thread, for Stateless bounds checking.	
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Format:	Ignore							
Ignored								
5	31:0	<p><b>Buffer Base Address</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td><b>MHC_A32_BBA</b></td> </tr> <tr> <td colspan="2">Specifies the surface address offset page [31:10] for A32 stateless messages.</td></tr> </table>	Project:	All	Format:	<b>MHC_A32_BBA</b>	Specifies the surface address offset page [31:10] for A32 stateless messages.	
Project:	All							
Format:	<b>MHC_A32_BBA</b>							
Specifies the surface address offset page [31:10] for A32 stateless messages.								
6-7	63:0	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Ignore</td> </tr> <tr> <td colspan="2">Ignored</td></tr> </table>	Project:	All	Format:	Ignore	Ignored	
Project:	All							
Format:	Ignore							
Ignored								

## SF\_CLIP\_VIEWPORT

SF_CLIP_VIEWPORT				
DWord	Bit	Description		
0	31:0	<b>Viewport Matrix Element m00</b> <table border="1"> <tr> <td>Format:</td> <td>IEEE_Float</td> </tr> </table>	Format:	IEEE_Float
Format:	IEEE_Float			
1	31:0	<b>Viewport Matrix Element m11</b> <table border="1"> <tr> <td>Format:</td> <td>IEEE_Float</td> </tr> </table>	Format:	IEEE_Float
Format:	IEEE_Float			
2	31:0	<b>Viewport Matrix Element m22</b> <table border="1"> <tr> <td>Format:</td> <td>IEEE_Float</td> </tr> </table>	Format:	IEEE_Float
Format:	IEEE_Float			
3	31:0	<b>Viewport Matrix Element m30</b> <table border="1"> <tr> <td>Format:</td> <td>IEEE_Float</td> </tr> </table>	Format:	IEEE_Float
Format:	IEEE_Float			
4	31:0	<b>Viewport Matrix Element m31</b> <table border="1"> <tr> <td>Format:</td> <td>IEEE_Float</td> </tr> </table>	Format:	IEEE_Float
Format:	IEEE_Float			
5	31:0	<b>Viewport Matrix Element m32</b> <table border="1"> <tr> <td>Format:</td> <td>IEEE_Float</td> </tr> </table>	Format:	IEEE_Float
Format:	IEEE_Float			
6	31:0	<b>Reserved</b> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ
Format:	MBZ			
7	31:0	<b>Reserved</b> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ
Format:	MBZ			
8	31:0	<b>X Min Clip Guardband</b> <table border="1"> <tr> <td>Format:</td> <td>IEEE_Float</td> </tr> </table> <p>. This 32-bit float represents the XMin guardband boundary (normalized to Viewport.XMin == -1.0f). This corresponds to the left boundary of the NDC guardband.</p> <p style="text-align: center;"><b>Workaround</b></p> <p>Workaround: Minimum allowed value for this field is -16384.</p>	Format:	IEEE_Float
Format:	IEEE_Float			
9	31:0	<b>X Max Clip Guardband</b> <table border="1"> <tr> <td>Format:</td> <td>IEEE_Float</td> </tr> </table> <p>This 32-bit float represents the XMax guardband boundary (normalized to Viewport..XMax == 1.0f). This corresponds to the right boundary of the NDC guardband.</p> <p style="text-align: center;"><b>Workaround</b></p> <p>Workaround: Maximum allowed value for this field is 16383.</p>	Format:	IEEE_Float
Format:	IEEE_Float			

SF_CLIP_VIEWPORT						
10	31:0	<p><b>Y Min Clip Guardband</b></p> <table border="1"> <tr> <td>Format:</td><td>IEEE_Float</td></tr> </table> <p>This 32-bit float represents the YMin guardband boundary (normalized to Viewport.YMin == -1.0f). This corresponds to the bottom boundary of the NDC guardband.</p> <p style="text-align: center;"><b>Workaround</b></p> <p>Workaround: Minimum allowed value for this field is -16384.</p>	Format:	IEEE_Float		
Format:	IEEE_Float					
11	31:0	<p><b>Y Max Clip Guardband</b></p> <table border="1"> <tr> <td>Format:</td><td>IEEE_Float</td></tr> </table> <p>This 32-bit float represents the YMax guardband boundary (normalized to Viewport.YMax == 1.0f). This corresponds to the top boundary of the NDC guardband.</p> <p style="text-align: center;"><b>Workaround</b></p> <p>Workaround: Maximum allowed value for this field is 16383.</p>	Format:	IEEE_Float		
Format:	IEEE_Float					
12 <b>Project:</b> BDW	31:0	<p><b>X Min ViewPort</b></p> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>IEEE_Float</td></tr> </table> <p>This 32-bit float represents the Viewport.XMin.</p> <p>This is the X min of the viewport extents as programmed by API, and this value should be programmed in Screen Space coordinate and not as normalized coordinate.</p>	Project:	BDW	Format:	IEEE_Float
Project:	BDW					
Format:	IEEE_Float					
13 <b>Project:</b> BDW	31:0	<p><b>X Max ViewPort</b></p> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>IEEE_Float</td></tr> </table> <p>This 32-bit float represents the Viewport.XMax.</p> <p>This is the X max of the viewport extents as programmed by API, and this value should be programmed in Screen Space coordinate and not as normalized coordinate.</p>	Project:	BDW	Format:	IEEE_Float
Project:	BDW					
Format:	IEEE_Float					
14 <b>Project:</b> BDW	31:0	<p><b>Y Min ViewPort</b></p> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>IEEE_Float</td></tr> </table> <p>This 32-bit float represents the Viewport.YMin.</p> <p>This is the Y min of the viewport extents as programmed by API, and this value should be programmed in Screen Space coordinate and not as normalized coordinate.</p>	Project:	BDW	Format:	IEEE_Float
Project:	BDW					
Format:	IEEE_Float					

## SF\_CLIP\_VIEWPORT

15	31:0	<b>Y Max ViewPort</b>
<b>Project:</b> BDW		Project: BDW
		Format: IEEE_Float
This 32-bit float represents the Viewport.Ymax.		
This is the Y max of the viewport extents as programmed by API, and this value should be programmed in Screen Space coordinate and not as normalized coordinate.		

## SF\_OUTPUT\_ATTRIBUTE\_DETAIL

SF_OUTPUT_ATTRIBUTE_DETAIL				
DWord	Bit	Description		
0	15	<p><b>Component Override W</b></p> <table border="1"> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>If set, the W component of this output Attribute is overridden by the W component of the constant vector specified by ConstantSource.</p>	Format:	Enable
Format:	Enable			
	14	<p><b>Component Override Z</b></p> <table border="1"> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>If set, the Z component of this output Attribute is overridden by the Z component of the constant vector specified by ConstantSource.</p>	Format:	Enable
Format:	Enable			
	13	<p><b>Component Override Y</b></p> <table border="1"> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>If set, the Y component of output Attribute is overridden by the Y component of the constant vector specified by ConstantSource.</p>	Format:	Enable
Format:	Enable			
	12	<p><b>Component Override X</b></p> <table border="1"> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>If set, the X component of output Attribute is overridden by the X component of the constant vector specified by ConstantSource.</p>	Format:	Enable
Format:	Enable			

<b>SF_OUTPUT_ATTRIBUTE_DETAIL</b>																			
11	<b>Swizzle Control Mode</b>	<table border="1" style="width: 100%;"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>U1 Enumerated Type</td></tr> </table> <p>When Attribute Swizzle Enable is ENABLED, this bit controls whether attributes 0-15 or 16-31 are subject to the following swizzle controls:</p> <ul style="list-style-type: none"> <li>• Component Override X/Y/Z/W</li> <li>• Constant Source</li> <li>• Swizzle Select</li> <li>• Source Attribute</li> <li>• WrapShortest Enables</li> </ul> <p>Note that the Number of SF Output Attributes field specifies how many attributes are output.</p> <p>Note: This field does not impact any functions which provide separate states for all 32 attributes (e.g., Point sprite, Constant interpolation).</p> <p>Note: This field is only valid for the first indexed attribute (Attribute[0]). For all other indices, it is Reserved and MBZ.</p>	Project:	BDW	Format:	U1 Enumerated Type													
Project:	BDW																		
Format:	U1 Enumerated Type																		
10:9	<b>Constant Source</b>	<table border="1" style="width: 100%;"> <tr> <td>Format:</td><td>U2 enumerated type</td></tr> </table> <p>This state selects a constant vector which can be used to override individual components of this Attribute</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #d9e1f2;"> <th style="text-align: center; padding: 2px;"><b>Value</b></th><th style="text-align: center; padding: 2px;"><b>Name</b></th><th style="text-align: center; padding: 2px;"><b>Description</b></th></tr> </thead> <tbody> <tr> <td style="text-align: center; padding: 2px;">0h</td><td style="text-align: center; padding: 2px;">CONST_0000</td><td style="text-align: center; padding: 2px;">Constant.xyzw = 0.0,0.0,0.0,0.0</td></tr> <tr> <td style="text-align: center; padding: 2px;">1h</td><td style="text-align: center; padding: 2px;">CONST_0001_FLOAT</td><td style="text-align: center; padding: 2px;">Constant.xyzw = 0.0,0.0,0.0,1.0</td></tr> <tr> <td style="text-align: center; padding: 2px;">2h</td><td style="text-align: center; padding: 2px;">CONST_1111_FLOAT</td><td style="text-align: center; padding: 2px;">Constant.xyzw = 1.0,1.0,1.0,1.0</td></tr> <tr> <td style="text-align: center; padding: 2px;">3h</td><td style="text-align: center; padding: 2px;">PRIM_ID</td><td style="text-align: center; padding: 2px;">Constant.xyzw = PrimID (replicated)</td></tr> </tbody> </table>	Format:	U2 enumerated type	<b>Value</b>	<b>Name</b>	<b>Description</b>	0h	CONST_0000	Constant.xyzw = 0.0,0.0,0.0,0.0	1h	CONST_0001_FLOAT	Constant.xyzw = 0.0,0.0,0.0,1.0	2h	CONST_1111_FLOAT	Constant.xyzw = 1.0,1.0,1.0,1.0	3h	PRIM_ID	Constant.xyzw = PrimID (replicated)
Format:	U2 enumerated type																		
<b>Value</b>	<b>Name</b>	<b>Description</b>																	
0h	CONST_0000	Constant.xyzw = 0.0,0.0,0.0,0.0																	
1h	CONST_0001_FLOAT	Constant.xyzw = 0.0,0.0,0.0,1.0																	
2h	CONST_1111_FLOAT	Constant.xyzw = 1.0,1.0,1.0,1.0																	
3h	PRIM_ID	Constant.xyzw = PrimID (replicated)																	
8	<b>Reserved</b>	<table border="1" style="width: 100%;"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ															
Format:	MBZ																		

SF_OUTPUT_ATTRIBUTE_DETAIL				
7:6		<b>Swizzle Select</b>		
<table border="1" style="width: 100%;"> <tr> <td style="padding: 2px;">Format:</td><td style="padding: 2px;">U2 enumerated type</td></tr> </table> <p>This state, along with Source Attribute, specifies the source for this output Attribute.</p>			Format:	U2 enumerated type
Format:	U2 enumerated type			
Value	Name	Description		
0h	INPUTATTR	This attribute is sourced from AttrInputReg[SourceAttribute]		
1h	INPUTATTR_FACING	If the object is front-facing, this attribute is sourced from AttrInputReg[SourceAttribute]. If the object is back-facing, this attribute is sourced from AttrInputReg[SourceAttribute+1].		
2h	INPUTATTR_W	This attribute is sourced from AttrInputReg[SourceAttribute]. The W component is copied to the X component.		
3h	INPUTATTR_FACING_W	If the object is front-facing, this attribute is sourced from AttrInputReg[SourceAttribute]. If the object is back-facing, this attribute is sourced from AttrInputReg[SourceAttribute+1]. The W component is copied to the X component.		
5				
<b>Reserved</b>				
<table border="1" style="width: 100%;"> <tr> <td style="padding: 2px;">Format:</td><td style="padding: 2px;">MBZ</td></tr> </table>		Format:	MBZ	
Format:	MBZ			
4:0				
<b>Source Attribute</b>				
<table border="1" style="width: 100%;"> <tr> <td style="padding: 2px;">Format:</td><td style="padding: 2px;">U5</td></tr> </table>		Format:	U5	
Format:	U5			
<p>This field selects the source attribute for this Attribute. Source attribute 0 corresponds to the first 128 bits of data indicated by Vertex URB Entry Read Offset</p>				

## SFC\_8x8\_AVs\_COEFFICIENTS

SFC_8x8_AVs_COEFFICIENTS						
Project: BDW Size (in bits): 256 Default Value: 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000						
Description						
ExistsIf = AVS						
DWord	Bit	Description				
0	31:24	<b>ZeroYFilterCoefficient1</b> <table border="1"> <tr> <td>Format:</td> <td>S1.6 2's Complement</td> </tr> <tr> <td colspan="2"><b>Range:</b> [-2, +2)</td></tr> </table>	Format:	S1.6 2's Complement	<b>Range:</b> [-2, +2)	
Format:	S1.6 2's Complement					
<b>Range:</b> [-2, +2)						
23:16	<b>ZeroXFilterCoefficient1</b> <table border="1"> <tr> <td>Format:</td> <td>S1.6 2's Complement</td> </tr> <tr> <td colspan="2"><b>Range:</b> [-2, +2)</td></tr> </table>	Format:	S1.6 2's Complement	<b>Range:</b> [-2, +2)		
Format:	S1.6 2's Complement					
<b>Range:</b> [-2, +2)						
15:8	<b>ZeroYFilterCoefficient0</b> <table border="1"> <tr> <td>Format:</td> <td>S1.6 2's Complement</td> </tr> <tr> <td colspan="2"><b>Range:</b> [-2, +2)</td></tr> </table>	Format:	S1.6 2's Complement	<b>Range:</b> [-2, +2)		
Format:	S1.6 2's Complement					
<b>Range:</b> [-2, +2)						
7:0	<b>ZeroXFilterCoefficient0</b> <table border="1"> <tr> <td>Format:</td> <td>S1.6 2's Complement</td> </tr> <tr> <td colspan="2"><b>Range:</b> [-2, +2)</td></tr> </table>	Format:	S1.6 2's Complement	<b>Range:</b> [-2, +2)		
Format:	S1.6 2's Complement					
<b>Range:</b> [-2, +2)						
1	31:24	<b>ZeroYFilterCoefficient3</b> <table border="1"> <tr> <td>Format:</td> <td>S1.6 2's Complement</td> </tr> <tr> <td colspan="2"><b>Range:</b> [-2, +2)</td></tr> </table>	Format:	S1.6 2's Complement	<b>Range:</b> [-2, +2)	
Format:	S1.6 2's Complement					
<b>Range:</b> [-2, +2)						
23:16	<b>ZeroXFilterCoefficient3</b> <table border="1"> <tr> <td>Format:</td> <td>S1.6 2's Complement</td> </tr> <tr> <td colspan="2"><b>Range:</b> [-2, +2)</td></tr> </table>	Format:	S1.6 2's Complement	<b>Range:</b> [-2, +2)		
Format:	S1.6 2's Complement					
<b>Range:</b> [-2, +2)						
15:8	<b>ZeroYFilterCoefficient2</b> <table border="1"> <tr> <td>Format:</td> <td>S1.6 2's Complement</td> </tr> <tr> <td colspan="2"><b>Range:</b> [-2, +2)</td></tr> </table>	Format:	S1.6 2's Complement	<b>Range:</b> [-2, +2)		
Format:	S1.6 2's Complement					
<b>Range:</b> [-2, +2)						
7:0	<b>ZeroXFilterCoefficient2</b> <table border="1"> <tr> <td>Format:</td> <td>S1.6 2's Complement</td> </tr> <tr> <td colspan="2"><b>Range:</b> [-2, +2)</td></tr> </table>	Format:	S1.6 2's Complement	<b>Range:</b> [-2, +2)		
Format:	S1.6 2's Complement					
<b>Range:</b> [-2, +2)						

SFC_8x8_AVs_COEFFICIENTS			
2	31:24	<b>ZeroYFilterCoefficient5</b>	
		Format: S1.6 2's Complement	
	23:16	<b>ZeroXFilterCoefficient5</b>	
		Format: S1.6 2's Complement	
		Range: [-2, +2)	
	15:8	<b>ZeroYFilterCoefficient4</b>	
		Format: S1.6 2's Complement	
		Range: [-2, +2)	
	7:0	<b>ZeroXFilterCoefficient4</b>	
		Format: S1.6 2's Complement	
		Range: [-2, +2)	
3	31:24	<b>ZeroYFilterCoefficient7</b>	
		Format: S1.6 2's Complement	
	23:16	<b>ZeroXFilterCoefficient7</b>	
		Format: S1.6 2's Complement	
		Range: [-2, +2)	
	15:8	<b>ZeroYFilterCoefficient6</b>	
		Format: S1.6 2's Complement	
		Range: [-2, +2)	
	7:0	<b>ZeroXFilterCoefficient6</b>	
		Format: S1.6 2's Complement	
		Range: [-2, +2)	
4	31:24	<b>OneXFilterCoefficient3</b>	
		Format: S1.6 2's Complement	
		Range: [-2.0, +2.0)	
	23:16	<b>OneXFilterCoefficient2</b>	
		Format: S1.6 2's Complement	
		Range: [-1.0, +1.0)	

<b>SFC_8x8_AV_S_COEFFICIENTS</b>			
	15:0	<b>Reserved</b>	
5	31:16	<b>Reserved</b>	
	15:8	<b>OneXFilterCoefficient5</b>	
	7:0	<b>OneXFilterCoefficient4</b>	
6	31:24	<b>OneYFilterCoefficient3</b>	
	23:16	<b>OneYFilterCoefficient2</b>	
	15:0	<b>Reserved</b>	
7	31:16	<b>Reserved</b>	
	15:8	<b>OneYFilterCoefficient5</b>	
	7:0	<b>OneYFilterCoefficient4</b>	

## SIMD4x2 Typed Surface 32-Bit Address Payload

MAP32B_TS SIMD4X2 - SIMD4x2 Typed Surface 32-Bit Address Payload				
DWord	Bit	Description		
0	31:0	<p><b>U0</b></p> <table border="1"> <tr> <td>Format:</td> <td>U32</td> </tr> </table> <p>Specifies the U channel address offset for slot 0.</p>	Format:	U32
Format:	U32			
1	31:0	<p><b>V0</b></p> <table border="1"> <tr> <td>Format:</td> <td>U32</td> </tr> </table> <p>Specifies the V channel address offset for slot 0.</p>	Format:	U32
Format:	U32			
2	31:0	<p><b>R0</b></p> <table border="1"> <tr> <td>Format:</td> <td>U32</td> </tr> </table> <p>Specifies the R channel address offset for slot 0.</p>	Format:	U32
Format:	U32			
3	31:0	<p><b>LOD0</b></p> <table border="1"> <tr> <td>Format:</td> <td><b>MACD_LOD</b></td> </tr> </table> <p>Specifies the LOD for slot 0.</p>	Format:	<b>MACD_LOD</b>
Format:	<b>MACD_LOD</b>			
4	31:0	<p><b>U1</b></p> <table border="1"> <tr> <td>Format:</td> <td>U32</td> </tr> </table> <p>Specifies the U channel address offset for slot 1.</p>	Format:	U32
Format:	U32			
5	31:0	<p><b>V1</b></p> <table border="1"> <tr> <td>Format:</td> <td>U32</td> </tr> </table> <p>Specifies the V channel address offset for slot 1.</p>	Format:	U32
Format:	U32			
6	31:0	<p><b>R1</b></p> <table border="1"> <tr> <td>Format:</td> <td>U32</td> </tr> </table> <p>Specifies the R channel address offset for slot 1.</p>	Format:	U32
Format:	U32			
7	31:0	<p><b>LOD1</b></p> <table border="1"> <tr> <td>Format:</td> <td><b>MACD_LOD</b></td> </tr> </table> <p>Specifies the LOD for slot 1.</p>	Format:	<b>MACD_LOD</b>
Format:	<b>MACD_LOD</b>			

## SIMD4x2 Untyped BUFFER Surface 32-Bit Address Payload

<b>MAP32B_USU SIMD4X2 - SIMD4x2 Untyped BUFFER Surface 32-Bit Address Payload</b>				
<b>DWord</b>	<b>Bit</b>	<b>Description</b>		
0	31:0	<p><b>U0</b></p> <table border="1"> <tr> <td>Format:</td> <td>U32</td> </tr> </table> <p>Specifies the U channel address offset for slot 0.</p>	Format:	U32
Format:	U32			
1-3	95:0	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>Ignore</td> </tr> </table> <p>Ignored</p>	Format:	Ignore
Format:	Ignore			
4	31:0	<p><b>U1</b></p> <table border="1"> <tr> <td>Format:</td> <td>U32</td> </tr> </table> <p>Specifies the U channel address offset for slot 1.</p>	Format:	U32
Format:	U32			
5-7	95:0	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>Ignore</td> </tr> </table> <p>Ignored</p>	Format:	Ignore
Format:	Ignore			

## SIMD4x2 Untyped BUFFER Surface 64-Bit Address Payload

<b>MAP64B_USU SIMD4X2 - SIMD4x2 Untyped BUFFER Surface 64-Bit Address Payload</b>				
<b>DWord</b>	<b>Bit</b>	<b>Description</b>		
0-1	63:0	<p><b>U0</b></p> <table border="1"> <tr> <td>Format:</td> <td>U64</td> </tr> </table> <p>Specifies the U channel address offset for slot 0.</p>	Format:	U64
Format:	U64			
2-3	63:0	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>Ignore</td> </tr> </table> <p>Ignored</p>	Format:	Ignore
Format:	Ignore			
4-5	63:0	<p><b>U1</b></p> <table border="1"> <tr> <td>Format:</td> <td>U64</td> </tr> </table> <p>Specifies the U channel address offset for slot 1.</p>	Format:	U64
Format:	U64			
6-7	63:0	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>Ignore</td> </tr> </table> <p>Ignored</p>	Format:	Ignore
Format:	Ignore			

## SIMD4x2 Untyped STRBUF Surface 32-Bit Address Payload

<b>MAP32B_USUV SIMD4X2 - SIMD4x2 Untyped STRBUF Surface 32-Bit Address Payload</b>				
<b>DWord</b>	<b>Bit</b>	<b>Description</b>		
0	31:0	<p><b>U0</b></p> <table border="1"> <tr> <td>Format:</td> <td>U32</td> </tr> </table> <p>Specifies the U channel address offset for slot 0.</p>	Format:	U32
Format:	U32			
1	31:0	<p><b>V0</b></p> <table border="1"> <tr> <td>Format:</td> <td>U32</td> </tr> </table> <p>Specifies the V channel address offset for slot 0.</p>	Format:	U32
Format:	U32			
2-3	63:0	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>Ignore</td> </tr> </table> <p>Ignored</p>	Format:	Ignore
Format:	Ignore			
4	31:0	<p><b>U1</b></p> <table border="1"> <tr> <td>Format:</td> <td>U32</td> </tr> </table> <p>Specifies the U channel address offset for slot 1.</p>	Format:	U32
Format:	U32			
5	31:0	<p><b>V1</b></p> <table border="1"> <tr> <td>Format:</td> <td>U32</td> </tr> </table> <p>Specifies the V channel address offset for slot 1.</p>	Format:	U32
Format:	U32			
6-7	63:0	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>Ignore</td> </tr> </table> <p>Ignored</p>	Format:	Ignore
Format:	Ignore			

## SIMD4x2 32-Bit Address Payload

<b>MAP32B SIMD4X2 - SIMD4x2 32-Bit Address Payload</b>				
<b>DWord</b>	<b>Bit</b>	<b>Description</b>		
0	31:0	<p><b>Offset0</b></p> <table border="1"> <tr> <td>Format:</td> <td>U32</td> </tr> </table> <p>Specifies the address offset for slot 0.</p>	Format:	U32
Format:	U32			
1-3	95:0	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>Ignore</td> </tr> </table> <p>Ignored</p>	Format:	Ignore
Format:	Ignore			
4	31:0	<p><b>Offset1</b></p> <table border="1"> <tr> <td>Format:</td> <td>U32</td> </tr> </table> <p>Specifies the address offset for slot 1.</p>	Format:	U32
Format:	U32			
5-7	95:0	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>Ignore</td> </tr> </table> <p>Ignored</p>	Format:	Ignore
Format:	Ignore			

## SIMD8 Dual Source Render Target Data Payload

<b>MDP_RTW_8DS - SIMD8 Dual Source Render Target Data Payload</b>						
<b>DWord</b>	<b>Bit</b>	<b>Description</b>				
0.0-0.7	255:0	<p><b>Src0 Red</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW_SIMD8</b></td></tr> </table> <p>Slots[7:0] or [15:8] of Src0 Red</p>	Project:	All	Format:	<b>MDP_DW_SIMD8</b>
Project:	All					
Format:	<b>MDP_DW_SIMD8</b>					
1.0-1.7	255:0	<p><b>Src0 Green</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW_SIMD8</b></td></tr> </table> <p>Slots[7:0] or [15:8] of Src0 Green</p>	Project:	All	Format:	<b>MDP_DW_SIMD8</b>
Project:	All					
Format:	<b>MDP_DW_SIMD8</b>					
2.0-2.7	255:0	<p><b>Src0 Blue</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW_SIMD8</b></td></tr> </table> <p>Slots[7:0] or [15:8] of Src0 Blue</p>	Project:	All	Format:	<b>MDP_DW_SIMD8</b>
Project:	All					
Format:	<b>MDP_DW_SIMD8</b>					
3.0-3.7	255:0	<p><b>Src0 Alpha</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW_SIMD8</b></td></tr> </table> <p>Slots[7:0] or [15:8] of Src0 Alpha</p>	Project:	All	Format:	<b>MDP_DW_SIMD8</b>
Project:	All					
Format:	<b>MDP_DW_SIMD8</b>					
4.0-4.7	255:0	<p><b>Src1 Red</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW_SIMD8</b></td></tr> </table> <p>Slots[7:0] or [15:8] of Src1 Red</p>	Project:	All	Format:	<b>MDP_DW_SIMD8</b>
Project:	All					
Format:	<b>MDP_DW_SIMD8</b>					

MDP_RTW_8DS - SIMD8 Dual Source Render Target Data Payload							
5.0-5.7	255:0	<b>Src1 Green</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW_SIMD8</b></td></tr> </table> Slots[7:0] or [15:8] of Src1 Green	Project:	All	Format:	<b>MDP_DW_SIMD8</b>	
Project:	All						
Format:	<b>MDP_DW_SIMD8</b>						
6.0-6.7	255:0	<b>Src1 Blue</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW_SIMD8</b></td></tr> </table> Slots[7:0] or [15:8] of Src1 Blue	Project:	All	Format:	<b>MDP_DW_SIMD8</b>	
Project:	All						
Format:	<b>MDP_DW_SIMD8</b>						
7.0-7.7	255:0	<b>Src1 Alpha</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW_SIMD8</b></td></tr> </table> Slots[7:0] or [15:8] of Src1 Alpha	Project:	All	Format:	<b>MDP_DW_SIMD8</b>	
Project:	All						
Format:	<b>MDP_DW_SIMD8</b>						

## SIMD8 LOD Message Address Payload Control

MACR_LOD SIMD8 - SIMD8 LOD Message Address Payload Control						
DWord	Bit	Description				
0.0	31:0	<b>Slot0 LOD</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MACD_LOD</b></td></tr> </table> Specifies the LOD for slot 0	Project:	All	Format:	<b>MACD_LOD</b>
Project:	All					
Format:	<b>MACD_LOD</b>					
0.1	31:0	<b>Slot1 LOD</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MACD_LOD</b></td></tr> </table> Specifies the LOD for slot 1	Project:	All	Format:	<b>MACD_LOD</b>
Project:	All					
Format:	<b>MACD_LOD</b>					
0.2	31:0	<b>Slot2 LOD</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MACD_LOD</b></td></tr> </table> Specifies the LOD for slot 2	Project:	All	Format:	<b>MACD_LOD</b>
Project:	All					
Format:	<b>MACD_LOD</b>					
0.3	31:0	<b>Slot3 LOD</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MACD_LOD</b></td></tr> </table> Specifies the LOD for slot 3	Project:	All	Format:	<b>MACD_LOD</b>
Project:	All					
Format:	<b>MACD_LOD</b>					
0.4	31:0	<b>Slot4 LOD</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MACD_LOD</b></td></tr> </table> Specifies the LOD for slot 4	Project:	All	Format:	<b>MACD_LOD</b>
Project:	All					
Format:	<b>MACD_LOD</b>					
0.5	31:0	<b>Slot5 LOD</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MACD_LOD</b></td></tr> </table> Specifies the LOD for slot 5	Project:	All	Format:	<b>MACD_LOD</b>
Project:	All					
Format:	<b>MACD_LOD</b>					

## MACR\_LOD SIMD8 - SIMD8 LOD Message Address Payload Control

0.6	31:0	<p><b>Slot6 LOD</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Project:</td><td style="padding: 2px;">All</td></tr> <tr> <td style="padding: 2px;">Format:</td><td style="padding: 2px;"><b>MACD_LOD</b></td></tr> </table> <p>Specifies the LOD for slot 6</p>	Project:	All	Format:	<b>MACD_LOD</b>
Project:	All					
Format:	<b>MACD_LOD</b>					
0.7	31:0	<p><b>Slot7 LOD</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Project:</td><td style="padding: 2px;">All</td></tr> <tr> <td style="padding: 2px;">Format:</td><td style="padding: 2px;"><b>MACD_LOD</b></td></tr> </table> <p>Specifies the LOD for slot 7</p>	Project:	All	Format:	<b>MACD_LOD</b>
Project:	All					
Format:	<b>MACD_LOD</b>					

## SIMD8 Render Target Data Payload

<b>MDP_RTW_8 - SIMD8 Render Target Data Payload</b>						
<b>DWord</b>	<b>Bit</b>	<b>Description</b>				
0.0-0.7	255:0	<p><b>Red</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW_SIMD8</b></td></tr> </table> <p>Slots [7:0] Red</p>	Project:	All	Format:	<b>MDP_DW_SIMD8</b>
Project:	All					
Format:	<b>MDP_DW_SIMD8</b>					
1.0-1.7	255:0	<p><b>Green</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW_SIMD8</b></td></tr> </table> <p>Slots [7:0] Green</p>	Project:	All	Format:	<b>MDP_DW_SIMD8</b>
Project:	All					
Format:	<b>MDP_DW_SIMD8</b>					
2.0-2.7	255:0	<p><b>Blue</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW_SIMD8</b></td></tr> </table> <p>Slots [7:0] Blue</p>	Project:	All	Format:	<b>MDP_DW_SIMD8</b>
Project:	All					
Format:	<b>MDP_DW_SIMD8</b>					
3.0-3.7	255:0	<p><b>Alpha</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW_SIMD8</b></td></tr> </table> <p>Slots [7:0] Alpha</p>	Project:	All	Format:	<b>MDP_DW_SIMD8</b>
Project:	All					
Format:	<b>MDP_DW_SIMD8</b>					

## SIMD8 Typed Surface 32-Bit Address Payload

### MAP32B\_TS SIMD8 - SIMD8 Typed Surface 32-Bit Address Payload

Project:	BDW					
Size (in bits):	1024					
Default Value:	0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000					
DWord	Bit	Description				
0.0-0.7	255:0	<p><b>U</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MACR_32b</b></td></tr> </table> <p>Specifies the U channel for slots [7:0]</p>	Project:	All	Format:	<b>MACR_32b</b>
Project:	All					
Format:	<b>MACR_32b</b>					
1.0-1.7	255:0	<p><b>V</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MACR_32b</b></td></tr> </table> <p>Specifies the V channel for slots [7:0]</p>	Project:	All	Format:	<b>MACR_32b</b>
Project:	All					
Format:	<b>MACR_32b</b>					
2.0-2.7	255:0	<p><b>R</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MACR_32b</b></td></tr> </table> <p>Specifies the R channel for slots [7:0]</p>	Project:	All	Format:	<b>MACR_32b</b>
Project:	All					
Format:	<b>MACR_32b</b>					
3.0-3.7	255:0	<p><b>LOD</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MACR_LOD SIMD8</b></td></tr> </table> <p>Specifies the LOD for slots [7:0]</p>	Project:	All	Format:	<b>MACR_LOD SIMD8</b>
Project:	All					
Format:	<b>MACR_LOD SIMD8</b>					

## SIMD8 Untyped BUFFER Surface 32-Bit Address Payload

### MAP32B\_USU SIMD8 - SIMD8 Untyped BUFFER Surface 32-Bit Address Payload

Project:	All					
Size (in bits):	256					
Default Value:	0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000					
DWord	Bit	Description				
0.0-0.7	255:0	<p><b>U</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MACR_32b</b></td></tr> </table> <p>Specifies the U channel for slots [7:0]</p>	Project:	All	Format:	<b>MACR_32b</b>
Project:	All					
Format:	<b>MACR_32b</b>					

## SIMD8 Untyped BUFFER Surface 64-Bit Address Payload

### MAP64B\_USU SIMD8 - SIMD8 Untyped BUFFER Surface 64-Bit Address Payload

Project:	All					
Size (in bits):	512					
Default Value:	0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000					
DWord	Bit	Description				
0.0-0.7	255:0	<p><b>U3_U0</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MACR_64b</b></td></tr> </table> <p>Specifies the U channel for slots [3:0]</p>	Project:	All	Format:	<b>MACR_64b</b>
Project:	All					
Format:	<b>MACR_64b</b>					
1.0-1.7	255:0	<p><b>U7_U4</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MACR_64b</b></td></tr> </table> <p>Specifies the U channel for slots [7:4]</p>	Project:	All	Format:	<b>MACR_64b</b>
Project:	All					
Format:	<b>MACR_64b</b>					

## SIMD8 Untyped STRBUF Surface 32-Bit Address Payload

<b>MAP32B_USUV SIMD8 - SIMD8 Untyped STRBUF Surface 32-Bit Address Payload</b>						
<b>DWord</b>	<b>Bit</b>	<b>Description</b>				
0.0-0.7	255:0	<p><b>U</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MACR_32b</b></td></tr> </table> <p>Specifies the U channel for slots [7:0]</p>	Project:	All	Format:	<b>MACR_32b</b>
Project:	All					
Format:	<b>MACR_32b</b>					
1.0-1.7	255:0	<p><b>V</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MACR_32b</b></td></tr> </table> <p>Specifies the V channel for slots [7:0]</p>	Project:	All	Format:	<b>MACR_32b</b>
Project:	All					
Format:	<b>MACR_32b</b>					

## SIMD16 Render Target Data Payload

MDP_RTW_16 - SIMD16 Render Target Data Payload						
DWord	Bit	Description				
0.0-0.7	255:0	<p><b>Red[7:0]</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW_SIMD8</b></td></tr> </table> <p>Slots [7:0] Red</p>	Project:	All	Format:	<b>MDP_DW_SIMD8</b>
Project:	All					
Format:	<b>MDP_DW_SIMD8</b>					
1.0-1.7	255:0	<p><b>Red[15:8]</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW_SIMD8</b></td></tr> </table> <p>Slots [15:8] Red</p>	Project:	All	Format:	<b>MDP_DW_SIMD8</b>
Project:	All					
Format:	<b>MDP_DW_SIMD8</b>					
2.0-2.7	255:0	<p><b>Green[7:0]</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW_SIMD8</b></td></tr> </table> <p>Slots [7:0] Green</p>	Project:	All	Format:	<b>MDP_DW_SIMD8</b>
Project:	All					
Format:	<b>MDP_DW_SIMD8</b>					
3.0-3.7	255:0	<p><b>Green[15:8]</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW_SIMD8</b></td></tr> </table> <p>Slots [15:8] Green</p>	Project:	All	Format:	<b>MDP_DW_SIMD8</b>
Project:	All					
Format:	<b>MDP_DW_SIMD8</b>					
4.0-4.7	255:0	<p><b>Blue[7:0]</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW_SIMD8</b></td></tr> </table> <p>Slots [7:0] Blue</p>	Project:	All	Format:	<b>MDP_DW_SIMD8</b>
Project:	All					
Format:	<b>MDP_DW_SIMD8</b>					

## MDP\_RTW\_16 - SIMD16 Render Target Data Payload

5.0-5.7	255:0	<b>Blue[15:8]</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Project:</td><td style="padding: 2px;">All</td></tr> <tr> <td style="padding: 2px;">Format:</td><td style="padding: 2px;"><b>MDP_DW SIMD8</b></td></tr> </table> <p style="margin-top: 5px;">Slots [15:8] Blue</p>	Project:	All	Format:	<b>MDP_DW SIMD8</b>
Project:	All					
Format:	<b>MDP_DW SIMD8</b>					
6.0-6.7	255:0	<b>Alpha[7:0]</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Project:</td><td style="padding: 2px;">All</td></tr> <tr> <td style="padding: 2px;">Format:</td><td style="padding: 2px;"><b>MDP_DW SIMD8</b></td></tr> </table> <p style="margin-top: 5px;">Slots [7:0] Alpha</p>	Project:	All	Format:	<b>MDP_DW SIMD8</b>
Project:	All					
Format:	<b>MDP_DW SIMD8</b>					
7.0-7.7	255:0	<b>Alpha[15:7]</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Project:</td><td style="padding: 2px;">All</td></tr> <tr> <td style="padding: 2px;">Format:</td><td style="padding: 2px;"><b>MDP_DW SIMD8</b></td></tr> </table> <p style="margin-top: 5px;">Slots [15:7] Alpha</p>	Project:	All	Format:	<b>MDP_DW SIMD8</b>
Project:	All					
Format:	<b>MDP_DW SIMD8</b>					

## SIMD16 Untyped BUFFER Surface 32-Bit Address Payload

<b>MAP32B_USU SIMD16 - SIMD16 Untyped BUFFER Surface 32-Bit Address Payload</b>						
<b>DWord</b>	<b>Bit</b>	<b>Description</b>				
0.0-0.7	255:0	<p><b>U[7:0]</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MACR_32b</b></td></tr> </table> <p>Specifies the U channel for slots [7:0]</p>	Project:	All	Format:	<b>MACR_32b</b>
Project:	All					
Format:	<b>MACR_32b</b>					
1.0-1.7	255:0	<p><b>U[15:8]</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MACR_32b</b></td></tr> </table> <p>Specifies the U channel for slots [15:8]</p>	Project:	All	Format:	<b>MACR_32b</b>
Project:	All					
Format:	<b>MACR_32b</b>					

## SIMD16 Untyped BUFFER Surface 64-Bit Address Payload

<b>MAP64B_USU SIMD16 - SIMD16 Untyped BUFFER Surface 64-Bit Address Payload</b>						
<b>DWord</b>	<b>Bit</b>	<b>Description</b>				
0.0-0.7	255:0	<p><b>U3_U0</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td><b>MACR_64b</b></td> </tr> </table> <p>Specifies the U channel for slots [3:0]</p>	Project:	All	Format:	<b>MACR_64b</b>
Project:	All					
Format:	<b>MACR_64b</b>					
1.0-1.7	255:0	<p><b>U7_U4</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td><b>MACR_64b</b></td> </tr> </table> <p>Specifies the U channel for slots [7:4]</p>	Project:	All	Format:	<b>MACR_64b</b>
Project:	All					
Format:	<b>MACR_64b</b>					
2.0-2.7	255:0	<p><b>U11_U8</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td><b>MACR_64b</b></td> </tr> </table> <p>Specifies the U channel for slots [11:8]</p>	Project:	All	Format:	<b>MACR_64b</b>
Project:	All					
Format:	<b>MACR_64b</b>					
3.0-3.7	255:0	<p><b>U15_U12</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td><b>MACR_64b</b></td> </tr> </table> <p>Specifies the U channel for slots [15:12]</p>	Project:	All	Format:	<b>MACR_64b</b>
Project:	All					
Format:	<b>MACR_64b</b>					

## SIMD16 Untyped STRBUF Surface 32-Bit Address Payload

<b>MAP32B_USUV SIMD16 - SIMD16 Untyped STRBUF Surface 32-Bit Address Payload</b>						
<b>DWord</b>	<b>Bit</b>	<b>Description</b>				
0.0-0.7	255:0	<p><b>U7_U0</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td><b>MACR_32b</b></td> </tr> </table> <p>Specifies the U channel for slots [7:0]</p>	Project:	All	Format:	<b>MACR_32b</b>
Project:	All					
Format:	<b>MACR_32b</b>					
1.0-1.7	255:0	<p><b>U15_U8</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td><b>MACR_32b</b></td> </tr> </table> <p>Specifies the U channel for slots [15:8]</p>	Project:	All	Format:	<b>MACR_32b</b>
Project:	All					
Format:	<b>MACR_32b</b>					
2.0-2.7	255:0	<p><b>V7_V0</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td><b>MACR_32b</b></td> </tr> </table> <p>Specifies the V channel for slots [7:0]</p>	Project:	All	Format:	<b>MACR_32b</b>
Project:	All					
Format:	<b>MACR_32b</b>					
3.0-3.7	255:0	<p><b>V15_V8</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td><b>MACR_32b</b></td> </tr> </table> <p>Specifies the V channel for slots [15:8]</p>	Project:	All	Format:	<b>MACR_32b</b>
Project:	All					
Format:	<b>MACR_32b</b>					

## SIMD 32-Bit Address Payload Control

<b>MACR_32B - SIMD 32-Bit Address Payload Control</b>						
<b>DWord</b>	<b>Bit</b>	<b>Description</b>				
0.0	31:0	<b>Offset0</b> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U32</td> </tr> </table> <p>Specifies the address offset for slot 0 in this payload register.</p>	Project:	All	Format:	U32
Project:	All					
Format:	U32					
0.1	31:0	<b>Offset1</b> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U32</td> </tr> </table> <p>Specifies the address offset for slot 1 in this payload register.</p>	Project:	All	Format:	U32
Project:	All					
Format:	U32					
0.2	31:0	<b>Offset2</b> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U32</td> </tr> </table> <p>Specifies the address offset for slot 2 in this payload register.</p>	Project:	All	Format:	U32
Project:	All					
Format:	U32					
0.3	31:0	<b>Offset3</b> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U32</td> </tr> </table> <p>Specifies the address offset for slot 3 in this payload register.</p>	Project:	All	Format:	U32
Project:	All					
Format:	U32					
0.4	31:0	<b>Offset4</b> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U32</td> </tr> </table> <p>Specifies the address offset for slot 4 in this payload register.</p>	Project:	All	Format:	U32
Project:	All					
Format:	U32					
0.5	31:0	<b>Offset5</b> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U32</td> </tr> </table> <p>Specifies the address offset for slot 5 in this payload register.</p>	Project:	All	Format:	U32
Project:	All					
Format:	U32					

## **MACR\_32B - SIMD 32-Bit Address Payload Control**

0.6	31:0	<p><b>Offset6</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Project:</td><td style="padding: 2px;">All</td></tr> <tr> <td style="padding: 2px;">Format:</td><td style="padding: 2px;">U32</td></tr> </table> <p>Specifies the address offset for slot 6 in this payload register.</p>	Project:	All	Format:	U32
Project:	All					
Format:	U32					
0.7	31:0	<p><b>Offset7</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Project:</td><td style="padding: 2px;">All</td></tr> <tr> <td style="padding: 2px;">Format:</td><td style="padding: 2px;">U32</td></tr> </table> <p>Specifies the address offset for slot 7 in this payload register.</p>	Project:	All	Format:	U32
Project:	All					
Format:	U32					

## SIMD 64-Bit Address Payload Control

<b>MACR_64B - SIMD 64-Bit Address Payload Control</b>						
<b>DWord</b>	<b>Bit</b>	<b>Description</b>				
0.0-0.1	63:0	<b>Offset0</b> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U64</td> </tr> </table> <p>Specifies the address offset for slot 0 in this payload register.</p>	Project:	All	Format:	U64
Project:	All					
Format:	U64					
0.2-0.3	63:0	<b>Offset1</b> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U64</td> </tr> </table> <p>Specifies the address offset for slot 1 in this payload register.</p>	Project:	All	Format:	U64
Project:	All					
Format:	U64					
0.4-0.5	63:0	<b>Offset2</b> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U64</td> </tr> </table> <p>Specifies the address offset for slot 2 in this payload register.</p>	Project:	All	Format:	U64
Project:	All					
Format:	U64					
0.6-0.7	63:0	<b>Offset3</b> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U64</td> </tr> </table> <p>Specifies the address offset for slot 3 in this payload register.</p>	Project:	All	Format:	U64
Project:	All					
Format:	U64					

## SIMD8 32-Bit Address Payload

MAP32B SIMD8 - SIMD8 32-Bit Address Payload						
DWord	Bit	Description				
0.0-0.7	255:0	<p><b>Offset[7:0]</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MACR_32b</b></td></tr> </table> <p>Specifies the address offset for Slots [7:0].</p>	Project:	All	Format:	<b>MACR_32b</b>
Project:	All					
Format:	<b>MACR_32b</b>					

## SIMD8 64-Bit Address Payload

<b>MAP64B SIMD8 - SIMD8 64-Bit Address Payload</b>						
<b>DWord</b>	<b>Bit</b>	<b>Description</b>				
0.0-0.7	255:0	<p><b>Offset[3:0]</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MACR_64b</b></td></tr> </table> <p>Specifies the address offset for slots [3:0].</p>	Project:	All	Format:	<b>MACR_64b</b>
Project:	All					
Format:	<b>MACR_64b</b>					
1.0-1.7	255:0	<p><b>Offset[7:4]</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MACR_64b</b></td></tr> </table> <p>Specifies the address offset for slots [7:4].</p>	Project:	All	Format:	<b>MACR_64b</b>
Project:	All					
Format:	<b>MACR_64b</b>					

## SIMD16 32-Bit Address Payload

MAP32B SIMD16 - SIMD16 32-Bit Address Payload						
DWord	Bit	Description				
0.0-0.7	255:0	<b>Offset[7:0]</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MACR_32b</b></td></tr> </table> <p>Specifies the address offset for slots [7:0].</p>	Project:	All	Format:	<b>MACR_32b</b>
Project:	All					
Format:	<b>MACR_32b</b>					
1.0-1.7	255:0	<b>Offset[15:8]</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MACR_32b</b></td></tr> </table> <p>Specifies the address offset for slots [15:8].</p>	Project:	All	Format:	<b>MACR_32b</b>
Project:	All					
Format:	<b>MACR_32b</b>					

## SIMD16 64-Bit Address Payload

<b>MAP64B SIMD16 - SIMD16 64-Bit Address Payload</b>						
<b>DWord</b>	<b>Bit</b>	<b>Description</b>				
0.0-0.7	255:0	<p><b>Offset[3:0]</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MACR_64b</b></td></tr> </table> <p>Specifies the address offsets for slots [3:0].</p>	Project:	All	Format:	<b>MACR_64b</b>
Project:	All					
Format:	<b>MACR_64b</b>					
1.0-1.7	255:0	<p><b>Offset[7:4]</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MACR_64b</b></td></tr> </table> <p>Specifies the address offsets for slots [7:4].</p>	Project:	All	Format:	<b>MACR_64b</b>
Project:	All					
Format:	<b>MACR_64b</b>					
2.0-2.7	255:0	<p><b>Offset[11:8]</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MACR_64b</b></td></tr> </table> <p>Specifies the address offsets for slots [11:8].</p>	Project:	All	Format:	<b>MACR_64b</b>
Project:	All					
Format:	<b>MACR_64b</b>					
3.0-3.7	255:0	<p><b>Offset[15:12]</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MACR_64b</b></td></tr> </table> <p>Specifies the address offsets for slots [15:12].</p>	Project:	All	Format:	<b>MACR_64b</b>
Project:	All					
Format:	<b>MACR_64b</b>					

## SIMD Mode 2 Message Descriptor Control Field

MDC_SM2 - SIMD Mode 2 Message Descriptor Control Field															
DWord	Bit	Description													
0	0	<p><b>SIMD Mode</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Enumeration</td> </tr> </table> <p>Specifies the SIMD mode of the message (number of slots processed)</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00h</td> <td>SIMD8</td> <td>SIMD8</td> </tr> <tr> <td>01h</td> <td>SIMD16</td> <td>SIMD16</td> </tr> </tbody> </table>	Project:	All	Format:	Enumeration	Value	Name	Description	00h	SIMD8	SIMD8	01h	SIMD16	SIMD16
Project:	All														
Format:	Enumeration														
Value	Name	Description													
00h	SIMD8	SIMD8													
01h	SIMD16	SIMD16													

## SIMD Mode 3 Message Descriptor Control Field

MDC_SM3 - SIMD Mode 3 Message Descriptor Control Field																			
DWord	Bit	Description																	
0	1:0	<p><b>SIMD Mode</b></p> <table border="1"> <tr> <td>Format:</td> <td>Enumeration</td> </tr> </table> <p>Specifies the SIMD mode of the message (number of slots processed)</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00h</td> <td>SIMD4x2</td> <td>SIMD4x2</td> </tr> <tr> <td>01h</td> <td>SIMD16</td> <td>SIMD16</td> </tr> <tr> <td>02h</td> <td>SIMD8</td> <td>SIMD8</td> </tr> <tr> <td>03h</td> <td>Reserved</td> <td>Ignored</td> </tr> </tbody> </table>	Format:	Enumeration	Value	Name	Description	00h	SIMD4x2	SIMD4x2	01h	SIMD16	SIMD16	02h	SIMD8	SIMD8	03h	Reserved	Ignored
Format:	Enumeration																		
Value	Name	Description																	
00h	SIMD4x2	SIMD4x2																	
01h	SIMD16	SIMD16																	
02h	SIMD8	SIMD8																	
03h	Reserved	Ignored																	

## SLM Surface Pixel Mask Message Header

<b>MH1_SLM_PSM - SLM Surface Pixel Mask Message Header</b>						
<b>DWord</b>	<b>Bit</b>	<b>Description</b>				
0-6	223:0	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>Ignore</td> </tr> <tr> <td colspan="2">Ignored</td> </tr> </table>	Format:	Ignore	Ignored	
Format:	Ignore					
Ignored						
7	31:0	<p><b>Pixel Sample Mask</b></p> <table border="1"> <tr> <td>Format:</td> <td><b>MHC_PSM</b></td> </tr> <tr> <td colspan="2">Specifies the 16-bit Pixel/Sample Mask used with SIMD16 and SIMD8 surfaces.</td> </tr> </table>	Format:	<b>MHC_PSM</b>	Specifies the 16-bit Pixel/Sample Mask used with SIMD16 and SIMD8 surfaces.	
Format:	<b>MHC_PSM</b>					
Specifies the 16-bit Pixel/Sample Mask used with SIMD16 and SIMD8 surfaces.						

## Slot Group 2 Message Descriptor Control Field

MDC_SG2 - Slot Group 2 Message Descriptor Control Field															
DWord	Bit	Description													
0	0	<p><b>SIMD Mode</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Enumeration</td> </tr> </table> <p>Controls which 8 bits of Pixel/Sample Mask in the message header are ANDed with the execution mask to determine which slots are accessed. This field is ignored if the header is not present.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00h</td> <td>SG8L</td> <td>Use low 8 slots</td> </tr> <tr> <td>01h</td> <td>SG8U</td> <td>Use high 8 slots</td> </tr> </tbody> </table>	Project:	All	Format:	Enumeration	Value	Name	Description	00h	SG8L	Use low 8 slots	01h	SG8U	Use high 8 slots
Project:	All														
Format:	Enumeration														
Value	Name	Description													
00h	SG8L	Use low 8 slots													
01h	SG8U	Use high 8 slots													

## Slot Group 3 Message Descriptor Control Field

MDC_SG3 - Slot Group 3 Message Descriptor Control Field																			
DWord	Bit	Description																	
0	1:0	<p><b>SIMD Mode</b></p> <table border="1"> <tr> <td>Format:</td> <td>Enumeration</td> </tr> </table> <p>Controls which 8 bits of Pixel/Sample Mask in the message header are ANDed with the execution mask to determine which slots are accessed. This field is ignored if the header is not present.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00h</td> <td>SG4x2</td> <td>SIMD4x2</td> </tr> <tr> <td>01h</td> <td>SG8L</td> <td>Use low 8 slots</td> </tr> <tr> <td>02h</td> <td>SG8U</td> <td>Use high 8 slots</td> </tr> <tr> <td>03h</td> <td>Reserved</td> <td>Ignored</td> </tr> </tbody> </table>	Format:	Enumeration	Value	Name	Description	00h	SG4x2	SIMD4x2	01h	SG8L	Use low 8 slots	02h	SG8U	Use high 8 slots	03h	Reserved	Ignored
Format:	Enumeration																		
Value	Name	Description																	
00h	SG4x2	SIMD4x2																	
01h	SG8L	Use low 8 slots																	
02h	SG8U	Use high 8 slots																	
03h	Reserved	Ignored																	

## Slot Group Select Render Cache Message Descriptor Control Field

MDC_RT_SGS - Slot Group Select Render Cache Message Descriptor Control Field															
DWord	Bit	Description													
0	0	<p><b>Slot Group Select</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td colspan="2">This field selects whether slots 15:0 or slots 31:16 are used for bypassed data. Bypassed data includes the antialias alpha, multisample coverage mask, and if the header is not present also includes the X/Y addresses and pixel enables. For 8- and 16-pixel dispatches, SLOTGRP_LO must be selected on every message. For 32-pixel dispatches, this field must be set correctly for each message based on which slots are currently being processed.</td> </tr> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> <tr> <td>00h</td><td>SLOTGRP_LO</td><td>Choose bypassed data for slots 15:0</td></tr> <tr> <td>01h</td><td>SLOTGRP_HI</td><td>Choose bypassed data for slots 31:16</td></tr> </table>	Project:	All	This field selects whether slots 15:0 or slots 31:16 are used for bypassed data. Bypassed data includes the antialias alpha, multisample coverage mask, and if the header is not present also includes the X/Y addresses and pixel enables. For 8- and 16-pixel dispatches, SLOTGRP_LO must be selected on every message. For 32-pixel dispatches, this field must be set correctly for each message based on which slots are currently being processed.		Value	Name	Description	00h	SLOTGRP_LO	Choose bypassed data for slots 15:0	01h	SLOTGRP_HI	Choose bypassed data for slots 31:16
Project:	All														
This field selects whether slots 15:0 or slots 31:16 are used for bypassed data. Bypassed data includes the antialias alpha, multisample coverage mask, and if the header is not present also includes the X/Y addresses and pixel enables. For 8- and 16-pixel dispatches, SLOTGRP_LO must be selected on every message. For 32-pixel dispatches, this field must be set correctly for each message based on which slots are currently being processed.															
Value	Name	Description													
00h	SLOTGRP_LO	Choose bypassed data for slots 15:0													
01h	SLOTGRP_HI	Choose bypassed data for slots 31:16													

## SO\_DECL

SO_DECL											
DWord	Bit	Description									
0	15:14	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	All	Format:	MBZ					
Project:	All										
Format:	MBZ										
	13:12	<p><b>Output Buffer Slot</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U2 Buffer Index</td> </tr> </table> <p>This field selects the destination output buffer slot.</p>	Project:	All	Format:	U2 Buffer Index					
Project:	All										
Format:	U2 Buffer Index										
	11	<p><b>Hole Flag</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Flag</td> </tr> </table> <p>If set, the Component Mask field indirectly specifies a number of 32-bit locations to skip over (leave unmodified in memory) in the selected output buffer. The Register Index field is ignored. The only permitted Component Mask values are as follows:</p> <table border="1"> <tr> <td>0x0 No Dwords are skipped over (SO_DECL performs no operation)</td> </tr> <tr> <td>0x1 (X) Skip 1 DWord</td> </tr> <tr> <td>0x3 (XY) Skip 2 DWords</td> </tr> <tr> <td>0x7 (XYZ) Skip 3 DWords</td> </tr> <tr> <td>0xF (XYZW) Skip 4 DWords</td> </tr> </table>	Project:	All	Format:	Flag	0x0 No Dwords are skipped over (SO_DECL performs no operation)	0x1 (X) Skip 1 DWord	0x3 (XY) Skip 2 DWords	0x7 (XYZ) Skip 3 DWords	0xF (XYZW) Skip 4 DWords
Project:	All										
Format:	Flag										
0x0 No Dwords are skipped over (SO_DECL performs no operation)											
0x1 (X) Skip 1 DWord											
0x3 (XY) Skip 2 DWords											
0x7 (XYZ) Skip 3 DWords											
0xF (XYZW) Skip 4 DWords											
	10	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	All	Format:	MBZ					
Project:	All										
Format:	MBZ										

## SO\_DECL

9:4	<b>Register Index</b>												
	Project:	All											
	Format:	U6 128-bit granular offset into the source vertex read data											
	<p>If Hole Flag is clear, this field specifies the 128-bit offset into the source vertex data which supplies the source data to be written to the destination buffer, where the individual 32-component destination locations are selected by Component Mask. e.g., Register Index 0 corresponds with the first 128 bits of the data read from the vertex URB entry (as per corresponding Vertex Read Offset state)</p> <p>There is only enough internal storage for the 128-bit vertex header and 32 128-bit vertex attributes.</p>												
	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="background-color: #e0e0ff; text-align: center;">Value</th><th style="background-color: #e0e0ff; text-align: center;">Name</th></tr> </thead> <tbody> <tr> <td>[0,32]</td><td></td></tr> <tr> <td>0h</td><td><b>[Default]</b></td></tr> </tbody> </table>		Value	Name	[0,32]		0h	<b>[Default]</b>					
Value	Name												
[0,32]													
0h	<b>[Default]</b>												
<b>Programming Notes</b>													
<p>It is the responsibility of software to map any API-visible source data specifications (e.g., vertex register number) into 128-bit granular URB read offsets.</p>													
<b>Component Mask</b>													
Project:	All												
Format:	MASK 4-bit Mask												
<p>This field is a 4-bit bitmask that selects which contiguous 32-bit component(s) are either written or skipped-over in the destination buffer. If this field is zero the SO_DECL operation is effectively a no-op. No data will be appended to the destination and the destination buffer's write pointer will not be advanced. If the <b>Hole Flag</b> is set, this field (if non-zero) indirectly specifies how much the destination buffer's write pointer should be advanced. See <b>Hole Flag</b> description above for restrictions on this field. If the <b>Hole Flag</b> is clear, this field (if non-zero) selects which source components are to be written to the destination buffer. The components must be contiguous, e.g. YZW is legal, but XZW is not. The selected source components are written to the destination buffer starting at the current write pointer, and then the write pointer is advanced past the written data. E.g., if YZW is specified, the three (YZW) components of the source register will be written to the destination buffer at the current write pointer, and the write pointer will be advanced by 3 DWords.</p>													
<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="background-color: #e0e0ff; text-align: center;">Value</th><th style="background-color: #e0e0ff; text-align: center;">Name</th></tr> </thead> <tbody> <tr> <td>0h</td><td><b>[Default]</b></td></tr> <tr> <td>xxx1b</td><td>SO_DECL_COMPMASK_X</td></tr> <tr> <td>xx1xb</td><td>SO_DECL_COMPMASK_Y</td></tr> <tr> <td>x1xxb</td><td>SO_DECL_COMPMASK_Z</td></tr> <tr> <td>1xxxb</td><td>SO_DECL_COMPMASK_W</td></tr> </tbody> </table>		Value	Name	0h	<b>[Default]</b>	xxx1b	SO_DECL_COMPMASK_X	xx1xb	SO_DECL_COMPMASK_Y	x1xxb	SO_DECL_COMPMASK_Z	1xxxb	SO_DECL_COMPMASK_W
Value	Name												
0h	<b>[Default]</b>												
xxx1b	SO_DECL_COMPMASK_X												
xx1xb	SO_DECL_COMPMASK_Y												
x1xxb	SO_DECL_COMPMASK_Z												
1xxxb	SO_DECL_COMPMASK_W												

## SO\_DECL\_ENTRY

SO_DECL_ENTRY				
DWord	Bit	Description		
0..1	63:48	<p><b>Stream 3 Decl</b></p> <table border="1"> <tr> <td>Format:</td> <td><b>SO_DECL</b></td> </tr> </table> <p>This field contains Stream 3 SO_DECL [n]</p>	Format:	<b>SO_DECL</b>
Format:	<b>SO_DECL</b>			
47:32	<p><b>Stream 2 Decl</b></p> <table border="1"> <tr> <td>Format:</td> <td><b>SO_DECL</b></td> </tr> </table> <p>This field contains Stream 2 SO_DECL [n]</p>	Format:	<b>SO_DECL</b>	
Format:	<b>SO_DECL</b>			
31:16	<p><b>Stream 1 Decl</b></p> <table border="1"> <tr> <td>Format:</td> <td><b>SO_DECL</b></td> </tr> </table> <p>This field contains Stream 1 SO_DECL [n]</p>	Format:	<b>SO_DECL</b>	
Format:	<b>SO_DECL</b>			
15:0	<p><b>Stream 0 Decl</b></p> <table border="1"> <tr> <td>Format:</td> <td><b>SO_DECL</b></td> </tr> </table> <p>This field contains Stream 0 SO_DECL [n]</p>	Format:	<b>SO_DECL</b>	
Format:	<b>SO_DECL</b>			

## SplitBaseAddress4KByteAligned

SplitBaseAddress4KByteAligned						
DWord	Bit	Description				
0 <b>Project:</b> All	31:12	<b>Base Address Low</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>GraphicsAddress[31:12]</td></tr> </table>	Project:	All	Format:	GraphicsAddress[31:12]
Project:	All					
Format:	GraphicsAddress[31:12]					
11:0	<b>Reserved</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	All	Format:	MBZ	
Project:	All					
Format:	MBZ					

## SplitBaseAddress64ByteAligned

SplitBaseAddress64ByteAligned				
DWord	Bit	Description		
0 <b>Project:</b> All	31:6	<b>Base Address Low</b>		
		<table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>GraphicsAddress[31:6]</td></tr> </table>	Project:	All
Project:	All			
Format:	GraphicsAddress[31:6]			
	5:0	<b>Reserved</b>		
		<table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	All
Project:	All			
Format:	MBZ			

## SrcRegNum

SrcRegNum											
<b>Description</b> Register Number The register number for the operand. For a GRF register, is the part of a register address that aligns to a 256-bit (32-byte) boundary. For an ARF register, this field is encoded such that MSBs identify the architecture register type and LSBs provide the register number. An ARF register can only be dst or src0. Any src1 or src2 operands cannot be ARF registers. RegNum and SubRegNum together provide the byte-aligned address for the origin of a register region. RegNum provides bits 12:5 of that address. For one-source and two-source instructions, SubregNum provides bits 4:0. For three-source instructions, the address must be DWord-aligned; SubRegNum provides bits 4:2 of the address and bits 1:0 are zero. This field is present for the direct addressing mode and not present for indirect addressing. This field applies to both source and destination operands.											
DWord	Bit	Description									
0	7:0	<b>Source Register Number</b> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0-127</td> <td>If {Dst/Src0/Src1/Src2}.RegFile==GRF</td> <td></td> </tr> <tr> <td>0-0ffh</td> <td>If {Dst/Src0/Src1/Src2}.RegFile==ARF</td> <td>This field is used to encode the architecture register as well as providing the register number. See GEN Execution Environment chapter for details.</td> </tr> </tbody> </table>	Value	Name	Description	0-127	If {Dst/Src0/Src1/Src2}.RegFile==GRF		0-0ffh	If {Dst/Src0/Src1/Src2}.RegFile==ARF	This field is used to encode the architecture register as well as providing the register number. See GEN Execution Environment chapter for details.
Value	Name	Description									
0-127	If {Dst/Src0/Src1/Src2}.RegFile==GRF										
0-0ffh	If {Dst/Src0/Src1/Src2}.RegFile==ARF	This field is used to encode the architecture register as well as providing the register number. See GEN Execution Environment chapter for details.									

## SrcSubRegNum

<b>SrcSubRegNum</b>			
Project:	BDW		
Source:	Eulsa		
Size (in bits):	5		
Default Value:	0x00000000		
<b>Description</b>			
Subregister Number The subregister number for the operand. For a GRF register, is the byte address within a 256-bit (32-byte) register. For an ARF register, determines the sub-register number according to the specified encoding for the given architecture register. RegNum and SubRegNum together provide the byte-aligned address for the origin of a GRF register region. RegNum provides bits 12:5 of that address. For one-source and two-source instructions, SubregNum provides bits 4:0. For three-source instructions, the address must be DWord-aligned; SubRegNum provides bits 4:2 of the address and bits 1:0 are zero.			
<b>Programming Notes</b>			
Note: The recommended instruction syntax uses subregister numbers within the GRF in units of actual data element size, corresponding to the data type used. For example for the F (Float) type, the assembler syntax uses subregister numbers 0 to 7, corresponding to subregister byte addresses of 0 to 28 in steps of 4, the element size.			
DWord	Bit	<b>Description</b>	
0	4:0	<b>Source Sub Register Number</b>	
Value	Name	<b>Description</b>	
0-31	If {Dst/Src0/Src1/Src2}.RegFile==GRF		
0-0ffh	If {Dst/Src0/Src1/Src2}.RegFile==ARF	This field is used to encode the architecture register as well as providing the register number. See GEN Execution Environment chapter for details.	

## SRD Interrupt Bit Definition

SRD Interrupt Bit Definition		
DWord	Bit	Description
0	31:30	<b>Reserved</b>
	29:27	<b>Reserved</b>
		Project: BDW
	26	<b>Reserved</b>
		Project: BDW
	25	<b>SRD_Exit_C</b>
		This event occurs on the first blank start after SRD exit on transcoder C.
	24	<b>SRD_PreWarn_C</b>
		This event occurs two display frames prior to entering SRD on transcoder C.
	23:19	<b>Reserved</b>
	18	<b>Reserved</b>
		Project: BDW
	17	<b>SRD_Exit_B</b>
		This event occurs on the first blank start after SRD exit on transcoder B.
	16	<b>SRD_PreWarn_B</b>
		This event occurs two display frames prior to entering SRD on transcoder B.
	15:11	<b>Reserved</b>
	10	<b>Reserved</b>
		Project: BDW
	9	<b>SRD_Exit_A</b>
		This event occurs on the first blank start after SRD exit on transcoder A.
	8	<b>SRD_PreWarn_A</b>
		This event occurs two display frames prior to entering SRD on transcoder A.
	7:3	<b>Reserved</b>
	2	<b>SRD_Aux_Error_EDP</b>
		This event occurs on the rising edge of the SRD Aux error (receive error or timeout) indication.
	1	<b>SRD_Exit_EDP</b>
		This event occurs on the first blank start after SRD exit on transcoder EDP.

## SRD Interrupt Bit Definition

	0	<b>SRD_PreWarn_EDP</b> This event occurs two display frames prior to entering SRD on transcoder EDP.					
		<table border="1"> <thead> <tr> <th>Workaround</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>The pre-warn interrupt event happens continuously during the entire frame before the capture frame. To prevent constant interrupts, mask this interrupt off after it is first received and don't unmask it until after the entire frame is known to be completed.</td> <td>BDW, EXCLUDE(BDW:GT2:G)</td> </tr> </tbody> </table>	Workaround	Project	The pre-warn interrupt event happens continuously during the entire frame before the capture frame. To prevent constant interrupts, mask this interrupt off after it is first received and don't unmask it until after the entire frame is known to be completed.	BDW, EXCLUDE(BDW:GT2:G)	
Workaround	Project						
The pre-warn interrupt event happens continuously during the entire frame before the capture frame. To prevent constant interrupts, mask this interrupt off after it is first received and don't unmask it until after the entire frame is known to be completed.	BDW, EXCLUDE(BDW:GT2:G)						

## Stateless Binding Table Index Message Descriptor Control Field

MDC_STATELESS - Stateless Binding Table Index Message Descriptor Control Field																		
DWord	Bit	Description																
0	7:0	<p><b>Binding Table Index</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Enumeration</td> </tr> </table> <p>Specifies the message is Stateless</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0FFh</td> <td>A32_A64 <b>[Default]</b></td> <td>Specifies a A32 or A64 Stateless access that is locally coherent (coherent within a thread group)</td> </tr> <tr> <td>0FDh</td> <td>A32_A64_NC</td> <td>Specifies a A32 or A64 Stateless access that is non-coherent (coherent within a thread).</td> </tr> <tr> <td>Others</td> <td>Reserved</td> <td>Ignored</td> </tr> </tbody> </table> <p><b>Restriction</b></p> <p>When using A32_A64_NC, SW must ensure that 2 threads do not both access the same cache line (64B)</p>	Project:	All	Format:	Enumeration	Value	Name	Description	0FFh	A32_A64 <b>[Default]</b>	Specifies a A32 or A64 Stateless access that is locally coherent (coherent within a thread group)	0FDh	A32_A64_NC	Specifies a A32 or A64 Stateless access that is non-coherent (coherent within a thread).	Others	Reserved	Ignored
Project:	All																	
Format:	Enumeration																	
Value	Name	Description																
0FFh	A32_A64 <b>[Default]</b>	Specifies a A32 or A64 Stateless access that is locally coherent (coherent within a thread group)																
0FDh	A32_A64_NC	Specifies a A32 or A64 Stateless access that is non-coherent (coherent within a thread).																
Others	Reserved	Ignored																

## Stateless Block Message Header

MH_A32_GO - Stateless Block Message Header								
DWord	Bit	Description						
0-1	63:0	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Ignore</td> </tr> <tr> <td colspan="2">Ignored</td></tr> </table>	Project:	All	Format:	Ignore	Ignored	
Project:	All							
Format:	Ignore							
Ignored								
2	31:0	<p><b>Global Offset</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U32</td> </tr> </table> <p>Specifies the global element index into the buffer, in units of Owords, Dwords, or Bytes (depending on the message).</p> <p><b>Programming Notes</b></p> <p>If the address offset calculated with the Buffer Base Address and Global Offset is greater than the PTSS size or the GeneralStateBufferSize, then the access is Out-of-Bounds.</p>	Project:	All	Format:	U32		
Project:	All							
Format:	U32							
3	31:0	<p><b>Per Thread Scratch Space</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td><b>MHC_PTSS</b></td> </tr> </table> <p>Specifies amount of scratch space used by this thread, for Stateless bounds checking.</p>	Project:	All	Format:	<b>MHC_PTSS</b>		
Project:	All							
Format:	<b>MHC_PTSS</b>							
4	31:0	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Ignore</td> </tr> <tr> <td colspan="2">Ignored</td></tr> </table>	Project:	All	Format:	Ignore	Ignored	
Project:	All							
Format:	Ignore							
Ignored								
5	31:0	<p><b>Buffer Base Address</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td><b>MHC_A32_BBA</b></td> </tr> </table> <p>Specifies the surface address offset page [31:10] for A32 stateless messages.</p>	Project:	All	Format:	<b>MHC_A32_BBA</b>		
Project:	All							
Format:	<b>MHC_A32_BBA</b>							

## MH\_A32\_GO - Stateless Block Message Header

6-7		63:0		Reserved	
				Project:	All
				Format:	Ignore
				Ignored	

## Stateless Surface Message Header

MH1_A32 - Stateless Surface Message Header								
DWord	Bit	Description						
0-4	159:0	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Ignore</td> </tr> <tr> <td colspan="2">Ignored</td></tr> </table>	Project:	All	Format:	Ignore	Ignored	
Project:	All							
Format:	Ignore							
Ignored								
5	31:0	<p><b>Buffer Base Address</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td><b>MHC_A32_BBA</b></td> </tr> </table> <p>Specifies the surface address offset page [31:10] for A32 stateless messages.</p>	Project:	All	Format:	<b>MHC_A32_BBA</b>		
Project:	All							
Format:	<b>MHC_A32_BBA</b>							
6-7	63:0	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Ignore</td> </tr> <tr> <td colspan="2">Ignored</td></tr> </table>	Project:	All	Format:	Ignore	Ignored	
Project:	All							
Format:	Ignore							
Ignored								

## Stateless Surface Pixel Mask Message Header

### MH1\_A32\_PSM - Stateless Surface Pixel Mask Message Header

Project:	BDW							
Source:	DataPort 1							
Size (in bits):	256							
Default Value:	0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x0000FFFF							
DWord	Bit	Description						
0-4	159:0	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>Ignore</td> </tr> <tr> <td colspan="2">Ignored</td></tr> </table>	Format:	Ignore	Ignored			
Format:	Ignore							
Ignored								
5	31:0	<p><b>Buffer Base Address</b></p> <table border="1"> <tr> <td>Format:</td> <td><b>MHC_A32_BBA</b></td> </tr> <tr> <td colspan="2">Specifies the surface address offset page [31:10] for A32 stateless messages.</td></tr> </table>	Format:	<b>MHC_A32_BBA</b>	Specifies the surface address offset page [31:10] for A32 stateless messages.			
Format:	<b>MHC_A32_BBA</b>							
Specifies the surface address offset page [31:10] for A32 stateless messages.								
6	31:0	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>Ignore</td> </tr> <tr> <td colspan="2">Ignored</td></tr> </table>	Format:	Ignore	Ignored			
Format:	Ignore							
Ignored								
7	31:0	<p><b>Pixel Sample Mask</b></p> <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Format:</td> <td><b>MHC_PSM</b></td> </tr> <tr> <td colspan="2">Specifies the 16-bit Pixel/Sample Mask used with SIMD16 and SIMD8 surfaces.</td></tr> </table>	Project:	BDW	Format:	<b>MHC_PSM</b>	Specifies the 16-bit Pixel/Sample Mask used with SIMD16 and SIMD8 surfaces.	
Project:	BDW							
Format:	<b>MHC_PSM</b>							
Specifies the 16-bit Pixel/Sample Mask used with SIMD16 and SIMD8 surfaces.								

## Subset Atomic Integer Trinary Operation Message Descriptor Control Field

MDC_AOP3S - Subset Atomic Integer Trinary Operation Message Descriptor Control Field															
DWord	Bit	Description													
0	3:0	<p><b>Atomic Integer Operation Type</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Enumeration</td> </tr> </table> <p>Specifies the atomic integer trinary operation to be performed</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0Eh</td> <td>AOP_CMPWR [Default]</td> <td>new_dst = (src0 == old_dst) ? src1 : old_dst</td> </tr> <tr> <td>Others</td> <td>Reserved</td> <td>Ignored</td> </tr> </tbody> </table> <p><b>Programming Notes</b></p> <p>When Return Data Control is set, old_dst is returned.</p>	Project:	All	Format:	Enumeration	Value	Name	Description	0Eh	AOP_CMPWR [Default]	new_dst = (src0 == old_dst) ? src1 : old_dst	Others	Reserved	Ignored
Project:	All														
Format:	Enumeration														
Value	Name	Description													
0Eh	AOP_CMPWR [Default]	new_dst = (src0 == old_dst) ? src1 : old_dst													
Others	Reserved	Ignored													

## Subset Reversed SIMD Mode 2 Message Descriptor Control Field

<b>MDC_SM2RS - Subset Reversed SIMD Mode 2 Message Descriptor Control Field</b>															
Project:	BDW														
Size (in bits):	1														
Default Value:	0x00000001														
DWord	Bit	Description													
0	0	<p><b>SIMD Mode</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>Enumeration</td></tr> </table> <p>Specifies the SIMD mode of the message (number of slots processed)</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0h</td><td>Reserved</td><td>Not used</td></tr> <tr> <td>01h</td><td>SIMD8 <b>[Default]</b></td><td>SIMD8</td></tr> </tbody> </table>	Project:	All	Format:	Enumeration	Value	Name	Description	0h	Reserved	Not used	01h	SIMD8 <b>[Default]</b>	SIMD8
Project:	All														
Format:	Enumeration														
Value	Name	Description													
0h	Reserved	Not used													
01h	SIMD8 <b>[Default]</b>	SIMD8													

## Subset SIMD Mode 2 Message Descriptor Control Field

MDC_SM2S - Subset SIMD Mode 2 Message Descriptor Control Field															
DWord	Bit	Description													
0	0	<b>SIMD Mode</b> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Enumeration</td> </tr> </table> <p>Specifies the SIMD mode of the message (number of slots processed)</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00h</td> <td>SIMD8</td> <td>SIMD8</td> </tr> <tr> <td>01h</td> <td>Reserved</td> <td>Ignored</td> </tr> </tbody> </table>	Project:	All	Format:	Enumeration	Value	Name	Description	00h	SIMD8	SIMD8	01h	Reserved	Ignored
Project:	All														
Format:	Enumeration														
Value	Name	Description													
00h	SIMD8	SIMD8													
01h	Reserved	Ignored													

## Subset SIMD Mode 3 Message Descriptor Control Field

### MDC\_SM3S - Subset SIMD Mode 3 Message Descriptor Control Field

Project: BDW  
 Size (in bits): 2  
 Default Value: 0x00000000

DWord	Bit	Description		
0	1:0	<b>SIMD Mode</b>		
		Project:	All	
		Format:	Enumeration	
		Specifies the SIMD mode of the message (number of slots processed)		
Value		Name	Description	
00h		SIMD4x2	SIMD4x2	
01h		Reserved	Ignored	
02h		SIMD8	SIMD8	
03h		Reserved	Ignored	

## Subspan Render Target Message Header Control

### MHC\_RT\_SUBSPAN - Subspan Render Target Message Header Control

Project: BDW  
Size (in bits): 32  
Default Value: 0x00000000

DWord	Bit	Description		
0	31:16	<b>Y</b>		
		<table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U16</td></tr> </table> <p>Y coordinate for upper-left pixel of this subspan</p>	Project:	All
Project:	All			
Format:	U16			
	15:0	<b>X</b>		
		<table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U16</td></tr> </table> <p>X coordinate for upper-left pixel of this subspan</p>	Project:	All
Project:	All			
Format:	U16			

## Surface Binding Table Index Message Descriptor Control Field

<b>MDC_BTS - Surface Binding Table Index Message Descriptor Control Field</b>																							
Project: BDW Size (in bits): 8 Default Value: 0x00000000																							
DWord	Bit	Description																					
0	7:0	<b>Binding Table Index</b> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Enumeration</td> </tr> <tr> <td colspan="2">Specifies the Binding Table index for the message, which must be a Surface State Model.</td></tr> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> <tr> <td>00h-0EFh</td><td>BTS</td><td>Index of Binding Table State Surfaces</td></tr> <tr> <td>F0h-0FBh</td><td>Reserved</td><td>Reserved for future use</td></tr> <tr> <td>0FCh</td><td>Reserved</td><td>Reserved for future use</td></tr> <tr> <td>Others</td><td>Reserved</td><td>Ignored</td></tr> </table>	Project:	All	Format:	Enumeration	Specifies the Binding Table index for the message, which must be a Surface State Model.		Value	Name	Description	00h-0EFh	BTS	Index of Binding Table State Surfaces	F0h-0FBh	Reserved	Reserved for future use	0FCh	Reserved	Reserved for future use	Others	Reserved	Ignored
Project:	All																						
Format:	Enumeration																						
Specifies the Binding Table index for the message, which must be a Surface State Model.																							
Value	Name	Description																					
00h-0EFh	BTS	Index of Binding Table State Surfaces																					
F0h-0FBh	Reserved	Reserved for future use																					
0FCh	Reserved	Reserved for future use																					
Others	Reserved	Ignored																					

## Surface or Stateless Binding Table Index Message Descriptor Control Field

<b>MDC_BTS_A32 - Surface or Stateless Binding Table Index Message Descriptor Control Field</b>																											
<b>DWord</b>	<b>Bit</b>	<b>Description</b>																									
0	7:0	<p><b>Binding Table Index</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Enumeration</td> </tr> </table> <p>Specifies the surface for the message, either Surface State Model or Stateless.</p> <table border="1"> <thead> <tr> <th><b>Value</b></th> <th><b>Name</b></th> <th><b>Description</b></th> </tr> </thead> <tbody> <tr> <td>00h-0EFh</td> <td>BTS</td> <td>Index of Binding Table State Surfaces</td> </tr> <tr> <td>F0h-OFBh</td> <td>Reserved</td> <td>Reserved for future use</td> </tr> <tr> <td>0FCh</td> <td>Reserved</td> <td>Reserved for future use</td> </tr> <tr> <td>OFFh</td> <td>A32_A64</td> <td>Specifies a A32 or A64 Stateless access that is locally coherent (coherent within a thread group)</td> </tr> <tr> <td>0FDh</td> <td>A32_A64_NC</td> <td>Specifies a A32 or A64 Stateless access that is non-coherent (coherent within a thread).</td> </tr> <tr> <td>Others</td> <td>Reserved</td> <td>Ignored</td> </tr> </tbody> </table> <p><b>Restriction</b></p> <p>When using A32_A64_NC, SW must ensure that 2 threads do not both access the same cache line (64B)</p>	Project:	All	Format:	Enumeration	<b>Value</b>	<b>Name</b>	<b>Description</b>	00h-0EFh	BTS	Index of Binding Table State Surfaces	F0h-OFBh	Reserved	Reserved for future use	0FCh	Reserved	Reserved for future use	OFFh	A32_A64	Specifies a A32 or A64 Stateless access that is locally coherent (coherent within a thread group)	0FDh	A32_A64_NC	Specifies a A32 or A64 Stateless access that is non-coherent (coherent within a thread).	Others	Reserved	Ignored
Project:	All																										
Format:	Enumeration																										
<b>Value</b>	<b>Name</b>	<b>Description</b>																									
00h-0EFh	BTS	Index of Binding Table State Surfaces																									
F0h-OFBh	Reserved	Reserved for future use																									
0FCh	Reserved	Reserved for future use																									
OFFh	A32_A64	Specifies a A32 or A64 Stateless access that is locally coherent (coherent within a thread group)																									
0FDh	A32_A64_NC	Specifies a A32 or A64 Stateless access that is non-coherent (coherent within a thread).																									
Others	Reserved	Ignored																									

## Surface Pixel Mask Message Header

<b>MH1_BTS_PSM - Surface Pixel Mask Message Header</b>						
Project: BDW Source: DataPort 1 Size (in bits): 256 Default Value: 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x0000FFFF						
<b>DWord</b>	<b>Bit</b>	<b>Description</b>				
0-6	223:0	<b>Reserved</b> <table border="1"> <tr> <td>Format:</td> <td>Ignore</td> </tr> <tr> <td colspan="2">Ignored</td></tr> </table>	Format:	Ignore	Ignored	
Format:	Ignore					
Ignored						
7	31:0	<b>Pixel Sample Mask</b> <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Format:</td> <td><b>MHC_PSM</b></td> </tr> </table> <p>Specifies the 16-bit Pixel/Sample Mask used with SIMD16 and SIMD8 surfaces.</p>	Project:	BDW	Format:	<b>MHC_PSM</b>
Project:	BDW					
Format:	<b>MHC_PSM</b>					

## SW Generated BINDING\_TABLE\_STATE

SW Generated BINDING_TABLE_STATE				
DWord	Bit	Description		
0	31:5	<p><b>Surface State Pointer</b></p> <table border="1"> <tr> <td>Format:</td> <td>SurfaceStateOffset[31:5]</td> </tr> </table> <p>This 32-byte aligned address points to a surface state block. This pointer is relative to the <b>Surface State Base Address</b></p> <p><b>Programming Notes</b></p> <p>Bit 5 of this pointer must be zero (i.e. <b>Surface State Pointer</b> must be 64-byte aligned).</p>	Format:	SurfaceStateOffset[31:5]
Format:	SurfaceStateOffset[31:5]			
4:0	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ	
Format:	MBZ			

## SZ OM S0A SIMD8 Render Target Data Payload

<b>MDP_RTW_ZMA8 - SZ OM S0A SIMD8 Render Target Data Payload</b>						
<b>DWord</b>	<b>Bit</b>	<b>Description</b>				
0.0-0.7	255:0	<p><b>Source 0 Alpha</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW_SIMD8</b></td></tr> </table> <p>Slots [7:0] Source 0 Alpha</p>	Project:	All	Format:	<b>MDP_DW_SIMD8</b>
Project:	All					
Format:	<b>MDP_DW_SIMD8</b>					
1.0-1.7	255:0	<p><b>oMask</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDPR_OMASK</b></td></tr> </table> <p>Slots [7:0] oMask. Upper half ignored.</p>	Project:	All	Format:	<b>MDPR_OMASK</b>
Project:	All					
Format:	<b>MDPR_OMASK</b>					
2.0-2.7	255:0	<p><b>Red</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW_SIMD8</b></td></tr> </table> <p>Slots [7:0] Red</p>	Project:	All	Format:	<b>MDP_DW_SIMD8</b>
Project:	All					
Format:	<b>MDP_DW_SIMD8</b>					
3.0-3.7	255:0	<p><b>Green</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW_SIMD8</b></td></tr> </table> <p>Slots [7:0] Green</p>	Project:	All	Format:	<b>MDP_DW_SIMD8</b>
Project:	All					
Format:	<b>MDP_DW_SIMD8</b>					
4.0-4.7	255:0	<p><b>Blue</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW_SIMD8</b></td></tr> </table> <p>Slots [7:0] Blue</p>	Project:	All	Format:	<b>MDP_DW_SIMD8</b>
Project:	All					
Format:	<b>MDP_DW_SIMD8</b>					

## MDP\_RTW\_ZMA8 - SZ OM S0A SIMD8 Render Target Data Payload

5.0-5.7	255:0	<b>Alpha</b>		
		<table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW SIMD8</b></td></tr> </table>	Project:	All
Project:	All			
Format:	<b>MDP_DW SIMD8</b>			
Slots [7:0] Alpha				
6.0-6.7	255:0	<b>Source Depth</b>		
		<table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW SIMD8</b></td></tr> </table>	Project:	All
Project:	All			
Format:	<b>MDP_DW SIMD8</b>			
Slots [7:0] Source Depth				

## SZ OM S0A SIMD16 Render Target Data Payload

<b>MDP_RTW_ZMA16 - SZ OM S0A SIMD16 Render Target Data Payload</b>						
<b>DWord</b>	<b>Bit</b>	<b>Description</b>				
0.0-1.7	511:0	<p><b>Source 0 Alpha</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW SIMD16</b></td></tr> </table> <p>Slots [15:0] Source 0 Alpha</p>	Project:	All	Format:	<b>MDP_DW SIMD16</b>
Project:	All					
Format:	<b>MDP_DW SIMD16</b>					
2.0-2.7	255:0	<p><b>oMask</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDPR_OMASK</b></td></tr> </table> <p>Slots [15:0] oMask</p>	Project:	All	Format:	<b>MDPR_OMASK</b>
Project:	All					
Format:	<b>MDPR_OMASK</b>					
3.0-4.7	511:0	<p><b>Red</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW SIMD16</b></td></tr> </table> <p>Slots [15:0] Red</p>	Project:	All	Format:	<b>MDP_DW SIMD16</b>
Project:	All					
Format:	<b>MDP_DW SIMD16</b>					

## **MDP\_RTW\_ZMA16 - SZ OM S0A SIMD16 Render Target Data Payload**

5.0-6.7	511:0	<p><b>Green</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW SIMD16</b></td></tr> </table> <p>Slots [15:0] Green</p>	Project:	All	Format:	<b>MDP_DW SIMD16</b>
Project:	All					
Format:	<b>MDP_DW SIMD16</b>					
7.0-8.7	511:0	<p><b>Blue</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW SIMD16</b></td></tr> </table> <p>Slots [15:0] Blue</p>	Project:	All	Format:	<b>MDP_DW SIMD16</b>
Project:	All					
Format:	<b>MDP_DW SIMD16</b>					
9.0-10.7	511:0	<p><b>Alpha</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW SIMD16</b></td></tr> </table> <p>Slots [15:0] Alpha</p>	Project:	All	Format:	<b>MDP_DW SIMD16</b>
Project:	All					
Format:	<b>MDP_DW SIMD16</b>					
11.0-12.7	511:0	<p><b>Source Depth</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW SIMD16</b></td></tr> </table> <p>Slots [15:0] Source Depth</p>	Project:	All	Format:	<b>MDP_DW SIMD16</b>
Project:	All					
Format:	<b>MDP_DW SIMD16</b>					

SZ OM SIMD8 Dual Source Render Target Data Payload

## MDP\_RTW\_ZM8DS - SZ OM SIMD8 Dual Source Render Target Data Payload

4.0-4.7	255:0	<b>Src0 Alpha</b>		
		<table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW_SIMD8</b></td></tr> </table> <p>Slots[7:0] or [15:8] of Src0 Alpha</p>	Project:	All
Project:	All			
Format:	<b>MDP_DW_SIMD8</b>			
5.0-5.7	255:0	<b>Src1 Red</b>		
		<table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW_SIMD8</b></td></tr> </table> <p>Slots[7:0] or [15:8] of Src1 Red</p>	Project:	All
Project:	All			
Format:	<b>MDP_DW_SIMD8</b>			
6.0-6.7	255:0	<b>Src1 Green</b>		
		<table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW_SIMD8</b></td></tr> </table> <p>Slots[7:0] or [15:8] of Src1 Green</p>	Project:	All
Project:	All			
Format:	<b>MDP_DW_SIMD8</b>			
7.0-7.7	255:0	<b>Src1 Blue</b>		
		<table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW_SIMD8</b></td></tr> </table> <p>Slots[7:0] or [15:8] of Src1 Blue</p>	Project:	All
Project:	All			
Format:	<b>MDP_DW_SIMD8</b>			
8.0-8.7	255:0	<b>Src1 Alpha</b>		
		<table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW_SIMD8</b></td></tr> </table> <p>Slots[7:0] or [15:8] of Src1 Alpha</p>	Project:	All
Project:	All			
Format:	<b>MDP_DW_SIMD8</b>			
9.0-9.7	255:0	<b>Source Depth</b>		
		<table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW_SIMD8</b></td></tr> </table> <p>Slots [7:0] or [15:8] of Source Depth</p>	Project:	All
Project:	All			
Format:	<b>MDP_DW_SIMD8</b>			

## SZ OM SIMD8 Render Target Data Payload

<b>MDP_RTW_ZM8 - SZ OM SIMD8 Render Target Data Payload</b>						
<b>DWord</b>	<b>Bit</b>	<b>Description</b>				
0.0-0.7	255:0	<p><b>oMask</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDPR_OMASK</b></td></tr> </table> <p>Slots [7:0] oMask. Upper half ignored.</p>	Project:	All	Format:	<b>MDPR_OMASK</b>
Project:	All					
Format:	<b>MDPR_OMASK</b>					
1.0-1.7	255:0	<p><b>Red</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW_SIMD8</b></td></tr> </table> <p>Slots [7:0] Red</p>	Project:	All	Format:	<b>MDP_DW_SIMD8</b>
Project:	All					
Format:	<b>MDP_DW_SIMD8</b>					
2.0-2.7	255:0	<p><b>Green</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW_SIMD8</b></td></tr> </table> <p>Slots [7:0] Green</p>	Project:	All	Format:	<b>MDP_DW_SIMD8</b>
Project:	All					
Format:	<b>MDP_DW_SIMD8</b>					
3.0-3.7	255:0	<p><b>Blue</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW_SIMD8</b></td></tr> </table> <p>Slots [7:0] Blue</p>	Project:	All	Format:	<b>MDP_DW_SIMD8</b>
Project:	All					
Format:	<b>MDP_DW_SIMD8</b>					
4.0-4.7	255:0	<p><b>Alpha</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW_SIMD8</b></td></tr> </table> <p>Slots [7:0] Alpha</p>	Project:	All	Format:	<b>MDP_DW_SIMD8</b>
Project:	All					
Format:	<b>MDP_DW_SIMD8</b>					

**MDP\_RTW\_ZM8 - SZ OM SIMD8 Render Target Data Payload**

5.0-5.7	255:0	<b>Source Depth</b>
		Project: All
		Format: <b>MDP_DW SIMD8</b>
Slots [7:0] Source Depth		

# SZ OM SIMD16 Render Target Data Payload

## MDP\_RTW\_ZM16 - SZ OM SIMD16 Render Target Data Payload

4.0-4.7	255:0	<b>Green[15:7]</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW_SIMD8</b></td></tr> </table> <p>Slots [15:8] Green</p>	Project:	All	Format:	<b>MDP_DW_SIMD8</b>
Project:	All					
Format:	<b>MDP_DW_SIMD8</b>					
5.0-5.7	255:0	<b>Blue[7:0]</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW_SIMD8</b></td></tr> </table> <p>Slots [7:0] Blue</p>	Project:	All	Format:	<b>MDP_DW_SIMD8</b>
Project:	All					
Format:	<b>MDP_DW_SIMD8</b>					
6.0-6.7	255:0	<b>Blue[15:8]</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW_SIMD8</b></td></tr> </table> <p>Slots [15:8] Blue</p>	Project:	All	Format:	<b>MDP_DW_SIMD8</b>
Project:	All					
Format:	<b>MDP_DW_SIMD8</b>					
7.0-7.7	255:0	<b>Alpha[7:0]</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW_SIMD8</b></td></tr> </table> <p>Slots [7:0] Alpha</p>	Project:	All	Format:	<b>MDP_DW_SIMD8</b>
Project:	All					
Format:	<b>MDP_DW_SIMD8</b>					
8.0-8.7	255:0	<b>Alpha[15:8]</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW_SIMD8</b></td></tr> </table> <p>Slots [15:8] Alpha</p>	Project:	All	Format:	<b>MDP_DW_SIMD8</b>
Project:	All					
Format:	<b>MDP_DW_SIMD8</b>					
9.0-9.7	255:0	<b>Source Depth[7:0]</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW_SIMD8</b></td></tr> </table> <p>Slots [7:0] Source Depth</p>	Project:	All	Format:	<b>MDP_DW_SIMD8</b>
Project:	All					
Format:	<b>MDP_DW_SIMD8</b>					
10.0-10.7	255:0	<b>Source Depth[15:8]</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW_SIMD8</b></td></tr> </table> <p>Slots [15:8] Source Depth</p>	Project:	All	Format:	<b>MDP_DW_SIMD8</b>
Project:	All					
Format:	<b>MDP_DW_SIMD8</b>					

## SZ S0A SIMD8 Render Target Data Payload

<b>MDP_RTW_ZA8 - SZ S0A SIMD8 Render Target Data Payload</b>						
<b>DWord</b>	<b>Bit</b>	<b>Description</b>				
0.0-0.7	255:0	<p><b>Source 0 Alpha</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW_SIMD8</b></td></tr> </table> <p>Slots [7:0] Source 0 Alpha</p>	Project:	All	Format:	<b>MDP_DW_SIMD8</b>
Project:	All					
Format:	<b>MDP_DW_SIMD8</b>					
1.0-1.7	255:0	<p><b>Red</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW_SIMD8</b></td></tr> </table> <p>Slots [7:0] Red</p>	Project:	All	Format:	<b>MDP_DW_SIMD8</b>
Project:	All					
Format:	<b>MDP_DW_SIMD8</b>					
2.0-2.7	255:0	<p><b>Green</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW_SIMD8</b></td></tr> </table> <p>Slots [7:0] Green</p>	Project:	All	Format:	<b>MDP_DW_SIMD8</b>
Project:	All					
Format:	<b>MDP_DW_SIMD8</b>					
3.0-3.7	255:0	<p><b>Blue</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW_SIMD8</b></td></tr> </table> <p>Slots [7:0] Blue</p>	Project:	All	Format:	<b>MDP_DW_SIMD8</b>
Project:	All					
Format:	<b>MDP_DW_SIMD8</b>					
4.0-4.7	255:0	<p><b>Alpha</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW_SIMD8</b></td></tr> </table> <p>Slots [7:0] Alpha</p>	Project:	All	Format:	<b>MDP_DW_SIMD8</b>
Project:	All					
Format:	<b>MDP_DW_SIMD8</b>					

## MDP\_RTW\_ZA8 - SZ SOA SIMD8 Render Target Data Payload

5.0-5.7	255:0	<b>Source Depth</b> <table border="1"><tr><td>Project:</td><td>All</td></tr><tr><td>Format:</td><td><b>MDP_DW SIMD8</b></td></tr></table> <p>Slots [7:0] Source Depth</p>	Project:	All	Format:	<b>MDP_DW SIMD8</b>
Project:	All					
Format:	<b>MDP_DW SIMD8</b>					

# SZ SOA SIMD16 Render Target Data Payload

MDP_RTW_ZA16 - SZ SOA SIMD16 Render Target Data Payload						
4.0-4.7	255:0	<b>Green[7:0]</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW SIMD8</b></td></tr> </table> Slots [7:0] Green	Project:	All	Format:	<b>MDP_DW SIMD8</b>
Project:	All					
Format:	<b>MDP_DW SIMD8</b>					
5.0-5.7	255:0	<b>Green[15:8]</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW SIMD8</b></td></tr> </table> Slots [15:8] Green	Project:	All	Format:	<b>MDP_DW SIMD8</b>
Project:	All					
Format:	<b>MDP_DW SIMD8</b>					
6.0-6.7	255:0	<b>Blue[7:0]</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW SIMD8</b></td></tr> </table> Slots [7:0] Blue	Project:	All	Format:	<b>MDP_DW SIMD8</b>
Project:	All					
Format:	<b>MDP_DW SIMD8</b>					
7.0-7.7	255:0	<b>Blue[15:7]</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW SIMD8</b></td></tr> </table> Slots [15:8] Blue	Project:	All	Format:	<b>MDP_DW SIMD8</b>
Project:	All					
Format:	<b>MDP_DW SIMD8</b>					
8.0-8.7	255:0	<b>Alpha[7:0]</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW SIMD8</b></td></tr> </table> Slots [7:0] Alpha	Project:	All	Format:	<b>MDP_DW SIMD8</b>
Project:	All					
Format:	<b>MDP_DW SIMD8</b>					
9.0-9.7	255:0	<b>Alpha[15:8]</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW SIMD8</b></td></tr> </table> Slots [15:8] Alpha	Project:	All	Format:	<b>MDP_DW SIMD8</b>
Project:	All					
Format:	<b>MDP_DW SIMD8</b>					
10.0-10.7	255:0	<b>Source Depth[7:0]</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW SIMD8</b></td></tr> </table> Slots [7:0] Source Depth	Project:	All	Format:	<b>MDP_DW SIMD8</b>
Project:	All					
Format:	<b>MDP_DW SIMD8</b>					
11.0-11.7	255:0	<b>Source Depth[15:8]</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW SIMD8</b></td></tr> </table> Slots [15:8] Source Depth	Project:	All	Format:	<b>MDP_DW SIMD8</b>
Project:	All					
Format:	<b>MDP_DW SIMD8</b>					

## SZ SIMD8 Dual Source Render Target Data Payload

<b>MDP_RTW_Z8DS - SZ SIMD8 Dual Source Render Target Data Payload</b>						
<b>DWord</b>	<b>Bit</b>	<b>Description</b>				
0.0-0.7	255:0	<p><b>Src0 Red</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW SIMD8</b></td></tr> </table> <p>Slots[7:0] or [15:8] of Src0 Red</p>	Project:	All	Format:	<b>MDP_DW SIMD8</b>
Project:	All					
Format:	<b>MDP_DW SIMD8</b>					
1.0-1.7	255:0	<p><b>Src0 Green</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW SIMD8</b></td></tr> </table> <p>Slots[7:0] or [15:8] of Src0 Green</p>	Project:	All	Format:	<b>MDP_DW SIMD8</b>
Project:	All					
Format:	<b>MDP_DW SIMD8</b>					
2.0-2.7	255:0	<p><b>Src0 Blue</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW SIMD8</b></td></tr> </table> <p>Slots[7:0] or [15:8] of Src0 Blue</p>	Project:	All	Format:	<b>MDP_DW SIMD8</b>
Project:	All					
Format:	<b>MDP_DW SIMD8</b>					
3.0-3.7	255:0	<p><b>Src0 Alpha</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW SIMD8</b></td></tr> </table> <p>Slots[7:0] or [15:8] of Src0 Alpha</p>	Project:	All	Format:	<b>MDP_DW SIMD8</b>
Project:	All					
Format:	<b>MDP_DW SIMD8</b>					

## **MDP\_RTW\_Z8DS - SZ SIMD8 Dual Source Render Target Data Payload**

4.0-4.7	255:0	<p><b>Src1 Red</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW SIMD8</b></td></tr> </table> <p>Slots[7:0] or [15:8] of Src1 Red</p>	Project:	All	Format:	<b>MDP_DW SIMD8</b>
Project:	All					
Format:	<b>MDP_DW SIMD8</b>					
5.0-5.7	255:0	<p><b>Src1 Green</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW SIMD8</b></td></tr> </table> <p>Slots[7:0] or [15:8] of Src1 Green</p>	Project:	All	Format:	<b>MDP_DW SIMD8</b>
Project:	All					
Format:	<b>MDP_DW SIMD8</b>					
6.0-6.7	255:0	<p><b>Src1 Blue</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW SIMD8</b></td></tr> </table> <p>Slots[7:0] or [15:8] of Src1 Blue</p>	Project:	All	Format:	<b>MDP_DW SIMD8</b>
Project:	All					
Format:	<b>MDP_DW SIMD8</b>					
7.0-7.7	255:0	<p><b>Src1 Alpha</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW SIMD8</b></td></tr> </table> <p>Slots[7:0] or [15:8] of Src1 Alpha</p>	Project:	All	Format:	<b>MDP_DW SIMD8</b>
Project:	All					
Format:	<b>MDP_DW SIMD8</b>					
8.0-8.7	255:0	<p><b>Source Depth</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW SIMD8</b></td></tr> </table> <p>Slots [7:0] or [15:8] of Source Depth</p>	Project:	All	Format:	<b>MDP_DW SIMD8</b>
Project:	All					
Format:	<b>MDP_DW SIMD8</b>					

## SZ SIMD8 Render Target Data Payload

<b>MDP_RTW_Z8 - SZ SIMD8 Render Target Data Payload</b>						
<b>DWord</b>	<b>Bit</b>	<b>Description</b>				
0.0-0.7	255:0	<b>Red</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW SIMD8</b></td></tr> </table> Slots [7:0] Red	Project:	All	Format:	<b>MDP_DW SIMD8</b>
Project:	All					
Format:	<b>MDP_DW SIMD8</b>					
1.0-1.7	255:0	<b>Green</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW SIMD8</b></td></tr> </table> Slots [7:0] Green	Project:	All	Format:	<b>MDP_DW SIMD8</b>
Project:	All					
Format:	<b>MDP_DW SIMD8</b>					
2.0-2.7	255:0	<b>Blue</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW SIMD8</b></td></tr> </table> Slots [7:0] Blue	Project:	All	Format:	<b>MDP_DW SIMD8</b>
Project:	All					
Format:	<b>MDP_DW SIMD8</b>					
3.0-3.7	255:0	<b>Alpha</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW SIMD8</b></td></tr> </table> Slots [7:0] Alpha	Project:	All	Format:	<b>MDP_DW SIMD8</b>
Project:	All					
Format:	<b>MDP_DW SIMD8</b>					
4.0-4.7	255:0	<b>Source Depth</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW SIMD8</b></td></tr> </table> Slots [7:0] Source Depth	Project:	All	Format:	<b>MDP_DW SIMD8</b>
Project:	All					
Format:	<b>MDP_DW SIMD8</b>					

## SZ SIMD16 Render Target Data Payload

MDP_RTW_Z16 - SZ SIMD16 Render Target Data Payload						
DWord	Bit	Description				
0.0-0.7	255:0	<p><b>Red[7:0]</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW SIMD8</b></td></tr> </table> <p>Slots [7:0] Red</p>	Project:	All	Format:	<b>MDP_DW SIMD8</b>
Project:	All					
Format:	<b>MDP_DW SIMD8</b>					
1.0-1.7	255:0	<p><b>Red[15:8]</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW SIMD8</b></td></tr> </table> <p>Slots [15:8] Red</p>	Project:	All	Format:	<b>MDP_DW SIMD8</b>
Project:	All					
Format:	<b>MDP_DW SIMD8</b>					
2.0-2.7	255:0	<p><b>Green[7:0]</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW SIMD8</b></td></tr> </table> <p>Slots [7:0] Green</p>	Project:	All	Format:	<b>MDP_DW SIMD8</b>
Project:	All					
Format:	<b>MDP_DW SIMD8</b>					
3.0-3.7	255:0	<p><b>Green[15:8]</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW SIMD8</b></td></tr> </table> <p>Slots [15:8] Green</p>	Project:	All	Format:	<b>MDP_DW SIMD8</b>
Project:	All					
Format:	<b>MDP_DW SIMD8</b>					

<b>MDP_RTW_Z16 - SZ SIMD16 Render Target Data Payload</b>							
4.0-4.7	255:0	<b>Blue[7:0]</b>	<table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW SIMD8</b></td></tr> </table> Slots [7:0] Blue	Project:	All	Format:	<b>MDP_DW SIMD8</b>
Project:	All						
Format:	<b>MDP_DW SIMD8</b>						
5.0-5.7	255:0	<b>Blue[15:8]</b>	<table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW SIMD8</b></td></tr> </table> Slots [15:8] Blue	Project:	All	Format:	<b>MDP_DW SIMD8</b>
Project:	All						
Format:	<b>MDP_DW SIMD8</b>						
6.0-6.7	255:0	<b>Alpha[7:0]</b>	<table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW SIMD8</b></td></tr> </table> Slots [7:0] Alpha	Project:	All	Format:	<b>MDP_DW SIMD8</b>
Project:	All						
Format:	<b>MDP_DW SIMD8</b>						
7.0-7.7	255:0	<b>Alpha[15:8]</b>	<table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW SIMD8</b></td></tr> </table> Slots [15:8] Alpha	Project:	All	Format:	<b>MDP_DW SIMD8</b>
Project:	All						
Format:	<b>MDP_DW SIMD8</b>						
8.0-8.7	255:0	<b>Source Depth[7:0]</b>	<table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW SIMD8</b></td></tr> </table> Slots [7:0] Source Depth	Project:	All	Format:	<b>MDP_DW SIMD8</b>
Project:	All						
Format:	<b>MDP_DW SIMD8</b>						
9.0-9.7	255:0	<b>Source Depth[15:8]</b>	<table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDP_DW SIMD8</b></td></tr> </table> Slots [15:8] Source Depth	Project:	All	Format:	<b>MDP_DW SIMD8</b>
Project:	All						
Format:	<b>MDP_DW SIMD8</b>						

## Thread EOT Message Descriptor

TS_EOT - Thread EOT Message Descriptor		
DWord	Bit	Description
0	31:29	<b>Reserved</b>
		Format: MBZ
	28:25	<b>Message Length</b>
		Default Value: 1h One GRF
		Format: U4
	24:20	<b>Response Length</b>
		Default Value: 0h Zero GRF
		Format: U5
	19	<b>Header Present</b>
		Format: MBZ
	18:1	<b>Reserved</b>
		Format: MBZ
	0	<b>Message Type</b>
		Default Value: 0h End Thread
		Format: Opcode
		End of Thread message opcode

## Thread Spawn Message Descriptor

Thread Spawn Message Descriptor																						
DWord	Bit	Description																				
0	31:20	<b>Reserved</b>																				
		Format:	MBZ																			
	19	<b>Header Present</b>																				
		Format:	MBZ																			
	<b>Programming Notes</b>																					
	This bit MBZ for all Thread Spawner messages.																					
	18:5	<b>Reserved</b>																				
		Format:	MBZ																			
	4	<b>Resource Select</b> This field specifies the resource associated with the action taken by the Opcode.																				
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> <th>Exists If</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Spawn Child</td> <td>Spawn a Child Thread</td> <td>[Opcode] == 'Spawn Thread'</td> </tr> <tr> <td>1</td> <td>Spawn Root</td> <td>Spawn a Root Thread</td> <td>[Opcode] == 'Spawn Thread'</td> </tr> <tr> <td>0</td> <td>Dereference Resource</td> <td>The URB Handle is Dereferenced</td> <td>[Opcode] == 'Dereference Resource'</td> </tr> <tr> <td>1</td> <td>Keep Resource</td> <td>The URBHandle is NOT Dereferenced</td> <td>[Opcode] == 'Dereference Resource'</td> </tr> </tbody> </table>		Value	Name	Description	Exists If	0	Spawn Child	Spawn a Child Thread	[Opcode] == 'Spawn Thread'	1	Spawn Root	Spawn a Root Thread	[Opcode] == 'Spawn Thread'	0	Dereference Resource	The URB Handle is Dereferenced	[Opcode] == 'Dereference Resource'	1	Keep Resource	The URBHandle is NOT Dereferenced
Value	Name	Description	Exists If																			
0	Spawn Child	Spawn a Child Thread	[Opcode] == 'Spawn Thread'																			
1	Spawn Root	Spawn a Root Thread	[Opcode] == 'Spawn Thread'																			
0	Dereference Resource	The URB Handle is Dereferenced	[Opcode] == 'Dereference Resource'																			
1	Keep Resource	The URBHandle is NOT Dereferenced	[Opcode] == 'Dereference Resource'																			
3:2	<b>Reserved</b>																					
		Format:	MBZ																			
1	<b>Requester Type</b> This field indicates whether the requesting thread is a root thread or a child thread. If it is a root thread, when Opcode is 0, FF managed resources are dereferenced. If it is a child thread and Opcode is 0, no resource is dereferenced; no action is required by the TS.																					
	<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Root Thread</td> </tr> <tr> <td>1</td> <td>Child Thread</td> </tr> </tbody> </table>			Value	Name	0	Root Thread	1	Child Thread													
Value	Name																					
0	Root Thread																					
1	Child Thread																					

## Thread Spawn Message Descriptor

	0	<b>Opcode</b> Indicates the operation performed by the message. A root thread must terminate with a message to TS (Opcode == 0 and EOT == 1). A child thread should also terminate with such a message. A thread cannot terminate with an Opcode of "spawn thread".
Value	Name	Description
0	Dereference Resource	also used for end of thread
1	Spawn Thread	

## TileW SIMD8 Data Control Dword

MDCD_TILEW - TileW SIMD8 Data Control Dword						
DWord	Bit	Description				
0	31:8	<b>Reserved</b>				
		<table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>Ignore</td></tr> <tr> <td colspan="2">Ignored</td></tr> </table>	Project:	All	Format:	Ignore
Project:	All					
Format:	Ignore					
Ignored						
	7:0	<b>Red</b>				
		<table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U8</td></tr> </table> <p>Specifies the value of the red channel to be read or written.</p>	Project:	All	Format:	U8
Project:	All					
Format:	U8					

## TileW SIMD8 Data Payload

MDP_TILEW SIMD8 - TileW SIMD8 Data Payload						
DWord	Bit	Description				
0.0	31:0	<p><b>Red Slot0</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDCD_TileW</b></td></tr> </table> <p>Specifies the Slot 0 red channel data</p>	Project:	All	Format:	<b>MDCD_TileW</b>
Project:	All					
Format:	<b>MDCD_TileW</b>					
0.1	31:0	<p><b>Red Slot1</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDCD_TileW</b></td></tr> </table> <p>Specifies the Slot 1 red channel data</p>	Project:	All	Format:	<b>MDCD_TileW</b>
Project:	All					
Format:	<b>MDCD_TileW</b>					
0.2	31:0	<p><b>Red Slot2</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDCD_TileW</b></td></tr> </table> <p>Specifies the Slot 2 red channel data</p>	Project:	All	Format:	<b>MDCD_TileW</b>
Project:	All					
Format:	<b>MDCD_TileW</b>					
0.3	31:0	<p><b>Red Slot3</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDCD_TileW</b></td></tr> </table> <p>Specifies the Slot 3 red channel data</p>	Project:	All	Format:	<b>MDCD_TileW</b>
Project:	All					
Format:	<b>MDCD_TileW</b>					
0.4	31:0	<p><b>Red Slot4</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDCD_TileW</b></td></tr> </table> <p>Specifies the Slot 4 red channel data</p>	Project:	All	Format:	<b>MDCD_TileW</b>
Project:	All					
Format:	<b>MDCD_TileW</b>					
0.5	31:0	<p><b>Red Slot5</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDCD_TileW</b></td></tr> </table> <p>Specifies the Slot 5 red channel data</p>	Project:	All	Format:	<b>MDCD_TileW</b>
Project:	All					
Format:	<b>MDCD_TileW</b>					

<b>MDP_TILEW SIMD8 - TileW SIMD8 Data Payload</b>						
0.6	31:0	<p><b>Red Slot6</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDCD_TileW</b></td></tr> </table> <p>Specifies the Slot 6 red channel data</p>	Project:	All	Format:	<b>MDCD_TileW</b>
Project:	All					
Format:	<b>MDCD_TileW</b>					
0.7	31:0	<p><b>Red Slot7</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>MDCD_TileW</b></td></tr> </table> <p>Specifies the Slot 7 red channel data</p>	Project:	All	Format:	<b>MDCD_TileW</b>
Project:	All					
Format:	<b>MDCD_TileW</b>					

## Transpose Message Header

MH_T - Transpose Message Header		
DWord	Bit	Description
0	31:0	<b>X Offset</b>
		Project: All
		Format: S31
		X offset (in bytes) of the upper left corner of the block into the surface.
		<b>Programming Notes</b>
1	31:0	<b>Y Offset</b>
		Project: All
		Format: S31
		Y offset (in rows) of the upper left corner of the block into the surface.
		<b>Programming Notes</b>
2	31:0	<b>Block Dimensions</b>
		Project: All
		Format: <b>MHC_BDIM</b>
		The height and width of the block to transpose.
3-7	159:0	<b>Reserved</b>
		Project: All
		Format: Ignore
		Ignored

## Untyped Write Channel Mask Message Descriptor Control Field

MDC_UW_CMASK - Untyped Write Channel Mask Message Descriptor Control Field																								
DWord	Bit	Description																						
0	3:0	<p><b>Mask</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>Enumeration</td> </tr> </table> <p>For untyped surface write messages, indicates which channels are included in the message payload and written to the surface.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00h</td> <td>RGBA [Default]</td> <td>Red, Green, Blue, and Alpha are included</td> </tr> <tr> <td>08h</td> <td>RGB</td> <td>Red, Green, and Blue are included</td> </tr> <tr> <td>0Ch</td> <td>RG</td> <td>Red and Green are included</td> </tr> <tr> <td>0Eh</td> <td>R</td> <td>Red is included</td> </tr> <tr> <td>Others</td> <td>Reserved</td> <td>Ignored</td> </tr> </tbody> </table>	Project:	All	Format:	Enumeration	Value	Name	Description	00h	RGBA [Default]	Red, Green, Blue, and Alpha are included	08h	RGB	Red, Green, and Blue are included	0Ch	RG	Red and Green are included	0Eh	R	Red is included	Others	Reserved	Ignored
Project:	All																							
Format:	Enumeration																							
Value	Name	Description																						
00h	RGBA [Default]	Red, Green, Blue, and Alpha are included																						
08h	RGB	Red, Green, and Blue are included																						
0Ch	RG	Red and Green are included																						
0Eh	R	Red is included																						
Others	Reserved	Ignored																						

## Upper Oword Block Data Payload

MDP_OW1U - Upper Oword Block Data Payload						
DWord	Bit	Description				
0.0-0.3	127:0	<b>Reserved</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>Ignore</td></tr> </table> Ignored	Project:	All	Format:	Ignore
Project:	All					
Format:	Ignore					
0.4-0.7	127:0	<b>Oword</b> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U128</td></tr> </table> Specifies the upper Oword data element	Project:	All	Format:	U128
Project:	All					
Format:	U128					

## VC1

VC1		
DWord	Bit	Description
0	15:8	<b>Reserved</b> Format: MBZ
	7	<b>Syncmarker Error</b> This flag indicates missing sync marker SEs coded in the bit-stream.
	6	<b>Mbmode SE Error</b> This flag indicates inconsistent Macroblock SEs coded in the bit-stream.
	5	<b>Transformtype SE Error</b> This flag indicates inconsistent transform type SEs coded in the bit-stream.
	4	<b>Coefficient Error</b> This flag indicates inconsistent Coefficient SEs coded in the bit-stream.
	3	<b>Motion Vector SE Error</b> This flag indicates inconsistent Motion Vector SEs coded in the bit-stream.
	2	<b>Coded Block Pattern CY SE Error</b> This flag indicates inconsistent CBPCY SEs coded in the bit-stream.
	1	<b>Mquant Error</b> This flag indicates inconsistent MQUANT SEs coded in the bit-stream.
	0	<b>MB Concealment Flag</b> . Each pulse from this flag indicates one MB is concealed by hardware.

## VCS Hardware-Detected Error Bit Definitions

VCS Hardware-Detected Error Bit Definitions							
DWord	Bit	Description					
0	15:3	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ			
Format:	MBZ						
2	<p><b>Command Privilege Violation Error</b></p> <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> </table> <p>This bit is set if a command classified as privileged is parsed in a non-privileged batch buffer. The command will be converted to a NOOP and parsing will continue.</p>	Project:	BDW				
Project:	BDW						
1	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ				
Format:	MBZ						
0	<p><b>Instruction Error</b></p> <p>This bit is set when the Renderer Instruction Parser detects an error while parsing an instruction. Instruction errors include:</p> <ul style="list-style-type: none"> <li>• Client ID value (Bits 31:29 of the Header) is not supported (only MI, 2D and 3D are supported).</li> <li>• Defeatured MI Instruction Opcodes:</li> </ul> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>1</td> <td></td> <td>Instruction Error detected</td> </tr> </tbody> </table> <p><b>Programming Notes</b></p> <p>This error indications cannot be cleared except by reset (i.e., it is a fatal error).</p>	Value	Name	Description	1		Instruction Error detected
Value	Name	Description					
1		Instruction Error detected					

## VEBOX\_ACE\_LACE\_STATE

VEBOX_ACE_LACE_STATE										
DWord	Bit	Description								
0	31:12	<b>Reserved</b> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	BDW	Format:	MBZ				
Project:	BDW									
Format:	MBZ									
	11:7	<b>Reserved</b> <table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ						
Format:	MBZ									
	6:2	<b>Skin Threshold</b> <table border="1"> <tr> <td>Format:</td><td>U5</td></tr> </table> <p>Used for Y analysis (min/max) for pixels which are higher than skin threshold.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>[1,31]</td><td></td></tr> <tr> <td>26</td><td><b>[Default]</b></td></tr> </tbody> </table>	Format:	U5	Value	Name	[1,31]		26	<b>[Default]</b>
Format:	U5									
Value	Name									
[1,31]										
26	<b>[Default]</b>									
	1	<b>Full Image Histogram</b> <table border="1"> <tr> <td>Default Value:</td><td>0</td></tr> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>Enable</td></tr> </table> <p>Used to ignore the area of interest for full image histogram. This applies to all statistics that are affected by AOI (Area of Interest).</p>	Default Value:	0	Project:	BDW	Format:	Enable		
Default Value:	0									
Project:	BDW									
Format:	Enable									
	0	<b>ACE Enable</b> <table border="1"> <tr> <td>Format:</td><td>Enable</td></tr> </table>	Format:	Enable						
Format:	Enable									
1	31:24	<b>Y3</b> <table border="1"> <tr> <td>Default Value:</td><td>76</td></tr> <tr> <td>Format:</td><td>U8</td></tr> </table> <p>The value of the y_pixel for point 3 in PWL.</p>	Default Value:	76	Format:	U8				
Default Value:	76									
Format:	U8									

## VEBOX\_ACE\_LACE\_STATE

	23:16	<p><b>Y2</b></p> <table border="1"> <tr> <td>Default Value:</td> <td>56</td> </tr> <tr> <td>Format:</td> <td>U8</td> </tr> </table> <p>The value of the y_pixel for point 2 in PWL.</p>	Default Value:	56	Format:	U8
Default Value:	56					
Format:	U8					
	15:8	<p><b>Y1</b></p> <table border="1"> <tr> <td>Default Value:</td> <td>36</td> </tr> <tr> <td>Format:</td> <td>U8</td> </tr> </table> <p>The value of the y_pixel for point 1 in PWL.</p>	Default Value:	36	Format:	U8
Default Value:	36					
Format:	U8					
	7:0	<p><b>Ymin</b></p> <table border="1"> <tr> <td>Default Value:</td> <td>16</td> </tr> <tr> <td>Format:</td> <td>U8</td> </tr> </table> <p>The value of the y_pixel for point 0 in PWL.</p>	Default Value:	16	Format:	U8
Default Value:	16					
Format:	U8					
2	31:24	<p><b>Y7</b></p> <table border="1"> <tr> <td>Default Value:</td> <td>156</td> </tr> <tr> <td>Format:</td> <td>U8</td> </tr> </table> <p>The value of the y_pixel for point 7 in PWL.</p>	Default Value:	156	Format:	U8
Default Value:	156					
Format:	U8					
	23:16	<p><b>Y6</b></p> <table border="1"> <tr> <td>Default Value:</td> <td>136</td> </tr> <tr> <td>Format:</td> <td>U8</td> </tr> </table> <p>The value of the y_pixel for point 6 in PWL.</p>	Default Value:	136	Format:	U8
Default Value:	136					
Format:	U8					
	15:8	<p><b>Y5</b></p> <table border="1"> <tr> <td>Default Value:</td> <td>116</td> </tr> <tr> <td>Format:</td> <td>U8</td> </tr> </table> <p>The value of the y_pixel for point 5 in PWL.</p>	Default Value:	116	Format:	U8
Default Value:	116					
Format:	U8					
	7:0	<p><b>Y4</b></p> <table border="1"> <tr> <td>Default Value:</td> <td>96</td> </tr> <tr> <td>Format:</td> <td>U8</td> </tr> </table> <p>The value of the y_pixel for point 4 in PWL.</p>	Default Value:	96	Format:	U8
Default Value:	96					
Format:	U8					
3	31:24	<p><b>Ymax</b></p> <table border="1"> <tr> <td>Default Value:</td> <td>235</td> </tr> <tr> <td>Format:</td> <td>U8</td> </tr> </table> <p>The value of the y_pixel for point 11 in PWL.</p>	Default Value:	235	Format:	U8
Default Value:	235					
Format:	U8					

## VEBOX ACE LACE STATE

	23:16	<b>Y10</b>
		Default Value: 216
		Format: U8
The value of the y_pixel for point 10 in PWL.		
	15:8	<b>Y9</b>
		Default Value: 196
		Format: U8
The value of the y_pixel for point 9 in PWL.		
	7:0	<b>Y8</b>
		Default Value: 176
		Format: U8
The value of the y_pixel for point 8 in PWL.		
4	31:24	<b>B4</b>
		Default Value: 96
		Format: U8
The value of the bias for point 4 in PWL.		
	23:16	<b>B3</b>
		Default Value: 76
		Format: U8
The value of the bias for point 3 in PWL.		
	15:8	<b>B2</b>
		Default Value: 56
		Format: U8
The value of the bias for point 2 in PWL.		
	7:0	<b>B1</b>
		Default Value: 36
		Format: U8
The value of the bias for point 1 in PWL.		
5	31:24	<b>B8</b>
		Default Value: 176
		Format: U8
The value of the bias for point 8 in PWL.		

## VEBOX\_ACE\_LACE\_STATE

	23:16	<b>B7</b>  Default Value: 156 Format: U8  The value of the bias for point 7 in PWL.
	15:8	<b>B6</b>  Default Value: 136 Format: U8  The value of the bias for point 6 in PWL.
	7:0	<b>B5</b>  Default Value: 116 Format: U8  The value of the bias for point 5 in PWL.
6	31:16	<b>Reserved</b>  Format: MBZ
	15:8	<b>B10</b>  Default Value: 216 Format: U8  The value of the bias for point 10 in PWL.
	7:0	<b>B9</b>  Default Value: 196 Format: U8  The value of the bias for point 9 in PWL.
7	31:27	<b>Reserved</b>  Format: MBZ
	26:16	<b>S1</b>  Default Value: 1024 Format: U1.10  The value of the slope for point 1 in PWL The default is 1024/1024
	15:11	<b>Reserved</b>  Format: MBZ

## VEBOX\_ACE\_LACE\_STATE

	10:0	<b>S0</b>
		Default Value: 1024
		Format: U1.10
The value of the slope for point 0 in PWL		
The default is 1024/1024		
8	31:27	<b>Reserved</b>
		Format: MBZ
	26:16	<b>S3</b>
		Default Value: 1024
		Format: U1.10
The value of the slope for point 3 in PWL		
The default is 1024/1024		
	15:11	<b>Reserved</b>
		Format: MBZ
	10:0	<b>S2</b>
		Default Value: 1024
		Format: U1.10
The value of the slope for point 2 in PWL		
The default is 1024/1024		
9	31:27	<b>Reserved</b>
		Format: MBZ
	26:16	<b>S5</b>
		Default Value: 1024
		Format: U1.10
The value of the slope for point 5 in PWL		
The default is 1024/1024		
	15:11	<b>Reserved</b>
		Format: MBZ

VEBOX_ACE_LACE_STATE						
	10:0	<b>S4</b>				
		<table border="1"> <tr> <td>Default Value:</td><td>1024</td></tr> <tr> <td>Format:</td><td>U1.10</td></tr> </table>	Default Value:	1024	Format:	U1.10
Default Value:	1024					
Format:	U1.10					
		The value of the slope for point 4 in PWL				
		The default is 1024/1024				
10	31:27	<b>Reserved</b>				
		<table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ		
Format:	MBZ					
	26:16	<b>S7</b>				
		<table border="1"> <tr> <td>Default Value:</td><td>1024</td></tr> <tr> <td>Format:</td><td>U1.10</td></tr> </table>	Default Value:	1024	Format:	U1.10
Default Value:	1024					
Format:	U1.10					
		The value of the slope for point 7 in PWL				
		The default is 1024/1024				
	15:11	<b>Reserved</b>				
		<table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ		
Format:	MBZ					
	10:0	<b>S6</b>				
		<table border="1"> <tr> <td>Default Value:</td><td>1024</td></tr> <tr> <td>Format:</td><td>U1.10</td></tr> </table>	Default Value:	1024	Format:	U1.10
Default Value:	1024					
Format:	U1.10					
		The default is 1024/1024				
11	31:27	<b>Reserved</b>				
		<table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ		
Format:	MBZ					
	26:16	<b>S9</b>				
		<table border="1"> <tr> <td>Default Value:</td><td>1024</td></tr> <tr> <td>Format:</td><td>U1.10</td></tr> </table>	Default Value:	1024	Format:	U1.10
Default Value:	1024					
Format:	U1.10					
		The value of the slope for point 9 in PWL				
		The default is 1024/1024				
	15:11	<b>Reserved</b>				
		<table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ		
Format:	MBZ					

VEBOX_ACE_LACE_STATE						
	10:0	<b>S8</b>				
		<table border="1"> <tr> <td>Default Value:</td><td>1024</td></tr> <tr> <td>Format:</td><td>U1.10</td></tr> </table>	Default Value:	1024	Format:	U1.10
Default Value:	1024					
Format:	U1.10					
		The value of the slope for point 8 in PWL				
		The default is 1024/1024				
12	31:16	<b>Reserved</b>				
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	BDW	Format:	MBZ
Project:	BDW					
Format:	MBZ					
	15:11	<b>Reserved</b>				
		<table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ		
Format:	MBZ					
	10:0	<b>S10</b>				
		<table border="1"> <tr> <td>Default Value:</td><td>1024</td></tr> <tr> <td>Format:</td><td>U1.10</td></tr> </table>	Default Value:	1024	Format:	U1.10
Default Value:	1024					
Format:	U1.10					
		The value of the slope for point 10 in PWL.				

## VEBOX\_ALPHA\_AOI\_STATE

VEBOX_ALPHA_AOI_STATE									
DWord	Bit	Description							
0	31:17	<p><b>Reserved</b></p> <table> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ					
Format:	MBZ								
16	<p><b>Alpha from State Select</b></p> <table> <tr> <td>Format:</td> <td>U1 Enumerated type</td> </tr> </table> <table> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>alpha is taken from message</td> </tr> <tr> <td>1</td> <td>alpha is taken from state</td> </tr> </tbody> </table>	Format:	U1 Enumerated type	Value	Name	0	alpha is taken from message	1	alpha is taken from state
Format:	U1 Enumerated type								
Value	Name								
0	alpha is taken from message								
1	alpha is taken from state								
<b>Programming Notes</b>									
If the input format does not have alpha available and the output format provides alpha, this bit should be set to 1. This should be 0 when Alpha Plane Enable is 1.									
15:12	<p><b>Reserved</b></p> <table> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ						
Format:	MBZ								
11:0	<p><b>Color Pipe Alpha</b></p> <table> <tr> <td>Format:</td> <td>U12</td> </tr> </table>	Format:	U12						
Format:	U12								
31:30	<p><b>Reserved</b></p> <table> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ						
Format:	MBZ								
29:16	<p><b>AOI Max X</b></p> <table> <tr> <td>Default Value:</td> <td>3</td> </tr> <tr> <td>Format:</td> <td>U14</td> </tr> </table>	Default Value:	3	Format:	U14				
Default Value:	3								
Format:	U14								
<b>Description</b>									
Area of Interest Minimum X - The ACE histogram and Skin Tone Detection statistic gathering will occur within the MinX/MinY to MaxX/MaxY area (inclusive). This value must be a multiple of 4 minus 1.									
The Area of Interest applies to the RGB Histogram and the White/Gray point sums as well.									
15:14	<p><b>Reserved</b></p> <table> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ						
Format:	MBZ								

<b>VEBOX_ALPHA_AOI_STATE</b>				
	13:0	<b>AOI Min X</b>		
		Default Value:	0	
		Format:	U14	
		This value must be a multiple of 4.		
2	31:30	<b>Reserved</b>		
		Format:	MBZ	
	29:16	<b>AOI Max Y</b>		
		Default Value:	3	
		Format:	U14	
		This value must be a multiple of 4 minus 1.		
	15:14	<b>Reserved</b>		
		Format:	MBZ	
	13:0	<b>AOI Min Y</b>		
		Default Value:	0	
		Format:	U14	
		This value must be a multiple of 4.		

## VEBOX\_CAPTURE\_PIPE\_STATE

VEBOX_CAPTURE_PIPE_STATE								
DWord	Bit	Description						
0	31:30	<b>Reserved</b> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	BDW	Format:	MBZ		
Project:	BDW							
Format:	MBZ							
	29:24	<b>Good Pixel Threshold</b> <table border="1"> <tr> <td>Format:</td><td>U6</td></tr> </table> <p>The difference threshold between adjacent pixels for a pixel to be considered "good".</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>Fh</td><td>[Default]</td></tr> </tbody> </table>	Format:	U6	Value	Name	Fh	[Default]
Format:	U6							
Value	Name							
Fh	[Default]							
	23	<b>Reserved</b> <table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ				
Format:	MBZ							
	22:20	<b>Shift Min Cost</b> <table border="1"> <tr> <td>Default Value:</td><td>1h</td></tr> <tr> <td>Format:</td><td>U3</td></tr> </table> <p>The amount to shift the H2/V2 versions of min_cost.</p>	Default Value:	1h	Format:	U3		
Default Value:	1h							
Format:	U3							
	19:16	<b>Scale For Average Min Cost</b> <table border="1"> <tr> <td>Default Value:</td><td>2h</td></tr> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>U4</td></tr> </table> <p>The amount to scale the min_cost difference during the Avg interpolation decision</p>	Default Value:	2h	Project:	BDW	Format:	U4
Default Value:	2h							
Project:	BDW							
Format:	U4							
	15:8	<b>Average Color Threshold</b> <table border="1"> <tr> <td>Format:</td><td>U8</td></tr> </table> <p>The threshold between two colors in a pixel for the Avg interpolation to be considered.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>64h</td><td>[Default]</td></tr> </tbody> </table>	Format:	U8	Value	Name	64h	[Default]
Format:	U8							
Value	Name							
64h	[Default]							

<b>VEBOX_CAPTURE_PIPE_STATE</b>			
	7:0	<b>Average Min Cost Threshold</b>	
		Default Value:	4Bh
		Project:	BDW
		Format:	U8
The threshold for the H and V Min_cost beyond which the Avg interpolation will be used.			
1	31:28	<b>Scale For Min Cost</b>	
		Default Value:	Ah
		The amount to scale the min_cost difference during the confidence check.	
	27:24	<b>Reserved</b>	
		Project:	BDW
		Format:	MBZ
	23:16	<b>Bad Color Threshold 1</b>	
		Default Value:	64h
		Format:	U8
		Color value threshold used during the bad pixel check.	
	15:8	<b>Bad Color Threshold 2</b>	
		Default Value:	AFh
		Format:	U8
		Color value threshold used during the bad pixel check.	
	7:4	<b>Reserved</b>	
		Project:	BDW
		Format:	MBZ
	3:0	<b>Bad Color Threshold 3</b>	
		Default Value:	Ah
		Format:	U4
		Color value threshold used during the bad pixel check.	
2	31:24	<b>Y Bright Value</b>	
		Default Value:	E6h
		The whitepoint threshold percentile in the Y histogram. Any pixel with Y value above this could be a whitepoint. This is the larger of the calculated Ybright value and the Ythreshold value, which is the minimum Y required to be considered a white point.	
		<b>Programming Notes</b>	
		"0000" is appended to the LSBs before comparing with Y.	

VEBOX_CAPTURE_PIPE_STATE											
	23:16	<p><b>Y Outlier Value</b></p> <table border="1"> <tr> <td>Default Value:</td><td>FDh</td></tr> </table> <p>The outlier threshold percentile in the Y histogram. Any pixel with Y value above this either clipped or an outlier in the image. These points will not be included in the white patch calculation.</p>	Default Value:	FDh							
Default Value:	FDh										
		<p style="text-align: center;"><b>Programming Notes</b></p> <p>"0000" is appended to the LSBs before comparing with Y.</p>									
	15:8	<p><b>UV Threshold Value</b></p> <p>The value denotes the maximum threshold of the ratio between U+V to Y can have to be considered a gray point.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>[255,0]</td><td></td><td>Encode a value from 255/256 to 0/256</td></tr> <tr> <td>64</td><td><b>[Default]</b></td><td><math>0.25 * 255 = 64</math></td></tr> </tbody> </table>	Value	Name	Description	[255,0]		Encode a value from 255/256 to 0/256	64	<b>[Default]</b>	$0.25 * 255 = 64$
Value	Name	Description									
[255,0]		Encode a value from 255/256 to 0/256									
64	<b>[Default]</b>	$0.25 * 255 = 64$									
	7:0	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	BDW	Format:	MBZ					
Project:	BDW										
Format:	MBZ										

## VEBOX\_CCM\_STATE

VEBOX_CCM_STATE								
DWord	Bit	Description						
0	31	<p><b>Color Correction Matrix Enable</b></p> <table border="1"> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>This bit enables the Color Correction Matrix, but not the Black Level Correction subtract, which is enabled whenever Demosaic is enabled. Demosaic must also be enabled if this is enabled.</p>	Format:	Enable				
Format:	Enable							
30	<p><b>Vignette Correction Format</b></p> <table border="1"> <tr> <td>Defines what shift should be assumed for the Vignette.</td> </tr> </table> <p>Correction input values:</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>U8.8</td> </tr> <tr> <td>1</td> <td>U4.12</td> </tr> </tbody> </table>	Defines what shift should be assumed for the Vignette.	Value	Name	0	U8.8	1	U4.12
Defines what shift should be assumed for the Vignette.								
Value	Name							
0	U8.8							
1	U4.12							
29:21	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ					
Format:	MBZ							
20:0	<p><b>C1: Coefficient of 3x3 Transform matrix</b></p> <table border="1"> <tr> <td>Default Value:</td> <td>000475h = 1141/4096</td> </tr> </table> <table border="1"> <tr> <td>Format:</td> <td>S8.12</td> </tr> </table>	Default Value:	000475h = 1141/4096	Format:	S8.12			
Default Value:	000475h = 1141/4096							
Format:	S8.12							
1	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ					
Format:	MBZ							
20:0	<p><b>C0: Coefficient of 3x3 Transform matrix</b></p> <table border="1"> <tr> <td>Default Value:</td> <td>000AE8h = 2792/4096</td> </tr> </table> <table border="1"> <tr> <td>Format:</td> <td>S8.12</td> </tr> </table>	Default Value:	000AE8h = 2792/4096	Format:	S8.12			
Default Value:	000AE8h = 2792/4096							
Format:	S8.12							
31:21	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ					
Format:	MBZ							
20:0	<p><b>C3: Coefficient of 3x3 Transform matrix</b></p> <table border="1"> <tr> <td>Default Value:</td> <td>000047h = 71/4096</td> </tr> </table> <table border="1"> <tr> <td>Format:</td> <td>S8.12</td> </tr> </table>	Default Value:	000047h = 71/4096	Format:	S8.12			
Default Value:	000047h = 71/4096							
Format:	S8.12							
31:21	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ					
Format:	MBZ							

VEBOX_CCM_STATE			
3	31:21	<b>Reserved</b>	
	Format:		MBZ
4	20:0	<b>C2: Coefficient of 3x3 Transform matrix</b>	
	Default Value:	000022h = 34/4096	
5	31:21	<b>Reserved</b>	
	Format:		MBZ
6	20:0	<b>C5: Coefficient of 3x3 Transform matrix</b>	
	Default Value:	1FFFCCh = -52/4096	
7	31:21	<b>Reserved</b>	
	Format:		MBZ
8	20:0	<b>C4: Coefficient of 3x3 Transform matrix</b>	
	Default Value:	000D23h = 3363/4096	
6	31:21	<b>Reserved</b>	
	Format:		MBZ
7	20:0	<b>C7: Coefficient of 3x3 Transform matrix</b>	
	Default Value:	0000A8h 168/4096	
7	31:21	<b>Reserved</b>	
	Format:		MBZ
8	20:0	<b>C6: Coefficient of 3x3 Transform matrix</b>	
	Default Value:	1FFFF4h = -12/4096	
8	31:21	<b>Reserved</b>	
	Format:		MBZ
8	20:0	<b>C8: Coefficient of 3x3 Transform matrix</b>	
	Default Value:	000D6Ah = 3434/4096	
8	31:21	<b>Reserved</b>	
	Format:		S8.12

## VEBOX\_Ch\_Dir\_Filter\_Coefficient

VEBOX_Ch_Dir_Filter_Coefficient						
DWord	Bit	Description				
0..1	63:56	<b>Filter Coefficient[7]</b> <table border="1"> <tr> <td>Format:</td> <td>S1.6 2's Complement</td> </tr> <tr> <td><b>Range:</b></td> <td>[-2, +2)</td> </tr> </table>	Format:	S1.6 2's Complement	<b>Range:</b>	[-2, +2)
Format:	S1.6 2's Complement					
<b>Range:</b>	[-2, +2)					
55:48	<b>Filter Coefficient[6]</b> <table border="1"> <tr> <td>Format:</td> <td>S1.6 2's Complement</td> </tr> <tr> <td><b>Range:</b></td> <td>[-2, +2)</td> </tr> </table>	Format:	S1.6 2's Complement	<b>Range:</b>	[-2, +2)	
Format:	S1.6 2's Complement					
<b>Range:</b>	[-2, +2)					
47:40	<b>Filter Coefficient[5]</b> <table border="1"> <tr> <td>Format:</td> <td>S1.6 2's Complement</td> </tr> <tr> <td><b>Range:</b></td> <td>[-2, +2)</td> </tr> </table>	Format:	S1.6 2's Complement	<b>Range:</b>	[-2, +2)	
Format:	S1.6 2's Complement					
<b>Range:</b>	[-2, +2)					
39:32	<b>Filter Coefficient[4]</b> <table border="1"> <tr> <td>Format:</td> <td>S1.6 2's Complement</td> </tr> <tr> <td><b>Range:</b></td> <td>[-2, +2)</td> </tr> </table>	Format:	S1.6 2's Complement	<b>Range:</b>	[-2, +2)	
Format:	S1.6 2's Complement					
<b>Range:</b>	[-2, +2)					
31:24	<b>Filter Coefficient[3]</b> <table border="1"> <tr> <td>Format:</td> <td>S1.6 2's Complement</td> </tr> <tr> <td><b>Range:</b></td> <td>[-2, +2)</td> </tr> </table>	Format:	S1.6 2's Complement	<b>Range:</b>	[-2, +2)	
Format:	S1.6 2's Complement					
<b>Range:</b>	[-2, +2)					
23:16	<b>Filter Coefficient[2]</b> <table border="1"> <tr> <td>Format:</td> <td>S1.6 2's Complement</td> </tr> <tr> <td><b>Range:</b></td> <td>[-2, +2)</td> </tr> </table>	Format:	S1.6 2's Complement	<b>Range:</b>	[-2, +2)	
Format:	S1.6 2's Complement					
<b>Range:</b>	[-2, +2)					
15:8	<b>Filter Coefficient[1]</b> <table border="1"> <tr> <td>Format:</td> <td>S1.6 2's Complement</td> </tr> <tr> <td><b>Range:</b></td> <td>[-2, +2)</td> </tr> </table>	Format:	S1.6 2's Complement	<b>Range:</b>	[-2, +2)	
Format:	S1.6 2's Complement					
<b>Range:</b>	[-2, +2)					
7:0	<b>Filter Coefficient[0]</b> <table border="1"> <tr> <td>Format:</td> <td>S1.6 2's Complement</td> </tr> <tr> <td><b>Range:</b></td> <td>[-2, +2)</td> </tr> </table>	Format:	S1.6 2's Complement	<b>Range:</b>	[-2, +2)	
Format:	S1.6 2's Complement					
<b>Range:</b>	[-2, +2)					

## VEBOX\_CSC\_STATE

VEBOX_CSC_STATE		
DWord	Bit	Description
0	31:29	<b>Reserved</b>
		Format: MBZ
	28:16	<b>C1</b>
		Default Value: 0
		Format: S2.10 2's complement
Transform coefficient.		
	15:3	<b>C0</b>
		Default Value: 1024
		Format: S2.10 2's complement
Transform coefficient.		
	2	<b>Reserved</b>
		Format: MBZ

## VEBOX\_CSC\_STATE

		<b>YUV_Channel_Swap</b>																			
	1	<table border="1" style="width: 100%;"> <tr> <td>Default Value:</td><td style="text-align: right;">0</td></tr> <tr> <td>Format:</td><td style="text-align: right;">Enable</td></tr> </table> <p>This bit should only be used with RGB output formats. When this bit is set, the YUV channels are swapped into the output RGB channels as shown in the following table:</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th></th><th colspan="2">YUV_Channel_Swap</th></tr> <tr> <th></th><th>0</th><th>1</th></tr> </thead> <tbody> <tr> <td>Y</td><td>R</td><td>G</td></tr> <tr> <td>U</td><td>G</td><td>B</td></tr> <tr> <td>V</td><td>B</td><td>R</td></tr> </tbody> </table>	Default Value:	0	Format:	Enable		YUV_Channel_Swap			0	1	Y	R	G	U	G	B	V	B	R
Default Value:	0																				
Format:	Enable																				
	YUV_Channel_Swap																				
	0	1																			
Y	R	G																			
U	G	B																			
V	B	R																			
		<b>Programming Notes</b>																			
		<p>The yuv_in and yuv_out state variables is used to offset the YUV values by <math>\frac{1}{2}</math> of their range before (for yuv_in) and after (for yuv_out) color space conversion; in addition yuv_out swapped the YUV channels. The per channel Offset in and Offset out state variables in combination with the YUV_Channel_Swap bit.</p>																			
	0	<b>Transform Enable</b>																			
		<table border="1" style="width: 100%;"> <tr> <td>Format:</td><td style="text-align: right;">Enable</td></tr> </table>	Format:	Enable																	
Format:	Enable																				
1	31:26	<b>Reserved</b>																			
		<table border="1" style="width: 100%;"> <tr> <td>Format:</td><td style="text-align: right;">MBZ</td></tr> </table>	Format:	MBZ																	
Format:	MBZ																				
	25:13	<b>C3</b>																			
		<table border="1" style="width: 100%;"> <tr> <td>Default Value:</td><td style="text-align: right;">0</td></tr> <tr> <td>Format:</td><td style="text-align: right;">S2.10 2's complement</td></tr> </table> <p>Transform coefficient.</p>	Default Value:	0	Format:	S2.10 2's complement															
Default Value:	0																				
Format:	S2.10 2's complement																				
	12:0	<b>C2</b>																			
		<table border="1" style="width: 100%;"> <tr> <td>Default Value:</td><td style="text-align: right;">0</td></tr> <tr> <td>Format:</td><td style="text-align: right;">S2.10 2's complement</td></tr> </table> <p>Transform coefficient.</p>	Default Value:	0	Format:	S2.10 2's complement															
Default Value:	0																				
Format:	S2.10 2's complement																				
2	31:26	<b>Reserved</b>																			
		<table border="1" style="width: 100%;"> <tr> <td>Format:</td><td style="text-align: right;">MBZ</td></tr> </table>	Format:	MBZ																	
Format:	MBZ																				
	25:13	<b>C5</b>																			
		<table border="1" style="width: 100%;"> <tr> <td>Default Value:</td><td style="text-align: right;">0</td></tr> <tr> <td>Format:</td><td style="text-align: right;">S2.10 2's complement</td></tr> </table> <p>Transform coefficient.</p>	Default Value:	0	Format:	S2.10 2's complement															
Default Value:	0																				
Format:	S2.10 2's complement																				

VEBOX_CSC_STATE			
	12:0	<b>C4</b>	
		Default Value:	1024
		Format:	S2.10 2's complement
		Transform coefficient.	
3	31:26	<b>Reserved</b>	
		Format:	MBZ
	25:13	<b>C7</b>	
		Default Value:	0
		Format:	S2.10 2's complement
		Transform coefficient.	
	12:0	<b>C6</b>	
		Default Value:	0
		Format:	S2.10 2's complement
		Transform coefficient.	
4	31:13	<b>Reserved</b>	
		Format:	MBZ
	12:0	<b>C8</b>	
		Default Value:	1024
		Format:	S2.10 2's complement
		Transform coefficient.	
5	31:22	<b>Reserved</b>	
		Format:	MBZ
	21:11	<b>Offset Out 1</b>	
		Default Value:	0
		Format:	S10 2's complement
		Offset out for Y/R.	
	10:0	<b>Offset in 1</b>	
		Default Value:	0
		Format:	S10 2's complement
		Offset in for Y/R.	
6	31:22	<b>Reserved</b>	
		Format:	MBZ

## VEBOX\_CSC\_STATE

		<b>VEBOX_CSC_STATE</b>				
	21:11	<b>Offset out 2</b>				
		<table border="1"> <tr> <td>Default Value:</td><td>0</td></tr> <tr> <td>Format:</td><td>S10 2's complement</td></tr> </table> <p>Offset out for U/G.</p>	Default Value:	0	Format:	S10 2's complement
Default Value:	0					
Format:	S10 2's complement					
	10:0	<b>Offset in 2</b>				
		<table border="1"> <tr> <td>Default Value:</td><td>0</td></tr> <tr> <td>Format:</td><td>S10 2's complement</td></tr> </table> <p>Offset in for U/G.</p>	Default Value:	0	Format:	S10 2's complement
Default Value:	0					
Format:	S10 2's complement					
7	31:22	<b>Reserved</b>				
		<table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ		
Format:	MBZ					
	21:11	<b>Offset out 3</b>				
		<table border="1"> <tr> <td>Default Value:</td><td>0</td></tr> <tr> <td>Format:</td><td>S10 2's complement</td></tr> </table> <p>Offset out for V/B.</p>	Default Value:	0	Format:	S10 2's complement
Default Value:	0					
Format:	S10 2's complement					
	10:0	<b>Offset in 3</b>				
		<table border="1"> <tr> <td>Default Value:</td><td>0</td></tr> <tr> <td>Format:</td><td>S10 2's complement</td></tr> </table> <p>Offset in for V/B.</p>	Default Value:	0	Format:	S10 2's complement
Default Value:	0					
Format:	S10 2's complement					

## **VEBOX\_DNDI\_STATE**

<b>VEBOX_DNDI_STATE</b>									
<b>DWord</b>	<b>Bit</b>	<b>Description</b>							
0	31:24	<p><b>Denoise STAD Threshold</b></p> <table border="1"> <tr> <td>Format:</td> <td>U8</td> </tr> <tr> <td colspan="2">Threshold for denoise sum of temporal absolute differences.</td></tr> </table>	Format:	U8	Threshold for denoise sum of temporal absolute differences.				
Format:	U8								
Threshold for denoise sum of temporal absolute differences.									
23:16	<p><b>Denoise Maximum History</b></p> <table border="1"> <tr> <td>Format:</td> <td>U8</td> </tr> <tr> <td colspan="2">Maximum allowed value for denoise history.</td></tr> <tr> <th>Value</th><th>Name</th></tr> <tr> <td>[128,240]</td><td></td></tr> </table>	Format:	U8	Maximum allowed value for denoise history.		Value	Name	[128,240]	
Format:	U8								
Maximum allowed value for denoise history.									
Value	Name								
[128,240]									
15:12	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ						
Format:	MBZ								
11:8	<p><b>Denoise History increase</b></p> <table border="1"> <tr> <td>Default Value:</td> <td>8h</td> </tr> <tr> <td>Format:</td> <td>U4</td> </tr> <tr> <td colspan="2">Amount that denoise_history is increased MAX:15</td></tr> </table>	Default Value:	8h	Format:	U4	Amount that denoise_history is increased MAX:15			
Default Value:	8h								
Format:	U4								
Amount that denoise_history is increased MAX:15									
7:0	<p><b>Denoise ASD Threshold</b></p> <table border="1"> <tr> <td>Format:</td> <td>U8</td> </tr> <tr> <td colspan="2">Threshold for denoise absolute sum of differences.</td></tr> <tr> <th>Value</th><th>Name</th></tr> <tr> <td>[0,63]</td><td></td></tr> </table>	Format:	U8	Threshold for denoise absolute sum of differences.		Value	Name	[0,63]	
Format:	U8								
Threshold for denoise absolute sum of differences.									
Value	Name								
[0,63]									
1	31:30	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ					
Format:	MBZ								

<b>VEBOX_DNDI_STATE</b>									
	29:24	<b>Temporal Difference Threshold</b>							
<table border="1"> <tr> <td>Format:</td><td>U6</td></tr> </table>				Format:	U6				
Format:	U6								
<b>Programming Notes</b>									
<b>Temporal Difference Threshold minus Low Temporal Difference Threshold</b> must be larger than 0 and less than or equal to 16, except when both thresholds are set to 0.									
	23:22	<b>Reserved</b>							
<table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>				Format:	MBZ				
Format:	MBZ								
	21:16	<b>Low Temporal Difference Threshold</b>							
<table border="1"> <tr> <td>Format:</td><td>U6</td></tr> </table>				Format:	U6				
Format:	U6								
<b>Programming Notes</b>									
<b>Temporal Difference Threshold minus Low Temporal Difference Threshold</b> must be larger than 0 and less than or equal to 16, except when both thresholds are set to 0.									
	15:13	<b>STMM C2</b>							
<table border="1"> <tr> <td>Format:</td><td>U3</td></tr> </table>				Format:	U3				
Format:	U3								
Bias for divisor in STMM equation.									
<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>[0,7]</td><td></td><td>Representing values [1,8]</td></tr> </tbody> </table>				Value	Name	Description	[0,7]		Representing values [1,8]
Value	Name	Description							
[0,7]		Representing values [1,8]							
	12:8	<b>Denoise Moving Pixel Threshold</b>							
<table border="1"> <tr> <td>Format:</td><td>U5</td></tr> </table>				Format:	U5				
Format:	U5								
Threshold for number of moving pixels to declare a block to be moving.									
<table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>[0,16]</td><td></td></tr> </tbody> </table>				Value	Name	[0,16]			
Value	Name								
[0,16]									
	7:0	<b>Denoise Threshold for Sum of Complexity Measure</b>							
<table border="1"> <tr> <td>Format:</td><td>U8</td></tr> </table>				Format:	U8				
Format:	U8								
2	31:30	<b>Reserved</b>							
<table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>				Format:	MBZ				
Format:	MBZ								
	29:24	<b>Good Neighbor Threshold</b>							
<table border="1"> <tr> <td>Format:</td><td>U6</td></tr> </table>				Format:	U6				
Format:	U6								
Difference from current pixel for neighboring pixels to be considered a good neighbor.									
MAX:63									
<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>4</td><td>[Default]</td><td>Depending on GNE of previous frame</td></tr> </tbody> </table>				Value	Name	Description	4	[Default]	Depending on GNE of previous frame
Value	Name	Description							
4	[Default]	Depending on GNE of previous frame							

VEBOX_DNDI_STATE									
	23:20	<b>Content Adaptive Threshold Slope</b>							
		Format:	U4						
		Determines the slope of the Content Adaptive Threshold. +1 added internally to get CAT_slope.							
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>9</td><td>[Default]</td><td>CAT_slope value = 10</td></tr> </tbody> </table>	Value	Name	Description	9	[Default]	CAT_slope value = 10	
Value	Name	Description							
9	[Default]	CAT_slope value = 10							
	19:16	<b>SAD Tight Threshold</b>							
		Default Value:	5						
		Format:	U4						
	15:14	<b>Smooth MV Threshold</b>							
		Format:	U2						
	13:12	<b>Reserved</b>							
		Format:	MBZ						
	11:8	<b>Block Noise Estimate Edge Threshold</b>							
		Default Value:	1						
		Format:	U4						
		Threshold for detecting an edge in block noise estimate. MAX:15							
	7:0	<b>Block Noise Estimate Noise Threshold</b>							
		Format:	U8						
		Threshold for noise maximum/minimum.							
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>[0,31]</td><td></td></tr> </tbody> </table>	Value	Name	[0,31]				
Value	Name								
[0,31]									
3	31	<b>STMM Blending Constant Select</b>							
3		Format:	U1						
3		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0</td><td>Use the blending constant for small values of STMM for stmm_md_th</td></tr> <tr> <td>1</td><td>Use the blending constant for large values of STMM for stmm_md_th</td></tr> </tbody> </table>	Value	Name	0	Use the blending constant for small values of STMM for stmm_md_th	1	Use the blending constant for large values of STMM for stmm_md_th	
Value	Name								
0	Use the blending constant for small values of STMM for stmm_md_th								
1	Use the blending constant for large values of STMM for stmm_md_th								
3	30:24	<b>Blending constant across time for large values of STMM</b>							
3		Default Value:	64						
3		Format:	U7						
3	23:16	<b>Blending constant across time for small values of STMM</b>							
3		Default Value:	125						
3		Format:	U8						
3	15:14	<b>Reserved</b>							
3		Format:	MBZ						

<b>VEBOX_DNDI_STATE</b>												
	13:8	<b>Multiplier for VECM</b> Format: U6 Determines the strength of the vertical edge complexity measure.										
	7:0	<b>Maximum STMM</b> Format: U8 Largest allowed STMM in blending equations										
4	31:24	<b>Minimum STMM</b> Format: U8 Smallest allowed STMM in blending equations										
	23:22	<b>STMM Shift Down</b> Format: U2 Amount to shift STMM down (quantize to fewer bits) <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr><td>0</td><td>Shift by 4</td></tr> <tr><td>1</td><td>Shift by 5</td></tr> <tr><td>2</td><td>Shift by 6</td></tr> <tr><td>3</td><td>Reserved</td></tr> </tbody> </table>	Value	Name	0	Shift by 4	1	Shift by 5	2	Shift by 6	3	Reserved
Value	Name											
0	Shift by 4											
1	Shift by 5											
2	Shift by 6											
3	Reserved											
	21:20	<b>STMM Shift Up</b> Format: U2 Amount to shift STMM up (set range). <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr><td>0</td><td>Shift by 6</td></tr> <tr><td>1</td><td>Shift by 7</td></tr> <tr><td>2</td><td>Shift by 8</td></tr> <tr><td>3</td><td>Reserved</td></tr> </tbody> </table>	Value	Name	0	Shift by 6	1	Shift by 7	2	Shift by 8	3	Reserved
Value	Name											
0	Shift by 6											
1	Shift by 7											
2	Shift by 8											
3	Reserved											
	19:16	<b>STMM Output Shift</b> Format: U4 Amount to shift output of STMM blend equation <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr><td>[0, 16]</td><td></td></tr> </tbody> </table> <b>Programming Notes</b> The value of this field must satisfy the following equation: stmm_max - stmm_min = 2 ^ stmm_output_shift	Value	Name	[0, 16]							
Value	Name											
[0, 16]												

VEBOX_DNDI_STATE											
	15:8	<b>SDI Threshold</b>	<table border="1"> <tr> <td>Format:</td><td>U8</td></tr> </table> <p>Threshold for angle detection in SDI algorithm.</p>	Format:	U8						
Format:	U8										
	7:0	<b>SDI Delta</b>	<table border="1"> <tr> <td>Format:</td><td>U8</td></tr> </table> <p>Delta value for angle detection in SDI algorithm.</p>	Format:	U8						
Format:	U8										
5	31:24	<b>SDI Fallback Mode 1 T1 Constant</b>	<table border="1"> <tr> <td>Format:</td><td>U8</td></tr> </table>	Format:	U8						
Format:	U8										
	23:16	<b>SDI Fallback Mode 1 T2 Constant</b>	<table border="1"> <tr> <td>Format:</td><td>U8</td></tr> </table>	Format:	U8						
Format:	U8										
	15:8	<b>SDI Fallback Mode 2 Constant (Angle2x1)</b>	<table border="1"> <tr> <td>Format:</td><td>U8</td></tr> </table>	Format:	U8						
Format:	U8										
	7:0	<b>FMD Temporal Difference Threshold</b>	<table border="1"> <tr> <td>Format:</td><td>U8</td></tr> </table>	Format:	U8						
Format:	U8										
6	31:24	<b>FMD #1 Vertical Difference Threshold</b>	<table border="1"> <tr> <td>Format:</td><td>U8</td></tr> </table>	Format:	U8						
Format:	U8										
	23:16	<b>FMD #2 Vertical Difference Threshold</b>	<table border="1"> <tr> <td>Format:</td><td>U8</td></tr> </table>	Format:	U8						
Format:	U8										
	15:14	<b>CAT Threshold</b>	<table border="1"> <tr> <td>Default Value:</td><td>0</td></tr> <tr> <td>Format:</td><td>U2</td></tr> </table>	Default Value:	0	Format:	U2				
Default Value:	0										
Format:	U2										
	13:8	<b>FMD Tear Threshold</b>	<table border="1"> <tr> <td>Format:</td><td>U6</td></tr> </table>	Format:	U6						
Format:	U6										
	7	<b>MCDI Enable</b>	<p>Use Motion Compensated Deinterlace algorithm.</p> <table border="1"> <tr> <td align="center"><b>Programming Notes</b></td></tr> </table> <p>This bit is Ignored if DI Enable is off.</p>	<b>Programming Notes</b>							
<b>Programming Notes</b>											
	6	<b>Progressive DN</b>	<table border="1"> <tr> <td>Format:</td><td>Enable</td></tr> </table> <p>Indicates that the denoise algorithm should assume progressive input when filtering neighboring pixels. <b>DI Enable</b> must be disabled when this field is enabled</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0</td><td>DN assumes interlaced video and filters alternate lines together</td></tr> <tr> <td>1</td><td>DN assumes progressive video and filters neighboring lines together</td></tr> </tbody> </table>	Format:	Enable	Value	Name	0	DN assumes interlaced video and filters alternate lines together	1	DN assumes progressive video and filters neighboring lines together
Format:	Enable										
Value	Name										
0	DN assumes interlaced video and filters alternate lines together										
1	DN assumes progressive video and filters neighboring lines together										

<b>VEBOX_DNDI_STATE</b>				
	5:4	<b>Reserved</b>		
		Format:	MBZ	
	3	<b>DN/DI Top First</b>		
		Format:	Enable	
		Indicates the top field is first in sequence, otherwise bottom is first		
		<b>Value</b>	<b>Name</b>	
		0	Bottom field occurs first in sequence	
		1	Top field occurs first in sequence	
	2:0	<b>Reserved</b>		
		Format:	MBZ	
7	31:29	<b>Reserved</b>		
		Format:	MBZ	
	28:23	<b>Initial Denoise History</b>		
		Default Value:	32	
		Format:	U6	
		Initial value for Denoise history for both Luma and Chroma.		
		(Dnmh_history_init * 4) <= (Dnmh_history_max)		
	22:19	<b>Neighbor Pixel Threshold</b>		
		Default Value:	10	
		Format:	U4	
	18	<b>Reserved</b>		
		Format:	MBZ	
	17:16	<b>Progressive Cadence Reconstruction For 2nd Field Of Previous Frame</b>		
		Format:	U2	
		<b>Value</b>	<b>Name</b>	<b>Description</b>
		0	Deinterlace	
		1	Put together with previous field in sequence	1st field of previous frame
		2	Put together with next field in sequence	1st field of current frame
	15:10	<b>MC Pixel Consistency Threshold</b>		
		Default Value:	25	
		Format:	U6	

VEBOX_DNDI_STATE																																						
	9:8	<b>Progressive Cadence Reconstruction for 1st Field of Current Frame</b>																																				
		<table border="1"> <tr> <td>Format:</td><td colspan="2">U2</td></tr> </table>			Format:	U2																																
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		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0</td><td>Deinterlace</td><td></td></tr> <tr> <td>1</td><td>Put together with previous field in sequence</td><td>2nd field of previous frame</td></tr> <tr> <td>2</td><td>Put together with next field in sequence</td><td>2nd field of current frame</td></tr> </tbody> </table>		Value	Name	Description	0	Deinterlace		1	Put together with previous field in sequence	2nd field of previous frame	2	Put together with next field in sequence	2nd field of current frame																							
Value	Name	Description																																				
0	Deinterlace																																					
1	Put together with previous field in sequence	2nd field of previous frame																																				
2	Put together with next field in sequence	2nd field of current frame																																				
	7:4	<b>SAD THB</b>																																				
		<table border="1"> <tr> <td>Default Value:</td><td colspan="2">10</td></tr> <tr> <td>Format:</td><td colspan="2">U4</td></tr> </table>			Default Value:	10		Format:	U4																													
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Format:	U4																																					
	3:0	<b>SAD THA</b>																																				
		<table border="1"> <tr> <td>Default Value:</td><td colspan="2">5</td></tr> <tr> <td>Format:</td><td colspan="2">U4</td></tr> </table>			Default Value:	5		Format:	U4																													
Default Value:	5																																					
Format:	U4																																					
8	31:24	<b>Reserved</b>																																				
		<table border="1"> <tr> <td>Format:</td><td colspan="2">MBZ</td></tr> </table>			Format:	MBZ																																
Format:	MBZ																																					
	23:16	<b>Chroma Denoise STAD Threshold</b>																																				
		<table border="1"> <tr> <td>Format:</td><td colspan="2" rowspan="2">U8</td></tr> <tr> <td colspan="4">Threshold for denoise sum of temporal absolute differences.</td></tr> </table>			Format:	U8		Threshold for denoise sum of temporal absolute differences.																														
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	15:13	<b>Reserved</b>																																				
		<table border="1"> <tr> <td>Format:</td><td colspan="2">MBZ</td></tr> </table>			Format:	MBZ																																
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	12	<b>Chroma Denoise Enable</b>																																				
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th></th></tr> </thead> <tbody> <tr> <td>1</td><td>The U and V chroma channels will be denoise filtered.</td><td></td></tr> <tr> <td>0</td><td>The U and V channels will be passed to the next stage after DN unchanged.</td><td></td></tr> </tbody> </table>			Value	Name		1	The U and V chroma channels will be denoise filtered.		0	The U and V channels will be passed to the next stage after DN unchanged.																										
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	11:6	<b>Chroma Temporal Difference Threshold</b>																																				
		<table border="1"> <tr> <td>Format:</td><td colspan="2" rowspan="4">U6</td></tr> <tr> <td colspan="3"> <table border="1"> <tr> <td colspan="4"><b>Programming Notes</b></td></tr> <tr> <td colspan="4">0 &lt; [Chroma Temporal Difference Threshold - Chroma Low Temporal Difference Threshold] &lt; 16 (Larger than 0 and less than or equal to 16)</td></tr> </table> </td></tr> <tr> <td></td><td>5:0</td><td colspan="3"><b>Chroma Low Temporal Difference Threshold</b></td></tr> <tr> <td></td><td></td><td rowspan="5"> <table border="1"> <tr> <td>Format:</td><td colspan="2" rowspan="4">U6</td></tr> <tr> <td colspan="3"> <table border="1"> <tr> <td colspan="4"><b>Programming Notes</b></td></tr> <tr> <td colspan="4">0 &lt; [Chroma Temporal Difference Threshold - Chroma Low Temporal Difference Threshold] &lt; 16 (Larger than 0 and less than or equal to 16)</td></tr> </table> </td></tr> </table></td></tr></table>	Format:	U6		<table border="1"> <tr> <td colspan="4"><b>Programming Notes</b></td></tr> <tr> <td colspan="4">0 &lt; [Chroma Temporal Difference Threshold - Chroma Low Temporal Difference Threshold] &lt; 16 (Larger than 0 and less than or equal to 16)</td></tr> </table>			<b>Programming Notes</b>				0 < [Chroma Temporal Difference Threshold - Chroma Low Temporal Difference Threshold] < 16 (Larger than 0 and less than or equal to 16)					5:0	<b>Chroma Low Temporal Difference Threshold</b>					<table border="1"> <tr> <td>Format:</td><td colspan="2" rowspan="4">U6</td></tr> <tr> <td colspan="3"> <table border="1"> <tr> <td colspan="4"><b>Programming Notes</b></td></tr> <tr> <td colspan="4">0 &lt; [Chroma Temporal Difference Threshold - Chroma Low Temporal Difference Threshold] &lt; 16 (Larger than 0 and less than or equal to 16)</td></tr> </table> </td></tr> </table>	Format:	U6		<table border="1"> <tr> <td colspan="4"><b>Programming Notes</b></td></tr> <tr> <td colspan="4">0 &lt; [Chroma Temporal Difference Threshold - Chroma Low Temporal Difference Threshold] &lt; 16 (Larger than 0 and less than or equal to 16)</td></tr> </table>			<b>Programming Notes</b>				0 < [Chroma Temporal Difference Threshold - Chroma Low Temporal Difference Threshold] < 16 (Larger than 0 and less than or equal to 16)			
Format:	U6																																					
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	5:0	<b>Chroma Low Temporal Difference Threshold</b>																																				
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<b>VEBOX_DNDI_STATE</b>						
9	31:12	<b>Reserved</b> Format: MBZ				
	11:8	<b>Hot Pixel Count</b> Format: U4 Number of neighboring pixels different more than <b>HotPixThr</b> before a pixel is considered hot. <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center; padding: 2px;">Value</th><th style="text-align: center; padding: 2px;">Name</th></tr> </thead> <tbody> <tr> <td style="padding: 2px;">[0,8]</td><td></td></tr> </tbody> </table> <b>Programming Notes</b> 0 will cause all pixels to be considered hot and will perform a median filter on the entire image.	Value	Name	[0,8]	
Value	Name					
[0,8]						
	7:0	<b>Hot Pixel Threshold</b> Format: U8 Threshold for a difference from the value of a neighboring pixel. Is shifted up to 12-bits before compare.				

## VEBOX\_Filter\_Coefficient

VEBOX_Filter_Coefficient				
DWord	Bit	Description		
0	7:0	<b>2's Complement Filter Coefficient</b> <table border="1"><tr><td>Format:</td><td>S1.6 2's Complement</td></tr></table> <b>Range:</b> [-2, +2)	Format:	S1.6 2's Complement
Format:	S1.6 2's Complement			

## VEBOX\_FORWARD\_GAMMA\_CORRECTION\_STATE

<b>VEBOX_FORWARD_GAMMA_CORRECTION_STATE</b>						
<b>DWord</b>	<b>Bit</b>	<b>Description</b>				
0	31:24	<b>PWL_Fwd_Gamma_Point 3</b> <table border="1"> <tr> <td>Default Value:</td><td>79</td></tr> <tr> <td>Format:</td><td>U8</td></tr> </table>	Default Value:	79	Format:	U8
Default Value:	79					
Format:	U8					
23:16	<b>PWL_Fwd_Gamma_Point 2</b> <table border="1"> <tr> <td>Default Value:</td><td>55</td></tr> <tr> <td>Format:</td><td>U8</td></tr> </table>	Default Value:	55	Format:	U8	
Default Value:	55					
Format:	U8					
15:8	<b>PWL_Fwd_Gamma_Point 1</b> <table border="1"> <tr> <td>Default Value:</td><td>30</td></tr> <tr> <td>Format:</td><td>U8</td></tr> </table>	Default Value:	30	Format:	U8	
Default Value:	30					
Format:	U8					
7:1	<b>Reserved</b> <table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ			
Format:	MBZ					
0	<b>Forward Gamma Correction Enable</b> <table border="1"> <tr> <td>Format:</td><td>Enable</td></tr> </table>	Format:	Enable			
Format:	Enable					
	<b>Programming Notes</b> <p><b>Demosaic</b> must also be enabled if this is enabled.</p>					
1	31:24	<b>PWL_Fwd_Gamma_Point 7</b> <table border="1"> <tr> <td>Default Value:</td><td>162</td></tr> <tr> <td>Format:</td><td>U8</td></tr> </table>	Default Value:	162	Format:	U8
Default Value:	162					
Format:	U8					
23:16	<b>PWL_Fwd_Gamma_Point 6</b> <table border="1"> <tr> <td>Default Value:</td><td>141</td></tr> <tr> <td>Format:</td><td>U8</td></tr> </table>	Default Value:	141	Format:	U8	
Default Value:	141					
Format:	U8					
15:8	<b>PWL_Fwd_Gamma_Point 5</b> <table border="1"> <tr> <td>Default Value:</td><td>122</td></tr> <tr> <td>Format:</td><td>U8</td></tr> </table>	Default Value:	122	Format:	U8	
Default Value:	122					
Format:	U8					

## VEBOX\_FORWARD\_GAMMA\_CORRECTION\_STATE

	7:0	<b>PWL_Fwd_Gamma_Point 4</b>
		Default Value: 101
		Format: U8
2	31:24	<b>PWL_Fwd_Gamma_Point 11</b>
		Default Value: 237
		Format: U8
	23:16	<b>PWL_Fwd_Gamma_Point 10</b>
		Default Value: 219
		Format: U8
2	15:8	<b>PWL_Fwd_Gamma_Point 9</b>
		Default Value: 200
		Format: U8
	7:0	<b>PWL_Fwd_Gamma_Point 8</b>
		Default Value: 181
		Format: U8
3	31:24	<b>PWL_Fwd_Gamma_Bias_4</b>
		Default Value: 33
		Format: U8
	23:16	<b>PWL_Fwd_Gamma_Bias_3</b>
		Default Value: 20
		Format: U8
3	15:8	<b>PWL_Fwd_Gamma_Bias_2</b>
		Default Value: 10
		Format: U8
	7:0	<b>PWL_Fwd_Gamma_Bias_1</b>
		Default Value: 3
		Format: U8
4	31:24	<b>PWL_Fwd_Gamma_Bias_8</b>
		Default Value: 117
		Format: U8
	23:16	<b>PWL_Fwd_Gamma_Bias_7</b>
		Default Value: 92
		Format: U8
4	15:8	<b>PWL_Fwd_Gamma_Bias_6</b>
		Default Value: 67
		Format: U8

<b>VEBOX_FORWARD_GAMMA_CORRECTION_STATE</b>			
	7:0	<b>PWL_Fwd_Gamma_Bias_5</b>	
		Default Value:	
		49	
		Format:	
5	31:24	<b>Reserved</b>	
		Format:	
	23:16	<b>PWL_Fwd_Gamma_Bias_11</b>	
		Default Value:	
		215	
		Format:	
	15:8	<b>PWL_Fwd_Gamma_Bias_10</b>	
		Default Value:	
		180	
		Format:	
	7:0	<b>PWL_Fwd_Gamma_Bias_9</b>	
		Default Value:	
		147	
		Format:	
6	31:28	<b>Reserved</b>	
		Format:	
	27:16	<b>PWL_Fwd_Gamma_Slope_1</b>	
		Default Value:	
		048h 72/256	
		Format:	
	15:12	<b>Reserved</b>	
		Format:	
	11:0	<b>PWL_Fwd_Gamma_Slope_0</b>	
		Default Value:	
		01Ah 26/256	
		Format:	
7	31:28	<b>Reserved</b>	
		Format:	
	27:16	<b>PWL_Fwd_Gamma_Slope_3</b>	
		Default Value:	
		097h 151/256	
		Format:	
	15:12	<b>Reserved</b>	
		Format:	
	11:0	<b>PWL_Fwd_Gamma_Slope_2</b>	
		Default Value:	
		06Bh 107/256	
		Format:	
8	31:28	<b>Reserved</b>	
		Format:	
		MBZ	

## VEBOX\_FORWARD\_GAMMA\_CORRECTION\_STATE

	27:16	<b>PWL_Fwd_Gamma_Slope_5</b>
		Default Value: 0F3h 243/256
		Format: U4.8
	15:12	<b>Reserved</b>
		Format: MBZ
	11:0	<b>PWL_Fwd_Gamma_Slope_4</b>
		Default Value: 0C3h 195/256
		Format: U4.8
9	31:28	<b>Reserved</b>
9		Format: MBZ
9	27:16	<b>PWL_Fwd_Gamma_Slope_7</b>
9		Default Value: 151h 337/256
9		Format: U4.8
9	15:12	<b>Reserved</b>
9		Format: MBZ
9	11:0	<b>PWL_Fwd_Gamma_Slope_6</b>
9		Default Value: 131h 305/256
9		Format: U4.8
10	31:28	<b>Reserved</b>
10		Format: MBZ
10	27:16	<b>PWL_Fwd_Gamma_Slope_9</b>
10		Default Value: 1BDh 445/256
10		Format: U4.8
10	15:12	<b>Reserved</b>
10		Format: MBZ
10	11:0	<b>PWL_Fwd_Gamma_Slope_8</b>
10		Default Value: 194h 404/256
10		Format: U4.8
11	31:28	<b>Reserved</b>
11		Format: MBZ
11	27:16	<b>PWL_Fwd_Gamma_Slope_11</b>
11		Default Value: 22Bh 555/256
11		Format: U4.8
11	15:12	<b>Reserved</b>
11		Format: MBZ

**VEBOX\_FORWARD\_GAMMA\_CORRECTION\_STATE**

	11:0	<b>PWL_Fwd_Gamma_Slope_10</b>
		Default Value: 1F2h 498/256
		Format: U4.8

## VEBOX\_FRONT\_END\_CSC\_STATE

VEBOX_FRONT_END_CSC_STATE		
DWord	Bit	Description
0	31:29	<b>Reserved</b>
		Format: MBZ
	28:16	<b>FECSC C1: Transform coefficient</b>
		Default Value: 0 0
		Format: S2.10
	15:3	<b>FECSC C0: Transform coefficient</b>
		Default Value: 400h 1024
		Format: S2.10
1	2:1	<b>Reserved</b>
		Format: MBZ
	0	<b>FFront End C SC Transform Enable</b>
		Format: Enable
		<b>Programming Notes</b>
		Demosaic must also be enabled if this is enabled.
2	31:26	<b>Reserved</b>
		Format: MBZ
	25:13	<b>FEC SC C3: Transform coefficient</b>
		Default Value: 0
		Format: S2.10
3	12:0	<b>FEC SC C2: Transform coefficient</b>
		Default Value: 0
		Format: S2.10
4	31:26	<b>Reserved</b>
		Format: MBZ

<b>VEBOX_FRONT_END_CSC_STATE</b>			
	25:13	<b>FEC SC C5: Transform coefficient</b>	
		Default Value:	0
	12:0	<b>FEC SC C4: Transform coefficient</b>	
		Default Value:	400h 1024
3	31:26	<b>Reserved</b>	
		Format:	MBZ
	25:13	<b>FEC SC C7: Transform coefficient</b>	
		Default Value:	0
4	12:0	<b>FEC SC C6: Transform coefficient</b>	
		Default Value:	0
		Format:	S2.10
	31:13	<b>Reserved</b>	
		Format:	MBZ
5	12:0	<b>FEC SC C8: Transform coefficient</b>	
		Default Value:	400h 1024
		Format:	S2.10
	31:22	<b>Reserved</b>	
		Format:	MBZ
6	21:11	<b>FEC SC Offset out 1: Offset out for Y/R</b>	
		Default Value:	0
		Format:	S10
	10:0	<b>FEC SC Offset in 1: Offset in for Y/R</b>	
		Default Value:	0
		Format:	S10
	31:22	<b>Reserved</b>	
		Format:	MBZ
	21:11	<b>FEC SC Offset out 2: Offset out for U/G</b>	
		Default Value:	0
		Format:	S10
	10:0	<b>FEC SC Offset in 2: Offset in for U/G</b>	
		Default Value:	0
		Format:	S10

VEBOX_FRONT_END_CSC_STATE		
7	31:22	<b>Reserved</b> Format: MBZ
	21:11	<b>FEC SC Offset out 3: Offset out for V/B</b> Default Value: 0 Format: S10
	10:0	<b>FEC SC Offset in 3: Offset in for V/B</b> Default Value: 0 Format: S10

## VEBOX\_GAMUT\_STATE

VEBOX_GAMUT_STATE								
DWord	Bit	Description						
0	31:25	<b>Reserved</b> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ				
Format:	MBZ							
	24:16	<b>A(r)</b> <table border="1"> <tr> <td>Default Value:</td> <td>436</td> </tr> <tr> <td>Format:</td> <td>U9</td> </tr> </table> <p>Gain_factor_R (default: 436, preferred range: 256-511)</p>	Default Value:	436	Format:	U9		
Default Value:	436							
Format:	U9							
	15	<b>Global Mode Enable</b> The gain factor derived from state CM(w) <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Advance Mode</td> </tr> <tr> <td>1</td> <td>Basic Mode</td> </tr> </tbody> </table>	Value	Name	0	Advance Mode	1	Basic Mode
Value	Name							
0	Advance Mode							
1	Basic Mode							
	14:10	<b>Reserved</b> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ				
Format:	MBZ							
	9:0	<b>CM(w)</b> <table border="1"> <tr> <td>Format:</td> <td>U10</td> </tr> </table> <p>WeightingFactorForGain_factor (only enabled when the GlobalModeEnable is on)</p>	Format:	U10				
Format:	U10							
1	31:26	<b>Reserved</b> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ				
Format:	MBZ							
	25:16	<b>CM(s)</b> <table border="1"> <tr> <td>Format:</td> <td>U2.8</td> </tr> </table> <p>AccurateColorComponentScaling (default: 640/256, preferred range: [512-1023]/256)</p> <p>The default is 640/256</p>	Format:	U2.8				
Format:	U2.8							

VEBOX_GAMUT_STATE		
	15	<b>Reserved</b> Format: MBZ
	14:8	<b>A(g)</b> Format: U7  Gain_factor_G (default: 26/256, preferred range: [26-127]/256) The default is 26/256
	7	<b>Reserved</b> Format: MBZ
	6:0	<b>A(b)</b> Format: U7  Gain_factor_B (default: 26/256, preferred range: [26-127]/256) The default is 26/256
2	31:26	<b>Reserved</b> Format: MBZ
	25:16	<b>R(s)</b> Format: U2.8  RedScaling (default: 768/256, preferred range: [512-1023]/256) The default is 768/256
	15:8	<b>CM(i)</b> Format: U0.8  AccurateColorComponentOffset (default: 192/256, preferred range: [0-192]/256) The default is 192/256
	7:0	<b>R(i)</b> Format: U0.8  RedOffset (default: 128/256, preferred range: [0-128]/256) The default is 128/256
3	31	<b>Reserved</b> Format: MBZ
	30:16	<b>C1</b> Format: S2.12  Coefficient of 3x3 Transform matrix The default is 1141/4096

<b>VEBOX_GAMUT_STATE</b>		
	15	<b>Reserved</b> Format: MBZ
	14:0	<b>C0</b> Format: S2.12  Coefficient of 3x3 Transform matrix The default is 2792/4096
4	31	<b>Reserved</b> Format: MBZ
	30:16	<b>C3</b> Format: S2.12  Coefficient of 3x3 Transform matrix The default is 71/4096
	15	<b>Reserved</b> Format: MBZ
	14:0	<b>C2</b> Format: S2.12  Coefficient of 3x3 Transform matrix The default is 34/4096
5	31	<b>Reserved</b> Format: MBZ
	30:16	<b>C5</b> Format: S2.12  Coefficient of 3x3 Transform matrix The default is -52/4096
	15	<b>Reserved</b> Format: MBZ
	14:0	<b>C4</b> Format: S2.12  Coefficient of 3x3 Transform matrix The default is 3663/4096
6	31	<b>Reserved</b> Format: MBZ

<b>VEBOX_GAMUT_STATE</b>			
	30:16	<b>C7</b>	
		Format:	S2.12
		Coefficient of 3x3 Transform matrix	
		The default is 168/4096	
	15	<b>Reserved</b>	
		Format:	MBZ
	14:0	<b>C6</b>	
		Format:	S2.12
		Coefficient of 3x3 Transform matrix	
		The default is -12/4096	
7	31:15	<b>Reserved</b>	
7		Format:	MBZ
7	14:0	<b>C8</b>	
7		Format:	S2.12
7		Coefficient of 3x3 Transform matrix	
7		The default is 3434/4096	
8	31:24	<b>PWL_Gamma_Point 4</b>	
8		Default Value:	9
8		Format:	U8
8		Point 4 for PWL for gamma correction	
8	23:16	<b>PWL_Gamma_Point 3</b>	
8		Default Value:	5
8		Format:	U8
8		Point 3 for PWL for gamma correction	
8	15:8	<b>PWL_Gamma_Point 2</b>	
8		Default Value:	2
8		Format:	U8
8		Point 2 for PWL for gamma correction	
8	7:0	<b>PWL_Gamma_Point 1</b>	
8		Default Value:	1
8		Format:	U8
8		Point 1 for PWL for gamma correction	

<b>VEBOX_GAMUT_STATE</b>			
9	31:24	<b>PWL_Gamma_Point 8</b>	
		Default Value:	65
		Point 8 for PWL for gamma correction	
		<b>PWL_Gamma_Point 7</b>	
10	23:16	Default Value:	42
		Point 7 for PWL for gamma correction	
		<b>PWL_Gamma_Point 6</b>	
		Default Value:	26
10	15:8	Point 6 for PWL for gamma correction	
		<b>PWL_Gamma_Point 5</b>	
		Default Value:	16
		Point 5 for PWL for gamma correction	
10	31:24	<b>Reserved</b>	
		Format:	MBZ
		<b>PWL_Gamma_Point 11</b>	
		Default Value:	187
10	23:16	Format:	U8
		Point 11 for PWL for gamma correction	
		<b>PWL_Gamma_Point 10</b>	
		Default Value:	136
10	15:8	Format:	U8
		Point 10 for PWL for gamma correction	
		<b>PWL_Gamma_Point 9</b>	
		Default Value:	96
10	7:0	Format:	U8
		Point 9 for PWL for gamma correction	
		<b>PWL_Gamma_Bias_4</b>	
		Default Value:	53
11	31:24	Format:	U8
		Bias 4 for PWL for gamma correction	

## VEBOX\_GAMUT\_STATE

	23:16	<b>PWL_Gamma_Bias_3</b>				
		<table border="1"> <tr> <td>Default Value:</td><td>38</td></tr> <tr> <td>Format:</td><td>U8</td></tr> </table> <p>Bias 3 for PWL for gamma correction</p>	Default Value:	38	Format:	U8
Default Value:	38					
Format:	U8					
	15:8	<b>PWL_Gamma_Bias_2</b>				
		<table border="1"> <tr> <td>Default Value:</td><td>23</td></tr> <tr> <td>Format:</td><td>U8</td></tr> </table> <p>Bias 2 for PWL for gamma correction</p>	Default Value:	23	Format:	U8
Default Value:	23					
Format:	U8					
	7:0	<b>PWL_Gamma_Bias_1</b>				
		<table border="1"> <tr> <td>Default Value:</td><td>13</td></tr> <tr> <td>Format:</td><td>U8</td></tr> </table> <p>Bias 1 for PWL for gamma correction</p>	Default Value:	13	Format:	U8
Default Value:	13					
Format:	U8					
12	31:24	<b>PWL_Gamma_Bias_8</b>				
		<table border="1"> <tr> <td>Default Value:</td><td>139</td></tr> <tr> <td>Format:</td><td>U8</td></tr> </table> <p>Bias 8 for PWL for gamma correction</p>	Default Value:	139	Format:	U8
Default Value:	139					
Format:	U8					
	23:16	<b>PWL_Gamma_Bias_7</b>				
		<table border="1"> <tr> <td>Default Value:</td><td>114</td></tr> <tr> <td>Format:</td><td>U8</td></tr> </table> <p>Bias 7 for PWL for gamma correction</p>	Default Value:	114	Format:	U8
Default Value:	114					
Format:	U8					
	15:8	<b>PWL_Gamma_Bias_6</b>				
		<table border="1"> <tr> <td>Default Value:</td><td>91</td></tr> <tr> <td>Format:</td><td>U8</td></tr> </table> <p>Bias 6 for PWL for gamma correction</p>	Default Value:	91	Format:	U8
Default Value:	91					
Format:	U8					
	7:0	<b>PWL_Gamma_Bias_5</b>				
		<table border="1"> <tr> <td>Default Value:</td><td>71</td></tr> <tr> <td>Format:</td><td>U8</td></tr> </table> <p>Bias 5 for PWL for gamma correction</p>	Default Value:	71	Format:	U8
Default Value:	71					
Format:	U8					
13	31:24	<b>Reserved</b>				
		<table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ		
Format:	MBZ					

<b>VEBOX_GAMUT_STATE</b>			
	23:16	<b>PWL_Gamma_Bias_11</b>	
		Default Value:	223
		Format:	U8
	15:8	Bias 11 for PWL for gamma correction	
		<b>PWL_Gamma_Bias_10</b>	
		Default Value:	193
	7:0	Format:	U8
		Bias 10 for PWL for gamma correction	
		<b>PWL_Gamma_Bias_9</b>	
	14	Default Value:	165
		Format:	U8
		Bias 9 for PWL for gamma correction	
	31:28	<b>Reserved</b>	
		Format:	MBZ
	27:16	<b>PWL_Gamma_Slope_1</b>	
		Format:	U4.8
	15:12	Slope 1 for PWL for gamma correction	
		The default is 2560/256	
	11:0	<b>Reserved</b>	
		Format:	MBZ
	31:28	<b>PWL_Gamma_Slope_0</b>	
		Format:	U4.8
	27:16	Slope 0 for PWL for gamma correction	
		The default is 3328/256	
	15:12	<b>Reserved</b>	
		Format:	MBZ
	15:12	<b>PWL_Gamma_Slope_3</b>	
		Format:	U4.8
	15:12	Slope 3 for PWL for gamma correction	
		The default is 960/256	
	15:12	<b>Reserved</b>	
		Format:	MBZ

VEBOX_GAMUT_STATE				
	11:0	<b>PWL_Gamma_Slope_2</b>		
		Format:	U4.8	
		Slope 2 for PWL for gamma correction		
		The default is 1280/256		
16	31:28	<b>Reserved</b>		
		Format:	MBZ	
	27:16	<b>PWL_Gamma_Slope_5</b>		
		Format:	U4.8	
		Slope 5 for PWL for gamma correction		
		The default is 512/256		
	15:12	<b>Reserved</b>		
		Format:	MBZ	
	11:0	<b>PWL_Gamma_Slope_4</b>		
		Format:	U4.8	
		Slope 4 for PWL for gamma correction		
		The default is 658/256		
17	31:28	<b>Reserved</b>		
		Format:	MBZ	
	27:16	<b>PWL_Gamma_Slope_7</b>		
		Format:	U4.8	
		Slope 7 for PWL for gamma correction		
		The default is 278/256		
	15:12	<b>Reserved</b>		
		Format:	MBZ	
	11:0	<b>PWL_Gamma_Slope_6</b>		
		Format:	U4.8	
		Slope 6 for PWL for gamma correction		
		The default is 368/256		
18	31:28	<b>Reserved</b>		
		Format:	MBZ	

<b>VEBOX_GAMUT_STATE</b>				
	27:16	<b>PWL_Gamma_Slope_9</b>		
		Format:	U4.8	
		Slope 9 for PWL for gamma correction		
		The default is 179/256		
	15:12	<b>Reserved</b>		
		Format:	MBZ	
	11:0	<b>PWL_Gamma_Slope_8</b>		
		Format:	U4.8	
		Slope 8 for PWL for gamma correction		
		The default is 215/256		
19	31:28	<b>Reserved</b>		
19		Format:	MBZ	
19	27:16	<b>PWL_Gamma_Slope_11</b>		
19		Format:	U4.8	
19		Slope 11 for PWL for gamma correction		
19		The default is 124/256		
19	15:12	<b>Reserved</b>		
19		Format:	MBZ	
19	11:0	<b>PWL_Gamma_Slope_10</b>		
19		Format:	U4.8	
19		Slope 10 for PWL for gamma correction		
19		The default is 151/256		
20	31:24	<b>PWL_INV_GAMMA_Point 4</b>		
20		Default Value:	101	
20		Format:	U8	
20		Point 4 for PWL for inverse gamma correction		
20	23:16	<b>PWL_INV_GAMMA_Point 3</b>		
20		Default Value:	79	
20		Format:	U8	
20		Point 3 for PWL for inverse gamma correction		

VEBOX_GAMUT_STATE			
	15:8	<b>PWL_INV_GAMMA_Point 2</b>	
		Default Value:	55
	7:0	Format:	U8
		Point 2 for PWL for inverse gamma correction	
	21	<b>PWL_INV_GAMMA_Point 1</b>	
		Default Value:	30
	31:24	Format:	U8
		Point 1 for PWL for inverse gamma correction	
	23:16	<b>PWL_INV_GAMMA_Point 8</b>	
		Format:	U8
	15:8	Point 8 for PWL for inverse gamma correction	
		<b>Value</b>	<b>Name</b>
	23:16	181	
		<b>Value</b>	<b>Name</b>
	15:8	<b>PWL_INV_GAMMA_Point 7</b>	
		Format:	U8
	15:8	Point 7 for PWL for inverse gamma correction	
		<b>Value</b>	<b>Name</b>
	7:0	162	
		<b>Value</b>	<b>Name</b>
	22	<b>PWL_INV_GAMMA_Point 6</b>	
		Format:	U8
	31:24	Point 6 for PWL for inverse gamma correction	
		<b>Value</b>	<b>Name</b>
	23:16	141	
		<b>Value</b>	<b>Name</b>
	7:0	<b>PWL_INV_GAMMA_Point 5</b>	
		Format:	U8
	22	Point 5 for PWL for inverse gamma correction	
		<b>Value</b>	<b>Name</b>
	31:24	122	
		<b>Value</b>	<b>Name</b>
	23:16	<b>Reserved</b>	
		Format:	MBZ
	23:16	<b>PWL_INV_GAMMA_Point 11</b>	
		Default Value:	237
		Format:	U8
		Point 11 for PWL for inverse gamma correction	

VEBOX_GAMUT_STATE			
	15:8	<b>PWL_INV_GAMMA_Point_10</b>	
		Default Value:	219
	7:0	<b>PWL_INV_GAMMA_Point_9</b>	
		Default Value:	200
	23	<b>PWL_INV_GAMMA_Bias_4</b>	
		Default Value:	33
		Format:	U8
		Bias 4 for PWL for inverse gamma correction	
	23:16	<b>PWL_INV_GAMMA_Bias_3</b>	
		Default Value:	20
		Format:	U8
		Bias 3 for PWL for inverse gamma correction	
	15:8	<b>PWL_INV_GAMMA_Bias_2</b>	
		Default Value:	10
		Format:	U8
		Bias 2 for PWL for inverse gamma correction	
	7:0	<b>PWL_INV_GAMMA_Bias_1</b>	
		Default Value:	3
		Format:	U8
		Bias 1 for PWL for inverse gamma correction	
	24	<b>PWL_INV_GAMMA_Bias_8</b>	
		Default Value:	117
		Format:	U8
		Bias 8 for PWL for inverse gamma correction	
	23:16	<b>PWL_INV_GAMMA_Bias_7</b>	
		Default Value:	92
		Format:	U8
		Bias 7 for PWL for inverse gamma correction	

VEBOX_GAMUT_STATE			
	15:8	<b>PWL_INV_GAMMA_Bias_6</b>	
		Default Value:	67
		Format:	U8
		Bias 6 for PWL for inverse gamma correction	
	7:0	<b>PWL_INV_GAMMA_Bias_5</b>	
		Default Value:	49
		Format:	U8
		Bias 5 for PWL for inverse gamma correction	
25	31:24	<b>Reserved</b>	
		Format:	MBZ
	23:16	<b>PWL_INV_GAMMA_Bias_11</b>	
		Default Value:	215
		Format:	U8
		Bias 11 for PWL for inverse gamma correction	
	15:8	<b>PWL_INV_GAMMA_Bias_10</b>	
		Default Value:	180
		Format:	U8
		Bias 10 for PWL for inverse gamma correction	
	7:0	<b>PWL_INV_GAMMA_Bias_9</b>	
		Default Value:	147
		Format:	U8
		Bias 9 for PWL for inverse gamma correction	
26	31:28	<b>Reserved</b>	
		Format:	MBZ
	27:16	<b>PWL_INV_GAMMA_Slope_1</b>	
		Format:	U4.8
		Slope 1 for PWL for gamma correction	
		The default is 72/256	
	15:12	<b>Reserved</b>	
		Format:	MBZ

VEBOX_GAMUT_STATE				
	11:0	<b>PWL_INV_GAMMA_Slope_0</b>		
		Format:	U4.8	
		Slope 0 for PWL for gamma correction		
		The default is 26/256		
27	31:28	<b>Reserved</b>		
		Format:	MBZ	
	27:16	<b>PWL_INV_GAMMA_Slope_3</b>		
		Format:	U4.8	
		Slope 3 for PWL for gamma correction		
		The default is 151/256		
	15:12	<b>Reserved</b>		
		Format:	MBZ	
	11:0	<b>PWL_INV_GAMMA_Slope_2</b>		
		Format:	U4.8	
		Slope 2 for PWL for gamma correction		
		The default is 107/256		
28	31:28	<b>Reserved</b>		
		Format:	MBZ	
	27:16	<b>PWL_INV_GAMMA_Slope_5</b>		
		Format:	U4.8	
		Slope 5 for PWL for gamma correction		
		The default is 243/256		
	15:12	<b>Reserved</b>		
		Format:	MBZ	
	11:0	<b>PWL_INV_GAMMA_Slope_4</b>		
		Format:	U4.8	
		Slope 4 for PWL for gamma correction		
		The default is 195/256		
29	31:28	<b>Reserved</b>		
		Format:	MBZ	

VEBOX_GAMUT_STATE				
	27:16	<b>PWL_INV_GAMMA_Slope_7</b>		
		Format:	U4.8	
		Slope 7 for PWL for gamma correction		
		The default is 337/256		
	15:12	<b>Reserved</b>		
		Format:	MBZ	
	11:0	<b>PWL_INV_GAMMA_Slope_6</b>		
		Format:	U4.8	
		Slope 6 for PWL for gamma correction		
		The default is 305/256		
30	31:28	<b>Reserved</b>		
		Format:	MBZ	
	27:16	<b>PWL_INV_GAMMA_Slope_9</b>		
		Format:	U4.8	
		Slope 9 for PWL for gamma correction		
		The default is 445/256		
	15:12	<b>Reserved</b>		
		Format:	MBZ	
	11:0	<b>PWL_INV_GAMMA_Slope_8</b>		
		Format:	U4.8	
		Slope 8 for PWL for gamma correction		
		The default is 404/256		
31	31:28	<b>Reserved</b>		
		Format:	MBZ	
	27:16	<b>PWL_INV_GAMMA_Slope_11</b>		
		Format:	U4.8	
		Slope 11 for PWL for gamma correction		
		The default is 555/256		
	15:12	<b>Reserved</b>		
		Format:	MBZ	

VEBOX_GAMUT_STATE				
	11:0	<b>PWL_INV_GAMMA_Slope_10</b>		
		Format:	U4.8	
		Slope 10 for PWL for gamma correction		
		The default is 498/256		
32	31	<b>Reserved</b>		
		Format:	MBZ	
	30:16	<b>Offset_in_G</b>		
		Default Value:	0	
		Format:	S14	
		The input offset for green component		
	15	<b>Reserved</b>		
		Format:	MBZ	
	14:0	<b>Offset_in_R</b>		
		Default Value:	0	
		Format:	S14	
		The input offset for red component		
33	31	<b>Reserved</b>		
		Format:	MBZ	
	30:16	<b>Offset_out_B</b>		
		Format:	S2.12	
		The input offset for green component		
		The default is -1246/4096		
	15	<b>Reserved</b>		
		Format:	MBZ	
	14:0	<b>Offset_in_B</b>		
		Default Value:	0	
		Format:	S14	
		The input offset for red component		
34	31	<b>Reserved</b>		
		Format:	MBZ	

VEBOX_GAMUT_STATE										
	30:16	<b>Offset_out_G</b>								
		Format:	S2.12							
		The input offset for green component								
		The default is -983/4096								
	15	<b>Reserved</b>								
		Format:	MBZ							
	14:0	<b>Offset_out_R</b>								
		Format:	S2.12							
		The input offset for red component								
		The default is -974/4096								
35	31	<b>Reserved</b>								
		Format:	MBZ							
	30	<b>FullRangeMappingEnable</b>								
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0</td><td>Basic Mode <b>[Default]</b></td></tr> <tr> <td>1</td><td>Advance Mode</td></tr> </tbody> </table>		Value	Name	0	Basic Mode <b>[Default]</b>	1	Advance Mode	
Value	Name									
0	Basic Mode <b>[Default]</b>									
1	Advance Mode									
	29:20	<b>d(in,default)</b>								
		Default Value:	205							
		Format:	U10							
		InnerTriangleMappingLength								
	19:10	<b>d(out, default)</b>								
		Default Value:	164							
		Format:	U10							
		OuterTriangleMappingLength								
	9:0	<b>d1(out)</b>								
		Default Value:	287							
		Format:	U10							
		OuterTriangleMappingLengthBelow								
36	31	<b>xvYccDecEncEnable</b>								
		This bit is valid only when ColorGamutCompressionnEnable is on.								
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>1</td><td>Both xvYcc decode and xvYcc encode are enabled <b>[Default]</b></td></tr> <tr> <td>0</td><td>To disable both xvYcc decode and xvYcc encode</td></tr> </tbody> </table>			Value	Name	1	Both xvYcc decode and xvYcc encode are enabled <b>[Default]</b>	0	To disable both xvYcc decode and xvYcc encode
Value	Name									
1	Both xvYcc decode and xvYcc encode are enabled <b>[Default]</b>									
0	To disable both xvYcc decode and xvYcc encode									

<b>VEBOX_GAMUT_STATE</b>																		
	30:28	<b>CompressionLineShift</b>																
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>3</td><td>[Default]</td></tr> <tr> <td>[0,4]</td><td></td></tr> </tbody> </table>	Value	Name	3	[Default]	[0,4]											
Value	Name																	
3	[Default]																	
[0,4]																		
	27:10	<b>Reserved</b>																
		<table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ														
Format:	MBZ																	
	9:0	<b>d1(in)</b>																
		<table border="1"> <tr> <td>Default Value:</td><td>820</td></tr> <tr> <td>Format:</td><td>U10</td></tr> </table>	Default Value:	820	Format:	U10	InnerTriangleMappingLengthBelow											
Default Value:	820																	
Format:	U10																	
37	31:30	<b>GCC BasicModeSelection</b>																
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>00b</td><td>Default</td><td></td></tr> <tr> <td>01b</td><td>Scaling Factor</td><td>Used along with Dword66 Bits 28:11</td></tr> <tr> <td>10b</td><td>Single Axis Gamma Correction</td><td>Used along with Dword67 Bit 29</td></tr> <tr> <td>11b</td><td>Scaling factor with fixed luma</td><td>Used along with Dword37 Bits 28:11</td></tr> </tbody> </table>	Value	Name	Description	00b	Default		01b	Scaling Factor	Used along with Dword66 Bits 28:11	10b	Single Axis Gamma Correction	Used along with Dword67 Bit 29	11b	Scaling factor with fixed luma	Used along with Dword37 Bits 28:11	
Value	Name	Description																
00b	Default																	
01b	Scaling Factor	Used along with Dword66 Bits 28:11																
10b	Single Axis Gamma Correction	Used along with Dword67 Bit 29																
11b	Scaling factor with fixed luma	Used along with Dword37 Bits 28:11																
	29	<b>LumaChormaOnlyCorrection</b>																
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0</td><td>Luma Only Correction [Default]</td></tr> <tr> <td>1</td><td>Chorma Only Correction</td></tr> </tbody> </table>	Value	Name	0	Luma Only Correction [Default]	1	Chorma Only Correction										
Value	Name																	
0	Luma Only Correction [Default]																	
1	Chorma Only Correction																	
	28:25	<b>Reserved</b>																
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Project:	BDW																	
Format:	MBZ																	
	24:11	<b>BasicModeScalingFactor</b>																
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Project:	BDW																	
Format:	U2.12																	
	10:1	<b>Reserved</b>																
		<table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ														
Format:	MBZ																	
	0	<b>Cpi Override</b>																
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0</td><td>[Default]</td></tr> <tr> <td>1</td><td>Override Cpi calculation</td></tr> </tbody> </table>	Value	Name	0	[Default]	1	Override Cpi calculation										
Value	Name																	
0	[Default]																	
1	Override Cpi calculation																	

## VEBOX\_PROCAMP\_STATE

VEBOX_PROCAMP_STATE								
DWord	Bit	Description						
0	31:28	<b>Reserved</b> <table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ				
Format:	MBZ							
27:17	<b>Contrast</b> <table border="1"> <tr> <td>Default Value:</td><td>80h = 1.0 in fixed point U4.7</td></tr> <tr> <td>Format:</td><td>U4.7</td></tr> <tr> <td colspan="2">Contrast magnitude.</td></tr> </table>	Default Value:	80h = 1.0 in fixed point U4.7	Format:	U4.7	Contrast magnitude.		
Default Value:	80h = 1.0 in fixed point U4.7							
Format:	U4.7							
Contrast magnitude.								
16:13	<b>Reserved</b> <table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ					
Format:	MBZ							
12:1	<b>Brightness</b> <table border="1"> <tr> <td>Default Value:</td><td>0 or 0.0</td></tr> <tr> <td>Format:</td><td>S7.4 2's complement</td></tr> <tr> <td colspan="2">Brightness magnitude.</td></tr> </table>	Default Value:	0 or 0.0	Format:	S7.4 2's complement	Brightness magnitude.		
Default Value:	0 or 0.0							
Format:	S7.4 2's complement							
Brightness magnitude.								
0	<b>PROCAMP Enable</b> <table border="1"> <tr> <td>Default Value:</td><td>1</td></tr> <tr> <td>Format:</td><td>Enable</td></tr> </table>	Default Value:	1	Format:	Enable			
Default Value:	1							
Format:	Enable							
31:16	<b>Cos_c_s</b> <table border="1"> <tr> <td>Default Value:</td><td>256</td></tr> <tr> <td>Format:</td><td>S7.8 2's complement</td></tr> <tr> <td colspan="2">UV multiplication cosine factor.</td></tr> </table>	Default Value:	256	Format:	S7.8 2's complement	UV multiplication cosine factor.		
Default Value:	256							
Format:	S7.8 2's complement							
UV multiplication cosine factor.								
1	15:0	<b>Sin_c_s</b> <table border="1"> <tr> <td>Default Value:</td><td>0</td></tr> <tr> <td>Format:</td><td>S7.8 2's complement</td></tr> <tr> <td colspan="2">UV multiplication sine factor.</td></tr> </table>	Default Value:	0	Format:	S7.8 2's complement	UV multiplication sine factor.	
Default Value:	0							
Format:	S7.8 2's complement							
UV multiplication sine factor.								

## VEBOX\_RGB\_TO\_GAMMA\_CORRECTION

VEBOX_RGB_TO_GAMMA_CORRECTION		
DWord	Bit	Description
0..1	63:48	<b>B-ch Corrected Value</b>
		Default Value: 0h
		Format: U16
	47:32	<b>G-ch Corrected Value</b>
		Default Value: 0h
		Format: U16
	31:16	<b>R-ch Corrected Value</b>
		Default Value: 0h
		Format: U16
	15:0	<b>Pixel Value</b>
		Default Value: 0h
		Format: U16

## VEBOX\_STD\_STE\_STATE

VEBOX_STD_STE_STATE								
DWord	Bit	Description						
0	31:24	<p><b>V_Mid</b></p> <table border="1"> <tr> <td>Default Value:</td><td>154</td></tr> <tr> <td>Format:</td><td>U8</td></tr> </table> <p>Rectangle middle-point V coordinate.</p>	Default Value:	154	Format:	U8		
Default Value:	154							
Format:	U8							
	23:16	<p><b>U_Mid</b></p> <table border="1"> <tr> <td>Default Value:</td><td>110</td></tr> <tr> <td>Format:</td><td>U8</td></tr> </table> <p>Rectangle middle-point U coordinate.</p>	Default Value:	110	Format:	U8		
Default Value:	110							
Format:	U8							
	15:10	<p><b>Hue_Max</b></p> <table border="1"> <tr> <td>Default Value:</td><td>14</td></tr> <tr> <td>Format:</td><td>U6</td></tr> </table> <p>Rectangle half width.</p>	Default Value:	14	Format:	U6		
Default Value:	14							
Format:	U6							
	9:4	<p><b>Sat_Max</b></p> <table border="1"> <tr> <td>Default Value:</td><td>31</td></tr> <tr> <td>Format:</td><td>U6</td></tr> </table> <p>Rectangle half length.</p>	Default Value:	31	Format:	U6		
Default Value:	31							
Format:	U6							
	3	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ				
Format:	MBZ							
	2	<p><b>Output Control</b></p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0</td><td>Output Pixels</td></tr> <tr> <td>1</td><td>Output STD Decisions</td></tr> </tbody> </table>	Value	Name	0	Output Pixels	1	Output STD Decisions
Value	Name							
0	Output Pixels							
1	Output STD Decisions							

## VEBOX\_STD\_STE\_STATE

	1	<b>STE Enable</b>
		Format: <span style="border: 1px solid black; padding: 2px;">Enable</span>
	0	<b>STD Enable</b>
		Format: <span style="border: 1px solid black; padding: 2px;">Enable</span>
<b>Programming Notes</b>		
This needs to be enabled if 'STD Score Output' is enabled.		
1	31	<b>Reserved</b>
		Project: <span style="border: 1px solid black; padding: 2px;">BDW</span>
		Format: <span style="border: 1px solid black; padding: 2px;">MBZ</span>
	30:28	<b>Diamond Margin</b>
		Default Value: <span style="border: 1px solid black; padding: 2px;">4</span>
		Format: <span style="border: 1px solid black; padding: 2px;">U3</span>
	27:21	<b>Diamond_du</b>
		Default Value: <span style="border: 1px solid black; padding: 2px;">0</span>
		Format: <span style="border: 1px solid black; padding: 2px;">S6 2's complement</span>
		Rhombus center shift in the sat-direction, relative to the rectangle center.
	20:18	<b>HS_margin</b>
		Default Value: <span style="border: 1px solid black; padding: 2px;">3</span>
		Format: <span style="border: 1px solid black; padding: 2px;">U3</span>
		Defines rectangle margin.
	17:10	<b>Cos(<math>\alpha</math>)</b>
		Default Value: <span style="border: 1px solid black; padding: 2px;">79</span>
		Format: <span style="border: 1px solid black; padding: 2px;">S0.7 2's complement</span>
		The default is 79/128
	9:8	<b>Reserved</b>
		Format: <span style="border: 1px solid black; padding: 2px;">MBZ</span>
	7:0	<b>Sin(<math>\alpha</math>)</b>
		Default Value: <span style="border: 1px solid black; padding: 2px;">101</span>
		Format: <span style="border: 1px solid black; padding: 2px;">S0.7 2's complement</span>
		The default is 101/128
2	31:21	<b>Reserved</b>
		Format: <span style="border: 1px solid black; padding: 2px;">MBZ</span>

## **VEBOX\_STD\_STE\_STATE**

		<b>Diamond_alpha</b>
	20:13	Default Value: 100 Format: U2.6 1/tan( $\beta$ ) The default is 100/64
	12:7	<b>Diamond_Th</b> Default Value: 35 Format: U6 Half length of the rhombus axis in the sat-direction.
	6:0	<b>Diamond_dv</b> Default Value: 0 Format: S6 2's complement Rhombus center shift in the hue-direction, relative to the rectangle center.
3	31:24	<b>Y_point_3</b> Default Value: 254 Format: U8 Third point of the Y piecewise linear membership function.
	23:16	<b>Y_point_2</b> Default Value: 47 Format: U8 Second point of the Y piecewise linear membership function.
	15:8	<b>Y_point_1</b> Default Value: 46 Format: U8 First point of the Y piecewise linear membership function.
	7	<b>VY_STD_Enable</b> Format: Enable Enables STD in the VY subspace.
	6:0	<b>Reserved</b> Format: MBZ
4	31:18	<b>Reserved</b> Format: MBZ

## VEBOX STD STE STATE

	17:13	<b>Y_Slope_2</b>
		Default Value: 31
		Format: U2.3
Slope between points Y3 and Y4.		
The default is 31/8		
	12:8	<b>Y_Slope_1</b>
		Default Value: 31
		Format: U2.3
Slope between points Y1 and Y2.		
The default is 31/8		
	7:0	<b>Y_point_4</b>
		Default Value: 255
		Format: U8
Fourth point of the Y piecewise linear membership function.		
5	31:16	<b>INV_Skin_types_margin</b>
		Default Value: 20 Skin_Type_margin
		Format: U0.16
$1/(2 * \text{Skin\_types\_margin})$		
	15:0	<b>INV_Margin_VYL</b>
		Format: U0.16
$1 / \text{Margin\_VYL}$ $1 / \text{Margin\_VYL} = 3300/65536$		
6	31:24	<b>P1L</b>
		Default Value: 216
		Format: U8
Y Point 1 of the lower part of the detection PWLF.		
	23:16	<b>POL</b>
		Default Value: 46
		Format: U8
Y Point 0 of the lower part of the detection PWLF.		

VEBOX_STD_STE_STATE			
	15:0	<b>INV_Margin_VYU</b>	
		Default Value:	1600
		Format:	U0.16
		$1 / \text{Margin\_VYU} = 1600/65536$	
7	31:24	<b>B1L</b>	
		Default Value:	130
		Format:	U8
		V Bias 1 of the lower part of the detection PWLF.	
	23:16	<b>B0L</b>	
		Default Value:	133
		Format:	U8
		V Bias 0 of the lower part of the detection PWLF.	
	15:8	<b>P3L</b>	
		Default Value:	236
		Format:	U8
		Y Point 3 of the lower part of the detection PWLF.	
	7:0	<b>P2L</b>	
		Default Value:	236
		Format:	U8
		Y Point 2 of the lower part of the detection PWLF.	
8	31:27	<b>Reserved</b>	
		Format:	MBZ
	26:16	<b>SOL</b>	
		Default Value:	FFBh
		Format:	S2.8 2's complement
		Slope 0 of the lower part of the detection PWLF.	
		The default is -5/256	
	15:8	<b>B3L</b>	
		Default Value:	130
		Format:	U8
		V Bias 3 of the lower part of the detection PWLF.	

VEBOX_STD_STE_STATE		
	7:0	<b>B2L</b> Default Value: 130 Format: U8 V Bias 2 of the lower part of the detection PWLF.
9	31:22	<b>Reserved</b> Format: MBZ
	21:11	<b>S2L</b> Default Value: 0 Format: S2.8 2's complement The default is 0/256
	10:0	<b>S1L</b> Default Value: 0 Format: S2.8 2's complement  Slope 1 of the lower part of the detection PWLF. The default is 0/256
10	31:27	<b>Reserved</b> Format: MBZ
	26:19	<b>P1U</b> Default Value: 66 Format: U8 Y Point 1 of the upper part of the detection PWLF.
	18:11	<b>POU</b> Default Value: 46 Format: U8 Y Point 0 of the upper part of the detection PWLF.
	10:0	<b>S3L</b> Default Value: 0 Format: S2.8 2's complement  Slope 3 of the lower part of the detection PWLF. The default is 0/256

## VEBOX\_STD\_STE\_STATE

11	31:24	<b>B1U</b>
		Default Value:
		Format:
		V Bias 1 of the upper part of the detection PWLF.
12	23:16	<b>BOU</b>
		Default Value:
		Format:
		V Bias 0 of the upper part of the detection PWLF.
	15:8	<b>P3U</b>
		Default Value:
		Format:
		Y Point 3 of the upper part of the detection PWLF.
	7:0	<b>P2U</b>
		Default Value:
		Format:
		Y Point 2 of the upper part of the detection PWLF.
	31:27	<b>Reserved</b>
	31:27	Format:
	31:27	MBZ
	26:16	<b>SOU</b>
		Default Value:
		Format:
		Slope 0 of the upper part of the detection PWLF.
		The default is 256/256
	15:8	<b>B3U</b>
		Default Value:
		Format:
		V Bias 3 of the upper part of the detection PWLF.
	7:0	<b>B2U</b>
		Default Value:
		Format:
		V Bias 2 of the upper part of the detection PWLF.

<b>VEBOX_STD_STE_STATE</b>				
13	31:22	<b>Reserved</b>		
		Format:	MBZ	
	21:11	<b>S2U</b>		
		Default Value:	F4Dh	
		Format:	S2.8 2's complement	
		Slope 2 of the upper part of the detection PWLF.		
		The default is -179/256		
	10:0	<b>S1U</b>		
		Default Value:	113	
		Format:	S2.8	
		Slope 1 of the upper part of the detection PWLF.		
		The default is 113/256		
14	31:28	<b>Reserved</b>		
		Format:	MBZ	
	27:20	<b>Skin_types_margin</b>		
		Default Value:	20	
		Format:	U8	
		Skin types Y margin Restrict Skin_types_thresh >= Skin_types_margin > 0 Restrict (Skin_types_thresh + Skin_types_margin) <= 255		
	19:12	<b>Skin_types_thresh</b>		
		Default Value:	120	
		Format:	U8	
		Skin types Y margin Restrict Skin_types_thresh >= Skin_types_margin > 0 Restrict (Skin_types_thresh + Skin_types_margin) <= 255		
	11	<b>Skin_Types_Enable</b>		
		Default Value:	0 Disable	
		Format:	Enable	
		Treat differently bright and dark skin types		
	10:0	<b>S3U</b>		
		Default Value:	0	
		Format:	S2.8 2's complement	
		Slope 3 of the upper part of the detection PWLF.		
		The default is 0/256		

VEBOX_STD_STE_STATE				
15	31	<b>Reserved</b>		
		Format:	MBZ	
	30:21	<b>SATB1</b>		
		Default Value:	8	
		Format:	S7.2 2's complement	
		First bias for the saturation PWLF (bright skin).		
		The default is 8/4		
	20:14	<b>SATP3</b>		
		Default Value:	31	
		Format:	S6 2's complement	
		Third point for the saturation PWLF (bright skin).		
	13:7	<b>SATP2</b>		
		Default Value:	6	
		Format:	S6 2's complement	
		Second point for the saturation PWLF (bright skin).		
	6:0	<b>SATP1</b>		
		Default Value:	6	
		Format:	S6 2's complement	
		First point for the saturation PWLF (bright skin).		
16	31	<b>Reserved</b>		
		Format:	MBZ	
	30:20	<b>SATSO</b>		
		Default Value:	297	
		Format:	U3.8	
		Zeroth slope for the saturation PWLF (bright skin)		
		The default is 297/256		
	19:10	<b>SATB3</b>		
		Default Value:	124	
		Format:	S7.2 2's complement	
		Third bias for the saturation PWLF (bright skin)		
		The default is 124/4		

<b>VEBOX_STD_STE_STATE</b>						
	9:0	<b>SATB2</b> <table border="1"> <tr> <td>Default Value:</td><td>8</td></tr> <tr> <td>Format:</td><td>S7.2 2's complement</td></tr> </table> <p>Second bias for the saturation PWLF (bright skin) The default is 8/4</p>	Default Value:	8	Format:	S7.2 2's complement
Default Value:	8					
Format:	S7.2 2's complement					
17	31:22	<b>Reserved</b> <table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ		
Format:	MBZ					
	21:11	<b>SATS2</b> <table border="1"> <tr> <td>Default Value:</td><td>297</td></tr> <tr> <td>Format:</td><td>U3.8</td></tr> </table> <p>Second slope for the saturation PWLF (bright skin) The default is 297/256</p>	Default Value:	297	Format:	U3.8
Default Value:	297					
Format:	U3.8					
	10:0	<b>SATS1</b> <table border="1"> <tr> <td>Default Value:</td><td>85</td></tr> <tr> <td>Format:</td><td>U3.8</td></tr> </table> <p>First slope for the saturation PWLF (bright skin) The default is 85/256</p>	Default Value:	85	Format:	U3.8
Default Value:	85					
Format:	U3.8					
18	31:25	<b>HUEP3</b> <table border="1"> <tr> <td>Default Value:</td><td>14</td></tr> <tr> <td>Format:</td><td>S6 2's complement</td></tr> </table> <p>Third point for the hue PWLF (bright skin)</p>	Default Value:	14	Format:	S6 2's complement
Default Value:	14					
Format:	S6 2's complement					
	24:18	<b>HUEP2</b> <table border="1"> <tr> <td>Default Value:</td><td>6</td></tr> <tr> <td>Format:</td><td>S6 2's complement</td></tr> </table> <p>Second point for the hue PWLF (bright skin)</p>	Default Value:	6	Format:	S6 2's complement
Default Value:	6					
Format:	S6 2's complement					
	17:11	<b>HUEP1</b> <table border="1"> <tr> <td>Default Value:</td><td>7Ah -6</td></tr> <tr> <td>Format:</td><td>S6 2's complement</td></tr> </table> <p>First point for the hue PWLF (bright skin)</p>	Default Value:	7Ah -6	Format:	S6 2's complement
Default Value:	7Ah -6					
Format:	S6 2's complement					

VEBOX_STD_STE_STATE				
	10:0	<b>SATS3</b>		
		Default Value:	256	
		Format:	U3.8	
		Third slope for the saturation PWLF (bright skin)		
		The default is 256/256		
19	31:30	<b>Reserved</b>		
		Format:	MBZ	
	29:20	<b>HUEB3</b>		
		Default Value:	56	
		Format:	S7.2 2's complement	
		Third bias for the hue PWLF (bright skin)		
		The default is 56/4		
	19:10	<b>HUEB2</b>		
		Default Value:	8	
		Format:	S7.2 2's complement	
		Second bias for the hue PWLF (bright skin)		
		The default is 8/4		
	9:0	<b>HUEB1</b>		
		Default Value:	8	
		Format:	S7.2 2's complement	
		First bias for the hue PWLF (bright skin)		
		The default is 8/4		
20	31:22	<b>Reserved</b>		
		Format:	MBZ	
	21:11	<b>HUES1</b>		
		Default Value:	85	
		Format:	U3.8	
		First slope for the hue PWLF (bright skin)		
		The default is 85/256		

<b>VEBOX_STD_STE_STATE</b>										
	10:0	<b>HUES0</b> <table border="1"> <tr> <td>Default Value:</td><td>384</td></tr> <tr> <td>Format:</td><td>U3.8</td></tr> <tr> <td colspan="2">Zeroth slope for the hue PWLF (bright skin)</td></tr> <tr> <td colspan="2">The default is 384/256</td></tr> </table>	Default Value:	384	Format:	U3.8	Zeroth slope for the hue PWLF (bright skin)		The default is 384/256	
Default Value:	384									
Format:	U3.8									
Zeroth slope for the hue PWLF (bright skin)										
The default is 384/256										
21	31:22	<b>Reserved</b> <table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ						
Format:	MBZ									
	21:11	<b>HUES3</b> <table border="1"> <tr> <td>Default Value:</td><td>256</td></tr> <tr> <td>Format:</td><td>U3.8</td></tr> <tr> <td colspan="2">Third slope for the hue PWLF (bright skin)</td></tr> <tr> <td colspan="2">The default is 256/256</td></tr> </table>	Default Value:	256	Format:	U3.8	Third slope for the hue PWLF (bright skin)		The default is 256/256	
Default Value:	256									
Format:	U3.8									
Third slope for the hue PWLF (bright skin)										
The default is 256/256										
	10:0	<b>HUES2</b> <table border="1"> <tr> <td>Default Value:</td><td>384</td></tr> <tr> <td>Format:</td><td>U3.8</td></tr> <tr> <td colspan="2">Second slope for the hue PWLF (bright skin)</td></tr> <tr> <td colspan="2">The default is 384/256</td></tr> </table>	Default Value:	384	Format:	U3.8	Second slope for the hue PWLF (bright skin)		The default is 384/256	
Default Value:	384									
Format:	U3.8									
Second slope for the hue PWLF (bright skin)										
The default is 384/256										
22	31	<b>Reserved</b> <table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ						
Format:	MBZ									
	30:21	<b>SATB1_DARK</b> <table border="1"> <tr> <td>Default Value:</td><td>0</td></tr> <tr> <td>Format:</td><td>S7.2 2's complement</td></tr> <tr> <td colspan="2">First bias for the saturation PWLF (dark skin)</td></tr> <tr> <td colspan="2">The default is 0/4</td></tr> </table>	Default Value:	0	Format:	S7.2 2's complement	First bias for the saturation PWLF (dark skin)		The default is 0/4	
Default Value:	0									
Format:	S7.2 2's complement									
First bias for the saturation PWLF (dark skin)										
The default is 0/4										
	20:14	<b>SATP3_DARK</b> <table border="1"> <tr> <td>Default Value:</td><td>31</td></tr> <tr> <td>Format:</td><td>S6 2's complement</td></tr> <tr> <td colspan="2">Third point for the saturation PWLF (dark skin)</td></tr> </table>	Default Value:	31	Format:	S6 2's complement	Third point for the saturation PWLF (dark skin)			
Default Value:	31									
Format:	S6 2's complement									
Third point for the saturation PWLF (dark skin)										
	13:7	<b>SATP2_DARK</b> <table border="1"> <tr> <td>Default Value:</td><td>31</td></tr> <tr> <td>Format:</td><td>S6 2's complement</td></tr> <tr> <td colspan="2">Second point for the saturation PWLF (dark skin)</td></tr> </table>	Default Value:	31	Format:	S6 2's complement	Second point for the saturation PWLF (dark skin)			
Default Value:	31									
Format:	S6 2's complement									
Second point for the saturation PWLF (dark skin)										

VEBOX_STD_STE_STATE			
	6:0	<b>SATP1_DARK</b>	
		Default Value:	FF5h
		Format:	S6 2's complement
First point for the saturation PWLF (dark skin) Default Value: -11			
23	31	<b>Reserved</b>	
		Format:	MBZ
	30:20	<b>SATSO_DARK</b>	
		Default Value:	397
		Format:	U3.8
Zeroth slope for the saturation PWLF (dark skin)			
The default is 397/256			
	19:10	<b>SATB3_DARK</b>	
		Default Value:	124
		Format:	S7.2 2's complement
Third bias for the saturation PWLF (dark skin)			
The default is 124/4			
	9:0	<b>SATB2_DARK</b>	
		Default Value:	124
		Format:	S7.2 2's complement
Second bias for the saturation PWLF (dark skin)			
The default is 124/4			
24	31:22	<b>Reserved</b>	
		Format:	MBZ
	21:11	<b>SATS2_DARK</b>	
		Default Value:	256
		Format:	U3.8
Second slope for the saturation PWLF (dark skin)			
The default is 256/256			

## VEBOX STD STE STATE

	10:0	<b>SATS1_DARK</b>		
		Default Value: 189		
		Format: U3.8		
		First slope for the saturation PWLF (dark skin)		
		The default is 189/256		
25	31:25	<b>HUEP3_DARK</b>		
		Default Value: 14		
		Format: S6 2's complement		
		Third point for the hue PWLF (dark skin).		
	24:18	<b>HUEP2_DARK</b>		
		Default Value: 2		
		Format: S6 2's complement		
		Second point for the hue PWLF (dark skin).		
	17:11	<b>HUEP1_DARK</b>		
		Default Value: 0		
		Format: S6 2's complement		
		First point for the hue PWLF (dark skin).		
	10:0	<b>SATS3_DARK</b>		
		Default Value: 256		
		Format: U3.8		
		Third slope for the saturation PWLF (dark skin)		
		The default is 256/256		
26	31:30	<b>Reserved</b>		
		Format: MBZ		
	29:20	<b>HUEB3_DARK</b>		
		Default Value: 56		
		Format: S7.2 2's complement		
		Third bias for the hue PWLF (dark skin).		
		The default is 56/4		

VEBOX_STD_STE_STATE				
	19:10	<b>HUEB2_DARK</b>		
		Default Value:	0	
		Format:	S7.2 2's complement	
		Second bias for the hue PWLF (dark skin).		
		The default is 0/4		
	9:0	<b>HUEB1_DARK</b>		
		Default Value:	0	
		Format:	S7.2 2's complement	
		First bias for the hue PWLF (dark skin).		
		The default is 0/4		
27	31:22	<b>Reserved</b>		
		Format:	MBZ	
	21:11	<b>HUES1_DARK</b>		
		Default Value:	256	
		Format:	U3.8	
		First slope for the hue PWLF (dark skin).		
		The default is 256/256		
	10:0	<b>HUES0_DARK</b>		
		Default Value:	299	
		Format:	U3.8	
		Zeroth slope for the hue PWLF (dark skin).		
		The default is 299/256		
28	31:22	<b>Reserved</b>		
		Format:	MBZ	
	21:11	<b>HUES3_DARK</b>		
		Default Value:	256	
		Format:	U3.8	
		Third slope for the hue PWLF (dark skin).		
		The default is 256/256		

**VEBOX\_STD\_STE\_STATE**

	10:0	<b>HUES2_DARK</b>
		Default Value:
		Format:
Second slope for the hue PWLF (dark skin).		
The default is 299/256		

## VEBOX\_TCC\_STATE

VEBOX_TCC_STATE		
DWord	Bit	Description
0	31:24	<b>SatFactor3</b>
		Default Value: 220
		Format: U1.7
		The saturation factor for yellow. The default is 220/128
	23:16	<b>SatFactor2</b>
		Default Value: 220
		Format: U1.7
		The saturation factor for red. The default is 220/128
	15:8	<b>SatFactor1</b>
		Default Value: 220
		Format: U1.7
		The saturation factor for magenta. The default is 220/128
	7	<b>TCC Enable</b>
	6:0	Format: Enable
	1	<b>Reserved</b>
		Format: MBZ
		<b>SatFactor6</b>
		Default Value: 220
		Format: U1.7
		The saturation factor for blue. The default is 220/128

VEBOX_TCC_STATE			
	23:16	<b>SatFactor5</b>	
		Default Value:	220
		Format:	U1.7
		The saturation factor for cyan.	
		The default is 220/128	
	15:8	<b>SatFactor4</b>	
		Default Value:	220
		Format:	U1.7
		The saturation factor for green.	
		The default is 220/128	
	7:0	<b>Reserved</b>	
		Format:	MBZ
2	31:30	<b>Reserved</b>	
		Format:	MBZ
	29:20	<b>BaseColor3</b>	
		Default Value:	483
		Format:	U10
		Base Color 3 - this value must be greater than BaseColor2	
	19:10	<b>BaseColor2</b>	
		Default Value:	307
		Format:	U10
		Base Color 2 - this value must be greater than BaseColor1	
	9:0	<b>BaseColor1</b>	
		Default Value:	145
		Format:	U10
		Base Color 1	
3	31:30	<b>Reserved</b>	
		Format:	MBZ
	29:20	<b>BaseColor6</b>	
		Default Value:	995
		Format:	U10
		Base Color 6 - this value must be greater than BaseColor5	

VEBOX_TCC_STATE						
	19:10	<b>BaseColor5</b> <table border="1"> <tr> <td>Default Value:</td><td>819</td></tr> <tr> <td>Format:</td><td>U10</td></tr> </table> <p>Base Color 5 - this value must be greater than BaseColor4</p>	Default Value:	819	Format:	U10
Default Value:	819					
Format:	U10					
	9:0	<b>BaseColor4</b> <table border="1"> <tr> <td>Default Value:</td><td>657</td></tr> <tr> <td>Format:</td><td>U10</td></tr> </table> <p>Base Color 4 - this value must be greater than BaseColor3</p>	Default Value:	657	Format:	U10
Default Value:	657					
Format:	U10					
4	31:16	<b>ColorTransitSlope23</b> <table border="1"> <tr> <td>Default Value:</td><td>744</td></tr> <tr> <td>Format:</td><td>U0.16</td></tr> </table> <p>The calculation result of <math>1 / (\text{BC3} - \text{BC2})</math> [1/62]</p>	Default Value:	744	Format:	U0.16
Default Value:	744					
Format:	U0.16					
	15:0	<b>ColorTransitSlope2</b> <table border="1"> <tr> <td>Default Value:</td><td>405</td></tr> <tr> <td>Format:</td><td>U0.16</td></tr> </table> <p>The calculation result of <math>1 / (\text{BC2} - \text{BC1})</math> [1/57]</p>	Default Value:	405	Format:	U0.16
Default Value:	405					
Format:	U0.16					
5	31:16	<b>ColorTransitSlope45</b> <table border="1"> <tr> <td>Default Value:</td><td>407</td></tr> <tr> <td>Format:</td><td>U0.16</td></tr> </table> <p>The calculation result of <math>1 / (\text{BC5} - \text{BC4})</math> [1/57]</p>	Default Value:	407	Format:	U0.16
Default Value:	407					
Format:	U0.16					
	15:0	<b>ColorTransitSlope34</b> <table border="1"> <tr> <td>Default Value:</td><td>1131</td></tr> <tr> <td>Format:</td><td>U0.16</td></tr> </table> <p>The calculation result of <math>1 / (\text{BC4} - \text{BC3})</math> [1/61]</p>	Default Value:	1131	Format:	U0.16
Default Value:	1131					
Format:	U0.16					
6	31:16	<b>ColorTransitSlope61</b> <table border="1"> <tr> <td>Default Value:</td><td>377</td></tr> <tr> <td>Format:</td><td>U0.16</td></tr> </table> <p>The calculation result of <math>1 / (\text{BC1} - \text{BC6})</math> [1/62]</p>	Default Value:	377	Format:	U0.16
Default Value:	377					
Format:	U0.16					
	15:0	<b>ColorTransitSlope56</b> <table border="1"> <tr> <td>Default Value:</td><td>372</td></tr> <tr> <td>Format:</td><td>U0.16</td></tr> </table> <p>The calculation result of <math>1 / (\text{BC6} - \text{BC5})</math> [1/62]</p>	Default Value:	372	Format:	U0.16
Default Value:	372					
Format:	U0.16					

<b>VEBOX_TCC_STATE</b>			
7	31:22	<b>ColorBias3</b>	
		Default Value:	0
		Format:	U2.8
		Color bias for BaseColor3.	
8	21:12	<b>ColorBias2</b>	
		Default Value:	150
		Format:	U2.8
		Color bias for BaseColor2. The default is 150/256	
	11:2	<b>ColorBias1</b>	
		Default Value:	0
		Format:	U2.8
		Color bias for BaseColor1.	
	1:0	<b>Reserved</b>	
	1:0	Format:	MBZ
9	31:22	<b>ColorBias6</b>	
		Default Value:	0
		Format:	U2.8
		Color bias for BaseColor6.	
	21:12	<b>ColorBias5</b>	
		Default Value:	0
		Format:	U2.8
		Color bias for BaseColor5.	
	11:2	<b>ColorBias4</b>	
		Default Value:	0
		Format:	U2.8
		Color bias for BaseColor4.	
	1:0	<b>Reserved</b>	
	1:0	Format:	MBZ
9	31	<b>Reserved</b>	
9	31	Format:	MBZ

VEBOX_TCC_STATE			
	30:24	<b>UV Threshold</b>	
		Default Value:	3
		Format:	U7
		Low UV threshold.	
	23:19	<b>Reserved</b>	
		Format:	MBZ
	18:16	<b>UV Threshold Bits</b>	
		Default Value:	3
		Format:	U3
		Low UV transition width bits.	
	15:13	<b>Reserved</b>	
		Format:	MBZ
	12:8	<b>STE Threshold</b>	
		Default Value:	0
		Format:	U5
		Skin tone pixels enhancement threshold.	
	7:3	<b>Reserved</b>	
		Format:	MBZ
	2:0	<b>STE Slope Bits</b>	
		Default Value:	0
		Format:	U3
		Skin tone pixels enhancement slope bits.	
10	31:16	<b>Inv_UVMaxColor</b>	
		Default Value:	146
		Format:	U16
		1 / UVMaxColor. Used for the SFs2 calculation.	
	15:9	<b>Reserved</b>	
		Format:	MBZ
	8:0	<b>UVMaxColor</b>	
		Default Value:	448
		Format:	U9
		The maximum absolute value of the legal UV pixels. Used for the SFs2 calculation.	

# VEBOX VERTEX TABLE

# VEBOX VERTEX TABLE

DWord	Bit	Description					
0..511	31:28	<b>Reserved</b> Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td></td><td>MBZ</td></tr></table>		MBZ			
	MBZ						
27:16	<b>Vertex table entry 0 - Lv (12 bits)</b> <table border="1" style="width: 100%;"><thead><tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr></thead><tbody><tr> <td>100h-ED6h</td> <td></td> <td>Range for Vertices BT601 and BT709</td> </tr></tbody></table>	Value	Name	Description	100h-ED6h		Range for Vertices BT601 and BT709
Value	Name	Description					
100h-ED6h		Range for Vertices BT601 and BT709					
15:12	<b>Reserved</b> Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td></td><td>MBZ</td></tr></table>		MBZ				
	MBZ						
11:0	<b>Vertex table entry 0 - Cv (12 bits)</b> <table border="1" style="width: 100%;"><thead><tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr></thead><tbody><tr> <td>400h-A00h</td> <td></td> <td>Range for Vertices BT601 and BT709</td> </tr></tbody></table>	Value	Name	Description	400h-A00h		Range for Vertices BT601 and BT709
Value	Name	Description					
400h-A00h		Range for Vertices BT601 and BT709					

## VECS Hardware-Detected Error Bit Definitions

VECS Hardware-Detected Error Bit Definitions							
DWord	Bit	Description					
0	15:3	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ			
Format:	MBZ						
2	<p><b>Command Privilege Violation Error</b></p> <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> </table> <p>This bit is set if a command classified as privileged is parsed in a non-privileged batch buffer. The command will be converted to a NOOP and parsing will continue.</p>	Project:	BDW				
Project:	BDW						
1	<p><b>Reserved</b></p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ				
Format:	MBZ						
0	<p><b>Instruction Error</b></p> <p>This bit is set when the Renderer Instruction Parser detects an error while parsing an instruction. Instruction errors include:</p> <ul style="list-style-type: none"> <li>• Client ID value (Bits 31:29 of the Header) is not supported (only MI, 2D and 3D are supported).</li> <li>• Defeatured MI Instruction Opcodes:</li> </ul> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>1</td> <td></td> <td>Instruction Error detected</td> </tr> </tbody> </table> <p><b>Programming Notes</b></p> <p>This error indications cannot be cleared except by reset (i.e., it is a fatal error).</p>	Value	Name	Description	1		Instruction Error detected
Value	Name	Description					
1		Instruction Error detected					

## VERTEX\_BUFFER\_STATE

VERTEX_BUFFER_STATE										
DWord	Bit	Description								
0	31:26	<p><b>Vertex Buffer Index</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U6 index</td> </tr> </table> <p>This field contains an index value which selects the VB state being defined.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>[0,32]</td> <td></td> </tr> </tbody> </table>	Project:	All	Format:	U6 index	Value	Name	[0,32]	
Project:	All									
Format:	U6 index									
Value	Name									
[0,32]										
This structure is used in 3DSTATE_VERTEX_BUFFERS to set the state associated with a VB. The VF function will use this state to determine how/where to extract vertex element data for all vertex elements associated with the VB.										
25:23		<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	All	Format:	MBZ				
Project:	All									
Format:	MBZ									
22:16		<p><b>Memory Object Control State</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td><b>MEMORY_OBJECT_CONTROL_STATE</b></td> </tr> </table> <p>Specifies the memory object control state for this vertex buffer.</p>	Project:	All	Format:	<b>MEMORY_OBJECT_CONTROL_STATE</b>				
Project:	All									
Format:	<b>MEMORY_OBJECT_CONTROL_STATE</b>									
15		<p><b>Reserved</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	All	Format:	MBZ				
Project:	All									
Format:	MBZ									
14		<p><b>Address Modify Enable</b></p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> </table> <p>If set, the Buffer Starting Address field is used to update the state of this buffer. If clear, that field is ignored and the previously-programmed value is maintained.</p>	Project:	All						
Project:	All									

## VERTEX BUFFER STATE

		<b>Null Vertex Buffer</b>						
	13	<table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>Enable</td></tr> </table> <p>This field enabled causes any fetch for vertex data to return 0.</p>	Project:	All	Format:	Enable		
Project:	All							
Format:	Enable							
		<b>Programming Notes</b>						
		VERTEX_BUFFER_STATE.Null Vertex Buffer must be set when the VERTEX_BUFFER_STATE.Buffer Size is 0x0.						
	12	<b>Reserved</b>						
		<table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	All	Format:	MBZ		
Project:	All							
Format:	MBZ							
	11:0	<b>Buffer Pitch</b>						
		<table border="1"> <tr> <td>Format:</td><td>U12 Count of bytes</td></tr> </table> <p>This field specifies the pitch in bytes of the structures accessed within the VB. This information is required in order to access elements in the VB via a structure index.</p>	Format:	U12 Count of bytes				
Format:	U12 Count of bytes							
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>[0,2048]</td><td></td><td>Bytes</td></tr> </tbody> </table>	Value	Name	Description	[0,2048]		Bytes
Value	Name	Description						
[0,2048]		Bytes						
		<b>Programming Notes</b>						
		<ul style="list-style-type: none"> <li>• Different VERTEX_BUFFER_STATE structures can refer to the same memory region using different Buffer Pitch values.</li> <li>• See note on 64-bit float alignment in Buffer Starting Address.</li> </ul>						
1..2	63:0	<b>Buffer Starting Address</b>						
		<table border="1"> <tr> <td>Format:</td><td>GraphicsAddress[63:0]Vertex_Buffer</td></tr> </table> <p>This field contains the byte-aligned Graphics Address LSBs of the first element of interest within the VB. Software must program this value with the combination (sum) of the base address of the memory resource and the byte offset from the base address to the starting structure within the buffer. If the Address ModifyEnable bit is clear, this field is ignored and the previous value of Buffer Starting Address for this buffer is maintained.</p>	Format:	GraphicsAddress[63:0]Vertex_Buffer				
Format:	GraphicsAddress[63:0]Vertex_Buffer							
		<b>Programming Notes</b>						
		<ul style="list-style-type: none"> <li>• 64-bit floating point values must be 64-bit aligned in memory, or UNPREDICTABLE data will be fetched. When accessing an element containing 64-bit floating point values, the Buffer Starting Address and Source Element Offset values must add to a 64-bit aligned address, and BufferPitch must be a multiple of 64-bits.</li> <li>• VBs can only be allocated in linear (not tiled) graphics memory.</li> <li>• As computed index values are, by definition, interpreted as unsigned values, there is no issue with accesses to locations before (lower address value) the start of the buffer. However, these wrapped indices are subject to Max Index checking (see below).</li> </ul>						

## VERTEX\_BUFFER\_STATE

3	31:0	<b>Buffer Size</b>				
		<table border="1"><tr><td>Format:</td><td>U32 Count of bytes</td></tr></table>	Format:	U32 Count of bytes		
Format:	U32 Count of bytes					
<p>This field specifies the size of the buffer in bytes. Vertex element accesses which straddle or go past the end of the buffer will return 0's for all elements. Note that BufferSize=0 indicates that there is no valid data in the buffer.</p> <table border="1"><thead><tr><th>Value</th><th>Name</th></tr></thead><tbody><tr><td>[0, FFFFFFFFh]</td><td></td></tr></tbody></table>			Value	Name	[0, FFFFFFFFh]	
Value	Name					
[0, FFFFFFFFh]						

## VERTEX\_ELEMENT\_STATE

VERTEX_ELEMENT_STATE	
Project:	All
Source:	RenderCS
Size (in bits):	64
Default Value:	0x00000000, 0x00000000
Description	
<p>This structure is used in 3DSTATE_VERTEX_ELEMENTS to set the state associated with a vertex element. A vertex element is defined as an entity supplying from one to four DWord vertex components, to be stored in the vertex URB entry.</p>	
<p>The number of supported vertex elements is 34.</p>	
<p>The VF function will use this state, and possibly the state of the associated vertex buffer, to fetch/generate the source vertex element data, perform any required format conversions, padding with zeros, and store the resulting destination vertex element data into the vertex URB entry.</p>	
Programming Notes	
<ul style="list-style-type: none"> <li>• The (new) 3DSTATE_VF_SGVS command is used to specify optional insertion of VertexID and/or InstanceID into the input vertex data, logically following the processing of the VERTEX_ELEMENT_STATE structures. The VFCOMP_STORE_VID/IID encodings are no longer available in VERTEX_ELEMENT_STATE.</li> <li>• When SourceElementFormat is set to one of the *64*_PASSTHRU formats, 64-bit components are stored in the URB without any conversion. In this case, vertex elements must be written as 128 or 256 bits, with VFCOMP_STORE_0 being used to pad the output as required. E.g., if R64_PASSTHRU is used to copy a 64-bit Red component into the URB, Component 1 must be specified as VFCOMP_STORE_0 (with Components 2,3 set to VFCOMP_NOSTORE) in order to output a 128-bit vertex element, or Components 1-3 must be specified as VFCOMP_STORE_0 in order to output a 256-bit vertex element. Likewise, use of R64G64B64_PASSTHRU requires Component 3 to be specified as VFCOMP_STORE_0 in order to output a 256-bit vertex element.</li> <li>• When SourceElementFormat is set to one of the *64*_PASSTHRU formats then VFCOMP_STORE_SRC must be used for every valid component.</li> <li>• Any SourceElementFormat of *64*_PASSTHRU cannot be used with an element which has edge flag enabled.</li> </ul>	
<p>The SourceElementFormat needs to be a single-component format with an element which has edge flag enabled.</p>	

DWord	Bit	Description													
0	31:26	<p><b>Vertex Buffer Index</b></p> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>U6</td></tr> </table> <p>This field specifies which vertex buffer the element is sourced from.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>[0,32]</td><td>Up to 33 VBs are supported</td></tr> </tbody> </table> <p><b>Programming Notes</b></p> <p>It is possible for a vertex element to include only internally-generated data (VertexID, etc.), in which case the associated vertex buffer state is ignored.</p>	Project:	BDW	Format:	U6	Value	Name	[0,32]	Up to 33 VBs are supported					
Project:	BDW														
Format:	U6														
Value	Name														
[0,32]	Up to 33 VBs are supported														
	25	<p><b>Valid</b></p> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>Boolean</td></tr> </table> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>1h</td><td>TRUE</td><td>this vertex element is used in vertex assembly</td></tr> <tr> <td>0h</td><td>FALSE</td><td>this vertex element is not used.</td></tr> </tbody> </table>	Project:	BDW	Format:	Boolean	Value	Name	Description	1h	TRUE	this vertex element is used in vertex assembly	0h	FALSE	this vertex element is not used.
Project:	BDW														
Format:	Boolean														
Value	Name	Description													
1h	TRUE	this vertex element is used in vertex assembly													
0h	FALSE	this vertex element is not used.													
	24:16	<p><b>Source Element Format</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td><b>SURFACE FORMAT</b></td></tr> </table> <p>Range: Valid formats are found in the 3D Primitive Processing FormatConversion portion of the vertex fetch chapter.</p> <p>Format: The encoding of this field is identical the Surface Format field of the SURFACE_STATE structure, as described in the Sampler chapter.</p> <p>This field specifies the format in which the memory-resident source data for this particular vertex element is stored in the memory buffer. This only applies to elements stored with VFCOMP_STORE_SRC component control. (All other component types have an explicit format).</p>	Project:	All	Format:	<b>SURFACE FORMAT</b>									
Project:	All														
Format:	<b>SURFACE FORMAT</b>														
	15	<p><b>Edge Flag Enable</b></p> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>Enable</td></tr> </table> <p><b>Description</b></p> <p>When ENABLED, the source element is interpreted as an EdgeFlag for the vertex. If the source element is zero, the EdgeFlag will be set to FALSE. If the source element is non-zero, the EdgeFlag will be set to TRUE. The EdgeFlag bit will travel down the fixed function pipeline along with the vertex handle, etc. and not be stored in the vertex data like the other vertex elements. Refer to the fixed function descriptions for how this EdgeFlag affects rendering.</p> <p>Edge flags are supported for the following primitive topology types only, otherwise EdgeFlagEnable must not be ENABLED.</p>	Project:	BDW	Format:	Enable									
Project:	BDW														
Format:	Enable														

## VERTEX\_ELEMENT\_STATE

		<ul style="list-style-type: none"> <li>• 3DPRIM_TRILIST*</li> <li>• 3DPRIM_TRISTRIP*</li> <li>• 3DPRIM_TRIFAN*</li> <li>• 3DPRIM_POLYGON</li> </ul> <p>If this bit is DISABLED for all valid VERTEX_ELEMENTS, the vertex will be assigned a default EdgeFlag of TRUE.</p> <p>Edge flags are supported for all primitive topology types.</p>								
		<p style="text-align: center;"><b>Programming Notes</b></p> <ul style="list-style-type: none"> <li>• This bit must only be ENABLED on the last valid VERTEX_ELEMENT structure.</li> <li>• When set, Component 0 Control must be set to VFCOMP_STORE_SRC, and Component 1-3 Control must be set to VFCOMP_NOSTORE.</li> </ul>								
14:12	<b>Reserved</b>	<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	All	Format:	MBZ				
Project:	All									
Format:	MBZ									
11:0	<b>Source Element Offset</b>	<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>U12 byte offset</td> </tr> </table> <p>Byte offset of the source vertex element data in the structures comprising the vertex buffer.</p> <table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>[0,2047]</td> <td></td> </tr> </tbody> </table>	Project:	All	Format:	U12 byte offset	Value	Name	[0,2047]	
Project:	All									
Format:	U12 byte offset									
Value	Name									
[0,2047]										
		<p style="text-align: center;"><b>Programming Notes</b></p> <p>See note on 64-bit float alignment in Buffer Starting Address.</p>								
1	31	<b>Reserved</b>								
		<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	All	Format:	MBZ				
Project:	All									
Format:	MBZ									
	30:28	<b>Component 0 Control</b>								
		<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td><b>3D_Vertex_Component_Control</b></td> </tr> </table> <p>Refer to the 3D_Vertex_Component_Control table below</p>	Project:	All	Format:	<b>3D_Vertex_Component_Control</b>				
Project:	All									
Format:	<b>3D_Vertex_Component_Control</b>									
	27	<b>Reserved</b>								
		<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	All	Format:	MBZ				
Project:	All									
Format:	MBZ									

## VERTEX\_ELEMENT\_STATE

<b>VERTEX_ELEMENT_STATE</b>		
26:24	<b>Component 1 Control</b>	
	Format:	<b>3D_Vertex_Component_Control</b>
	Refer to the 3D_Vertex_Component_Control table below	
23	<b>Reserved</b>	
	Project:	All
	Format:	MBZ
22:20	<b>Component 2 Control</b>	
	Format:	<b>3D_Vertex_Component_Control</b>
	Refer to the 3D_Vertex_Component_Control table below	
19	<b>Reserved</b>	
	Project:	All
	Format:	MBZ
18:16	<b>Component 3 Control</b>	
	Format:	<b>3D_Vertex_Component_Control</b>
	Refer to the 3D_Vertex_Component_Control table below	
15:8	<b>Reserved</b>	
	Project:	All
	Format:	MBZ
7:0	<b>Reserved</b>	
	Project:	
	Format:	MBZ

## Vertical Line Stride Override Message Descriptor Control Field

### MDC\_VLSO - Vertical Line Stride Override Message Descriptor Control Field

Project: BDW  
Size (in bits): 3  
Default Value: 0x00000000

DWord	Bit	Description				
0	2	<p><b>Vertical Line Stride Override</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>Enable</td></tr> </table> <p>If set, override the Vertical Line Stride and Vertical Line Stride Offset fields in the surface state with the fields below.</p>	Project:	All	Format:	Enable
Project:	All					
Format:	Enable					
	1	<p><b>Vertical Line Stride</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U1</td></tr> </table> <p>Specifies number of lines (0 or 1) to skip between logically adjacent lines - provides support of interleaved (field) surfaces as textures.</p>	Project:	All	Format:	U1
Project:	All					
Format:	U1					
	0	<p><b>Vertical Line Stride Offset</b></p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U1</td></tr> </table> <p>Specifies the offset of the initial line from the beginning of the buffer. Ignored when Override VerticalLine Stride is 0.</p>	Project:	All	Format:	U1
Project:	All					
Format:	U1					

## VFE\_STATE\_EX

<b>VFE_STATE_EX</b>			
<b>DWord</b>	<b>Bit</b>	<b>Description</b>	
0	31:8	<b>Reserved</b>	
	7:0	<b>Reserved</b>	Format: MBZ
1	31:0	<b>VFE Control</b> This field is used by VFE depending on the mode of operation. See the following tables for details. If VFE Mode = AVC-IT or AVC-MC, this field is valid as defined in Table 1 13. If VFE Mode = VC1-IT, this field is valid as defined in Table 1 14. Otherwise, this field is reserved.	
2	31:0	<b>Interface Descriptor Remap Table</b> This field contains the interface descriptor remap table entries for the first 8 kernel indices. Each table entry has 4 bits, providing a remapping range of [0, 15]. The input of this table is the Interface Descriptor Offset within the MEDIA_OBJECT or MEDIA_OBJECT_EX command. As the table is limited to map the first 16 values, any Interface Descriptor Offset greater than 15 is not remapped. Bits 31:28: Remap for index = 7 Bits 27:24: Remap for index = 6 Bits 23:20: Remap for index = 5 Bits 19:16: Remap for index = 4 Bits 15:12: Remap for index = 3 Bits 11:8: Remap for index = 2 Bits 7:4: Remap for index = 1 Bits 3:0: Remap for index = 0	
3	31:0	<b>Interface Descriptor Remap Table (cont)</b> This field contains the interface descriptor remap table entries for the next 8 kernel indices (index = 8...15). Each table entry has 4 bits, providing a remapping range of [0, 15]. Bits 31:28: Remap for index = 15 Bits 27:24: Remap for index = 14 Bits 23:20: Remap for index = 13 Bits 19:16: Remap for index = 12 Bits 15:12: Remap for index = 11 Bits 11:8: Remap for index = 10 Bits 7:4: Remap for index = 9 Bits 3:0: Remap for index = 8	

VFE_STATE_EX									
4	31	<b>Scoreboard Enable</b>							
		Project:							
		This field enables and disables the hardware scoreboard in the Media Pipeline. If this field is cleared, hardware ignores the following scoreboard state fields.							
		This should be enabled at all times in the state and the scoreboard enable field in the MEDIA_OBJECT command should be use instead. If this field is disabled, the scratch space pointer calculation will be incorrect and any attempt to use the scoreboard later will result in a hardware hang.							
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0</td><td>Scoreboard disabled</td></tr> <tr> <td>1</td><td>Scoreboard enabled</td></tr> </tbody> </table>	Value	Name	0	Scoreboard disabled	1	Scoreboard enabled	
Value	Name								
0	Scoreboard disabled								
1	Scoreboard enabled								
	30	<b>Scoreboard Type</b>							
		Project:							
		This field selects the type of scoreboard in use.							
		This field must be zero (stalling scoreboard)							
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0</td><td>Stalling Scoreboard</td></tr> <tr> <td>1</td><td>Reserved (for Non-stalling scoreboard)</td></tr> </tbody> </table>	Value	Name	0	Stalling Scoreboard	1	Reserved (for Non-stalling scoreboard)	
Value	Name								
0	Stalling Scoreboard								
1	Reserved (for Non-stalling scoreboard)								
	29:8	<b>Reserved</b>							
		Format:	MBZ						
	7:0	<b>Scoreboard Mask</b>							
		Project:							
		Format:	Boolean						
		Each bit indicates the corresponding dependency scoreboard is enabled. The scoreboard is based on the relative (X, Y) distance from the current threads' (X, Y) position.							
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>[0,7]</td><td>Bit n</td><td>Score n is enabled</td></tr> </tbody> </table>	Value	Name	Description	[0,7]	Bit n	Score n is enabled	
Value	Name	Description							
[0,7]	Bit n	Score n is enabled							
5	31:28	<b>Scoreboard 3 Delta Y</b>							
		Project:							
		Format:	S3						
		Relative vertical distance of the dependent instance assigned to scoreboard 3, in the form of 2's compliment.							

<b>VFE_STATE_EX</b>			
	27:24	<b>Scoreboard 3 Delta X</b>	
		Project:	
		Format:	S3
		Relative horizontal distance of the dependent instance assigned to scoreboard 3, in the form of 2's compliment.	
	23:16	<b>Scoreboard 2 Delta (X, Y)</b>	
		Project:	
	15:8	<b>Scoreboard 1 Delta (X, Y)</b>	
		Project:	
	7:0	<b>Scoreboard 0 Delta (X, Y)</b>	
		Project:	
6	31:24	<b>Scoreboard 7 Delta (X, Y)</b>	
		Project:	
	23:16	<b>Scoreboard 6 Delta (X, Y)</b>	
		Project:	
	15:8	<b>Scoreboard 5 Delta (X, Y)</b>	
		Project:	
	7:0	<b>Scoreboard 4 Delta (X, Y)</b>	
		Project:	
7	31:0	<b>Reserved</b>	
		Format:	MBZ

## VP8 Encoder StreamOut Format

VP8 Encoder StreamOut Format		
DWord	Bit	Description
0	31:24	<b>MbY</b> Format: <input type="text"/> U8
	23:16	<b>MbX</b> Format: <input type="text"/> U8
	15:8	<b>MbClock16</b> Format: <input type="text"/> U8
	7:3	<b>Reserved</b> Format: <input type="text"/> MBZ
	2	<b>MbRcFlag</b> Format: <input type="text"/> U1
	1	<b>MBLevelInterMBConformanceFlag</b> Format: <input type="text"/> U1
	0	<b>MBLevelIntraMBConformanceFlag</b> Format: <input type="text"/> U1
1	31:29	<b>Reserved</b> Format: <input type="text"/> MBZ
	28:16	<b>MB_Residual_BitCount</b> Format: <input type="text"/> U13
	15:13	<b>Reserved</b> Format: <input type="text"/> MBZ
	12:0	<b>MB_Total_BitCount</b> Format: <input type="text"/> U13
2	31:25	<b>Reserved</b> Format: <input type="text"/> MBZ
	24:0	<b>Cbp</b> Format: <input type="text"/> U25
3	31	<b>Reserved</b> Format: <input type="text"/> MBZ

VP8 Encoder StreamOut Format		
	30	<b>LastMbFlag</b>
		Format: U1
	29	<b>IntraMBFlag</b>
		Format: U1
	28:24	<b>MBType5Bits</b>
		Format: U5
	23:19	<b>Reserved</b>
		Format: MBZ
	18	<b>QindexClampHigh</b>
		Format: U1
	17	<b>QindexClampLow</b>
		Format: U1
	16	<b>CoeffClampStatus</b>
		Format: U1
	15:0	<b>Reserved</b>
		Format: MBZ

## WD Interrupt Bit Definition

WD Interrupt Bit Definition				
DWord	Bit	Description		
0	7	<p><b>Unused_Int_7</b></p> <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> </table> <p>These interrupts are currently unused.</p>	Project:	BDW
Project:	BDW			
	6	<p><b>WD_GTT_Fault</b></p> <p>This event occurs when a GTT fault is detected.</p>		
	5	<p><b>WD_Vblank</b></p> <p>This event occurs at the start of the WD internal vertical blank. This vertical blank starts at capsync and ends at framestart.</p>		
	4	<p><b>WD_Capture_sync</b></p> <p>This event occurs when WD counter reached the programmed frame time interval.</p>		
	3	<p><b>WD_Capturing</b></p> <p>This event occurs when WD capture starts to capture pixels.</p>		
	2	<p><b>WD_Capture_Complete</b></p> <p>This event occurs when WD capture completes for the current frame.</p>		
	1	<p><b>WD_TG_Late_Run</b></p> <p>This event occurs when capsync for the next frame occurred before WD completed capturing all the pixels in the previous frame.</p>		
	0	<p><b>Reserved</b></p>		