



Intel® Open Source HD Graphics and Intel Iris™ Graphics

Programmer's Reference Manual

For the 2014-2015 Intel Core™ Processors, Celeron™
Processors and Pentium™ Processors based on the "Broadwell"
Platform

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WD_IIR	1808
WD_IMR.....	1809
WD_PERF_CNT	1810
WD_QUICKCAP_CTRL	1811
WD_STATUS.....	1813
WD_STRIDE	1814
WD_SURF.....	1815
WD_TAIL_CFG	1816
WD_WNIC_MSG_ADDR	1817
WGBOX State Arbitration Priority Control	1818
WGBOX Video CSR 8	1819
WGBOX Video CSR 99	1820
WIDI LRA 0	1821
WIDI LRA 1	1822
WIDI TLB Control Register	1823
WM_LINETIME.....	1824

WM_LP	1826
WM_LP_SPR	1828
WM_MISC	1829
WM_PIPE	1830
WRID_VALID_REG0	1832
WRID_VALID_REG1	1833
WRID_VALID_REG2	1834
Write Watermark	1835
WRPLL_CTL	1836
ZTLB LRA 0	1839
ZTLB LRA 1	1840

Advanced Features Capabilities Identifier and Next Pointer

AFCIDNP_0_2_0_PCI - Advanced Features Capabilities Identifier and Next Pointer

Register Space:	PCI: 0/2/0			
Project:	BDW			
Default Value:	0x00000013			
Size (in bits):	16			
Address:	000A4h			
When this capability is linked into the list, the second function of the Internal Graphics Device can be reset independently of the first function.				
DWord	Bit	Description		
0	15:8	NEXT_PTR		
		<table border="1"> <tr> <td>Default Value:</td><td>0000000b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>This contains a pointer to next item in capabilities list. This is the final capability in the list and is hardwired to 00h.</p>	Default Value:	0000000b
Default Value:	0000000b			
Access:	RO			
	7:0	CAP_ID		
		<table border="1"> <tr> <td>Default Value:</td><td>00010011b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Hardwired value of 13h identifies that this PCI Function is capable of Advanced Features.</p>	Default Value:	00010011b
Default Value:	00010011b			
Access:	RO			

Advanced Features Control

AFCTL_0_2_0_PCI - Advanced Features Control						
DWord	Bit	Description				
0	0	<p>Initiate Function Level Reset</p> <table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W Set</td></tr> </table> <p>FLR Resettable A write of 1b initiates Function Level Reset (FLR). FLR requirements are defined in the PCI Express Base Specification. Registers and state information that do not apply to conventional PCI are exempt from the FLR requirements given there. Once written 1, FLR will be initiated. During FLR, a read will return 1's since device 2 reads abort. Once FLR completes, hardware will clear the bit to 0. If a local panel is powered on and configured to power down on reset, the FLR will typically take several hundred milliseconds to complete. The worst possible, although unrealistic, delay is 5 seconds.</p>	Default Value:	0b	Access:	R/W Set
Default Value:	0b					
Access:	R/W Set					

Advanced Features Length and Capabilities

AFLC_0_2_0_PCI - Advanced Features Length and Capabilities								
Register Space: PCI: 0/2/0 Project: BDW Default Value: 0x00000306 Size (in bits): 16 Address: 000A6h								
DWord	Bit	Description						
0	9	FLR Capability <table border="1"> <tr> <td>Default Value:</td><td>1b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> <tr> <td colspan="2">Hardwired to 1 to indicate support for Function Level Reset (FLR).</td></tr> </table>	Default Value:	1b	Access:	RO	Hardwired to 1 to indicate support for Function Level Reset (FLR).	
Default Value:	1b							
Access:	RO							
Hardwired to 1 to indicate support for Function Level Reset (FLR).								
8	TXP Capability <table border="1"> <tr> <td>Default Value:</td><td>1b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> <tr> <td colspan="2">Hardwired to 1 to indicate support for the Transactions Pending bit.</td></tr> </table>	Default Value:	1b	Access:	RO	Hardwired to 1 to indicate support for the Transactions Pending bit.		
Default Value:	1b							
Access:	RO							
Hardwired to 1 to indicate support for the Transactions Pending bit.								
7:0	Capability Length <table border="1"> <tr> <td>Default Value:</td><td>00000110b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> <tr> <td colspan="2">Hardwired to 06h to indicate the Advanced Features capability structure requires 6 bytes of configuration space.</td></tr> </table>	Default Value:	00000110b	Access:	RO	Hardwired to 06h to indicate the Advanced Features capability structure requires 6 bytes of configuration space.		
Default Value:	00000110b							
Access:	RO							
Hardwired to 06h to indicate the Advanced Features capability structure requires 6 bytes of configuration space.								

Advanced Features Status

AFSTS_0_2_0_PCI - Advanced Features Status		
DWord	Bit	Description
0	0	Transactions Pending
		Default Value:
		Access:
		1: The Function has issued one or more non-posted transactions which have not been completed, including non-posted transactions that a target has terminated with Retry. 0 (hardwired): All non-posted transactions have been completed.

Advanced Scheduler Reset Request Messages

ASSRREQ - Advanced Scheduler Reset Request Messages					
DWord	Bit	Description			
0	31:16	<p>Message Mask</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Message Mask In order to write to bits 15:0, the corresponding message mask bits must be written. For example, for bit 14 to be set, bit 30 needs to be 1 : 40004000</p>	Access:	RO	
Access:	RO				
15:4	<p>Reserved</p> <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Reserved</p>	Project:	BDW	Access:	RO
Project:	BDW				
Access:	RO				
3	<p>VINunit cmfxrst reset request message (2nd Vbox)</p> <table border="1"> <tr> <td>Access:</td> <td>R/W Set</td> </tr> </table> <p>CMFX Reset Request Message from the VINunit in 2nd Vbox: '1' : CMFX Reset Requested - This bit is cleared by the CP upon completion of the reset request '0' : CMFX Reset Not Requested</p>	Access:	R/W Set		
Access:	R/W Set				
2	<p>VINunit cmfxrst Reset Request message</p> <table border="1"> <tr> <td>Access:</td> <td>R/W Set</td> </tr> </table> <p>CMFX Reset Request Message from the VINunit: '1' : CMFX Reset Requested - This bit is cleared by the CP upon completion of the reset request '0' : CMFX Reset Not Requested</p>	Access:	R/W Set		
Access:	R/W Set				
1	<p>Render AS Reset Request Message</p> <table border="1"> <tr> <td>Access:</td> <td>R/W Set</td> </tr> </table> <p>Render AS Reset Request Message from the CSunit: '1' : Render AS Reset Requested - This bit is cleared by the CP upon completion of the reset request '0' : Render AS Reset Not Requested</p>	Access:	R/W Set		
Access:	R/W Set				

ASSRREQ - Advanced Scheduler Reset Request Messages

	0	Media AS Reset Request Message
		Access: R/W Set
		Media AS Reset Request Message from the VCSunit: '1' : Media AS Reset Requested - This bit is cleared by the CP upon completion of the reset request '0' : Media AS Reset Not Requested

Aggregate Perf Counter A0

OAPERF_A0 - Aggregate Perf Counter A0		
DWord	Bit	Description
0	31:0	<p>Considerations</p> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>
This register reflects the count value of the OA Performance counter A0. DefaultValue="00000000h"		

Aggregate Perf Counter A0 Upper DWord

OAPERF_A0_UPPER - Aggregate Perf Counter A0 Upper DWord

Register Space: MMIO: 0/2/0

Project: BDW

Default Value: 0x00000000

Access: R/W

Size (in bits): 32

Address: 02804h

This register enables the current live value of performance counter A0 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description			
0	31:8	Reserved	<table border="1"> <tr> <td>Format:</td> <td>PBC</td> </tr> </table>	Format:	PBC
Format:	PBC				
7:0	Upper Value	<table border="1"> <tr> <td>Format:</td> <td>U8</td> </tr> </table> <p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U8	
Format:	U8				

Aggregate Perf Counter A1

OAPERF_A1 - Aggregate Perf Counter A1		
Register Space: MMIO: 0/2/0		
Project: BDW		
Default Value: 0x00000000		
Access: R/W		
Size (in bits): 32		
Address: 02808h		
Valid Projects: [BDW]		
This register reflects the count value of the OA Performance counter A1. DefaultValue="00000000h"		
DWord	Bit	Description
0	31:0	<p>Considerations</p> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>

Aggregate Perf Counter A1 Upper DWord

OAPERF_A1_UPPER - Aggregate Perf Counter A1 Upper DWord

Register Space: MMIO: 0/2/0

Project: BDW

Default Value: 0x00000000

Access: R/W

Size (in bits): 32

Address: 0280Ch

This register enables the current live value of performance counter A1 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description	
0	31:8	Reserved	Format: PBC
	7:0	Upper Value	Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A2

OAPERF_A2 - Aggregate Perf Counter A2		
Register Space: MMIO: 0/2/0		
Project: BDW		
Default Value: 0x00000000		
Access: R/W		
Size (in bits): 32		
Address: 02810h		
This register reflects the count value of the OA Performance counter A2. DefaultValue="00000000h"		
DWord	Bit	Description
0	31:0	Considerations This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A2 Upper DWord

OAPERF_A2_UPPER - Aggregate Perf Counter A2 Upper DWord

Register Space: MMIO: 0/2/0

Project: BDW

Default Value: 0x00000000

Access: R/W

Size (in bits): 32

Address: 02814h

This register enables the current live value of performance counter A2 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description			
0	31:8	Reserved	<table border="1"> <tr> <td>Format:</td> <td>PBC</td> </tr> </table>	Format:	PBC
Format:	PBC				
7:0	Upper Value	<table border="1"> <tr> <td>Format:</td> <td>U8</td> </tr> </table> <p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U8	
Format:	U8				

Aggregate Perf Counter A3

OAPERF_A3 - Aggregate Perf Counter A3		
DWord	Bit	Description
0	31:0	<p>Considerations</p> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>
This register reflects the count value of the OA Performance counter A3. DefaultValue="00000000h"		

Aggregate Perf Counter A3 Upper DWord

OAPERF_A3_UPPER - Aggregate Perf Counter A3 Upper DWord

Register Space: MMIO: 0/2/0

Project: BDW

Default Value: 0x00000000

Access: R/W

Size (in bits): 32

Address: 0281Ch

This register enables the current live value of performance counter A3 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description	
0	31:8	Reserved	Format: PBC
	7:0	Upper Value	Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A4

OAPERF_A4 - Aggregate Perf Counter A4		
Register Space: MMIO: 0/2/0		
Project: BDW		
Default Value: 0x00000000		
Access: R/W		
Size (in bits): 32		
Address: 02820h		
This register reflects the count value of the OA Performance counter A4. DefaultValue="00000000h"		
DWord	Bit	Description
0	31:0	Considerations This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A4 Upper DWord

OAPERF_A4_UPPER - Aggregate Perf Counter A4 Upper DWord

Register Space: MMIO: 0/2/0

Project: BDW

Default Value: 0x00000000

Access: R/W

Size (in bits): 32

Address: 02824h

This register enables the current live value of performance counter A4 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description	
0	31:8	Reserved	Format: PBC
	7:0	Upper Value	Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A5

OAPERF_A5 - Aggregate Perf Counter A5		
DWord	Bit	Description
0	31:0	<p>Considerations</p> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>
This register reflects the count value of the OA Performance counter A5. DefaultValue="00000000h"		

Aggregate Perf Counter A5 Upper DWord

OAPERF_A5_UPPER - Aggregate Perf Counter A5 Upper DWord

Register Space: MMIO: 0/2/0

Project: BDW

Default Value: 0x00000000

Access: R/W

Size (in bits): 32

Address: 0282Ch

This register enables the current live value of performance counter A5 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description	
0	31:8	Reserved	Format: PBC
	7:0	Upper Value	Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A6

OAPERF_A6 - Aggregate Perf Counter A6		
Register Space: MMIO: 0/2/0		
DWord	Bit	Description
0	31:0	<p>Considerations</p> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>

Aggregate Perf Counter A6 Upper DWord

OAPERF_A6_UPPER - Aggregate Perf Counter A6 Upper DWord

Register Space: MMIO: 0/2/0

Project: BDW

Default Value: 0x00000000

Access: R/W

Size (in bits): 32

Address: 02834h

This register enables the current live value of performance counter A6 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description			
0	31:8	Reserved	<table border="1"> <tr> <td>Format:</td> <td>PBC</td> </tr> </table>	Format:	PBC
Format:	PBC				
7:0	Upper Value	<table border="1"> <tr> <td>Format:</td> <td>U8</td> </tr> </table> <p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U8	
Format:	U8				

Aggregate Perf Counter A7

OAPERF_A7 - Aggregate Perf Counter A7		
DWord	Bit	Description
0	31:0	<p>Considerations</p> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>
This register reflects the count value of the OA Performance counter A7. DefaultValue="00000000h"		

Aggregate Perf Counter A7 Upper DWord

OAPERF_A7_UPPER - Aggregate Perf Counter A7 Upper DWord

Register Space: MMIO: 0/2/0

Project: BDW

Default Value: 0x00000000

Access: R/W

Size (in bits): 32

Address: 0283Ch

This register enables the current live value of performance counter A7 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description	
0	31:8	Reserved	Format: PBC
	7:0	Upper Value	Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A8

OAPERF_A8 - Aggregate Perf Counter A8		
DWord	Bit	Description
0	31:0	<p>Considerations</p> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>
This register reflects the count value of the OA Performance counter A8. DefaultValue="00000000h"		

Aggregate Perf Counter A8 Upper DWord

OAPERF_A8_UPPER - Aggregate Perf Counter A8 Upper DWord

Register Space: MMIO: 0/2/0

Project: BDW

Default Value: 0x00000000

Access: R/W

Size (in bits): 32

Address: 02844h

This register enables the current live value of performance counter A8 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description			
0	31:8	Reserved	<table border="1"> <tr> <td>Format:</td> <td>PBC</td> </tr> </table>	Format:	PBC
Format:	PBC				
7:0	Upper Value	<table border="1"> <tr> <td>Format:</td> <td>U8</td> </tr> </table> <p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U8	
Format:	U8				

Aggregate Perf Counter A9

OAPERF_A9 - Aggregate Perf Counter A9		
DWord	Bit	Description
0	31:0	<p>Considerations</p> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>
This register reflects the count value of the OA Performance counter A9. DefaultValue="00000000h"		

Aggregate Perf Counter A9 Upper DWord

OAPERF_A9_UPPER - Aggregate Perf Counter A9 Upper DWord

Register Space: MMIO: 0/2/0

Project: BDW

Default Value: 0x00000000

Access: R/W

Size (in bits): 32

Address: 0284Ch

This register enables the current live value of performance counter A9 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description	
0	31:8	Reserved	Format: PBC
	7:0	Upper Value	Format: U8 This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Aggregate Perf Counter A10

OAPERF_A10 - Aggregate Perf Counter A10		
DWord	Bit	Description
0	31:0	<p>Considerations</p> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>
This register reflects the count value of the OA Performance counter A10. DefaultValue="0000000h"		

Aggregate Perf Counter A10 Upper DWord

OAPERF_A10_UPPER - Aggregate Perf Counter A10 Upper DWord				
DWord	Bit	Description		
0	31:8	<p>Reserved</p> <table border="1"> <tr> <td>Format:</td> <td>PBC</td> </tr> </table>	Format:	PBC
Format:	PBC			
7:0	<p>Upper Value</p> <table border="1"> <tr> <td>Format:</td> <td>U8</td> </tr> </table> <p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U8	
Format:	U8			

Aggregate Perf Counter A11

OAPERF_A11 - Aggregate Perf Counter A11		
DWord	Bit	Description
0	31:0	<p>Considerations</p> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>
This register reflects the count value of the OA Performance counter A11. DefaultValue="0000000h"		

Aggregate Perf Counter A11 Upper DWord

OAPERF_A11_UPPER - Aggregate Perf Counter A11 Upper DWord				
DWord	Bit	Description		
0	31:8	<p>Reserved</p> <table border="1"> <tr> <td>Format:</td> <td>PBC</td> </tr> </table>	Format:	PBC
Format:	PBC			
7:0	<p>Upper Value</p> <table border="1"> <tr> <td>Format:</td> <td>U8</td> </tr> </table> <p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U8	
Format:	U8			

Aggregate Perf Counter A12

OAPERF_A12 - Aggregate Perf Counter A12		
DWord	Bit	Description
0	31:0	<p>Considerations</p> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>
This register reflects the count value of the OA Performance counter A12. DefaultValue="0000000h"		

Aggregate Perf Counter A12 Upper DWord

OAPERF_A12_UPPER - Aggregate Perf Counter A12 Upper DWord				
DWord	Bit	Description		
0	31:8	<p>Reserved</p> <table border="1"> <tr> <td>Format:</td> <td>PBC</td> </tr> </table>	Format:	PBC
Format:	PBC			
7:0	<p>Upper Value</p> <table border="1"> <tr> <td>Format:</td> <td>U8</td> </tr> </table> <p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U8	
Format:	U8			

Aggregate Perf Counter A13

OAPERF_A13 - Aggregate Perf Counter A13		
DWord	Bit	Description
0	31:0	<p>Considerations</p> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>
This register reflects the count value of the OA Performance counter A13. DefaultValue="0000000h"		

Aggregate Perf Counter A13 Upper DWord

OAPERF_A13_UPPER - Aggregate Perf Counter A13 Upper DWord				
DWord	Bit	Description		
0	31:8	<p>Reserved</p> <table border="1"> <tr> <td>Format:</td> <td>PBC</td> </tr> </table>	Format:	PBC
Format:	PBC			
7:0	<p>Upper Value</p> <table border="1"> <tr> <td>Format:</td> <td>U8</td> </tr> </table> <p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U8	
Format:	U8			

Aggregate Perf Counter A14

OAPERF_A14 - Aggregate Perf Counter A14		
DWord	Bit	Description
0	31:0	<p>Considerations</p> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>
This register reflects the count value of the OA Performance counter A14. DefaultValue="0000000h"		

Aggregate Perf Counter A14 Upper DWord

OAPERF_A14_UPPER - Aggregate Perf Counter A14 Upper DWord				
DWord	Bit	Description		
0	31:8	<p>Reserved</p> <table border="1"> <tr> <td>Format:</td> <td>PBC</td> </tr> </table>	Format:	PBC
Format:	PBC			
7:0	<p>Upper Value</p> <table border="1"> <tr> <td>Format:</td> <td>U8</td> </tr> </table> <p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U8	
Format:	U8			

Aggregate Perf Counter A15

OAPERF_A15 - Aggregate Perf Counter A15		
DWord	Bit	Description
0	31:0	<p>Considerations</p> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>
This register reflects the count value of the OA Performance counter A15. DefaultValue="0000000h"		

Aggregate Perf Counter A15 Upper DWord

OAPERF_A15_UPPER - Aggregate Perf Counter A15 Upper DWord				
DWord	Bit	Description		
0	31:8	<p>Reserved</p> <table border="1"> <tr> <td>Format:</td> <td>PBC</td> </tr> </table>	Format:	PBC
Format:	PBC			
7:0	<p>Upper Value</p> <table border="1"> <tr> <td>Format:</td> <td>U8</td> </tr> </table> <p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U8	
Format:	U8			

Aggregate Perf Counter A16

OAPERF_A16 - Aggregate Perf Counter A16		
DWord	Bit	Description
0	31:0	<p>Considerations</p> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>
This register reflects the count value of the OA Performance counter A16. DefaultValue="0000000h"		

Aggregate Perf Counter A16 Upper DWord

OAPERF_A16_UPPER - Aggregate Perf Counter A16 Upper DWord				
DWord	Bit	Description		
0	31:8	<p>Reserved</p> <table border="1"> <tr> <td>Format:</td> <td>PBC</td> </tr> </table>	Format:	PBC
Format:	PBC			
7:0	<p>Upper Value</p> <table border="1"> <tr> <td>Format:</td> <td>U8</td> </tr> </table> <p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U8	
Format:	U8			

Aggregate Perf Counter A17

OAPERF_A17 - Aggregate Perf Counter A17		
DWord	Bit	Description
0	31:0	<p>Considerations</p> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>
This register reflects the count value of the OA Performance counter A17. DefaultValue="0000000h"		

Aggregate Perf Counter A17 Upper DWord

OAPERF_A17_UPPER - Aggregate Perf Counter A17 Upper DWord				
Register Space:	MMIO: 0/2/0			
Project:	BDW			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Address:	0288Ch			
<p>This register enables the current live value of performance counter A17 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>				
DWord	Bit	Description		
0	31:8	<p>Reserved</p> <table border="1"> <tr> <td>Format:</td> <td>PBC</td> </tr> </table>	Format:	PBC
Format:	PBC			
7:0	<p>Upper Value</p> <table border="1"> <tr> <td>Format:</td> <td>U8</td> </tr> </table> <p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U8	
Format:	U8			

Aggregate Perf Counter A18

OAPERF_A18 - Aggregate Perf Counter A18		
DWord	Bit	Description
0	31:0	<p>Considerations</p> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>
This register reflects the count value of the OA Performance counter A9. DefaultValue="00000000h"		

Aggregate Perf Counter A18 Upper DWord

OAPERF_A18_UPPER - Aggregate Perf Counter A18 Upper DWord				
DWord	Bit	Description		
0	31:8	<p>Reserved</p> <table border="1"> <tr> <td>Format:</td> <td>PBC</td> </tr> </table>	Format:	PBC
Format:	PBC			
7:0	<p>Upper Value</p> <table border="1"> <tr> <td>Format:</td> <td>U8</td> </tr> </table> <p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U8	
Format:	U8			

Aggregate Perf Counter A19

OAPERF_A19 - Aggregate Perf Counter A19		
Register Space: MMIO: 0/2/0		
DWord	Bit	Description
0	31:0	<p>Considerations</p> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>

Aggregate Perf Counter A19 Upper DWord

OAPERF_A19_UPPER - Aggregate Perf Counter A19 Upper DWord				
DWord	Bit	Description		
0	31:8	<p>Reserved</p> <table border="1"> <tr> <td>Format:</td> <td>PBC</td> </tr> </table>	Format:	PBC
Format:	PBC			
7:0	<p>Upper Value</p> <table border="1"> <tr> <td>Format:</td> <td>U8</td> </tr> </table> <p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U8	
Format:	U8			

Aggregate Perf Counter A20

OAPERF_A20 - Aggregate Perf Counter A20		
Register Space: MMIO: 0/2/0		
DWord	Bit	Description
0	31:0	<p>Considerations</p> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>

Aggregate Perf Counter A20 Upper DWord

OAPERF_A20_UPPER - Aggregate Perf Counter A20 Upper DWord				
Register Space:	MMIO: 0/2/0			
Project:	BDW			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Address:	028A4h			
<p>This register enables the current live value of performance counter A20 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>				
DWord	Bit	Description		
0	31:8	<p>Reserved</p> <table border="1"> <tr> <td>Format:</td> <td>PBC</td> </tr> </table>	Format:	PBC
Format:	PBC			
7:0	<p>Upper Value</p> <table border="1"> <tr> <td>Format:</td> <td>U8</td> </tr> </table> <p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U8	
Format:	U8			

Aggregate Perf Counter A21

OAPERF_A21 - Aggregate Perf Counter A21		
DWord	Bit	Description
0	31:0	<p>Considerations</p> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>
This register reflects the count value of the OA Performance counter A21. DefaultValue="0000000h"		

Aggregate Perf Counter A21 Upper DWord

OAPERF_A21_UPPER - Aggregate Perf Counter A21 Upper DWord				
Register Space:	MMIO: 0/2/0			
Project:	BDW			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Address:	028ACh			
<p>This register enables the current live value of performance counter A21 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>				
DWord	Bit	Description		
0	31:8	<p>Reserved</p> <table border="1"> <tr> <td>Format:</td> <td>PBC</td> </tr> </table>	Format:	PBC
Format:	PBC			
7:0	<p>Upper Value</p> <table border="1"> <tr> <td>Format:</td> <td>U8</td> </tr> </table> <p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U8	
Format:	U8			

Aggregate Perf Counter A22

OAPERF_A22 - Aggregate Perf Counter A22		
DWord	Bit	Description
0	31:0	<p>Considerations</p> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>
This register reflects the count value of the OA Performance counter A22. DefaultValue="0000000h"		

Aggregate Perf Counter A22 Upper DWord

OAPERF_A22_UPPER - Aggregate Perf Counter A22 Upper DWord				
DWord	Bit	Description		
0	31:8	<p>Reserved</p> <table border="1"> <tr> <td>Format:</td> <td>PBC</td> </tr> </table>	Format:	PBC
Format:	PBC			
7:0	<p>Upper Value</p> <table border="1"> <tr> <td>Format:</td> <td>U8</td> </tr> </table> <p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U8	
Format:	U8			

Aggregate Perf Counter A23

OAPERF_A23 - Aggregate Perf Counter A23		
DWord	Bit	Description
0	31:0	<p>Considerations</p> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>
This register reflects the count value of the OA Performance counter A23. DefaultValue="0000000h"		

Aggregate Perf Counter A23 Upper DWord

OAPERF_A23_UPPER - Aggregate Perf Counter A23 Upper DWord				
Register Space:	MMIO: 0/2/0			
Project:	BDW			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Address:	028BCh			
<p>This register enables the current live value of performance counter A23 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>				
DWord	Bit	Description		
0	31:8	<p>Reserved</p> <table border="1"> <tr> <td>Format:</td> <td>PBC</td> </tr> </table>	Format:	PBC
Format:	PBC			
7:0	<p>Upper Value</p> <table border="1"> <tr> <td>Format:</td> <td>U8</td> </tr> </table> <p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U8	
Format:	U8			

Aggregate Perf Counter A24

OAPERF_A24 - Aggregate Perf Counter A24		
DWord	Bit	Description
0	31:0	<p>Considerations</p> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>
This register reflects the count value of the OA Performance counter A24. DefaultValue="0000000h"		

Aggregate Perf Counter A24 Upper DWord

OAPERF_A24_UPPER - Aggregate Perf Counter A24 Upper DWord				
DWord	Bit	Description		
0	31:8	<p>Reserved</p> <table border="1"> <tr> <td>Format:</td> <td>PBC</td> </tr> </table>	Format:	PBC
Format:	PBC			
7:0	<p>Upper Value</p> <table border="1"> <tr> <td>Format:</td> <td>U8</td> </tr> </table> <p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U8	
Format:	U8			

Aggregate Perf Counter A25

OAPERF_A25 - Aggregate Perf Counter A25		
DWord	Bit	Description
0	31:0	<p>Considerations</p> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>
This register reflects the count value of the OA Performance counter A25. DefaultValue="0000000h"		

Aggregate Perf Counter A25 Upper DWord

OAPERF_A25_UPPER - Aggregate Perf Counter A25 Upper DWord				
DWord	Bit	Description		
0	31:8	<p>Reserved</p> <table border="1"> <tr> <td>Format:</td> <td>PBC</td> </tr> </table>	Format:	PBC
Format:	PBC			
7:0	<p>Upper Value</p> <table border="1"> <tr> <td>Format:</td> <td>U8</td> </tr> </table> <p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U8	
Format:	U8			

Aggregate Perf Counter A26

OAPERF_A26 - Aggregate Perf Counter A26		
DWord	Bit	Description
0	31:0	<p>Considerations</p> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>
This register reflects the count value of the OA Performance counter A26. DefaultValue="0000000h"		

Aggregate Perf Counter A26 Upper DWord

OAPERF_A26_UPPER - Aggregate Perf Counter A26 Upper DWord				
Register Space:	MMIO: 0/2/0			
Project:	BDW			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Address:	028D4h			
<p>This register enables the current live value of performance counter A26 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>				
DWord	Bit	Description		
0	31:8	<p>Reserved</p> <table border="1"> <tr> <td>Format:</td> <td>PBC</td> </tr> </table>	Format:	PBC
Format:	PBC			
7:0	<p>Upper Value</p> <table border="1"> <tr> <td>Format:</td> <td>U8</td> </tr> </table> <p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U8	
Format:	U8			

Aggregate Perf Counter A27

OAPERF_A27 - Aggregate Perf Counter A27		
DWord	Bit	Description
0	31:0	<p>Considerations</p> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>
This register reflects the count value of the OA Performance counter A27. DefaultValue="0000000h"		

Aggregate Perf Counter A27 Upper DWord

OAPERF_A27_UPPER - Aggregate Perf Counter A27 Upper DWord				
Register Space:	MMIO: 0/2/0			
Project:	BDW			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Address:	028DCh			
<p>This register enables the current live value of performance counter A27 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>				
DWord	Bit	Description		
0	31:8	<p>Reserved</p> <table border="1"> <tr> <td>Format:</td> <td>PBC</td> </tr> </table>	Format:	PBC
Format:	PBC			
7:0	<p>Upper Value</p> <table border="1"> <tr> <td>Format:</td> <td>U8</td> </tr> </table> <p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U8	
Format:	U8			

Aggregate Perf Counter A28

OAPERF_A28 - Aggregate Perf Counter A28		
DWord	Bit	Description
0	31:0	<p>Considerations</p> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>
This register reflects the count value of the OA Performance counter A28. DefaultValue="0000000h"		

Aggregate Perf Counter A28 Upper DWord

OAPERF_A28_UPPER - Aggregate Perf Counter A28 Upper DWord				
Register Space:	MMIO: 0/2/0			
Project:	BDW			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Address:	028E4h			
<p>This register enables the current live value of performance counter A28 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>				
DWord	Bit	Description		
0	31:8	<p>Reserved</p> <table border="1"> <tr> <td>Format:</td> <td>PBC</td> </tr> </table>	Format:	PBC
Format:	PBC			
7:0	<p>Upper Value</p> <table border="1"> <tr> <td>Format:</td> <td>U8</td> </tr> </table> <p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U8	
Format:	U8			

Aggregate Perf Counter A29

OAPERF_A29 - Aggregate Perf Counter A29		
DWord	Bit	Description
0	31:0	<p>Considerations</p> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>
This register reflects the count value of the OA Performance counter A29. DefaultValue="0000000h"		

Aggregate Perf Counter A29 Upper DWord

OAPERF_A29_UPPER - Aggregate Perf Counter A29 Upper DWord				
DWord	Bit	Description		
0	31:8	<p>Reserved</p> <table border="1"> <tr> <td>Format:</td> <td>PBC</td> </tr> </table>	Format:	PBC
Format:	PBC			
7:0	<p>Upper Value</p> <table border="1"> <tr> <td>Format:</td> <td>U8</td> </tr> </table> <p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U8	
Format:	U8			

Aggregate Perf Counter A30

OAPERF_A30 - Aggregate Perf Counter A30		
DWord	Bit	Description
0	31:0	<p>Considerations</p> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>
This register reflects the count value of the OA Performance counter A30. DefaultValue="0000000h"		

Aggregate Perf Counter A30 Upper DWord

OAPERF_A30_UPPER - Aggregate Perf Counter A30 Upper DWord				
Register Space:	MMIO: 0/2/0			
Project:	BDW			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Address:	028F4h			
<p>This register enables the current live value of performance counter A30 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>				
DWord	Bit	Description		
0	31:8	<p>Reserved</p> <table border="1"> <tr> <td>Format:</td> <td>PBC</td> </tr> </table>	Format:	PBC
Format:	PBC			
7:0	<p>Upper Value</p> <table border="1"> <tr> <td>Format:</td> <td>U8</td> </tr> </table> <p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U8	
Format:	U8			

Aggregate Perf Counter A31

OAPERF A31 - Aggregate Perf Counter A31						
DWord	Bit	Description				
0	31:0	<p>Considerations</p> <table border="1"> <tr> <td>Format:</td> <td>U32</td> </tr> <tr> <td colspan="2">This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</td></tr> </table>	Format:	U32	This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.	
Format:	U32					
This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.						
This register reflects the count value of the OA Performance counter A31						

Aggregate Perf Counter A31 Upper DWord

OAPERF_A31_UPPER - Aggregate Perf Counter A31 Upper DWord				
Register Space:	MMIO: 0/2/0			
Project:	BDW			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Address:	028FCh			
<p>This register enables the current live value of performance counter A31 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>				
DWord	Bit	Description		
0	31:8	<p>Reserved</p> <table border="1"> <tr> <td>Format:</td> <td>PBC</td> </tr> </table>	Format:	PBC
Format:	PBC			
7:0	<p>Upper Value</p> <table border="1"> <tr> <td>Format:</td> <td>U8</td> </tr> </table> <p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U8	
Format:	U8			

Aggregate_Perf_Counter_A32

OAPERF_A32 - Aggregate_Perf_Counter_A32						
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x00000000 Access: R/W Size (in bits): 32						
Address: 02900h Valid Projects: [BDW]						
This register reflects the count value of the OA Performance counter A32						
DWord	Bit	Description				
0	31:0	Considerations <table border="1"> <tr> <td>Format:</td><td>U32</td></tr> <tr> <td colspan="2">This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</td></tr> </table>	Format:	U32	This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.	
Format:	U32					
This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.						

Aggregate_Perf_Counter_A33

OAPERF_A33 - Aggregate_Perf_Counter_A33						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Access:	R/W					
Size (in bits):	32					
Address:	02904h					
Valid Projects:	[BDW]					
This register reflects the count value of the OA Performance counter A33						
DWord	Bit	Description				
0	31:0	<p>Considerations</p> <table border="1"> <tr> <td>Format:</td><td>U32</td></tr> <tr> <td colspan="2">This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</td></tr> </table>	Format:	U32	This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.	
Format:	U32					
This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.						

Aggregate_Perf_Counter_A34

OAPERF_A34 - Aggregate_Perf_Counter_A34				
DWord	Bit	Description		
0	31:0	<p>Considerations</p> <table border="1"> <tr> <td>Format:</td> <td>U32</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32
Format:	U32			

Aggregate_Perf_Counter_A35

OAPERF_A35 - Aggregate_Perf_Counter_A35				
DWord	Bit	Description		
0	31:0	<p>Considerations</p> <table border="1"> <tr> <td>Format:</td> <td>U32</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32
Format:	U32			
This register reflects the count value of the OA Performance counter A35				

All Engine Fault Register

FAULT_REG - All Engine Fault Register						
DWord	Bit	Description				
0	31:1	<p>All Engine Fault Register</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000000000000000000000000000b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Bit[31:15]: Reserved. Bit[14:12]: Engine ID: 000b - GFX. 001b - MFX0. 010b - MFX1. 011b - VEBX. 100b - BLT. 110b - WIDI. Bit[11]: Reserved. Bit[10:3]: SRCID of Fault. This is the Source ID of the unit that requested the cycle that generated the First Page fault for this engine. This value is locked and not updated on subsequent faults, until the valid bit of this register is cleared by SW. Bit[2:1]: Fault Type (GFX_FT): Type of Fault recorded: 00b - Invalid PTE Fault. 01b - Invalid PDE Fault. 10b - Invalid PDPE Fault. 11b - Invalid PML4E Fault. This value is locked and not updated on subsequent faults, until the valid bit of this register is cleared by SW. All bits are only valid with bit[0]=1.</p>	Default Value:	00000000000000000000000000000000b	Access:	R/W
Default Value:	00000000000000000000000000000000b					
Access:	R/W					
0	0	<p>Valid Bit</p> <table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>This bit indicates that the first fault for this engine has been recorded. It can only be cleared by SW, which also clears the other fields.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					

ARAT C6 Disallow Threshold

ARAT_C6DIS - ARAT C6 Disallow Threshold						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	0A178h					
DWord	Bit	Description				
0	31:0	<p>C6 Disallow Threshold for ARAT</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td colspan="2">Threshold, in 10ns increments to prevent short C6.</td></tr> </table>	Access:	R/W	Threshold, in 10ns increments to prevent short C6.	
Access:	R/W					
Threshold, in 10ns increments to prevent short C6.						

ARAT Delta (LSB)

ARAT_TDELTALOW - ARAT Delta (LSB)						
DWord	Bit	Description				
0	31:2	<p>Lower Bits of Delta Time for ARAT</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>Bits [31:2] of Delta Time, in 10ns increments. Bits 1:0 dropped. This means the granularity is 40ns increments. For example, [31:2]=b1 means the delta time is 40ns.</td><td></td> </tr> </table>	Access:	R/W	Bits [31:2] of Delta Time, in 10ns increments. Bits 1:0 dropped. This means the granularity is 40ns increments. For example, [31:2]=b1 means the delta time is 40ns.	
Access:	R/W					
Bits [31:2] of Delta Time, in 10ns increments. Bits 1:0 dropped. This means the granularity is 40ns increments. For example, [31:2]=b1 means the delta time is 40ns.						
1	<p>ARAT Mode</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>0b: One-Shot Mode (default). 1b: Periodic Mode.</td><td></td> </tr> </table>	Access:	R/W	0b: One-Shot Mode (default). 1b: Periodic Mode.		
Access:	R/W					
0b: One-Shot Mode (default). 1b: Periodic Mode.						
0	<p>ARAT Enable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>0b: ARAT Disabled (default). 1b: ARAT Enabled.</td><td></td> </tr> </table>	Access:	R/W	0b: ARAT Disabled (default). 1b: ARAT Enabled.		
Access:	R/W					
0b: ARAT Disabled (default). 1b: ARAT Enabled.						

ARAT Delta (MSB)

ARAT_TDELTA_HIGH - ARAT Delta (MSB)		
DWord	Bit	Description
0	23:0	Upper Bits of Delta Time for ARAT Access: R/W Bits [55:32] of Delta Time, in 10ns increments.

ARB_CTL

ARB_CTL											
Register Space: MMIO: 0/2/0 Project: BDW 0x16661056 [BDW] Access: R/W Size (in bits): 32											
Address: 45000h-45003h Name: Display Arbitration Control 1 ShortName: ARB_CTL Valid Projects: BDW Power: Always on Reset: soft											
DWord	Bit	Description									
0	31	Reserved									
	30	Reserved									
	29:26	HP Queue Watermark									
		<table border="1"> <tr> <td>Default Value:</td><td>0101b 6 entries</td></tr> <tr> <td>Project:</td><td>BDW</td></tr> </table> <p>The value in this register indicates the number of entries the high priority queue should have before it can be read. The value is zero based.</p>	Default Value:	0101b 6 entries	Project:	BDW					
Default Value:	0101b 6 entries										
Project:	BDW										
25:24	LP Write Request Limit										
	<p>The value in this register indicates the maximum number of back to back LP write requests that will be accepted from a single client before re-arbitrating.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>00b</td><td>1</td></tr> <tr> <td>01b</td><td>2</td></tr> <tr> <td>10b</td><td>4 [Default]</td></tr> <tr> <td>11b</td><td>8</td></tr> </tbody> </table>	Value	Name	00b	1	01b	2	10b	4 [Default]	11b	8
Value	Name										
00b	1										
01b	2										
10b	4 [Default]										
11b	8										
23:20	TLB Request Limit										
	<p>The value in this register indicates the maximum number of TLB requests that can be made in an arbitration loop. Zero is not a valid programming.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0110b</td><td>6 [Default]</td></tr> <tr> <td>[1,15]</td><td></td></tr> </tbody> </table>	Value	Name	0110b	6 [Default]	[1,15]					
Value	Name										
0110b	6 [Default]										
[1,15]											
19:16	TLB Request InFlight Limit										
	<p>The value in this register indicates the maximum number of TLB (or VTd) requests that can be in flight at any given time. Zero is not a valid programming.</p>										

ARB_CTL			
		Value	Name
		0110b	6 [Default]
		[1,15]	
15	FBC Watermark Disable Setting this bit disables the FBC watermarks.		
		Value	Name
		0b	Enable
		1b	Disable
14:13	Tiled Address Swizzling DRAM configuration registers show if memory address swizzling is needed.		
		Value	Name
		00b	No Display
		01b	Reserved
		10b	Reserved
		11b	Reserved
12:8	HP Page Break Limit The value in this register represents the maximum number of page breaks allowed in a HP request chain. Zero is not a valid programming.		
		Value	Name
		10000b	16 [Default]
		[1,31]	
7	Reserved		
6:0	HP Data Request Limit The value in this register represents the maximum number of cachelines allowed in a HP request chain.		
		Value	Name
		1010110b	86 [Default]
		[1,127]	
		Restriction	
		This value must always be programmed greater than 8.	

ARB_CTL2

ARB_CTL2		
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x20000600 Access: R/W Size (in bits): 32		
Address: 45004h-45007h Name: Display Arbitration Control 2 ShortName: ARB_CTL2 Valid Projects: BDW Power: Always on Reset: soft		
DWord	Bit	Description
0	31	Reserved
	30	Reserved
29:28		Format: MBZ
	LP WD Write Request Limit	The value in this register indicates the maximum number of back to back LP write requests that will be accepted from WD before re-arbitrating.
	Value	Name
	00b	1
	01b	2
	10b	4 [Default]
	11b	8
27:25	Reserved	
	Format:	MBZ
24	GroupReqs DKS	
	Project:	BDW
	This field selects whether arbiter requests are grouped for this plane.	
	Value	Name
	0b	Do not group
	1b	Group

ARB_CTL2

23	GroupReqs CursorC	
	Project:	BDW
	This field selects whether arbiter requests are grouped for this plane.	
	Value	Name
	0b	Do not group
	1b	Group
22	GroupReqs SpriteC	
	Project:	BDW
	This field selects whether arbiter requests are grouped for this plane.	
	Value	Name
	0b	Do not group
	1b	Group
21	GroupReqs PrimaryC	
	Project:	BDW
	This field selects whether arbiter requests are grouped for this plane.	
	Value	Name
	0b	Do not group
	1b	Group
20	GroupReqs CursorB	
	Project:	BDW
	This field selects whether arbiter requests are grouped for this plane.	
	Value	Name
	0b	Do not group
	1b	Group
19	GroupReqs SpriteB	
	Project:	BDW
	This field selects whether arbiter requests are grouped for this plane.	
	Value	Name
	0b	Do not group
	1b	Group
18	GroupReqs PrimaryB	
	Project:	BDW
	This field selects whether arbiter requests are grouped for this plane.	
	Value	Name
	0b	Do not group
	1b	Group

ARB_CTL2

		GroupReqs CursorA										
	17	<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> </table> <p>This field selects whether arbiter requests are grouped for this plane.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Do not group</td></tr> <tr> <td>1b</td><td>Group</td></tr> </tbody> </table>	Project:	BDW	Value	Name	0b	Do not group	1b	Group		
Project:	BDW											
Value	Name											
0b	Do not group											
1b	Group											
	16	GroupReqs SpriteA										
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> </table> <p>This field selects whether arbiter requests are grouped for this plane.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Do not group</td></tr> <tr> <td>1b</td><td>Group</td></tr> </tbody> </table>	Project:	BDW	Value	Name	0b	Do not group	1b	Group		
Project:	BDW											
Value	Name											
0b	Do not group											
1b	Group											
	15	GroupReqs PrimaryA										
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> </table> <p>This field selects whether arbiter requests are grouped for this plane.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Do not group</td></tr> <tr> <td>1b</td><td>Group</td></tr> </tbody> </table>	Project:	BDW	Value	Name	0b	Do not group	1b	Group		
Project:	BDW											
Value	Name											
0b	Do not group											
1b	Group											
	14	Reserved										
		<table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ								
Format:	MBZ											
	13	Reserved										
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	BDW	Format:	MBZ						
Project:	BDW											
Format:	MBZ											
	12	Reserved										
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	BDW	Format:	MBZ						
Project:	BDW											
Format:	MBZ											
	11	Reserved										
	10:9	Inflight LP Read Request Limit										
		<p>The value in this register represents the maximum number of LP read request transactions that can be inflight at any given time.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>00b</td><td>1 LP</td></tr> <tr> <td>01b</td><td>2 LP</td></tr> <tr> <td>10b</td><td>3 LP</td></tr> <tr> <td>11b</td><td>4 LP [Default]</td></tr> </tbody> </table>	Value	Name	00b	1 LP	01b	2 LP	10b	3 LP	11b	4 LP [Default]
Value	Name											
00b	1 LP											
01b	2 LP											
10b	3 LP											
11b	4 LP [Default]											
	8	Reserved										
		<table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ								
Format:	MBZ											

ARB_CTL2												
	7	Reserved										
		Project: BDW										
	6	Reserved										
		Format: MBZ										
	5:4	Inflight HP Read Request Limit The value in this register represents the maximum number of HP read request transactions that can be inflight at any given time. <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>00b</td><td>128 HP</td></tr> <tr> <td>01b</td><td>64 HP</td></tr> <tr> <td>10b</td><td>32 HP</td></tr> <tr> <td>11b</td><td>16 HP</td></tr> </tbody> </table>	Value	Name	00b	128 HP	01b	64 HP	10b	32 HP	11b	16 HP
Value	Name											
00b	128 HP											
01b	64 HP											
10b	32 HP											
11b	16 HP											
	3	Reserved										
		Project: BDW										
		Format: MBZ										
	2	Reserved										
		Format: MBZ										
	1:0	RTID FIFO Watermark The value in this register represents the watermark value for the RTID FIFO. HP transactions will start only when the FIFO level is above or equal the watermark. <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>00b</td><td>8 RTIDs</td></tr> <tr> <td>01b</td><td>16 RTIDs</td></tr> <tr> <td>10b</td><td>32 RTIDs</td></tr> <tr> <td>11b</td><td>Reserved</td></tr> </tbody> </table>	Value	Name	00b	8 RTIDs	01b	16 RTIDs	10b	32 RTIDs	11b	Reserved
Value	Name											
00b	8 RTIDs											
01b	16 RTIDs											
10b	32 RTIDs											
11b	Reserved											

Arbiter Control Register

GARBCNTLREG - Arbiter Control Register						
DWord	Bit	Description				
0	31	Reserved				
	30	Disables hashing function <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Disables hashing function to generate bank_id[1:0] for L3\$ bank accessing, and forces the use of address[7:6] for bank_id[1:0]. 0: (default) Hash function enabled to generate L3\$ bank IDs. 1: L3\$ address[7:6] used as L3\$ bank IDs. Incf_csr_l3bankidhashdis. (This bit needs to set corresponding bit lpfcon_csr_l3bankidhashdis in LPFC.)</p>	Access:	R/W		
Access:	R/W					
	29:28	Arbitration priority order between RCC and MSC <table border="1"> <tr> <td>Default Value:</td> <td>10b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Arbitration priority order between RCC and MSC. 00b/11b: Invalid; default setting used. 10b: Default setting; RCC MSC (i.e., MSC has higher priority). 01b: RCC MSC (i.e., RCC has higher priority). Incf_csr_rcc_msc_pri[1:0].</p>	Default Value:	10b	Access:	R/W
Default Value:	10b					
Access:	R/W					
	27:22	Arbitration priority order between RCZ, STC, and HIZ <table border="1"> <tr> <td>Default Value:</td> <td>100100b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Arbitration priority order between RCZ, STC, and HIZ. 100100b: Default setting; RCZ STC HIZ. (i.e., RCZ has lowest priority; HIZ has highest priority). 100001b: RCZ ; HIZ ; STC. 011000b: STC ; RCZ ; HIZ. 010010b: STC ; HIZ ; RCZ. 001001b: HIZ ; RCZ ; STC. 000110b: HIZ ; STC ; RCZ. Note: Others settings are invalid, and result in use of default. Incf_csr_rcz_stc_hiz_pri[5:0].</p>	Default Value:	100100b	Access:	R/W
Default Value:	100100b					
Access:	R/W					

GARBCNTLREG - Arbiter Control Register

	21:19	Write data port arbitration priority between Z client writes and L3\$ evictions				
		<table border="1"> <tr> <td>Default Value:</td><td>010b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Z Max Write Request Limit Count (GFXC_MRLC). This is the MAX number of Allowed Requests Count - These counters keep track of the accepted requests from each engine. Requests are counted, regardless of kind of cycle (both Slice 0 and 1). Minimum count value must be = 1. Incf_csr_wdpagapz[2:0].</p>	Default Value:	010b	Access:	R/W
Default Value:	010b					
Access:	R/W					
	18:16	Write data port arbitration priority between C client writes and Z/L3\$ writes/evictions				
		<table border="1"> <tr> <td>Default Value:</td><td>010b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>C Max Request Limit Count (GFXZ_MRLC). This is the MAX number of Allowed Requests Count - These counters keep track of the accepted requests from each engine. Requests are counted, regardless of kind of cycle (both Slice 0 and 1). Minimum count value must be = 1. Incf_csr_wdpagapc[2:0].</p>	Default Value:	010b	Access:	R/W
Default Value:	010b					
Access:	R/W					
	15	Reserved				
		<table border="1"> <tr> <td>Access:</td><td>RO</td></tr> </table>	Access:	RO		
Access:	RO					
	14:12	L3 Max Write Request Limit Count				
		<table border="1"> <tr> <td>Default Value:</td><td>100b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>L3 Max Write Request Limit Count (GFXL3_MRLC). This is the MAX number of Allowed Requests Count - These counters keep track of the accepted requests from each engine. Requests are counted, regardless of kind of cycle (Miss/Hit/Present). Minimum count value must be = 1. Incf_csr_wdpagapl3[2:0].</p>	Default Value:	100b	Access:	R/W
Default Value:	100b					
Access:	R/W					
	11:9	Reserved				
		<table border="1"> <tr> <td>Access:</td><td>RO</td></tr> </table>	Access:	RO		
Access:	RO					
	8	GAPs_fixarb_en				
		<table border="1"> <tr> <td>Default Value:</td><td>1b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Incf_csr_gaps_fixarb_en.</p>	Default Value:	1b	Access:	R/W
Default Value:	1b					
Access:	R/W					
	6:0	Reserved				
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Project:	BDW	Access:	RO
Project:	BDW					
Access:	RO					

Arbiter Mode Control Register

ARB_MODE - Arbiter Mode Control Register		
DWord	Bit	Description
0	31:16	Mask Bits Default Value: 0000000000000000b Access: RO Mask Bits act as Write Enables for the bits[15:0] of this register.
	15	Extra Register Bit 15 Default Value: 0b Access: R/W Bit 15 toggles (XOR) the meaning of Per Client Write Drop Enables (Register 40b4); If 0, drop per client happens as stated in register 40b4 definition; If 1, the meaning changes, and a 1 on a bit in register 40b4 means dont drop while 0 means drop. In this case, the default (for clients not included in 40b4) will be drop enabled.
	14	Extra Register Bit 14 Default Value: 0b Project: BDW Access: R/W PD load disable - When this bit is set, the PD load is disabled for GFX/MFX0/MFX1. A-step: Default Value: 0 B-step: Default Value: 0 - Bug ID: 1905990 Future steppings can have value 1.
	13	DC GDR Default Value: 0b Access: R/W
	12	HIZ GDR Default Value: 0b Access: R/W
	11	STC GDR Default Value: 0b Access: R/W

ARB_MODE - Arbiter Mode Control Register				
	10	BLB GDR		
		Default Value:	0b	
		Access:	R/W	
	9	GAM PD GDR		
		Default Value:	0b	
		Access:	R/W	
	8	Extra Register Bit 8		
		Default Value:	0b	
		Access:	R/W	
		Description		
		Reserved.		
	7:6	Cacheability Attribute Override		
		Default Value:	00b	
		Access:	R/W	
		00b No override. 01b UC (LLC/eLLC) - Allocation age is don't care. 10b WT in LLC/eLLC - Aged is 3. 11b WB in LLC/eLLC - Aged is 3. The above conditions apply for the following conditions only: 1. Register overwrite except for GTT, CFG and L3 coherent wcil cycles 2. Read- GTTRD, CFGRD 3. Write- GTTWR, CFGWR, DMWR (with gam_ci_wcoherenttype[2:0] = "001" WCIL* w/self snoop)		
	5	Extra Register Bit 5		
		Default Value:	0b	
		Access:	R/W	
		Reserved.		
	4	VMC GDR Enable		
		Default Value:	0b	
		Access:	R/W	
		When this bit is set, data requested from the VMC client is generated by the GDR Algorithm.		
	3	Texture Cache (MT) GDR Enable Bit		
		Default Value:	0b	
		Access:	R/W	
		When this bit is set, data requested from the Texture Cache (MT) client is generated by the GDR algorithm.		

ARB_MODE - Arbiter Mode Control Register

		Depth (RCZ) Cache GDR Enable bit						
	2	<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Depth Cache GDR enable bit. Project: All. Format: U1. When this bit is set, data requested from the Depth Cache client is generated by the GDR algorithm (See GDR algorithm in xxx section).</p>	Default Value:	0b	Access:	R/W		
Default Value:	0b							
Access:	R/W							
	1	<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>When this bit is set, data requested from the Color Cache (RCC) client is generated by the GDR algorithm.</p>	Default Value:	0b	Access:	R/W		
Default Value:	0b							
Access:	R/W							
	0	<table border="1"> <tr> <td>GTT Accesses GDR</td><td></td></tr> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>When this bit is enabled along with the Client's GDR bit, PPGTT and GGTT requests for this memory access are also tagged as GDR to SQ.</p>	GTT Accesses GDR		Default Value:	0b	Access:	R/W
GTT Accesses GDR								
Default Value:	0b							
Access:	R/W							

ASL Storage

ASLS_0_2_0_PCI - ASL Storage						
DWord	Bit	Description				
0	31:0	<p>Device Switching Storage</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000000000000000000000000000b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Software controlled usage to support device switching.</p>	Default Value:	00000000000000000000000000000000b	Access:	R/W
Default Value:	00000000000000000000000000000000b					
Access:	R/W					

Async Slice Count Select Register

ASYNC_SLICE_COUNT - Async Slice Count Select Register						
DWord	Bit	Description				
0	2:0	<p>ASYNC Slice Count</p> <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Slice Count Request in Asynchronous Mode: 001b = 1 slice. 010b = 2 slices. 011b = 3 slices.</p>	Project:	BDW	Access:	R/W
Project:	BDW					
Access:	R/W					

ATS Capability

ATS_CAP_0_2_0_PCI - ATS Capability			
Register Space: PCI: 0/2/0 Project: BDW Default Value: 0x00000020 Size (in bits): 16			
Address: 00204h			
ATS Capability reports support for Device-TLBs on Device-2, compliant to PCI Express ATS specification.			
DWord	Bit	Description	
0	5	Page Aligned Request	
		Default Value:	1b
	4:0	Access:	RO
		Hardwired to 1, the Untranslated Address is always aligned to a 4096 byte boundary. Processor Graphics reports value of 1b indicating all VT-d and SVM translations are page-aligned.	
	4:0	Invalidate Queue Depth	
		Default Value:	00000b
		Access:	RO
		The number of Invalidate Requests that the endpoint can accept before putting back pressure on the upstream connection. Hardwired to 0h, the function can accept 32 Invalidate Requests.	

ATS Control

ATS_CTRL_0_2_0_PCI - ATS Control						
DWord	Bit	Description				
0	15	<p>ATS Enable</p> <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>When Set, the function is enabled to cache translations. Processor graphics ignores this field, as GT uses GTLB as IOTLB and only pretends to software that it has a Device-TLB. Software is expected to Set this field before configuring extended context-entry for Device2 with Page Request Enable field Set. For compatibility, this field is implemented as RW as software can read it to determine ATS enable status.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
	14:5	<p>Reserved</p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ		
Format:	MBZ					
	4:0	<p>Smallest Translation Unit</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>This value indicates to the Endpoint the minimum number of 4096-byte blocks that is indicated in a Translation Completion or Invalidate Request. This is a power of 2 multiple and the number of blocks is 2^{STU}. A value of 0 indicates one block and value 1F indicates 2^{31} blocks. For IGD this must be programmed to 0h for 4KB as smallest translation unit.</p>	Default Value:	00000b	Access:	R/W
Default Value:	00000b					
Access:	R/W					

ATS Extended Capability Header

ATS_EXTCAP_0_2_0_PCI - ATS Extended Capability Header		
DWord	Bit	Description
0	31:20	Next Capability Offset
		Default Value: 001100000000b Access: RO
		This is a hardwired pointer to the next item in the capabilities list. Value 300h in this field provides the offset for Page-Request Capability.
	19:16	Version
		Default Value: 0001b Access: RO
		Hardwired to capability version 1.
	15:0	Capability ID
		Default Value: 0000000000001111b Access: RO
		Hardwired to the ATS Extended Capability ID

AUD_CONFIG

AUD_CONFIG											
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x0070FA60 Access: R/W Size (in bits): 32											
Address:			65000h-65003h								
Name:			Audio Configuration Transcoder A								
ShortName:			AUD_TCA_CONFIG								
Power:			off/on								
Reset:			soft								
Address:			65100h-65103h								
Name:			Audio Configuration Transcoder B								
ShortName:			AUD_TCB_CONFIG								
Power:			off/on								
Reset:			soft								
Address:			65200h-65203h								
Name:			Audio Configuration Transcoder C								
ShortName:			AUD_TCC_CONFIG								
Power:			off/on								
Reset:			soft								
This register configures the audio output. There is one instance of this register per transcoder A/B/C. Each Transcoder is independent of the other.											
DWord	Bit	Description									
0	31:30	Reserved									
	29	N value Index									
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>HDMI [Default]</td><td>N value read on bits 27:20 and 15:4 reflects HDMI N value. Bits 27:20 and 15:4 are programmable to any N value. Default h7FA6 when bit 28 is not set.</td></tr> <tr> <td>1b</td><td>DisplayPort</td><td>N value read on bits 27:20 and 15:4 reflects DisplayPort N value. Set this bit to 1 before programming N value register. When this bit is set to 1, 27:20 and 15:4 will reflect the current N value. Default is h8000 when bit 28 is not set.</td></tr> </tbody> </table>		Value	Name	Description	0b	HDMI [Default]	N value read on bits 27:20 and 15:4 reflects HDMI N value. Bits 27:20 and 15:4 are programmable to any N value. Default h7FA6 when bit 28 is not set.	1b	DisplayPort
Value	Name	Description									
0b	HDMI [Default]	N value read on bits 27:20 and 15:4 reflects HDMI N value. Bits 27:20 and 15:4 are programmable to any N value. Default h7FA6 when bit 28 is not set.									
1b	DisplayPort	N value read on bits 27:20 and 15:4 reflects DisplayPort N value. Set this bit to 1 before programming N value register. When this bit is set to 1, 27:20 and 15:4 will reflect the current N value. Default is h8000 when bit 28 is not set.									
28	N programming enable This bit enables programming of N values for non-CEA modes. Please note that the transcoder to which audio is attached must be disabled when changing this field.										

AUD_CONFIG																																									
	27:20	Upper N value																																							
		<table border="1"> <tr> <td>Default Value:</td><td>0000011b</td></tr> </table> <p>These are bits [19:12] of programmable N values for non-CEA modes. Bit 29 of this register must also be written in order to enable programming. Please note that the transcoder to which audio is attached must be disabled when changing this field. See bit 29 description for default values.</p>	Default Value:	0000011b																																					
Default Value:	0000011b																																								
	19:16	Pixel Clock HDMI																																							
		<p>This is the target frequency of the CEA/HDMI video mode to which the audio stream is added. This value is used for generating N_CTS packets. This refers to only HDMI Pixel clock and does not refer to DisplayPort Link clock. DisplayPort Link clock does not require this programming.</p> <p>Note: The transcoder on which audio is attached must be disabled when changing this field.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>[Default]</td><td></td></tr> <tr> <td>0000b</td><td>25.2 / 1.001 MHz</td><td>25.2 / 1.001 MHz</td></tr> <tr> <td>0001b</td><td>25.2 MHz</td><td>25.2 MHz (Program this value for pixel clocks not listed in this field)</td></tr> <tr> <td>0010b</td><td>27 MHz</td><td>27 MHz</td></tr> <tr> <td>0011b</td><td>27 * 1.001 MHz</td><td>27 * 1.001 MHz</td></tr> <tr> <td>0100b</td><td>54 MHz</td><td>54 MHz</td></tr> <tr> <td>0101b</td><td>54 * 1.001 MHz</td><td>54 * 1.001 MHz</td></tr> <tr> <td>0110b</td><td>74.25 / 1.001 MHz</td><td>74.25 / 1.001 MHz</td></tr> <tr> <td>0111b</td><td>74.25 MHz</td><td>74.25 MHz</td></tr> <tr> <td>1000b</td><td>148.5 / 1.001 MHz</td><td>148.5 / 1.001 MHz</td></tr> <tr> <td>1001b</td><td>148.5 MHz</td><td>148.5 MHz</td></tr> <tr> <td>Others</td><td>Reserved</td><td>Reserved</td></tr> </tbody> </table>	Value	Name	Description	0b	[Default]		0000b	25.2 / 1.001 MHz	25.2 / 1.001 MHz	0001b	25.2 MHz	25.2 MHz (Program this value for pixel clocks not listed in this field)	0010b	27 MHz	27 MHz	0011b	27 * 1.001 MHz	27 * 1.001 MHz	0100b	54 MHz	54 MHz	0101b	54 * 1.001 MHz	54 * 1.001 MHz	0110b	74.25 / 1.001 MHz	74.25 / 1.001 MHz	0111b	74.25 MHz	74.25 MHz	1000b	148.5 / 1.001 MHz	148.5 / 1.001 MHz	1001b	148.5 MHz	148.5 MHz	Others	Reserved	Reserved
Value	Name	Description																																							
0b	[Default]																																								
0000b	25.2 / 1.001 MHz	25.2 / 1.001 MHz																																							
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0111b	74.25 MHz	74.25 MHz																																							
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1001b	148.5 MHz	148.5 MHz																																							
Others	Reserved	Reserved																																							
	15:4	Lower N value																																							
		<table border="1"> <tr> <td>Default Value:</td><td>111110100110b</td></tr> </table> <p>These are bits [11:0] of programmable N values for non-CEA modes. Bit 29 of this register must also be written in order to enable programming. Please note that the transcoder to which audio is attached must be disabled when changing this field. See bit 29 description for default values</p>	Default Value:	111110100110b																																					
Default Value:	111110100110b																																								
	3	Reserved																																							
	2:0	Reserved																																							

AUD_DIP_ELD_CTRL_ST

AUD_DIP_ELD_CTRL_ST			
Register Space:	MMIO: 0/2/0		
Project:	BDW		
Default Value:	0x00005400		
Access:	R/W		
Size (in bits):	32		
Address:	650B4h-650B7h		
Name:	Audio Control State for DIP and ELD Transcoder A		
ShortName:	AUD_TCA_DIP_ELD_CTRL_ST		
Power:	off/on		
Reset:	soft		
Address:	651B4h-651B7h		
Name:	Audio Control State for DIP and ELD Transcoder B		
ShortName:	AUD_TCB_DIP_ELD_CTRL_ST		
Power:	off/on		
Reset:	soft		
Address:	652B4h-652B7h		
Name:	Audio Control State for DIP and ELD Transcoder C		
ShortName:	AUD_TCC_DIP_ELD_CTRL_ST		
Power:	off/on		
Reset:	soft		
There is one instance of this register per transcoder A/B/C.			
DWord	Bit	Description	
0	31	Reserved	
		Project:	BDW
		Format:	MBZ

AUD DIP ELD CTRL ST

30:29	<p>DIP Port Select</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Project:</td><td style="padding: 2px;">BDW</td></tr> <tr> <td style="padding: 2px;">Access:</td><td style="padding: 2px;">RO</td></tr> </table> <p>This read-only bit reflects which port is used to transmit the DIP data. This can only change when DIP is disabled. If one or more audio-related DIP packets is enabled and audio is enabled on a digital port, these bits will reflect the digital port to which audio is directed. For DP MST, this is the device select/pipe select.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="background-color: #e0f2ff; text-align: center; padding: 2px;">Value</th><th style="background-color: #e0f2ff; text-align: center; padding: 2px;">Name</th><th style="background-color: #e0f2ff; text-align: center; padding: 2px;">Description</th></tr> </thead> <tbody> <tr> <td style="padding: 2px;">00b</td><td style="padding: 2px;">Reserved [Default]</td><td style="padding: 2px;">Reserved</td></tr> <tr> <td style="padding: 2px;">01b</td><td style="padding: 2px;">Digital Port B</td><td style="padding: 2px;">Digital Port B</td></tr> <tr> <td style="padding: 2px;">10b</td><td style="padding: 2px;">Digital Port C</td><td style="padding: 2px;">Digital Port C</td></tr> <tr> <td style="padding: 2px;">11b</td><td style="padding: 2px;">Digital Port D</td><td style="padding: 2px;">Digital Port D</td></tr> </tbody> </table>			Project:	BDW	Access:	RO	Value	Name	Description	00b	Reserved [Default]	Reserved	01b	Digital Port B	Digital Port B	10b	Digital Port C	Digital Port C	11b	Digital Port D	Digital Port D										
Project:	BDW																															
Access:	RO																															
Value	Name	Description																														
00b	Reserved [Default]	Reserved																														
01b	Digital Port B	Digital Port B																														
10b	Digital Port C	Digital Port C																														
11b	Digital Port D	Digital Port D																														
28:25	<p>Reserved</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Format:</td><td style="padding: 2px;">MBZ</td></tr> </table>			Format:	MBZ																											
Format:	MBZ																															
24:21	<p>DIP type enable status</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td><td style="padding: 2px;">RO</td></tr> </table> <p>These bits reflect the DIP types enabled. It can be updated while the port is enabled. Within 2 vblank periods, the DIP is guaranteed to have been transmitted. Disabling a DIP type results in setting the contents of that DIP buffer to zero. A reserved setting reflects a disabled DIP.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="background-color: #e0f2ff; text-align: center; padding: 2px;">Value</th><th style="background-color: #e0f2ff; text-align: center; padding: 2px;">Name</th><th style="background-color: #e0f2ff; text-align: center; padding: 2px;">Description</th></tr> </thead> <tbody> <tr> <td style="padding: 2px;">0000b</td><td style="padding: 2px;">[Default]</td><td style="padding: 2px;"></td></tr> <tr> <td style="padding: 2px;">XXX0b</td><td style="padding: 2px;">DIP Disable</td><td style="padding: 2px;">Audio DIP disabled</td></tr> <tr> <td style="padding: 2px;">XXX1b</td><td style="padding: 2px;">DIP Enable</td><td style="padding: 2px;">Audio DIP enabled</td></tr> <tr> <td style="padding: 2px;">XX0Xb</td><td style="padding: 2px;">ACP Disable</td><td style="padding: 2px;">Generic 1 (ACP) DIP disabled</td></tr> <tr> <td style="padding: 2px;">XX1Xb</td><td style="padding: 2px;">ACP Enable</td><td style="padding: 2px;">Generic 1 (ACP) DIP enabled</td></tr> <tr> <td style="padding: 2px;">X0XXb</td><td style="padding: 2px;">Generic 2 Disable</td><td style="padding: 2px;">Generic 2 DIP disabled</td></tr> <tr> <td style="padding: 2px;">X1XXb</td><td style="padding: 2px;">Generic 2 Enable</td><td style="padding: 2px;">Generic 2 DIP enabled, can be used by ISRC1 or ISRC2</td></tr> <tr> <td style="padding: 2px;">1XXXb</td><td style="padding: 2px;">Reserved</td><td style="padding: 2px;">Reserved</td></tr> </tbody> </table>			Access:	RO	Value	Name	Description	0000b	[Default]		XXX0b	DIP Disable	Audio DIP disabled	XXX1b	DIP Enable	Audio DIP enabled	XX0Xb	ACP Disable	Generic 1 (ACP) DIP disabled	XX1Xb	ACP Enable	Generic 1 (ACP) DIP enabled	X0XXb	Generic 2 Disable	Generic 2 DIP disabled	X1XXb	Generic 2 Enable	Generic 2 DIP enabled, can be used by ISRC1 or ISRC2	1XXXb	Reserved	Reserved
Access:	RO																															
Value	Name	Description																														
0000b	[Default]																															
XXX0b	DIP Disable	Audio DIP disabled																														
XXX1b	DIP Enable	Audio DIP enabled																														
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1XXXb	Reserved	Reserved																														

AUD_DIP_ELD_CTRL_ST

		DIP buffer index This field is used during read of different DIPs, and during read or write of ELD data. These bits are used as an index to their respective DIP or ELD buffers. When the index is not valid, the contents of the DIP will return all 0s.																		
	20:18	<table border="1" style="width: 100%;"> <thead> <tr> <th style="background-color: #e0e0ff;">Value</th> <th style="background-color: #e0e0ff;">Name</th> <th style="background-color: #e0e0ff;">Description</th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>Audio [Default]</td> <td>Audio DIP (31 bytes of address space, 31 bytes of data)</td> </tr> <tr> <td>001b</td> <td>Gen 1</td> <td>Generic 1 (ACP) Data Island Packet (31 bytes of address space, 31 bytes of data)</td> </tr> <tr> <td>010b</td> <td>Gen 2</td> <td>Generic 2 (ISRC1) Data Island Packet (31 bytes of address space, 31 bytes of data)</td> </tr> <tr> <td>011b</td> <td>Gen 3</td> <td>Generic 3 (ISRC2) Data Island Packet (31 bytes of address space, 31 bytes of data)</td> </tr> <tr> <td>Others</td> <td>Reserved</td> <td>Reserved</td> </tr> </tbody> </table>	Value	Name	Description	000b	Audio [Default]	Audio DIP (31 bytes of address space, 31 bytes of data)	001b	Gen 1	Generic 1 (ACP) Data Island Packet (31 bytes of address space, 31 bytes of data)	010b	Gen 2	Generic 2 (ISRC1) Data Island Packet (31 bytes of address space, 31 bytes of data)	011b	Gen 3	Generic 3 (ISRC2) Data Island Packet (31 bytes of address space, 31 bytes of data)	Others	Reserved	Reserved
Value	Name	Description																		
000b	Audio [Default]	Audio DIP (31 bytes of address space, 31 bytes of data)																		
001b	Gen 1	Generic 1 (ACP) Data Island Packet (31 bytes of address space, 31 bytes of data)																		
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011b	Gen 3	Generic 3 (ISRC2) Data Island Packet (31 bytes of address space, 31 bytes of data)																		
Others	Reserved	Reserved																		
	17:16	DIP transmission frequency <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Access:</td> <td style="width: 50%; text-align: right;">RO</td> </tr> </table> <p>These bits reflect the frequency of DIP transmission for the DIP buffer type designated in bits 20:18. When writing DIP data, this value is also latched when the first DW of the DIP is written. When read, this value reflects the DIP transmission frequency for the DIP buffer designated in bits 20:18.</p> <table border="1" style="width: 100%;"> <thead> <tr> <th style="background-color: #e0e0ff;">Value</th> <th style="background-color: #e0e0ff;">Name</th> <th style="background-color: #e0e0ff;">Description</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>Disable [Default]</td> <td>Disabled</td> </tr> <tr> <td>01b</td> <td>Reserved</td> <td>Reserved</td> </tr> <tr> <td>10b</td> <td>Send Once</td> <td>Send Once</td> </tr> <tr> <td>11b</td> <td>Best Effort</td> <td>Best effort (Send at least every other vsync)</td> </tr> </tbody> </table>	Access:	RO	Value	Name	Description	00b	Disable [Default]	Disabled	01b	Reserved	Reserved	10b	Send Once	Send Once	11b	Best Effort	Best effort (Send at least every other vsync)	
Access:	RO																			
Value	Name	Description																		
00b	Disable [Default]	Disabled																		
01b	Reserved	Reserved																		
10b	Send Once	Send Once																		
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	15	Reserved <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Format:</td> <td style="width: 50%; text-align: right;">MBZ</td> </tr> </table>	Format:	MBZ																
Format:	MBZ																			
	14:10	ELD buffer size <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Default Value:</td> <td style="width: 50%; text-align: right;">10101b</td> </tr> <tr> <td>Access:</td> <td style="text-align: right;">RO</td> </tr> </table> <p>This field reflects the size of the ELD buffer in DWORDs (84 Bytes of ELD)</p>	Default Value:	10101b	Access:	RO														
Default Value:	10101b																			
Access:	RO																			
	9:5	ELD access address Selects the DWORD address for access to the ELD buffer (84 bytes). The value wraps back to zero when incremented past the max addressing value 0x1F. This field change takes effect immediately after being written. The read value indicates the current access address.																		
	4	ELD ACK Acknowledgement from the audio driver that ELD read has been completed																		

AUD_DIP_ELD_CTRL_ST

	3:0	DIP access address Selects the DWORD address for access to the DIP buffers. The value wraps back to zero when it incremented past the max addressing value of 0xF. This field change takes effect immediately after being written. The read value indicates the current access address.
--	-----	---

AUD_EDID_DATA

AUD_EDID_DATA	
Register Space:	MMIO: 0/2/0
Project:	BDW
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	65050h-65053h
Name:	Audio EDID Data Block Transcoder A
ShortName:	AUD_TCA_EDID_DATA
Power:	off/on
Reset:	soft
Address:	65150h-65153h
Name:	Audio EDID Data Block Transcoder B
ShortName:	AUD_TCB_EDID_DATA
Power:	off/on
Reset:	soft
Address:	65250h-65253h
Name:	Audio EDID Data Block Transcoder C
ShortName:	AUD_TCC_EDID_DATA
Power:	off/on
Reset:	soft
<p>These registers contain the HDMI/DP data block from the EDID. The graphics driver reads the EDID and writes the structure to these registers. The vendor specific data block may be longer than 8 bytes, but the driver must not write more than 48 bytes to the buffer. The EDID format is Version 3 within the CEA-861B specification. The HDMI/DP Vendor Specific Data Block is described in version 1.1 of the HDMI specification. These values are returned from the device as the HDMI/DP Vendor Specific Data Block response to a Get HDMI/DP Widget command.</p> <p>Writing sequence:</p> <ul style="list-style-type: none"> • Video software sets ELD invalid, and sets the ELD access address to 0, or to the desired DWORD to be written. • Video software writes ELD data 1 DWORD at a time. The ELD access address autoincrements with each DWORD write, wrapping around to address 0 when the max buffer address size of 0xF has been reached. • Please note that software must write an entire DWORD at a time. • Please note that the audio driver checks the valid bit with each byte read of the ELD. This means that the video driver can unilaterally write ELD irrespective of audio driver ELD read status. <p>Reading sequence:</p> <ul style="list-style-type: none"> • Video software sets the ELD access address to 0, or to the desired DWORD to be read. 	

AUD_EDID_DATA

- Video software reads ELD data 1 DWORD at a time. The ELD access address autoincrements with each DWORD read, wrapping around to address 0 when the max buffer address size of 0xF has been reached.

There is one instance of this register per transcoder A/B/C.

DWord	Bit	Description
0	31:0	EDID Data Block Please note that the contents of this buffer are not cleared when ELD is disabled. The contents of this buffer are cleared during FLR.

AUD_INFOFR

AUD_INFOFR		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Address:	65054h-65057h	
Name:	Audio Widget Data Island Packet Transcoder A	
ShortName:	AUD_TCA_INFOFR	
Power:	off/on	
Reset:	soft	
Address:	65154h-65157h	
Name:	Audio Widget Data Island Packet Transcoder B	
ShortName:	AUD_TCB_INFOFR	
Power:	off/on	
Reset:	soft	
Address:	65254h-65257h	
Name:	Audio Widget Data Island Packet Transcoder C	
ShortName:	AUD_TCC_INFOFR	
Power:	off/on	
Reset:	soft	
When the IF type or dword index is not valid, the contents of the DIP will return all 0s. These values are programmed by the audio driver in an HDMI/DP Widget Set command. They are returned one byte at a time from the device on the HD audio bus as the HDMI/DP DIP response to a Get HDMI/DP Widget command. To fetch a specific byte, the audio driver should send an HDMI/DP Widget HDMI/DP DIP Index Pointer Set command to set the index, then fetch the indexed byte using the HDMI/DP DIP get.		
DWord	Bit	Description
0	31:0	Data Island Packet Data This reflects the contents of the DIP indexed by the DIP access address. The contents of this buffer are cleared during function reset or HD audio link reset.

AUD_M_CTS_ENABLE

AUD_M_CTS_ENABLE			
Register Space:	MMIO: 0/2/0		
Project:	BDW		
Default Value:	0x00000000		
Access:	R/W		
Size (in bits):	32		
Address:	65028h-6502Bh		
Name:	Audio M and CTS Programming Enable Transcoder A		
ShortName:	AUD_TCA_M_CTS_ENABLE		
Power:	off/on		
Reset:	soft		
Address:	65128h-6512Bh		
Name:	Audio M and CTS Programming Enable Transcoder B		
ShortName:	AUD_TCB_M_CTS_ENABLE		
Power:	off/on		
Reset:	soft		
Address:	65228h-6522Bh		
Name:	Audio M and CTS Programming Enable Transcoder C		
ShortName:	AUD_TCC_M_CTS_ENABLE		
Power:	off/on		
Reset:	soft		
There is one instance of this register per transcoder A/B/C.			
DWord	Bit	Description	
0	31:22	Reserved	
	21	CTS M value Index	
		Value	Name
		0b	CTS [Default]
		1b	M
		CTS value read on bits 19:0 reflects CTS value. Bit 19:0 is programmable to any CTS value. default is 0	
		M value read on bits 19:0 reflects DisplayPort M value. Set this bit to 1 before programming M value register. When this is set to 1 19:0 will reflect the current M value	
	20	Enable CTS or M prog When set will enable CTS or M programming.	
	19:0	CTS programming These are bits [19:0] of programmable CTS values for non-CEA modes. Bit 21 of this register must also be written in order to enable programming. Please note that the transcoder to which audio is attached must be disabled when changing this field.	

AUD_MISC_CTRL

AUD_MISC_CTRL				
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x00000044 Access: R/W Size (in bits): 32				
Address: 65010h-65013h Name: Audio Converter 1 Misc Control ShortName: AUD_C1_MISC_CTRL Power: off/on Reset: soft				
Address: 65110h-65113h Name: Audio Converter 2 Misc Control ShortName: AUD_C2_MISC_CTRL Power: off/on Reset: soft				
Address: 65210h-65213h Name: Audio Converter 3 Misc Control ShortName: AUD_C3_MISC_CTRL Power: off/on Reset: soft				
There is one instance of this register per audio converter 1/2/3.				
DWord	Bit	Description		
0	31:9	Reserved <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ
Format:	MBZ			
8	Reserved			
7:4	Output Delay <table border="1"> <tr> <td>Default Value:</td> <td>0100b</td> </tr> </table> <p>The number of samples between when the sample is received from the HD Audio link and when it appears as an analog signal at the pin.</p>	Default Value:	0100b	
Default Value:	0100b			
3	Reserved <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ	
Format:	MBZ			

AUD_MISC_CTRL												
	2	Sample Fabrication EN bit										
Access:			R/W									
This bit indicates whether internal fabrication of audio samples is enabled during a link underrun.												
<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Disable</td><td>Audio fabrication disabled</td></tr> <tr> <td>1b</td><td>Enable [Default]</td><td>Audio fabrication enabled</td></tr> </tbody> </table>				Value	Name	Description	0b	Disable	Audio fabrication disabled	1b	Enable [Default]	Audio fabrication enabled
Value	Name	Description										
0b	Disable	Audio fabrication disabled										
1b	Enable [Default]	Audio fabrication enabled										
	1	Pro Allowed										
Access:			R/W									
By default, the audio device is configured to consumer mode and does not allow the mode to be changed to professional mode by an HD Audio verb. When Pro is allowed by setting this configuration bit, the HD Audio codec allows a verb to set the device into professional mode.												
Note: Setting this configuration bit does not change the default Pro bit value to be 1. Pro must be set to 1 through the normal process, using a verb.												
<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Consumer [Default]</td><td>Consumer use only</td></tr> <tr> <td>1b</td><td>Professional</td><td>Professional use allowed</td></tr> </tbody> </table>				Value	Name	Description	0b	Consumer [Default]	Consumer use only	1b	Professional	Professional use allowed
Value	Name	Description										
0b	Consumer [Default]	Consumer use only										
1b	Professional	Professional use allowed										
	0	Reserved										
Format:			MBZ									

AUD_PIN_ELD_CP_VLD

AUD_PIN_ELD_CP_VLD										
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x00000000 Access: R/W Size (in bits): 32										
Address: 650C0h-650C3h Name: Audio Pin ELD and CP Ready Status ShortName: AUD_PIN_ELD_CP_VLD Power: off/on Reset: soft										
This register is used for handshaking between the audio and video drivers for interrupt management. For each transcoder, ELD is sent by the display software to the audio software via an unsolicited response when the ELD ready bit is set. Display software sets this bit as part of enabling the audio-enabled digital device/transcoder. To support DP MST, this bit is transcoder-based, and hardware will use it appropriately to send the status to the audio driver using device widgets. Both HDMI and DP1.1 will also be transcoder based as shown below.										
DWord	Bit	Description								
0	31:12	Reserved <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> </table>	Project:	BDW						
Project:	BDW									
11	Audio InactiveC Inactive: When this bit is set, a digital display sink device has been attached but not active for streaming audio. <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Disable</td><td>Device is active for streaming audio data</td></tr> <tr> <td>1b</td><td>Enable</td><td>Device is connected but not active</td></tr> </tbody> </table>	Value	Name	Description	0b	Disable	Device is active for streaming audio data	1b	Enable	Device is connected but not active
Value	Name	Description								
0b	Disable	Device is active for streaming audio data								
1b	Enable	Device is connected but not active								
10	Audio Output EnableC This bit directs audio to the device connected to this transcoder. When enabled along with Inactive set to 0 and audio data is available, the audio data will be combined with the video data and sent over this transcoder. The audio unit uses the status of this bit to indicate presence of the HDMI/DP output to the audio driver. <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Disable</td><td>No Audio output</td></tr> <tr> <td>1b</td><td>Valid</td><td>Audio is enabled</td></tr> </tbody> </table>	Value	Name	Description	0b	Disable	No Audio output	1b	Valid	Audio is enabled
Value	Name	Description								
0b	Disable	No Audio output								
1b	Valid	Audio is enabled								

AUD_PIN_ELD_CP_VLD

	9	CP ReadyC This R/W bit reflects the state of CP request from the audio unit. When an audio CP request has been serviced, it must be reset to 1 by the video software to indicate that the CP request has been serviced. This is transcoder based.									
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Pending or Not Ready</td><td>CP request pending or not ready to receive requests</td></tr> <tr> <td>1b</td><td>Ready</td><td>CP request ready</td></tr> </tbody> </table>	Value	Name	Description	0b	Pending or Not Ready	CP request pending or not ready to receive requests	1b	Ready	CP request ready
Value	Name	Description									
0b	Pending or Not Ready	CP request pending or not ready to receive requests									
1b	Ready	CP request ready									
	8	ELD validC This R/W bit reflects the state of the ELD data written to the ELD RAM. After writing the ELD data, the video software must set this bit to 1 to indicate that the ELD data is valid. At audio codec initialization, or on a hotplug event, this bit is set to 0 by the video software. This bit is reflected in the audio pin complex widget as the ELD valid status bit. This is transcoder based.									
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Invalid</td><td>ELD data invalid (default, when writing ELD data, set 0 by software)</td></tr> <tr> <td>1b</td><td>Valid</td><td>ELD data valid (Set by video software only)</td></tr> </tbody> </table>	Value	Name	Description	0b	Invalid	ELD data invalid (default, when writing ELD data, set 0 by software)	1b	Valid	ELD data valid (Set by video software only)
Value	Name	Description									
0b	Invalid	ELD data invalid (default, when writing ELD data, set 0 by software)									
1b	Valid	ELD data valid (Set by video software only)									
	7	Audio InactiveB Inactive: When this bit is set, a digital display sink device has been attached but not active for streaming audio.									
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Disable</td><td>Device is active for streaming audio data</td></tr> <tr> <td>1b</td><td>Enable</td><td>Device is connected but not active</td></tr> </tbody> </table>	Value	Name	Description	0b	Disable	Device is active for streaming audio data	1b	Enable	Device is connected but not active
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	6	Audio Output EnableB This bit directs audio to the device connected to this transcoder. When enabled along with Inactive set to 0 and audio data is available, the audio data will be combined with the video data and sent over this transcoder. The audio unit uses the status of this bit to indicate presence of the HDMI/DP output to the audio driver. This is transcoder based.									
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Value	Name	Description									
0b	Disable	No audio output									
1b	Enable	Audio is enabled									
	5	CP ReadyB See CP_ReadyC description.									
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Not Ready</td><td>CP request pending or not ready to receive requests</td></tr> <tr> <td>1b</td><td>Ready</td><td>CP request ready</td></tr> </tbody> </table>	Value	Name	Description	0b	Not Ready	CP request pending or not ready to receive requests	1b	Ready	CP request ready
Value	Name	Description									
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AUD_PIN_ELD_CP_VLD

	3	Audio InactiveA Inactive: When this bit is set, a digital display sink device has been attached but not active for streaming audio.									
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	2	Audio Output EnableA This bit directs audio to the device connected to this transcoder. When enabled along with Inactive set to 0 and audio data is available, the audio data will be combined with the video data and sent over this transcoder. The audio unit uses the status of this bit to indicate presence of the HDMI/DP output to the audio driver. This is transcoder based.									
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Value	Name	Description									
0b	Disable	No audio output									
1b	Enable	Audio is enabled									
	1	CP ReadyA See CP_ReadyC description.									
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Not Ready</td><td>CP request pending or not ready to receive requests</td></tr> <tr> <td>1b</td><td>Ready</td><td>CP request ready</td></tr> </tbody> </table>	Value	Name	Description	0b	Not Ready	CP request pending or not ready to receive requests	1b	Ready	CP request ready
Value	Name	Description									
0b	Not Ready	CP request pending or not ready to receive requests									
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	0	ELD validA See ELD_validC descripion.									
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Invalid</td><td>ELD data invalid (default, when writing ELD data, set 0 by software)</td></tr> <tr> <td>1b</td><td>Valid</td><td>ELD data valid (Set by video software only)</td></tr> </tbody> </table>	Value	Name	Description	0b	Invalid	ELD data invalid (default, when writing ELD data, set 0 by software)	1b	Valid	ELD data valid (Set by video software only)
Value	Name	Description									
0b	Invalid	ELD data invalid (default, when writing ELD data, set 0 by software)									
1b	Valid	ELD data valid (Set by video software only)									

AUD_PIN_PIPE_CONN_ENTRY_LNGTH

AUD_PIN_PIPE_CONN_ENTRY_LNGTH		
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x00000001 Access: RO Size (in bits): 32		
Address: 650A8h-650ABh Name: Audio Connection List Entry and Length Transcoder A ShortName: AUD_TCA_PIN_PIPE_CONN_ENTRY_LNGTH_RO Power: off/on Reset: soft		
Address: 651A8h-651ABh Name: Audio Connection List Entry and Length Transcoder B ShortName: AUD_TCB_PIN_PIPE_CONN_ENTRY_LNGTH_RO Power: off/on Reset: soft		
Address: 652A8h-652ABh Name: Audio Connection List Entry and Length Transcoder C ShortName: AUD_TCC_PIN_PIPE_CONN_ENTRY_LNGTH_RO Power: off/on Reset: soft		
These values are returned from the device as the Connection List Length response to a Get Pin Widget command or Get Device Widget command if DP MST. There is one instance of this register per transcoder A/B/C.		
DWord	Bit	Description
0	31:16	Reserved
	15:8	Connection List Entry Connection to Convertor Widget Node 0x03
	7	Long Form This bit indicates whether the items in the connection list are long form or short form. This bit is hardwired to 0 (items in connection list are short form)
	6:0	Connection List Length Default Value: 0000001b This field indicates the number of items in the connection list. If this field is 2, there is only one hardwired input possible, which is read from the Connection List, and there is no Connection Select Control.

AUD_PIPE_CONN_SEL_CTRL

AUD_PIPE_CONN_SEL_CTRL							
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x00030303 Access: RO Size (in bits): 32							
Address: 650ACh-650AFh Name: Audio Pipe Connection Select Control ShortName: AUD_PIN_PIPE_CONN_SEL_CTRL_RO Power: off/on Reset: soft							
These values are returned from the device as the Connection List Length response to a Get Pin Widget command or Get Device Widget command for DP MST.							
DWord	Bit	Description					
0	31:24	Reserved <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> </table>	Project:	BDW			
Project:	BDW						
23:16	Connection select Control D Connection Index Currently Set [Default 0x00], Port D Widget is set to 0x02 <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Project</th></tr> </thead> <tbody> <tr> <td>03h</td><td>[Default]</td><td>BDW</td></tr> </tbody> </table>	Value	Name	Project	03h	[Default]	BDW
Value	Name	Project					
03h	[Default]	BDW					
15:8	Connection select Control C Connection Index Currently Set [Default 0x00], Port C Widget is set to 0x01 <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Project</th></tr> </thead> <tbody> <tr> <td>03h</td><td>[Default]</td><td>BDW</td></tr> </tbody> </table>	Value	Name	Project	03h	[Default]	BDW
Value	Name	Project					
03h	[Default]	BDW					
7:0	Connection select Control B Connection Index Currently Set [Default 0x00], Port B Widget is set to 0x00 <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Project</th></tr> </thead> <tbody> <tr> <td>03h</td><td>[Default]</td><td>BDW</td></tr> </tbody> </table>	Value	Name	Project	03h	[Default]	BDW
Value	Name	Project					
03h	[Default]	BDW					

AUD_PWRST

AUD_PWRST							
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0xFFFFFFFF Access: RO Size (in bits): 32							
Address: 6504Ch-6504Fh Name: Audio Power State Read Only ShortName: AUD_PWRST_RO Power: off/on Reset: soft							
These values are returned from the device as the Power State response to a Get Audio Function Group command.							
DWord	Bit	Description					
0	31:28	Reserved <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> </table>	Project:	BDW			
Project:	BDW						
27:26	Func Grp Dev PwrSt Curr <table border="1"> <tr> <td>Format:</td><td>Audio Power State Format</td></tr> </table> Function Group Device current power state <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>11b</td><td></td></tr> </tbody> </table>	Format:	Audio Power State Format	Value	Name	11b	
Format:	Audio Power State Format						
Value	Name						
11b							
25:24	Func Grp Dev PwrSt Set <table border="1"> <tr> <td>Format:</td><td>Audio Power State Format</td></tr> </table> Function Group Device power state that was set <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>11b</td><td></td></tr> </tbody> </table>	Format:	Audio Power State Format	Value	Name	11b	
Format:	Audio Power State Format						
Value	Name						
11b							
23:22	Converter3 Widget PwrSt Curr <table border="1"> <tr> <td>Format:</td><td>Audio Power State Format</td></tr> </table> Converter3 Widget current power state <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>11b</td><td></td></tr> </tbody> </table>	Format:	Audio Power State Format	Value	Name	11b	
Format:	Audio Power State Format						
Value	Name						
11b							
21:20	Converter3 Widget PwrSt Req <table border="1"> <tr> <td>Format:</td><td>Audio Power State Format</td></tr> </table> Converter3 Widget power state that was requested by audio software <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>11b</td><td></td></tr> </tbody> </table>	Format:	Audio Power State Format	Value	Name	11b	
Format:	Audio Power State Format						
Value	Name						
11b							

AUD_PWRST															
	19:18	Convertor2 Widget PwrSt Curr <table border="1"> <tr> <td>Format:</td><td>Audio Power State Format</td></tr> <tr> <td colspan="3">Converor2 Widget current power state</td></tr> <tr> <td align="center" colspan="2">Value</td><td align="center" colspan="2">Name</td></tr> <tr> <td align="center" colspan="2">11b</td><td align="center" colspan="2"></td></tr> </table>	Format:	Audio Power State Format	Converor2 Widget current power state			Value		Name		11b			
Format:	Audio Power State Format														
Converor2 Widget current power state															
Value		Name													
11b															
	17:16	Convertor2 Widget PwrSt Req <table border="1"> <tr> <td>Format:</td><td>Audio Power State Format</td></tr> <tr> <td colspan="3">Converter2 Widget power state that was requested by audio software</td></tr> <tr> <td align="center" colspan="2">Value</td><td align="center" colspan="2">Name</td></tr> <tr> <td align="center" colspan="2">11b</td><td align="center" colspan="2"></td></tr> </table>	Format:	Audio Power State Format	Converter2 Widget power state that was requested by audio software			Value		Name		11b			
Format:	Audio Power State Format														
Converter2 Widget power state that was requested by audio software															
Value		Name													
11b															
	15:14	Convertor1 Widget PwrSt Curr <table border="1"> <tr> <td>Format:</td><td>Audio Power State Format</td></tr> <tr> <td colspan="3">Converter1 Widget current power state</td></tr> <tr> <td align="center" colspan="2">Value</td><td align="center" colspan="2">Name</td></tr> <tr> <td align="center" colspan="2">11b</td><td align="center" colspan="2"></td></tr> </table>	Format:	Audio Power State Format	Converter1 Widget current power state			Value		Name		11b			
Format:	Audio Power State Format														
Converter1 Widget current power state															
Value		Name													
11b															
	13:12	Convertor1 Widget PwrSt Req <table border="1"> <tr> <td>Format:</td><td>Audio Power State Format</td></tr> <tr> <td colspan="3">Converter1 Widget power state that was requested by audio software</td></tr> <tr> <td align="center" colspan="2">Value</td><td align="center" colspan="2">Name</td></tr> <tr> <td align="center" colspan="2">11b</td><td align="center" colspan="2"></td></tr> </table>	Format:	Audio Power State Format	Converter1 Widget power state that was requested by audio software			Value		Name		11b			
Format:	Audio Power State Format														
Converter1 Widget power state that was requested by audio software															
Value		Name													
11b															
	11:10	PinD Widget PwrSt Curr <table border="1"> <tr> <td>Format:</td><td>Audio Power State Format</td></tr> <tr> <td colspan="3">PinD Widget current power stateFor DP MST this represents Device3 power state</td></tr> <tr> <td align="center" colspan="2">Value</td><td align="center" colspan="2">Name</td></tr> <tr> <td align="center" colspan="2">11b</td><td align="center" colspan="2"></td></tr> </table>	Format:	Audio Power State Format	PinD Widget current power stateFor DP MST this represents Device3 power state			Value		Name		11b			
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Value		Name													
11b															
	9:8	PinD Widget PwrSt Set <table border="1"> <tr> <td>Format:</td><td>Audio Power State Format</td></tr> <tr> <td colspan="3">PinD Widget power state that was setFor DP MST this represents Device3 power state</td></tr> <tr> <td align="center" colspan="2">Value</td><td align="center" colspan="2">Name</td></tr> <tr> <td align="center" colspan="2">11b</td><td align="center" colspan="2"></td></tr> </table>	Format:	Audio Power State Format	PinD Widget power state that was setFor DP MST this represents Device3 power state			Value		Name		11b			
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Value		Name													
11b															
	7:6	PinC Widget PwrSt Curr <table border="1"> <tr> <td>Format:</td><td>Audio Power State Format</td></tr> <tr> <td colspan="3">PinC Widget current power stateFor DP MST this represents Device2 power state</td></tr> <tr> <td align="center" colspan="2">Value</td><td align="center" colspan="2">Name</td></tr> <tr> <td align="center" colspan="2">11b</td><td align="center" colspan="2"></td></tr> </table>	Format:	Audio Power State Format	PinC Widget current power stateFor DP MST this represents Device2 power state			Value		Name		11b			
Format:	Audio Power State Format														
PinC Widget current power stateFor DP MST this represents Device2 power state															
Value		Name													
11b															

AUD_PWRST				
	5:4	PinC Widget PwrSt Set		
		Format:	Audio Power State Format	
		PinC Widget power state that was setFor DP MST this represents Device2 power state		
		Value	Name	
		11b		
	3:2	PinB Widget PwrSt Curr		
		Format:	Audio Power State Format	
		PinB Widget current power stateFor DP MST this represents Device1 power state		
		Value	Name	
		11b		
	1:0	PinB Widget PwrSt Set		
		Format:	Audio Power State Format	
		PinB Widget power state that was setFor DP MST this represents Device1 power state		
		Value	Name	
		11b		

AUD_RID

AUD_RID			
Register Space:	MMIO: 0/2/0		
Project:	BDW		
Default Value:	0x00100000		
Access:	RO		
Size (in bits):	32		
Address:	65024h-65027h		
Name:	Audio Revision ID Read Only		
ShortName:	AUD_RID_RO		
Power:	off/on		
Reset:	soft		
These values are returned from the device as the Revision ID response to a Get Root Node command.			
DWord	Bit	Description	
0	31:24	Reserved	
	23:20	Major Revision	
		<table border="1"> <tr> <td>Default Value:</td><td>1h</td></tr> </table> <p>The major revision number (left of the decimal) of the HD Audio Spec to which the codec is fully compliant. This field is hardwired within the device.</p>	Default Value:
Default Value:	1h		
19:16	Minor Revision		
	<table border="1"> <tr> <td>Default Value:</td><td>0h</td></tr> </table> <p>The minor revision number (rights of the decimal) or dot number of the HD Audio Spec to which the codec is fully compliant. This field is hardwired within the device.</p>	Default Value:	0h
Default Value:	0h		
15:8	15:8	Revision ID	
		<table border="1"> <tr> <td>Default Value:</td><td>00h</td></tr> </table> <p>The vendor revision number for this given Device ID. This field is hardwired within the device.</p>	Default Value:
Default Value:	00h		
7:0	7:0	Stepping ID	
		<table border="1"> <tr> <td>Default Value:</td><td>00h</td></tr> </table> <p>An optional vendor stepping number within the given Revision ID. This field is hardwired within the device.</p>	Default Value:
Default Value:	00h		

AUD_VID_DID

AUD_VID_DID										
Register Space:	MMIO: 0/2/0									
Project:	BDW									
	0x80862808 [BDW]									
Access:	RO									
Size (in bits):	32									
Address:	65020h-65023h									
Name:	Audio Vendor ID / Device ID Read Only									
ShortName:	AUD_VID_DID_RO									
Power:	off/on									
Reset:	soft									
These values are returned from the device as the Vendor ID/ Device ID response to a Get Root Node command.										
DWord	Bit	Description								
0	31:16	Vendor ID								
		<table border="1"> <tr> <td>Default Value:</td><td>8086h</td></tr> <tr> <td colspan="2">Used to identify the codec within the PnP system. This field is hardwired within the device.</td></tr> </table>	Default Value:	8086h	Used to identify the codec within the PnP system. This field is hardwired within the device.					
Default Value:	8086h									
Used to identify the codec within the PnP system. This field is hardwired within the device.										
	15:0	Device ID								
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td colspan="2">Constant used to identify the codec within the PnP system. This field is set by the device hardware.</td></tr> <tr> <th>Value</th><th>Name</th><th>Project</th></tr> <tr> <td>2808h</td><td>Broadwell [Default]</td><td>BDW</td></tr> </table>	Project:	BDW	Constant used to identify the codec within the PnP system. This field is set by the device hardware.		Value	Name	Project	2808h
Project:	BDW									
Constant used to identify the codec within the PnP system. This field is set by the device hardware.										
Value	Name	Project								
2808h	Broadwell [Default]	BDW								

AUD_WD_CNTRL

AUD_WD_CNTRL											
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x00000540 Access: R/W Size (in bits): 32											
Address: 65800h-65803h Name: Audio WD Control ShortName: AUD_WD_CNTRL Power: off/on Reset: soft											
DWord	Bit	Description									
0	31	Audio Inactive WD Inactive: When this bit is set, wireless display device has been attached but not active for streaming audio. <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Disable</td><td>Device is active for streaming audio data</td></tr> <tr> <td>1b</td><td>Enable</td><td>Device is connected but not active</td></tr> </tbody> </table>	Value	Name	Description	0b	Disable	Device is active for streaming audio data	1b	Enable	Device is connected but not active
Value	Name	Description									
0b	Disable	Device is active for streaming audio data									
1b	Enable	Device is connected but not active									
Audio Output Enable WD This bit directs audio to the Wireless Device. When enabled along with Inactive set to 0 and audio data is available, the audio data will be sent to the Wireless memory. <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Disable</td><td>No Audio output</td></tr> <tr> <td>1b</td><td>Valid</td><td>Audio is enabled</td></tr> </tbody> </table>	Value	Name	Description	0b	Disable	No Audio output	1b	Valid	Audio is enabled		
Value	Name	Description									
0b	Disable	No Audio output									
1b	Valid	Audio is enabled									
29	CP Ready WD This R/W bit reflects the state of CP request from the audio unit. When an audio CP request has been serviced, it must be reset to 1 by the display software to indicate that the CP request has been serviced. <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Pending or Not Ready</td><td>CP request pending or not ready to receive requests</td></tr> <tr> <td>1b</td><td>Ready</td><td>CP request ready</td></tr> </tbody> </table>	Value	Name	Description	0b	Pending or Not Ready	CP request pending or not ready to receive requests	1b	Ready	CP request ready	
Value	Name	Description									
0b	Pending or Not Ready	CP request pending or not ready to receive requests									
1b	Ready	CP request ready									

AUD_WD_CNTRL

	28	ELD valid WD This R/W bit reflects the state of the ELD data written to the ELD RAM. After writing the ELD data, the video software must set this bit to 1 to indicate that the ELD data is valid. At audio codec initialization, or on a hotplug event, this bit is set to 0 by the video software. This bit is reflected in the audio pin complex widget as the ELD valid status bit.									
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Invalid</td> <td>ELD data invalid (default, when writing ELD data, set 0 by software)</td> </tr> <tr> <td>1b</td> <td>Valid</td> <td>ELD data valid (Set by video software only)</td> </tr> </tbody> </table>	Value	Name	Description	0b	Invalid	ELD data invalid (default, when writing ELD data, set 0 by software)	1b	Valid	ELD data valid (Set by video software only)
Value	Name	Description									
0b	Invalid	ELD data invalid (default, when writing ELD data, set 0 by software)									
1b	Valid	ELD data valid (Set by video software only)									
	27:24	Reserved									
		<table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ							
Format:	MBZ										
	23	Reserved									
		<table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	BDW	Format:	MBZ					
Project:	BDW										
Format:	MBZ										
	22:20	Reserved									
		<table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	BDW	Format:	MBZ					
Project:	BDW										
Format:	MBZ										
	19:11	Reserved									
		<table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ							
Format:	MBZ										
	10:6	ELD buffer size									
		<table border="1"> <tr> <td>Default Value:</td> <td>10101b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Default Value:	10101b	Access:	RO					
Default Value:	10101b										
Access:	RO										
		This field reflects the size of the ELD buffer in DWORDs (84 Bytes of ELD)									
	5:1	ELD access address Selects the DWORD address for access to the ELD buffer (84 bytes). The value wraps back to zero when incremented past the max addressing value 0x1F. This field change takes effect immediately after being written. The read value indicates the current access address.									
	0	ELD ACK Acknowledgement from the audio driver that ELD read has been completed									

AUD_WD_DMA_UBASEADR

AUD_WD_DMA_UBASEADR		
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x00000000 Access: R/W Size (in bits): 32		
Address: 65824h-65827h Name: Audio WD Input DMA Upper Base Address ShortName: AUD_WD_DMA_UBASEADR Power: off/on Reset: soft		
DWord	Bit	Description
0	31:0	Aud WD DMA UBADR This field specifies the upper base address of the Input DMA. It must be at least 64B (cache line) aligned. It must not be modified when the stream is playing. It can only be modified when the WD enable bit 30 is not set in the Audio WD Control register.

AUD_WD_EDID_DATA

AUD_WD_EDID_DATA		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	65810h-65813h	
Name:	Audio WD EDID Data	
ShortName:	AUD_WD_EDID_DATA	
Power:	off/on	
Reset:	soft	
<p>This register contains the Wireless data block from the EDID. The graphics driver reads the EDID and writes the structure to these registers. The vendor specific data block may be longer than 8 bytes, but the driver must not write more than 48 bytes to the buffer. The EDID format is Version 3 within the CEA-861B specification. The HDMI/DP Vendor Specific Data Block is described in version 1.1 of the HDMI specification. These values are returned from the device as the HDMI/DP Vendor Specific Data Block response to a Get Wireless Widget command. Writing sequence:</p> <ul style="list-style-type: none"> • Video software sets ELD invalid, and sets the ELD access address to 0, or to the desired DWORD to be written. • Video software writes ELD data 1 DWORD at a time. The ELD access address autoincrements with each DWORD write, wrapping around to address 0 when the max buffer address size has been reached. • Please note that software must write an entire DWORD at a time. • Please note that the audio driver checks the valid bit with each byte read of the ELD. This means that the video driver can unilaterally write ELD irrespective of audio driver ELD read status. <p>Reading sequence:</p> <ul style="list-style-type: none"> • Video software sets the ELD access address to 0, or to the desired DWORD to be read. • Video software reads ELD data 1 DWORD at a time. The ELD access address autoincrements with each DWORD read, wrapping around to address 0 when the max buffer address size has been reached. 		
DWord	Bit	Description
0	31:0	<p>EDID Data Block</p> <p>This field specifies the EDID data block. Please note that the contents of this buffer are not cleared when ELD is disabled. The contents of this buffer are cleared during a device 2 FLR.</p>

Audio Codec Interrupt Definition

Audio Codec Interrupt Definition					
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x00000000 Size (in bits): 32					
Address: 44480h-4448Fh Name: Audio Codec Interrupts ShortName: AUD_INTERRUPT Valid Projects: BDW Power: Always on Reset: soft					
This table indicates which events are mapped to each bit of the Audio Codec Interrupt registers. 0x44480 = ISR 0x44484 = IMR 0x44488 = IIR 0x4448C = IER					
DWord	Bit	Description			
0	31	Audio_Power_State_change_DDI_D The ISR is an active high pulse when there is a power state change for audio for DDI D.			
	30	Audio_Power_State_change_DDI_C The ISR is an active high pulse when there is a power state change for audio for DDI C.			
	29	Audio_Power_State_change_DDI_B The ISR is an active high pulse when there is a power state change for audio for DDI B.			
	28	Audio_Power_State_change_WD_0 <table border="1"> <thead> <tr> <th colspan="2">Description</th> </tr> </thead> <tbody> <tr> <td colspan="2">This interrupt event is not connected on Broadwell.</td> </tr> </tbody> </table>	Description		This interrupt event is not connected on Broadwell.
Description					
This interrupt event is not connected on Broadwell.					
27	Spare 27 <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> </table>	Project:	BDW		
Project:	BDW				
26	Spare 26				
25	Spare 25				
24	Spare 24				
23	Spare 23				
22	Spare 22				
21	Spare 21				
20	Spare 20				
19	Spare 19				
18	Spare 18				

Audio Codec Interrupt Definition

	Project:	BDW
17	Spare 17	
	Project:	BDW
16	Spare 16	
	Project:	BDW
15	Spare 15	
	Project:	BDW
14	Reserved	
13	Reserved	
12	Spare 12	
11	Spare 11	
	Project:	BDW
10	Reserved	
9	Reserved	
8:7	Unused_Int_8_7	These interrupts are currently unused.
6	Reserved	
5	Reserved	
4:3	Unused_Int_4_3	These interrupts are currently unused.
2	Reserved	
1	Reserved	
0	Spare 0	
	Project:	BDW

Auto Draw End Offset

3DPRIM_END_OFFSET - Auto Draw End Offset				
DWord	Bit	Description		
0	31:0	<p>End Offset</p> <table border="1"> <tr> <td>Format:</td> <td>U32</td> </tr> </table> <p>This register is used to store the end offset value used by the Vertex Fetch to determine when to stop processing the 3D_PRIMITIVE command. This register is valid when the End Offset Enable is set in the 3D_PRIMITIVE command.</p>	Format:	U32
Format:	U32			

AVC GAM Slave Counter High part

AVC_GAM_SLAVE_CTR_H - AVC GAM Slave Counter High part								
DWord	Bit	Description						
0	31:0	<p>AVC GAM SLave Counter High</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td colspan="2">AVC GAM Slave counter[63:32]</td></tr> </table>	Default Value:	00000000h	Access:	R/W	AVC GAM Slave counter[63:32]	
Default Value:	00000000h							
Access:	R/W							
AVC GAM Slave counter[63:32]								

AVC GAM Slave Counter Low part

AVC_GAM_SLAVE_CTR_L - AVC GAM SlaveCounterLowpart						
DWord	Bit	Description				
0	31:0	<p>AVC GAM SLave Counter Low</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>AVC GAM Slave counter[31:0]</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

Base Data of Stolen Memory

BDSM_0_0_0_PCI - Base Data of Stolen Memory						
DWord	Bit	Description				
0	31:20	<p>Graphics Base of Stolen Memory</p> <table border="1"> <tr> <td>Default Value:</td> <td>000000000000b</td> </tr> <tr> <td>Access:</td> <td>R/W Lock</td> </tr> </table> <p>This register contains bits 31 to 20 of the base address of stolen DRAM memory. BIOS determines the base of graphics stolen memory by subtracting the graphics stolen memory size (PCI Device 0 offset 52 bits 6:4) from TOLUD (PCI Device 0 offset BC bits 31:20).</p>	Default Value:	000000000000b	Access:	R/W Lock
Default Value:	000000000000b					
Access:	R/W Lock					
	19:1	<p>Reserved</p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ		
Format:	MBZ					
	0	<p>Lock</p> <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W Key Lock</td> </tr> </table> <p>This bit will lock all writeable settings in this register, including itself.</p>	Default Value:	0b	Access:	R/W Key Lock
Default Value:	0b					
Access:	R/W Key Lock					

Base of GTT Stolen Memory

BGSM_0_0_0_PCI - Base of GTT Stolen Memory			
Register Space: PCI: 0/0/0 Project: BDW Default Value: 0x00000000 Size (in bits): 32			
Address: 000B4h			
This register contains the base address of stolen DRAM memory for the GTT.			
DWord	Bit	Description	
0	31:20	Graphics Base of GTT Stolen Memory	
		Default Value:	000000000b
		Access:	R/W Lock
This register contains the base address of stolen DRAM memory for the GTT. BIOS determines the base of GTT stolen memory by subtracting the GTT graphics stolen memory size (PCI Device 0 offset 52 bits 11:8) from the Graphics Base of Data Stolen Memory (PCI Device 0 offset B0 bits 31:20).			
	19:1	Reserved	
		Format:	MBZ
	0	Lock	
		Default Value:	0b
		Access:	R/W Key Lock
This bit will lock all writeable settings in this register, including itself.			

Batch Address Difference Register

BB_ADDR_DIFF - Batch Address Difference Register

Register Space:	MMIO: 0/2/0
Project:	BDW
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02154h-02157h
Name:	Batch Address Difference Register
ShortName:	BB_ADDR_DIFF_RCSUNIT
Address:	12154h-12157h
Name:	Batch Address Difference Register
ShortName:	BB_ADDR_DIFF_VCSUNIT0
Address:	1A154h-1A157h
Name:	Batch Address Difference Register
ShortName:	BB_ADDR_DIFF_VECSUNIT
Address:	1C154h-1C157h
Name:	Batch Address Difference Register
ShortName:	BB_ADDR_DIFF_VCSUNIT1
Address:	22154h-22157h
Name:	Batch Address Difference Register
ShortName:	BB_ADDR_DIFF_BCSUNIT

This register contains the difference between the start of the last batch and where the last initiated Batch Buffer is currently fetching commands.

Programming Notes

Programming Restriction:

This register should NEVER be programmed by driver, this is for HW internal use only.

DWord	Bit	Description				
0	31:2	Batch Buffer Address Difference <table border="1"> <tr> <td>Format:</td> <td>GraphicsAddress[31:2]</td> </tr> <tr> <td colspan="2">This field specifies the DWord-aligned difference between the starting address of the batch buffer and where the last initiated Batch Buffer is currently fetching commands.</td> </tr> </table>	Format:	GraphicsAddress[31:2]	This field specifies the DWord-aligned difference between the starting address of the batch buffer and where the last initiated Batch Buffer is currently fetching commands.	
Format:	GraphicsAddress[31:2]					
This field specifies the DWord-aligned difference between the starting address of the batch buffer and where the last initiated Batch Buffer is currently fetching commands.						
1:0	Reserved <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ			
Format:	MBZ					

Batch Buffer Head Pointer Register

BB_ADDR - Batch Buffer Head Pointer Register			
Register Space:	MMIO: 0/2/0		
Project:	BDW		
Default Value:	0x00000000		
Access:	RO		
Size (in bits):	32		
Address:	02140h-02143h		
Name:	Batch Buffer Head Pointer Register		
ShortName:	BB_ADDR_RCSUNIT		
Address:	12140h-12143h		
Name:	Batch Buffer Head Pointer Register		
ShortName:	BB_ADDR_VCSUNIT0		
Address:	1A140h-1A143h		
Name:	Batch Buffer Head Pointer Register		
ShortName:	BB_ADDR_VECSUNIT		
Address:	1C140h-1C143h		
Name:	Batch Buffer Head Pointer Register		
ShortName:	BB_ADDR_VCSUNIT1		
Address:	22140h-22143h		
Name:	Batch Buffer Head Pointer Register		
ShortName:	BB_ADDR_BCSUNIT		
This register contains the current DWord Graphics Memory Address of the last-initiated batch buffer.			
Programming Notes			
Programming Restriction: This register should NEVER be programmed by driver. This is for HW internal use only.			
DWord	Bit	Description	
0	31:2	Batch Buffer Head Pointer	
		Project:	BDW
	1	Format:	GraphicsAddress[31:2]
		This field specifies the DWord-aligned Graphics Memory Address where the last initiated Batch Buffer is currently fetching commands. If no batch buffer is currently active, the Valid bit will be 0 and this field will be meaningless.	
		Reserved	Format: MBZ

BB_ADDR - Batch Buffer Head Pointer Register

	0	Valid		
		Format:	U1	
Value	Name	Description		
0h	Invalid [Default]	Batch buffer Invalid		
1h	Valid	Batch buffer Valid		

Batch Buffer Per Context Pointer

BB_PER_CTX_PTR - Batch Buffer Per Context Pointer	
Register Space:	MMIO: 0/2/0
Project:	BDW
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	021C0h-021C3h
Name:	Batch Buffer Per Context Pointer
ShortName:	BB_PER_CTX_PTR_RCSUNIT
Address:	121C0h-121C3h
Name:	Batch Buffer Per Context Pointer
ShortName:	BB_PER_CTX_PTR_VCSUNIT0
Address:	1A1C0h-1A1C3h
Name:	Batch Buffer Per Context Pointer
ShortName:	BB_PER_CTX_PTR_VECSUNIT
Address:	1C1C0h-1C1C3h
Name:	Batch Buffer Per Context Pointer
ShortName:	BB_PER_CTX_PTR_VCSUNIT1
Address:	221C0h-221C3h
Name:	Batch Buffer Per Context Pointer
ShortName:	BB_PER_CTX_PTR_BCSUNIT
This register is used to program the batch buffer address to be executed between context restore and execution of ring/execution list if enabled. This will only get executed due to regular context save/restore and not during power restore. This register is part of the execution list context and will be executed per context. Only supported if execution list is enabled. There is no preempting workloads within the Per Context Batch Buffer.	
Programming Notes	
BlitterCS/VideoCS/VideoCS2/VideoEnhancementCS: This register functionality is not supported and must not be programmed for these command streamers.	
Render CS: Per Context Batch Buffer execution must not look at the MI_RS_CONTROL or Wait For Event status that are restored for the corresponding context. Ex: A context with MI_RS_CONTROL status with RS disabled doesn't stop Render CS from triggering Resource Streamer to execute Per Context Batch Buffer when " RS Enabled Batch Buffer Per Context " is set.	
Source	
BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS	
RenderCS	

BB_PER_CTX_PTR - Batch Buffer Per Context Pointer

RenderCS: The following commands are not supported within a Per Context Batch Buffer:

Command Name
MI_WAIT_FOR_EVENT
MI_ARB_CHECK
MI_RS_CONTROL
MI_REPORT_HEAD
MI_URB_ATOMIC_ALLOC
MI_SUSPEND_FLUSH
MI_TOPOLOGY_FILTER
MI_RS_CONTEXT
MI_SET_CONTEXT
MI_URB_CLEAR
MI_SEMAPHORE_WAIT (Memory Poll Mode). Note: MI_SEMAPHORE_WAIT in register poll mode is supported.
MI_SEMAPHORE_SIGNAL
MI_BATCH_BUFFER_START
MI_CONDITIONAL_BATCH_BUFFER_END
MEDIA_OBJECT_WALKER
GPGPU_WALKER
3DPRIMITIVE
3DSTATE_BINDING_TABLE_POINTERS_VS
3DSTATE_BINDING_TABLE_POINTERS_HS
3DSTATE_BINDING_TABLE_POINTERS_DS
3DSTATE_BINDING_TABLE_POINTERS_GS
3DSTATE_BINDING_TABLE_POINTERS_PS
3DSTATE_GATHER_CONSTANT_VS
3DSTATE_GATHER_CONSTANT_GS
3DSTATE_GATHER_CONSTANT_HS
3DSTATE_GATHER_CONSTANT_DS
3DSTATE_GATHER_CONSTANT_PS
3DSTATE_DX9_CONSTANTF_VS
3DSTATE_DX9_CONSTANTF_HS
3DSTATE_DX9_CONSTANTF_DS
3DSTATE_DX9_CONSTANTF_GS
3DSTATE_DX9_CONSTANTF_PS
3DSTATE_DX9_CONSTANTI_VS

RenderCS

BB_PER_CTX_PTR - Batch Buffer Per Context Pointer

3DSTATE_DX9_CONSTANTI_HS
3DSTATE_DX9_CONSTANTI_DS
3DSTATE_DX9_CONSTANTI_GS
3DSTATE_DX9_CONSTANTI_PS
3DSTATE_DX9_CONSTANTB_VS
3DSTATE_DX9_CONSTANTB_HS
3DSTATE_DX9_CONSTANTB_DS
3DSTATE_DX9_CONSTANTB_GS
3DSTATE_DX9_CONSTANTB_PS
3DSTATE_DX9_LOCAL_VALID_VS
3DSTATE_DX9_LOCAL_VALID_DS
3DSTATE_DX9_LOCAL_VALID_HS
3DSTATE_DX9_LOCAL_VALID_GS
3DSTATE_DX9_LOCAL_VALID_PS
3DSTATE_DX9_GENERATE_ACTIVE_VS
3DSTATE_DX9_GENERATE_ACTIVE_HS
3DSTATE_DX9_GENERATE_ACTIVE_DS
3DSTATE_DX9_GENERATE_ACTIVE_GS
3DSTATE_DX9_GENERATE_ACTIVE_PS
3DSTATE_BINDING_TABLE_EDIT_VS
3DSTATE_BINDING_TABLE_EDIT_GS
3DSTATE_BINDING_TABLE_EDIT_HS
3DSTATE_BINDING_TABLE_EDIT_DS
3DSTATE_BINDING_TABLE_EDIT_PS
3DSTATE_CONSTANT_VS
3DSTATE_CONSTANT_GS
3DSTATE_CONSTANT_PS
3DSTATE_CONSTANT_HS
3DSTATE_CONSTANT_DS

Workaround

Workaround :

To work around a known HW issue, SW must do the below Programming Sequence prior to programming MI_BATCH_BUFFER_END command in BB_PER_CTX_PTR. SW must ensure both MI_LOAD_REGISTER_REG and MI_BATCH_BUFFER_END commands mentioned in the below sequence are placed in the same cacheline of memory.

1. MI_LOAD_REGISTER_IMM: 0x00800000 à 0x20C0

BB_PER_CTX_PTR - Batch Buffer Per Context Pointer

2. MI_ATOMIC
 - a. Set "CS STALL" (Dword0[17])
 - b. "Return Data Control" enabled (Dword0[16])
 - c. "ATOMIC OPCODE" set to LOAD operation (Dword0[15:8]= 0x4)
 - d. "Memory Address" set to scratch space in GFX memory.
 - e. "Operand1 Data Dword 0" must be programmed to 0x0080_0080
3. MI_LOAD_REGISTER_MEM
 - a. Set "Async Mode Enable" (Dword0[21])
 - b. "Memory Address" set to same as in MI_ATOMIC command above.
 - c. "Register Address" set to 0x20C0
4. MI_LOAD_REGISTER_REG: 0x215C à 0x215C
5. MI_BATCH_BUFFER_END // Note that there shouldn't be any commands programmed between step4 & step5 and also these commands must be placed in the same cacheline of memory.

Additional Note:

This workaround need not be applied when Resource Streamer (RS) is not enabled or when a Resource Streamer enabled context is guaranteed not to be preempted.

- Preemption of RS enabled workload can be avoided by
- Bracketing the RS enabled workload with MI_ARB_ON_OFF (Arbitration Disable) and MI_ARB_ON_OFF (Arbitration Enable) command. MI_ARB_ON_OFF is a privileged command and can only be programmed in ring buffer or in privileged batch buffer (batch buffer in GGTT memory).
- Pending execlist submitted must not trigger preemption of the ongoing RS enabled workload due to following reasons
- First context of the pending execlist submitted is not the same as the ongoing RS enabled context.
- Force restore bit set for the submitted pending execlist.

BB_PER_CTX_PTR - Batch Buffer Per Context Pointer

DWord	Bit	Description		
0	31:12	<p>Batch Buffer Per Context Address</p> <table border="1"> <tr> <td>Format:</td> <td>U20</td> </tr> </table> <p>Pointer to the Context in memory to be executed as a batch.</p>	Format:	U20
Format:	U20			
11:2	<p>Reserved</p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ	
Format:	MBZ			
1	<p>RS Enabled Batch Buffer Per Context</p> <table border="1"> <tr> <td>Format:</td> <td>U1</td> </tr> </table> <p>If set, the command stream will enable the RS to parse commands.</p> <p>Programming Notes</p> <p>This must be set when programming the resource streamer pool commands (3DSTATE_BINDING_TABLE_POOL_ALLOC, 3DSTATE_GATHER_POOL_ALLOC, and 3DSTATE_DX9_CONSTANT_BUFFER_POOL_ALLOC) in order for the pool alloc fields to be valid in both the render engine and resource streamer.</p>	Format:	U1	
Format:	U1			
0	<p>Batch Buffer Per Context Valid</p> <table border="1"> <tr> <td>Format:</td> <td>U1</td> </tr> </table> <p>If set, the command stream will execute the context from the Batch Buffer Per Context Address prior to the execution of actual submitted workloads.</p>	Format:	U1	
Format:	U1			

Batch Buffer Start Head Pointer Register

BB_START_ADDR - Batch Buffer Start Head Pointer Register

Register Space: MMIO: 0/2/0

Project: BDW

Source: RenderCS

Default Value: 0x00000000

Access: R/W

Size (in bits): 32

Address: 02150h

This register contains the address specified in the last MI_START_BATCH_BUFFER command.

Programming Notes

Programming Restriction:

This register should NEVER be programmed by driver, this is for HW internal use only.

DWord	Bit	Description		
0	31:2	<p>Batch Buffer Start Head Pointer</p> <table border="1"> <tr> <td>Format:</td> <td>GraphicsAddress[31:2]</td> </tr> </table> <p>This field specifies the DWord-aligned Graphics Memory Address where the last initiated Batch Buffer starting address.</p>	Format:	GraphicsAddress[31:2]
Format:	GraphicsAddress[31:2]			
<p>Preempted Batch Buffer RS Control Stop Flag</p> <table border="1"> <tr> <td>Format:</td> <td>Flag</td> </tr> </table> <p>This field specifies RS Control Stop Flag when a batch buffer is preempted. This is for HW internal use and should not be written by SW. This bit gets reset when RS_PREEMPTED field of RS_PREEMPT_STATUS is written Zero. This bit is set by:</p> <ul style="list-style-type: none"> • Ctx restore of this bit • MI_RS_CONTROL_STOP (except for the ctx restore command) <p>This bit is cleared by:</p> <ul style="list-style-type: none"> • MI_RS_CONTROL_START • Any Batch start except resubmitted RS batch • A batch end that doesn't include preemption • Ctx save <p>Writing 0 to bit[0] of the RS STATUS register</p>	Format:	Flag		
Format:	Flag			
0	<p>Reserved</p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ	
Format:	MBZ			

Batch Buffer Start Head Pointer Register for Upper DWord

BB_START_ADDR_UDW - Batch Buffer Start Head Pointer Register for Upper DWord				
Register Space:	MMIO: 0/2/0			
Project:	BDW			
Source:	RenderCS			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Address:	02170h			
This register contains the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space specified in the last MI_START_BATCH_BUFFER command.				
Programming Notes				
Programming Restriction: This register should NEVER be programmed by driver, this is for HW internal use only.				
DWord	Bit	Description		
0	31:16	Reserved <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Format:</td><td style="width: 50%;">MBZ</td></tr> </table>	Format:	MBZ
	Format:	MBZ		
15:0	Batch Buffer Start Head Pointer Upper DWORD <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Format:</td><td style="width: 50%;">GraphicsAddress[47:32]</td></tr> </table> <p>This field specifies the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space for the last initiated Batch Buffer starting address.</p>	Format:	GraphicsAddress[47:32]	
Format:	GraphicsAddress[47:32]			

Batch Buffer State Register

BB_STATE - Batch Buffer State Register						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000 [BDW]					
Access:	RO					
Size (in bits):	32					
Address:	02110h-02113h					
Name:	Batch Buffer State Register					
ShortName:	BB_STATE_RCSUNIT					
Address:	12110h-12113h					
Name:	Batch Buffer State Register					
ShortName:	BB_STATE_VCSUNIT0					
Address:	1A110h-1A113h					
Name:	Batch Buffer State Register					
ShortName:	BB_STATE_VECSUNIT					
Address:	1C110h-1C113h					
Name:	Batch Buffer State Register					
ShortName:	BB_STATE_VCSUNIT1					
Address:	22110h-22113h					
Name:	Batch Buffer State Register					
ShortName:	BB_STATE_BCSUNIT					
This register contains the attributes of the current batch buffer initiated from the Ring Buffer.						
This register should not be written by software. These fields should only get written by a context restore. Software should always set these fields via the MI_BATCH_BUFFER_START command when initiating a batch buffer. This register is saved and restored with context.						
DWord	Bit	Description				
0	31:8	Reserved				
		Project:	All			
	7	Reserved				
		Project:	All			
		Source:	BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS			
		Format:	MBZ			

BB_STATE - Batch Buffer State Register

	7	Resource Streamer Enable									
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Source:</td><td>RenderCS</td></tr> <tr> <td>Format:</td><td>U1</td></tr> </table>	Project:	BDW	Source:	RenderCS	Format:	U1			
Project:	BDW										
Source:	RenderCS										
Format:	U1										
		When this bit is set, the Resource Streamer will execute the batch buffer. When this bit is clear the Resource Streamer will not execute the batch buffer.									
	6	Reserved									
	6	2nd Level Buffer Security Indicator									
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Source:</td><td>VideoCS, VideoCS2</td></tr> <tr> <td>Exists If:</td><td>//VCS, VCS2</td></tr> </table>	Project:	BDW	Source:	VideoCS, VideoCS2	Exists If:	//VCS, VCS2			
Project:	BDW										
Source:	VideoCS, VideoCS2										
Exists If:	//VCS, VCS2										
		If set, VCS is fetching 2nd level batch commands from a PPGTT address space. If clear, GGTT. If execlists are enabled and this is set, the batch buffer is non-secure and cannot execute privileged commands nor access privileged (GGTT) memory. It will be accessed via the PPGTT. If clear, this batch buffer is secure and will be accessed via the GGTT. Note: When execlists are enabled this field reflects the effective security level and may not be the same as the Buffer Security Indicator written using MI_BATCH_BUFFER_START.									
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0h</td><td>MIBUFFER_SECURE [Default]</td><td>Located in GGTT memory</td></tr> <tr> <td>1h</td><td>MIBUFFER_NONSECURE</td><td>Located in PPGTT memory</td></tr> </tbody> </table>	Value	Name	Description	0h	MIBUFFER_SECURE [Default]	Located in GGTT memory	1h	MIBUFFER_NONSECURE	Located in PPGTT memory
Value	Name	Description									
0h	MIBUFFER_SECURE [Default]	Located in GGTT memory									
1h	MIBUFFER_NONSECURE	Located in PPGTT memory									
	6	2nd Level Buffer Security Indicator									
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Source:</td><td>BlitterCS, VideoEnhancementCS</td></tr> <tr> <td>Exists If:</td><td>//BCS, VECS</td></tr> <tr> <td>Format:</td><td>MI_2ndBufferSecurityType</td></tr> </table>	Project:	BDW	Source:	BlitterCS, VideoEnhancementCS	Exists If:	//BCS, VECS	Format:	MI_2ndBufferSecurityType	
Project:	BDW										
Source:	BlitterCS, VideoEnhancementCS										
Exists If:	//BCS, VECS										
Format:	MI_2ndBufferSecurityType										
		If set, VECS is fetching 2nd level batch commands from a PPGTT address space. If clear, GGTT. If execlists are enabled and this is set, the batch buffer is non-secure and cannot execute privileged commands nor access privileged (GGTT) memory. It will be accessed via the PPGTT. If clear, this batch buffer is secure and will be accessed via the GGTT.									
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0h</td><td>MIBUFFER_SECURE [Default]</td><td>Located in GGTT memory</td></tr> <tr> <td>1h</td><td>MIBUFFER_NONSECURE</td><td>Located in PPGTT memory</td></tr> </tbody> </table>	Value	Name	Description	0h	MIBUFFER_SECURE [Default]	Located in GGTT memory	1h	MIBUFFER_NONSECURE	Located in PPGTT memory
Value	Name	Description									
0h	MIBUFFER_SECURE [Default]	Located in GGTT memory									
1h	MIBUFFER_NONSECURE	Located in PPGTT memory									
		Programming Notes									
		When execlists are enabled, this field reflects the effective security level and may not be the same as the Buffer Security Indicator written using MI_BATCH_BUFFER_START.									

BB_STATE - Batch Buffer State Register

	5	Address Space Indicator									
		<table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> </table> <p>Note: This field reflects the effective address space indicator security level and may not be the same as the Address Space Indicator written using MI_BATCH_BUFFER_START.</p>	Project:	BDW							
Project:	BDW										
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>GGTT [Default]</td> <td>This Batch buffer is located in GGTT memory and is privileged</td> </tr> <tr> <td>1h</td> <td>PPGTT</td> <td>This Batch buffer is located in PPGTT memory and is non-privileged.</td> </tr> </tbody> </table>	Value	Name	Description	0h	GGTT [Default]	This Batch buffer is located in GGTT memory and is privileged	1h	PPGTT	This Batch buffer is located in PPGTT memory and is non-privileged.
Value	Name	Description									
0h	GGTT [Default]	This Batch buffer is located in GGTT memory and is privileged									
1h	PPGTT	This Batch buffer is located in PPGTT memory and is non-privileged.									
	4	Reserved									
	4	Reserved									
		<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Source:</td> <td>BlitterCS</td> </tr> <tr> <td>Exists If:</td> <td>//BCS</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	All	Source:	BlitterCS	Exists If:	//BCS	Format:	MBZ	
Project:	All										
Source:	BlitterCS										
Exists If:	//BCS										
Format:	MBZ										
	3:0	Reserved									
		<table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	All	Format:	MBZ					
Project:	All										
Format:	MBZ										

Batch Buffer Upper Head Pointer Preemption Register

BB_PREAMPT_ADDR_UDW - Batch Buffer Upper Head Pointer Preemption Register

Register Space:	MMIO: 0/2/0
Project:	BDW
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	0216Ch-0216Fh
Name:	Batch Buffer Upper Head Pointer Preemption Register
ShortName:	BB_PREAMPT_ADDR_UDW_RCSUNIT
Address:	1216Ch-1216Fh
Name:	Batch Buffer Upper Head Pointer Preemption Register
ShortName:	BB_PREAMPT_ADDR_UDW_VCSUNIT0
Address:	1A16Ch-1A16Fh
Name:	Batch Buffer Upper Head Pointer Preemption Register
ShortName:	BB_PREAMPT_ADDR_UDW_VECSUNIT
Address:	1C16Ch-1C16Fh
Name:	Batch Buffer Upper Head Pointer Preemption Register
ShortName:	BB_PREAMPT_ADDR_UDW_VCSUNIT1
Address:	2216Ch-2216Fh
Name:	Batch Buffer Upper Head Pointer Preemption Register
ShortName:	BB_PREAMPT_ADDR_UDW_BCSUNIT
This register contains the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space of the last preempted batch buffer. This register follows the same rules as the BB_PREAMPT_ADDR register.	

Programming Notes

Programming Restriction: This register should NEVER be programmed by driver, this is for HW internal use only.

DWord	Bit	Description
0	31:16	Reserved
	Format:	MBZ
15:0	Batch Buffer Head Pointer Upper DWORD	
	Format:	GraphicsAddress[47:32]
This field specifies the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space of the last preempted batch buffer.		

Batch Buffer Upper Head Pointer Register

BB_ADDR_UDW - Batch Buffer Upper Head Pointer Register		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Address:	02168h-0216Bh	
Name:	Batch Buffer Upper Head Pointer Register	
ShortName:	BB_ADDR_UDW_RCSUNIT	
Address:	12168h-1216Bh	
Name:	Batch Buffer Upper Head Pointer Register	
ShortName:	BB_ADDR_UDW_VCSUNIT0	
Address:	1A168h-1A16Bh	
Name:	Batch Buffer Upper Head Pointer Register	
ShortName:	BB_ADDR_UDW_VECSUNIT	
Address:	1C168h-1C16Bh	
Name:	Batch Buffer Upper Head Pointer Register	
ShortName:	BB_ADDR_UDW_VCSUNIT1	
Address:	22168h-2216Bh	
Name:	Batch Buffer Upper Head Pointer Register	
ShortName:	BB_ADDR_UDW_BCSUNIT	
This register contains the current Upper DWord of Graphics Memory Address of the last-initiated batch buffer.		
Programming Restriction:		
This register should NEVER be programmed by driver. This is for HW internal use only.		
DWord	Bit	Description
0	31:16	Reserved Format: <input type="text"/> MBZ
	15:0	Batch Buffer Head Pointer Upper DWORD Format: <input type="text"/> GraphicsAddress[47:32] This field specifies the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space where the last initiated Batch Buffer is currently fetching commands. If no batch buffer is currently active, the Valid bit in BB_ADDR will be 0 and this field is meaningless.

BCS_PREEMPTION_HINT

BCS_PREEMPTION_HINT - BCS_PREEMPTION_HINT

Register Space: MMIO: 0/2/0

Project: BDW

Source: BlitterCS

Default Value: 0x00000000

Access: R/W

Size (in bits): 32

Address: 224BCh

This register contains the Head pointer offset in to the Ring Buffer or the Dword aligned Graphics address in to the Batch Buffer corresponding to either MI_ARB_CHECK called Preemption Hint Address. When Preemption Hint Address is enabled, BCS will honor UHPTTR only on parsing MI_ARB_CHK at Preemption Hint Address.

This register contains the Head pointer offset into the Ring Buffer or the Dword aligned Graphics address into the Batch Buffer corresponding to the below listed commands in execlist mode of operation

- MI_ARB_CHECK
- MI_WAIT_FOR_EVENT
- MI_SEMAPHORE_WAIT

Programming Notes

Programming Restriction: This register should NEVER be programmed in functional mode, this should be used only in validation mode to achieve deterministic behavior of UHPTTR being sampled by a given MI_ARB_CHECK in command stream. Programmer has to ensure that BCS Preemption Hint register gets programmed before UHPTTR is programmed and well before BCS crosses the corresponding execution point. Preemption hint for both RingBuffer and Batch Buffer can't be enabled simultaneously.

DWord	Bit	Description				
0	31:2	Preempted Hint Address <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Format:</td><td style="padding: 2px;">U30</td></tr> <tr> <td style="padding: 2px;">Format:</td><td style="padding: 2px;">GraphicsAddress[31:2]</td></tr> </table> <p>This field contains the Head offset in to the Ring Buffer when Preemption Hint is set to Ring Buffer and Dword aligned Graphics Address in to the batch buffer when Preemption Hint is set to Batch Buffer.</p>	Format:	U30	Format:	GraphicsAddress[31:2]
Format:	U30					
Format:	GraphicsAddress[31:2]					
	1	Batch Buffer Preemption Hint <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Format:</td><td style="padding: 2px; text-align: center;">Enable</td></tr> </table>	Format:	Enable		
Format:	Enable					
Value	Name	Description				
0h	Disabled	Preemption hint is disabled in batch buffer.				
1h	Enabled	Preemption hint is enabled in ring buffer and preemption hint address corresponds to the instruction in Batch Buffer.				

BCS_PREEMPTION_HINT - BCS_PREEMPTION_HINT

	0	Ring Preemption Hint									
		<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Format:</td> <td style="padding: 2px; text-align: right;">Enable</td> </tr> </table>	Format:	Enable							
Format:	Enable										
		<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="background-color: #d9e1f2; width: 10%;">Value</th><th style="background-color: #d9e1f2; width: 10%;">Name</th><th style="background-color: #d9e1f2; width: 80%;">Description</th></tr> </thead> <tbody> <tr> <td style="text-align: center;">0h</td><td style="text-align: center;">Disable</td><td>Preemption hint is disabled in ring buffer.</td></tr> <tr> <td style="text-align: center;">1h</td><td style="text-align: center;">Enabled</td><td>Preemption hint is enabled in ring buffer and preemption hint address corresponds to the instruction in Ring Buffer.</td></tr> </tbody> </table>	Value	Name	Description	0h	Disable	Preemption hint is disabled in ring buffer.	1h	Enabled	Preemption hint is enabled in ring buffer and preemption hint address corresponds to the instruction in Ring Buffer.
Value	Name	Description									
0h	Disable	Preemption hint is disabled in ring buffer.									
1h	Enabled	Preemption hint is enabled in ring buffer and preemption hint address corresponds to the instruction in Ring Buffer.									

BCS_PREEMPTION_HINT_UDW

BCS_PREEMPTION_HINT_UDW - BCS_PREEMPTION_HINT_UDW				
Register Space:	MMIO: 0/2/0			
Project:	BDW			
Source:	BlitterCS			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Address:	224C8h			
<p>This register contains the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space of the Batch Buffer corresponding to MI_ARB_CHECK command called Preemption Hint Address.</p>				
Programming Notes				
Programming Restriction: This register should NEVER be programmed in functional mode, this should be used only in validation mode to achieve deterministic behavior of UHPTR being sampled by a given MI_ARB_CHK in command stream.				
DWord	Bit	Description		
0	31:16	Reserved <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Format:</td><td style="width: 50%;">MBZ</td></tr> </table>	Format:	MBZ
	Format:	MBZ		
15:0	Preempted Hint Address Upper DWORD <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Format:</td><td style="width: 50%;">GraphicsAddress[47:32]</td></tr> </table> <p>This field contains the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space of the batch buffer when Preemption Hint is set to Batch Buffer. This field is not valid when Preemption Hint is set to Ring Buffer.</p>	Format:	GraphicsAddress[47:32]	
Format:	GraphicsAddress[47:32]			

BCS Active Upper Head Pointer Register

BCS_ACTHD_UDW - BCS Active Upper Head Pointer Register					
Register Space:	MMIO: 0/2/0				
Project:	BDW				
Source:	BlitterCS				
Default Value:	0x00000000				
Access:	RO				
Size (in bits):	32				
Address:	2205Ch				
This register contains the Head "Pointer" (4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space) of the currently-active batch buffer.					
DWord	Bit	Description			
0	31:16	Reserved <table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ	
Format:	MBZ				
15:0	Head Pointer Upper DWORD <table border="1"> <tr> <td>Default Value:</td><td>0h</td></tr> <tr> <td>Format:</td><td>GraphicsAddress[47:32]</td></tr> </table> <p>4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space corresponding to the Head Pointer of the currently-active batch buffer.</p>	Default Value:	0h	Format:	GraphicsAddress[47:32]
Default Value:	0h				
Format:	GraphicsAddress[47:32]				

BCS Context ID Preemption Hint

BCS_CTXID_PREEMPTION_HINT - BCS Context ID Preemption Hint				
Register Space:	MMIO: 0/2/0			
Project:	BDW			
Source:	BlitterCS			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Address:	224CCh			
<p>This register contains the Context ID of a context in exelist mode of operation. In exelist mode of operation BCS_PREEMPTION_HINT registers are looked at by Blitter Command Streamer on executing a context having Context ID that matches with the contents of this register. This register contents are valid and looked at only in exelist mode of operation.</p>				
Programming Notes				
<p>This register should NEVER be programmed in functional mode, this must be used only in validation mode to achieve deterministic preemption behavior in exelist mode of operation.</p>				
DWord	Bit	Description		
0	31:0	<p>Context ID Preemption Hint</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Format:</td><td style="padding: 2px; text-align: right;">U32</td></tr> </table> <p>If 0 this field has no effect. If nonzero it indicates the only context ID that can be preempted when execlists are enabled. A preemption attempt when the context ID of the currently executing ring context does not match this field will be ignored.</p>	Format:	U32
Format:	U32			

BCS Context Sizes

BCS_CXT_SIZE - BCS Context Sizes												
DWord	Bit	Description										
0	31:13	Reserved <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	All	Format:	MBZ						
Project:	All											
Format:	MBZ											
	12:8	BCS Context Size <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U5</td></tr> </table> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Project</th></tr> </thead> <tbody> <tr> <td>Ah</td><td>[Default]</td><td>BDW</td></tr> </tbody> </table>	Project:	All	Format:	U5	Value	Name	Project	Ah	[Default]	BDW
Project:	All											
Format:	U5											
Value	Name	Project										
Ah	[Default]	BDW										
	7:5	Reserved <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	All	Format:	MBZ						
Project:	All											
Format:	MBZ											
	4:0	Exclist Context Size <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>U5</td></tr> </table> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Project</th></tr> </thead> <tbody> <tr> <td>5h</td><td>[Default]</td><td>BDW</td></tr> </tbody> </table>	Project:	BDW	Format:	U5	Value	Name	Project	5h	[Default]	BDW
Project:	BDW											
Format:	U5											
Value	Name	Project										
5h	[Default]	BDW										

BCS Context Timestamp Count

BCS_CTX_TIMESTAMP - BCS Context Timestamp Count						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Source:	BlitterCS					
Default Value:	0x00000000					
Access:	R/W					
Size (in bits):	32					
Address:	223A8h					
<p>This register provides a mechanism to obtain cumulative run time of a GPU context on HW. This register gets context save/restored on a context switch. SW must reset this register on very first submission of a context to HW, then afterwards gets context save/restored maintaining the cumulative run time of the corresponding context. Note that the value of this register can be obtained in a 3D pipeline-synchronous fashion without a pipeline flush by using the PIPE_CONTROL command. See 3D Geometry Pipeline in the "3D and Media" volume. This register (effectively) counts at a constant frequency by adjusting the increment amount according to the actual reference clock frequency. SW therefore does not need to know the reference clock frequency. This register gets reset on an engine reset.</p>						
This register is context save restore on a context switch.						
DWord	Bit	Description				
0	31:0	<p>Timestamp Value</p> <table border="1"> <tr> <td>Format:</td><td>U32</td></tr> <tr> <td colspan="2">This register increments for every 80 ns of time.</td></tr> </table>	Format:	U32	This register increments for every 80 ns of time.	
Format:	U32					
This register increments for every 80 ns of time.						

BCS Counter for the Blitter Engine

BCS_CNTR - BCS Counter for the Blitter Engine				
Register Space: MMIO: 0/2/0				
Project: BDW				
Source: BlitterCS				
Default Value: 0xFFFFFFFF				
Access: R/W				
Size (in bits): 32				
Address: 22178h				
DWord	Bit	Description		
0	31:0	<p>Count Value</p> <table border="1"> <tr> <td>Default Value:</td> <td>ffffffffffh</td> </tr> </table> <p>Writing a Zero value to this register starts the counting. Writing a Value of FFFF FFFF to this counter stops the counter.</p>	Default Value:	ffffffffffh
Default Value:	ffffffffffh			

BCS Error Identity Register

BCS_EIR - BCS Error Identity Register														
Register Space: MMIO: 0/2/0 Project: BDW Source: BlitterCS Default Value: 0x00000000 Access: R/WC Size (in bits): 32														
Address: 220B0h														
The EIR register contains the persistent values of Hardware-Detected Error Condition bits. Any bit set in this register will cause the Master Error bit in the ISR to be set. The EIR register is also used by software to clear detected errors (by writing a '1' to the appropriate bit(s) except for the unrecoverable bits described.).														
DWord	Bit	Description												
0	31:16	Reserved <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	All	Format:	MBZ								
Project:	All													
Format:	MBZ													
15:0	Error Identity Bits <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>Array of Error condition bits See Table 1 5. Hardware-Detected Error Bits</td></tr> </table> <p>This register contains the persistent values of ESR error status bits that are unmasked via the EMR register. The logical OR of all (defined) bits in this register is reported in the Master Error bit of the Interrupt Status Register. To clear an error condition, software must first clear the error by writing a '1' to the appropriate bit(s) in this field. If required, software should then proceed to clear the Master Error bit of the IIR.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0h</td><td>[Default]</td><td></td></tr> <tr> <td>1h</td><td>Error occurred</td><td>Error occurred</td></tr> </tbody> </table>	Project:	All	Format:	Array of Error condition bits See Table 1 5. Hardware-Detected Error Bits	Value	Name	Description	0h	[Default]		1h	Error occurred	Error occurred
Project:	All													
Format:	Array of Error condition bits See Table 1 5. Hardware-Detected Error Bits													
Value	Name	Description												
0h	[Default]													
1h	Error occurred	Error occurred												
Programming Notes														
Writing a '1' to a set bit will cause that error condition to be cleared. However, the Instruction Error bit (Bit 0) cannot be cleared except by reset (i.e., it is a fatal error).														

BCS Error Mask Register

BCS_EMR - BCS Error Mask Register		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Source:	BlitterCS 0xFFFFFFFF [BDW]	
Access:	R/W	
Size (in bits):	32	
Address:	220B4h	
<p>The EMR register is used by software to control which Error Status Register bits are "masked" or "unmasked". "Unmasked" bits will be reported in the EIR, thus setting the Master Error ISR bit and possibly triggering a CPU interrupt, and will persist in the EIR until cleared by software. "Masked" bits will not be reported in the EIR and therefore cannot generate Master Error conditions or CPU interrupts.</p> <p>Undefined or reserved bits in the Hardware Detected Error Bit Table will always return a read value of '1'</p>		
DWord	Bit	Description
0	31:16	Reserved
		Default Value: FFFFh
		Project: BDW
	15:0	Error Mask Bits Project: All Format: Array of error condition mask bits See Table 1.5. Hardware-Detected Error Bits This register contains a bit mask that selects which error condition bits (from the ESR) are reported in the EIR.
Value	Name	Description
0000h	Not Masked	Will be reported in the EIR
FFFFh	Masked [Default]	Will not be reported in the EIR

BCS Error Status Register

BCS_ESR - BCS Error Status Register			
Register Space: MMIO: 0/2/0 Project: BDW Source: BlitterCS Default Value: 0x00000000 Access: RO Size (in bits): 32			
Address: 220B8h			
The ESR register contains the current values of all Hardware-Detected Error condition bits (these are all by definition "persistent"). The EMR register selects which of these error conditions are reported in the persistent EIR (i.e., set bits must be cleared by software) and thereby causing a Master Error interrupt condition to be reported in the ISR.			
DWord	Bit	Description	
0	31:16	Reserved	
		Project:	All
	15:0	Error Status Bits	
		Project:	All
		Format:	Array of error condition bits See Table 1 5. Hardware-Detected Error Bits
		This register contains the non-persistent values of all hardware-detected error condition bits.	
Value	Name	Description	Project
0h	[Default]		
1h	Error Condition Detected	Error Condition detected	All

BCS Execute Condition Code Register

BCS_EXCC - BCS Execute Condition Code Register

Register Space: MMIO: 0/2/0

Project: BDW

Source: BlitterCS

Default Value: 0x00000000

Access: R/W, RO

Size (in bits): 32

Trusted Type: 1

Address: 22028h

This register contains user defined and hardware generated conditions that are used by MI_WAIT_FOR_EVENT commands. An MI_WAIT_FOR_EVENT instruction excludes the executing ring from arbitration if the selected event evaluates to a 1, while instruction is discarded if the condition evaluates to a 0. Once excluded, a ring is enabled into arbitration when the selected condition evaluates to a 0. This register also contains control for the invalidation of indirect state pointers on context restore.

DWord	Bit	Description		
0	31:16	Mask Bits		
		Format:	Mask[15:0]	
		These bits serve as a write enable for bits 15:0. If this register is written with any of these bits clear the corresponding bit in the field 15:0 will not be modified. Reading these bits always returns 0s.		
	15	Reserved		
		Format:	MBZ	
	14	Context Wait for V-blank on Pipe-C		
		Project:	BDW	
			This field when set indicates the corresponding context has executed MI_WAIT_FOR_EVENT with "Display Pipe C Vertical Blank Wait Enable" set. This is an internal HW flag and should not be accessed by SW.	
13	Context Wait for V-blank on Pipe-B			
		Project:	BDW	
			This field when set indicates the corresponding context has executed MI_WAIT_FOR_EVENT with "Display Pipe B Vertical Blank Wait Enable" set. This is an internal HW flag and should not be accessed by SW.	
12	Context Wait for V-blank on Pipe-A			
		Project:	BDW	
			This field when set indicates the corresponding context has executed MI_WAIT_FOR_EVENT with "Display Pipe A Vertical Blank Wait Enable" set. This is an internal HW flag and should not be accessed by SW.	
11:5	Reserved			
		Format:	MBZ	

BCS_EXCC - BCS Execute Condition Code Register

	4:0	Reserved
		Project: BDW
		Format: MBZ

BCS General Purpose Register

BCS_GPR - BCS General Purpose Register			
Register Space:	MMIO: 0/2/0		
Project:	BDW		
Source:	BlitterCS		
Default Value:	0x00000000, 0x00000000		
Access:	R/W		
Size (in bits):	64		
Address:	22600h-2267Fh		
This is a general purpose register bank of sixteen 64-bit registers, used as temporary storage by the MI_MATH command to do ALU operations.			
Programming Notes			
Any operation that initiates a read to register 0x2266C will return the value of 0x2260c register. This does not include context save or MI_MATH command operation.	BDW		
DWord	Bit	Description	
0	63:0	Reserved	Format: MBZ

BCS Hardware Status Mask Register

BCS_HWSTAM - BCS Hardware Status Mask Register								
Register Space:	MMIO: 0/2/0							
Project:	BDW							
Source:	BlitterCS							
Default Value:	0xFFFFFFFF							
Access:	R/W							
Size (in bits):	32							
Trusted Type:	1							
Address:	22098h							
Access: RO for Reserved Control bits								
<p>The HWSTAM register has the same format as the Interrupt Control Registers. The bits in this register are "mask" bits that prevent the corresponding bits in the Interrupt Status Register from generating a "Hardware Status Write" (PCI write cycle). Any unmasked interrupt bit (HWSTAM bit set to 0) will allow the Interrupt Status Register to be written to the ISR location (within the memory page specified by the Hardware Status Page Address Register) when that Interrupt Status Register bit changes state.</p>								
Programming Notes								
<p>To write the interrupt to the HWSP, the corresponding IMR bit must also be clear (enabled). At most 1 bit can be unmasked at any given time.</p>								
DWord	Bit	Description						
0	31:0	Hardware Status Mask Register <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Default Value:</td><td style="padding: 2px;">FFFFFFFFFFh</td></tr> <tr> <td style="padding: 2px;">Project:</td><td style="padding: 2px;">All</td></tr> <tr> <td style="padding: 2px;">Format:</td><td style="padding: 2px;">Array of Masks</td></tr> </table> <p style="margin-top: 2px;">refer to Table 5-1 in Interrupt Control Register section for bit definitions</p>	Default Value:	FFFFFFFFFFh	Project:	All	Format:	Array of Masks
Default Value:	FFFFFFFFFFh							
Project:	All							
Format:	Array of Masks							

BCS Idle Switch Delay

BCS_IDLEDLY - BCS Idle Switch Delay						
DWord	Bit	Description				
0	31:21	Reserved <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	All	Format:	MBZ
Project:	All					
Format:	MBZ					
20:0	IDLE Delay <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U21</td></tr> </table> <p>Minimum number of micro-seconds allowed</p>	Project:	All	Format:	U21	
Project:	All					
Format:	U21					

BCS Instruction Parser Mode Register

BCS_INSTPM - BCS Instruction Parser Mode Register					
Register Space: MMIO: 0/2/0					
Project: BDW					
Source: BlitterCS					
Default Value: 0x00000000					
Access: R/W					
Size (in bits): 32					
Trusted Type: 1					
Address: 220C0h					
Desc					
DWord	Bit	Description			
0	31:16	Mask Bits <table border="1"> <tr> <td>Format:</td><td>Mask[15:0]</td></tr> </table> <p>Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)</p>	Format:	Mask[15:0]	
Format:	Mask[15:0]				
15:11	Reserved <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	All	Format:	MBZ
Project:	All				
Format:	MBZ				
10	Reserved <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	BDW	Format:	MBZ
Project:	BDW				
Format:	MBZ				
9	Reserved <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	BDW	Format:	MBZ
Project:	BDW				
Format:	MBZ				
8:7	Reserved <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	All	Format:	MBZ
Project:	All				
Format:	MBZ				
6:5	Reserved <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	BDW	Format:	MBZ
Project:	BDW				
Format:	MBZ				
4:0	Reserved <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	All	Format:	MBZ
Project:	All				
Format:	MBZ				

BCS Interrupt Mask Register

BCS_IMR - BCS Interrupt Mask Register																							
DWord	Bit	Description																					
0	31:0	Interrupt Mask Bits																					
<table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>Array of interrupt mask bits Refer to Table 5-1 in Interrupt Control Register section for bit definitions</td></tr> </table> <p>This field contains a bit mask which selects which interrupt bits (from the ISR) are reported in the IIR.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th><th>Project</th></tr> </thead> <tbody> <tr> <td>FFFF FFFFh</td><td>[Default]</td><td></td><td></td></tr> <tr> <td>0h</td><td>Not Masked</td><td>Will be reported in the IIR</td><td>All</td></tr> <tr> <td>1h</td><td>Masked</td><td>Will not be reported in the IIR</td><td>All</td></tr> </tbody> </table>				Project:	All	Format:	Array of interrupt mask bits Refer to Table 5-1 in Interrupt Control Register section for bit definitions	Value	Name	Description	Project	FFFF FFFFh	[Default]			0h	Not Masked	Will be reported in the IIR	All	1h	Masked	Will not be reported in the IIR	All
Project:	All																						
Format:	Array of interrupt mask bits Refer to Table 5-1 in Interrupt Control Register section for bit definitions																						
Value	Name	Description	Project																				
FFFF FFFFh	[Default]																						
0h	Not Masked	Will be reported in the IIR	All																				
1h	Masked	Will not be reported in the IIR	All																				

BCS Mode Register for Software Interface

BCS_MI_MODE - BCS Mode Register for Software Interface														
Register Space:	MMIO: 0/2/0													
Project:	BDW													
Source:	BlitterCS 0x00000200 [BDW]													
Access:	R/W													
Size (in bits):	32													
Address:	2209Ch-2209Fh													
The MI_MODE register contains information that controls software interface aspects of the command parser.														
DWord	Bit	Description												
0	31:16	Masks A 1 in a bit in this field allows the modification of the corresponding bit in Bits 15:0												
	15	Suspend Flush <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td colspan="2">Mask: MMIO(0x209c)#31</td></tr> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> <tr> <td>0h</td><td>No Delay</td><td>HW will not delay flush, this bit will get cleared by MI_SUSPEND_FLUSH as well</td></tr> <tr> <td>1h</td><td>Delay Flush</td><td>Suspend flush is active</td></tr> </table>	Project:	All	Mask: MMIO(0x209c)#31		Value	Name	Description	0h	No Delay	HW will not delay flush, this bit will get cleared by MI_SUSPEND_FLUSH as well	1h	Delay Flush
Project:	All													
Mask: MMIO(0x209c)#31														
Value	Name	Description												
0h	No Delay	HW will not delay flush, this bit will get cleared by MI_SUSPEND_FLUSH as well												
1h	Delay Flush	Suspend flush is active												
14:12	Reserved Read/Write													
11	Invalidate UHPT enable If bit set H/W clears the valid bit of BCS_UHPT (4134h, bit 0) when current active head pointer is equal to UHPT.													
10	Atomic Read Return for MI_COPY_MEM_MEM <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> <tr> <td>0h</td><td>Disable [Default]</td><td>Hardware does a regular memory fence write to complete the write to the destination address before moving to the next instruction.</td></tr> <tr> <td>1h</td><td>Enable</td><td>Hardware does Atomic Move with Read Return to complete the write to the destination address before moving to the next instruction.</td></tr> </table>	Project:	BDW	Value	Name	Description	0h	Disable [Default]	Hardware does a regular memory fence write to complete the write to the destination address before moving to the next instruction.	1h	Enable	Hardware does Atomic Move with Read Return to complete the write to the destination address before moving to the next instruction.		
Project:	BDW													
Value	Name	Description												
0h	Disable [Default]	Hardware does a regular memory fence write to complete the write to the destination address before moving to the next instruction.												
1h	Enable	Hardware does Atomic Move with Read Return to complete the write to the destination address before moving to the next instruction.												
9	Ring Idle (Read Only Status Bit) <i>Writes to this bit are not allowed.</i> <table border="1"> <tr> <th>Value</th><th>Name</th></tr> <tr> <td>0</td><td>Parser not idle</td></tr> <tr> <td>1</td><td>Parser idle [Default]</td></tr> </table>	Value	Name	0	Parser not idle	1	Parser idle [Default]							
Value	Name													
0	Parser not idle													
1	Parser idle [Default]													
8	MI_FLUSH This bit is used to flush the command parser. It is a write-only bit.													
7	MI_FLUSH_FLUSH This bit is used to flush the command parser. It is a write-only bit.													
6	MI_FLUSH_FLUSH_FLUSH This bit is used to flush the command parser. It is a write-only bit.													
5	MI_FLUSH_FLUSH_FLUSH_FLUSH This bit is used to flush the command parser. It is a write-only bit.													

BCS_MI_MODE - BCS Mode Register for Software Interface

	8	Stop Ring Software must set this bit to force the Ring and Command Parser to Idle. Software must read a 1 in Ring Idle bit after setting this bit to ensure that the hardware is idle. <i>Software must clear this bit for Ring to resume normal operation.</i>						
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Normal Operation [Default]</td> </tr> <tr> <td>1</td> <td>Parser is turned off</td> </tr> </tbody> </table>	Value	Name	0	Normal Operation [Default]	1	Parser is turned off
Value	Name							
0	Normal Operation [Default]							
1	Parser is turned off							
	7:2	Reserved Read/Write						
	1	Bypass Fence Write If set, this bit will bypass all writes during flushes, independent of programming. This includes post-sync op bits, the implicit TLB invalidate write (set in GFX_MODE[13]), and sync flush fences. <i>Note this is only intended for work-arounds</i>						
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Normal Operation</td> </tr> <tr> <td>1</td> <td>Bypass</td> </tr> </tbody> </table>	Value	Name	0	Normal Operation	1	Bypass
Value	Name							
0	Normal Operation							
1	Bypass							
	0	Reserved Read/Write						

BCS Primary DMA Engine Fetch Upper Address

BCS_DMA_FADD_P_UDW - BCS Primary DMA Engine Fetch Upper Address		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Source:	BlitterCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Address:	22060h	
This register contains the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space of the instruction being fetched by the Primary DMA engine. This register contents are valid only when Batch Buffer is active.		
DWord	Bit	Description
0	31:16	Reserved Format: MBZ
	15:0	Current DMA Address Upper DWORD Format: GraphicsAddress[47:32] This field contains 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space of the batch buffer that the "Primary" instruction parser DMA engine is currently accessing (fetching). Note that this address will typically lead the Head offset (as instructions must be fetched before execution).

BCS Reported Timestamp Count

BCS_TIMESTAMP - BCS Reported Timestamp Count						
DWord	Bit	Description				
0	63:36	<p>Reserved</p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	All	Format:	MBZ
Project:	All					
Format:	MBZ					
35:0	<p>Timestamp Value</p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U36</td></tr> </table> <p>This register toggles every 80 ns. The upper 28 bits are zero.</p>	Project:	All	Format:	U36	
Project:	All					
Format:	U36					

BCS Reset Control Register

BCS_RESET_CTRL - BCS Reset Control Register				
DWord	Bit	Description		
0	31:16	<p>Mask Bits</p> <table border="1"> <tr> <td>Format:</td> <td>Mask[15:0]</td> </tr> </table> <p>Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)</p>	Format:	Mask[15:0]
Format:	Mask[15:0]			
15:2	<p>Reserved</p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ	
Format:	MBZ			
1	<p>Ready for Reset</p> <table border="1"> <tr> <td>Format:</td> <td>U1</td> </tr> </table> <p>When set indicates blitter engine is ready for reset. This bit gets cleared on engine reset or when Soft Reset In progress is cleared.</p>	Format:	U1	
Format:	U1			
0	<p>Request Reset</p> <table border="1"> <tr> <td>Format:</td> <td>U1</td> </tr> </table> <p>When set indicates SW wishes to reset the blitter engine. On seeing this bit set Command Streamer will take appropriate action and set Ready For Reset status bit. This bit gets cleared on engine reset.</p>	Format:	U1	
Format:	U1			

BCS Ring Buffer Next Context ID Register

BCS_RNCID - BCS Ring Buffer Next Context ID Register		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Source:	BlitterCS	
Default Value:	0x00000000, 0x00000000	
Access:	R/W	
Size (in bits):	64	
Address:	22198h-2219Fh	
This register contains the <i>next</i> ring context ID associated with the ring buffer.		
Programming Notes		
<p>The current context (RCCID) register can be updated indirectly from this register on a context switch event. Note that the only time a context switch can occur is when MI_ARB_CHECK enables preemption or the current context runs dry (head pointer becomes equal to tail pointer).</p>		
DWord	Bit	Description
0	63:0	Unnamed See Context Descriptor for BCS

BCS Semaphore Polling Interval on Wait

BCS_SEMA_WAIT_POLL - BCS Semaphore Polling Interval on Wait						
Register Space: MMIO: 0/2/0 Project: BDW Source: BlitterCS Default Value: 0x00000000 Access: R/W Size (in bits): 32						
Address: 2224Ch						
The SEMA_WAIT_POLL register contains Poll Interval field which specifies the minimum number of microseconds allowed for command streamer to wait before re-fetching the data from the address mentioned in the MI_SEMAPHORE_WAIT command on WAIT Mode set to POLL until the condition is satisfied while the context is not switched out. When value of 0 is written the poll interval will be equal to the memory latency of the read completion.						
DWord	Bit	Description				
0	31:21	Reserved <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	All	Format:	MBZ
Project:	All					
Format:	MBZ					
20:0	Poll Interval <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U21</td></tr> </table> Minimum number of micro-seconds allowed	Project:	All	Format:	U21	
Project:	All					
Format:	U21					

BCS SW Control

BCS_SWCTRL - BCS SW Control						
Register Space: MMIO: 0/2/0 Project: BDW Source: BlitterCS Default Value: 0x00000000 Access: r/w Size (in bits): 32 Trusted Type: 1						
DWord	Bit	Description				
0	31:16	Mask <table border="1"> <tr> <td>Access:</td> <td>WO</td> </tr> <tr> <td>Format:</td> <td>Mask</td> </tr> </table>	Access:	WO	Format:	Mask
Access:	WO					
Format:	Mask					
	15:4	Reserved <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	BDW	Format:	MBZ
Project:	BDW					
Format:	MBZ					
	3:2	Reserved <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	BDW	Format:	MBZ
Project:	BDW					
Format:	MBZ					
	1	Tile Y Destination <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Format:</td> <td>U1</td> </tr> </table> <p>Programming this bit makes the HW treat all destination surfaces as Tile Y. This bit over-rides the setting of the destination format in the packet provided to the blitter command streamer. SW is required to flush the HW before changing the polarity of this bit. This bit is part of the context save/restore.</p>	Project:	BDW	Format:	U1
Project:	BDW					
Format:	U1					
	0	Tile Y Source <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Format:</td> <td>U1</td> </tr> </table> <p>Programming this bit makes the HW treat all source surfaces as Tile Y. This bit over-rides the setting of the source format in the packet provided to the blitter command streamer. SW is required to flush the HW before changing the polarity of this bit. This bit is part of the context save/restore.</p>	Project:	BDW	Format:	U1
Project:	BDW					
Format:	U1					

BCS Watchdog Counter Threshold

BCS_CTR_THRSH - BCS Watchdog Counter Threshold						
DWord	Bit	Description				
0	31:0	<p>Counter logic Threshold</p> <table border="1"> <tr> <td>Default Value:</td> <td>00150000h</td> </tr> <tr> <td>Format:</td> <td>U32</td> </tr> </table> <p>This field specifies the threshold that the hardware checks against for the value of the blitter clock counter before generating an interrupt. The counter in hardware generates an interrupt when the threshold is reached, rolls over and starts counting again. The interrupt generated is the "Media Hang Notify" interrupt since this watchdog timer is intended primarily to remedy VLD hangs on the main pipeline.</p>	Default Value:	00150000h	Format:	U32
Default Value:	00150000h					
Format:	U32					

BITPLANE CYCLE CONTROL REGISTER

BITPLANE_CTRL - BITPLANE CYCLE CONTROL REGISTER							
Register Space:	MMIO: 0/2/0						
Default Value:	0x00000000						
Size (in bits):	32						
Bitplane Cycle Control Register							
DWord	Bit	Description					
0	30:19	Reserved <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Default Value:</td><td style="padding: 2px;">000000000000000b</td></tr> <tr> <td style="padding: 2px;">Access:</td><td style="padding: 2px;">RO</td></tr> </table>		Default Value:	000000000000000b	Access:	RO
Default Value:	000000000000000b						
Access:	RO						

Bitstream Output Bit Count for the last Syntax Element Report Register

MFC_BITSTREAM_SE_BITCOUNT_SLICE - Bitstream Output Bit Count for the last Syntax Element Report Register		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Source:	VideoCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	128D4h	
Name:	VDBOX1	
Valid Projects:	[BDW]	
Address:	1C8D4h	
Name:	VDBOX2	
Valid Projects:	[BDW:GT3]	
This register stores the count of number of bits in the bitstream for the last syntax element before padding. The bit count is before the byte-aligned alignment padding insertion, but includes the stop-one-bit. This register is part of the context save and restore.		
DWord	Bit	Description
0	31:0	MFC Bitstream Syntax Element Bit Count Total number of bits in the bitstream output before padding. This count is updated each time the internal counter is incremented.

Bitstream Output Byte Count Per Slice Report Register

MFC_BITSTREAM_BYTECOUNT_SLICE - Bitstream Output Byte Count Per Slice Report Register		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Source:	VideoCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	128D0h	
Valid Projects:	[BDW]	
Address:	1C8D0h	
Valid Projects:	[BDW:GT3]	
This register stores the count of bytes of the bitstream output. This register is part of the context save and restore.		
DWord	Bit	Description
0	31:0	MFC Bitstream Byte Count Total number of bytes in the bitstream output from the encoder. This count is updated for every time the internal bitstream counter is incremented.

Bitstream Output Minimal Size Padding Count Report Register

MFC_AVC_MINSIZE_PADDING_COUNT - Bitstream Output Minimal Size Padding Count Report Register		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Source:	VideoCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	12814h	
Name:	VDBOX1	
Valid Projects:	[BDW]	
Address:	1C814h	
Name:	VDBOX2	
Valid Projects:	[BDW:GT3]	
This register stores the count in bytes of minimal size padding insertion . It is primarily provided for statistical data gathering . This register is part of the context save and restore.		
DWord	Bit	Description
0	31:0	MFC AVC MinSize Padding Count Total number of bytes in the bitstream output contributing to minimal size padding operation. This count is updated each time when the padding count is incremented.

BLC_PWM_CTL

BLC_PWM_CTL												
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x00000000 Access: R/W Size (in bits): 32												
Address: 48250h-48253h Name: Backlight PWM Control ShortName: BLC_PWM_CTL Valid Projects: BDW Power: Always on Reset: soft												
This register controls the backlight PWM logic going to the display utility pin on the CPU.												
DWord	Bit	Description										
0	31	<p>PWM Enable This bit enables the PWM logic.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Disable</td><td>PWM disabled</td></tr> <tr> <td>1b</td><td>Enable</td><td>PWM enabled</td></tr> </tbody> </table> <p>Restriction The display utility pin must be configured correctly to output the PWM. Program the frequency and duty cycle before enabling PWM.</p>	Value	Name	Description	0b	Disable	PWM disabled	1b	Enable	PWM enabled	
Value	Name	Description										
0b	Disable	PWM disabled										
1b	Enable	PWM enabled										
<p>Pipe Select This field selects which vertical blank will be used for backlight blinking.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>00b</td><td>Pipe A</td><td>Use Pipe A</td></tr> <tr> <td>01b</td><td>Pipe B</td><td>Use Pipe B</td></tr> <tr> <td>10b</td><td>Pipe C</td><td>Use Pipe C</td></tr> </tbody> </table>	Value	Name	Description	00b	Pipe A	Use Pipe A	01b	Pipe B	Use Pipe B	10b	Pipe C	Use Pipe C
Value	Name	Description										
00b	Pipe A	Use Pipe A										
01b	Pipe B	Use Pipe B										
10b	Pipe C	Use Pipe C										
<p>Blinking Enable This bit enables backlight blinking. When enabled, the backlight will be driven on at the programmed brightness during vertical blank and driven off during vertical active.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Disable</td></tr> <tr> <td>1b</td><td>Enable</td></tr> </tbody> </table>	Value	Name	0b	Disable	1b	Enable						
Value	Name											
0b	Disable											
1b	Enable											

BLC_PWM_CTL												
	27	PWM Granularity This field controls the granularity (minimum increment) of the PWM backlight control counter.										
		<table border="1"><thead><tr><th>Value</th><th>Name</th><th>Description</th></tr></thead><tbody><tr><td>0b</td><td>128</td><td>PWM frequency adjustment on 128 clock increments</td></tr><tr><td>1b</td><td>8</td><td>PWM frequency adjustment on 8 clock increments</td></tr></tbody></table>	Value	Name	Description	0b	128	PWM frequency adjustment on 128 clock increments	1b	8	PWM frequency adjustment on 8 clock increments	
Value	Name	Description										
0b	128	PWM frequency adjustment on 128 clock increments										
1b	8	PWM frequency adjustment on 8 clock increments										
	26:0	Reserved										

BLC_PWM_DATA

BLC_PWM_DATA		
DWord	Bit	Description
0	31:16	<p>Backlight Frequency</p> <p>This field determines the number of time base events in total for a complete cycle of modulated backlight control. This field is programmed based on the frequency of the clock that is being used and the desired PWM frequency. This value represents the period of the PWM stream in CD clocks multiplied by 128 (default increment) or 8 (alternate increment selected by BLC_PWM_CTL PWM_Granularity).</p>
	15:0	<p>Backlight Duty Cycle</p> <p>This field determines the number of time base events for the active portion of the PWM backlight control. A value of zero will turn the backlight off. A value equal to the backlight modulation frequency field will be full on. Updates will take affect at the end of the current PWM cycle. This value represents the active time of the PWM stream in CD clock periods multiplied by 128 (default increment) or 8 (alternate increment selected by BLC_PWM_CTL PWM_Granularity).</p>
Restriction		
This should never be larger than the frequency field.		

Blitter Mode Register

BLT_MODE - Blitter Mode Register								
Register Space: MMIO: 0/2/0 Project: BDW Source: BlitterCS Default Value: 0x00000000 Access: R/W Size (in bits): 32 Trusted Type: 1								
Address: 2229Ch								
DWord	Bit	Description						
0	31:16	Mask Bits <table border="1"> <tr> <td>Format:</td><td>Mask[15:0]</td></tr> </table> <p>Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)</p>	Format:	Mask[15:0]				
Format:	Mask[15:0]							
	15	Exelist Enable <table border="1"> <tr> <td>Default Value:</td><td>0h</td></tr> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Mask:</td><td>MMIO#31</td></tr> </table> <p>When set, software can utilize the exelist registers to load a context into hardware. When this bit is clear the Exelist mechanism cannot be used. The ring must be loaded via MMIO access.</p>	Default Value:	0h	Project:	BDW	Mask:	MMIO#31
Default Value:	0h							
Project:	BDW							
Mask:	MMIO#31							
		Programming Notes <p>This bit is not intended to be changed dynamically. Changing the value of this bit while rendering is in progress will have UNDEFINED results. This bit should be changed only after a full reset and before submitting any commands to the device</p>						
	14	Interrupt Steering Bit <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>U1</td></tr> </table> <p>When set, Command Streamer sends interrupt messages to the SHIM of the ON CHIP Micro Controller through message channel. When reset, Command Streamer sends the interrupt messages to Display Engine as config writes on GAM interface.</p>	Project:	BDW	Format:	U1		
Project:	BDW							
Format:	U1							
	13:10	Reserved <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	All	Format:	MBZ		
Project:	All							
Format:	MBZ							

BLT_MODE - Blitter Mode Register

	9	Per-Process GTT Enable		
		Project:	All	
		Format:	Enable Per-Process GTT BS Mode Enable	
		Value	Name	Description
		0h	PPGTT Disable [Default]	When clear, the Global GTT will be used to translate memory access from designated commands and for commands that select the PPGTT as their translation space.
		1h	PPGTT Enable	When set, the PPGTT will be used to translate memory access from designated commands and for commands that select the PPGTT as their translation space.
		Programming Notes		
		This bit is used for enabling PPGTT access in Ring Buffer mode of scheduling. Privilege field in context descriptor states the same in Execlist Mode of scheduling. This field should be set before programming PDP0/1/2/3 registers in order to set the PPGTT translation of memory access.		
	8	Reserved		
		Project:	All	
	7	64Bit Virtual Addressing Enable		
		Project:	BDW	
		Format:	Enable	
		Per-Process GTT Enable		
		Value	Name	Description
		0h	64Bit Virtual Addressing Disable [Default]	When clear indicates GFX operating in 32bit Virtual Addressing for PPGTT based memory access.
		1h	64Bit Virtual Addressing Enable	When Set indicates GFX operating in 64bit (48bit Canonical) Virtual Addressing for PPGTT based memory access.
		Programming Notes		
		This bit is only valid when PPGTT is enabled in ring buffer mode of scheduling. Context Descriptor has a similar bit to control 64bit virtual addressing in execlist mode of scheduling. Irrespective of this field set or clear virtual addresses translated through GTT are always 32Bit. This field should be programmed before enabling PPGTT access. When this field is not set or for GTT virtual addresses, Graphics Address [47:32] field of any commands or register exercised by SW should be programmed to 0x0.		
	6:5	Reserved		
		Project:	BDW	
	4	Reserved		
		Project:	BDW	

BLT_MODE - Blitter Mode Register			
	3:1	Reserved	
		Project:	All
	0	Privilege Check Disable	
		Project:	BDW
		Format:	Enable
This field when set, disables Privilege Violation checks on non-privileged batch buffers. When set Privileged commands are allowed to be executed from non-privileged batch buffers.			

Blitter TLB Control Register

BTCR - Blitter TLB Control Register						
DWord	Bit	Description				
0	31:1	<p>Reserved</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000000000000000000000000000b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Default Value:	00000000000000000000000000000000b	Access:	RO
Default Value:	00000000000000000000000000000000b					
Access:	RO					
	0	<p>Invalidate TLBs on the corresponding Engine</p> <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>SW writes 1 to invalidate the TLBs for the associated engine and HW clears the bit when invalidation is complete. To ensure proper invalidation of the TLBs, SW has to ensure the corresponding engine's HW pipeline is flushed and cleared from all its memory accesses. Otherwise HW cannot guarantee the proper invalidation for TLBs.</p> <p>This bit is self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					

BLT Context Element Descriptor (High Part)

BLT_CTX_EDR_H - BLT Context Element Descriptor (High Part)		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04504h	
DWord	Bit	Description
0	31:0	BLT Context Element Descriptor (High Part)
		Default Value: 00000000h
		Access: R/W

BLT Context Element Descriptor (Low Part)

BLT_CTX_EDR_L - BLT Context Element Descriptor (Low Part)		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000009	
Size (in bits):	32	
Address:	04500h	
DWord	Bit	Description
0	31:0	BLT Context Element Descriptor (Low Part)
		Default Value: 00000009h
		Access: R/W

BLT Context Element Descriptor (Low Part)

BLT_CTX_EDR_L - BLT Context Element Descriptor (Low Part)		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000009	
Size (in bits):	32	
Address:	04500h	
DWord	Bit	Description
0	31:0	BLT Context Element Descriptor
		Default Value: 00000009h
		Access: R/W

BLT Fault Counter

BLT_FAULT_CNTR - BLT Fault Counter		
DWord	Bit	Description
0	31:0	BLT Fault Counter
		Default Value: 00000000h
		Access: RO

BLT Fixed Counter

BLT_FIXED_CNTR - BLT Fixed Counter		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	045BCh	
DWord	Bit	Description
0	31:0	BLT Fixed Counter Default Value: 0000000h Access: RO

BLT PDP0/PML4/PASID Descriptor (High Part)

BLT_CTX_PDP0_H - BLT PDP0/PML4/PASID Descriptor (High Part)						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	0450Ch					
DWord	Bit	Description				
0	31:0	BLT PDP0/PML4/PASID Descriptor (High Part)				
		<table border="1"><tr><td>Default Value:</td><td>00000000h</td></tr><tr><td>Access:</td><td>R/W</td></tr></table>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

BLT PDP0/PML4/PASID Descriptor (Low Part)

BLT_CTX_PDP0_L - BLT PDP0/PML4/PASID Descriptor (Low Part)		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04508h	
DWord	Bit	Description
0	31:0	BLT PDP0/PML4/PASID Descriptor (Low Part)
		Default Value: 00000000h
		Access: R/W

BLT PDP1 Descriptor Register (High Part)

BLT_CTX_PDP1_H - BLT PDP1 Descriptor Register (High Part)		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04514h	
DWord	Bit	Description
0	31:0	BLT PDP1 Descriptor Register (High Part)
		Default Value: 00000000h
		Access: R/W

BLT PDP1 Descriptor Register (Low Part)

BLT_CTX_PDP1_L - BLT PDP1 Descriptor Register (Low Part)		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04510h	
DWord	Bit	Description
0	31:0	BLT PDP1 Descriptor Register (Low Part)
		Default Value: 00000000h
		Access: R/W

BLT PDP2 Descriptor Register (High Part)

BLT_CTX_PDP2_H - BLT PDP2 Descriptor Register (High Part)		
DWord	Bit	Description
0	31:0	BLT PDP2 Descriptor Register (High Part)
		Default Value: 00000000h
		Access: R/W

BLT PDP2 Descriptor Register (Low Part)

BLT_CTX_PDP2_L - BLT PDP2 Descriptor Register (Low Part)		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04518h	
DWord	Bit	Description
0	31:0	BLT PDP2 Descriptor Register (Low Part)
		Default Value: 00000000h
		Access: R/W

BLT PDP3 Descriptor Register (High Part)

BLT_CTX_PDP3_H - BLT PDP3 Descriptor Register (High Part)		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04524h	
DWord	Bit	Description
0	31:0	BLT PDP3 Descriptor Register (High Part)
		Default Value: 00000000h
		Access: R/W

BLT PDP3 Descriptor Register (Low Part)

BLT_CTX_PDP3_L - BLT PDP3 Descriptor Register (Low Part)		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04520h	
DWord	Bit	Description
0	31:0	BLT PDP3 Descriptor Register (Low Part)
		Default Value: 00000000h
		Access: R/W

Boolean_Counter_B0

OAPERF_B0 - Boolean_Counter_B0						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Access:	R/W					
Size (in bits):	32					
Address:	02920h					
Valid Projects:	[BDW]					
<p>This register enables the current live value of performance counter B0 to be read. Since what conditions cause B0 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.</p>						
DWord	Bit	Description				
0	31:0	<p>Considerations</p> <table border="1"> <tr> <td>Format:</td><td>U32</td></tr> <tr> <td colspan="2">This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</td></tr> </table>	Format:	U32	This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.	
Format:	U32					
This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.						

Boolean_Counter_B1

OAPERF_B1 - Boolean_Counter_B1						
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x00000000 Access: R/W Size (in bits): 32						
Address: 02924h Valid Projects: [BDW]						
This register enables the current live value of performance counter B1 to be read. Since what conditions cause B1 to increment are defined by the programming of CEC1-0/CEC1-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.						
DWord	Bit	Description				
0	31:0	Considerations <table border="1"> <tr> <td>Format:</td><td>U32</td></tr> <tr> <td colspan="2">This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</td></tr> </table>	Format:	U32	This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.	
Format:	U32					
This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.						

Boolean_Counter_B2

OAPERF_B2 - Boolean_Counter_B2						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Access:	R/W					
Size (in bits):	32					
Address:	02928h					
Valid Projects:	[BDW]					
<p>This register enables the current live value of performance counter B2 to be read. Since what conditions cause B2 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.</p>						
DWord	Bit	Description				
0	31:0	<p>Considerations</p> <table border="1"> <tr> <td>Format:</td><td>U32</td></tr> <tr> <td colspan="2">This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</td></tr> </table>	Format:	U32	This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.	
Format:	U32					
This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.						

Boolean_Counter_B3

OAPERF_B3 - Boolean_Counter_B3						
DWord	Bit	Description				
0	31:0	<p>Considerations</p> <table border="1"> <tr> <td>Format:</td> <td>U32</td> </tr> <tr> <td colspan="2">This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</td></tr> </table>	Format:	U32	This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.	
Format:	U32					
This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.						

Boolean_Counter_B4

OAPERF_B4 - Boolean_Counter_B4						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Access:	R/W					
Size (in bits):	32					
Address:	02930h					
Valid Projects:	[BDW]					
<p>This register enables the current live value of performance counter B4 to be read. Since what conditions cause B4 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.</p>						
DWord	Bit	Description				
0	31:0	<p>Considerations</p> <table border="1"> <tr> <td>Format:</td><td>U32</td></tr> <tr> <td colspan="2">This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</td></tr> </table>	Format:	U32	This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.	
Format:	U32					
This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.						

Boolean_Counter_B5

OAPERF_B5 - Boolean_Counter_B5						
DWord	Bit	Description				
0	31:0	<p>Considerations</p> <table border="1"> <tr> <td>Format:</td> <td>U32</td> </tr> <tr> <td colspan="2">This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</td></tr> </table>	Format:	U32	This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.	
Format:	U32					
This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.						

Boolean_Counter_B6

OAPERF_B6 - Boolean_Counter_B6						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Access:	R/W					
Size (in bits):	32					
Address:	02938h					
Valid Projects:	[BDW]					
<p>This register enables the current live value of performance counter B6 to be read. Since what conditions cause B6 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.</p>						
DWord	Bit	Description				
0	31:0	<p>Considerations</p> <table border="1"> <tr> <td>Format:</td><td>U32</td></tr> <tr> <td colspan="2">This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</td></tr> </table>	Format:	U32	This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.	
Format:	U32					
This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.						

Boolean_Counter_B7

OAPERF_B7 - Boolean_Counter_B7						
DWord	Bit	Description				
0	31:0	<p>Considerations</p> <table border="1"> <tr> <td>Format:</td> <td>U32</td> </tr> <tr> <td colspan="2">This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</td></tr> </table>	Format:	U32	This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.	
Format:	U32					
This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.						
This register enables the current live value of performance counter B7 to be read. Since what conditions cause B7 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.						

BOOT VECTOR

BOOTMSG - BOOT VECTOR				
DWord	Bit	Description		
0	31:0	<p>Boot Vector Message</p> <table border="1"> <tr> <td>Access:</td> <td>R/W Lock</td> </tr> </table> <p>Boot vector is pass through. MBC gets the boot message from GPMunit and forwards it to MSQC. Breakdown of message is done in MSQC. Details: if b[26] = 1 C6SliceA = b[20:17]; C6SliceB= d[13:10] C6Way = 0 C6Area = 0 if b[26] = 0 C6Way = b[25:21], C6Slice = d[20:17]; C6Area = d[17:10] Context Restore = b[6] Reset Type = b[6:5] Ring Stop ID = b[4:0]</p>	Access:	R/W Lock
Access:	R/W Lock			
This register gets locked by the Hardware once written and is cleared only during the reset. This is extra protection given against Illegal Programming.				

BTB Not Consumed By RCS

BTP_PRODUCE_COUNT - BTB Not Consumed By RCS		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	02480h	
This register keeps track of the outstanding BTP produced by RS which are not yet consumed by Render Command Streamer. This register is part of the render context save and restore.		
Programming Notes		
This register should not be programmed by SW.		
DWord	Bit	Description
0	31:0	BTP Produce Count This register keeps track of the outstanding BTP produced by RS which are not yet consumed by Render Command Streamer. This register is part of the render context save and restore.

BTP Commands Parsed By RCS

BTP_PARSE_COUNT - BTP Commands Parsed By RCS		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	02490h	
This register keeps track of the BTP commands parsed by RCS prior to encountering the Draw Call in an RS enabled Batch Buffer which has BTP Pool Alloc Valid. BTP parse count should be less than equal to the BTP produce count for Command Streamer to make progress on a 3D_PRIMITIVE command. BTP Parse count is subtracted from the BTP Produce Count upon parsing 3D_PRIMITIVE command. This register is part of the render context save and restore. This register should not be programmed by SW.		
DWord	Bit	Description
0	31:0	<p>BTP Parse Count</p> <p>This register keeps track of the BTP commands parsed by RCS prior to encountering the Draw Call in an RS enabled Batch Buffer which has BTP Pool Alloc Valid. BTP parse count should be less than equal to the BTP produce count for Command Streamer to make progress on a 3D_PRIMITIVE command. BTP Parse count is subtracted from the BTP Produce Count upon parsing 3D_PRIMITIVE command.</p>

Cache Line Size

CLS_0_2_0_PCI - Cache LineSize						
DWord	Bit	Description				
0	7:0	Cache Line Size <table border="1"> <tr> <td>Default Value:</td><td>00000000b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>This field is hardwired to 0s. The IGD as a PCI compliant master does not use the Memory Write and Invalidate command and, in general, does not perform operations based on cache line size.</p>	Default Value:	00000000b	Access:	RO
Default Value:	00000000b					
Access:	RO					

Cache Mode Register 0

CACHE_MODE_0 - Cache Mode Register 0						
Register Space: MMIO: 0/2/0 Project: BDW Source: RenderCS 0x00000004 [BDW:GT2:G1, BDW:GT2:H, BDW:GT3:H, BDW:GT3E:J] Access: R/W Size (in bits): 32						
Address: 07000h Valid Projects: [BDW]						
Description						
<p>This register is used to control the operation of the Render and Sampler L2 Caches. All reserved bits are implemented as read/write.</p> <p>Before changing the value of this register, GFX pipeline must be idle i.e. full flush is required.</p> <p>This Register is saved and restored as part of Context.</p>						
RegisterType = MMIO_SVL						
DWord	Bit	Description				
0	31:16	Mask				
		<table border="1"> <tr> <td>Access:</td><td>WO</td></tr> <tr> <td>Format:</td><td>Mask[15:0]</td></tr> </table> <p>A 1 in a bit in this field allows the modification of the corresponding bit in Bits 15:0.</p>	Access:	WO	Format:	Mask[15:0]
Access:	WO					
Format:	Mask[15:0]					
	15	Sampler L2 Disable				
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>r/w</td></tr> <tr> <td>Format:</td><td>Disable</td></tr> </table>	Project:	BDW	Access:	r/w
Project:	BDW					
Access:	r/w					
Format:	Disable					
Value	Name	Description				
0h	[Default]	Sampler L2 Cache Enabled.				
1h		Sampler L2 Cache Disabled. All accesses are treated as misses.				

CACHE_MODE_0 - Cache Mode Register 0

	14:12	MSAA Compression Plane Number Threshold for eLLC																											
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>r/w</td></tr> </table>	Project:	BDW	Access:	r/w																							
Project:	BDW																												
Access:	r/w																												
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0h</td><td>threshold0 [Default]</td><td>Cache only planeID = 0 in eLLC.</td></tr> <tr> <td>1h</td><td>threshold1</td><td>Cache only planeID = 0, 1 in eLLC.</td></tr> <tr> <td>2h</td><td>threshold2</td><td>Cache only planeID = 0..2 in eLLC.</td></tr> <tr> <td>3h</td><td>threshold3</td><td>Cache only planeID = 0..3 in eLLC.</td></tr> <tr> <td>4h</td><td>threshold4</td><td>Cache only planeID = 0..4 in eLLC.</td></tr> <tr> <td>5h</td><td>threshold5</td><td>Cache only planeID = 0..5 in eLLC.</td></tr> <tr> <td>6h</td><td>threshold6</td><td>Cache only planeID = 0..6 in eLLC.</td></tr> <tr> <td>7h</td><td>threshold7</td><td>Cache only planeID = 0..7 in eLLC.</td></tr> </tbody> </table>	Value	Name	Description	0h	threshold0 [Default]	Cache only planeID = 0 in eLLC.	1h	threshold1	Cache only planeID = 0, 1 in eLLC.	2h	threshold2	Cache only planeID = 0..2 in eLLC.	3h	threshold3	Cache only planeID = 0..3 in eLLC.	4h	threshold4	Cache only planeID = 0..4 in eLLC.	5h	threshold5	Cache only planeID = 0..5 in eLLC.	6h	threshold6	Cache only planeID = 0..6 in eLLC.	7h	threshold7	Cache only planeID = 0..7 in eLLC.
Value	Name	Description																											
0h	threshold0 [Default]	Cache only planeID = 0 in eLLC.																											
1h	threshold1	Cache only planeID = 0, 1 in eLLC.																											
2h	threshold2	Cache only planeID = 0..2 in eLLC.																											
3h	threshold3	Cache only planeID = 0..3 in eLLC.																											
4h	threshold4	Cache only planeID = 0..4 in eLLC.																											
5h	threshold5	Cache only planeID = 0..5 in eLLC.																											
6h	threshold6	Cache only planeID = 0..6 in eLLC.																											
7h	threshold7	Cache only planeID = 0..7 in eLLC.																											
		<p style="text-align: center;">Programming Notes</p> <p>This bit-field is programmed based on MSAA. When MSAA compression is enabled, these settings affect HW, else it is ignored. For 16X MSAA only lower 8 planes can be cached in eLLC.</p>																											
	11	Sampler Set Remapping for 3D Disable																											
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>r/w</td></tr> </table>	Project:	BDW	Access:	r/w																							
Project:	BDW																												
Access:	r/w																												
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0h</td><td>Enable Set Remap [Default]</td><td>Set remapping for 3d enabled</td></tr> <tr> <td>1h</td><td>Disable Set Remap</td><td>Set remapping for 3d disabled</td></tr> </tbody> </table>	Value	Name	Description	0h	Enable Set Remap [Default]	Set remapping for 3d enabled	1h	Disable Set Remap	Set remapping for 3d disabled																		
Value	Name	Description																											
0h	Enable Set Remap [Default]	Set remapping for 3d enabled																											
1h	Disable Set Remap	Set remapping for 3d disabled																											
	10	Reserved																											
		<table border="1"> <tr> <td>Access:</td><td>r/w</td></tr> <tr> <td>Format:</td><td>PBC</td></tr> </table>	Access:	r/w	Format:	PBC																							
Access:	r/w																												
Format:	PBC																												
	9	Sampler L2 TLB Prefetch Enable																											
		<table border="1"> <tr> <td>Access:</td><td>r/w</td></tr> </table>	Access:	r/w																									
Access:	r/w																												
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0h</td><td>[Default]</td><td>TLB Prefetch Disabled</td></tr> <tr> <td>1h</td><td></td><td>TLB Prefetch Enabled</td></tr> </tbody> </table>	Value	Name	Description	0h	[Default]	TLB Prefetch Disabled	1h		TLB Prefetch Enabled																		
Value	Name	Description																											
0h	[Default]	TLB Prefetch Disabled																											
1h		TLB Prefetch Enabled																											
	8	Reserved																											

CACHE_MODE_0 - Cache Mode Register 0

	7:6	Sampler L2 Request Arbitration																	
		Project:	BDW																
		Access:	r/w																
		Format:	U2																
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td></td> <td>Round Robin</td> </tr> <tr> <td>01b</td> <td></td> <td>Fetch are Highest Priority</td> </tr> <tr> <td>10b</td> <td></td> <td>Constants are Highest Priority</td> </tr> <tr> <td>11b</td> <td></td> <td>Reserved</td> </tr> </tbody> </table>			Value	Name	Description	00b		Round Robin	01b		Fetch are Highest Priority	10b		Constants are Highest Priority	11b		Reserved
Value	Name	Description																	
00b		Round Robin																	
01b		Fetch are Highest Priority																	
10b		Constants are Highest Priority																	
11b		Reserved																	
	5	STC Eviction Policy																	
		Project:	BDW																
		Access:	r/w																
		Format:	Disable																
		<p>If this bit is set, STCunit will have LRA as replacement policy. The default value i.e. (when this bit is reset) indicates that non-LRA eviction policy. This bit must be reset. LRA replacement policy is not supported.</p> <table border="1"> <thead> <tr> <th>Programming Notes</th> </tr> </thead> <tbody> <tr> <td>If this bit is set to "1", bit 4 of 0x7010h must also be set to "1".</td> </tr> </tbody> </table>			Programming Notes	If this bit is set to "1", bit 4 of 0x7010h must also be set to "1".													
Programming Notes																			
If this bit is set to "1", bit 4 of 0x7010h must also be set to "1".																			
	4	RCC Eviction Policy																	
		Project:	BDW																
		Access:	r/w																
		Format:	Disable																
		<p>If this bit is set, RCCunit will have LRA as replacement policy. The default value i.e. (when this bit is reset) indicates that non-LRA eviction policy. This bit must be reset. LRA replacement policy is not supported.</p> <table border="1"> <thead> <tr> <th>Programming Notes</th> </tr> </thead> <tbody> <tr> <td>If this bit is set to "1", bit 7 of 0x7010h must also be set to "1".</td> </tr> </tbody> </table>			Programming Notes	If this bit is set to "1", bit 7 of 0x7010h must also be set to "1".													
Programming Notes																			
If this bit is set to "1", bit 7 of 0x7010h must also be set to "1".																			
	3	Reserved																	

CACHE_MODE_0 - Cache Mode Register 0

	2	Hierarchical Z RAW Stall Optimization Disable									
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>r/w</td></tr> <tr> <td>Format:</td><td>U1</td></tr> </table> <p>The Hierarchical Z RAW Stall Optimization allows non-overlapping polygons in the same 8x4 pixel/sample area to be processed without stalling waiting for the earlier ones to write to Hierarchical Z buffer.</p>	Project:	BDW	Access:	r/w	Format:	U1			
Project:	BDW										
Access:	r/w										
Format:	U1										
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0h</td><td>Enable</td><td>Enables the hierarchical Z RAW Stall Optimization.</td></tr> <tr> <td>1h</td><td>Disable [Default]</td><td>Disables the hierarchical Z RAW Stall Optimization.</td></tr> </tbody> </table>	Value	Name	Description	0h	Enable	Enables the hierarchical Z RAW Stall Optimization.	1h	Disable [Default]	Disables the hierarchical Z RAW Stall Optimization.
Value	Name	Description									
0h	Enable	Enables the hierarchical Z RAW Stall Optimization.									
1h	Disable [Default]	Disables the hierarchical Z RAW Stall Optimization.									
		Programming Notes									
		This bit must be set to 0 to enable the Hierarchical Z RAW stall optimization.									
	1	Disable clock gating in the pixel backend									
		<table border="1"> <tr> <td>Access:</td><td>r/w</td></tr> <tr> <td>Format:</td><td>Disable</td></tr> </table> <p>MCL related clock gating is disabled in the pixel backend. Before setting this bit to 1, the instruction/state caches must be invalidated. [DevGT:{WKA}]</p>	Access:	r/w	Format:	Disable					
Access:	r/w										
Format:	Disable										
	0	Render Cache Operational Flush Enable									
		<table border="1"> <tr> <td>Project:</td><td>>BDW*:G0, BDW:GT2:G1</td></tr> <tr> <td>Access:</td><td>r/w</td></tr> <tr> <td>Format:</td><td>Enable</td></tr> </table>	Project:	>BDW*:G0, BDW:GT2:G1	Access:	r/w	Format:	Enable			
Project:	>BDW*:G0, BDW:GT2:G1										
Access:	r/w										
Format:	Enable										
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0h</td><td>Disable [Default]</td><td>Operational Flush Disabled (recommended for performance when not rendering to the front buffer)</td></tr> <tr> <td>1h</td><td>Enable</td><td>Operational Flush Enabled (required when rendering to the front buffer)</td></tr> </tbody> </table>	Value	Name	Description	0h	Disable [Default]	Operational Flush Disabled (recommended for performance when not rendering to the front buffer)	1h	Enable	Operational Flush Enabled (required when rendering to the front buffer)
Value	Name	Description									
0h	Disable [Default]	Operational Flush Disabled (recommended for performance when not rendering to the front buffer)									
1h	Enable	Operational Flush Enabled (required when rendering to the front buffer)									
	0	BDW Slice shutdown fix disable									
		<table border="1"> <tr> <td>Project:</td><td>BDW, EXCLUDE(BDW:GT2:G1)</td></tr> <tr> <td>Access:</td><td>r/w</td></tr> </table>	Project:	BDW, EXCLUDE(BDW:GT2:G1)	Access:	r/w					
Project:	BDW, EXCLUDE(BDW:GT2:G1)										
Access:	r/w										
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>1</td><td>Disable</td><td>Disables Slice Shutdown fix.</td></tr> <tr> <td>0</td><td>Enable [Default]</td><td>Enables Slice Shutdown fix.</td></tr> </tbody> </table>	Value	Name	Description	1	Disable	Disables Slice Shutdown fix.	0	Enable [Default]	Enables Slice Shutdown fix.
Value	Name	Description									
1	Disable	Disables Slice Shutdown fix.									
0	Enable [Default]	Enables Slice Shutdown fix.									

Cache Mode Register 1

CACHE_MODE_1 - Cache Mode Register 1

Register Space:	MMIO: 0/2/0
Project:	BDW
Source:	RenderCS 0x00000180 [BDW]
Access:	R/W
Size (in bits):	32
Address:	07004h
Valid Projects:	[BDW]

Description

RegisterType: MMIO_SVL

Before changing the value of this register, GFX pipeline must be idle; i.e., full flush is required. This Register is saved and restored as part of Context.

DWord	Bit	Description												
0	31:16	<p>Mask</p> <table border="1"> <tr> <td>Access:</td> <td>WO</td> </tr> <tr> <td>Mask:</td> <td>MASK</td> </tr> <tr> <td>Format:</td> <td>Mask[15:0]</td> </tr> </table> <p>Must be set to modify corresponding data bit. Reads to this field returns zero.</p>	Access:	WO	Mask:	MASK	Format:	Mask[15:0]						
Access:	WO													
Mask:	MASK													
Format:	Mask[15:0]													
	15	<p>Reserved</p> <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	BDW	Format:	MBZ								
Project:	BDW													
Format:	MBZ													
	14	<p>MSC Resolve Optimization Disable</p> <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Access:</td> <td>r/w</td> </tr> <tr> <td>Format:</td> <td>U1</td> </tr> </table> <p>Setting this bit causes MSC to mark cachelines dirty and appropriately update MSC during the classic clear resolve pass. Default value, i.e. resetting this bit, suppresses MSC buffer modification during the classic clear resolve pass.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>1h</td> <td>Disable</td> </tr> <tr> <td>0h</td> <td>Enable [Default]</td> </tr> </tbody> </table>	Project:	BDW	Access:	r/w	Format:	U1	Value	Name	1h	Disable	0h	Enable [Default]
Project:	BDW													
Access:	r/w													
Format:	U1													
Value	Name													
1h	Disable													
0h	Enable [Default]													

CACHE_MODE_1 - Cache Mode Register 1

	13	NP EARLY Z FAILS DISABLE									
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>r/w</td></tr> </table>	Project:	BDW	Access:	r/w					
Project:	BDW										
Access:	r/w										
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0h</td><td>Disable [Default]</td><td>When NP PMA FIX ENABLE = 1, clearing this bit disables IZ to conservatively fail pixels.</td></tr> <tr> <td>1h</td><td>Enable</td><td>When NP PMA FIX ENABLE = 1, IZ does conservatively fail any NP pixels.</td></tr> </tbody> </table>	Value	Name	Description	0h	Disable [Default]	When NP PMA FIX ENABLE = 1, clearing this bit disables IZ to conservatively fail pixels.	1h	Enable	When NP PMA FIX ENABLE = 1, IZ does conservatively fail any NP pixels.
Value	Name	Description									
0h	Disable [Default]	When NP PMA FIX ENABLE = 1, clearing this bit disables IZ to conservatively fail pixels.									
1h	Enable	When NP PMA FIX ENABLE = 1, IZ does conservatively fail any NP pixels.									
Programming Notes											
This bit must be set when NP PMA FIX ENABLE = 1											
This bit must not be set when NP PMA FIX ENABLE = 0											
	12	HIZ Eviction Policy									
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>r/w</td></tr> <tr> <td>Format:</td><td>U1</td></tr> </table>	Project:	BDW	Access:	r/w	Format:	U1			
Project:	BDW										
Access:	r/w										
Format:	U1										
		If this bit is set, Hizunit will have LRA as replacement policy. The default value i.e. (when this bit is reset) indicates the non-LRA eviction policy. For performance reasons, this bit must be reset.									
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0h</td><td>[Default]</td><td>Non-LRA eviction Policy</td></tr> <tr> <td>1h</td><td></td><td>LRA eviction Policy</td></tr> </tbody> </table>	Value	Name	Description	0h	[Default]	Non-LRA eviction Policy	1h		LRA eviction Policy
Value	Name	Description									
0h	[Default]	Non-LRA eviction Policy									
1h		LRA eviction Policy									
Programming Notes											
If this bit is set to "1", bit 3 of 0x7010h must also be set to "1"											

CACHE_MODE_1 - Cache Mode Register 1

	11	NP PMA FIX ENABLE									
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>r/w</td></tr> </table>	Project:	BDW	Access:	r/w					
Project:	BDW										
Access:	r/w										
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0h</td><td>Disable [Default]</td><td>Enables stalling PMA behavior for NP depth pixels in the early depth pipeline. (Legacy behavior)</td></tr> <tr> <td>1h</td><td>Enable</td><td>Enables non-stalling PMA behavior for NP depth pixels in the early depth pipeline.</td></tr> </tbody> </table>	Value	Name	Description	0h	Disable [Default]	Enables stalling PMA behavior for NP depth pixels in the early depth pipeline. (Legacy behavior)	1h	Enable	Enables non-stalling PMA behavior for NP depth pixels in the early depth pipeline.
Value	Name	Description									
0h	Disable [Default]	Enables stalling PMA behavior for NP depth pixels in the early depth pipeline. (Legacy behavior)									
1h	Enable	Enables non-stalling PMA behavior for NP depth pixels in the early depth pipeline.									
		<p style="text-align: center;">Programming Notes</p> <p>SW must set this bit in order to enable this fix when following expression is TRUE.</p> <pre>3DSTATE_WM::ForceThreadDispatch != 1 && ! (3DSTATE_RASTER::ForceSampleCount != NUMRASTERSAMPLES_0) && (3DSTATE_DEPTH_BUFFER::SURFACE_TYPE != NULL) && (3DSTATE_DEPTH_BUFFER:: HIZ Enable) && !(3DSTATE_WM::EDSC_Mode == 2) && (3DSTATE_PS_EXTRA::PixelShaderValid) && !(3DSTATE_WM_HZ_OP::DepthBufferClear 3DSTATE_WM_HZ_OP::DepthBufferResolve 3DSTATE_WM_HZ_OP::Hierarchical Depth Buffer Resolve Enable 3DSTATE_WM_HZ_OP::StencilBufferClear) && (3DSTATE_WM_DEPTH_STENCIL::DepthTestEnable) && ((3DSTATE_PS_EXTRA::PixelShaderKillsPixels 3DSTATE_PS_EXTRA:: oMask Present to RenderTarget 3DSTATE_PS_BLEND::AlphaToCoverageEnable 3DSTATE_PS_BLEND::AlphaTestEnable 3DSTATE_WM_CHROMAKEY::ChromaKeyKillEnable) && (3DSTATE_WM::ForceKillPix != ForceOff && (3DSTATE_WM_DEPTH_STENCIL::DepthWriteEnable && 3DSTATE_DEPTH_BUFFER::DEPTH_WRITE_ENABLE) (3DSTATE_WM_DEPTH_STENCIL::Stencil Buffer Write Enable && 3DSTATE_DEPTH_BUFFER::STENCIL_WRITE_ENABLE && 3DSTATE_STENCIL_BUFFER::STENCIL_BUFFER_ENABLE)))) (3DSTATE_PS_EXTRA:: Pixel Shader Computed Depth mode != PSCDEPTH_OFF))</pre>									
	10	Reserved									
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> </table>	Project:	BDW							
Project:	BDW										
	9	Reserved									
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>r/w</td></tr> </table>	Project:	BDW	Access:	r/w					
Project:	BDW										
Access:	r/w										

CACHE_MODE_1 - Cache Mode Register 1

8:7	Sampler Cache Set XOR selection															
	Project:	BDW														
	Access:	r/w														
	Format:	U2														
	These bits have an impact only when the Sampler cache is configured in 16 way set associative mode. If the cache is being used for immediate data or for blitter data these bits have no effect.															
	<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>00b</td><td>None</td><td>No XOR.</td></tr> <tr> <td>01b</td><td>Scheme 1</td><td> <p>New_set_mask[3:0] = Tiled_address[16:13]. New_set[3:0] less than or = New_set_mask[3:0] ^ Old_set[3:0].</p> <p>Rationale: These bits can distinguish among 16 different equivalent classes of virtual pages. These bits also represent the lsb for tile rows ranging from a pitch of 1 tile to 16 tiles.</p> </td></tr> <tr> <td>10b</td><td>Scheme 2</td><td> <p>New_set_mask[3] = Tiled_address[17] ^ Tiled_address[16]. New_set_mask[2] = Tiled_address[16] ^ Tiled_address[15]. New_set_mask[1] = Tiled_address[15] ^ Tiled_address[14]. New_set_mask[0] = Tiled_address[14] ^ Tiled_address[13]. New_set[3:0] less than or = New_set_mask[3:0] ^ Old_set[3:0].</p> <p>Rationale: More bits on each XOR can give better statistical uniformity on sets and since two lsbs are taken for each tile row size, it reduces the chance of aliasing on sets.</p> </td></tr> <tr> <td>11b</td><td>Scheme 3 [Default]</td><td> <p>New_set_mask[3] = Tiled_address[22] ^ Tiled_address[21] ^ Tiled_address[20] ^ Tiled_address[19]. New_set_mask[2] = Tiled_address[18] ^ Tiled_address[17] ^ Tiled_address[16]. New_set_mask[1] = Tiled_address[15] ^ Tiled_address[14]. New_set_mask[0] = Tiled_address[13]. New_set[3:0] less than or = New_set_mask[3:0] ^ Old_set[3:0].</p> <p>Rationale: More bits on each XOR can give better statistical uniformity on sets and since each XOR has different bits, it reduces the chance of aliasing on sets even more.</p> </td></tr> </tbody> </table>	Value	Name	Description	00b	None	No XOR.	01b	Scheme 1	<p>New_set_mask[3:0] = Tiled_address[16:13]. New_set[3:0] less than or = New_set_mask[3:0] ^ Old_set[3:0].</p> <p>Rationale: These bits can distinguish among 16 different equivalent classes of virtual pages. These bits also represent the lsb for tile rows ranging from a pitch of 1 tile to 16 tiles.</p>	10b	Scheme 2	<p>New_set_mask[3] = Tiled_address[17] ^ Tiled_address[16]. New_set_mask[2] = Tiled_address[16] ^ Tiled_address[15]. New_set_mask[1] = Tiled_address[15] ^ Tiled_address[14]. New_set_mask[0] = Tiled_address[14] ^ Tiled_address[13]. New_set[3:0] less than or = New_set_mask[3:0] ^ Old_set[3:0].</p> <p>Rationale: More bits on each XOR can give better statistical uniformity on sets and since two lsbs are taken for each tile row size, it reduces the chance of aliasing on sets.</p>	11b	Scheme 3 [Default]	<p>New_set_mask[3] = Tiled_address[22] ^ Tiled_address[21] ^ Tiled_address[20] ^ Tiled_address[19]. New_set_mask[2] = Tiled_address[18] ^ Tiled_address[17] ^ Tiled_address[16]. New_set_mask[1] = Tiled_address[15] ^ Tiled_address[14]. New_set_mask[0] = Tiled_address[13]. New_set[3:0] less than or = New_set_mask[3:0] ^ Old_set[3:0].</p> <p>Rationale: More bits on each XOR can give better statistical uniformity on sets and since each XOR has different bits, it reduces the chance of aliasing on sets even more.</p>
Value	Name	Description														
00b	None	No XOR.														
01b	Scheme 1	<p>New_set_mask[3:0] = Tiled_address[16:13]. New_set[3:0] less than or = New_set_mask[3:0] ^ Old_set[3:0].</p> <p>Rationale: These bits can distinguish among 16 different equivalent classes of virtual pages. These bits also represent the lsb for tile rows ranging from a pitch of 1 tile to 16 tiles.</p>														
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11b	Scheme 3 [Default]	<p>New_set_mask[3] = Tiled_address[22] ^ Tiled_address[21] ^ Tiled_address[20] ^ Tiled_address[19]. New_set_mask[2] = Tiled_address[18] ^ Tiled_address[17] ^ Tiled_address[16]. New_set_mask[1] = Tiled_address[15] ^ Tiled_address[14]. New_set_mask[0] = Tiled_address[13]. New_set[3:0] less than or = New_set_mask[3:0] ^ Old_set[3:0].</p> <p>Rationale: More bits on each XOR can give better statistical uniformity on sets and since each XOR has different bits, it reduces the chance of aliasing on sets even more.</p>														
This field should be programmed as "00b" corresponding to NO XOR option when the 3D map performance fix in MT is enabled using the field " Sampler Set Remapping for 3D Disable " in CACHE_MODE_0 - Cache Mode Register 0 .																

CACHE_MODE_1 - Cache Mode Register 1

	6	4X4 RCPFE-STC Optimization Disable									
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>r/w</td></tr> <tr> <td>Format:</td><td>Disable</td></tr> </table>	Project:	BDW	Access:	r/w	Format:	Disable			
Project:	BDW										
Access:	r/w										
Format:	Disable										
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0h</td><td>[Default]</td><td>Enables two contiguous 4x2s to be collected as 4X4 access for STC interface. This allows for less bank collision and less RAM power on STC.</td></tr> <tr> <td>1h</td><td></td><td>Disables this optimization and therefore only one valid 4x2 is sent to STC on the 4X4 interface.</td></tr> </tbody> </table>	Value	Name	Description	0h	[Default]	Enables two contiguous 4x2s to be collected as 4X4 access for STC interface. This allows for less bank collision and less RAM power on STC.	1h		Disables this optimization and therefore only one valid 4x2 is sent to STC on the 4X4 interface.
Value	Name	Description									
0h	[Default]	Enables two contiguous 4x2s to be collected as 4X4 access for STC interface. This allows for less bank collision and less RAM power on STC.									
1h		Disables this optimization and therefore only one valid 4x2 is sent to STC on the 4X4 interface.									
		<table border="1"> <thead> <tr> <th>Restriction</th></tr> </thead> <tbody> <tr> <td></td></tr> </tbody> </table>	Restriction								
Restriction											
	5	MCS Cache Disable									
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>r/w</td></tr> <tr> <td>Format:</td><td>Disable</td></tr> </table> <p>For Programming restrictions please refer to the 3D Pipeline.</p>	Project:	BDW	Access:	r/w	Format:	Disable			
Project:	BDW										
Access:	r/w										
Format:	Disable										
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0h</td><td>[Default]</td><td>MCS cache enabled. It allows RTs with MCS buffer enabled to be rendered using either MSAA compression for MSRT OR with color clear feature for non MSRT.</td></tr> <tr> <td>1h</td><td></td><td>MCS cache is disabled. Hence no MSAA compression for MSRT and no color clear for non-MSRT.</td></tr> </tbody> </table>	Value	Name	Description	0h	[Default]	MCS cache enabled. It allows RTs with MCS buffer enabled to be rendered using either MSAA compression for MSRT OR with color clear feature for non MSRT.	1h		MCS cache is disabled. Hence no MSAA compression for MSRT and no color clear for non-MSRT.
Value	Name	Description									
0h	[Default]	MCS cache enabled. It allows RTs with MCS buffer enabled to be rendered using either MSAA compression for MSRT OR with color clear feature for non MSRT.									
1h		MCS cache is disabled. Hence no MSAA compression for MSRT and no color clear for non-MSRT.									
	4	Reserved									
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>r/w</td></tr> <tr> <td>Format:</td><td>PBC</td></tr> </table>	Project:	BDW	Access:	r/w	Format:	PBC			
Project:	BDW										
Access:	r/w										
Format:	PBC										
	3	Depth Read Hit Write-Only Optimization Disable									
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>r/w</td></tr> <tr> <td>Format:</td><td>Disable</td></tr> </table>	Project:	BDW	Access:	r/w	Format:	Disable			
Project:	BDW										
Access:	r/w										
Format:	Disable										
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0h</td><td>[Default]</td><td>Read Hit Write-only optimization is enabled in the Depth cache (RCZ).</td></tr> <tr> <td>1h</td><td></td><td>Read Hit Write-only optimization is disabled in the Depth cache (RCZ).</td></tr> </tbody> </table>	Value	Name	Description	0h	[Default]	Read Hit Write-only optimization is enabled in the Depth cache (RCZ).	1h		Read Hit Write-only optimization is disabled in the Depth cache (RCZ).
Value	Name	Description									
0h	[Default]	Read Hit Write-only optimization is enabled in the Depth cache (RCZ).									
1h		Read Hit Write-only optimization is disabled in the Depth cache (RCZ).									

CACHE_MODE_1 - Cache Mode Register 1

	2	RCZ Read after expansion control fix 2	
		Project:	BDW
		Access:	r/w
		Format:	Enable
Value	Name	Description	
0h	[Default]	[BDW] RCZ will always issue a read request to memory, even if it was previously allocated as expansion Cacheline	
1h		[BDW] RCZ will suppress the read request to memory if it was allocated as a expansion Cacheline	
1	Reserved		
		Project:	BDW
		Access:	r/w
		Format:	PBC
0	Reserved		
		Project:	BDW

Capabilities A

CAPID0_A_0_0_0_PCI - Capabilities A						
DWord	Bit	Description				
0	31	Display HD Audio Disable <table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W Key Firmware Only</td></tr> </table> 0: Display HD Audio Enabled 1: Display HD Audio Disabled	Default Value:	0b	Access:	R/W Key Firmware Only
Default Value:	0b					
Access:	R/W Key Firmware Only					
	30	PEG12 Disable <table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W Key Firmware Only</td></tr> </table>	Default Value:	0b	Access:	R/W Key Firmware Only
Default Value:	0b					
Access:	R/W Key Firmware Only					
	29	PEG11 Disable <table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W Key Firmware Only</td></tr> </table>	Default Value:	0b	Access:	R/W Key Firmware Only
Default Value:	0b					
Access:	R/W Key Firmware Only					
	28	PEG10 Disable <table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W Key Firmware Only</td></tr> </table>	Default Value:	0b	Access:	R/W Key Firmware Only
Default Value:	0b					
Access:	R/W Key Firmware Only					
	27	PCI Express Link Width Upconfig Disable <table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W Firmware Only</td></tr> </table>	Default Value:	0b	Access:	R/W Firmware Only
Default Value:	0b					
Access:	R/W Firmware Only					
	26	DMI Width <table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W Firmware Only</td></tr> </table>	Default Value:	0b	Access:	R/W Firmware Only
Default Value:	0b					
Access:	R/W Firmware Only					
	25	ECC Disable <table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W Firmware Only</td></tr> </table>	Default Value:	0b	Access:	R/W Firmware Only
Default Value:	0b					
Access:	R/W Firmware Only					
	24	Force DRAM ECC Enabled <table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W Firmware Only</td></tr> </table>	Default Value:	0b	Access:	R/W Firmware Only
Default Value:	0b					
Access:	R/W Firmware Only					

CAPID0_A_0_0_0_PCI - Capabilities A

	23	VTd Disable
		Default Value: 0b
		Access: R/W Firmware Only
0: Enable VTd 1: Disable VTd		
	22	DMI Gen 2 Disable
		Default Value: 0b
		Access: R/W Firmware Only
	21	PEG Gen 2 Disable
		Default Value: 0b
		Access: R/W Firmware Only
	20:19	DDR Size
		Default Value: 00b
		Access: R/W Firmware Only
	18	Bclk overclocking disable
		Default Value: 0b
		Access: R/W Firmware Only
	17	Disable 1N Mode
		Default Value: 0b
		Access: R/W Firmware Only
	16	Full ULT Fuse Read Disable
		Default Value: 0b
		Access: R/W Firmware Only
	15	Camarillo Device Disable
		Default Value: 0b
		Access: R/W Firmware Only
	14	2 DIMMS per Channel Disable
		Default Value: 0b
		Access: R/W Firmware Only
	13	X2APIC Enabled
		Default Value: 0b
		Access: R/W Firmware Only
	12	Performance Dual Channel Disable
		Default Value: 0b
		Access: R/W Firmware Only

CAPID0_A_0_0_0_PCI - Capabilities A

	11	Internal Graphics Disable				
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W Key Firmware Only</td></tr> </table>	Default Value:	0b	Access:	R/W Key Firmware Only
Default Value:	0b					
Access:	R/W Key Firmware Only					
		<p>0b: There is a graphics engine within this CPU. Internal Graphics Device (Device 2) is enabled and all of its memory and I/O spaces are accessible. Configuration cycles to Device 2 will be completed within the CPU. All non-SMM memory and IO accesses to VGA will be handled based on Memory and IO enables of Device 2 and IO registers within Device 2 and VGA Enable of the PCI to PCI bridge control (If PCI Express GFX attach is supported). A selected amount of Graphics Memory space is pre-allocated from the main memory based on Graphics Mode Select (GMS in the GGC Register). Graphics Memory is pre-allocated above TSEG Memory. 1b: There is no graphics engine within this CPU. Internal Graphics Device (Device 2) and all of its memory and I/O functions are disabled. Configuration cycle targeted to Device 2 will be passed on. All non-SMM memory and IO accesses to VGA will be handled based on VGA Enable of the PCI to PCI bridge control. Device 2 is disabled and hidden.</p>				
	10	Reserved				
	9:8	Capability Device ID				
		<table border="1"> <tr> <td>Default Value:</td><td>00b</td></tr> <tr> <td>Access:</td><td>R/W Firmware Only</td></tr> </table>	Default Value:	00b	Access:	R/W Firmware Only
Default Value:	00b					
Access:	R/W Firmware Only					
	7:4	Compatibility Rev ID				
		<table border="1"> <tr> <td>Default Value:</td><td>0000b</td></tr> <tr> <td>Access:</td><td>R/W Firmware Only</td></tr> </table> <p>This is an 8-bit value that indicates the revision identification number for the Host Device 0.</p>	Default Value:	0000b	Access:	R/W Firmware Only
Default Value:	0000b					
Access:	R/W Firmware Only					
	3	DDR Overclocking				
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W Firmware Only</td></tr> </table>	Default Value:	0b	Access:	R/W Firmware Only
Default Value:	0b					
Access:	R/W Firmware Only					
	2	IA Overclocking Enabled by DSKU				
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W Firmware Only</td></tr> </table>	Default Value:	0b	Access:	R/W Firmware Only
Default Value:	0b					
Access:	R/W Firmware Only					
	1	DDR Write VRef				
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W Firmware Only</td></tr> </table>	Default Value:	0b	Access:	R/W Firmware Only
Default Value:	0b					
Access:	R/W Firmware Only					
	0	DDR3L Enable				
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W Firmware Only</td></tr> </table>	Default Value:	0b	Access:	R/W Firmware Only
Default Value:	0b					
Access:	R/W Firmware Only					

Capabilities B

CAPID0_B_0_0_0_PCI - Capabilities B		
DWord	Bit	Description
0	31	SPARE31
		Default Value: 0b
		Access: R/W Firmware Only
	30	IA Overclocking DSKU Control Disable
		Default Value: 0b
		Access: R/W Firmware Only
	29	IA Overclocking Enable
		Default Value: 0b
		Access: R/W Firmware Only
	28	SMT Capability
		Default Value: 0b
		Access: R/W Firmware Only
27:25	27:25	Cache Size Capability
		Default Value: 000b
		Access: R/W Firmware Only
	24	SPARE24
		Default Value: 0b
		Access: R/W Firmware Only
	23:21	DDR3 Maximum Frequency Capability with 100 Memory
		Default Value: 000b
		Access: R/W Firmware Only
20	20	Gen3 Disable Fuse for PCIe PEG Controllers
		Default Value: 0b
		Access: R/W Firmware Only
	19	Package Type
		Default Value: 0b
		Access: R/W Firmware Only

CAPID0_B_0_0_0_PCI - Capabilities B							
	18	Additive Graphics Enabled					
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W Firmware Only</td></tr> </table>	Default Value:	0b	Access:	R/W Firmware Only	0 - Additive Graphics Disabled 1- Additive Graphics Enabled
Default Value:	0b						
Access:	R/W Firmware Only						
	17	Additive Graphics Capable					
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W Firmware Only</td></tr> </table>	Default Value:	0b	Access:	R/W Firmware Only	0 - Capable of Additive Graphics 1 - Not capable of Additive Graphics
Default Value:	0b						
Access:	R/W Firmware Only						
	16	Primary PEG Port x16 Disable					
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W Firmware Only</td></tr> </table>	Default Value:	0b	Access:	R/W Firmware Only	
Default Value:	0b						
Access:	R/W Firmware Only						
	15:12	SPARE15_12					
		<table border="1"> <tr> <td>Default Value:</td><td>0000b</td></tr> <tr> <td>Access:</td><td>R/W Firmware Only</td></tr> </table>	Default Value:	0000b	Access:	R/W Firmware Only	
Default Value:	0000b						
Access:	R/W Firmware Only						
	11	Reserved					
	10:8	SPARE10_8					
		<table border="1"> <tr> <td>Default Value:</td><td>000b</td></tr> <tr> <td>Access:</td><td>R/W Firmware Only</td></tr> </table>	Default Value:	000b	Access:	R/W Firmware Only	
Default Value:	000b						
Access:	R/W Firmware Only						
	7	Reserved					
	6:4	DDR3 Maximum Frequency Capability					
		<table border="1"> <tr> <td>Default Value:</td><td>000b</td></tr> <tr> <td>Access:</td><td>R/W Firmware Only</td></tr> </table>	Default Value:	000b	Access:	R/W Firmware Only	
Default Value:	000b						
Access:	R/W Firmware Only						
	3	SPARE3					
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W Firmware Only</td></tr> </table>	Default Value:	0b	Access:	R/W Firmware Only	
Default Value:	0b						
Access:	R/W Firmware Only						
	2	DDR4 Enable					
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W Firmware Only</td></tr> </table>	Default Value:	0b	Access:	R/W Firmware Only	
Default Value:	0b						
Access:	R/W Firmware Only						
	1	Dual PEG Force x1 when VGA Enabled					
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W Firmware Only</td></tr> </table>	Default Value:	0b	Access:	R/W Firmware Only	
Default Value:	0b						
Access:	R/W Firmware Only						
	0	Single PEG Force x1 when VGA Enabled					
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W Firmware Only</td></tr> </table>	Default Value:	0b	Access:	R/W Firmware Only	
Default Value:	0b						
Access:	R/W Firmware Only						

Capabilities Control

CAPCTRL0_0_2_0_PCI - Capabilities Control				
DWord	Bit	Description		
0	11:8	CAPID Version		
		<table border="1"> <tr> <td>Default Value:</td> <td>0001b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>This field is hardwired to the value 1h to identify the first revision of the CAPID register definition.</p>	Default Value:	0001b
Default Value:	0001b			
Access:	RO			
	7:0	CAPID Length		
		<table border="1"> <tr> <td>Default Value:</td> <td>00001100b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>This field is hardwired to the value 0Ch to indicate the structure length (12 bytes).</p>	Default Value:	00001100b
Default Value:	00001100b			
Access:	RO			

Capabilities Pointer

CAPPOINT_0_2_0_PCI-CapabilitiesPointer						
Register Space:	PCI: 0/2/0					
Project:	BDW					
Default Value:	0x00000090					
Size (in bits):	8					
Address:	00034h					
This register points to a linked list of capabilities implemented by this device.						
DWord	Bit	Description				
0	7:0	<p>Capabilities Pointer Value</p> <table border="1"> <tr> <td>Default Value:</td><td>10010000b</td></tr> <tr> <td>Access:</td><td>RO Variant</td></tr> </table> <p>This field contains an offset into the function's PCI Configuration Space for the first item in the New Capabilities Linked List.</p>	Default Value:	10010000b	Access:	RO Variant
Default Value:	10010000b					
Access:	RO Variant					

Capabilities Pointer

CAPPTR - Capabilities Pointer						
DWord	Bit	Description				
0	31:8	Reserved <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ		
Format:	MBZ					
	7:0	Capability Pointer <table border="1"> <tr> <td>Default Value:</td> <td>50h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Indicates that the first capability pointer offset is offset 50h.</p>	Default Value:	50h	Access:	RO
Default Value:	50h					
Access:	RO					

Capability Identifier

CAPID0_0_2_0_PCI - Capability Identifier						
Register Space:	PCI: 0/2/0					
Project:	BDW					
Default Value:	0x00000009					
Size (in bits):	16					
Address:	00040h					
DWord	Bit	Description				
0	15:8	Next Capability Pointer				
		<table border="1"> <tr> <td>Default Value:</td><td>00000000b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> <tr> <td colspan="2">This field is hardwired to 00h indicating the end of the capabilities linked list.</td></tr> </table>	Default Value:	00000000b	Access:	RO
Default Value:	00000000b					
Access:	RO					
This field is hardwired to 00h indicating the end of the capabilities linked list.						
	7:0	Capability Identifier				
		<table border="1"> <tr> <td>Default Value:</td><td>00001001b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> <tr> <td colspan="2">This field is hardwired to the value 09h to identify the CAP_ID assigned by the PCI SIG for vendor dependent capability pointers.</td></tr> </table>	Default Value:	00001001b	Access:	RO
Default Value:	00001001b					
Access:	RO					
This field is hardwired to the value 09h to identify the CAP_ID assigned by the PCI SIG for vendor dependent capability pointers.						

CDCLK_FREQ

CDCLK_FREQ				
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x0000001C1 Access: R/W Size (in bits): 32				
Address: 46200h-46203h Name: CD Clock Frequency ShortName: CDCLK_FREQ Power: Always on Reset: global				
DWord	Bit	Description		
0	31:10	Reserved <table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ
Format:	MBZ			
9:0	CDclk frequency <table border="1"> <tr> <td>Default Value:</td><td>01 1100 0001b 450MHz</td></tr> </table> <p>Program this field to the CD clock frequency minus one. This is used to generate a divided down clock for miscellaneous timers in display. The CD clock frequency is selected in LCPLL_CTL.</p>	Default Value:	01 1100 0001b 450MHz	
Default Value:	01 1100 0001b 450MHz			

CGE_CTRL

CGE_CTRL								
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x00000000 Access: Double Buffered Size (in bits): 32 Double Buffer Update Point: Start of vertical blank								
Address: 49080h-49083h Name: Pipe A Color Gamut Enhancement Control ShortName: CGE_CTRL_A Valid Projects: BDW Power: Always on Reset: soft								
Address: 49180h-49183h Name: Pipe B Color Gamut Enhancement Control ShortName: CGE_CTRL_B Valid Projects: BDW Power: off/on Reset: soft								
Address: 49280h-49283h Name: Pipe C Color Gamut Enhancement Control ShortName: CGE_CTRL_C Valid Projects: BDW Power: off/on Reset: soft								
DWord	Bit	Description						
0	31	CGE Enable This bit enables the Color Gamut Enhancement logic. <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Disable</td></tr> <tr> <td>1b</td><td>Enable</td></tr> </tbody> </table>	Value	Name	0b	Disable	1b	Enable
Value	Name							
0b	Disable							
1b	Enable							
Reserved Format: MBZ								

CGE_WEIGHT

CGE_WEIGHT				
Register Space:	MMIO: 0/2/0			
Project:	BDW			
Default Value:	0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000			
Access:	R/W			
Size (in bits):	160			
Address:	49090h-490A3h			
Name:	Pipe A Color Gamut Enhancement Weights			
ShortName:	CGE_WEIGHT_A_*			
Valid Projects:	BDW			
Power:	Always on			
Reset:	soft			
Address:	49190h-491A3h			
Name:	Pipe B Color Gamut Enhancement Weights			
ShortName:	CGE_WEIGHT_B_*			
Valid Projects:	BDW			
Power:	off/on			
Reset:	soft			
Address:	49290h-492A3h			
Name:	Pipe C Color Gamut Enhancement Weights			
ShortName:	CGE_WEIGHT_C_*			
Valid Projects:	BDW			
Power:	off/on			
Reset:	soft			
These are the weights contained in the lookup up table (LUT) used in pipe color gamut enhancement. LUT index 0 contains the weight for the least saturated colors, and LUT index 16 contains the weight for the most saturated colors. Weight values can range from 00000b (100% of the enhanced output color is from the pipe gamma and CSC output corrected color) to 100000b (100% of the enhanced output color is from the pipe gamma and CSC input color).				
Restriction				
The weight values should only be changed while color gamut enhancement is disabled, otherwise screen artifacts may show temporarily.				
DWord	Bit	Description		
0	31:30	Reserved		
		Format: MBZ		
	29:24	CGE Weight Index 3 This is the weight value for this color gamut enhancement LUT index.		

CGE_WEIGHT		
	23:22	Reserved Format: <input type="text"/> MBZ
	21:16	CGE Weight Index 2 This is the weight value for this color gamut enhancement LUT index.
	15:14	Reserved Format: <input type="text"/> MBZ
	13:8	CGE Weight Index 1 This is the weight value for this color gamut enhancement LUT index.
	7:6	Reserved Format: <input type="text"/> MBZ
	5:0	CGE Weight Index 0 This is the weight value for this color gamut enhancement LUT index.
	1	31:30 Reserved Format: <input type="text"/> MBZ
	29:24	CGE Weight Index 7 This is the weight value for this color gamut enhancement LUT index.
	23:22	Reserved Format: <input type="text"/> MBZ
	21:16	CGE Weight Index 6 This is the weight value for this color gamut enhancement LUT index.
	15:14	Reserved Format: <input type="text"/> MBZ
	13:8	CGE Weight Index 5 This is the weight value for this color gamut enhancement LUT index.
	7:6	Reserved Format: <input type="text"/> MBZ
	5:0	CGE Weight Index 4 This is the weight value for this color gamut enhancement LUT index.
	2	31:30 Reserved Format: <input type="text"/> MBZ
	29:24	CGE Weight Index 11 This is the weight value for this color gamut enhancement LUT index.
	23:22	Reserved Format: <input type="text"/> MBZ
	21:16	CGE Weight Index 10 This is the weight value for this color gamut enhancement LUT index.
	15:14	Reserved Format: <input type="text"/> MBZ

CGE_WEIGHT		
	13:8	CGE Weight Index 9 This is the weight value for this color gamut enhancement LUT index.
	7:6	Reserved Format: <input type="text"/> MBZ
	5:0	CGE Weight Index 8 This is the weight value for this color gamut enhancement LUT index.
3	31:30	Reserved Format: <input type="text"/> MBZ
	29:24	CGE Weight Index 15 This is the weight value for this color gamut enhancement LUT index.
	23:22	Reserved Format: <input type="text"/> MBZ
	21:16	CGE Weight Index 14 This is the weight value for this color gamut enhancement LUT index.
	15:14	Reserved Format: <input type="text"/> MBZ
	13:8	CGE Weight Index 13 This is the weight value for this color gamut enhancement LUT index.
	7:6	Reserved Format: <input type="text"/> MBZ
	5:0	CGE Weight Index 12 This is the weight value for this color gamut enhancement LUT index.
	31:6	Reserved Format: <input type="text"/> MBZ
	5:0	CGE Weight Index 16 This is the weight value for this color gamut enhancement LUT index.

CLASS

CLASS						
DWord	Bit	Description				
0	31:24	<p>Base Class Code</p> <table border="1"> <tr> <td>Default Value:</td> <td>04h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>This register indicates that the function implements a multimedia device.</p>	Default Value:	04h	Access:	RO
Default Value:	04h					
Access:	RO					
23:16	<p>Sub Class Code</p> <table border="1"> <tr> <td>Default Value:</td> <td>03h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>This indicates the device is an Intel HD Audio audio device, in the context of a multimedia device.</p>	Default Value:	03h	Access:	RO	
Default Value:	03h					
Access:	RO					
15:8	<p>Programming Interface</p> <table border="1"> <tr> <td>Default Value:</td> <td>00h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Value assigned to the Intel HD Audio controller.</p>	Default Value:	00h	Access:	RO	
Default Value:	00h					
Access:	RO					
7:0	<p>Revision ID</p> <table border="1"> <tr> <td>Default Value:</td> <td>00h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Indicates the device specific revision identifier.</p>	Default Value:	00h	Access:	RO	
Default Value:	00h					
Access:	RO					

Class Code

CC_0_2_0_PCI - Class Code						
DWord	Bit	Description				
0	23:16	<p>Base Class Code</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000011b</td> </tr> <tr> <td>Access:</td> <td>RO Variant</td> </tr> </table> <p>This is an 8-bit value that indicates the base class code. When MGGC0[VAMEN] is 0 this code has the value 03h, indicating a Display Controller. When MGGC0[VAMEN] is 1 this code has the value 04h, indicating a Multimedia Device.</p>	Default Value:	00000011b	Access:	RO Variant
Default Value:	00000011b					
Access:	RO Variant					
	15:8	<p>Sub-Class Code</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000b</td> </tr> <tr> <td>Access:</td> <td>RO Variant</td> </tr> </table> <p>When MGGC0[VAMEN] is 0 this value will be determined based on Device 0 GGC register, GMS and IVD fields. 00h: VGA compatible 80h: Non VGA (GMS = "00h" or IVD = "1b") When MGGC0[VAMEN] is 1, this value is 80h, indicating other multimedia device.</p>	Default Value:	00000000b	Access:	RO Variant
Default Value:	00000000b					
Access:	RO Variant					
	7:0	<p>Programming Interface</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>When MGGC0[VAMEN] is 0 this value is 00h, indicating a Display Controller. When MGGC0[VAMEN] is 1 this value is 00h, indicating a NOP.</p>	Default Value:	00000000b	Access:	RO
Default Value:	00000000b					
Access:	RO					

Clipper Invocation Counter

CL_INVOCATION_COUNT - Clipper Invocation Counter		
DWord	Bit	Description
0	63:32	CL Invocation Count Report UDW Number of objects entering the clipper stage. Updated only when Statistics Enable is set in CLIP_STATE (see the Clipper Chapter in the 3D Volume.)
	31:0	CL Invocation Count Report LDW Number of objects entering the clipper stage. Updated only when Statistics Enable is set in CLIP_STATE (see the Clipper Chapter in the 3D Volume.)

Clipper Primitives Counter

CL_PRIMITIVES_COUNT - Clipper Primitives Counter		
Register Space: MMIO: 0/2/0 Project: BDW Source: RenderCS Default Value: 0x00000000, 0x00000000 Access: R/W Size (in bits): 64 Trusted Type: 1		
Address: 02340h Valid Projects: BDW		
This register reflects the total number of primitives that have been output by the clipper. This register is part of the context save and restore.		
DWord	Bit	Description
0	63:32	Clipped Primitives Output Count UDW Total number of primitives output by the clipper stage. This count is updated for every primitive output by the clipper stage, as long as Statistics Enable is set in SF_STATE (see the Clipper and SF Chapters in the 3D Volume.)
	31:0	Clipped Primitives Output Count LDW Total number of primitives output by the clipper stage. This count is updated for every primitive output by the clipper stage, as long as Statistics Enable is set in SF_STATE (see the Clipper and SF Chapters in the 3D Volume.)

CLKGATE Messaging Register for Clocking Unit

MSG_CLKGATE_GCP - CLKGATE Messaging Register for Clocking Unit

Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	16					
Address:	0802Ch					
Message registers have bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16]. To set bit0, for example, the data would be 0x0001_0001. To clear bit0, for example, the data would be 0x0001_0000. Note that mask bit is the data bit offset + 16. Message registers are protected from non-GT writes via the Message Channel.						
DWord	Bit	Description				
0	15:7	Reserved <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Project:	BDW	Access:	RO
Project:	BDW					
Access:	RO					
6	Gate cmclk Acknowledgement (VCS1) <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Gate cmclk Acknowledgement (VCS1). 1'b0: Clocks are ungated (default). 1'b1: Clocks are gated.</p>	Access:	R/W			
Access:	R/W					
5	Gate cwclk Acknowledgement (WIN) <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Gate cwclk Acknowledgement (WIN). 1'b0: Clocks are ungated (default). 1'b1: Clocks are gated.</p>	Access:	R/W			
Access:	R/W					
4	Reserved					
3	Gate cfclk Acknowledgement (CS) <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Gate cfclk Acknowledgement (CS). 1'b0: Clocks are ungated (default). 1'b1: Clocks are gated.</p>	Access:	R/W			
Access:	R/W					
2	Gate cvclk Acknowledgement (VECS) <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Gate cvclk Acknowledgement (VECS). 1'b0: Clocks are ungated (default). 1'b1: Clocks are gated.</p>	Access:	R/W			
Access:	R/W					
1						

MSG_CLKGATE_GCP - CLKGATE Messaging Register for Clocking Unit

	1	Gate cmclk Acknowledgement (VCS0)		
		<table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Gate cmclk Acknowledgement (VCS0). 1'b0: Clocks are ungated (default). 1'b1: Clocks are gated.</p>	Access:	R/W
Access:	R/W			
	0	Gate crclk Acknowledgement (CS)		
		<table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Gate crclk Acknowledgement (CS). 1'b0: Clocks are ungated (default). 1'b1: Clocks are gated.</p>	Access:	R/W
Access:	R/W			

Clock Gating Messages

CGMSG - Clock Gating Messages						
DWord	Bit	Description				
0	31:16	<p>Message Mask</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Message Mask In order to write to bits 15:0, the corresponding message mask bits must be written. For example, for bit 14 to be set, bit 30 needs to be 1 : 40004000</p>	Access:	RO		
Access:	RO					
	15:7	<p>Reserved</p> <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Reserved</p>	Project:	BDW	Access:	RO
Project:	BDW					
Access:	RO					
	6	<p>Media 1 Clock gating control message</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Gate Media 1 (2nd Vbox) Clock Message : '0' : Media 1 Clock Un-gate Request (un-gates the cmclk clock in the 2n Media block) '1' : Media 1 Clock Gate Request (gates the cmclk clock in the 2nd Media block)</p>	Access:	R/W		
Access:	R/W					
	5	<p>WIDI Clock Gating control Message</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Gate WIDI Clock Message : '0' : WIDI Clock Un-gate Request (un-gates the cwclk clock) '1' : WIDI Clock Gate Request (gates the cwclk clock)</p>	Access:	R/W		
Access:	R/W					
	4	<p>Reserved</p>				
	3	<p>Fix Function Clock gating Control Message</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Gate Fix Clock Message : '0' : Fix Clock Un-gate Request (un-gates the cfclk/cf2xclk clock) '1' : Fix Clock Gate Request (gates the cfclk/cf2xclk clock)</p>	Access:	R/W		
Access:	R/W					
	2	<p>VEbox Clock gating Control message</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Gate VE-box Clock Message : '0' : VEbox Clock Un-gate Request (un-gates the cvclk clock) '1' : VEbox Clock Gate Request (gates the cvclk clock)</p>	Access:	R/W		
Access:	R/W					

CGMSG - Clock Gating Messages			
	1	Media 0 Clock Gating Control Message	
		<table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Gate Media Clock Message : '0' : Media 0 Clock Un-gate Request (un-gates the cmclk clock) '1' : Media 0 Clock Gate Request (gates the cmclk clock)</p>	Access:
Access:	R/W		
	0	Row Clock Gating Control Message	
		<table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Gate Row Clocks Message : '0' : Row Clock Un-gate Request (un-gates the crclk and cr2xclk clocks) '1' : Row Clock Gate Request (gates the crclk and cr2xclk clocks)</p>	Access:
Access:	R/W		

CLS

CLS		
Register Space: PCI: 0/3/0 Project: BDW Default Value: 0x00000000 Access: R/W Size (in bits): 32		
Address: 0000Ch-0000Fh Name: Cache Line Size, Latency Timer, Header Type and Built in Self Test ShortName: CLS Power: Always on Reset: global		
DWord	Bit	Description
0	31:8	Reserved Format: MBZ
	7:0	Cache Line Size Default Value: 00h Access: R/W Doesn't apply to PCI Express. PCI Express spec requires this to be implemented as a R/W register but has no functional impact on the Display HD Audio. The cacheline size is always 64B.

Color/Depth Write FIFO Watermarks

CZWMRK - Color/Depth Write FIFO Watermarks		
Register Space: MMIO: 0/2/0		
Project: BDW		
Source: RenderCS		
Default Value: 0x00000000		
Access: R/W		
Size (in bits): 32		
Trusted Type: 1		
Address: 04060h		
This register is directly mapped to the current Virtual Addresses in the MTTLB (Texture and constant cache TLB).		
DWord	Bit	Description
0	31:24	Reserved
		Format: MBZ
	23:18	Color Wr Burst Size This is the maximum size of the requests burst, from the last High Watermark trip, before reevaluating the High Watermark again.
	17:16	Reserved
		Format: MBZ
	15:12	Color Wr FIFO High Watermark This is the number of accumulated Color writes that will trigger a Burst of Z Writes.
	11:6	Z Wr Burst Size This is the maximum size of the requests burst, from the last High Watermark trip, before reevaluating the High Watermark again.
	5:4	Reserved
		Format: MBZ
	3:0	Z Wr FIFO High Watermark This is the number of accumulated Depth writes that will trigger a Burst of Z Writes.

Command and Status

CMD_STS - Command and Status						
DWord	Bit	Description				
0	31	<p>Detected Parity Error</p> <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Not implemented. Hardwired to 0.</p>	Default Value:	0b	Access:	RO
Default Value:	0b					
Access:	RO					
	30	<p>SERR# Status</p> <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Not implemented. Hardwired to 0.</p>	Default Value:	0b	Access:	RO
Default Value:	0b					
Access:	RO					
	29	<p>Received Master Abort</p> <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Not implemented. Hardwired to 0.</p>	Default Value:	0b	Access:	RO
Default Value:	0b					
Access:	RO					
	28	<p>Received Target Abort</p> <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Not implemented. Hardwired to 0.</p>	Default Value:	0b	Access:	RO
Default Value:	0b					
Access:	RO					
	27	<p>Signaled Target-Abort</p> <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Not implemented. Hardwired to 0.</p>	Default Value:	0b	Access:	RO
Default Value:	0b					
Access:	RO					
	26:25	<p>DEVSEL# Timing Status</p> <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Does not apply. Hardwired to 00b.</p>	Default Value:	0b	Access:	RO
Default Value:	0b					
Access:	RO					

CMD_STS - Command and Status												
	24	Master Data Parity Error										
		Default Value:	0b									
		Access:	RO									
		Not implemented. Hardwired to 0.										
	23	Fast Back to Back Capable										
		Default Value:	0b									
		Access:	RO									
		Does not apply. Hardwired to 0.										
	22	Reserved										
		Format:	MBZ									
	21	66 MHz Capable										
		Default Value:	0b									
		Access:	RO									
		Does not apply. Hardwired to 0.										
	20	Capabilities List Exists										
		Default Value:	1b									
		Access:	RO									
		Indicates dHDA contains a capabilities list. The first item is pointed to by looking at configuration offset 34h.										
	19	Interrupt Status										
		Access:	RO									
		Reflects the state of the INTx# signal at the input of the enable/disable circuit. Note that this bit is not set by an MSI.										
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Cleared [Default]</td><td>This bit is a 0 after the interrupt is cleared (independent of the state of the Interrupt Disable bit in the command register).</td></tr> <tr> <td>1b</td><td>Asserted</td><td>The INTx# is asserted.</td></tr> </tbody> </table>		Value	Name	Description	0b	Cleared [Default]	This bit is a 0 after the interrupt is cleared (independent of the state of the Interrupt Disable bit in the command register).	1b	Asserted	The INTx# is asserted.
Value	Name	Description										
0b	Cleared [Default]	This bit is a 0 after the interrupt is cleared (independent of the state of the Interrupt Disable bit in the command register).										
1b	Asserted	The INTx# is asserted.										
	18:11	Reserved										
		Format:	MBZ									
	10	Interrupt Disable										
		Access:	R/W									
		Enables the device to assert an INTx#. Note that this bit does not affect the generation of MSI's.										
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Cleared [Default]</td><td>When cleared, the INTx# signal may be asserted</td></tr> <tr> <td>1b</td><td>Deasserted</td><td>When set, the Intel HD Audio controller's INTx# signal will be deasserted</td></tr> </tbody> </table>		Value	Name	Description	0b	Cleared [Default]	When cleared, the INTx# signal may be asserted	1b	Deasserted	When set, the Intel HD Audio controller's INTx# signal will be deasserted
Value	Name	Description										
0b	Cleared [Default]	When cleared, the INTx# signal may be asserted										
1b	Deasserted	When set, the Intel HD Audio controller's INTx# signal will be deasserted										

CMD_STS - Command and Status								
9	Fast Back to Back Enable	Default Value: Access: Not implemented. Hardwired to 0.						
8	SERR Enable	Default Value: Access: Functionality not implemented. This bit is R/W to pass PCIe compliance testing.						
7	Wait Cycle Control	Default Value: Access: Not implemented. Hardwired to 0.						
6	Parity Error Response	Default Value: Access: Functionality not implemented. This bit is R/W to pass PCIe compliance testing.						
5	VGA Palette Snoop	Default Value: Access: Not implemented. Hardwired to 0.						
4	Memory Write and Invalidate Enable	Default Value: Access: Not implemented. Hardwired to 0.						
3	Special Cycle Enable	Default Value: Access: Not implemented. Hardwired to 0.						
2	Bus Master Enable	Access: Controls standard PCI Express bus mastering capabilities for Memory and IO, reads and writes. Note that this also controls MSI generation since MSI are essentially Memory writes. <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center; background-color: #e0e0ff;">Value</th><th style="text-align: center; background-color: #e0e0ff;">Name</th></tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td><td>Disable [Default]</td></tr> <tr> <td style="text-align: center;">1b</td><td>Enable</td></tr> </tbody> </table>	Value	Name	0b	Disable [Default]	1b	Enable
Value	Name							
0b	Disable [Default]							
1b	Enable							

CMD_STS - Command and Status		
	1	Reserved
	0	I/O Space
		Default Value: 0b
		Access: RO
		The Intel HD Audio controller does not implement IO Space, therefore this bit is hardwired to 0.

Configuration Register0 for RPUnit

CONFIG0 - Configuration Register0 for RPUnit							
DWord	Bit	Description					
0	31	<p>Lock for RW/L Fields in this Register</p> <table border="1"> <tr> <td>Access:</td> <td>R/W Lock</td> </tr> <tr> <td colspan="2">0 = Bits of CONFIG0 register are R/W. 1 = All bits of CONFIG0 register are RO (including this lock bit). Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). Lock is reset on a restore after context is captured.</td> </tr> </table>	Access:	R/W Lock	0 = Bits of CONFIG0 register are R/W. 1 = All bits of CONFIG0 register are RO (including this lock bit). Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). Lock is reset on a restore after context is captured.		
Access:	R/W Lock						
0 = Bits of CONFIG0 register are R/W. 1 = All bits of CONFIG0 register are RO (including this lock bit). Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). Lock is reset on a restore after context is captured.							
30:0	<p>Placeholder Bits</p> <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Access:</td> <td>R/W Lock</td> </tr> <tr> <td colspan="2">Placeholder bits for implementation or ECO loops.</td></tr> </table>	Project:	BDW	Access:	R/W Lock	Placeholder bits for implementation or ECO loops.	
Project:	BDW						
Access:	R/W Lock						
Placeholder bits for implementation or ECO loops.							

Configuration Register1 for RPMinit

CONFIG1 - Configuration Register1 for RPMinit							
DWord	Bit	Description					
0	31	<p>Lock for RW/L Fields in this Register</p> <table border="1"> <tr> <td>Access:</td> <td>R/W Lock</td> </tr> <tr> <td colspan="2">0 = Bits of CONFIG0 register are R/W. 1 = All bits of CONFIG0 register are RO (including this lock bit). Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). Lock is reset on a restore after context is captured.</td> </tr> </table>	Access:	R/W Lock	0 = Bits of CONFIG0 register are R/W. 1 = All bits of CONFIG0 register are RO (including this lock bit). Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). Lock is reset on a restore after context is captured.		
Access:	R/W Lock						
0 = Bits of CONFIG0 register are R/W. 1 = All bits of CONFIG0 register are RO (including this lock bit). Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). Lock is reset on a restore after context is captured.							
30:0	<p>Placeholder Bits</p> <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Access:</td> <td>R/W Lock</td> </tr> <tr> <td colspan="2">Placeholder bits for implementation or ECO loops.</td></tr> </table>	Project:	BDW	Access:	R/W Lock	Placeholder bits for implementation or ECO loops.	
Project:	BDW						
Access:	R/W Lock						
Placeholder bits for implementation or ECO loops.							

Configuration Register for RCPunit

RCPCONFIG - Configuration Register for RCPunit						
DWord	Bit	Description				
0	31:5	<p>Placeholder Bits</p> <table border="1"> <tr> <td>Access:</td> <td>R/W Lock</td> </tr> </table> <p>Placeholder bits for implementation or ECO loops.</p>	Access:	R/W Lock		
Access:	R/W Lock					
	4	Reserved				
	3	<p>RPMunit Clock Gating Disable in Uncore Well</p> <table border="1"> <tr> <td>Default Value:</td> <td>1b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Clock Gating Disable Control: '0': Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality). '1': Clock Gating Disabled. (i.e., clocks are toggling, always) (DEFAULT).</p>	Default Value:	1b	Access:	R/W
Default Value:	1b					
Access:	R/W					
	2	<p>MGSRunit Clock Gating Disable in Uncore Well</p> <table border="1"> <tr> <td>Default Value:</td> <td>1b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Clock Gating Disable Control: '0': Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality). '1': Clock Gating Disabled. (i.e., clocks are toggling, always) (DEFAULT).</p>	Default Value:	1b	Access:	R/W
Default Value:	1b					
Access:	R/W					
	1	<p>MDRBunit Clock Gating Disable in Uncore Well</p> <table border="1"> <tr> <td>Default Value:</td> <td>1b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Clock Gating Disable Control: '0': Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality). '1': Clock Gating Disabled. (i.e., clocks are toggling, always) (DEFAULT).</p>	Default Value:	1b	Access:	R/W
Default Value:	1b					
Access:	R/W					

RCPCONFIG - Configuration Register for RCPunit

	0	MCRunit Clock Gating Disable in Uncore Well
		Default Value:
		Access:
<p>Clock Gating Disable Control: '0': Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality). '1': Clock Gating Disabled. (i.e., clocks are toggling, always) (DEFAULT).</p>		

Context Load Protocol Register BLT

BLT_CTX_LD_PRTCL - Context Load Protocol Register BLT

Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000 [BDW]	
Size (in bits):	32	
Address:	04014h	
DWord	Bit	Description
0	31:16	Mask Bits
		Default Value:
15	15	Context Load Protocol Register - BCS 15
		Default Value:
14	14	Context Load Protocol Register - BCS 14
		Default Value:
13	13	Context Load Protocol Register - BCS 13
		Default Value:
12	12	Context Load Protocol Register - BCS 12
		Default Value:
11	11	Context Load Protocol Register - BCS 11
		Default Value:

For Future Use.
This bit is self clear.

BLT_CTX_LD_PRTCL - Context Load Protocol Register BLT

	10	Context Load Protocol Register - BCS 10	
		Default Value:	0b
		Access:	R/W
		For Future Use. This bit is self clear.	
	9	Context Load Protocol Register - BCS 9	
		Default Value:	0b
		Access:	R/W
		For Future Use. This bit is self clear.	
	8	Context Load Protocol Register - BCS 8	
		Default Value:	0b
		Access:	R/W
		For Future Use. This bit is self clear.	
	7	Context Load Protocol Register - BCS 7	
		Default Value:	0b
		Access:	R/W
		For Future Use. This bit is self clear.	
	6	Context Load Protocol Register - BCS 6	
		Default Value:	0b
		Access:	R/W
		For Future Use. This bit is self clear.	
	5	Context Load Protocol Register - BCS 5	
		Default Value:	0b
		Access:	R/W
		For Future Use. This bit is self clear.	
	4	Context Load Protocol Register - BCS 4	
		Default Value:	0b
		Access:	R/W
		For Future Use. This bit is self clear.	

BLT_CTX_LD_PRTCL - Context Load Protocol Register BLT

	3	Context Load Protocol Register - BCS 3						
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Bit 3 = Context Complete. Only valid with Bit 2 asserted and indicates whether the context switching out as complete vs. incomplete. This bit is self clear.</p>	Default Value:	0b	Project:	BDW	Access:	R/W
Default Value:	0b							
Project:	BDW							
Access:	R/W							
	2	Context Load Protocol Register - BCS 2						
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Context Load Protocol Register (Written by BCS) Bit 2 = Request from BCS to GAM for context save readiness. GAM will acknowledge appropriated steps taken. This bit is self clear.</p>	Default Value:	0b	Access:	R/W		
Default Value:	0b							
Access:	R/W							
	1	Context Load Protocol Register - BCS 1						
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Context Load Protocol Register (Written by BCS) Bit 1 = Context Launched. This bit is self clear.</p>	Default Value:	0b	Access:	R/W		
Default Value:	0b							
Access:	R/W							
	0	Context Load Protocol Register - BCS 0						
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Context Load Protocol Register (Written by BCS) Bit 0 = Context Available. This bit is self clear.</p>	Default Value:	0b	Access:	R/W		
Default Value:	0b							
Access:	R/W							

Context Load Protocol Register CS

GFX_CTX_LD_PRTCL - Context Load Protocol Register CS						
DWord	Bit	Description				
0	31:16	Mask Bits <table border="1"> <tr> <td>Default Value:</td> <td>0000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Default Value:	0000h	Access:	RO
Default Value:	0000h					
Access:	RO					
	15	Context Load Protocol Register - CS 15 <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>For Future Use. This bit is self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
	14	Context Load Protocol Register - CS 14 <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>For Future Use. This bit is self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
	13	Context Load Protocol Register - CS 13 <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>For Future Use. This bit is self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
	12	Context Load Protocol Register - CS 12 <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>For Future Use. This bit is self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					

GFX_CTX_LD_PRTCL - Context Load Protocol Register CS

	11	Context Load Protocol Register - CS 11	
		Default Value:	0b
		Access:	R/W
		For Future Use. This bit is self clear.	
	10	Context Load Protocol Register - CS 10	
		Default Value:	0b
		Access:	R/W
		For Future Use. This bit is self clear.	
	9	Context Load Protocol Register - CS 9	
		Default Value:	0b
		Access:	R/W
		For Future Use. This bit is self clear.	
	8	Context Load Protocol Register - CS 8	
		Default Value:	0b
		Access:	R/W
		For Future Use. This bit is self clear.	
	7	Context Load Protocol Register - CS 7	
		Default Value:	0b
		Access:	R/W
		For Future Use. This bit is self clear.	
	6	Context Load Protocol Register - CS 6	
		Default Value:	0b
		Access:	R/W
		For Future Use. This bit is self clear.	
	5	Context Load Protocol Register - CS 5	
		Default Value:	0b
		Access:	R/W
		For Future Use. This bit is self clear.	

GFX_CTX_LD_PRTCL - Context Load Protocol Register CS

	4	Context Load Protocol Register - CS 4						
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>For Future Use. This bit is self clear.</p>	Default Value:	0b	Access:	R/W		
Default Value:	0b							
Access:	R/W							
	3	Context Load Protocol Register - CS 3						
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Bit 3 = Context Complete. Only valid with Bit 2 asserted and indicates whether the context switching out as complete vs. incomplete. This bit is self clear.</p>	Default Value:	0b	Project:	BDW	Access:	R/W
Default Value:	0b							
Project:	BDW							
Access:	R/W							
	2	Context Load Protocol Register - CS 2						
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Context Load Protocol Register (Written by CS) Bit 2 = Request from CS to GAM for context save readiness. GAM will acknowledge appropriated steps taken. This bit is self clear.</p>	Default Value:	0b	Access:	R/W		
Default Value:	0b							
Access:	R/W							
	1	Context Load Protocol Register - CS 1						
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Context Load Protocol Register (Written by CS) Bit 1 = Context Launched. This bit is self clear.</p>	Default Value:	0b	Access:	R/W		
Default Value:	0b							
Access:	R/W							
	0	Context Load Protocol Register - CS 0						
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Context Load Protocol Register (Written by CS) Bit 0 = Context Available. This bit is self clear.</p>	Default Value:	0b	Access:	R/W		
Default Value:	0b							
Access:	R/W							

Context Load Protocol Register VCS0

MFX0_CTX_LD_PRTCL - Context Load Protocol Register VCS0						
DWord	Bit	Description				
0	31:16	<p>Mask Bits</p> <table border="1"> <tr> <td>Default Value:</td> <td>0000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Default Value:	0000h	Access:	RO
Default Value:	0000h					
Access:	RO					
	15	<p>Context Load Protocol Register - VCS0 15</p> <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>For Future Use. This bit is self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
	14	<p>Context Load Protocol Register - VCS0 14</p> <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>For Future Use. This bit is self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
	13	<p>Context Load Protocol Register - VCS0 13</p> <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>For Future Use. This bit is self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
	12	<p>Context Load Protocol Register - VCS0 12</p> <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>For Future Use. This bit is self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					

MFX0_CTX_LD_PRTCL - Context Load Protocol Register VCS0

	11	Context Load Protocol Register - VCS0 11	
		Default Value:	0b
		Access:	R/W
		For Future Use. This bit is self clear.	
	10	Context Load Protocol Register - VCS0 10	
		Default Value:	0b
		Access:	R/W
		For Future Use. This bit is self clear.	
	9	Context Load Protocol Register - VCS0 9	
		Default Value:	0b
		Access:	R/W
		For Future Use. This bit is self clear.	
	8	Context Load Protocol Register - VCS0 8	
		Default Value:	0b
		Access:	R/W
		For Future Use. This bit is self clear.	
	7	Context Load Protocol Register - VCS0 7	
		Default Value:	0b
		Access:	R/W
		For Future Use. This bit is self clear.	
	6	Context Load Protocol Register - VCS0 6	
		Default Value:	0b
		Access:	R/W
		For Future Use. This bit is self clear.	
	5	Context Load Protocol Register - VCS0 5	
		Default Value:	0b
		Access:	R/W
		For Future Use. This bit is self clear.	

MFX0_CTX_LD_PRTCL - Context Load Protocol Register VCS0

	4	Context Load Protocol Register - VCS0 4						
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>For Future Use. This bit is self clear.</p>	Default Value:	0b	Access:	R/W		
Default Value:	0b							
Access:	R/W							
	3	Context Load Protocol Register - VCS0 3						
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Bit 3 = Context Complete. Only valid with Bit 2 asserted and indicates whether the context switching out as complete vs. incomplete. This bit is self clear.</p>	Default Value:	0b	Project:	BDW	Access:	R/W
Default Value:	0b							
Project:	BDW							
Access:	R/W							
	2	Context Load Protocol Register - VCS0 2						
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Context Load Protocol Register (Written by VCS0) Bit 2 = Request from VCS0 to GAM for context save readiness. GAM will acknowledge appropriated steps taken. This bit is self clear.</p>	Default Value:	0b	Access:	R/W		
Default Value:	0b							
Access:	R/W							
	1	Context Load Protocol Register - VCS0 1						
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Context Load Protocol Register (Written by VCS0) Bit 1 = Context Launched. This bit is self clear.</p>	Default Value:	0b	Access:	R/W		
Default Value:	0b							
Access:	R/W							
	0	Context Load Protocol Register - VCS0 0						
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Context Load Protocol Register (Written by VCS0) Bit 0 = Context Available. This bit is self clear.</p>	Default Value:	0b	Access:	R/W		
Default Value:	0b							
Access:	R/W							

Context Load Protocol Register VCS1

MFX1_CTX_LD_PRTCL - Context Load Protocol Register VCS1						
DWord	Bit	Description				
0	31:16	Mask Bits <table border="1"> <tr> <td>Default Value:</td> <td>0000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Default Value:	0000h	Access:	RO
Default Value:	0000h					
Access:	RO					
	15	Context Load Protocol Register - VCS1 15 <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>For Future Use. This bit is self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
	14	Context Load Protocol Register - VCS1 14 <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>For Future Use. This bit is self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
	13	Context Load Protocol Register - VCS1 13 <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>For Future Use. This bit is self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
	12	Context Load Protocol Register - VCS1 12 <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>For Future Use. This bit is self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					

MFX1_CTX_LD_PRTCL - Context Load Protocol Register VCS1

	11	Context Load Protocol Register - VCS1 11	
		Default Value:	0b
		Access:	R/W
		For Future Use. This bit is self clear.	
	10	Context Load Protocol Register - VCS1 10	
		Default Value:	0b
		Access:	R/W
		For Future Use. This bit is self clear.	
	9	Context Load Protocol Register - VCS1 9	
		Default Value:	0b
		Access:	R/W
		For Future Use. This bit is self clear.	
	8	Context Load Protocol Register - VCS1 8	
		Default Value:	0b
		Access:	R/W
		For Future Use. This bit is self clear.	
	7	Context Load Protocol Register - VCS1 7	
		Default Value:	0b
		Access:	R/W
		For Future Use. This bit is self clear.	
	6	Context Load Protocol Register - VCS1 6	
		Default Value:	0b
		Access:	R/W
		For Future Use. This bit is self clear.	
	5	Context Load Protocol Register - VCS1 5	
		Default Value:	0b
		Access:	R/W
		For Future Use. This bit is self clear.	

MFX1_CTX_LD_PRTCL - Context Load Protocol Register VCS1

	4	Context Load Protocol Register - VCS1 4						
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>For Future Use. This bit is self clear.</p>	Default Value:	0b	Access:	R/W		
Default Value:	0b							
Access:	R/W							
	3	Context Load Protocol Register - VCS1 3						
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Bit 3 = Context Complete. Only valid with Bit 2 asserted and indicates whether the context switching out as complete vs. incomplete. This bit is self clear.</p>	Default Value:	0b	Project:	BDW	Access:	R/W
Default Value:	0b							
Project:	BDW							
Access:	R/W							
	2	Context Load Protocol Register - VCS1 2						
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Context Load Protocol Register (Written by VCS1) Bit 2 = Request from VCS1 to GAM for context save readiness. GAM will acknowledge appropriated steps taken. This bit is self clear.</p>	Default Value:	0b	Access:	R/W		
Default Value:	0b							
Access:	R/W							
	1	Context Load Protocol Register - VCS1 1						
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Context Load Protocol Register (Written by VCS1) Bit 1 = Context Launched This bit is self clear.</p>	Default Value:	0b	Access:	R/W		
Default Value:	0b							
Access:	R/W							
	0	Context Load Protocol Register - VCS1 0						
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Context Load Protocol Register (Written by VCS1) Bit 0 = Context Available. This bit is self clear.</p>	Default Value:	0b	Access:	R/W		
Default Value:	0b							
Access:	R/W							

Context Load Protocol Register VEBX

VEBX_CTX_LD_PRTCL - Context Load Protocol Register VEBX						
DWord	Bit	Description				
0	31:16	<p>Mask Bits</p> <table border="1"> <tr> <td>Default Value:</td> <td>0000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Default Value:	0000h	Access:	RO
Default Value:	0000h					
Access:	RO					
	15	<p>Context Load Protocol Register - VEBX 15</p> <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>For Future Use. This bit is self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
	14	<p>Context Load Protocol Register - VEBX 14</p> <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>For Future Use. This bit is self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
	13	<p>Context Load Protocol Register - VEBX 13</p> <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>For Future Use. This bit is self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
	12	<p>Context Load Protocol Register - VEBX 12</p> <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>For Future Use. This bit is self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					

VEBX_CTX_LD_PRTCL - Context Load Protocol Register VEBX

	11	Context Load Protocol Register - VEBX 11		
		Default Value:	0b	
		Access:	R/W	
		For Future Use. This bit is self clear.		
	10	Context Load Protocol Register - VEBX 10		
		Default Value:	0b	
		Access:	R/W	
		For Future Use. This bit is self clear.		
	9	Context Load Protocol Register - VEBX 9		
		Default Value:	0b	
		Access:	R/W	
		For Future Use. This bit is self clear.		
	8	Context Load Protocol Register - VEBX 8		
		Default Value:	0b	
		Access:	R/W	
		For Future Use. This bit is self clear.		
	7	Context Load Protocol Register - VEBX 7		
		Default Value:	0b	
		Access:	R/W	
		For Future Use. This bit is self clear.		
	6	Context Load Protocol Register - VEBX 6		
		Default Value:	0b	
		Access:	R/W	
		For Future Use. This bit is self clear.		
	5	Context Load Protocol Register - VEBX 5		
		Default Value:	0b	
		Access:	R/W	
		For Future Use. This bit is self clear.		

VEBX_CTX_LD_PRTCL - Context Load Protocol Register VEBX

	4	Context Load Protocol Register - VEBX 4						
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>For Future Use. This bit is self clear.</p>	Default Value:	0b	Access:	R/W		
Default Value:	0b							
Access:	R/W							
	3	Context Load Protocol Register - VEBX 3						
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Bit 3 = Context Complete. Only valid with Bit 2 asserted and indicates whether the context switching out as complete vs. incomplete. This bit is self clear.</p>	Default Value:	0b	Project:	BDW	Access:	R/W
Default Value:	0b							
Project:	BDW							
Access:	R/W							
	2	Context Load Protocol Register - VEBX 2						
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Context Load Protocol Register (Written by VEBX) Bit 2 = Request from VEBX to GAM for context save readiness. GAM will acknowledge appropriated steps taken. This bit is self clear.</p>	Default Value:	0b	Access:	R/W		
Default Value:	0b							
Access:	R/W							
	1	Context Load Protocol Register - VEBX 1						
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Context Load Protocol Register (Written by VEBX) Bit 1 = Context Launched. This bit is self clear.</p>	Default Value:	0b	Access:	R/W		
Default Value:	0b							
Access:	R/W							
	0	Context Load Protocol Register - VEBX 0						
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Context Load Protocol Register (Written by VEBX) Bit 0 = Context Available. This bit is self clear.</p>	Default Value:	0b	Access:	R/W		
Default Value:	0b							
Access:	R/W							

Context Restore Request To TDL

TDL_CONTEXT_RESTORE - Context Restore Request To TDL			
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x00000000 Access: WO Size (in bits): 32			
Address: 0E440h Valid Projects: [BDW]			
DWord	Bit	Description	
0	31:17	Reserved	
		Format:	MBZ
	16	Context Restore Mask	
		Value	Name
		1	Bit 0 and bit 16 both need to be 1 for Context restore request
0	15:1	Reserved	
		Format:	MBZ
0	0	Context Restore	
		Value	Name
		1	Bit 0 and bit 16 both need to be 1 for Context restore request

Context Save Request To TDL

TDL_CONTEXT_SAVE - Context Save Request To TDL								
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x00000000 Access: WO Size (in bits): 32								
Address: 0E4FCh Valid Projects: [BDW]								
DWord	Bit	Description						
0	31:17	Reserved						
		Format:	MBZ					
	16	Context Save Mask						
		<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="background-color: #d9e1f2;">Value</th><th style="background-color: #d9e1f2;">Name</th><th style="background-color: #d9e1f2;">Description</th></tr> </thead> <tbody> <tr> <td>1</td><td></td><td>Bit 0 and Bit 16 both need to be '1' for Context Save Request</td></tr> </tbody> </table>		Value	Name	Description	1	
Value	Name	Description						
1		Bit 0 and Bit 16 both need to be '1' for Context Save Request						
	15:1	Reserved						
		Format:	MBZ					
	0	Context Save						
		<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="background-color: #d9e1f2;">Value</th><th style="background-color: #d9e1f2;">Name</th><th style="background-color: #d9e1f2;">Description</th></tr> </thead> <tbody> <tr> <td>1</td><td></td><td>Bit 0 and Bit 16 both need to be '1' for Context Save Request</td></tr> </tbody> </table>		Value	Name	Description	1	
Value	Name	Description						
1		Bit 0 and Bit 16 both need to be '1' for Context Save Request						

Context Sizes

CXT_SIZE - Context Sizes			
Register Space: MMIO: 0/2/0 Project: BDW Source: RenderCS Default Value: 0x05655582 Access: R/W Size (in bits): 32 Trusted Type: 1			
Address: 021A8h			
The actual size of a logical rendering context is the amount of data stored/restored during a context switch and is measured in 64B cache lines.			
This register will be power context save/restored. Note that this register will default to the correct value, so software should not have to modify it.			
DWord	Bit	Description	
0	31:27	Reserved	Format: MBZ
	26:24	Ring Context Size	Default Value: 5h This field indicates the Ring context data that needs to be save/restored.
	23:16	Render Context Size	Default Value: 65h This field indicates the size of the render context data that needs to be save/restored when extended mode is not enabled for a context; this also excludes VF, VFE, and URB context size.
	15:8	SOL Context Offset	Default Value: 55h This field indicates the cacheline aligned offset of the SOL context in the render context image starting from Ring Context. Note that in exelist of scheduling Ring context itself is at 4KB offset from LRCA.
	7:0	VF and VFE State Context Size	Default Value: 82h This field indicates the amount of VF and VFE unit data context save/restored in cachelines.

Context Status Buffer Contents

CTXT_ST_BUF - Context Status Buffer Contents				
Register Space:	MMIO	0/2/0		
Project:	BDW			
Default Value:	0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000			
Access:	R/W			
Size (in bits):	384			
Trusted Type:	1			
Address:	02370h-0239Fh			
Name:	Context Status Buffer Contents			
ShortName:	CTXT_ST_BUF_RCSUNIT			
Address:	12370h-1239Fh			
Name:	Context Status Buffer Contents			
ShortName:	CTXT_ST_BUF_VCSUNIT0			
Address:	1A370h-1A39Fh			
Name:	Context Status Buffer Contents			
ShortName:	CTXT_ST_BUF_VECSUNIT			
Address:	1C370h-1C39Fh			
Name:	Context Status Buffer Contents			
ShortName:	CTXT_ST_BUF_VCSUNIT1			
Address:	22370h-2239Fh			
Name:	Context Status Buffer Contents			
ShortName:	CTXT_ST_BUF_BCSUNIT			
Contents of the ExecList 0 in HW.				
Programming Notes				
This structure contains the Context Switch status locations Context Status 0 to Context Status 5.				
DWord	Bit	Description		
0	63:32	Context Status 0 UDW		
	Format:	Context Status		
1	31:0	Context Status 0 LDW		
	Format:	Context Status		
1	63:32	Context Status 1 UDW		
	Format:	Context Status		
1	31:0	Context Status 1 LDW		
	Format:	Context Status		

CTXT_ST_BUF - Context Status Buffer Contents		
2	63:32	Context Status 2 UDW Format: Context Status
	31:0	Context Status 2 LDW Format: Context Status
3	63:32	Context Status 3 UDW Format: Context Status
	31:0	Context Status 3 LDW Format: Context Status
4	63:32	Context Status 4 UDW Format: Context Status
	31:0	Context Status 4 LDW Format: Context Status
5	63:32	Context Status 5 UDW Format: Context Status
	31:0	Context Status 5 LDW Format: Context Status

CORB (Command Output Ring Buffer)- Lower Base Address

CORBLBASE - CORB (Command Output Ring Buffer)- Lower Base Address								
Register Space:	MMIO: 0/3/0							
Project:	BDW							
Default Value:	0x00000000							
Access:	R/W							
Size (in bits):	32							
Address:	00040h-00043h							
DWord	Bit	Description						
0	31:7	CORBLBASE						
		<table border="1"> <tr> <td>Default Value:</td> <td>0h</td> </tr> <tr> <td colspan="2">Lower address of the Command Output Ring Buffer, allowing the CORB Base Address to be assigned on any 128-B boundary.</td></tr> <tr> <td colspan="2" style="text-align: center;">Programming Notes</td></tr> <tr> <td colspan="2">This field must not be written when the DMA engine is running or the DMA transfer may be corrupted.</td></tr> </table>	Default Value:	0h	Lower address of the Command Output Ring Buffer, allowing the CORB Base Address to be assigned on any 128-B boundary.		Programming Notes	
Default Value:	0h							
Lower address of the Command Output Ring Buffer, allowing the CORB Base Address to be assigned on any 128-B boundary.								
Programming Notes								
This field must not be written when the DMA engine is running or the DMA transfer may be corrupted.								
	6:0	CORBLBASE LOWER BITS						
		<table border="1"> <tr> <td>Default Value:</td> <td>0h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td colspan="2">CORB Lower Base Unimplemented Bits: Hardwired to 0. This requires the CORB to be allocated with 128-byte granularity to allow for cache line fetch optimizations.</td></tr> </table>	Default Value:	0h	Access:	RO	CORB Lower Base Unimplemented Bits: Hardwired to 0. This requires the CORB to be allocated with 128-byte granularity to allow for cache line fetch optimizations.	
Default Value:	0h							
Access:	RO							
CORB Lower Base Unimplemented Bits: Hardwired to 0. This requires the CORB to be allocated with 128-byte granularity to allow for cache line fetch optimizations.								

CORB (Command Output Ring Buffer)- Upper Base Address

CORBUBASE - CORB (Command Output Ring Buffer)- Upper BaseAddress		
Register Space: MMIO: 0/3/0 Project: BDW Default Value: 0x00000000 Access: R/W Size (in bits): 32		
Address: 00044h-00047h		
DWord	Bit	Description
0	31:0	CORBUBASE Upper 32 bits of address of the Command Output Ring Buffer. <div style="border: 1px solid #ccc; padding: 2px;"> Programming Notes This register field must not be written when the DMA engine is running or the DMA transfer may be corrupted. </div>

CORB Control_Status_Size

CORBCTL_STS_SIZE - CORB Control_Status_Size					
DWord	Bit	Description			
0	31:24	Reserved <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ	
Format:	MBZ				
23:20	CORB Size Capability <table border="1"> <tr> <td>Default Value:</td> <td>4h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Programming Notes</p> <p>The default value, 0100b, indicates that the PCH only supports a CORB size of 256 CORB entries (1024B).</p>	Default Value:	4h	Access:	RO
Default Value:	4h				
Access:	RO				
19:18	Reserved <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ		
Format:	MBZ				
17:16	CORB SIZE <table border="1"> <tr> <td>Default Value:</td> <td>10b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Programming Notes</p> <p>The default value, 0100b, indicates that the PCH only supports a CORB size of 256 CORB entries (1024B).</p>	Default Value:	10b	Access:	RO
Default Value:	10b				
Access:	RO				
15:9	Reserved <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ		
Format:	MBZ				
8	CMEI <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> </table> <p>Programming Notes</p> <p>Memory Error (CMEI): Hardwired to '0' as memory errors are not tracked.</p>	Default Value:	0b		
Default Value:	0b				
7:2	Reserved <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ		
Format:	MBZ				

CORBCTL_STS_SIZE - CORB Control_Status_Size

	1	Enable CORB DMA Engine											
		Access:		R/W Variant									
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>DMA Stop</td> <td>See ProgramminNotes</td> </tr> <tr> <td>1b</td> <td>DMA Run</td> <td>See ProgramminNotes</td> </tr> </tbody> </table>		Value	Name	Description	0b	DMA Stop	See ProgramminNotes	1b	DMA Run	See ProgramminNotes	
Value	Name	Description											
0b	DMA Stop	See ProgramminNotes											
1b	DMA Run	See ProgramminNotes											
		Programming Notes											
		After SW writes a 0 to this bit, the HW may not stop immediately. The hardware will physically update the bit to a 0 when the DMA engine is truly stopped. SW must read a 0 from this bit to verify that the DMA is truly stopped.											
	0	Memory Error Interrupt Enable											
		Access:		R/W									
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disable [Default]</td> <td>Disable MEI</td> </tr> <tr> <td>1b</td> <td>Enable</td> <td>Enable MEI</td> </tr> </tbody> </table>		Value	Name	Description	0b	Disable [Default]	Disable MEI	1b	Enable	Enable MEI	
Value	Name	Description											
0b	Disable [Default]	Disable MEI											
1b	Enable	Enable MEI											
		Programming Notes											
		The access to this bit field is RW but no functionality as memory errors are not tracked.											

CORB Read/Write Pointers

CORBRWP - CORB Read/Write Pointers													
Register Space: MMIO: 0/3/0 Project: BDW Default Value: 0x00000000 Access: R/W Size (in bits): 32													
DWord	Bit	Description											
0	31	<p>CORB Read Pointer Reset</p> <table border="1"> <tr> <td>Access:</td> <td>R/W Variant</td> </tr> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> <tr> <td>0b</td> <td>Clear_Reset [Default]</td> <td>See ProgrammingNotes</td> </tr> <tr> <td>1b</td> <td>Set_Reset</td> <td>See ProgrammingNotes</td> </tr> </table> <p>Programming Notes</p> <p>Software writes a 1 to this bit to reset the CORB Read Pointer to 0 and clear any residual pre-fetched commands in the CORB hardware buffer within the Intel Audio controller. The hardware will physically update this bit to 1 when the CORB Pointer reset is complete. Software must read a 1 to verify that the reset completed correctly. Software must clear this bit back to 0 and read back the 0 to verify that the clear completed correctly. The CORB DMA engine must be stopped prior to resetting the Read Pointer or else DMA transfer may be corrupted.</p>	Access:	R/W Variant	Value	Name	Description	0b	Clear_Reset [Default]	See ProgrammingNotes	1b	Set_Reset	See ProgrammingNotes
Access:	R/W Variant												
Value	Name	Description											
0b	Clear_Reset [Default]	See ProgrammingNotes											
1b	Set_Reset	See ProgrammingNotes											
30:24		<p>Reserved</p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ									
Format:	MBZ												
23:16		<p>CORB Read Pointer</p> <table border="1"> <tr> <td>Default Value:</td> <td>00h</td> </tr> <tr> <td>Access:</td> <td>RO Variant</td> </tr> </table> <p>Programming Notes</p> <p>Software reads this field to determine how many commands it can write to the CORB without over-running. The value read indicates the CORB Read Pointer offset in Dword granularity. The offset entry read from this field has been successfully fetched by the DMA controller and may be over-written by software. Supports 256 CORB entries (256 x 4B=1KB). This field may be read while the DMA engine is running.</p>	Default Value:	00h	Access:	RO Variant							
Default Value:	00h												
Access:	RO Variant												
15:8		<p>Reserved</p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ									
Format:	MBZ												

CORBRWP - CORB Read/Write Pointers

CORB Write Pointer	
Default Value:	00h
Access:	R/W
Programming Notes	
Software writes the last valid CORB entry offset into this field in Dword granularity. The DMA engine fetches commands from the CORB until the Read Pointer matches the Write Pointer. Supports 256 CORB entries (256 x 4B=1KB). This field may be written while the DMA engine is running.	

Count Active Channels Dispatched

TS_GPGPU_THREADS_DISPATCHED - Count Active Channels Dispatched						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Source:	RenderCS					
Default Value:	0x00000000, 0x00000000					
Access:	R/W					
Size (in bits):	64					
Trusted Type:	1					
Address:	02290h					
<p>This register is used to count the number of active channels that TS sends for dispatch. For each dispatch the active bits in the execution mask are summed and added to this register. This register is reset when a write occurs to 2290h</p>						
DWord	Bit	Description				
0	63:32	GPGPU_THREADS_DISPATCHED UDW <table border="1"> <tr> <td>Format:</td><td>U32</td></tr> <tr> <td colspan="2">This count is increased by the number of active bits in the execution mask each time the TS sends a GPGPU dispatch.</td></tr> </table>	Format:	U32	This count is increased by the number of active bits in the execution mask each time the TS sends a GPGPU dispatch.	
Format:	U32					
This count is increased by the number of active bits in the execution mask each time the TS sends a GPGPU dispatch.						
31:0	GPGPU_THREADS_DISPATCHED LDW <table border="1"> <tr> <td>Format:</td><td>U32</td></tr> <tr> <td colspan="2">This count is increased by the number of active bits in the execution mask each time the TS sends a GPGPU dispatch.</td></tr> </table>	Format:	U32	This count is increased by the number of active bits in the execution mask each time the TS sends a GPGPU dispatch.		
Format:	U32					
This count is increased by the number of active bits in the execution mask each time the TS sends a GPGPU dispatch.						

CSC_COEFF

CSC_COEFF			
Register Space:	MMIO: 0/2/0		
Project:	BDW		
Default Value:	0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000		
Access:	Double Buffered		
Size (in bits):	192		
Double Buffer	Start of vertical blank after armed		
Update Point:			
Double Buffer Armed Write to CSC_MODE			
By:			
Address:	49010h-49027h		
Name:	Pipe A CSC Coefficients		
ShortName:	CSC_COEFF_A_*		
Valid Projects:	BDW		
Power:	Always on		
Reset:	soft		
Address:	49110h-49127h		
Name:	Pipe B CSC Coefficients		
ShortName:	CSC_COEFF_B_*		
Valid Projects:	BDW		
Power:	off/on		
Reset:	soft		
Address:	49210h-49227h		
Name:	Pipe C CSC Coefficients		
ShortName:	CSC_COEFF_C_*		
Valid Projects:	BDW		
Power:	off/on		
Reset:	soft		
DWord	Bit	Description	
0	31:16	RY Format: CSC COEFFICIENT FORMAT	
	15:0	GY Format: CSC COEFFICIENT FORMAT	
1	31:16	BY Format: CSC COEFFICIENT FORMAT	

CSC_COEFF			
	15:0	Reserved	
2	31:16	RU	
	15:0	GU	
3	31:16	BU	
	15:0	Reserved	
4	31:16	RV	
	15:0	GV	
5	31:16	BV	
	15:0	Reserved	

Format: MBZ

Format: **CSC COEFFICIENT FORMAT**

Format: **CSC COEFFICIENT FORMAT**

Format: **CSC COEFFICIENT FORMAT**

Format: MBZ

Format: **CSC COEFFICIENT FORMAT**

Format: **CSC COEFFICIENT FORMAT**

Format: MBZ

CSC_MODE

CSC_MODE				
Register Space:	MMIO: 0/2/0			
Project:	BDW			
Default Value:	0x00000000			
Access:	Double Buffered			
Size (in bits):	32			
Double Buffer Update Point:	Start of vertical blank			
Address:	49028h-4902Bh			
Name:	Pipe A CSC Mode			
ShortName:	CSC_MODE_A			
Valid Projects:	BDW			
Power:	Always on			
Reset:	soft			
Address:	49128h-4912Bh			
Name:	Pipe B CSC Mode			
ShortName:	CSC_MODE_B			
Valid Projects:	BDW			
Power:	off/on			
Reset:	soft			
Address:	49228h-4922Bh			
Name:	Pipe C CSC Mode			
ShortName:	CSC_MODE_C			
Valid Projects:	BDW			
Power:	off/on			
Reset:	soft			
Description				
Writes to this register arm CSC registers for this pipe.				
DWord	Bit	Description		
0	31:2	Reserved		

CSC_MODE		
1	CSC Position	
	Project:	BDW
Selects the CSC position in the pipe. This is ignored when split gamma mode is selected in the pipe config register.		
	Value	Name
	0b	CSC After
0	1b	CSC Before
	Reserved	
0	Format:	MBZ

CSC_POSTOFF

CSC_POSTOFF				
Register Space:	MMIO: 0/2/0			
Project:	BDW			
Default Value:	0x00000000, 0x00000000, 0x00000000			
Access:	Double Buffered			
Size (in bits):	96			
Double Buffer	Start of vertical blank after armed			
Update Point:				
Double Buffer Armed Write to CSC_MODE				
By:				
Address:	49040h-4904Bh			
Name:	Pipe A CSC Post-Offsets			
ShortName:	CSC_POSTOFF_A_*			
Valid Projects:	BDW			
Power:	Always on			
Reset:	soft			
Address:	49140h-4914Bh			
Name:	Pipe B CSC Post-Offsets			
ShortName:	CSC_POSTOFF_B_*			
Valid Projects:	BDW			
Power:	off/on			
Reset:	soft			
Address:	49240h-4924Bh			
Name:	Pipe C CSC Post-Offsets			
ShortName:	CSC_POSTOFF_C_*			
Valid Projects:	BDW			
Power:	off/on			
Reset:	soft			
The post-offset is intended to add an offset from 0 on the Y or RGB channels and to convert UV channels from 2's complement to excess 0.5 as they exit pipe color space conversion (CSC).				
DWord	Bit	Description		
0	31:13	Reserved <table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ
	Format:	MBZ		
12:0	PostCSC High Offset This value is used to give an offset to the high color channel as it exits CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).			

CSC_POSTOFF			
1	31:13	Reserved	Format: MBZ
	12:0	PostCSC Medium Offset This value is used to give an offset to the medium color channel as it exits CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).	
2	31:13	Reserved	Format: MBZ
	12:0	PostCSC Low Offset This value is used to give an offset to the low color channel as it exits CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).	

CSC_PREOFF

CSC_PREOFF		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000, 0x00000000, 0x00000000	
Access:	Double Buffered	
Size (in bits):	96	
Double Buffer	Start of vertical blank after armed	
Update Point:		
Double Buffer Armed Write to CSC_MODE		
By:		
Address:	49030h-4903Bh	
Name:	Pipe A CSC Pre-Offsets	
ShortName:	CSC_PREOFF_A_*	
Valid Projects:	BDW	
Power:	Always on	
Reset:	soft	
Address:	49130h-4913Bh	
Name:	Pipe B CSC Pre-Offsets	
ShortName:	CSC_PREOFF_B_*	
Valid Projects:	BDW	
Power:	off/on	
Reset:	soft	
Address:	49230h-4923Bh	
Name:	Pipe C CSC Pre-Offsets	
ShortName:	CSC_PREOFF_C_*	
Valid Projects:	BDW	
Power:	off/on	
Reset:	soft	
The pre-offset is intended to remove an offset from 0 on the Y or RGB channels and to convert UV channels from excess 0.5 to 2's complement as they enter pipe color space conversion (CSC).		
DWord	Bit	Description
0	31:13	Reserved
		Format: MBZ
	12:0	PreCSC High Offset This value is used to give an offset to the high color channel as it enters CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).

CSC_PREOFF			
1	31:13	Reserved	Format: MBZ
	12:0	PreCSC Medium Offset This value is used to give an offset to the medium color channel as it enters CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).	
2	31:13	Reserved	Format: MBZ
	12:0	PreCSC Low Offset This value is used to give an offset to the low color channel as it enters CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).	

CS Context Timestamp Count

CS_CTX_TIMESTAMP - CS Context Timestamp Count						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Source:	RenderCS					
Default Value:	0x00000000					
Access:	R/W					
Size (in bits):	32					
Address:	023A8h					
<p>This register provides a mechanism to obtain cumulative run time of a GPU context on HW. This register gets context save/restored on a context switch. SW must reset this register on very first submission of a context to HW, then afterwards gets context save/restored maintaining the cumulative run time of the corresponding context. This register (effectively) counts at a constant frequency by adjusting the increment amount according to the actual reference clock frequency. SW therefore does not need to know the reference clock frequency. This register gets reset on an engine reset.</p> <p>This register is context save restore on a context switch. The time to execute the context switch is included in the CS_CTX_TIMESTAMP register.</p>						
DWord	Bit	Description				
0	31:0	<p>Timestamp Value</p> <table border="1"> <tr> <td>Format:</td><td>U32</td></tr> <tr> <td colspan="2">This register increments for every 80 ns of time.</td></tr> </table>	Format:	U32	This register increments for every 80 ns of time.	
Format:	U32					
This register increments for every 80 ns of time.						

CS General Purpose Register

CS_GPR - CS General Purpose Register	
Register Space:	MMIO: 0/2/0
Project:	BDW
Source:	RenderCS
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Address:	02600h
Name:	CS General Purpose Register 0
ShortName:	CS_GPR_R_0
Address:	02608h
Name:	CS General Purpose Register 1
ShortName:	CS_GPR_R_1
Address:	02610h
Name:	CS General Purpose Register 2
ShortName:	CS_GPR_R_2
Address:	02618h
Name:	CS General Purpose Register 3
ShortName:	CS_GPR_R_3
Address:	02620h
Name:	CS General Purpose Register 4
ShortName:	CS_GPR_R_4
Address:	02628h
Name:	CS General Purpose Register 5
ShortName:	CS_GPR_R_5
Address:	02630h
Name:	CS General Purpose Register 6
ShortName:	CS_GPR_R_6
Address:	02638h
Name:	CS General Purpose Register 7
ShortName:	CS_GPR_R_7
Address:	02640h
Name:	CS General Purpose Register 8
ShortName:	CS_GPR_R_8
Address:	02648h

CS_GPR - CS General Purpose Register

Name: CS General Purpose Register 9
 ShortName: CS_GPR_R_9

Address: 02650h
 Name: CS General Purpose Register 10
 ShortName: CS_GPR_R_10

Address: 02658h
 Name: CS General Purpose Register 11
 ShortName: CS_GPR_R_11

Address: 02660h
 Name: CS General Purpose Register 12
 ShortName: CS_GPR_R_12

Address: 02668h
 Name: CS General Purpose Register 13
 ShortName: CS_GPR_R_13

Address: 02670h
 Name: CS General Purpose Register 14
 ShortName: CS_GPR_R_14

Address: 02678h
 Name: CS General Purpose Register 15
 ShortName: CS_GPR_R_15

This is a General Purpose Register bank of sixteen 64bit registers, which will be used as temporary storage by MI_MATH command to do ALU operations.

GPR Index	MMIO Offset
R_0	0x2600
R_1	0x2608
R_2	0x2610
R_3	0x2618
R_4	0x2620
R_5	0x2628
R_6	0x2630
R_7	0x2638
R_8	0x2640
R_9	0x2648
R_10	0x2650
R_11	0x2658
R_12	0x2660

CS_GPR - CS General Purpose Register

R_13	0x2668			
R_14	0x2670			
R_15	0x2678			
DWord	Bit	Description		
0	63:0	<p>CS_GPR_DATA</p> <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> </table> <p>This register is a temporary register for ALU operations. See MI_MATH command for more details.</p>	Project:	BDW
Project:	BDW			

CSPREEMPT

CSPREEMPT - CSPREEMPT						
Register Space: MMIO: 0/2/0 Project: BDW Source: RenderCS Default Value: 0x00000000 Access: R/W Size (in bits): 32 Trusted Type: 1 Address: 024B0h						
Programming Notes						
This is for HW internal usage and must not be written by SW.						
DWord	Bit	Description				
0	31:16	Mask Bits <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Project:</td><td style="width: 50%;">BDW</td></tr> <tr> <td>Format:</td><td>Mask[15:0]</td></tr> </table> <p>Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)</p>	Project:	BDW	Format:	Mask[15:0]
	Project:	BDW				
	Format:	Mask[15:0]				
15:1	Reserved <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Project:</td><td style="width: 50%;">BDW</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	BDW	Format:	MBZ	
Project:	BDW					
Format:	MBZ					
0	Unnamed <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Project:</td><td style="width: 50%;">BDW</td></tr> <tr> <td>Format:</td><td>Disable</td></tr> </table> <p>This is a message bit written by the cross CS in case of GT4-CBR/SFR mode of operation. To set this bit both bit[0] and bit[16] (mask) needs to be set. This bit set indicates CS in other GT has reached a preemption point. This bit gets reset by CS when preemption takes place.</p>	Project:	BDW	Format:	Disable	
Project:	BDW					
Format:	Disable					

CS Reset Control Register

CS_RESET_CTRL - CS Reset Control Register				
DWord	Bit	Description		
0	31:16	<p>Mask Bits</p> <table border="1"> <tr> <td>Format:</td> <td>Mask[15:0]</td> </tr> </table> <p>Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)</p>	Format:	Mask[15:0]
Format:	Mask[15:0]			
15:2	<p>Reserved</p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ	
Format:	MBZ			
1	<p>Ready for Reset</p> <table border="1"> <tr> <td>Format:</td> <td>U1</td> </tr> </table> <p>When set indicates render engine is ready for reset. This bit gets cleared on engine reset or when Soft Reset In progress is cleared.</p>	Format:	U1	
Format:	U1			
0	<p>Request Reset</p> <table border="1"> <tr> <td>Format:</td> <td>U1</td> </tr> </table> <p>When set indicates SW wishes to reset the render engine. On seeing this bit set Command Streamer will take appropriate action and set Ready For Reset status bit. This bit gets cleared on engine reset.</p>	Format:	U1	
Format:	U1			

CTX REG 1

CTXREG1-CTXREG1								
DWord	Bit	Description						
0	31:0	CTXSIZE <table border="1"> <tr> <td>Default Value:</td><td>000002FFh</td></tr> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> Register to store value for number of CTX DWORD.	Default Value:	000002FFh	Project:	BDW	Access:	RO
Default Value:	000002FFh							
Project:	BDW							
Access:	RO							

CTX reg 2

CTXREG2 - CTX reg 2						
DWord	Bit	Description				
0	31:1	CTX Register 2 <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> <tr> <td>RSVD</td><td></td></tr> </table>	Access:	R/W	RSVD	
Access:	R/W					
RSVD						
0	CTXRESTOREDONE <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> <tr> <td colspan="2">CTX restore done bit. Will be written to 1 during the last CTX restore cycle.</td></tr> </table>	Access:	R/W	CTX restore done bit. Will be written to 1 during the last CTX restore cycle.		
Access:	R/W					
CTX restore done bit. Will be written to 1 during the last CTX restore cycle.						

CUR_BASE

CUR_BASE				
Register Space:	MMIO: 0/2/0			
Project:	BDW			
Default Value:	0x00000000			
Access:	Double Buffered			
Size (in bits):	32			
Double Buffer Update Point:	Start of vertical blank or pipe not enabled			
Address:	70084h-70087h			
Name:	Cursor A Base Address			
ShortName:	CUR_BASE_A			
Valid Projects:	BDW			
Power:	Always on			
Reset:	soft			
Address:	71084h-71087h			
Name:	Cursor B Base Address			
ShortName:	CUR_BASE_B			
Valid Projects:	BDW			
Power:	off/on			
Reset:	soft			
Address:	72084h-72087h			
Name:	Cursor C Base Address			
ShortName:	CUR_BASE_C			
Valid Projects:	BDW			
Power:	off/on			
Reset:	soft			
Writes to this register arm cursor registers for this pipe.				
DWord	Bit	Description		
0	31:12	<p>Cursor Base 31:12</p> <table border="1"> <tr> <td>Format:</td><td>GraphicsAddress[31:12]</td></tr> </table> <p>This field specifies bits 31:12 of the graphics address of the base of the cursor for hi-res mode. When performing 180 degree rotation, this address does not need to change, hardware will internally offset to start from the last pixel of the last line of the cursor.</p> <p>Workaround</p> <p>To prevent false VT-d type 6 errors, use 64KB address alignment and allocate an extra 2 Page Table Entries (PTEs) beyond the end of the displayed surface. Only the PTEs will be used, not the pages themselves.</p>	Format:	GraphicsAddress[31:12]
Format:	GraphicsAddress[31:12]			

CUR_BASE		
		Restriction
	The cursor surface address must be 4K byte aligned. The cursor must be in linear memory, it cannot be tiled.	
11:7	Reserved	Project: BDW
6:4	Reserved	Project: BDW
3	Reserved	
2	Reserved	
1:0	Reserved	

CUR_CTL

CUR_CTL		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Access:	Double Buffered	
Size (in bits):	32	
Double Buffer Update Point:	Start of vertical blank or pipe not enabled; after armed	
Double Buffer Armed Write to CUR_BASE or cursor not enabled By:		
Address:	70080h-70083h	
Name:	Cursor A Control	
ShortName:	CUR_CTL_A	
Valid Projects:	BDW	
Power:	Always on	
Reset:	soft	
Address:	71080h-71083h	
Name:	Cursor B Control	
ShortName:	CUR_CTL_B	
Valid Projects:	BDW	
Power:	off/on	
Reset:	soft	
Address:	72080h-72083h	
Name:	Cursor C Control	
ShortName:	CUR_CTL_C	
Valid Projects:	BDW	
Power:	off/on	
Reset:	soft	
The cursor is enabled by programming a valid cursor mode in the cursor mode select fields. The cursor is disabled by programming all 0s in the cursor mode select fields.		
DWord	Bit	Description
0	31:28	Reserved
	27	Reserved
	Project:	BDW

CUR_CTL								
	26	Gamma Enable This bit enables pipe gamma correction for the cursor pixel data. In VGA pop-up operation, the cursor data will always bypass gamma. <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Disable</td></tr> <tr> <td>1b</td><td>Enable</td></tr> </tbody> </table>	Value	Name	0b	Disable	1b	Enable
Value	Name							
0b	Disable							
1b	Enable							
	25	Reserved						
	24	Pipe CSC Enable This bit enables pipe color space conversion for the cursor pixel data. <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Disable</td></tr> <tr> <td>1b</td><td>Enable</td></tr> </tbody> </table>	Value	Name	0b	Disable	1b	Enable
Value	Name							
0b	Disable							
1b	Enable							
	23	Reserved Project: BDW						
	22:16	Reserved						
	15	180 Rotation This mode causes the cursor image to be rotated 180 degrees. In addition to setting this bit, the cursor position must be adjusted to match the physical orientation of the display. <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0b</td><td>No rotation</td></tr> <tr> <td>1b</td><td>180 degree rotation</td></tr> </tbody> </table> Restriction Only 32 bits per pixel cursors can be rotated. This field must be zero when the cursor format is 2 bits per pixel.	Value	Name	0b	No rotation	1b	180 degree rotation
Value	Name							
0b	No rotation							
1b	180 degree rotation							
	14	Trickle Feed Enable <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Enable</td></tr> <tr> <td>1b</td><td>Disable</td></tr> </tbody> </table> Restriction Do not program this field to 1b.	Value	Name	0b	Enable	1b	Disable
Value	Name							
0b	Enable							
1b	Disable							
	13:12	Reserved						

CUR_CTL																			
	11:10	Force Alpha Plane Select																	
		<table border="1"> <tr> <td>Project:</td><td colspan="2">BDW</td></tr> </table>			Project:	BDW													
Project:	BDW																		
		<p>This field selects which planes the cursor alpha value will be forced for. It is used together with the Force Alpha Value field.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>00b</td><td>Disable</td><td>Disable alpha forcing</td></tr> <tr> <td>01b</td><td>Sprite</td><td>Enable alpha forcing where cursor overlaps sprite pixels</td></tr> <tr> <td>10b</td><td>Primary</td><td>Enable alpha forcing where cursor overlaps primary pixels</td></tr> <tr> <td>11b</td><td>Both</td><td>Enable alpha forcing where cursor overlaps either sprite or primary pixels.</td></tr> </tbody> </table>			Value	Name	Description	00b	Disable	Disable alpha forcing	01b	Sprite	Enable alpha forcing where cursor overlaps sprite pixels	10b	Primary	Enable alpha forcing where cursor overlaps primary pixels	11b	Both	Enable alpha forcing where cursor overlaps either sprite or primary pixels.
Value	Name	Description																	
00b	Disable	Disable alpha forcing																	
01b	Sprite	Enable alpha forcing where cursor overlaps sprite pixels																	
10b	Primary	Enable alpha forcing where cursor overlaps primary pixels																	
11b	Both	Enable alpha forcing where cursor overlaps either sprite or primary pixels.																	
	9:8	Force Alpha Value																	
		<p>This field controls the behavior of cursor when alpha blending onto certain plane pixels. It is used together with the Force Alpha Plane Select field.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>00b</td><td>Disable</td><td>Cursor pixels alpha blend normally over any plane.</td></tr> <tr> <td>01b</td><td>50</td><td>Cursor pixels with alpha \geq 50% are made fully opaque where they overlap the selected plane(s). Cursor pixels with alpha < 50% are made fully transparent where they overlap the selected plane(s).</td></tr> <tr> <td>10b</td><td>75</td><td>Cursor pixels with alpha \geq 75% are made fully opaque where they overlap the selected plane(s). Cursor pixels with alpha < 75% are made fully transparent where they overlap the selected plane(s).</td></tr> <tr> <td>11b</td><td>100</td><td>Cursor pixels with alpha = 100% are made fully opaque where they overlap the selected plane(s). Cursor pixels with alpha < 100% are made fully transparent where they overlap the selected plane(s).</td></tr> </tbody> </table>			Value	Name	Description	00b	Disable	Cursor pixels alpha blend normally over any plane.	01b	50	Cursor pixels with alpha \geq 50% are made fully opaque where they overlap the selected plane(s). Cursor pixels with alpha < 50% are made fully transparent where they overlap the selected plane(s).	10b	75	Cursor pixels with alpha \geq 75% are made fully opaque where they overlap the selected plane(s). Cursor pixels with alpha < 75% are made fully transparent where they overlap the selected plane(s).	11b	100	Cursor pixels with alpha = 100% are made fully opaque where they overlap the selected plane(s). Cursor pixels with alpha < 100% are made fully transparent where they overlap the selected plane(s).
Value	Name	Description																	
00b	Disable	Cursor pixels alpha blend normally over any plane.																	
01b	50	Cursor pixels with alpha \geq 50% are made fully opaque where they overlap the selected plane(s). Cursor pixels with alpha < 50% are made fully transparent where they overlap the selected plane(s).																	
10b	75	Cursor pixels with alpha \geq 75% are made fully opaque where they overlap the selected plane(s). Cursor pixels with alpha < 75% are made fully transparent where they overlap the selected plane(s).																	
11b	100	Cursor pixels with alpha = 100% are made fully opaque where they overlap the selected plane(s). Cursor pixels with alpha < 100% are made fully transparent where they overlap the selected plane(s).																	
		Restriction																	
		<p>Force Alpha is only for use with ARGB cursor formats.</p>																	
	7:6	Reserved																	

CUR_CTL																																															
5:0	Cursor Mode Select This field selects the cursor mode. Cursor is disabled when the selection is 000000b and enabled when the selection is any other value. The cursor vertical size can be overridden by the size reduction mode.																																														
<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr><td>000000b</td><td>Disable</td><td>Cursor is disabled</td></tr> <tr><td>000010b</td><td>128x128 32bpp AND/INV</td><td>128x128 32bpp AND/INVERT</td></tr> <tr><td>000011b</td><td>256x256 32bpp AND/INV</td><td>256x256 32bpp AND/INVERT</td></tr> <tr><td>000100b</td><td>64x64 2bpp 3-color</td><td>64x64 2bpp Indexed 3-color and transparency</td></tr> <tr><td>000101b</td><td>64x64 2bpp 2-color</td><td>64x64 2bpp Indexed AND/XOR 2-color</td></tr> <tr><td>000110b</td><td>64x64 2bpp 4-color</td><td>64x64 2bpp Indexed 4-color</td></tr> <tr><td>000111b</td><td>64x64 32bpp AND/INV</td><td>64x64 32bpp AND/INVERT</td></tr> <tr><td>100010b</td><td>128x128 32bpp ARGB</td><td>128x128 32bpp ARGB (8:8:8:8 MSB-A:R:G:B)</td></tr> <tr><td>100011b</td><td>256x256 32bpp ARGB</td><td>256x256 32bpp ARGB (8:8:8:8 MSB-A:R:G:B)</td></tr> <tr><td>100100b</td><td>64x64 32bpp AND/XOR</td><td>64x64 32bpp AND/XOR</td></tr> <tr><td>100101b</td><td>128x128 32bpp AND/XOR</td><td>128x128 32bpp AND/XOR</td></tr> <tr><td>100110b</td><td>256x256 32bpp AND/XOR</td><td>256x256 32bpp AND/XOR</td></tr> <tr><td>100111b</td><td>64x64 32bpp ARGB</td><td>64x64 32bpp ARGB (8:8:8:8 MSB-A:R:G:B)</td></tr> <tr><td>Others</td><td>Reserved</td><td>Reserved</td></tr> </tbody> </table>			Value	Name	Description	000000b	Disable	Cursor is disabled	000010b	128x128 32bpp AND/INV	128x128 32bpp AND/INVERT	000011b	256x256 32bpp AND/INV	256x256 32bpp AND/INVERT	000100b	64x64 2bpp 3-color	64x64 2bpp Indexed 3-color and transparency	000101b	64x64 2bpp 2-color	64x64 2bpp Indexed AND/XOR 2-color	000110b	64x64 2bpp 4-color	64x64 2bpp Indexed 4-color	000111b	64x64 32bpp AND/INV	64x64 32bpp AND/INVERT	100010b	128x128 32bpp ARGB	128x128 32bpp ARGB (8:8:8:8 MSB-A:R:G:B)	100011b	256x256 32bpp ARGB	256x256 32bpp ARGB (8:8:8:8 MSB-A:R:G:B)	100100b	64x64 32bpp AND/XOR	64x64 32bpp AND/XOR	100101b	128x128 32bpp AND/XOR	128x128 32bpp AND/XOR	100110b	256x256 32bpp AND/XOR	256x256 32bpp AND/XOR	100111b	64x64 32bpp ARGB	64x64 32bpp ARGB (8:8:8:8 MSB-A:R:G:B)	Others	Reserved	Reserved
Value	Name	Description																																													
000000b	Disable	Cursor is disabled																																													
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000101b	64x64 2bpp 2-color	64x64 2bpp Indexed AND/XOR 2-color																																													
000110b	64x64 2bpp 4-color	64x64 2bpp Indexed 4-color																																													
000111b	64x64 32bpp AND/INV	64x64 32bpp AND/INVERT																																													
100010b	128x128 32bpp ARGB	128x128 32bpp ARGB (8:8:8:8 MSB-A:R:G:B)																																													
100011b	256x256 32bpp ARGB	256x256 32bpp ARGB (8:8:8:8 MSB-A:R:G:B)																																													
100100b	64x64 32bpp AND/XOR	64x64 32bpp AND/XOR																																													
100101b	128x128 32bpp AND/XOR	128x128 32bpp AND/XOR																																													
100110b	256x256 32bpp AND/XOR	256x256 32bpp AND/XOR																																													
100111b	64x64 32bpp ARGB	64x64 32bpp ARGB (8:8:8:8 MSB-A:R:G:B)																																													
Others	Reserved	Reserved																																													
<p style="text-align: center;">Programming Notes</p> <p>INVERT, XOR, and alpha blends may not look as expected when the plane underlying the cursor is YUV or extended range RGB. Out of range RGB values will be clamped prior to alpha blending, INVERT, or XOR with cursor. It is recommended to use Force Alpha when cursor is alpha blending onto a plane of a different color space or extended gamut.</p> <p>The AND/INVERT format uses the most significant byte (MSB) to control the color. If MSB is 0xFF: Cursor is opaque. Show cursor color from three least significant bytes. If MSB is 0x00: Cursor is transparent. Three least significant bytes must be zero. If MSB is not 0x00 or 0xFF: Cursor inverts the color of the surface underneath.</p> <p>The AND/XOR format uses the most significant byte (MSB) to control the color. If MSB is 0xFF: Cursor is opaque. Show cursor color from three least significant bytes. If MSB is 0x00: Cursor is transparent. Three least significant bytes must be zero. If MSB is not 0x00 or 0xFF: The three least significant bytes are XOR'd with the color of the surface underneath.</p>																																															

CUR_FBC_CTL

CUR_FBC_CTL								
Register Space:	MMIO: 0/2/0							
Project:	BDW							
Default Value:	0x00000000							
Access:	Double Buffered							
Size (in bits):	32							
Double Buffer Update Point:	Start of vertical blank or pipe not enabled; after armed							
Double Buffer Armed Write to CUR_BASE or cursor not enabled By:								
Address:	700A0h-700A3h							
Name:	Cursor A FBC Control							
ShortName:	CUR_FBC_CTL_A							
Valid Projects:	BDW							
Power:	Always on							
Reset:	soft							
Address:	710A0h-710A3h							
Name:	Cursor B FBC Control							
ShortName:	CUR_FBC_CTL_B							
Valid Projects:	BDW							
Power:	off/on							
Reset:	soft							
Address:	720A0h-720A3h							
Name:	Cursor C FBC Control							
ShortName:	CUR_FBC_CTL_C							
Valid Projects:	BDW							
Power:	off/on							
Reset:	soft							
DWord	Bit	Description						
0	31	Size Reduction Enable This enables cursor size reduction logic. The cursor engine will fetch and display the programmed reduced number of lines, then go transparent for the rest of the frame. <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Disable</td></tr> <tr> <td>1b</td><td>Enable</td></tr> </tbody> </table>	Value	Name	0b	Disable	1b	Enable
Value	Name							
0b	Disable							
1b	Enable							

CUR_FBC_CTL		
		<p style="text-align: center;">Restriction</p> <p>Cursor size reduction is not allowed with 2bpp cursor formats or cursor 180 degree rotation. The reduced scan lines field must be programmed with a valid value when cursor size reduction is enabled.</p>
	30:8	Reserved
	7:0	<p>Reduced Scan Lines</p> <p>This specifies the number of scan lines of cursor data to fetch and display when cursor size reduction is enabled. The value programmed is the size minus one.</p> <p style="text-align: center;">Restriction</p> <p>The minimum size is 8 lines, programmed as 07h. The maximum size can not be greater than the normal size when size reduction is not enabled.</p>

CUR_PAL

CUR_PAL			
Register Space:	MMIO: 0/2/0		
Project:	BDW		
Default Value:	0x00000000		
Access:	Double Buffered		
Size (in bits):	32		
Double Buffer Update Point:	Start of vertical blank or pipe not enabled		
Address:	70090h-7009Fh		
Name:	Cursor A Palette		
ShortName:	CUR_PAL_A_*		
Valid Projects:	BDW		
Power:	Always on		
Reset:	soft		
Address:	71090h-7109Fh		
Name:	Cursor B Palette		
ShortName:	CUR_PAL_B_*		
Valid Projects:	BDW		
Power:	off/on		
Reset:	soft		
Address:	72090h-7209Fh		
Name:	Cursor C Palette		
ShortName:	CUR_PAL_C_*		
Valid Projects:	BDW		
Power:	off/on		
Reset:	soft		
The cursor palette provides color information when using the indexed cursor modes. There are 4 instances of this register format per cursor. The table below describes how the cursor mode and index value will select between the cursor palette colors, AND/XOR, transparency, and destination invert.			
Index Value	2 color mode	3 color mode	4 color mode
00	CUR_PAL 0	CUR_PAL 0	CUR_PAL 0
01	CUR_PAL 1	CUR_PAL 1	CUR_PAL 1
10	Transparent	Transparent	CUR_PAL 2
11	Invert Destination	CUR_PAL 3	CUR_PAL 3
DWord	Bit	Description	
0	31:24	Reserved	

CUR_PAL		
	23:16	Palette Red This field is the cursor palette red value
	15:8	Palette Green This field is the cursor palette green value.
	7:0	Palette Blue This field is the cursor palette blue value.

CUR_POS

CUR_POS		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Access:	Double Buffered	
Size (in bits):	32	
Double Buffer Update Point:	Start of vertical blank or pipe not enabled	
Address:	70088h-7008Bh	
Name:	Cursor A Position	
ShortName:	CUR_POS_A	
Valid Projects:	BDW	
Power:	Always on	
Reset:	soft	
Address:	71088h-7108Bh	
Name:	Cursor B Position	
ShortName:	CUR_POS_B	
Valid Projects:	BDW	
Power:	off/on	
Reset:	soft	
Address:	72088h-7208Bh	
Name:	Cursor C Position	
ShortName:	CUR_POS_C	
Valid Projects:	BDW	
Power:	off/on	
Reset:	soft	
This register specifies the screen position of the cursor. The origin of the cursor position is always the upper left corner of the display pipe source image area. When performing 180 degree rotation, the cursor image is rotated by hardware, but the position is not, so it should be adjusted if it is desired to maintain the same apparent position on a physically rotated display.		
Restriction		
The cursor must have at least a single pixel positioned over the pipe source area.		
DWord	Bit	Description
0	31	Y Position Sign This specifies the sign of the vertical position of the cursor upper left corner.

CUR_POS					
	30:28				
	Reserved <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	BDW	Format:	MBZ
Project:	BDW				
Format:	MBZ				
	27:16				
	Y Position Magnitude <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> </table> <p>This specifies the magnitude of the vertical position of the cursor upper left corner in lines.</p>	Project:	BDW		
Project:	BDW				
	15				
	X Position Sign <p>This specifies the sign of the horizontal position of the cursor upper left corner.</p>				
	14:13				
	Reserved <table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ		
Format:	MBZ				
	12:0				
	X Position Magnitude <p>This specifies the magnitude of the horizontal position of the cursor upper left corner in pixels.</p>				

Current Context Register

CCID - Current Context Register										
Register Space: MMIO: 0/2/0 Project: BDW Source: RenderCS Default Value: 0x00000000 Access: R/W Size (in bits): 32										
Address: 02180h										
This register contains the current logical rendering context address associated with the ring buffer in ring buffer mode of scheduling. This register contents are not valid in Exec-List mode of scheduling.										
Programming Notes										
The CCID register must not be written directly (via MMIO) unless the Command Streamer is completely idle (i.e., the Ring Buffer is empty and the pipeline is idle). Note that, under normal conditions, the CCID register should only be updated from the command stream using the MI_SET_CONTEXT command.										
DWord	Bit	Description								
0	31:12	Logical Render Context Address (LRCA) <table border="1"> <tr> <td>Default Value:</td><td>0h</td></tr> <tr> <td>Format:</td><td>GraphicsAddress[31:12]</td></tr> </table> <p>This field contains the 4 KB-aligned Graphics Memory Address of the current Logical Rendering Context. Bit 11 MBZ.</p>	Default Value:	0h	Format:	GraphicsAddress[31:12]				
Default Value:	0h									
Format:	GraphicsAddress[31:12]									
11:10	Reserved <table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ							
Format:	MBZ									
9	HD DVD Context <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0h</td><td>Regular Context</td><td></td></tr> <tr> <td>1h</td><td>HD DVD Context</td><td>Special considerations for TDP allow for higher voltage and frequency.</td></tr> </tbody> </table>	Value	Name	Description	0h	Regular Context		1h	HD DVD Context	Special considerations for TDP allow for higher voltage and frequency.
Value	Name	Description								
0h	Regular Context									
1h	HD DVD Context	Special considerations for TDP allow for higher voltage and frequency.								
8	Reserved <table border="1"> <tr> <td>Format:</td><td>Must Be One</td></tr> </table>	Format:	Must Be One							
Format:	Must Be One									
7:4	Reserved <table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ							
Format:	MBZ									
3	Extended State Save Enable <table border="1"> <tr> <td>Format:</td><td>Enable</td></tr> </table> <p>If set, the extended state identified in the Logical Context Data section of the Memory Data Formats chapter, is saved as part of switching away from this logical context.</p>	Format:	Enable							
Format:	Enable									

CCID - Current Context Register															
	2	Extended State Restore Enable													
<table border="1"> <tr> <td>Format:</td><td>Enable</td></tr> </table> <p>If set, the extended state identified in the Logical Context Data section of the Memory Data Formats chapter, was loaded (or restored) as part of switching to this logical context.</p>				Format:	Enable										
Format:	Enable														
	1	Reserved													
<table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>				Format:	MBZ										
Format:	MBZ														
<table border="1"> <tr> <td>Value</td><td>Name</td><td colspan="2">Description</td></tr> <tr> <td>0h</td><td>Invalid [Default]</td><td colspan="2">The other fields of this register are invalid. A switch away from the context will not invoke a context save operation.</td></tr> <tr> <td>1h</td><td>Valid</td><td colspan="2">The other fields of this register are valid, and a switch from the context will invoke the normal context save/restore operations.</td></tr> </table>				Value	Name	Description		0h	Invalid [Default]	The other fields of this register are invalid. A switch away from the context will not invoke a context save operation.		1h	Valid	The other fields of this register are valid, and a switch from the context will invoke the normal context save/restore operations.	
Value	Name	Description													
0h	Invalid [Default]	The other fields of this register are invalid. A switch away from the context will not invoke a context save operation.													
1h	Valid	The other fields of this register are valid, and a switch from the context will invoke the normal context save/restore operations.													

Current Idle/Busy/Avg Count for Freq Down Recommendation

RP_STATUS6 - Current Idle/Busy/Avg Count for Freq Down Recommendation				
DWord	Bit	Description		
0	31:24	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
Access:	RO			
23:0	<p>Current Busy in Down EI</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Reports the current busyness in the down evaluation interval.</p> <p>0 = 0 usec. 1 = 1.28 usec. 2 = 2.56 usec. 3 = 3.84 usec. FF FFFF = 21.474 sec. pmcr_current_ei_down_busy[23:0].</p>	Access:	RO	
Access:	RO			

Current Idle/Busy/Avg Count for Freq Up Recommendation

RP_STATUS5 - Current Idle/Busy/Avg Count for Freq Up Recommendation				
DWord	Bit	Description		
0	31:24	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
Access:	RO			
23:0	Current Busy in UP EI <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Reports the current busyness in the UP evaluation interval.</p> <p>0 = 0 usec. 1 = 1.28 usec. 2 = 2.56 usec. 3 = 3.84 usec. FF FFFF = 21.474 sec.</p> <p>pmcr_current_ei_up_busy[23:0].</p>	Access:	RO	
Access:	RO			

Current Time in DOWN EI

RP_STATUS4 - Current Time in DOWN EI				
Register Space:	MMIO: 0/2/0			
Project:	BDW			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0A05Ch			
DWord	Bit	Description		
0	31:24	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
Access:	RO			
23:0	Current Time in Down EI <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Reports the current Time in the down evaluation interval. 0 = 0 usec. 1 = 1.28 usec. 2 = 2.56 usec. 3 = 3.84 usec. FF FFFF = 21.474 sec. pmcr_current_ei_down_time[23:0].</p>	Access:	RO	
Access:	RO			

Current Time in UP EI

RP_STATUS3 - Current Time in UP EI				
DWord	Bit	Description		
0	31:24	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
Access:	RO			
23:0	<p>Current Time</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Reports the current time in UP EI. 0 = 0 usec. 1 = 1.28 usec. 2 = 2.56 usec. 3 = 3.84 usec. FF FFFF = 21.474 sec. pmcr_current_ei_up_time[23:0].</p>	Access:	RO	
Access:	RO			

Customizable Event Creation 0-0

CEC0-0 - Customizable Event Creation 0-0															
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x00000000 Access: R/W Size (in bits): 32															
Address: 02770h Valid Projects: [BDW]															
This register is used to define custom counter event 0, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.															
DWord	Bit	Description													
0	31:21	Negate													
		Project:	BDW												
		Format:	U11												
The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B !C)). Note that LSB of this field affects bit 0 of the selected input bus.															
<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th><th>Programming Notes</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Pass-through</td><td>Input bit is passed through to comparator as is</td><td></td></tr> <tr> <td>1b</td><td>Negated</td><td>Input bit is negated before passing to comparator</td><td>[BDW] If the input bit is negated using any bit in this field, then the corresponding Considerations bit in the CEC0-1 register must also be set.</td></tr> </tbody> </table>				Value	Name	Description	Programming Notes	0b	Pass-through	Input bit is passed through to comparator as is		1b	Negated	Input bit is negated before passing to comparator	[BDW] If the input bit is negated using any bit in this field, then the corresponding Considerations bit in the CEC0-1 register must also be set.
Value	Name	Description	Programming Notes												
0b	Pass-through	Input bit is passed through to comparator as is													
1b	Negated	Input bit is negated before passing to comparator	[BDW] If the input bit is negated using any bit in this field, then the corresponding Considerations bit in the CEC0-1 register must also be set.												
Source Select															
Format:	U2														
Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section).															
<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th><th></th></tr> </thead> <tbody> <tr> <td>01b</td><td>Prev Event</td><td>Selects the conditioned/flopped input from the last CEC block as the input bus to CEC0 block</td><td></td></tr> <tr> <td>11b</td><td>Reserved</td><td></td><td></td></tr> </tbody> </table>				Value	Name	Description		01b	Prev Event	Selects the conditioned/flopped input from the last CEC block as the input bus to CEC0 block		11b	Reserved		
Value	Name	Description													
01b	Prev Event	Selects the conditioned/flopped input from the last CEC block as the input bus to CEC0 block													
11b	Reserved														

CEC0-0 - Customizable Event Creation 0-0

	18:3	Compare Value		
		Format:	U16	
<p>The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator (see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.</p>				
	2:0	Compare Function		
		Format:	U3	
<p>This field selects the function used by the CEC0 comparator when comparing the compare value to the value active on the CEC0 conditioned input bus (see block diagram in the Custom Event Counters section).</p>				
Value	Name	Description		
000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)		
001b	Greater Than	Compare and assert output if greater than		
010b	Equal	Compare and assert output if equal to (Can also be used as AND function)		
011b	Greater Than or Equal	Compare and assert output if greater than or equal		
100b	Less Than	Compare and assert output if less than		
101b	Not Equal	Compare and assert output if not equal		
110b	Less Than or Equal	Compare and assert output if less than or equal		
111b	Reserved			

Customizable Event Creation 1-0

CEC1-0 - Customizable Event Creation 1-0													
Register Space:	MMIO: 0/2/0												
Project:	BDW												
Default Value:	0x00000000												
Access:	R/W												
Size (in bits):	32												
Address:	02778h												
Valid Projects:	[BDW]												
This register is used to define custom counter event 1, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.													
DWord	Bit	Description											
0	31:21	Negate											
		Project:	BDW										
		Format:	U11										
The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B !C)). Note that LSB of this field affects bit 0 of the selected input bus.													
<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th><th>Programming Notes</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Pass-through</td><td>Input bit is passed through to comparator as is</td><td></td></tr> <tr> <td>1b</td><td>Negated</td><td>Input bit is negated before passing to comparator</td><td>[BDW] If the input bit is negated using any bit in this field, then the corresponding Considerations bit in the CEC1-1 register must also be set.</td></tr> </tbody> </table>		Value	Name	Description	Programming Notes	0b	Pass-through	Input bit is passed through to comparator as is		1b	Negated	Input bit is negated before passing to comparator	[BDW] If the input bit is negated using any bit in this field, then the corresponding Considerations bit in the CEC1-1 register must also be set.
Value	Name	Description	Programming Notes										
0b	Pass-through	Input bit is passed through to comparator as is											
1b	Negated	Input bit is negated before passing to comparator	[BDW] If the input bit is negated using any bit in this field, then the corresponding Considerations bit in the CEC1-1 register must also be set.										
Source Select Format: <table border="1"> <tr> <td>U2</td> </tr> </table> Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section).		U2											
U2													
<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>01b</td><td>Prev Event</td><td>Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block</td></tr> <tr> <td>11b</td><td>Reserved</td><td></td></tr> </tbody> </table>		Value	Name	Description	01b	Prev Event	Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block	11b	Reserved				
Value	Name	Description											
01b	Prev Event	Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block											
11b	Reserved												
Compare Value Format: <table border="1"> <tr> <td>U16</td> </tr> </table> The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator (see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.		U16											
U16													

CEC1-0 - Customizable Event Creation 1-0

2:0	Compare Function																											
	Format:	U3																										
	This field selects the function used by the CEC comparator when comparing the compare value to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section).																											
	<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>000b</td><td>Any Are Equal</td><td>Compare and assert output if any are equal (Can be used as OR function)</td></tr> <tr> <td>001b</td><td>Greater Than</td><td>Compare and assert output if greater than</td></tr> <tr> <td>010b</td><td>Equal</td><td>Compare and assert output if equal to (Can also be used as AND function)</td></tr> <tr> <td>011b</td><td>Greater Than or Equal</td><td>Compare and assert output if greater than or equal</td></tr> <tr> <td>100b</td><td>Less Than</td><td>Compare and assert output if less than</td></tr> <tr> <td>101b</td><td>Not Equal</td><td>Compare and assert output if not equal</td></tr> <tr> <td>110b</td><td>Less Than or Equal</td><td>Compare and assert output if less than or equal</td></tr> <tr> <td>111b</td><td>Reserved</td><td></td></tr> </tbody> </table>		Value	Name	Description	000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)	001b	Greater Than	Compare and assert output if greater than	010b	Equal	Compare and assert output if equal to (Can also be used as AND function)	011b	Greater Than or Equal	Compare and assert output if greater than or equal	100b	Less Than	Compare and assert output if less than	101b	Not Equal	Compare and assert output if not equal	110b	Less Than or Equal	Compare and assert output if less than or equal	111b	Reserved
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101b	Not Equal	Compare and assert output if not equal																										
110b	Less Than or Equal	Compare and assert output if less than or equal																										
111b	Reserved																											

Customizable Event Creation 1-1

CEC1-1 - Customizable Event Creation 1-1											
Register Space:	MMIO: 0/2/0										
Project:	BDW										
Default Value:	0x00000000										
Access:	R/W										
Size (in bits):	32										
Address:	0277Ch										
This register configures the input conditioning portion of CEC (custom event creation) block 1, bit definitions in this register refer to the CEC block diagram.											
DWord	Bit	Description									
0	31:16	Considerations This 16-bit field allows individual bits of the bus selected as the input to CEC block to be delayed by 1 clock relative to the non-delayed bits in the bus (see block diagram in the Custom Event Counters section). See CEC0-1 register definition for an example use case.									
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Live</td><td>Input bit is not delayed by 1 clock before event calculation</td></tr> <tr> <td>1b</td><td>Delayed</td><td>Input bit is delayed by 1 clock before event calculation</td></tr> </tbody> </table>	Value	Name	Description	0b	Live	Input bit is not delayed by 1 clock before event calculation	1b	Delayed	Input bit is delayed by 1 clock before event calculation
Value	Name	Description									
0b	Live	Input bit is not delayed by 1 clock before event calculation									
1b	Delayed	Input bit is delayed by 1 clock before event calculation									
Mask This 16-bit field allows individual input bits to be ignored in custom event calculation. See block diagram in the Custom Event Counters section for more details on where this field is used.											
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Customizable Event Creation 2-0

CEC2-0 - Customizable Event Creation 2-0

Register Space: MMIO: 0/2/0

Project: BDW

Default Value: 0x00000000

Access: R/W

Size (in bits): 32

Address: 02780h

Valid Projects: [BDW]

This register is used to define custom counter event 2, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.

DWord	Bit	Description														
0	31:21	Negate														
		Project:	BDW													
		Format:	U11													
		The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B !C)). Note that LSB of this field affects bit 0 of the selected input bus.														
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		Format:	U16													
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CEC2-0 - Customizable Event Creation 2-0

2:0	Compare Function																											
	Format:	U3																										
	<p>This field selects the function used by the CEC comparator when comparing the compare value to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section).</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #d9e1f2;"> <th style="text-align: left; padding: 2px;">Value</th><th style="text-align: left; padding: 2px;">Name</th><th style="text-align: left; padding: 2px;">Description</th></tr> </thead> <tbody> <tr><td style="padding: 2px;">000b</td><td style="padding: 2px;">Any Are Equal</td><td style="padding: 2px;">Compare and assert output if any are equal (Can be used as OR function)</td></tr> <tr><td style="padding: 2px;">001b</td><td style="padding: 2px;">Greater Than</td><td style="padding: 2px;">Compare and assert output if greater than</td></tr> <tr><td style="padding: 2px;">010b</td><td style="padding: 2px;">Equal</td><td style="padding: 2px;">Compare and assert output if equal to (Can also be used as AND function)</td></tr> <tr><td style="padding: 2px;">011b</td><td style="padding: 2px;">Greater Than or Equal</td><td style="padding: 2px;">Compare and assert output if greater than or equal</td></tr> <tr><td style="padding: 2px;">100b</td><td style="padding: 2px;">Less Than</td><td style="padding: 2px;">Compare and assert output if less than</td></tr> <tr><td style="padding: 2px;">101b</td><td style="padding: 2px;">Not Equal</td><td style="padding: 2px;">Compare and assert output if not equal</td></tr> <tr><td style="padding: 2px;">110b</td><td style="padding: 2px;">Less Than or Equal</td><td style="padding: 2px;">Compare and assert output if less than or equal</td></tr> <tr><td style="padding: 2px;">111b</td><td style="padding: 2px;">Reserved</td><td style="padding: 2px;"></td></tr> </tbody> </table>		Value	Name	Description	000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)	001b	Greater Than	Compare and assert output if greater than	010b	Equal	Compare and assert output if equal to (Can also be used as AND function)	011b	Greater Than or Equal	Compare and assert output if greater than or equal	100b	Less Than	Compare and assert output if less than	101b	Not Equal	Compare and assert output if not equal	110b	Less Than or Equal	Compare and assert output if less than or equal	111b	Reserved
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101b	Not Equal	Compare and assert output if not equal																										
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111b	Reserved																											

Customizable Event Creation 2-1

CEC2-1 - Customizable Event Creation 2-1											
Register Space:	MMIO: 0/2/0										
Project:	BDW										
Default Value:	0x00000000										
Access:	R/W										
Size (in bits):	32										
Address:	02784h										
This register configures the input conditioning portion of CEC (custom event creation) block 2, bit definitions in this register refer to the CEC block diagram.											
DWord	Bit	Description									
0	31:16	Considerations This 16-bit field allows individual bits of the bus selected as the input to CEC block to be delayed by 1 clock relative to the non-delayed bits in the bus (see block diagram in the Custom Event Counters section). See CEC0-1 register definition for an example use case.									
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Customizable Event Creation 3-0

CEC3-0 - Customizable Event Creation 3-0															
Register Space:	MMIO: 0/2/0														
Project:	BDW														
Default Value:	0x00000000														
Access:	R/W														
Size (in bits):	32														
Address:	02788h														
Valid Projects:	[BDW]														
This register is used to define custom counter event 3, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.															
DWord	Bit	Description													
0	31:21	Negate													
		Project:	BDW												
	Format:		U11												
		The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B !C)). Note that LSB of this field affects bit 0 of the selected input bus.													
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0b	Pass-through	Input bit is passed through to comparator as is													
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CEC3-0 - Customizable Event Creation 3-0

2:0	Compare Function																											
	Format:	U3																										
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Customizable Event Creation 3-1

CEC3-1 - Customizable Event Creation 3-1									
Register Space:	MMIO: 0/2/0								
Project:	BDW								
Default Value:	0x00000000								
Access:	R/W								
Size (in bits):	32								
Address:	0278Ch								
This register configures the input conditioning portion of CEC (custom event creation) block 3, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.									
DWord	Bit	Description							
0	31:16	Considerations This 16-bit field allows individual bits of the bus selected as the input to CEC block to be delayed by 1 clock relative to the non-delayed bits in the bus (see block diagram in the Custom Event Counters section). See CEC0-1 register definition for an example use case.							
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Customizable Event Creation 4-0

CEC4-0 - Customizable Event Creation 4-0													
Register Space:		MMIO: 0/2/0											
Project:		BDW											
Default Value:		0x00000000											
Access:		R/W											
Size (in bits):		32											
Address: 02790h													
<p>This register is used to define custom counter event 4, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.</p>													
DWord	Bit	Description											
0	31:21	Negate											
		Project:	BDW										
		Format:	U11										
		<p>The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B !C)). Note that LSB of this field affects bit 0 of the selected input bus.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th><th>Programming Notes</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Pass-through</td><td>Input bit is passed through to comparator as is</td><td></td></tr> <tr> <td>1b</td><td>Negated</td><td>Input bit is negated before passing to comparator</td><td>[BDW] If the input bit is negated using any bit in this field, then the corresponding Considerations bit in the CEC4-1 register must also be set.</td></tr> </tbody> </table>		Value	Name	Description	Programming Notes	0b	Pass-through	Input bit is passed through to comparator as is		1b	Negated
Value	Name	Description	Programming Notes										
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1b	Negated	Input bit is negated before passing to comparator	[BDW] If the input bit is negated using any bit in this field, then the corresponding Considerations bit in the CEC4-1 register must also be set.										
0	20:19	Source Select											
		Format:	U2										
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CEC4-0 - Customizable Event Creation 4-0

2:0	Compare Function																											
	Format:	U3																										
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Customizable Event Creation 5-0

CEC5-0 - Customizable Event Creation 5-0																			
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x00000000 Access: R/W Size (in bits): 32																			
Address: 02798h																			
This register is used to define custom counter event 5, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.																			
DWord	Bit	Description																	
0	31:21	Negate																	
		Project:		BDW															
		Format:		U11															
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Value	Name	Description	Programming Notes																
0b	Pass-through	Input bit is passed through to comparator as is																	
1b	Negated	Input bit is negated before passing to comparator	[BDW] If the input bit is negated using any bit in this field, then the corresponding Considerations bit in the CEC5-1 register must also be set.																
0	20:19	Source Select																	
		Format:		U2															
		Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section).																	
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CEC5-0 - Customizable Event Creation 5-0

2:0	Compare Function																											
	Format:	U3																										
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101b	Not Equal	Compare and assert output if not equal																										
110b	Less Than or Equal	Compare and assert output if less than or equal																										
111b	Reserved																											

Customizable Event Creation 5-1

CEC5-1 - Customizable Event Creation 5-1

Register Space: MMIO: 0/2/0

Project: BDW

Default Value: 0x00000000

Access: R/W

Size (in bits): 32

Address: 0279Ch

This register configures the input conditioning portion of CEC (custom event creation) block 5, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.

DWord	Bit	Description									
0	31:16	<p>Considerations</p> <p>This 16-bit field allows individual bits of the bus selected as the input to CEC block to be delayed by 1 clock relative to the non-delayed bits in the bus (see block diagram in the Custom Event Counters section). See CEC0-1 register definition for an example use case.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Live</td> <td>Input bit is not delayed by 1 clock before event calculation</td> </tr> <tr> <td>1b</td> <td>Delayed</td> <td>Input bit is delayed by 1 clock before event calculation</td> </tr> </tbody> </table>	Value	Name	Description	0b	Live	Input bit is not delayed by 1 clock before event calculation	1b	Delayed	Input bit is delayed by 1 clock before event calculation
Value	Name	Description									
0b	Live	Input bit is not delayed by 1 clock before event calculation									
1b	Delayed	Input bit is delayed by 1 clock before event calculation									
	15:0	<p>Mask</p> <p>This 16-bit field allows individual input bits to be ignored in custom event calculation. See block diagram in the Custom Event Counters section for more details on where this field is used.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Unmasked</td> <td>Input bit is considered in event calculation</td> </tr> <tr> <td>1b</td> <td>Masked</td> <td>Input bit is ignored in event calculation</td> </tr> </tbody> </table>	Value	Name	Description	0b	Unmasked	Input bit is considered in event calculation	1b	Masked	Input bit is ignored in event calculation
Value	Name	Description									
0b	Unmasked	Input bit is considered in event calculation									
1b	Masked	Input bit is ignored in event calculation									

Customizable Event Creation 6-0

CEC6-0 - Customizable Event Creation 6-0																				
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x00000000 Access: R/W Size (in bits): 32																				
Address: 027A0h																				
This register is used to define custom counter event 6, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.																				
DWord	Bit	Description																		
0	31:21	Negate <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>U11</td></tr> </table> <p>The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B !C)). Note that LSB of this field affects bit 0 of the selected input bus.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th><th>Programming Notes</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Pass-through</td><td>Input bit is passed through to comparator as is</td><td></td></tr> <tr> <td>1b</td><td>Negated</td><td>Input bit is negated before passing to comparator</td><td>[BDW] If the input bit is negated using any bit in this field, then the corresponding Considerations bit in the CEC6-1 register must also be set.</td></tr> </tbody> </table>			Project:	BDW	Format:	U11	Value	Name	Description	Programming Notes	0b	Pass-through	Input bit is passed through to comparator as is		1b	Negated	Input bit is negated before passing to comparator	[BDW] If the input bit is negated using any bit in this field, then the corresponding Considerations bit in the CEC6-1 register must also be set.
Project:	BDW																			
Format:	U11																			
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Source Select <table border="1"> <tr> <td>Format:</td><td>U2</td></tr> </table> <p>Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section).</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>01b</td><td>Prev Event</td><td>Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block</td></tr> <tr> <td>11b</td><td>Reserved</td><td></td></tr> </tbody> </table>			Format:	U2	Value	Name	Description	01b	Prev Event	Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block	11b	Reserved								
Format:	U2																			
Value	Name	Description																		
01b	Prev Event	Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block																		
11b	Reserved																			
Compare Value <table border="1"> <tr> <td>Format:</td><td>U16</td></tr> </table> <p>The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator (see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.</p>			Format:	U16																
Format:	U16																			

CEC6-0 - Customizable Event Creation 6-0

2:0	Compare Function																											
	Format:	U3																										
	<p>This field selects the function used by the CEC comparator when comparing the compare value to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section).</p>																											
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110b	Less Than or Equal	Compare and assert output if less than or equal																										
111b	Reserved																											

Customizable Event Creation 6-1

CEC6-1 - Customizable Event Creation 6-1									
Register Space:	MMIO: 0/2/0								
Project:	BDW								
Default Value:	0x00000000								
Access:	R/W								
Size (in bits):	32								
Address:	027A4h								
This register configures the input conditioning portion of CEC (custom event creation) block 6, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.									
DWord	Bit	Description							
0	31:16	Considerations This 16-bit field allows individual bits of the bus selected as the input to CEC block to be delayed by 1 clock relative to the non-delayed bits in the bus (see block diagram in the Custom Event Counters section). See CEC0-1 register definition for an example use case.							
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Value	Name	Description							
0b	Live	Input bit is not delayed by 1 clock before event calculation							
1b	Delayed	Input bit is delayed by 1 clock before event calculation							
	15:0	Mask This 16-bit field allows individual input bits to be ignored in custom event calculation. See block diagram in the Custom Event Counters section for more details on where this field is used.							
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Value	Name	Description							
0b	Unmasked	Input bit is considered in event calculation							
1b	Masked	Input bit is ignored in event calculation							

Customizable Event Creation 7-0

CEC7-0 - Customizable Event Creation 7-0																			
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x00000000 Access: R/W Size (in bits): 32																			
Address: 027A8h																			
This register is used to define custom counter event 7, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.																			
DWord	Bit	Description																	
0	31:21	Negate																	
		Project:		BDW															
		Format:		U11															
The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B !C)). Note that LSB of this field affects bit 0 of the selected input bus.																			
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Value	Name	Description	Programming Notes																
0b	Pass-through	Input bit is passed through to comparator as is																	
1b	Negated	Input bit is negated before passing to comparator	[BDW] If the input bit is negated using any bit in this field, then the corresponding Considerations bit in the CEC7-1 register must also be set.																
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		Format:		U2															
		Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section).																	
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		Format:		U16															
The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator (see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.																			

CEC7-0 - Customizable Event Creation 7-0

2:0	Compare Function																											
	Format:	U3																										
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101b	Not Equal	Compare and assert output if not equal																										
110b	Less Than or Equal	Compare and assert output if less than or equal																										
111b	Reserved																											

Customizable Event Creation 7-1

CEC7-1 - Customizable Event Creation 7-1											
Register Space:	MMIO: 0/2/0										
Project:	BDW										
Default Value:	0x00000000										
Access:	R/W										
Size (in bits):	32										
Address:	027ACh										
<p>This register configures the input conditioning portion of CEC (custom event creation) block 3, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.</p>											
DWord	Bit	Description									
0	31:16	Considerations This 16-bit field allows individual bits of the bus selected as the input to CEC block to be delayed by 1 clock relative to the non-delayed bits in the bus (see block diagram in the Custom Event Counters section). See CEC0-1 register definition for an example use case.									
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Value	Name	Description									
0b	Unmasked	Input bit is considered in event calculation									
1b	Masked	Input bit is ignored in event calculation									

CVS TLB LRA 0

CVS_TLB_LRA_0 - CVS TLB LRA 0							
DWord	Bit	Description					
0	31	Reserved <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Default Value:	0b	Access:	RO	
Default Value:	0b						
Access:	RO						
30:24	CVS LRA1 Max <table border="1"> <tr> <td>Default Value:</td> <td>1011111b</td> </tr> <tr> <td>Project:</td> <td>BDW, :GT2:B</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Maximum value of programmable LRA1.</p>	Default Value:	1011111b	Project:	BDW, :GT2:B	Access:	R/W
Default Value:	1011111b						
Project:	BDW, :GT2:B						
Access:	R/W						
23	Reserved <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Default Value:	0b	Access:	RO		
Default Value:	0b						
Access:	RO						
22:16	CVS LRA1 Min <table border="1"> <tr> <td>Default Value:</td> <td>0100000b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Minimum value of programmable LRA1.</p>	Default Value:	0100000b	Access:	R/W		
Default Value:	0100000b						
Access:	R/W						
15	Reserved <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Default Value:	0b	Access:	RO		
Default Value:	0b						
Access:	RO						
14:8	CVS LRA0 Max <table border="1"> <tr> <td>Default Value:</td> <td>0011111b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Maximum value of programmable LRA0.</p>	Default Value:	0011111b	Access:	R/W		
Default Value:	0011111b						
Access:	R/W						
7	Reserved <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Default Value:	0b	Access:	RO		
Default Value:	0b						
Access:	RO						

CVS_TLB_LRA_0 - CVS TLB LRA 0		
	6:0	CVS LRA0 Min Default Value: 0000000b Access: R/W Minimum value of programmable LRA0.

CVS TLB LRA 1

CVS_TLB_LRA_1 - CVS TLB LRA 1						
DWord	Bit	Description				
0	31	Reserved <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Default Value:	0b	Access:	RO
Default Value:	0b					
Access:	RO					
30:24	CVS LRA3 Max <table border="1"> <tr> <td>Default Value:</td> <td>1111111b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>For Future Use. Not Used in DevBDW.</p>	Default Value:	1111111b	Access:	R/W	
Default Value:	1111111b					
Access:	R/W					
23	Reserved <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Default Value:	0b	Access:	RO	
Default Value:	0b					
Access:	RO					
22:16	CVS LRA3 Min <table border="1"> <tr> <td>Default Value:</td> <td>0000000b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>For Future Use. Not Used in DevBDW.</p>	Default Value:	0000000b	Access:	R/W	
Default Value:	0000000b					
Access:	R/W					
15	Reserved <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Default Value:	0b	Access:	RO	
Default Value:	0b					
Access:	RO					
14:8	CVS LRA2 Max <table border="1"> <tr> <td>Default Value:</td> <td>1111111b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Maximum value of programmable LRA2.</p>	Default Value:	1111111b	Access:	R/W	
Default Value:	1111111b					
Access:	R/W					
7	Reserved <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Default Value:	0b	Access:	RO	
Default Value:	0b					
Access:	RO					

CVS_TLB_LRA_1 - CVS TLB LRA 1		
	6:0	CVS LRA2 Min Default Value: 1100000b Access: R/W Minimum value of programmable LRA2.

CVS TLB LRA 2

CVS_TLB_LRA_2 - CVS TLB LRA 2						
DWord	Bit	Description				
0	31:8	Reserved <table border="1"> <tr> <td>Default Value:</td><td>000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	000000h	Access:	RO
Default Value:	000000h					
Access:	RO					
	7:6	RS LRA <table border="1"> <tr> <td>Default Value:</td><td>00b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Which LRA should RS use</p>	Default Value:	00b	Access:	R/W
Default Value:	00b					
Access:	R/W					
	5:4	CS LRA <table border="1"> <tr> <td>Default Value:</td><td>01b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Which LRA should CS use.</p>	Default Value:	01b	Access:	R/W
Default Value:	01b					
Access:	R/W					
	3:2	SOL LRA <table border="1"> <tr> <td>Default Value:</td><td>10b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Which LRA should SOL use.</p>	Default Value:	10b	Access:	R/W
Default Value:	10b					
Access:	R/W					
	1:0	VF LRA <table border="1"> <tr> <td>Default Value:</td><td>10b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Which LRA should VF use.</p>	Default Value:	10b	Access:	R/W
Default Value:	10b					
Access:	R/W					

DAC_CTL

DAC_CTL																	
Register Space: MMIO: 0/2/0 Project: DevLPT:H Default Value: 0x00040000 Access: R/W Size (in bits): 32																	
Address: E1100h-E1103h Name: Analog Port CRT DAC Control ShortName: DAC_CTL Power: Always on Reset: soft																	
DWord	Bit	Description															
0	31	Port Enable This bit enables or disables the analog port CRT DAC and syncs outputs. The CRT DAC capability disable fuse (SFUSE_STRAP bit 6) can override so that this port can not be enabled. <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Disable</td><td>Disable the analog port DAC and disable output of syncs</td></tr> <tr> <td>1b</td><td>Enable</td><td>Enable the analog port DAC and enable output of syncs</td></tr> </tbody> </table>	Value	Name	Description	0b	Disable	Disable the analog port DAC and disable output of syncs	1b	Enable	Enable the analog port DAC and enable output of syncs						
Value	Name	Description															
0b	Disable	Disable the analog port DAC and disable output of syncs															
1b	Enable	Enable the analog port DAC and enable output of syncs															
30:26	Reserved Format: MBZ																
25:24	25:24	CRT HPD Channel Status Access: RO These bits indicate which color channels were found to be attached on the last hot plug detection cycle. These bits go to the SDE_ISR CRT hot plug register bit. <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>00b</td><td>None</td><td>No channels attached</td></tr> <tr> <td>01b</td><td>Blue</td><td>Blue channel only is attached</td></tr> <tr> <td>10b</td><td>Green</td><td>Green channel only is attached</td></tr> <tr> <td>11b</td><td>Both</td><td>Both blue and green channel attached</td></tr> </tbody> </table>	Value	Name	Description	00b	None	No channels attached	01b	Blue	Blue channel only is attached	10b	Green	Green channel only is attached	11b	Both	Both blue and green channel attached
Value	Name	Description															
00b	None	No channels attached															
01b	Blue	Blue channel only is attached															
10b	Green	Green channel only is attached															
11b	Both	Both blue and green channel attached															
23	CRT HPD Enable Hot plug detection is used to set status bits on the connection or disconnection of a CRT to the analog port CRT DAC. <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Disable</td><td>CRT hot plug detection is disabled</td></tr> <tr> <td>1b</td><td>Enable</td><td>CRT hot plug detection is enabled</td></tr> </tbody> </table>	Value	Name	Description	0b	Disable	CRT hot plug detection is disabled	1b	Enable	CRT hot plug detection is enabled							
Value	Name	Description															
0b	Disable	CRT hot plug detection is disabled															
1b	Enable	CRT hot plug detection is enabled															

DAC_CTL																	
22	CRT HPD Activation Period This bit sets the activation period for the CRT hot plug circuit.	<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>64 rawclk</td><td>64 rawclk periods</td></tr> <tr> <td>1b</td><td>128 rawclk</td><td>128 rawclk periods</td></tr> </tbody> </table>	Value	Name	Description	0b	64 rawclk	64 rawclk periods	1b	128 rawclk	128 rawclk periods						
Value	Name	Description															
0b	64 rawclk	64 rawclk periods															
1b	128 rawclk	128 rawclk periods															
21	CRT HPD Warmup Time This bit sets the warmup time for the CRT hot plug circuit.	<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>4ms</td><td>Approximately 4ms</td></tr> <tr> <td>1b</td><td>8ms</td><td>Approximately 8ms</td></tr> </tbody> </table>	Value	Name	Description	0b	4ms	Approximately 4ms	1b	8ms	Approximately 8ms						
Value	Name	Description															
0b	4ms	Approximately 4ms															
1b	8ms	Approximately 8ms															
20	CRT HPD Sampling Period This bit determines the length of time between sampling periods when the transcoder is disabled.	<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>2 seconds</td><td>Approximately 2 seconds</td></tr> <tr> <td>1b</td><td>4 seconds</td><td>Approximately 4 seconds</td></tr> </tbody> </table>	Value	Name	Description	0b	2 seconds	Approximately 2 seconds	1b	4 seconds	Approximately 4 seconds						
Value	Name	Description															
0b	2 seconds	Approximately 2 seconds															
1b	4 seconds	Approximately 4 seconds															
19:18	CRT HPD Voltage Value Value to drive to the DAC to determine whether the analog port is connected to a CRT.	<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>00b</td><td>0x90</td><td>0x90</td></tr> <tr> <td>01b</td><td>0xA0 [Default]</td><td>0xA0</td></tr> <tr> <td>10b</td><td>0xB0</td><td>0xB0</td></tr> <tr> <td>11b</td><td>0xC0</td><td>0xC0</td></tr> </tbody> </table>	Value	Name	Description	00b	0x90	0x90	01b	0xA0 [Default]	0xA0	10b	0xB0	0xB0	11b	0xC0	0xC0
Value	Name	Description															
00b	0x90	0x90															
01b	0xA0 [Default]	0xA0															
10b	0xB0	0xB0															
11b	0xC0	0xC0															
17	Reserved	Format: MBZ															
16	Force CRT HPD Trigger Triggers a CRT hotplug/unplug detection cycle independent of the hot plug detection enable bit. This bit is automatically cleared after the detection is completed. The result of this trigger is reflected in the CRT Hot Plug Detection Status. Software must reset status after a force CRT detect trigger.	<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>No Trigger</td><td>No Trigger</td></tr> <tr> <td>1b</td><td>Force Trigger</td><td>Force Trigger</td></tr> </tbody> </table>	Value	Name	Description	0b	No Trigger	No Trigger	1b	Force Trigger	Force Trigger						
Value	Name	Description															
0b	No Trigger	No Trigger															
1b	Force Trigger	Force Trigger															
15:5	Reserved	Format: MBZ															

DAC_CTL											
	4	VSYNC Polarity Control The output VSYNC polarity is controlled by this bit. This is used to implement display modes that require inverted polarity syncs and to set the disabled state of the VSYNC signal. <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Low</td><td>Active Low</td></tr> <tr> <td>1b</td><td>High</td><td>Active High</td></tr> </tbody> </table>	Value	Name	Description	0b	Low	Active Low	1b	High	Active High
Value	Name	Description									
0b	Low	Active Low									
1b	High	Active High									
	3	Hsync Polarity Control The output HSYNC polarity is controlled by this bit. This is used to implement display modes that require inverted polarity syncs and to set the disabled state of the HSYNC signal. <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Low</td><td>Active Low</td></tr> <tr> <td>1b</td><td>High</td><td>Active High</td></tr> </tbody> </table>	Value	Name	Description	0b	Low	Active Low	1b	High	Active High
Value	Name	Description									
0b	Low	Active Low									
1b	High	Active High									
	2:0	Reserved Format: MBZ									

DATAM

DATAM			
Register Space:		MMIO: 0/2/0	
Project:		BDW	
Default Value:		0x00000000	
Access:		R/W	
Size (in bits):		32	
Address:		60030h-60033h	
Name:		Transcoder A Data M Value 1	
ShortName:		TRANS_DATAM1_A	
Valid Projects:		BDW	
Power:		off/on	
Reset:		soft	
Address:		61030h-61033h	
Name:		Transcoder B Data M Value 1	
ShortName:		TRANS_DATAM1_B	
Valid Projects:		BDW	
Power:		off/on	
Reset:		soft	
Address:		62030h-62033h	
Name:		Transcoder C Data M Value 1	
ShortName:		TRANS_DATAM1_C	
Valid Projects:		BDW	
Power:		off/on	
Reset:		soft	
Address:		6F030h-6F033h	
Name:		Transcoder EDP Data M Value 1	
ShortName:		TRANS_DATAM1_EDP	
Valid Projects:		BDW	
Power:		Always on	
Reset:		soft	
Description			Project
There is one instance of this register for each transcoder A/B/C/EDP. This register is double buffered to update on the next MSA after LINKN is written.			BDW
DWord	Bit	Description	
0	31	Reserved	
		Format:	MBZ

DATAM

	30:25	TU or VCpayload Size In DisplayPort SST mode this field is the size of the transfer unit, minus one. Typically it is programmed with a value of 63 for TU size of 64. In DisplayPort MST mode this field is the Virtual Channel payload size, minus one.		
Restriction				
	24	In DisplayPort MST mode the Virtual Channel payload size must not be programmed greater than 62 (resulting payload size of 63). In DisplayPort MST mode the Virtual Channel payload size must not be changed while the Virtual Channel is enabled, even after a transcoder has been disabled.		
	23:0	Reserved <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Format:</td> <td style="width: 50%;">MBZ</td> </tr> </table> Data M value This field is the data M value for internal use.	Format:	MBZ
Format:	MBZ			

DATAN

DATAN		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	60034h-60037h	
Name:	Transcoder A Data N Value 1	
ShortName:	TRANS_DATAN1_A	
Valid Projects:	BDW	
Power:	off/on	
Reset:	soft	
Address:	61034h-61037h	
Name:	Transcoder B Data N Value 1	
ShortName:	TRANS_DATAN1_B	
Valid Projects:	BDW	
Power:	off/on	
Reset:	soft	
Address:	62034h-62037h	
Name:	Transcoder C Data N Value 1	
ShortName:	TRANS_DATAN1_C	
Valid Projects:	BDW	
Power:	off/on	
Reset:	soft	
Address:	6F034h-6F037h	
Name:	Transcoder EDP Data N Value 1	
ShortName:	TRANS_DATAN1_EDP	
Valid Projects:	BDW	
Power:	Always on	
Reset:	soft	
Description		Project
There is one instance of this register for each transcoder A/B/C/EDP. This register is double buffered to update on the next MSA after LINKN is written.		BDW
DWord	Bit	Description
0	31:24	Reserved
		Format:
		MBZ

DATAN

23:0

Data N value

This field is the data N value for internal use.

DDI_AUX_CTL

DDI_AUX_CTL										
Register Space: MMIO: 0/2/0 Project: BDW 0x000300E1 [BDW] Access: R/W Size (in bits): 32										
Address: 64010h-64013h Name: DDI A AUX Channel Control ShortName: DDI_AUX_CTL_A Valid Projects: BDW Power: Always on Reset: soft										
Restriction										
Restriction : DDI A AUX channel transactions must not be sent while SRD is enabled. SRD must be completely disabled before a DDI A AUX channel transaction can be sent.										
DWord	Bit	Description								
0	31	Send Busy <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px; text-align: right;">R/W Set</td> </tr> <tr> <td colspan="2" style="padding: 2px;">Writing this bit with 1b initiates the transaction, when read this bit will be a 1b until the transmission completes. The transaction is completed when the response is received or when a timeout occurs. This is a sticky bit. Write a 1b to this bit to set it and initiate the transaction. Hardware will clear it when the transaction completes.</td> </tr> <tr> <td colspan="2" style="padding: 2px; text-align: center;">Workaround</td> </tr> <tr> <td colspan="2" style="padding: 2px;">Set the Timeout timer value to at least 600us before initiating a transaction.</td> </tr> </table>	Access:	R/W Set	Writing this bit with 1b initiates the transaction, when read this bit will be a 1b until the transmission completes. The transaction is completed when the response is received or when a timeout occurs. This is a sticky bit. Write a 1b to this bit to set it and initiate the transaction. Hardware will clear it when the transaction completes.		Workaround		Set the Timeout timer value to at least 600us before initiating a transaction.	
Access:	R/W Set									
Writing this bit with 1b initiates the transaction, when read this bit will be a 1b until the transmission completes. The transaction is completed when the response is received or when a timeout occurs. This is a sticky bit. Write a 1b to this bit to set it and initiate the transaction. Hardware will clear it when the transaction completes.										
Workaround										
Set the Timeout timer value to at least 600us before initiating a transaction.										
Restriction <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td colspan="2" style="padding: 2px;">Do not change any fields while Send Busy is asserted. Do not write a 1b again until transaction completes.</td> </tr> </table>	Do not change any fields while Send Busy is asserted. Do not write a 1b again until transaction completes.									
Do not change any fields while Send Busy is asserted. Do not write a 1b again until transaction completes.										
Done <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px; text-align: right;">R/WC</td> </tr> <tr> <td colspan="2" style="padding: 2px;">A sticky bit that indicates the transaction has completed. Write a 1 to this bit to clear the event</td> </tr> <tr> <th style="padding: 2px;">Value</th><th style="padding: 2px;">Name</th></tr> <tr> <td style="padding: 2px;">0b</td><td style="padding: 2px;">Not done</td></tr> <tr> <td style="padding: 2px;">1b</td><td style="padding: 2px;">Done</td></tr> </table>	Access:	R/WC	A sticky bit that indicates the transaction has completed. Write a 1 to this bit to clear the event		Value	Name	0b	Not done	1b	Done
Access:	R/WC									
A sticky bit that indicates the transaction has completed. Write a 1 to this bit to clear the event										
Value	Name									
0b	Not done									
1b	Done									

DDI_AUX_CTL																			
29	Interrupt on Done	<table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Access:</td><td style="width: 50%;">R/W</td></tr> </table> <p>Enable an interrupt when the transaction completes or times out.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th><th style="text-align: center;">Name</th></tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td><td>Enable</td></tr> <tr> <td style="text-align: center;">1b</td><td>Disable</td></tr> </tbody> </table>	Access:	R/W	Value	Name	0b	Enable	1b	Disable									
Access:	R/W																		
Value	Name																		
0b	Enable																		
1b	Disable																		
28	Time out error	<table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Access:</td><td style="width: 50%;">R/WC</td></tr> </table> <p>A sticky bit that indicates the transaction has timed out. Write a 1 to this bit to clear the event.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th><th style="text-align: center;">Name</th></tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td><td>Not error</td></tr> <tr> <td style="text-align: center;">1b</td><td>Error</td></tr> </tbody> </table>	Access:	R/WC	Value	Name	0b	Not error	1b	Error									
Access:	R/WC																		
Value	Name																		
0b	Not error																		
1b	Error																		
27:26	Time out timer value	<table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Access:</td><td style="width: 50%;">R/W</td></tr> </table> <p>Used to determine how long to wait for receiver response before timing out.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th><th style="text-align: center;">Name</th><th style="text-align: center;">Programming Notes</th></tr> </thead> <tbody> <tr> <td style="text-align: center;">00b</td><td>400us</td><td>BDW Do not use this setting.</td></tr> <tr> <td style="text-align: center;">01b</td><td>600us</td><td></td></tr> <tr> <td style="text-align: center;">10b</td><td>800us</td><td></td></tr> <tr> <td style="text-align: center;">11b</td><td>1600us</td><td></td></tr> </tbody> </table>	Access:	R/W	Value	Name	Programming Notes	00b	400us	BDW Do not use this setting.	01b	600us		10b	800us		11b	1600us	
Access:	R/W																		
Value	Name	Programming Notes																	
00b	400us	BDW Do not use this setting.																	
01b	600us																		
10b	800us																		
11b	1600us																		
25	Receive error	<table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Access:</td><td style="width: 50%;">R/WC</td></tr> </table> <p>A sticky bit that indicates that the data received was corrupted, not in multiples of a full byte, or more than 20 bytes. Write a 1 to this bit to clear the event.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th><th style="text-align: center;">Name</th></tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td><td>Not Error</td></tr> <tr> <td style="text-align: center;">1b</td><td>Error</td></tr> </tbody> </table>	Access:	R/WC	Value	Name	0b	Not Error	1b	Error									
Access:	R/WC																		
Value	Name																		
0b	Not Error																		
1b	Error																		
24:20	Message Size	<table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Access:</td><td style="width: 50%;">Write/Read Status</td></tr> </table> <p>The value written to this field indicates the total number bytes to transmit (including the header). The value read from this field indicates the number of bytes received, including the header, in the last transaction transaction. Sync/Stop are not part of the message or the message size. Reads of this field will give the response message size. The read value will not be valid while Send/Busy bit 31 is asserted.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <th style="text-align: center;">Restriction</th></tr> <tr> <td>Message sizes of 0 or >20 are not allowed. Reads and writes are valid only when the done bit is set and timeout or receive error has not occurred.</td></tr> </table>	Access:	Write/Read Status	Restriction	Message sizes of 0 or >20 are not allowed. Reads and writes are valid only when the done bit is set and timeout or receive error has not occurred.													
Access:	Write/Read Status																		
Restriction																			
Message sizes of 0 or >20 are not allowed. Reads and writes are valid only when the done bit is set and timeout or receive error has not occurred.																			

DDI_AUX_CTL							
	19:16 Precharge Time						
	<table border="1"> <tr> <td>Default Value:</td><td>0011b 6us</td></tr> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Used to determine the precharge time for the Aux Channel. During this time the Aux Channel will drive the SYNC pattern. Every microsecond gives one additional SYNC pulse beyond the hard coded 26 SYNC pulses. The value is the number of microseconds times 2. Default is 3 decimal which gives 6us of precharge which is 6 extra SYNC pulses for a total of 32.</p>	Default Value:	0011b 6us	Project:	BDW	Access:	R/W
Default Value:	0011b 6us						
Project:	BDW						
Access:	R/W						
	15 Reserved						
	14:12 Reserved						
	<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> </table>	Project:	BDW				
Project:	BDW						
	11 Reserved						
	10:0 2X Bit Clock divider						
	<table border="1"> <tr> <td>Default Value:</td><td>00 1110 0001b 225</td></tr> <tr> <td>Project:</td><td>BDW</td></tr> </table> <p>This field is used to determine the 2X bit clock the Aux Channel logic runs on. This value divides the input clock frequency down to 2X bit clock rate. It should be programmed to get as close as possible to the ideal rate of 2MHz. The input clock is the cdclk. Default is 225 decimal which divides the default 450 MHz cdclk input clock to become 2MHz bit clock.</p>	Default Value:	00 1110 0001b 225	Project:	BDW		
Default Value:	00 1110 0001b 225						
Project:	BDW						
	Restriction						
	The default value only works with cdclk 450 MHz. It must be programmed if the CD clock frequency is changed.						

DDI_AUX_DATA

DDI_AUX_DATA		
Register Space: MMIO: 0/2/0		
Project: BDW		
Default Value: 0x00000000		
Access: Write/Read Status		
Size (in bits): 32		
Address: 64014h-64027h		
Name: DDI A AUX Channel Data		
ShortName: DDI_AUX_DATA_A_*		
Valid Projects: BDW		
Power: Always on		
Reset: soft		
There are 5 DWords of this register format per instance.		
DWord	Bit	Description
0	31:0	AUX CH DATA This field contains a DWord of the AUX message. Writes to this register give the data to transmit during the transaction. The MSbyte is transmitted first. Reads to this register will give the response data after transaction complete. The read value will not be valid while the Aux Channel Control Register Send/Busy bit is asserted

DDI_BUF_CTL

DDI_BUF_CTL	
Register Space:	MMIO: 0/2/0
Project:	BDW
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	64000h-64003h
Name:	DDI A Buffer Control
ShortName:	DDI_BUF_CTL_A
Valid Projects:	BDW
Power:	Always on
Reset:	soft
Address:	64100h-64103h
Name:	DDI B Buffer Control
ShortName:	DDI_BUF_CTL_B
Valid Projects:	BDW
Power:	Always on
Reset:	soft
Address:	64200h-64203h
Name:	DDI C Buffer Control
ShortName:	DDI_BUF_CTL_C
Valid Projects:	BDW
Power:	Always on
Reset:	soft
Address:	64300h-64303h
Name:	DDI D Buffer Control
ShortName:	DDI_BUF_CTL_D
Valid Projects:	BDW
Power:	Always on
Reset:	soft
Address:	64400h-64403h
Name:	DDI E Buffer Control
ShortName:	DDI_BUF_CTL_E
Valid Projects:	BDW
Power:	Always on
Reset:	soft

DDI_BUF_CTL

There is one DDI Buffer Control per each DDI A/B/C/D/E/F.

DWord	Bit	Description						
0	31	DDI Buffer Enable This bit enables the DDI buffer.						
		<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center; background-color: #e0e0ff;">Value</th> <th style="text-align: center; background-color: #e0e0ff;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td> <td>Disable</td> </tr> <tr> <td style="text-align: center;">1b</td> <td>Enable</td> </tr> </tbody> </table>		Value	Name	0b	Disable	1b
Value	Name							
0b	Disable							
1b	Enable							
30	Reserved							
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">MBZ</td> </tr> </table>		Format:	MBZ				
Format:	MBZ							
29:28	Reserved							
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Project:</td> <td style="width: 30%;">BDW</td> </tr> </table>		Project:	BDW				
Project:	BDW							
27:24	DP Vswing Emp Sel							
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Project:</td> <td style="width: 30%;">BDW</td> </tr> </table>		Project:	BDW				
Project:	BDW							
Description								
These bits are used to select the voltage swing and emphasis for DisplayPort and FDI.								
This field is ignored for HDMI and DVI. The values programmed in DDI_BUF_TRANS determine the voltage swing and emphasis for each selection.								
Value		Name	Description					
0000b- 1000b	Select 0 - Select 8	Select from buffer translations 0 through 8. Valid with all DDIs.						
Reserved		<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">MBZ</td> </tr> </table>		Format:	MBZ			
Format:	MBZ							

DDI_BUF_CTL

	16	<p>Port Reversal This field enables lane reversal within the port. Lane reversal swaps the data on the lanes as they are output from the port.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center; background-color: #e0e0ff;">Value</th><th style="text-align: center; background-color: #e0e0ff;">Name</th></tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td><td>Not reversed</td></tr> <tr> <td style="text-align: center;">1b</td><td>Reversed</td></tr> </tbody> </table> <p>Programming Notes DDI B, C, D, and F reversal always swaps the four lanes, so lane 0 is swapped with lane 3, and lane 1 is swapped with lane 2. If DDIA Lane Capability Control selects DDIA x2, then DDI A reversal swaps the two lanes, so lane 0 is swapped with lane 1. If DDIA Lane Capability Control selects DDIA x4, then DDI A reversal swaps the four lanes, so lane 0 is swapped with lane 3, and lane 1 is swapped with lane 2.</p> <p>Restriction This field must not be changed while the DDI is enabled. DDI E does not support reversal.</p>	Value	Name	0b	Not reversed	1b	Reversed			
Value	Name										
0b	Not reversed										
1b	Reversed										
	15:8	<p>Reserved</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 75%;">Format:</td><td style="width: 25%;">MBZ</td></tr> </table>	Format:	MBZ							
Format:	MBZ										
	7	<p>DDI Idle Status Access: RO This bit indicates when the DDI buffer is idle.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center; background-color: #e0e0ff;">Value</th><th style="text-align: center; background-color: #e0e0ff;">Name</th></tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td><td>Buffer Not Idle</td></tr> <tr> <td style="text-align: center;">1b</td><td>Buffer Idle</td></tr> </tbody> </table>	Value	Name	0b	Buffer Not Idle	1b	Buffer Idle			
Value	Name										
0b	Buffer Not Idle										
1b	Buffer Idle										
	6:5	<p>Reserved</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 75%;">Format:</td><td style="width: 25%;">MBZ</td></tr> </table>	Format:	MBZ							
Format:	MBZ										
	4	<p>DDIA Lane Capability Control This bit selects how lanes are shared between DDI A and DDI E. This field is only used in the DDI A instance of this register. See the DDI A and DDI E lane mapping table in the Introduction section.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center; background-color: #e0e0ff;">Value</th><th style="text-align: center; background-color: #e0e0ff;">Name</th><th style="text-align: center; background-color: #e0e0ff;">Description</th></tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td><td>DDIA x2</td><td>DDI A supports 2 lanes and DDI E supports 2 lanes</td></tr> <tr> <td style="text-align: center;">1b</td><td>DDIA x4</td><td>DDI A supports 4 lanes and DDI E is not used</td></tr> </tbody> </table> <p>Restriction This field must be programmed at system boot based on board configuration and may not be changed afterwards.</p>	Value	Name	Description	0b	DDIA x2	DDI A supports 2 lanes and DDI E supports 2 lanes	1b	DDIA x4	DDI A supports 4 lanes and DDI E is not used
Value	Name	Description									
0b	DDIA x2	DDI A supports 2 lanes and DDI E supports 2 lanes									
1b	DDIA x4	DDI A supports 4 lanes and DDI E is not used									

DDI_BUF_CTL																										
	3:1	<p>DP Port Width Selection</p> <table border="1"> <thead> <tr> <th colspan="3">Description</th> </tr> </thead> <tbody> <tr> <td colspan="2">This bit selects the number of lanes to be enabled on the DDI link for DisplayPort or FDI.</td><td></td></tr> <tr> <td colspan="2">This field is ignored for HDMI and DVI which always use all 4 lanes.</td><td></td></tr> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> <tr> <td>000b</td><td>x1</td><td>x1 Mode</td></tr> <tr> <td>001b</td><td>x2</td><td>x2 Mode</td></tr> <tr> <td>011b</td><td>x4</td><td>x4 Mode (not allowed with DDI E, some restrictions with DDI A)</td></tr> <tr> <td>Others</td><td>Reserved</td><td>Reserved</td></tr> </tbody> </table> <p>Restriction</p> <p>When in DisplayPort or FDI modes the value selected here must match the value selected in the DDI Buffer Control register for the DDI attached to this pipe.</p> <p>This field must not be changed while the DDI is enabled. DDI E only supports x1 and x2 when DDI_BUF_CTL_A DDIA Lane Capability Control is set to DDIA x2, otherwise DDI E is not supported. DDI A (EDP) supports x1, x2, and x4 when DDI_BUF_CTL_A DDIA Lane Capability Control is set to DDIA x4, otherwise DDI A only supports x1 and x2.</p>	Description			This bit selects the number of lanes to be enabled on the DDI link for DisplayPort or FDI.			This field is ignored for HDMI and DVI which always use all 4 lanes.			Value	Name	Description	000b	x1	x1 Mode	001b	x2	x2 Mode	011b	x4	x4 Mode (not allowed with DDI E, some restrictions with DDI A)	Others	Reserved	Reserved
Description																										
This bit selects the number of lanes to be enabled on the DDI link for DisplayPort or FDI.																										
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Value	Name	Description																								
000b	x1	x1 Mode																								
001b	x2	x2 Mode																								
011b	x4	x4 Mode (not allowed with DDI E, some restrictions with DDI A)																								
Others	Reserved	Reserved																								
	0	<p>Init Display Detected</p> <table border="1"> <tr> <td>Access:</td><td>RO</td></tr> <tr> <td colspan="2">Strap indicating whether a display was detected on this port during initialization. It signifies the level of the port detect pin at boot. This bit is only informative. It does not prevent this port from being enabled in hardware. This field only indicates the DDIA detection. Detection for other ports is read from SFUSE_STRAP.</td></tr> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> <tr> <td>0b</td><td>Not Detected</td><td>Digital display not detected during initialization</td></tr> <tr> <td>1b</td><td>Detected</td><td>Digital display detected during initialization</td></tr> </table>	Access:	RO	Strap indicating whether a display was detected on this port during initialization. It signifies the level of the port detect pin at boot. This bit is only informative. It does not prevent this port from being enabled in hardware. This field only indicates the DDIA detection. Detection for other ports is read from SFUSE_STRAP.		Value	Name	Description	0b	Not Detected	Digital display not detected during initialization	1b	Detected	Digital display detected during initialization											
Access:	RO																									
Strap indicating whether a display was detected on this port during initialization. It signifies the level of the port detect pin at boot. This bit is only informative. It does not prevent this port from being enabled in hardware. This field only indicates the DDIA detection. Detection for other ports is read from SFUSE_STRAP.																										
Value	Name	Description																								
0b	Not Detected	Digital display not detected during initialization																								
1b	Detected	Digital display detected during initialization																								

DDI_BUF_TRANS

DDI_BUF_TRANS	
Register Space:	MMIO: 0/2/0
Project:	BDW 0x00FFFFFFh, 0006000E [BDW]
Access:	R/W
Size (in bits):	64
Address:	64E00h-64E4Fh
Name:	DDI A Buffer Translation
ShortName:	DDI_BUF_TRANS_A_*
Valid Projects:	BDW
Power:	Always on
Reset:	global
Address:	64E60h-64EAfh
Name:	DDI B Buffer Translation
ShortName:	DDI_BUF_TRANS_B_*
Valid Projects:	BDW
Power:	Always on
Reset:	global
Address:	64EC0h-64F0Fh
Name:	DDI C Buffer Translation
ShortName:	DDI_BUF_TRANS_C_*
Valid Projects:	BDW
Power:	Always on
Reset:	global
Address:	64F20h-64F6Fh
Name:	DDI D Buffer Translation
ShortName:	DDI_BUF_TRANS_D_*
Valid Projects:	BDW
Power:	Always on
Reset:	global
Address:	64F80h-64FCFh
Name:	DDI E Buffer Translation
ShortName:	DDI_BUF_TRANS_E_*
Valid Projects:	BDW
Power:	Always on
Reset:	global

DDI_BUF_TRANS

Description

These registers define the DDI buffer settings required for different voltage swing and emphasis selections. In HDMI or DVI mode the HDMI/DVI translation registers are automatically selected.

In DisplayPort or FDI mode the DDI Buffer Control register programming will select which of these registers is used to drive the buffer. For each DDI A/B/C/D/E there are 10 instances of this 2 DWord register format. The first 9 instances (18 Dwords) are entries 0-8 which are used for DisplayPort and FDI. The last instance (2 Dwords) is entry 9 which is used for HDMI and DVI.

Programming Notes

The recommended values are listed below this table.

Restriction

These registers must be programmed with valid values prior to enabling DDI_BUF_CTL.

DWord	Bit	Description							
0	31	Balance Leg Enable This field controls the Balance Leg enable for the DDI buffer. <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th><th style="text-align: center;">Name</th></tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td><td>Disable</td></tr> <tr> <td style="text-align: center;">1b</td><td>Enable</td></tr> </tbody> </table>		Value	Name	0b	Disable	1b	Enable
Value	Name								
0b	Disable								
1b	Enable								
30:24	Reserved <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Project:</td><td style="width: 50%;">BDW</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>		Project:	BDW	Format:	MBZ			
Project:	BDW								
Format:	MBZ								
23:0	DeEmp Level Default Value: FFFFFFh Project: BDW This field controls the De-emphasis level for the DDI buffer.								
1	31:21	Reserved <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Format:</td><td style="width: 50%;">MBZ</td></tr> </table>		Format:	MBZ				
Format:	MBZ								
20:16	VRef Sel This field controls the voltage reference select for the DDI buffer. <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th><th style="text-align: center;">Name</th><th style="text-align: center;">Project</th></tr> </thead> <tbody> <tr> <td style="text-align: center;">00110b</td><td>[Default]</td><td>BDW</td></tr> </tbody> </table>		Value	Name	Project	00110b	[Default]	BDW	
Value	Name	Project							
00110b	[Default]	BDW							
15:5	Reserved <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Project:</td><td style="width: 50%;">BDW</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>		Project:	BDW	Format:	MBZ			
Project:	BDW								
Format:	MBZ								

DDI_BUF_TRANS		
	4:0	Vswing
Default Value:		01110b
Project:		BDW
This field controls the voltage swing for the DDI buffer.		

DE_PIPE_INTERRUPT

DE_PIPE_INTERRUPT		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	44400h-4440Fh	
Name:	Display Engine Pipe A Interrupts	
ShortName:	DE_PIPE_INTERRUPT_A	
Valid Projects:	BDW	
Power:	Always on	
Reset:	soft	
Address:	44410h-4441Fh	
Name:	Display Engine Pipe B Interrupts	
ShortName:	DE_PIPE_INTERRUPT_B	
Valid Projects:	BDW	
Power:	off/on	
Reset:	soft	
Address:	44420h-4442Fh	
Name:	Display Engine Pipe C Interrupts	
ShortName:	DE_PIPE_INTERRUPT_C	
Valid Projects:	BDW	
Power:	off/on	
Reset:	soft	
Description		
This table indicates which events are mapped to each bit of the Display Engine Pipe Interrupt registers. The IER enabled Display Engine Pipe Interrupt IIR (sticky) bits are ORed together to generate the DE_Pipe Interrupts Pending bit in the Master Interrupt Control register. There is one full set of Display Engine Pipe interrupts per display pipes A/B/C. The STEREO3D_EVENT_MASK selects between left eye and right eye reporting of vertical blank, vertical sync, and scanline events in stereo 3D modes.		
0x44400 = ISR A, 0x44410 = ISR B, 0x44420 = ISR C 0x44404 = IMR A, 0x44414 = IMR B, 0x44424 = IMR C 0x44408 = IIR A, 0x44418 = IIR B, 0x44428 = IIR C 0x4440C = IER A, 0x4441C = IER B, 0x4442C = IER C		
DWord	Bit	Description
0	31	Underrun The ISR is an active high pulse when there is an underrun on the transcoder attached to this pipe.

DE_PIPE_INTERRUPT

		Unused_Int_30				
	30	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Project:</td> <td style="padding: 2px;">BDW</td> </tr> <tr> <td colspan="2" style="padding: 2px;">These interrupts are currently unused.</td> </tr> </table>	Project:	BDW	These interrupts are currently unused.	
Project:	BDW					
These interrupts are currently unused.						
Reserved						
	28	Reserved				
	27:13	Unused_Int_27_13 <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Project:</td> <td style="padding: 2px;">BDW</td> </tr> <tr> <td colspan="2" style="padding: 2px;">These interrupts are currently unused.</td> </tr> </table>	Project:	BDW	These interrupts are currently unused.	
Project:	BDW					
These interrupts are currently unused.						
	12	DPST_Histogram_event The ISR is an active high pulse on the DPST Histogram event on this pipe.				
	11	Unused_Int_11 <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Project:</td> <td style="padding: 2px;">BDW</td> </tr> <tr> <td colspan="2" style="padding: 2px;">These interrupts are currently unused.</td> </tr> </table>	Project:	BDW	These interrupts are currently unused.	
Project:	BDW					
These interrupts are currently unused.						
	10	Cursor_GTT_Fault_Status <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Project:</td> <td style="padding: 2px;">BDW</td> </tr> <tr> <td colspan="2" style="padding: 2px;">The ISR is an active high pulse when a GTT fault is detected for the cursor on this pipe.</td> </tr> </table>	Project:	BDW	The ISR is an active high pulse when a GTT fault is detected for the cursor on this pipe.	
Project:	BDW					
The ISR is an active high pulse when a GTT fault is detected for the cursor on this pipe.						
	9	Sprite_GTT_Fault_Status <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Project:</td> <td style="padding: 2px;">BDW</td> </tr> <tr> <td colspan="2" style="padding: 2px;">The ISR is an active high pulse when a GTT fault is detected for the sprite on this pipe.</td> </tr> </table>	Project:	BDW	The ISR is an active high pulse when a GTT fault is detected for the sprite on this pipe.	
Project:	BDW					
The ISR is an active high pulse when a GTT fault is detected for the sprite on this pipe.						
	8	Primary_GTT_Fault_Status <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Project:</td> <td style="padding: 2px;">BDW</td> </tr> <tr> <td colspan="2" style="padding: 2px;">The ISR is an active high pulse when a GTT fault is detected for the primary plane on this pipe.</td> </tr> </table>	Project:	BDW	The ISR is an active high pulse when a GTT fault is detected for the primary plane on this pipe.	
Project:	BDW					
The ISR is an active high pulse when a GTT fault is detected for the primary plane on this pipe.						
	7:6	Unused_Int_7_6 <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Project:</td> <td style="padding: 2px;">BDW</td> </tr> <tr> <td colspan="2" style="padding: 2px;">These interrupts are currently unused.</td> </tr> </table>	Project:	BDW	These interrupts are currently unused.	
Project:	BDW					
These interrupts are currently unused.						
	5	Sprite_Flip_Done <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Project:</td> <td style="padding: 2px;">BDW</td> </tr> <tr> <td colspan="2" style="padding: 2px;">The ISR is an active high pulse when the flip is done for the sprite plane on this pipe.</td> </tr> </table>	Project:	BDW	The ISR is an active high pulse when the flip is done for the sprite plane on this pipe.	
Project:	BDW					
The ISR is an active high pulse when the flip is done for the sprite plane on this pipe.						
	4	Primary_Flip_Done <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Project:</td> <td style="padding: 2px;">BDW</td> </tr> <tr> <td colspan="2" style="padding: 2px;">The ISR is an active high pulse when the flip is done for the primary plane on this pipe.</td> </tr> </table>	Project:	BDW	The ISR is an active high pulse when the flip is done for the primary plane on this pipe.	
Project:	BDW					
The ISR is an active high pulse when the flip is done for the primary plane on this pipe.						

DE_PIPE_INTERRUPT			
	3	Unused_Int_3	
		Project:	BDW
		These interrupts are currently unused.	
	2	Scan_Line_Event	The ISR is an active high pulse on the scan line event of the transcoder attached to this pipe.
	1	Vsync	The ISR is an active high level for the duration of the vertical sync of the transcoder attached to this pipe.
	0	Vblank	The ISR is an active high level for the duration of the vertical blank of the transcoder attached to this pipe.

DE_RR_DEST

DE_RR_DEST									
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x00000000 Access: R/W Size (in bits): 32									
Address: 44058h-4405Bh Name: Render Response Destination ShortName: DE_RR_DEST Valid Projects: BDW Power: Always on Reset: soft									
This register selects the destination of certain render responses that may go to CS, BCS, or both. In order for a response to be sent to a particular destination, the event must occur, the event must be unmasked, and that destination must be selected.									
DWord	Bit	Description							
0	31:6	Reserved <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	BDW	Format:	MBZ			
Project:	BDW								
Format:	MBZ								
5:4	Pipe C Vertical Blank Destination This field selects the destination for the render response sent on pipe C start of vertical blank. <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>00b</td><td>CS</td></tr> <tr> <td>01b</td><td>BCS</td></tr> <tr> <td>10b,11b</td><td>Both CS and BCS</td></tr> </tbody> </table>	Value	Name	00b	CS	01b	BCS	10b,11b	Both CS and BCS
Value	Name								
00b	CS								
01b	BCS								
10b,11b	Both CS and BCS								
3:2	Pipe B Vertical Blank Destination This field selects the destination for the render response sent on pipe B start of vertical blank. <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>00b</td><td>CS</td></tr> <tr> <td>01b</td><td>BCS</td></tr> <tr> <td>10b,11b</td><td>Both CS and BCS</td></tr> </tbody> </table>	Value	Name	00b	CS	01b	BCS	10b,11b	Both CS and BCS
Value	Name								
00b	CS								
01b	BCS								
10b,11b	Both CS and BCS								

DE_RR_DEST

1:0

Pipe A Vertical Blank Destination

This field selects the destination for the render response sent on pipe A start of vertical blank.

Value	Name
00b	CS
01b	BCS
10b,11b	Both CS and BCS

DE_RRMR

DE_RRMR			
Register Space:	MMIO: 0/2/0		
Project:	BDW		
Default Value:	0x00000000		
Access:	R/W		
Size (in bits):	32		
Address:	44050h-44053h		
Name:	Render Response Mask		
ShortName:	DE_RRMR		
Power:	Always on		
Reset:	soft		
<p>See the render response message definition table to find the source event for each bit. The render response message is sent from the display engine to the render command streamer (CS) or blitter command streamer (BCS). The message is used to inform CS and BCS of certain display events. This register is used to control which render response message bits are masked or unmasked. Unmasked bits will cause a render response message to be sent and will be reported in that message. Unmasked bits will not be reported and will not cause a render response message to be sent. Vertical blank events occur periodically while the associated display pipe timing generator is running and will be reported in a render response to CS or BCS (depending on DE_RR_DEST destination selection) if un-masked here. Scanline events occur after they have been initiated through MMIO writes or LRI to the Display Load Scan Lines register. A flip event will be reported in a render response to CS if un-masked here and the Display Load Scanline source is CS. A flip event will be reported in a render response to BCS if un-masked here and the Display Load Scanline source is BCS. Flip done events occur after they have been initiated through MI_DISPLAY_FLIP or MMIO write to plane surface address registers. A flip event will be reported in a render response to CS if un-masked here and the flip source is CS. A flip event will be reported in a render response to BCS if un-masked here and the flip source is BCS.</p>			
Programming Notes			
<p>Programming this register can be done through MMIO or a command streamer LOAD_REGISTER_IMMEDIATE (LRI) command. When using LRI care must be taken to follow all the programming rules for LRI targeting the display engine. Unmasked events will wake GT as they occur, so for improved power savings it is recommended to only unmask events that are required.</p>			
Restriction			
<p>Events must be unmasked prior to waiting for them with a MI_WAIT_FOR_EVENT ring command, or in the case of flips or scanlines, prior to starting the flip or loading the scanline.</p>			
DWord	Bit	Description	
0	31:30	Reserved	Format: MBZ

DE_RRMR																			
	29:0	DE RRMR																	
Format: Display Engine Render Response Message Definition																			
This field contains a bit mask which selects which events cause and are reported in the render response message.																			
<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th colspan="2">Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Not Masked</td><td colspan="2">Not Masked - will cause a message to be sent and will be reported in that message</td></tr> <tr> <td>1b</td><td>Masked</td><td colspan="2">Masked - will not cause a message to be sent or be reported in a message</td></tr> <tr> <td>2070EF2Fh</td><td>All Masked [Default]</td><td colspan="2"></td></tr> </tbody> </table>				Value	Name	Description		0b	Not Masked	Not Masked - will cause a message to be sent and will be reported in that message		1b	Masked	Masked - will not cause a message to be sent or be reported in a message		2070EF2Fh	All Masked [Default]		
Value	Name	Description																	
0b	Not Masked	Not Masked - will cause a message to be sent and will be reported in that message																	
1b	Masked	Masked - will not cause a message to be sent or be reported in a message																	
2070EF2Fh	All Masked [Default]																		

DE Misc Interrupt Definition

DE Misc Interrupt Definition					
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x00000000 Size (in bits): 32					
Address: 44460h-4446Fh Name: Display Engine Miscellaneous Interrupts ShortName: DE_MISC_INTERRUPT Valid Projects: BDW Power: Always on Reset: soft					
This table indicates which events are mapped to each bit of the Display Engine Miscellaneous Interrupt registers. 0x44460 = ISR 0x44464 = IMR 0x44468 = IIR 0x4446C = IER					
DWord	Bit	Description			
0	31	Poison The ISR is an active high pulse on receiving the poison response to a memory transaction.			
	30	Reserved <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	BDW	Format:
Project:	BDW				
Format:	MBZ				
29	Invalid_GTT_page_table_entry <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> </table> The ISR is an active high pulse on receiving the iMPH invalid GTT page table entry indication.	Project:	BDW		
Project:	BDW				
28	Invalid_page_table_entry_data <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> </table> The ISR is an active high pulse on receiving the iMPH invalid page table entry data indication.	Project:	BDW		
Project:	BDW				
27	GSE <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> </table> The ISR is an active high pulse on the GSE system level event.	Project:	BDW		
Project:	BDW				
26	Reserved <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	BDW	Format:	MBZ
Project:	BDW				
Format:	MBZ				
25	Reserved				

DE Misc Interrupt Definition

	24	Reserved					
	23	WD0_Interrupts_Combined	The ISR is an active high level while any of the WD0_IIR bits are set.				
	22	SVM Device Mode PRQ Event	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Project:</td> <td style="padding: 2px; text-align: right;">BDW</td> </tr> </table> <p>The ISR is an active high pulse on receiving the iMPH SVM Device Mode PRQ event indication. This event indicates that a GT advanced context encountered a recoverable page fault.</p>	Project:	BDW		
Project:	BDW						
	21	SVM Device Mode VTD Fault	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Project:</td> <td style="padding: 2px; text-align: right;">BDW</td> </tr> </table> <p>The ISR is an active high pulse on receiving the iMPH SVM Device Mode VT-d fault indication. This event indicates GT encountered a non-recoverable translation fault.</p>	Project:	BDW		
Project:	BDW						
	20	SVM Device Mode Wait Descriptor Completion	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Project:</td> <td style="padding: 2px; text-align: right;">BDW</td> </tr> </table> <p>The ISR is an active high pulse on receiving the iMPH SVM Device Mode Wait Descriptor Completion indication. This event indicates that IMPH completed Invalidation Wait Descriptor.</p>	Project:	BDW		
Project:	BDW						
	19	SRD_Interrupts_Combined	The ISR is an active high level while any of the SRD_IIR bits are set.				
	18	Reserved	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Project:</td> <td style="padding: 2px; text-align: right;">BDW</td> </tr> <tr> <td style="padding: 2px;">Format:</td> <td style="padding: 2px; text-align: right;">MBZ</td> </tr> </table>	Project:	BDW	Format:	MBZ
Project:	BDW						
Format:	MBZ						
	17:16	Reserved	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Format:</td> <td style="padding: 2px; text-align: right;">MBZ</td> </tr> </table>	Format:	MBZ		
Format:	MBZ						
	15	GTC_CPU_Interrupts_Combined	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Project:</td> <td style="padding: 2px; text-align: right;">BDW</td> </tr> </table> <p>The ISR is an active high level while any of the GTC_CPU_IIR bits are set.</p>	Project:	BDW		
Project:	BDW						
	14:9	Reserved	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Format:</td> <td style="padding: 2px; text-align: right;">MBZ</td> </tr> </table>	Format:	MBZ		
Format:	MBZ						
	7:1	Reserved	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Format:</td> <td style="padding: 2px; text-align: right;">MBZ</td> </tr> </table>	Format:	MBZ		
Format:	MBZ						

DE Port Interrupt Definition

DE Port Interrupt Definition				
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x00000000 Size (in bits): 32				
Address: 44440h-4444Fh Name: Display Engine Port Interrupts ShortName: DE_PORT_INTERRUPT Valid Projects: BDW Power: Always on Reset: soft				
This table indicates which events are mapped to each bit of the Display Engine Port Interrupt registers. 0x44440 = ISR 0x44444 = IMR 0x44448 = IIR 0x4444C = IER				
DWord	Bit	Description		
0	31:30	Reserved <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> </table>	Project:	BDW
Project:	BDW			
29	Reserved <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> </table>	Project:	BDW	
Project:	BDW			
28	Reserved <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> </table>	Project:	BDW	
Project:	BDW			
9:8	Reserved <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> </table>	Project:	BDW	
Project:	BDW			
27:4	Reserved <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> </table>	Project:	BDW	
Project:	BDW			
3	DisplayPort_A_Hotplug <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> </table> <p>The ISR gives the live state of the Digital Port A HPD pin when the HPD input is enabled. The IIR is set if a short or long pulse is detected when HPD input is enabled.</p>	Project:	BDW	
Project:	BDW			
2	Reserved			
1	Reserved <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> </table>	Project:	BDW	
Project:	BDW			
0	AUX_Channel_A <p>The ISR is an active high pulse on the AUX DDI A done event. This event will not occur for SRD AUX done.</p>			

Depth/Early Depth TLB Partitioning Register

ZSHR - Depth/Early Depth TLB Partitioning Register

Register Space: MMIO: 0/2/0

Project: BDW

Source: RenderCS

Default Value: 0x00000020

Access: R/W

Size (in bits): 32

Trusted Type: 1

Address: 04050h

This register is used to determine the number of TLB entries from the total of 64 available to be used by the Depth partition of the TLB. The rest of the entries are used for the Early Depth/Stencil TLB.

DWord	Bit	Description	
0	31:6	Reserved	
	5:0	Number of TLB Entries Out of 64 used for Depth TLB Default Value: 32 The rest are be used for Early Depth/Stencil TLB. Default value is 32.	MBZ

Device Capabilities

DEVCAP - Device Capabilities					
DWord	Bit	Description			
0	31:29	Reserved <table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ	
Format:	MBZ				
28	Function Level Reset <table border="1"> <tr> <td>Default Value:</td><td>1b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>dHDA supports FLR capability.</p>	Default Value:	1b	Access:	RO
Default Value:	1b				
Access:	RO				
27:26	Captured Slot Power Limit Scale <table border="1"> <tr> <td>Default Value:</td><td>00b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Hardwired to 0.</p>	Default Value:	00b	Access:	RO
Default Value:	00b				
Access:	RO				
25:18	Captured Slot Power Limit Value <table border="1"> <tr> <td>Default Value:</td><td>00h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Hardwired to 0.</p>	Default Value:	00h	Access:	RO
Default Value:	00h				
Access:	RO				
17:15	Reserved <table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ		
Format:	MBZ				
14	Power Indicator Present <table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Hardwired to 0.</p>	Default Value:	0b	Access:	RO
Default Value:	0b				
Access:	RO				
13	Attention Indicator Present <table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Hardwired to 0.</p>	Default Value:	0b	Access:	RO
Default Value:	0b				
Access:	RO				

DEVCAP - Device Capabilities						
	12	Reserved Format: MBZ				
	11:9	Endpoint L1 Acceptable Latency Default Value: 111b Access: RO				
	Programming Notes					
	Max value not valid.					
	8:6	Endpoint L0s Acceptable Latency Default Value: 111b Access: RO				
	Programming Notes					
	Max value not valid.					
	5	Extended Tag Field Support Default Value: 0b Access: RO Indicates 5 bit tag supported.				
	4:3	Phantom Functions Supported Default Value: 00b Access: RO Phantom functions unsupported.				
	2:0	Max Payload Size Supported Access: RO				
	<table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>000b</td><td></td></tr> </tbody> </table>		Value	Name	000b	
Value	Name					
000b						
	Programming Notes					
	128B maximum payload size capability.					

Device Control and Status

DEVC_DEVS - Device Control and Status						
DWord	Bit	Description				
0	31:22	Reserved <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ		
Format:	MBZ					
	21	Transactions Pending <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>A 1 indicates that the dHDA has issued Non-Posted requests which have not been completed. A 0 indicates that Completions for all Non-Posted Requests have been received.</p>	Default Value:	0b	Access:	RO
Default Value:	0b					
Access:	RO					
	20	AUX Power Detected <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Hardwired to 0 (no AUX power source).</p>	Default Value:	0b	Access:	RO
Default Value:	0b					
Access:	RO					
	19	Unsupported Request Detected <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Not implemented.</p>	Default Value:	0b	Access:	RO
Default Value:	0b					
Access:	RO					
	18	Fatal Error Detected <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Not implemented.</p>	Default Value:	0b	Access:	RO
Default Value:	0b					
Access:	RO					
	17	Non-Fatal Error Detected <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Not implemented.</p>	Default Value:	0b	Access:	RO
Default Value:	0b					
Access:	RO					

DEVC_DEVS - Device Control and Status

DEVC_DEVS - Device Control and Status						
16	Correctable Error Detected	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Default Value:</td><td style="padding: 2px;">0b</td></tr> <tr> <td style="padding: 2px;">Access:</td><td style="padding: 2px;">RO</td></tr> </table> <p>Not implemented.</p>	Default Value:	0b	Access:	RO
Default Value:	0b					
Access:	RO					
15	Initiate FLR	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Default Value:</td><td style="padding: 2px;">0b</td></tr> <tr> <td style="padding: 2px;">Access:</td><td style="padding: 2px;">R/W</td></tr> </table> <p>When set, initiates function level reset. Value stays as '1' until FLR complete, at which point the value transitions back to '0'. Writes of '0' have no effect.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
14:12	Max Read Request Size	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Default Value:</td><td style="padding: 2px;">000b</td></tr> <tr> <td style="padding: 2px;">Access:</td><td style="padding: 2px;">RO</td></tr> </table> <p>Hardwired to 000 enabling 128 B maximum read request size.</p>	Default Value:	000b	Access:	RO
Default Value:	000b					
Access:	RO					
11	No Snoop Enable	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Default Value:</td><td style="padding: 2px;">1b</td></tr> <tr> <td style="padding: 2px;">Access:</td><td style="padding: 2px;">R/W</td></tr> </table> <p>When set, dHDA may use non-snooped transactions where appropriate. Not affected by FLR.</p>	Default Value:	1b	Access:	R/W
Default Value:	1b					
Access:	R/W					
10	Auxiliary Power PM Enable	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Default Value:</td><td style="padding: 2px;">0b</td></tr> <tr> <td style="padding: 2px;">Access:</td><td style="padding: 2px;">RO</td></tr> </table> <p>dHDA does not draw AUX power.</p>	Default Value:	0b	Access:	RO
Default Value:	0b					
Access:	RO					
9	Phantom Functions Enable	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Default Value:</td><td style="padding: 2px;">0b</td></tr> <tr> <td style="padding: 2px;">Access:</td><td style="padding: 2px;">RO</td></tr> </table> <p>Hardwired to 0.</p>	Default Value:	0b	Access:	RO
Default Value:	0b					
Access:	RO					
8	Extended Tag Field Enable	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Default Value:</td><td style="padding: 2px;">0b</td></tr> <tr> <td style="padding: 2px;">Access:</td><td style="padding: 2px;">RO</td></tr> </table> <p>Hardwired to 0.</p>	Default Value:	0b	Access:	RO
Default Value:	0b					
Access:	RO					
7:5	Max Payload Size	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Default Value:</td><td style="padding: 2px;">00b</td></tr> <tr> <td style="padding: 2px;">Access:</td><td style="padding: 2px;">RO</td></tr> </table> <p>Hardwired to 000 indicating 128B.</p>	Default Value:	00b	Access:	RO
Default Value:	00b					
Access:	RO					

DEVC_DEVS - Device Control and Status		
	4	Enable Relaxed Ordering Default Value: 0b Access: RO Hardwired to 0.
	3	Unsupported Request Reporting Enable Default Value: 0b Access: R/W Not implemented. This bit is RW for PCIe compliance.
	2	Fatal Error Reporting Enable Default Value: 0b Access: R/W Not implemented. This bit is RW for PCIe compliance.
	1	Non-Fatal Error Reporting Enable Default Value: 0b Access: R/W Not implemented. This bit is RW for PCIe compliance.
	0	Correctable Error Reporting Enable Default Value: 0b Access: R/W Not implemented. This bit is RW for PCIe compliance.

Device Enable

DEVEN_0_0_0_PCI - Device Enable			
DWord	Bit	Description	
0	14	Chap Enable	
		Default Value:	0b
		Access:	R/W Lock
	13:8	Reserved	
		Format:	MBZ
	7	Device 4 Enable	
		Default Value:	1b
		Access:	R/W Lock
	6	Reserved	
		Format:	MBZ
5	Device 3 enable for Display HD Audio		
		Default Value:	1b
4	4	Access:	R/W Lock
		0: Bus 0 Device 3 is disabled and hidden 1: Bus 0 Device 3 is enabled and visible This bit will be set to 0b and remain 0b if Device 3 capability is disabled.	
	3	Internal Graphics Engine	
		Default Value:	1b
	2	Access:	R/W Lock
		0: Bus 0 Device 2 is disabled and hidden 1: Bus 0 Device 2 is enabled and visible This bit will be set to 0b and remain 0b if Device 2 capability is disabled.	
	3	PEG10 Enable	
		Default Value:	1b
	2	Access:	R/W Lock
		PEG11 Enable	
		Default Value:	1b
		Access:	R/W Lock

DEVEN_0_0_0_PCI - Device Enable			
1	PEG12 Enable	Default Value:	1b
		Access:	R/W Lock
0	Host Bridge	Default Value:	1b
		Access:	RO

Device Identification

DID2_0_2_0_PCI - Device Identification						
DWord	Bit	Description				
0	15:4	<p>Device Identification Number MSB</p> <table border="1"> <tr> <td>Default Value:</td><td>000101100000b</td></tr> <tr> <td>Access:</td><td>R/W Firmware Only</td></tr> </table> <p>This is the upper part of a 16 bit value assigned to the device.</p>	Default Value:	000101100000b	Access:	R/W Firmware Only
Default Value:	000101100000b					
Access:	R/W Firmware Only					
3:2	<p>Device Identification Number SKU</p> <table border="1"> <tr> <td>Default Value:</td><td>00b</td></tr> <tr> <td>Access:</td><td>RO Variant</td></tr> </table> <p>These are bits 3:2 of the 16 bit value assigned to the device.</p>	Default Value:	00b	Access:	RO Variant	
Default Value:	00b					
Access:	RO Variant					
1:0	<p>Device Identification Number LSB</p> <table border="1"> <tr> <td>Default Value:</td><td>10b</td></tr> <tr> <td>Access:</td><td>RO Variant</td></tr> </table> <p>This is the lower part of a 16 bit value assigned to the device.</p>	Default Value:	10b	Access:	RO Variant	
Default Value:	10b					
Access:	RO Variant					

Display HD Audio Lower Base Address

DHDALBAR - Display HD Audio Lower Base Address							
Register Space: PCI: 0/3/0 Project: BDW Default Value: 0x00000004 Access: R/W Size (in bits): 32							
Address: 00010h-00013h Power: Always on Reset: global							
DWord	Bit	Description					
0	31:14	Lower Base Address	<table border="1"> <tr> <td>Default Value:</td><td>0000h</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Lower Base Address (MBA): Base address for the Intel HD Audio controller's memory mapped configuration registers. 16 Kbytes are requested by hardwiring bits 13:4 to 0's.</p>	Default Value:	0000h	Access:	R/W
Default Value:	0000h						
Access:	R/W						
13:4	ADM	<table border="1"> <tr> <td>Default Value:</td><td>0000000000b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Hardwired to 0.</p>	Default Value:	0000000000b	Access:	RO	
Default Value:	0000000000b						
Access:	RO						
3	Prefetchable	<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Indicates that this BAR is NOT prefetchable.</p>	Default Value:	0b	Access:	RO	
Default Value:	0b						
Access:	RO						
2:1	Address Range	<table border="1"> <tr> <td>Default Value:</td><td>10b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Indicates that this BAR can be located anywhere in 64-bit address space.</p>	Default Value:	10b	Access:	RO	
Default Value:	10b						
Access:	RO						
0	Space Type	<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Indicates that this BAR is located in memory space.</p>	Default Value:	0b	Access:	RO	
Default Value:	0b						
Access:	RO						

Display HD Audio Upper Base Address

DHDAUBAR - Display HD Audio Upper Base Address						
DWord	Bit	Description				
0	31:0	<p>Upper Base Address</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Upper 32 bits of the Base address for the Intel HD Audio controller's memory mapped configuration registers.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

Display Message Forward Status Register

DISPLAY_MESSAGE_FORWARD_STATUS - Display Message Forward Status Register		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000 [BDW]	
Access:	R/W	
Size (in bits):	32	
Address:	022E8h	
Name:	RCS Display Message Forward Status Register	
ShortName:	RCS_DISPLAY_MESSAGE_FORWARD_STATUS	
Address:	122E8h-122EBh	
Name:	Display Message Forward Status Register	
ShortName:	DISPLAY_MESSAGE_FORWARD_STATUS_VCSUNIT0	
Address:	1A2E8h-1A2EBh	
Name:	Display Message Forward Status Register	
ShortName:	DISPLAY_MESSAGE_FORWARD_STATUS_VECSUNIT	
Address:	1C2E8h-1C2EBh	
Name:	Display Message Forward Status Register	
ShortName:	DISPLAY_MESSAGE_FORWARD_STATUS_VCSUNIT1	
Address:	222E8h	
Name:	BCS Display Message Forward Status Register	
ShortName:	BCS_DISPLAY_MESSAGE_FORWARD_STATUS	
This register stores the internal HW status flags related to display message forward logic. This register should not be accessed by SW. This register is part of power context image. Note: Even though this register exists in VideoCS and VideoEnhancementCS, individual bit driven functionality is not supported.		
DWord	Bit	Description
0	31:30	Reserved
		Source: RenderCS, BlitterCS
		Format: MBZ
	29:28	Reserved
	27:26	Reserved
	25:24	
	23:22	
	21:20	
	19:18	

DISPLAY_MESSAGE_FORWARD_STATUS - Display Message Forward Status Register

17:16	
15:14	
13:12	
11:10	
9:8	
7:6	
5:4	
3:2	
1:0	

DMA Position in Buffer

DPIB - DMA Position in Buffer		
Register Space: MMIO: 0/3/0 Project: BDW Default Value: 0x00000000 Access: RO Variant Size (in bits): 32		
Address: 01084h-01087h Name: Position in Buffer for DMA1 ShortName: DPIB_1		
Address: 010A4h-010A7h Name: Position in Buffer for DMA2 ShortName: DPIB_2		
Address: 010C4h-010C7h Name: Position in Buffer for DMA3 ShortName: DPIB_3		
DWord	Bit	Description
0	31:0	DMA Position in Buffer <div style="border: 1px solid black; padding: 2px;"> Default Value: 00h </div> <p>Indicates the number of bytes "processed" by the corresponding DMA engine from the beginning of the BDL.</p>

DMA Position Lower Base Address

DPLBASE - DMA Position Lower Base Address											
DWord	Bit	Description									
0	31:7	<p>DMA Position Lower Base Address</p> <table border="1"> <tr> <td>Default Value:</td> <td>0000000h</td> </tr> </table> <p>Lower 32 bits of the DMA Position Buffer Base Address. This register field must not be written when any DMA engine is running or the DMA transfer may be corrupted. This same address is used by the Flush Control, and must be programmed with a valid value before the FLCNRTL bit is set.</p>	Default Value:	0000000h							
Default Value:	0000000h										
	6:1	<p>DPLBASE LOWER BITS</p> <table border="1"> <tr> <td>Default Value:</td> <td>0h</td> </tr> </table> <p>DPIB Lower Base Address Unimplemented Bits: Hardwired to 0 to force 128-byte buffer alignment for cache line fetch optimizations. These are RO bits.</p>	Default Value:	0h							
Default Value:	0h										
	0	<p>DMA Position Buffer Enable</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disable [Default]</td> <td>See ProgramminNotes</td> </tr> <tr> <td>1b</td> <td>Enable</td> <td>See ProgramminNotes</td> </tr> </tbody> </table> <p>Programming Notes</p> <p>When this bit is set to a '1', the controller will write the DMA positions of each of the DMA engines to the buffer in main memory periodically (typically once/frame). Software can use this value to know what data in memory is valid data. The controller must guarantee that the values in the DMA Position Buffer that the software can read represent positions in the stream for which valid data exists in the Stream's DMA buffer. This has particular relevance in systems which support isochronous transfer; the stream positions in the software-visible memory buffer must represent stream data which has reached the Global Observation point.</p>	Value	Name	Description	0b	Disable [Default]	See ProgramminNotes	1b	Enable	See ProgramminNotes
Value	Name	Description									
0b	Disable [Default]	See ProgramminNotes									
1b	Enable	See ProgramminNotes									

DMA Position Upper Base Address

DPUBASE - DMA Position Upper Base Address				
DWord	Bit	Description		
0	31:0	<p>DPUBASE</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> </table> <p>DMA Position Upper Base Address: Upper 32 bits of address of the DMA Position Buffer Base Address. This register field must not be written when the DMA engine is running or the DMA transfer may be corrupted.</p>	Default Value:	00000000h
Default Value:	00000000h			

DP_AUX_CTL

DP_AUX_CTL			
Register Space:	MMIO: 0/2/0		
Project:	DevLPT		
Default Value:	0x0003003F		
Access:	R/W Special		
Size (in bits):	32		
Address:	E4110h-E4113h		
Name:	DisplayPort B AUX Channel Control		
ShortName:	DP_AUX_CTL_B		
Power:	Always on		
Reset:	soft		
Address:	E4210h-E4213h		
Name:	DisplayPort C AUX Channel Control		
ShortName:	DP_AUX_CTL_C		
Power:	Always on		
Reset:	soft		
Address:	E4310h-E4313h		
Name:	DisplayPort D AUX Channel Control		
ShortName:	DP_AUX_CTL_D		
Power:	Always on		
Reset:	soft		
Restriction			
The DisplayPort D AUX Channel is not connected in some SKUs.			
DWord	Bit	Description	
0	31	Send Busy	
		Access:	R/W Set
		Writing this bit with 1b initiates the transaction, when read this bit will be a 1b until the transmission completes. The transaction is completed when the response is received or when a timeout occurs. Do not write a 1b again until transaction completes. This is a sticky bit. Write a 1b to this bit to set it and initiate the transaction. Hardware will clear it when the transaction completes.	
Value		Name	
0b		Not Busy	
1b		Send or Busy	

DP_AUX_CTL																	
		<p>Programming Notes</p> <p>It is recommended to retry at least 3 times after any failed transaction. Do not change any fields while Send/Busy bit 31 is asserted.</p>															
		<p>Workaround</p> <p>On LP systems with ISCLK PLL shutdown enabled, display register C2020h bit 12 must be set to 1b before sending an AUX Channel transaction. If no other feature requires register C2020h bit 12, it can be cleared to 0b after the AUX Channel transaction is complete. To save power, register C2020h bit 12 must be cleared to 0b when internal graphics is put in the D3 device power state.</p>															
		<p>30 Done</p> <table border="1"> <tr> <td>Access:</td><td>R/WC</td></tr> </table> <p>A sticky bit that indicates the transaction has completed. Write a 1 to this bit to clear the event.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Not done</td><td>Transaction not done</td></tr> <tr> <td>1b</td><td>Done</td><td>Transaction done</td></tr> </tbody> </table>	Access:	R/WC	Value	Name	Description	0b	Not done	Transaction not done	1b	Done	Transaction done				
Access:	R/WC																
Value	Name	Description															
0b	Not done	Transaction not done															
1b	Done	Transaction done															
		<p>29 Interrupt on Done</p> <p>Enable an interrupt in the hotplug status register when the transaction completes or times out.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Disable</td><td>Disable interrupt on done</td></tr> <tr> <td>1b</td><td>Enable</td><td>Enable interrupt on done</td></tr> </tbody> </table>	Value	Name	Description	0b	Disable	Disable interrupt on done	1b	Enable	Enable interrupt on done						
Value	Name	Description															
0b	Disable	Disable interrupt on done															
1b	Enable	Enable interrupt on done															
		<p>28 Time out error</p> <table border="1"> <tr> <td>Access:</td><td>R/WC</td></tr> </table> <p>A sticky bit that indicates the transaction has timed out. Write a 1 to this bit to clear the event.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>No error</td><td>No time out error</td></tr> <tr> <td>1b</td><td>Error</td><td>Time out error</td></tr> </tbody> </table>	Access:	R/WC	Value	Name	Description	0b	No error	No time out error	1b	Error	Time out error				
Access:	R/WC																
Value	Name	Description															
0b	No error	No time out error															
1b	Error	Time out error															
		<p>27:26 Time out timer value</p> <p>Used to determine how long to wait for receiver response before timing out.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>00b</td><td>400us</td><td>400us</td></tr> <tr> <td>01b</td><td>600us</td><td>600us</td></tr> <tr> <td>10b</td><td>800us</td><td>800us</td></tr> <tr> <td>11b</td><td>1600us</td><td>1600us</td></tr> </tbody> </table>	Value	Name	Description	00b	400us	400us	01b	600us	600us	10b	800us	800us	11b	1600us	1600us
Value	Name	Description															
00b	400us	400us															
01b	600us	600us															
10b	800us	800us															
11b	1600us	1600us															

DP_AUX_CTL																		
25	Receive error	<p>Access: R/WC</p> <p>A sticky bit that indicates that the data received was corrupted, not in multiples of a full byte, or more than 20 bytes. Write a 1 to this bit to clear the event.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>No error</td><td>No receive error</td></tr> <tr> <td>1b</td><td>Error</td><td>Receive error</td></tr> </tbody> </table>	Value	Name	Description	0b	No error	No receive error	1b	Error	Receive error							
Value	Name	Description																
0b	No error	No receive error																
1b	Error	Receive error																
24:20	Message Size	<p>This field is used to indicate the total number bytes to transmit (including the header). It also indicates the number of bytes received in a transaction (including the header). This field is valid only when the done bit is set, and if timeout or receive error has not occurred. Sync/Stop patterns are not counted as part of the message or the message size. Reads of this field will give the response message size. The read value will not be valid while Send/Busy bit 31 is asserted. Message sizes of 0 or >20 are not allowed.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>00000b</td><td>0 bytes</td></tr> </tbody> </table>	Value	Name	00000b	0 bytes												
Value	Name																	
00000b	0 bytes																	
19:16	Precharge Time	<p>Default Value: 0011b 6us</p> <p>Used to determine the precharge time for the Aux Channel drivers. During this time the Aux Channel will drive the SYNC pattern. Every microsecond gives one additional SYNC pulse beyond the hard coded 26 SYNC pulses. The value is the number of microseconds times 2. Default is 3 decimal, which gives 6us of precharge, which is 6 extra SYNC pulses for a total of 32.</p>																
15	Reserved																	
14	Reserved																	
13	Reserved																	
12	Reserved																	
11	Reserved																	
10:0	2X Bit Clock divider	<p>This field determines the 2X bit clock the Aux Channel logic runs on. This value divides the input clock frequency down to 2X bit clock rate. It should be programmed to get as close as possible to the ideal rate of 2 MHz. The input clock is the raw clock.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Project</th></tr> </thead> <tbody> <tr> <td>03Fh</td><td>125 MHz [Default]</td><td>DevLPT:H</td></tr> <tr> <td>048h</td><td>Workaround</td><td>DevLPT:H</td></tr> <tr> <td>00Ch</td><td>24 MHz [Default]</td><td>DevLPT:LP</td></tr> </tbody> </table> <table border="1"> <thead> <tr> <th>Workaround</th><th>Project</th></tr> </thead> <tbody> <tr> <td>On LPT:H use a divider value of 63 decimal (03Fh). If there is a failure, retry at least 3 times with 63, then retry at least 3 times with 72 decimal (048h).</td><td>DevLPT:H</td></tr> </tbody> </table>	Value	Name	Project	03Fh	125 MHz [Default]	DevLPT:H	048h	Workaround	DevLPT:H	00Ch	24 MHz [Default]	DevLPT:LP	Workaround	Project	On LPT:H use a divider value of 63 decimal (03Fh). If there is a failure, retry at least 3 times with 63, then retry at least 3 times with 72 decimal (048h).	DevLPT:H
Value	Name	Project																
03Fh	125 MHz [Default]	DevLPT:H																
048h	Workaround	DevLPT:H																
00Ch	24 MHz [Default]	DevLPT:LP																
Workaround	Project																	
On LPT:H use a divider value of 63 decimal (03Fh). If there is a failure, retry at least 3 times with 63, then retry at least 3 times with 72 decimal (048h).	DevLPT:H																	

DP_AUX_DATA

DP_AUX_DATA		
Register Space: MMIO: 0/2/0 Project: DevLPT Default Value: 0x00000000 Access: Write/Read Status Size (in bits): 32		
Address:		E4114h-E4127h
Name:		DisplayPort B AUX Channel Data
ShortName:		DP_AUX_DATA_B_*
Power:		Always on
Reset:		soft
Address:		E4214h-E4227h
Name:		DisplayPort C AUX Channel Data
ShortName:		DP_AUX_DATA_C_*
Power:		Always on
Reset:		soft
Address:		E4314h-E4327h
Name:		DisplayPort D AUX Channel Data
ShortName:		DP_AUX_DATA_D_*
Power:		Always on
Reset:		soft
There are 5 instances of this register format per AUX channel.		
DWord	Bit	Description
0	31:0	AUX CH DATA This field contains a DWord of the AUX message. Writes to this register give the data to transmit during the transaction. The MSbyte is transmitted first. Reads to this register will give the response data after transaction complete. The read value will not be valid while the Aux Channel Control Register Send/Busy bit is asserted.

DP_TP_CTL

DP_TP_CTL	
Register Space:	MMIO: 0/2/0
Project:	BDW
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	64040h-64043h
Name:	DDI A DisplayPort Transport Control
ShortName:	DP_TP_CTL_A
Valid Projects:	BDW
Power:	Always on
Reset:	soft
Address:	64140h-64143h
Name:	DDI B DisplayPort Transport Control
ShortName:	DP_TP_CTL_B
Valid Projects:	BDW
Power:	off/on
Reset:	soft
Address:	64240h-64243h
Name:	DDI C DisplayPort Transport Control
ShortName:	DP_TP_CTL_C
Valid Projects:	BDW
Power:	off/on
Reset:	soft
Address:	64340h-64343h
Name:	DDI D DisplayPort Transport Control
ShortName:	DP_TP_CTL_D
Valid Projects:	BDW
Power:	off/on
Reset:	soft
Address:	64440h-64443h
Name:	DDI E DisplayPort Transport Control
ShortName:	DP_TP_CTL_E
Valid Projects:	BDW
Power:	off/on
Reset:	soft

DP_TP_CTL																	
DWord	Bit	Description															
0	31	<p>Transport Enable This bit enables the DisplayPort transport function.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Disable</td></tr> <tr> <td>1b</td><td>Enable</td></tr> </tbody> </table>	Value	Name	0b	Disable	1b	Enable									
Value	Name																
0b	Disable																
1b	Enable																
	30:28	<p>Reserved</p> <table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ													
Format:	MBZ																
	27	<p>Transport Mode Select</p> <table border="1"> <thead> <tr> <th colspan="3">Description</th></tr> </thead> <tbody> <tr> <td colspan="3">This bit selects between DisplayPort SST and MST modes of operation. This bit is ignored by DDI A (EDP) and DDI E since they do not support multistreaming.</td></tr> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> <tr> <td>0b</td><td>SST mode</td><td>DisplayPort SST mode</td></tr> <tr> <td>1b</td><td>MST mode</td><td>DisplayPort MST mode</td></tr> </tbody> </table> <p>Restriction</p> <p>The DisplayPort mode (SST or MST) selected here must match the mode selected in the Transcoder DDI Function Control registers for the transcoders attached to this transport. This field must not be changed while the DDI function is enabled.</p> <p>FDI does not support MST mode.</p>	Description			This bit selects between DisplayPort SST and MST modes of operation. This bit is ignored by DDI A (EDP) and DDI E since they do not support multistreaming.			Value	Name	Description	0b	SST mode	DisplayPort SST mode	1b	MST mode	DisplayPort MST mode
Description																	
This bit selects between DisplayPort SST and MST modes of operation. This bit is ignored by DDI A (EDP) and DDI E since they do not support multistreaming.																	
Value	Name	Description															
0b	SST mode	DisplayPort SST mode															
1b	MST mode	DisplayPort MST mode															
	26	<p>Reserved</p> <table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ													
Format:	MBZ																
	25	<p>Force ACT</p> <table border="1"> <thead> <tr> <th colspan="3">Description</th></tr> </thead> <tbody> <tr> <td colspan="3">This bit forces DisplayPort MST ACT to be sent one time at the next link frame boundary. After ACT is sent, as indicated in the ACT sent status bit, this bit can be cleared and set again to send ACT again. This bit is ignored by DDI A (EDP) and DDI E since they do not support multistreaming.</td></tr> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> <tr> <td>0b</td><td>Do not force</td><td>Do not force ACT to be sent</td></tr> <tr> <td>1b</td><td>Force</td><td>Force ACT to be sent one time</td></tr> </tbody> </table>	Description			This bit forces DisplayPort MST ACT to be sent one time at the next link frame boundary. After ACT is sent, as indicated in the ACT sent status bit, this bit can be cleared and set again to send ACT again. This bit is ignored by DDI A (EDP) and DDI E since they do not support multistreaming.			Value	Name	Description	0b	Do not force	Do not force ACT to be sent	1b	Force	Force ACT to be sent one time
Description																	
This bit forces DisplayPort MST ACT to be sent one time at the next link frame boundary. After ACT is sent, as indicated in the ACT sent status bit, this bit can be cleared and set again to send ACT again. This bit is ignored by DDI A (EDP) and DDI E since they do not support multistreaming.																	
Value	Name	Description															
0b	Do not force	Do not force ACT to be sent															
1b	Force	Force ACT to be sent one time															
	24:21	<p>Reserved</p> <table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ													
Format:	MBZ																
	20:19	<p>Reserved</p> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	BDW	Format:	MBZ											
Project:	BDW																
Format:	MBZ																

DP_TP_CTL								
18	Enhanced Framing Enable							
	Description							
	This bit selects enhanced framing for DisplayPort SST or FDI.							
	Hardware internally enables enhanced framing for DisplayPort MST.							
	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center; padding: 2px;">Value</th><th style="text-align: center; padding: 2px;">Name</th></tr> </thead> <tbody> <tr> <td style="padding: 2px;">0b</td><td style="padding: 2px;">Disabled</td></tr> <tr> <td style="padding: 2px;">1b</td><td style="padding: 2px;">Enabled</td></tr> </tbody> </table>		Value	Name	0b	Disabled	1b	Enabled
Value	Name							
0b	Disabled							
1b	Enabled							
	Restriction							
	In DisplayPort MST mode this bit must be set to Disabled. This field must not be changed while the DDI function is enabled.							
17:16	Reserved							
	Format:	MBZ						
15	FDI Auto Train Enable							
	Project:	BDW						
	This bit enables FDI auto-training on this port.							
	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center; padding: 2px;">Value</th><th style="text-align: center; padding: 2px;">Name</th></tr> </thead> <tbody> <tr> <td style="padding: 2px;">0b</td><td style="padding: 2px;">Disable</td></tr> <tr> <td style="padding: 2px;">1b</td><td style="padding: 2px;">Enable</td></tr> </tbody> </table>		Value	Name	0b	Disable	1b	Enable
Value	Name							
0b	Disable							
1b	Enable							
	Programming Notes							
	See the mode set enable sequence for usage.							
	Restriction							
	Do not change this bit while the port is enabled. This bit must not be set when the DDI Function is not in FDI mode.							
14:11	Reserved							
	Format:	MBZ						

DP_TP_CTL																							
10:8	DP Link Training Enable These bits are used for DisplayPort link initialization as defined in the DisplayPort specification. DP_TP_STATUS has an indication that the required number of idle patterns has been sent.																						
<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>000b</td><td>Pattern 1</td><td>Training Pattern 1 enabled</td></tr> <tr> <td>001b</td><td>Pattern 2</td><td>Training Pattern 2 enabled</td></tr> <tr> <td>010b</td><td>Idle</td><td>Idle Pattern enabled</td></tr> <tr> <td>011b</td><td>Normal</td><td>Link not in training: Send normal pixels</td></tr> <tr> <td>100b</td><td>Pattern 3</td><td>Training Pattern 3 enabled</td></tr> <tr> <td>Others</td><td>Reserved</td><td>Reserved</td></tr> </tbody> </table>			Value	Name	Description	000b	Pattern 1	Training Pattern 1 enabled	001b	Pattern 2	Training Pattern 2 enabled	010b	Idle	Idle Pattern enabled	011b	Normal	Link not in training: Send normal pixels	100b	Pattern 3	Training Pattern 3 enabled	Others	Reserved	Reserved
Value	Name	Description																					
000b	Pattern 1	Training Pattern 1 enabled																					
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011b	Normal	Link not in training: Send normal pixels																					
100b	Pattern 3	Training Pattern 3 enabled																					
Others	Reserved	Reserved																					
Restriction																							
When enabling the port, it must be turned on with pattern 1 enabled. When retraining a link, the port must be disabled, then re-enabled with pattern 1 enabled.																							
7	Reserved																						
6	Alternate SR Enable This bit enables the DisplayPort Alternate Scrambler Reset, intended for use only with embedded DisplayPort receivers.																						
<table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Disable</td></tr> <tr> <td>1b</td><td>Enable</td></tr> </tbody> </table>			Value	Name	0b	Disable	1b	Enable															
Value	Name																						
0b	Disable																						
1b	Enable																						
Restriction																							
This field must not be changed while the DDI function is enabled.																							
5:0	Reserved																						
	Format:	MBZ																					

DP_TP_STATUS

DP_TP_STATUS			
Register Space:	MMIO: 0/2/0		
Project:	BDW		
Default Value:	0x00000000		
Access:	R/W		
Size (in bits):	32		
Address:	64144h-64147h		
Name:	DDI B DisplayPort Transport Status		
ShortName:	DP_TP_STATUS_B		
Valid Projects:	BDW		
Power:	off/on		
Reset:	soft		
Address:	64244h-64247h		
Name:	DDI C DisplayPort Transport Status		
ShortName:	DP_TP_STATUS_C		
Valid Projects:	BDW		
Power:	off/on		
Reset:	soft		
Address:	64344h-64347h		
Name:	DDI D DisplayPort Transport Status		
ShortName:	DP_TP_STATUS_D		
Valid Projects:	BDW		
Power:	off/on		
Reset:	soft		
Address:	64444h-64447h		
Name:	DDI E DisplayPort Transport Status		
ShortName:	DP_TP_STATUS_E		
Valid Projects:	BDW		
Power:	off/on		
Reset:	soft		
There is one DisplayPort Transport Status register per each DDI B/C/D/E/F. DDI A does not have a status register.			
DWord	Bit	Description	
0	31:28	Reserved	
		Format:	MBZ

DP_TP_STATUS													
27	Idle Link Frame Status	<table border="1"> <tr> <td>Access:</td><td>R/WC</td></tr> </table> <p>This bit indicates if a link frame boundary has been sent in idle pattern. This is a sticky bit, cleared by writing 1b to it.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Idle link frame not sent</td></tr> <tr> <td>1b</td><td>Idle link frame sent</td></tr> </tbody> </table>	Access:	R/WC	Value	Name	0b	Idle link frame not sent	1b	Idle link frame sent			
Access:	R/WC												
Value	Name												
0b	Idle link frame not sent												
1b	Idle link frame sent												
26	Active Link Frame Status	<table border="1"> <tr> <td>Access:</td><td>R/WC</td></tr> </table> <p>This bit indicates if a link frame boundary has been sent in active (at least one VC enabled). This is a sticky bit, cleared by writing 1b to it.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Active link frame not sent</td></tr> <tr> <td>1b</td><td>Active link frame sent</td></tr> </tbody> </table>	Access:	R/WC	Value	Name	0b	Active link frame not sent	1b	Active link frame sent			
Access:	R/WC												
Value	Name												
0b	Active link frame not sent												
1b	Active link frame sent												
25	Min Idles Sent	<table border="1"> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>This bit indicates that the minimum required number of idle patterns has been sent when DP_TP_CTL is set to send idle patterns. This bit will clear itself when DP_TP_CTL is not longer set to send idle patterns.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Min idles not sent</td></tr> <tr> <td>1b</td><td>Min idles sent</td></tr> </tbody> </table>	Access:	RO	Value	Name	0b	Min idles not sent	1b	Min idles sent			
Access:	RO												
Value	Name												
0b	Min idles not sent												
1b	Min idles sent												
24	ACT Sent Status	<table border="1"> <tr> <td>Access:</td><td>R/WC</td></tr> </table> <p>This bit indicates if DisplayPort MST ACT has been sent. This is a sticky bit, cleared by writing 1b to it.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0b</td><td>ACT not sent</td></tr> <tr> <td>1b</td><td>ACT sent</td></tr> </tbody> </table>	Access:	R/WC	Value	Name	0b	ACT not sent	1b	ACT sent			
Access:	R/WC												
Value	Name												
0b	ACT not sent												
1b	ACT sent												
23	Mode Status	<table border="1"> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>This bit indicates what mode the transport is currently in.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>SST</td><td>Single-stream mode</td></tr> <tr> <td>1b</td><td>MST</td><td>Multi-stream mode</td></tr> </tbody> </table>	Access:	RO	Value	Name	Description	0b	SST	Single-stream mode	1b	MST	Multi-stream mode
Access:	RO												
Value	Name	Description											
0b	SST	Single-stream mode											
1b	MST	Multi-stream mode											
22:18	Reserved	<table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ									
Format:	MBZ												

DP_TP_STATUS																			
	17:16	Streams Enabled																	
		<table border="1"> <tr> <td>Access:</td><td colspan="2">RO</td></tr> </table> <p>This field indicates the number of streams (transcoders) enabled on this port during multistream operation. This field should be ignored in single stream mode.</p>			Access:	RO													
Access:	RO																		
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>00b</td><td>Zero</td><td>Zero streams enabled</td></tr> <tr> <td>01b</td><td>One</td><td>One stream enabled</td></tr> <tr> <td>10b</td><td>Two</td><td>Two streams enabled</td></tr> <tr> <td>11b</td><td>Three</td><td>Three streams enabled</td></tr> </tbody> </table>			Value	Name	Description	00b	Zero	Zero streams enabled	01b	One	One stream enabled	10b	Two	Two streams enabled	11b	Three	Three streams enabled
Value	Name	Description																	
00b	Zero	Zero streams enabled																	
01b	One	One stream enabled																	
10b	Two	Two streams enabled																	
11b	Three	Three streams enabled																	
	15:13	Reserved		Format: MBZ															
	12	FDI Auto Train Done																	
		<table border="1"> <tr> <td>Project:</td><td colspan="2">BDW</td></tr> <tr> <td>Access:</td><td colspan="2">RO</td></tr> </table> <p>This bit indicates when FDI auto-training completes on this port.</p>			Project:	BDW		Access:	RO										
Project:	BDW																		
Access:	RO																		
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Not Done</td><td>Auto-training is not complete or not started</td></tr> <tr> <td>1b</td><td>Done</td><td>Auto-training is complete</td></tr> </tbody> </table>			Value	Name	Description	0b	Not Done	Auto-training is not complete or not started	1b	Done	Auto-training is complete						
Value	Name	Description																	
0b	Not Done	Auto-training is not complete or not started																	
1b	Done	Auto-training is complete																	
	11:10	Reserved																	
		Format: MBZ																	
	9:8	Payload Mapping VC2																	
		<table border="1"> <tr> <td>Access:</td><td colspan="2">RO</td></tr> </table> <p>This field indicates which transcoder is mapped to Virtual Channel 2 during multistream operation. This field should be ignored if the number of streams enabled is less than three. This field should be ignored in single stream mode.</p>			Access:	RO													
Access:	RO																		
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>00b</td><td>A</td><td>Transcoder A mapped to this VC</td></tr> <tr> <td>01b</td><td>B</td><td>Transcoder B mapped to this VC</td></tr> <tr> <td>10b</td><td>C</td><td>Transcoder C mapped to this VC</td></tr> <tr> <td>11b</td><td>Reserved</td><td>Reserved</td></tr> </tbody> </table>			Value	Name	Description	00b	A	Transcoder A mapped to this VC	01b	B	Transcoder B mapped to this VC	10b	C	Transcoder C mapped to this VC	11b	Reserved	Reserved
Value	Name	Description																	
00b	A	Transcoder A mapped to this VC																	
01b	B	Transcoder B mapped to this VC																	
10b	C	Transcoder C mapped to this VC																	
11b	Reserved	Reserved																	
	7:6	Reserved																	
		Format: MBZ																	

DP_TP_STATUS																	
5:4	Payload Mapping VC1																
	Access:	RO															
This field indicates which transcoder is mapped to Virtual Channel 1 during multistream operation. This field should be ignored if the number of streams enabled is less than two. This field should be ignored in single stream mode.																	
	<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>00b</td><td>A</td><td>Transcoder A mapped to this VC</td></tr> <tr> <td>01b</td><td>B</td><td>Transcoder B mapped to this VC</td></tr> <tr> <td>10b</td><td>C</td><td>Transcoder C mapped to this VC</td></tr> <tr> <td>11b</td><td>Reserved</td><td>Reserved</td></tr> </tbody> </table>		Value	Name	Description	00b	A	Transcoder A mapped to this VC	01b	B	Transcoder B mapped to this VC	10b	C	Transcoder C mapped to this VC	11b	Reserved	Reserved
Value	Name	Description															
00b	A	Transcoder A mapped to this VC															
01b	B	Transcoder B mapped to this VC															
10b	C	Transcoder C mapped to this VC															
11b	Reserved	Reserved															
3:2	Reserved																
	Format:	MBZ															
1:0	Payload Mapping VC0																
	Access:	RO															
This field indicates which transcoder is mapped to Virtual Channel 0 during multistream operation. This field should be ignored if the number of streams enabled is less than one. This field should be ignored in single stream mode.																	
	<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>00b</td><td>A</td><td>Transcoder A mapped to this VC</td></tr> <tr> <td>01b</td><td>B</td><td>Transcoder B mapped to this VC</td></tr> <tr> <td>10b</td><td>C</td><td>Transcoder C mapped to this VC</td></tr> <tr> <td>11b</td><td>Reserved</td><td>Reserved</td></tr> </tbody> </table>		Value	Name	Description	00b	A	Transcoder A mapped to this VC	01b	B	Transcoder B mapped to this VC	10b	C	Transcoder C mapped to this VC	11b	Reserved	Reserved
Value	Name	Description															
00b	A	Transcoder A mapped to this VC															
01b	B	Transcoder B mapped to this VC															
10b	C	Transcoder C mapped to this VC															
11b	Reserved	Reserved															

DPST_BIN

DPST_BIN		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Source:	BSpec	
Default Value:	0x00000000	
Access:	Double Buffered	
Size (in bits):	32	
Double Buffer Update Point:	Start of vertical blank	
Address:	490C4h-490C7h	
Name:	Pipe A DPST Bin Data	
ShortName:	DPST_BIN_A	
Valid Projects:	BDW	
Power:	Always on	
Reset:	soft	
Address:	491C4h-491C7h	
Name:	Pipe B DPST Bin Data	
ShortName:	DPST_BIN_B	
Valid Projects:	BDW	
Power:	off/on	
Reset:	soft	
Address:	492C4h-492C7h	
Name:	Pipe C DPST Bin Data	
ShortName:	DPST_BIN_C	
Valid Projects:	BDW	
Power:	off/on	
Reset:	soft	
Access to this address are steered to the correct register by programming the Bin Register Function Select and the Bin Register Index. Updates take place at the start of vertical blank.		
DWord	Bit	Description
0	31	Busy Bit If (DPST_CTL:Bin Register Function Select = Threshold Count) {This is a read only bit. If set, the engine is busy and the rest of the register is undefined. If clear, the register contains valid data.} {This bit is reserved.}
	30:24	Reserved

DPST_BIN		
	23:0	Data If (DPST_CTL : Bin Register Function Select = Threshold Count) {Bits 23:0 are read only bits. They indicate the total number of pixels in this bin. The bin value is updated when guardband interrupt delay is met, and is not valid until after a histogram event has occurred. The bin value will stop incrementing once the maximum has been reached.} {Bits 23:10 are reserved and should be written as zeroes. Bits 9:0 are R/W double-buffered and program the correction value for this bin. Writes to this register are double buffered on the next vblank. The value written here is the 10bit corrected channel value for the lowest point of the bin.}

DPST_CTL

DPST_CTL										
Register Space:	MMIO: 0/2/0									
Project:	BDW									
Source:	BSpec									
Default Value:	0x00000000									
Access:	R/W									
Size (in bits):	32									
Address:	490C0h-490C3h									
Name:	Pipe A DPST Control									
ShortName:	DPST_CTL_A									
Valid Projects:	BDW									
Power:	Always on									
Reset:	soft									
Address:	491C0h-491C3h									
Name:	Pipe B DPST Control									
ShortName:	DPST_CTL_B									
Valid Projects:	BDW									
Power:	off/on									
Reset:	soft									
Address:	492C0h-492C3h									
Name:	Pipe C DPST Control									
ShortName:	DPST_CTL_C									
Valid Projects:	BDW									
Power:	off/on									
Reset:	soft									
DWord	Bit	Description								
0	31	Reserved								
	30:28	Reserved								
	27	Reserved								
	26:25	Reserved								
	24	Histogram Mode Select								
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>YUV</td><td>YUV Luma Mode</td></tr> <tr> <td>1b</td><td>HSV</td><td>HSV Intensity Mode</td></tr> </tbody> </table>	Value	Name	Description	0b	YUV	YUV Luma Mode	1b	HSV
Value	Name	Description								
0b	YUV	YUV Luma Mode								
1b	HSV	HSV Intensity Mode								
23:16	Reserved									
15	Reserved									

DPST_CTL			
14:13	Enhancement mode		
	Value	Name	Description
	00b	Direct	Direct look up mode
	01b	Additive	Additive mode
	10b	Multiplicative	Multiplicative mode
12	Reserved		
	Bin Register Function Select This field indicates what data is being written to or read from the bin data register.		
11	Value	Name	Description
	0b	TC	Threshold Count. A read from the bin data register returns that bin's threshold value from the most recent vblank load event (guardband threshold trip). Valid range for the Bin Index is 0 to 31.
	1b	Reserved	Reserved
10:7 Reserved			
6:0	Bin Register Index This field indicates the bin number whose data can be accessed through the bin data register. This value is automatically incremented by a read or a write to the bin data register if the busy bit is not set.		

DPST_GUARD

DPST_GUARD			
Register Space:	MMIO: 0/2/0		
Project:	BDW		
Default Value:	0x00000000		
Access:	Double Buffered		
Size (in bits):	32		
Double Buffer Update Point:	Start of vertical blank		
Address:	490C8h-490CBh		
Name:	Pipe A DPST Threshold Guardband		
ShortName:	DPST_GUARD_A		
Valid Projects:	BDW		
Power:	Always on		
Reset:	soft		
Address:	491C8h-491CBh		
Name:	Pipe B DPST Threshold Guardband		
ShortName:	DPST_GUARD_B		
Valid Projects:	BDW		
Power:	off/on		
Reset:	soft		
Address:	492C8h-492CBh		
Name:	Pipe C DPST Threshold Guardband		
ShortName:	DPST_GUARD_C		
Valid Projects:	BDW		
Power:	off/on		
Reset:	soft		
Updates take place at the start of vertical blank.			
DWord	Bit	Description	
0	31	Histogram Interrupt enable	
Value	Name	Description	
0b	Disable	Disabled	
1b	Enable	This generates a histogram interrupt once a Histogram event occurs.	

DPST_GUARD			
30	Histogram Event status		
	Access:	R/WC	
	When a Histogram event has occurred, this will get set by the hardware. For any more Histogram events to occur, clear this bit by writing a '1'.		
	Value	Name	Description
	0b	Not Occurred	Histogram event has not occurred
	1b	Occured	Histogram event has occurred
	Workaround		
	The Histogram Event status may not clear if it is written with a 1b to clear it and the Histogram Interrupt enable field is changed from 0b to 1b in the same MMIO write. To guarantee the event status is cleared, separate the single MMIO write into two writes.		
29:22	Guardband Interrupt Delay		
	An interrupt is always generated after this many consecutive frames of the guardband threshold being surpassed. This value is double buffered on start of vblank.		
	Restriction		
	A value of 0 is invalid.		
21:0	Threshold Guardband		
	This value is used to determine the guardband for the threshold interrupt generation. This single value is used for all the segments. This value is double buffered on start of vblank. This value is shifted left 2 bits (multiplied by 4) for use with the 24 bit bin values.		

DS Invocation Counter

DS_INVOCATION_COUNT - DS Invocation Counter

Register Space:	MMIO: 0/2/0
Project:	BDW
Source:	RenderCS
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Trusted Type:	1

Address: 02308h

This register stores the number of domain points shaded by the DS threads. Domain points which hit in the DS cache will not cause this register to increment. Note that the spawning of a DS thread which shades two domain points will cause this counter to increment by two. This register is part of the context save and restore.

DWord	Bit	Description
0	63:32	DS Invocation Count UDW Number of domain points shaded by the DS threads. Updated only when DS Function Enable and Statistics Enable are set in 3DSTATE_DS
	31:0	DS Invocation Count LDW Number of domain points shaded by the DS threads. Updated only when DS Function Enable and Statistics Enable are set in 3DSTATE_DS

DX9 Constants Not Consumed By RCS

DX9CONST_PRODUCE_COUNT - DX9 Constants Not Consumed By RCS		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	02484h	
This register keeps track of the outstanding DX9 Constants produced by RS which are not yet consumed by Render Command Streamer. This register is part of the render context save and restore. This register should not be programmed by SW.		
DWord	Bit	Description
0	31:0	DX9 Constants Produce Count This register keeps track of the outstanding DX9 Constants produced by RS which are not yet consumed by Render Command Streamer. This register is part of the render context save and restore.

DX9 Constants Prsed By RCS

DX9CONST_PARSE_COUNT - DX9 Constants Prsed By RCS		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	02494h	
<p>This register keeps track of the DX9 Constant commands parsed by RCS prior to encountering the Draw Call in an RS enabled Batch Buffer which has DX9 Pool Alloc Valid. DX9 parse count should be less then equal to the DX9 produce count for Command Streamer to make progress on a 3D_PRIMITIVE command. DX9 Parse count is subtracted from the DX9 Produce Count upon parsing 3D_PRIMITIVE command. This register is part of the render context save and restore. This register should not be programmed by SW.</p>		
DWord	Bit	Description
0	31:0	<p>DX9 Constants Produce Count</p> <p>This register keeps track of the DX9 Constant commands parsed by RCS prior to encountering the Draw Call in an RS enabled Batch Buffer which has DX9 Pool Alloc Valid. DX9 parse count should be less then equal to the DX9 produce count for Command Streamer to make progress on a 3D_PRIMITIVE command. DX9 Parse count is subtracted from the DX9 Produce Count upon parsing 3D_PRIMITIVE command.</p>

ECO Bits - Bus Reset Domain with Lock bit

ECO_BUSRST - ECO Bits - Bus Reset Domain with Lock bit					
Register Space: MMIO: 0/2/0					
Project: BDW					
Default Value: 0x00000000					
Size (in bits): 32					
Address: 0A194h					
Lock bit ECOLOCK applies to all RW/L fields this register. These bits are not reset on FLR (device reset).					
DWord	Bit	Description			
0	31	ECO Bits - Bus Reset Domain - LOCK BIT <table border="1"> <tr> <td>Access:</td><td>R/W Lock</td></tr> </table>	Access:	R/W Lock	
Access:	R/W Lock				
30:1	ECO Bits - Bus Reset Domain <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>R/W Lock</td></tr> </table> Register bits that have no connection to design. Used to enable/disable changes to the design that were put in during the ECO process. pmcr_eco_bits[31:0].	Project:	BDW	Access:	R/W Lock
Project:	BDW				
Access:	R/W Lock				
0	Reserved				

ECO Bits - Device Reset Domain

ECO_DEV_RST - ECO Bits - Device Reset Domain						
DWord	Bit	Description				
0	31:0	<p>ECO Bits - Device Reset Domain</p> <table> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td colspan="2">Register bits that have no connection to design. Used to enable/disable changes to the design that were put in during the ECO process.</td></tr> </table>	Access:	R/W	Register bits that have no connection to design. Used to enable/disable changes to the design that were put in during the ECO process.	
Access:	R/W					
Register bits that have no connection to design. Used to enable/disable changes to the design that were put in during the ECO process.						

ECO Message Register

ECO_MSG - ECO Message Register				
DWord	Bit	Description		
0	15	<p>Placeholder for ECO Bit 15</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>ECO Bits 1'b0: (default). Register definition are modified if ECOs are required.</p>	Access:	R/W
Access:	R/W			
	14	<p>Placeholder for ECO Bit 14</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>ECO Bits 1'b0: (default). Register definition are modified if ECOs are required.</p>	Access:	R/W
Access:	R/W			
	13	<p>Placeholder for ECO Bit 13</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>ECO Bits 1'b0: (default). Register definition are modified if ECOs are required.</p>	Access:	R/W
Access:	R/W			
	12	<p>Placeholder for ECO Bit 12</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>ECO Bits 1'b0: (default). Register definition are modified if ECOs are required.</p>	Access:	R/W
Access:	R/W			
	11	<p>Placeholder for ECO Bit 11</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>ECO Bits 1'b0: (default). Register definition are modified if ECOs are required.</p>	Access:	R/W
Access:	R/W			

ECO_MSG - ECO Message Register						
	10	Placeholder for ECO Bit 10 <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>ECO Bits 1'b0: (default). Register definition are modified if ECOs are required.</p>	Access:	R/W		
Access:	R/W					
	9	Placeholder for ECO Bit 9 <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>ECO Bits 1'b0: (default). Register definition are modified if ECOs are required.</p>	Access:	R/W		
Access:	R/W					
	8	Placeholder for ECO Bit 8 <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>ECO Bits 1'b0: (default). Register definition are modified if ECOs are required.</p>	Access:	R/W		
Access:	R/W					
	7	Placeholder for ECO Bit 7 <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>ECO Bits 1'b0: (default). Register definition are modified if ECOs are required.</p>	Access:	R/W		
Access:	R/W					
	6	Placeholder for ECO Bit 6 <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>ECO Bits 1'b0: (default). Register definition are modified if ECOs are required.</p>	Access:	R/W		
Access:	R/W					
	5	Placeholder for ECO Bit 5 <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>ECO Bits 1'b0: (default). Register definition are modified if ECOs are required.</p>	Access:	R/W		
Access:	R/W					
	4	Placeholder for ECO Bit 4 <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>ECO Bits 1'b0: (default). Register definition are modified if ECOs are required.</p>	Project:	BDW	Access:	R/W
Project:	BDW					
Access:	R/W					
	3	Placeholder for ECO Bit 3 <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>ECO Bits 1'b0: (default). Register definition are modified if ECOs are required.</p>	Access:	R/W		
Access:	R/W					

ECO_MSG - ECO Message Register									
	2	Placeholder for ECO Bit 2	<table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>ECO Bits 1'b0: (default). Register definition are modified if ECOs are required.</p>	Access:	R/W				
Access:	R/W								
	1	Placeholder for ECO Bit 1	<table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>ECO Bits 1'b0: (default). Register definition are modified if ECOs are required.</p>	Access:	R/W				
Access:	R/W								
	0	GAM IDLE Status	<table border="1"> <tr> <td>Default Value:</td><td>1b</td></tr> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>New bit Added to support BDW B0 DCN # 221294 1'b1 : GAM is IDLE (default). 1'b0 : GAM is BUSY</p>	Default Value:	1b	Project:	BDW	Access:	R/W
Default Value:	1b								
Project:	BDW								
Access:	R/W								

ECO Reserved

ECORESRV - ECOReserved						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000 [BDW]					
Size (in bits):	32					
Address:	09898h					
ECO Reserved bits						
DWord	Bit	Description				
31:0	ECO Reserved Bits <table border="1" style="margin-left: 20px;"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>R/WC</td></tr> </table>	Project:	BDW	Access:	R/WC	
Project:	BDW					
Access:	R/WC					

Element Descriptor Register

ELEM_DESCRIPTOR - Element Descriptor Register		
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x00000000, 0x00000000 Access: RO Size (in bits): 64		
Address:		04500h
Name:		BCS Element Descriptor Register
ShortName:		BCS_ELEM_DESCRIPTOR
Address:		04400h
Name:		RCS Element Descriptor Register
ShortName:		RCS_ELEM_DESCRIPTOR
Address:		04440h
Name:		VCS Element Descriptor Register
ShortName:		VCS_ELEM_DESCRIPTOR
Address:		04480h
Name:		VCS2 Element Descriptor Register
ShortName:		VCS2_ELEM_DESCRIPTOR
Valid Projects:		[BDW:GT3]
Address:		044C0h
Name:		VECS Element Descriptor Register
ShortName:		VECS_ELEM_DESCRIPTOR
Element Information: The register is populated by command streamer and consumed by GAM		
DWord	Bit	Description
0	63:32	Context ID Context identification number assigned to separate this context from others. Context IDs need to be recycled in such a way that there could not be two active context with the same ID. This is a unique identification number by which a context is identified and referenced
	31:12	LRCA Command Streamer Only
	11:9	Function Number GFX device is considered to be on Bus0 with device number of 2. Function number is normally assigned as "0" however for gfx virtualization; there would be different function numbers which needs to be attached to context. Not used in Gen8.

ELEM_DESCRIPTOR - Element Descriptor Register

	8	Privileged Context / GGTT vs PPGTT mode In Legacy Context: Defines the page tables to be used. This is how page walker come to know PPGTT vs GGTT selection for the entire context. In Advanced Context: Defines the privilege level for the context															
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0h</td><td>[Default]</td><td>Use Global GTT (In Legacy Context) User Mode Context (In Advanced Context)</td></tr> <tr> <td>1h</td><td></td><td>Use Per-Process GTT (In Legacy Context) Supervisor Mode Context (In Advanced Context)</td></tr> </tbody> </table>	Value	Name	Description	0h	[Default]	Use Global GTT (In Legacy Context) User Mode Context (In Advanced Context)	1h		Use Per-Process GTT (In Legacy Context) Supervisor Mode Context (In Advanced Context)						
Value	Name	Description															
0h	[Default]	Use Global GTT (In Legacy Context) User Mode Context (In Advanced Context)															
1h		Use Per-Process GTT (In Legacy Context) Supervisor Mode Context (In Advanced Context)															
	7:6	Fault Model															
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>00h</td><td>[Default]</td><td>Fault and Hang.</td></tr> <tr> <td>01h</td><td></td><td>Reserved</td></tr> <tr> <td>10h</td><td></td><td>Reserved</td></tr> <tr> <td>11h</td><td></td><td>Reserved</td></tr> </tbody> </table>	Value	Name	Description	00h	[Default]	Fault and Hang.	01h		Reserved	10h		Reserved	11h		Reserved
Value	Name	Description															
00h	[Default]	Fault and Hang.															
01h		Reserved															
10h		Reserved															
11h		Reserved															
	5	Deeper IA coherency Support In Advanced Context: Defines the level of IA coherency															
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0h</td><td>[Default]</td><td>IA coherency is provided at LLC level for all streams of GPU (i.e. gen7.5 like mode)</td></tr> <tr> <td>1h</td><td></td><td>IA coherency is provided at L3 level for EU data accesses of GPU</td></tr> </tbody> </table>	Value	Name	Description	0h	[Default]	IA coherency is provided at LLC level for all streams of GPU (i.e. gen7.5 like mode)	1h		IA coherency is provided at L3 level for EU data accesses of GPU						
Value	Name	Description															
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1h		IA coherency is provided at L3 level for EU data accesses of GPU															
	4	A and D Support / 32 and 64b Address Support In Legacy Context: Defines 32b vs 64b (48b canonical) addressing format In Advanced Context: Defines A/D bit support															
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0h</td><td>[Default]</td><td>32b addressing format (In Legacy Context) A/D bit management in page tables is NOT supported (In Advanced Context)</td></tr> <tr> <td>1h</td><td></td><td>64b (48b canonical) addressing format (In Legacy Context) A/D bit management in page tables is supported (In Advanced Context)</td></tr> </tbody> </table>	Value	Name	Description	0h	[Default]	32b addressing format (In Legacy Context) A/D bit management in page tables is NOT supported (In Advanced Context)	1h		64b (48b canonical) addressing format (In Legacy Context) A/D bit management in page tables is supported (In Advanced Context)						
Value	Name	Description															
0h	[Default]	32b addressing format (In Legacy Context) A/D bit management in page tables is NOT supported (In Advanced Context)															
1h		64b (48b canonical) addressing format (In Legacy Context) A/D bit management in page tables is supported (In Advanced Context)															
	3	Context Type: Legacy vs Advanced Defines the context type. Note that: Bits [8:4] differs in functions when legacy vs advanced context modes are selected.															
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0h</td><td>[Default]</td><td>Advanced Context: Defines the rest of the advanced capabilities (i.e. OS page table support, fault models...). Note that advanced context is not bounded to GPGPU.</td></tr> <tr> <td>1h</td><td></td><td>Legacy Context: Defines the context as legacy mode which is similar to prior generations of gen8.</td></tr> </tbody> </table>	Value	Name	Description	0h	[Default]	Advanced Context: Defines the rest of the advanced capabilities (i.e. OS page table support, fault models...). Note that advanced context is not bounded to GPGPU.	1h		Legacy Context: Defines the context as legacy mode which is similar to prior generations of gen8.						
Value	Name	Description															
0h	[Default]	Advanced Context: Defines the rest of the advanced capabilities (i.e. OS page table support, fault models...). Note that advanced context is not bounded to GPGPU.															
1h		Legacy Context: Defines the context as legacy mode which is similar to prior generations of gen8.															
	2	FR Command Streamer Specific															

ELEM_DESCRIPTOR - Element Descriptor Register

	1	Scheduling Mode		
		Project:		BDW
		Value	Name	Description
		0h	[Default]	Indicates exelist mode of scheduling.
		1h		Indicates Ring Buffer mode of scheduling.
	0	Valid		Indicates that element descriptor is valid. If GAM is programmed with an invalid descriptor, it will continue but flag an error.

EMRR Mask LSB

EMRRMASK_LSB - EMRR Mask LSB						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	09208h					
EMRR Mask Value						
DWord	Bit	Description				
0	31:12	<p>EMRR_MASK_LSB</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td colspan="2">EMRR MASK VALUE.</td></tr> </table>	Access:	RO	EMRR MASK VALUE.	
Access:	RO					
EMRR MASK VALUE.						
11	<p>EMRR_ENABLE</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td colspan="2">EMRR Enable.</td></tr> </table>	Access:	RO	EMRR Enable.		
Access:	RO					
EMRR Enable.						
10	<p>EMRR_LOCK</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td colspan="2">EMRR LOCK bit.</td></tr> </table>	Access:	RO	EMRR LOCK bit.		
Access:	RO					
EMRR LOCK bit.						
9:0	<p>Spares</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO			
Access:	RO					

EMRR Mask MSB

EMRRMASK_MSB - EMRR Mask MSB				
Register Space: MMIO: 0/2/0				
Project: BDW				
Default Value: 0x00000000				
Size (in bits): 32				
Address: 0920Ch				
EMRR Mask Value				
DWord	Bit	Description		
0	31:7	Spares <table border="1"> <tr> <td>Access:</td><td>RO</td></tr> </table>	Access:	RO
Access:	RO			
6:0	EMRR_MASK_MSB <table border="1"> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>EMRR MASK VALUE.</p>	Access:	RO	
Access:	RO			

Engines-Idle Interrupt Configuration Register

INTERRUPT_ENGINES_IDLE - Engines-Idle Interrupt Configuration Register				
Register Space:	MMIO: 0/2/0			
Project:	BDW			
Default Value:	0x000000FC			
Size (in bits):	8			
Address:	0A16Ch			
DWord	Bit	Description		
0	7:1	Engines_idle Interrupt Mask		
		<table border="1"> <tr> <td>Default Value:</td><td>1111110b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Engine Bits. 1b = wait for this engine to indicate c6 idleness. 0b = don't wait for this engine to indicate c6 idleness. Generally expect to use to wait for all except render. [0] = cs. [1] = bcs. [2] = vcs0. [3] = vcs1. [4] = vecs. [6] = win.</p>	Default Value:	1111110b
Default Value:	1111110b			
Access:	R/W			
	0	Engines_idle Interrupt Enabled		
		<table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Enable Interrupt. Is cleared once serviced.</p>	Access:	R/W
Access:	R/W			

Error Identity Register

EIR - Error Identity Register							
Register Space: MMIO: 0/2/0 Project: BDW Source: RenderCS Default Value: 0x00000000 Access: R/W, RO Size (in bits): 32							
Address: 020B0h							
The EIR register contains the persistent values of Hardware-Detected Error Condition bits. Any bit set in this register will cause the Master Error bit in the ISR to be set. The EIR register is also used by software to clear detected errors (by writing a 1 to the appropriate bit(s)), except for the unrecoverable bits described.							
Restriction							
Restriction : EIR register contents are not power or render context save/restored. EIR register contents of an engine will get lost when the corresponding graphics engine (Render, Video, Video Enhancement, Blitter) is power down.							
DWord	Bit	Description					
0	31:16	Reserved <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Format:</td> <td style="padding: 2px;">MBZ</td> </tr> </table>	Format:	MBZ			
	Format:	MBZ					
15:0	Error Identity Bits <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Format:</td> <td style="padding: 2px;">Array of Error condition bits See the table titled Hardware-Detected Error Bits.</td> </tr> </table> <p>This register contains the persistent values of ESR error status bits that are unmasks via the EMR register. (See Table Table 3-3. Hardware-Detected Error Bits). The logical OR of all (defined) bits in this register is reported in the Master Error bit of the Interrupt Status Register. In order to clear an error condition, software must first clear the error by writing a 1 to the appropriate bit(s) in this field. If required, software should then proceed to clear the Master Error bit of the IIR. Reserved bits are RO.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%;">Value</th><th style="width: 50%;">Name</th></tr> </thead> <tbody> <tr> <td style="text-align: center; padding: 2px;">1h</td><td style="padding: 2px;">Error occurred</td></tr> </tbody> </table>	Format:	Array of Error condition bits See the table titled Hardware-Detected Error Bits.	Value	Name	1h	Error occurred
Format:	Array of Error condition bits See the table titled Hardware-Detected Error Bits.						
Value	Name						
1h	Error occurred						
Programming Notes							
Writing a 1 to a set bit will cause that error condition to be cleared. However, neither the Page Table Error bit (Bit 4) nor the Instruction Error bit (Bit 0) can be cleared except by reset (i.e., it is a fatal error).							

Error Mask Register

EMR - Error Mask Register																
DWord	Bit	Description														
0	31:8	<p>Reserved</p> <table border="1"> <tr> <td>Default Value:</td><td>FFFFFh</td></tr> <tr> <td>Format:</td><td>Must Be One</td></tr> </table> <p>Programming Notes</p> <p>These bits are not implemented in HW and must be set to '1'</p>	Default Value:	FFFFFh	Format:	Must Be One										
Default Value:	FFFFFh															
Format:	Must Be One															
	7:0	<p>Error Mask Bits</p> <table border="1"> <tr> <td>Format:</td><td>Array of error condition mask bits See the table titled Hardware-Detected Error Bits.</td></tr> </table> <p>This register contains a bit mask that selects which error condition bits (from the ESR) are reported in the EIR.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>FFh</td><td>[Default]</td><td></td></tr> <tr> <td>0h</td><td>Not Masked</td><td>Will be reported in the EIR</td></tr> <tr> <td>1h</td><td>Masked</td><td>Will not be reported in the EIR</td></tr> </tbody> </table>	Format:	Array of error condition mask bits See the table titled Hardware-Detected Error Bits.	Value	Name	Description	FFh	[Default]		0h	Not Masked	Will be reported in the EIR	1h	Masked	Will not be reported in the EIR
Format:	Array of error condition mask bits See the table titled Hardware-Detected Error Bits.															
Value	Name	Description														
FFh	[Default]															
0h	Not Masked	Will be reported in the EIR														
1h	Masked	Will not be reported in the EIR														

Error Reporting Register

ERR - Error Reporting Register				
DWord	Bit	Description		
0	31:5	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Reserved.</p>	Access:	RO
Access:	RO			
	4	<p>First Content Buffer Ready 0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>First Content Buffer Ready 0 (FRSNTBFR0). First Content Buffer Ready: This bit gets set by the HW when the buffer is completely filled up and cleared by the driver when the contents of this buffer are copied out of memory. Is set by lpfc_lpconf_buffer0_ready (pulse). lpconf_lpfc_buffer0_ready (static signal to lpfc).</p>	Access:	R/W
Access:	R/W			
	3	<p>Second Buffer ready slice 0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Second Content Buffer Ready slice 0 (SCNBFR0). Second Content Buffer Ready: This bit gets set by the HW when the buffer is completely filled up and cleared by the driver when the contents of this buffer are copied out of memory. Is set by lpfc_lpconf_buffer1_ready (pulse). lpconf_lpfc_buffer1_ready (static signal to lpfc).</p>	Access:	R/W
Access:	R/W			
	2	<p>Write Expire Error Slice 0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Write Expired Error slice 0 (WEERRO). Write Expired Error: If DMA controller could not get a chance to push the write of 64Bytes to LTSEQ and data gets clobbered with the new expiration of the save timer, this error bit is set to indicate something went wrong. Signal -lpfc_lpconf_wrexp_error.</p>	Access:	R/W
Access:	R/W			
	1	<p>Buffer full Error Slice 0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Buffer full Error Slice 0 (BFFLERO). Set by lpfc_lpconf_error_buffer_full. When all buffers are full lpfc sets this bit or if only 1 buffer is enabled then lpfc sets this bit when the buffer is full.</p>	Access:	R/W
Access:	R/W			

ERR - Error Reporting Register

	0	Reserved	
		Access:	RO
Reserved.			

Error Status Register

ESR - Error Status Register									
DWord	Bit	Description							
0	31:16	<p>Reserved</p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ					
Format:	MBZ								
15:0	<p>Error Status Bits</p> <table border="1"> <tr> <td>Format:</td> <td>Array of error condition bits See the table titled Hardware-Detected Error Bits.</td> </tr> <tr> <td>This register contains the non-persistent values of all hardware-detected error condition bits.</td> <td></td> </tr> </table> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>1h</td> <td>Error Condition Detected</td> </tr> </tbody> </table>	Format:	Array of error condition bits See the table titled Hardware-Detected Error Bits.	This register contains the non-persistent values of all hardware-detected error condition bits.		Value	Name	1h	Error Condition Detected
Format:	Array of error condition bits See the table titled Hardware-Detected Error Bits.								
This register contains the non-persistent values of all hardware-detected error condition bits.									
Value	Name								
1h	Error Condition Detected								

EU Enable Fuses for Slice0

EU_ENABLE_SLICE0 - EU Enable Fuses for Slice0		
DWord	Bit	Description
0	31:0	EU Enable Fuses for Slice0 Access: R/W

EU Enable Fuses for Slice1

EU_ENABLE_SLICE1 - EU Enable Fuses for Slice1		
DWord	Bit	Description
0	31:0	EU Enable Fuses for Slice1 Access: R/W

EU Enable Fuses for Slice2

EU_ENABLE_SLICE2 - EU Enable Fuses for Slice2				
Register Space:	MMIO: 0/2/0			
Project:	BDW			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0A268h			
<p>This register saves the value of Slice2 EU Enables during a slice change. PM restores these values to TDL once slice change is complete.</p> <p>Note that this register is not power context saved because it is always updated by MBC before a slice change occurs.</p>				
DWord	Bit	Description		
0	31:0	EU Enable Fuses for Slice2 <table border="1" style="margin-top: 2px;"> <tr> <td>Access:</td><td>R/W</td></tr> </table>	Access:	R/W
Access:	R/W			

EU Mask Programming

TD_PM_MODE_EUCOUNT - EU Mask Programming

Register Space:	MMIO: 0/2/0									
Project:	BDW									
Default Value:	0x00000000									
Access:	WO									
Size (in bits):	32									
Address:	0E4F8h									
Name:	EU Mask Programming Slice 0									
ShortName:	TD_PM_MODE_EUCOUNT_S0									
Valid Projects:	[BDW]									
Address:	0E5F8h									
Name:	EU Mask Programming Slice 1									
ShortName:	TD_PM_MODE_EUCOUNT_S1									
Valid Projects:	[BDW]									
Address:	0E6F8h									
Name:	EU Mask Programming Slice 2									
ShortName:	TD_PM_MODE_EUCOUNT_S2									
Valid Projects:	[BDW]									
<hr/>										
DWord	Bit	Description								
0	31:24	Reserved								
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	BDW	Format:	MBZ				
Project:	BDW									
Format:	MBZ									
23	SubSlice 2 EU 7 Enable									
	<table border="1"> <tr> <td>Format:</td><td>Enable</td></tr> <tr> <td align="center" colspan="2"><hr/></td></tr> <tr> <th>Value</th><th>Name</th></tr> <tr> <td>0</td><td>Enabled [Default]</td></tr> <tr> <td>1</td><td>Disabled</td></tr> </table>	Format:	Enable	<hr/>		Value	Name	0	Enabled [Default]	1
Format:	Enable									
<hr/>										
Value	Name									
0	Enabled [Default]									
1	Disabled									
22	22	SubSlice 2 EU 6 Enable								
		<table border="1"> <tr> <td>Format:</td><td>Enable</td></tr> <tr> <td align="center" colspan="2"><hr/></td></tr> <tr> <th>Value</th><th>Name</th></tr> <tr> <td>0</td><td>Enabled [Default]</td></tr> <tr> <td>1</td><td>Disabled</td></tr> </table>	Format:	Enable	<hr/>		Value	Name	0	Enabled [Default]
Format:	Enable									
<hr/>										
Value	Name									
0	Enabled [Default]									
1	Disabled									

TD_PM_MODE_EUCOUNT - EU Mask Programming

	21	SubSlice 2 EU 5 Enable							
		Format: <input type="text"/> Enable							
		<table border="1"><thead><tr><th>Value</th><th>Name</th></tr></thead><tbody><tr><td>0</td><td>Enabled [Default]</td></tr><tr><td>1</td><td>Disabled</td></tr></tbody></table>		Value	Name	0	Enabled [Default]	1	Disabled
Value	Name								
0	Enabled [Default]								
1	Disabled								
	20	SubSlice 2 EU 4 Enable							
		Format: <input type="text"/> Enable							
		<table border="1"><thead><tr><th>Value</th><th>Name</th></tr></thead><tbody><tr><td>0</td><td>Enabled [Default]</td></tr><tr><td>1</td><td>Disabled</td></tr></tbody></table>		Value	Name	0	Enabled [Default]	1	Disabled
Value	Name								
0	Enabled [Default]								
1	Disabled								
	19	SubSlice 2 EU 3 Enable							
		Format: <input type="text"/> Enable							
		<table border="1"><thead><tr><th>Value</th><th>Name</th></tr></thead><tbody><tr><td>0</td><td>Enabled [Default]</td></tr><tr><td>1</td><td>Disabled</td></tr></tbody></table>		Value	Name	0	Enabled [Default]	1	Disabled
Value	Name								
0	Enabled [Default]								
1	Disabled								
	18	SubSlice 2 EU 2 Enable							
		Format: <input type="text"/> Enable							
		<table border="1"><thead><tr><th>Value</th><th>Name</th></tr></thead><tbody><tr><td>0</td><td>Enabled [Default]</td></tr><tr><td>1</td><td>Disabled</td></tr></tbody></table>		Value	Name	0	Enabled [Default]	1	Disabled
Value	Name								
0	Enabled [Default]								
1	Disabled								
	17	SubSlice 2 EU 1 Enable							
		Format: <input type="text"/> Enable							
		<table border="1"><thead><tr><th>Value</th><th>Name</th></tr></thead><tbody><tr><td>0</td><td>Enabled [Default]</td></tr><tr><td>1</td><td>Disabled</td></tr></tbody></table>		Value	Name	0	Enabled [Default]	1	Disabled
Value	Name								
0	Enabled [Default]								
1	Disabled								
	16	SubSlice 2 EU 0 Enable							
		Format: <input type="text"/> Enable							
		<table border="1"><thead><tr><th>Value</th><th>Name</th></tr></thead><tbody><tr><td>0</td><td>Enabled [Default]</td></tr><tr><td>1</td><td>Disabled</td></tr></tbody></table>		Value	Name	0	Enabled [Default]	1	Disabled
Value	Name								
0	Enabled [Default]								
1	Disabled								

TD_PM_MODE_EUCOUNT - EU Mask Programming

	15	SubSlice 1 EU 7 Enable							
		Format: <input type="text"/> Enable							
		<table border="1" style="width: 100%;"><thead><tr><th style="text-align: center;">Value</th><th style="text-align: center;">Name</th></tr></thead><tbody><tr><td style="text-align: center;">0</td><td>Enabled [Default]</td></tr><tr><td style="text-align: center;">1</td><td>Disabled</td></tr></tbody></table>		Value	Name	0	Enabled [Default]	1	Disabled
Value	Name								
0	Enabled [Default]								
1	Disabled								
	14	SubSlice 1 EU 6 Enable							
		Format: <input type="text"/> Enable							
		<table border="1" style="width: 100%;"><thead><tr><th style="text-align: center;">Value</th><th style="text-align: center;">Name</th></tr></thead><tbody><tr><td style="text-align: center;">0</td><td>Enabled [Default]</td></tr><tr><td style="text-align: center;">1</td><td>Disabled</td></tr></tbody></table>		Value	Name	0	Enabled [Default]	1	Disabled
Value	Name								
0	Enabled [Default]								
1	Disabled								
	13	SubSlice 1 EU 5 Enable							
		Format: <input type="text"/> Enable							
		<table border="1" style="width: 100%;"><thead><tr><th style="text-align: center;">Value</th><th style="text-align: center;">Name</th></tr></thead><tbody><tr><td style="text-align: center;">0</td><td>Enabled [Default]</td></tr><tr><td style="text-align: center;">1</td><td>Disabled</td></tr></tbody></table>		Value	Name	0	Enabled [Default]	1	Disabled
Value	Name								
0	Enabled [Default]								
1	Disabled								
	12	SubSlice 1 EU 4 Enable							
		Format: <input type="text"/> Enable							
		<table border="1" style="width: 100%;"><thead><tr><th style="text-align: center;">Value</th><th style="text-align: center;">Name</th></tr></thead><tbody><tr><td style="text-align: center;">0</td><td>Enabled [Default]</td></tr><tr><td style="text-align: center;">1</td><td>Disabled</td></tr></tbody></table>		Value	Name	0	Enabled [Default]	1	Disabled
Value	Name								
0	Enabled [Default]								
1	Disabled								
	11	SubSlice 1 EU 3 Enable							
		Format: <input type="text"/> Enable							
		<table border="1" style="width: 100%;"><thead><tr><th style="text-align: center;">Value</th><th style="text-align: center;">Name</th></tr></thead><tbody><tr><td style="text-align: center;">0</td><td>Enabled [Default]</td></tr><tr><td style="text-align: center;">1</td><td>Disabled</td></tr></tbody></table>		Value	Name	0	Enabled [Default]	1	Disabled
Value	Name								
0	Enabled [Default]								
1	Disabled								
	10	SubSlice 1 EU 2 Enable							
		Format: <input type="text"/> Enable							
		<table border="1" style="width: 100%;"><thead><tr><th style="text-align: center;">Value</th><th style="text-align: center;">Name</th></tr></thead><tbody><tr><td style="text-align: center;">0</td><td>Enabled [Default]</td></tr><tr><td style="text-align: center;">1</td><td>Disabled</td></tr></tbody></table>		Value	Name	0	Enabled [Default]	1	Disabled
Value	Name								
0	Enabled [Default]								
1	Disabled								

TD_PM_MODE_EUCOUNT - EU Mask Programming

	9	SubSlice 1 EU 1 Enable							
		Format: <input type="text"/> Enable							
		<table border="1"><thead><tr><th>Value</th><th>Name</th></tr></thead><tbody><tr><td>0</td><td>Enabled [Default]</td></tr><tr><td>1</td><td>Disabled</td></tr></tbody></table>		Value	Name	0	Enabled [Default]	1	Disabled
Value	Name								
0	Enabled [Default]								
1	Disabled								
	8	SubSlice 1 EU 0 Enable							
		Format: <input type="text"/> Enable							
		<table border="1"><thead><tr><th>Value</th><th>Name</th></tr></thead><tbody><tr><td>0</td><td>Enabled [Default]</td></tr><tr><td>1</td><td>Disabled</td></tr></tbody></table>		Value	Name	0	Enabled [Default]	1	Disabled
Value	Name								
0	Enabled [Default]								
1	Disabled								
	7	SubSlice 0 EU 7 Enable							
		Format: <input type="text"/> Enable							
		<table border="1"><thead><tr><th>Value</th><th>Name</th></tr></thead><tbody><tr><td>0</td><td>Enabled [Default]</td></tr><tr><td>1</td><td>Disabled</td></tr></tbody></table>		Value	Name	0	Enabled [Default]	1	Disabled
Value	Name								
0	Enabled [Default]								
1	Disabled								
	6	SubSlice 0 EU 6 Enable							
		Format: <input type="text"/> Enable							
		<table border="1"><thead><tr><th>Value</th><th>Name</th></tr></thead><tbody><tr><td>0</td><td>Enabled [Default]</td></tr><tr><td>1</td><td>Disabled</td></tr></tbody></table>		Value	Name	0	Enabled [Default]	1	Disabled
Value	Name								
0	Enabled [Default]								
1	Disabled								
	5	SubSlice 0 EU 5 Enable							
		Format: <input type="text"/> Enable							
		<table border="1"><thead><tr><th>Value</th><th>Name</th></tr></thead><tbody><tr><td>0</td><td>Enabled [Default]</td></tr><tr><td>1</td><td>Disabled</td></tr></tbody></table>		Value	Name	0	Enabled [Default]	1	Disabled
Value	Name								
0	Enabled [Default]								
1	Disabled								
	4	SubSlice 0 EU 4 Enable							
		Format: <input type="text"/> Enable							
		<table border="1"><thead><tr><th>Value</th><th>Name</th></tr></thead><tbody><tr><td>0</td><td>Enabled [Default]</td></tr><tr><td>1</td><td>Disabled</td></tr></tbody></table>		Value	Name	0	Enabled [Default]	1	Disabled
Value	Name								
0	Enabled [Default]								
1	Disabled								

TD_PM_MODE_EUCOUNT - EU Mask Programming

		SubSlice 0 EU 3 Enable						
	3	Format: <input type="text"/> Enable						
		<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center; background-color: #d9e1f2;">Value</th> <th style="text-align: center; background-color: #d9e1f2;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td><td>Enabled [Default]</td></tr> <tr> <td style="text-align: center;">1</td><td>Disabled</td></tr> </tbody> </table>	Value	Name	0	Enabled [Default]	1	Disabled
Value	Name							
0	Enabled [Default]							
1	Disabled							
	2	SubSlice 0 EU 2 Enable						
		Format: <input type="text"/> Enable						
		<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center; background-color: #d9e1f2;">Value</th> <th style="text-align: center; background-color: #d9e1f2;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td><td>Enabled [Default]</td></tr> <tr> <td style="text-align: center;">1</td><td>Disabled</td></tr> </tbody> </table>	Value	Name	0	Enabled [Default]	1	Disabled
Value	Name							
0	Enabled [Default]							
1	Disabled							
	1	SubSlice 0 EU 1 Enable						
		Format: <input type="text"/> Enable						
		<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center; background-color: #d9e1f2;">Value</th> <th style="text-align: center; background-color: #d9e1f2;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td><td>Enabled [Default]</td></tr> <tr> <td style="text-align: center;">1</td><td>Disabled</td></tr> </tbody> </table>	Value	Name	0	Enabled [Default]	1	Disabled
Value	Name							
0	Enabled [Default]							
1	Disabled							
	0	SubSlice 0 EU 0 Enable						
		Format: <input type="text"/> Enable						
		<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center; background-color: #d9e1f2;">Value</th> <th style="text-align: center; background-color: #d9e1f2;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td><td>Enabled [Default]</td></tr> <tr> <td style="text-align: center;">1</td><td>Disabled</td></tr> </tbody> </table>	Value	Name	0	Enabled [Default]	1	Disabled
Value	Name							
0	Enabled [Default]							
1	Disabled							

EventBus (U2C) - Boot Vector

EVTBUS0 - EventBus (U2C) - Boot Vector				
DWord	Bit	Description		
0	31:0	<p>EventBus Message - Boot Vector</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>These bits are not reset on FLR.</p>	Access:	R/W
Access:	R/W			
Uncore-to-Core messages are written in this register. RPM intercepts from eventbus and forwards to GPM. GPM monitors message channel for this address and sets flag to handle appropriately. Self-clears flag after sampling. IA cannot read/write to this register.				

EventBus (U2C) - CPD Vector

EVTBUS4 - EventBus (U2C) - CPD Vector				
DWord	Bit	Description		
0	31:0	<p>EventBus Message - CPD Vector</p> <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>These bits are not reset on FLR.</p>	Access:	R/W
Access:	R/W			

EventBus (U2C) - IDI Vector

EVTBUS1 - EventBus (U2C) - IDI Vector				
DWord	Bit	Description		
0	31:0	<p>EventBus Message - IDI Vector</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>These bits are not reset on FLR.</p>	Access:	R/W
Access:	R/W			

EventBus (U2C) - TSC LSB Vector

EVTBUS2 - EventBus (U2C) - TSC LSB Vector				
DWord	Bit	Description		
0	31:0	<p>EventBus Message - TSC LSB Vector</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>These bits are not reset on FLR.</p>	Access:	R/W
Access:	R/W			

EventBus (U2C) - TSC MSB Vector

EVTBUS3 - EventBus (U2C) - TSC MSB Vector						
DWord	Bit	Description				
0	31:0	<p>EventBus Message - TSC MSB Vector</p> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>These bits are not reset on FLR.</p>	Project:	BDW	Access:	R/W
Project:	BDW					
Access:	R/W					

Event selection and base counters

LPFCREG2 - Event selection and base counters				
DWord	Bit	Description		
0	31:24	<p>Counter 7 client</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Incf_lpfc_cnt7_client[7:0].</p> <p>Client Encoding (hex):</p> <ul style="list-style-type: none"> GAFS Rd 00 GAFS Wr 01 HDC0 Data Rd 02 HDC0 Const Rd 03 HDC0 URB Rd 04 HDC0 Data Wr 05 HDC0 URB Wr 06 HDC1 Data Rd 07 HDC1 Const Rd 08 HDC1 URB Rd 09 HDC1 Data Wr 0A HDC1 URB Wr 0B TDL0 Rd 0C TDL1 Rd 0D Tex0 Rd 0E Tex1 Rd 0F Tex2 Rd (reserved) 10 Tex3 Rd (reserved) 11 SBE Rd 12 IC0 Rd 13 IC1 Rd 14 SARB Rd 15 Aggregated Tex 16 SLM0 Rd 17 SLM1 Rd 18 SLM0 Wr 19 SLM1 Wr 1A SLM0 Atomics 1B SLM1 Atomics 1C Reserved 1D Reserved 1E Reserved 1F 	Access:	R/W
Access:	R/W			

LPFCREG2 - Event selection and base counters

	<p>FF Stalls 20 HDC Stalls 21 TDL Stalls 22 Texture Stalls 23 IC Stalls 24 SBE Stalls 25 SLM Stalls 26 Bank0 Total Hits 40 Bank0 Total Cycles 41 Bank0 Total Rds 42 Bank0 Total Wrs 43 Bank0 FF Rds 44 Bank0 FF Wrs 45 Bank0 DC Rds 46 Bank0 DC Wrs 47 Bank0 DC Hits 48 rsvd 49 Bank0 Tex Rds 4A Bank0 Tex Hits 4B Bank0 IC Rds 4C Bank0 IC Hits 4D Reserved 4E Reserved 4F Bank1 Events 50-5F (except 59-reserved) Bank2 Events 60-6F(except 69-reserved) Bank3 Events 70-7F(except 79-reserved) MSC Rd 80 MSC Wr 81 STC Rd 82 STC Wr 83 Hiz Rd 84 Hiz Wr 85 RCZ Rd 86 RCZ Wr 87 RCC Rd 88 RCC Wr 89 LTCD0 Err Corr EE LTCD1 Err Corr EF LTCD2 Err Corr F0 LTCD3 Err Corr F1 LTCD0 Err UnCorr F2 LTCD1 Err UnCorr F3 LTCD2 Err UnCorr F4 LTCD3 Err UnCorr F5 Counter#7 Client Selection: This field controls which client's request stream is observed in counter#7.</p>
--	---

LPFCREG2 - Event selection and base counters

	23:16	Counter 6 client	Access:	R/W
Incf_lpfc_cnt6_client[7:0]. Counter#6 Client Selection: This field controls which client's request stream is observed in counter#6.				
	15:8	Counter 5 client	Access:	R/W
Incf_lpfc_cnt5_client[7:0]. Counter#5 Client Selection: This field controls which client's request stream is observed in counter#5.				
	7:0	Counter 4 client	Access:	R/W
Incf_lpfc_cnt4_client[7:0]. Counter#4 Client Selection: This field controls which client's request stream is observed in counter#4.				

Event Selection and Base Counters1

LPFCREG1 - Event Selection and Base Counters1				
DWord	Bit	Description		
0	31:24	<p>Counter 3 client</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Incf_lpfc_cnt3_client[7:0]. Counter#3 Client Selection: This field controls which client's request stream is observed in counter#3.</p>	Access:	R/W
Access:	R/W			
23:16	<p>Counter 2 client</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Incf_lpfc_cnt2_client[7:0]. Counter#2 Client Selection: This field controls which client's request stream is observed in counter#2.</p>	Access:	R/W	
Access:	R/W			
15:8	<p>Counter 1 Client</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Incf_lpfc_cnt1_client[7:0]. Counter#1 Client Selection: This field controls which client's request stream is observed in counter#1.</p>	Access:	R/W	
Access:	R/W			
7:0	<p>Counter0 Client</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Incf_lpfc_cnt0_client[7:0]. Counter#0 Client Selection: This field controls which client's request stream is observed in counter#0.</p>	Access:	R/W	
Access:	R/W			

Execlist Status

EXECLIST_STATUS - Execlist Status			
Register Space:	MMIO: 0/2/0		
Project:	BDW		
Default Value:	0x00000001, 0x00000000		
Access:	RO		
Size (in bits):	64		
Address:	02234h-0223Bh		
Name:	RCS Execlist Status		
ShortName:	EXECLIST_STATUS_RCSUNIT		
Address:	12234h-1223Bh		
Name:	RCS Execlist Status		
ShortName:	EXECLIST_STATUS_VCSUNIT0		
Address:	1A234h-1A23Bh		
Name:	RCS Execlist Status		
ShortName:	EXECLIST_STATUS_VECSUNIT		
Address:	1C234h-1C23Bh		
Name:	RCS Execlist Status		
ShortName:	EXECLIST_STATUS_VCSUNIT1		
Address:	22234h-2223Bh		
Name:	RCS Execlist Status		
ShortName:	EXECLIST_STATUS_BCSUNIT		
This register contains the pointers and full indicator for the Execlist Queue and the context ID of the currently running context. DefaultValue = UUUU UUU1h (4:0 default to 00001b, others UNDEFINED).			
DWord	Bit	Description	
0	63:32	Current Context ID	
		Format:	U32
		Contains the context ID of the currently running context.	
	31:30	Reserved	
		Project:	BDW
		Format:	MBZ
29:27	Reserved		MBZ
		Format:	MBZ
26:19	Reserved		BDW
		Format:	MBZ

EXECLIST_STATUS - Execlist Status

	18	Reserved																	
	17	Reserved																	
	16	Arbitration Enable																	
		Project:	BDW																
		Format:	U1																
		This field reflects the Arbitration Flag set by the MI_ARB_ON_OFF command in Command Streamer.																	
	15:14	Current Active Element Status																	
		Project:	BDW																
		Format:	U2																
		Points at the element being executed in current Execlist (if there is one).																	
		<table border="1"> <thead> <tr> <th>Value</th><th colspan="2">Name</th></tr> </thead> <tbody> <tr> <td>00b</td><td colspan="2">No Active Element being executed</td></tr> <tr> <td>01b</td><td colspan="2">Element0 of current execlist being executed</td></tr> <tr> <td>10b</td><td colspan="2">Element1 of current execlist being executed</td></tr> <tr> <td>11b</td><td colspan="2">Reserved</td></tr> </tbody> </table>			Value	Name		00b	No Active Element being executed		01b	Element0 of current execlist being executed		10b	Element1 of current execlist being executed		11b	Reserved	
Value	Name																		
00b	No Active Element being executed																		
01b	Element0 of current execlist being executed																		
10b	Element1 of current execlist being executed																		
11b	Reserved																		
	13:5	Last Context Switch Reason																	
		Project:	BDW																
		Access:	R/W																
		Format:	U9																
		This field contains the switch reason for the last context to switch away, as captured in the Context Status Dword, bits 8:0.																	
		Programming Notes																	
		This field should not written by SW.																	
	4	Execlist 0 Valid																	
		Project:	BDW																
		Format:	Flag																
		This bit is set when the first DW for this Execlist port 0 is written through the submission port, and will not be cleared till the CSB is updated and the command stream is switching to the next execution list. If no execution list is pending, the transition of this bit from one to zero guarantees there will be no preemption on the next submission.																	
		<table border="1"> <thead> <tr> <th>Value</th><th colspan="2">Name</th></tr> </thead> <tbody> <tr> <td>0</td><td colspan="2">Invalid [Default]</td></tr> <tr> <td>1</td><td colspan="2">Valid</td></tr> </tbody> </table>			Value	Name		0	Invalid [Default]		1	Valid							
Value	Name																		
0	Invalid [Default]																		
1	Valid																		

EXECLIST_STATUS - Execlist Status

		Execlist 1 Valid											
	3	<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>Flag</td></tr> </table> <p>This bit is set when the first DW for this Execlist port 1 is written through the submission port, and will not be cleared till the CSB is updated and the command stream is switching to the next execution list. If no execution list is pending, the transition of this bit from one to zero guarantees there will be no preemption on the next submission.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0</td><td>Invalid [Default]</td></tr> <tr> <td>1</td><td>Valid</td></tr> </tbody> </table>	Project:	BDW	Format:	Flag	Value	Name	0	Invalid [Default]	1	Valid	
Project:	BDW												
Format:	Flag												
Value	Name												
0	Invalid [Default]												
1	Valid												
	2	Execlist Queue Full <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> </table> <p>When [Execlist Write Pointer] and [Current Execlist Pointer] are equal, this bit differentiates between Queue Full and Queue Empty.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0</td><td>Execlist Queue Empty [Default]</td><td></td></tr> <tr> <td>1</td><td>Execlist Queue Full</td><td>There is a current and a pending execlist.</td></tr> </tbody> </table>	Project:	BDW	Value	Name	Description	0	Execlist Queue Empty [Default]		1	Execlist Queue Full	There is a current and a pending execlist.
Project:	BDW												
Value	Name	Description											
0	Execlist Queue Empty [Default]												
1	Execlist Queue Full	There is a current and a pending execlist.											
	1	Execlist Write Pointer <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>ExeclistContentsIndex</td></tr> </table> <p>Determines which Execlist will be the next submitted to. When a new execlist is submitted, this pointer increments to point to the next execlist slot.</p>	Project:	BDW	Format:	ExeclistContentsIndex							
Project:	BDW												
Format:	ExeclistContentsIndex												
	0	Current Execlist Pointer <table border="1"> <tr> <td>Default Value:</td><td>1h</td></tr> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>ExeclistContentsIndex</td></tr> </table> <p>Points at the currently executing Execlist (if there is one). This pointer advances when the first context of new execlist is restored.</p>	Default Value:	1h	Project:	BDW	Format:	ExeclistContentsIndex					
Default Value:	1h												
Project:	BDW												
Format:	ExeclistContentsIndex												

Exelist Submit Port Register

EXECLIST_SUBMITPORT - Exelist Submit Port Register	
Register Space:	MMIO: 0/2/0
Project:	BDW
Default Value:	0x00000000
Access:	WO
Size (in bits):	32
Address:	02230h-02233h
Name:	Exelist Submit Port Register
ShortName:	EXECLIST_SUBMITPORT_RCSUNIT
Address:	12230h-12233h
Name:	Exelist Submit Port Register
ShortName:	EXECLIST_SUBMITPORT_VCSUNIT0
Address:	1A230h-1A233h
Name:	Exelist Submit Port Register
ShortName:	EXECLIST_SUBMITPORT_VECSUNIT
Address:	1C230h-1C233h
Name:	Exelist Submit Port Register
ShortName:	EXECLIST_SUBMITPORT_VCSUNIT1
Address:	22230h-22233h
Name:	Exelist Submit Port Register
ShortName:	EXECLIST_SUBMITPORT_BCSUNIT
SW should submit a new pending exelist to this register. The DWs of the context descriptors must be written in a specific order: Element 1 must be written first and then Element 0. For each Element, DW1 must be written first followed by DW0. Context descriptors for both the elements must be written even if only one context are being submitted. The valid bits of the unused context descriptors should be set to 0.	
Order of DW Submission to the Exelist Port	
Element 1, High Dword	
Element 1, Low Dword	
Element 0, High Dword	
Element 0, Low Dword	
If a exelist of only one element is being submitted, it must be submitted in Element 0. It is UNDEFINED to submit a exelist with the valid bit of Element 0 clear (an "empty" exelist). It is possible that one or all of the contexts submitted in a exelists are "empty"; that is, have head and tail pointers equal to each other indicating no commands to be run. All of the valid bits in the Exelist Element Status Registers for the "about to be submitted" exelist will be cleared when the first DW (DW1 of Element 1) is written to the submit port. Submission of the Element 0 Context Descriptor low Dword with the valid bit set is interpreted as a request to switch (as soon as possible) to the new exelist, i.e., a pre-emption request.	

EXECLIST_SUBMITPORT - Exelist Submit Port Register

If a submitted Exelist's Element 0 Context Descriptor LRCA matches the LRCA of the currently executing context, then the newly submitted exelist will become the currently executing exelist without any context switch and without any impact to the executing context except that it will re-sample the tail pointer from the context image. This is done in case more commands have been inserted into its ring buffer between the first exelist submission and the 2nd.

Programming Notes	Source			
SW must ensure the contexts submitted to both the context descriptors in the exelist are different, i.e SW must not submit the same context descriptor to both the elements of the exelist.				
Workaround	Source			
<p>Workaround :</p> <p>SW must always ensure there are valid commands to be executed by HW on a context submission, i.e ring buffer head pointer must not be equal to the ring buffer head pointer on context submission to HW for execution.</p> <p>Additional Note:</p> <p>This WA need not be applied when the arbitration is not disabled prior to executing "Batch Buffer Per Context Pointer" as part of context restore. Arbitration can be disabled prior to executing "Batch Buffer Per Context Pointer" by programming MI_ARB_ON_OFF (arbitration disable) in indirect context pointer.</p>	RenderCS			
<p>Workaround :</p> <p>SW must always ensure a preempted context submitted to HW doesn't undergo lite restore due to the same context getting submitted on the next Exelist submission.</p> <p>This can be achieved by setting "Force Restore Bit" in the context descriptor of the context getting submitted and if the same context is known to be submitted to HW for execution on the earlier Exelist submission Or</p> <p>SW on submitting a preempted context must wait for the context to switch out before submitting the same context to the Exelist Submit Port.</p> <p>Note:</p> <p>This WA need not be applied when "Force Sync Command Ordering" bit of INSTPM register is not disabled (programmed to value '0') during execution of "Batch Buffer Per Context Pointer" during context restore. "Force Sync Command Ordering" can be disabled prior to or during execution of "Batch Buffer Per Context Pointer" by programming INSTPM register using MI_LOAD_REGISTER_IMM command in Indirect Context Pointer or in "Batch Buffer Per Context Pointer".</p> <p>Disabling of "Force Sync Command Ordering" during "Batch Buffer Per Context Pointer" execution was required to address Resource Streamer related preemption issue, this WA is not applied when Resource Streamer (RS) is not enabled or when a Resource Streamer enabled context is not preemptable.</p>				
DWord	Bit	Description		
0	31:0	Context Descriptor DW <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Format:</td><td style="padding: 2px;">Context Descriptor</td></tr> </table>	Format:	Context Descriptor
Format:	Context Descriptor			

EXECLIST_SUBMITPORT - Execlist Submit Port Register

		See "Context Descriptor Format" for format. The element that this DW is submitted as and whether it is the high DW or the low DW is determined by order. This register must be written to 4 times in order to submit a execlist.
--	--	--

Execute Condition Code Register

EXCC - Execute Condition Code Register					
Register Space: MMIO: 0/2/0 Project: BDW Source: RenderCS Default Value: 0x00000000 Access: R/W, RO Size (in bits): 32 Trusted Type: 1					
Address: 02028h					
<p>This register contains user defined and hardware generated conditions that are used by MI_WAIT_FOR_EVENT commands. An MI_WAIT_FOR_EVENT instruction excludes the executing ring from arbitration if the selected event evaluates to a 1, while instruction is discarded if the condition evaluates to a 0. Once excluded a ring is enabled into arbitration when the selected condition evaluates to a 0.</p> <p>This register also contains control for the invalidation of indirect state pointers on context restore.</p>					
DWord	Bit	Description			
0	31:16	Mask Bits <table border="1"> <tr> <td>Format:</td><td>Mask[15:0]</td></tr> </table> <p>These bits serve as a write enable for bits 15:0. If this register is written with any of these bits clear the corresponding bit in the field 15:0 will not be modified. Reading these bits always returns 0s.</p>	Format:	Mask[15:0]	
Format:	Mask[15:0]				
15	Reserved <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	BDW	Format:	MBZ
Project:	BDW				
Format:	MBZ				
14	Context Wait for V-blank on Pipe-C <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> </table> <p>This field when set indicates the corresponding context has executed MI_WAIT_FOR_EVENT with "Display Pipe C Vertical Blank Wait Enable" set. This is an internal HW flag and should not be accessed by SW.</p>	Project:	BDW		
Project:	BDW				
13	Context Wait for V-blank on Pipe-B <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> </table> <p>This field when set indicates the corresponding context has executed MI_WAIT_FOR_EVENT with "Display Pipe B Vertical Blank Wait Enable" set. This is an internal HW flag and should not be accessed by SW.</p>	Project:	BDW		
Project:	BDW				
12	Context Wait for V-blank on Pipe-A <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> </table> <p>This field when set indicates the corresponding context has executed MI_WAIT_FOR_EVENT with "Display Pipe A Vertical Blank Wait Enable" set. This is an internal HW flag and should not be accessed by SW.</p>	Project:	BDW		
Project:	BDW				

EXCC - Execute Condition Code Register

	11	Pending Indirect State Dirty Bit	
		Project:	BDW
		Access:	RO
		This field keeps track of whether or not an indirect state pointer command has been parsed in the current context. Clears either on a context save or explicitly through a flush command. This bit is Read Only.	
	10:7	Pending Indirect State Counter	
		Project:	BDW
		This field keeps track of the maximum number of indirect state pointers pending in the system. When the register is saved/restored, it saves either a value of 1 or 0. This field is Read-Only.	
	6:5	Reserved	
		Format:	MBZ
	4:0	User Defined Condition Codes	
		The software may signal a Stream Semaphore by setting the Mask bit and Signal Bit together to match the bit field specified in a WAIT_FOR_EVENT (Semaphore).	

Extended Mode 4

EM4 - Extended Mode 4																							
Register Space: MMIO: 0/3/0 Project: BDW Default Value: 0x00000004 Access: R/W Size (in bits): 32																							
Address: 0100Ch-0100Fh																							
DWord	Bit	Description																					
0	31:18	Reserved																					
		Format:	MBZ																				
	17:0	MVALUE																					
		Default Value:	00004h																				
This is the M Value programming for the DDA. This M value is used to convert the 450MHz to 24MHz. Default value is 4. Below is the table for programming M value for different CDclk frequencies.																							
<table border="1"> <thead> <tr> <th>CDCLK FREQ</th><th>M Value</th><th>N Value</th><th>Comment</th></tr> </thead> <tbody> <tr> <td>450MHz</td><td>4 (4h)</td><td>75 (4Bh)</td><td>Default</td></tr> <tr> <td>337.5MHz</td><td>16 (10h)</td><td>225 (E1h)</td><td></td></tr> <tr> <td>540MHz</td><td>4 (4h)</td><td>90 (5Ah)</td><td></td></tr> <tr> <td>675</td><td>8 (8h)</td><td>225 (E1h)</td><td></td></tr> </tbody> </table>				CDCLK FREQ	M Value	N Value	Comment	450MHz	4 (4h)	75 (4Bh)	Default	337.5MHz	16 (10h)	225 (E1h)		540MHz	4 (4h)	90 (5Ah)		675	8 (8h)	225 (E1h)	
CDCLK FREQ	M Value	N Value	Comment																				
450MHz	4 (4h)	75 (4Bh)	Default																				
337.5MHz	16 (10h)	225 (E1h)																					
540MHz	4 (4h)	90 (5Ah)																					
675	8 (8h)	225 (E1h)																					

Extended Mode 5

EM5 - Extended Mode 5			
Register Space: MMIO: 0/3/0 Project: BDW Default Value: 0x00000004B Access: R/W Size (in bits): 32			
Address: 01010h-01013h			
DWord	Bit	Description	
0	31:18	Reserved	
		Format:	MBZ
	17:0	NVALUE	
		Default Value:	0004Bh
This is the N Value programming for the DDA. This N value is used to convert the 450MHz to 24MHz. Default value is 75. Below is the table to program N value for different CDclk frequencies.			
CDCLK FREQ			
450MHz	4 (4h)	75 (4Bh)	Default
337.5MHz	16 (10h)	225 (E1h)	
540MHz	4 (4h)	90 (5Ah)	
675MHz	8 (8h)	225 (E1h)	

Extra ECO Register

EXTRA_ECOREG - Extra ECO Register						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04590h					
DWord	Bit	Description				
0	31:0	Extra ECO Register <table border="1"><tr><td>Default Value:</td><td>0000000h</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> <p>Not currently used.</p>	Default Value:	0000000h	Access:	R/W
Default Value:	0000000h					
Access:	R/W					

FAULT_TLB_RD_DATA0 Register

FAULT_TLB_RD_DATA0 - FAULT_TLB_RD_DATA0 Register								
DWord	Bit	Description						
0	31:0	FAULT_TLB_READ_DATA0 Register <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> <tr> <td colspan="2">Fault cycle Virtual address [43:12]</td></tr> </table>	Default Value:	00000000h	Access:	RO	Fault cycle Virtual address [43:12]	
Default Value:	00000000h							
Access:	RO							
Fault cycle Virtual address [43:12]								

FAULT_TLB_RD_DATA1 Register

FAULT_TLB_RD_DATA1 - FAULT_TLB_RD_DATA1 Register												
DWord	Bit	Description										
0	31:0	FAULT_TLB_READ_DATA1 Register <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> <tr> <td>Bit[31:5] Reserved</td><td></td></tr> <tr> <td>Bit[4] Cycle GTT SEL (1-GGTT Cycle, 0-PPGTT Cycle)</td><td></td></tr> <tr> <td>Bit[3:0] Fault cycle Virtual address [47:44]</td><td></td></tr> </table>	Default Value:	00000000h	Access:	RO	Bit[31:5] Reserved		Bit[4] Cycle GTT SEL (1-GGTT Cycle, 0-PPGTT Cycle)		Bit[3:0] Fault cycle Virtual address [47:44]	
Default Value:	00000000h											
Access:	RO											
Bit[31:5] Reserved												
Bit[4] Cycle GTT SEL (1-GGTT Cycle, 0-PPGTT Cycle)												
Bit[3:0] Fault cycle Virtual address [47:44]												

Fault Switch Out

FAULT_SO - Fault SwitchOut		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04590h	
DWord	Bit	Description
0	31:0	Fault Switch Out
		Default Value: 00000000h
		Access: R/W

FBC_CFB_BASE

FBC_CFB_BASE				
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x00000000 Access: R/W Size (in bits): 32				
Address: 43200h-43203h Name: FBC Compressed Buffer Address ShortName: FBC_CFB_BASE Valid Projects: BDW Power: Always on Reset: soft				
Restriction				
The contents of this register must not be changed while compression is enabled.				
DWord	Bit	Description		
0	31:28	Reserved Format: MBZ		
	27:12	CFB Offset Address This register specifies bits 27:12 of the offset of the Compressed Frame Buffer from the base of stolen memory.		
	Programming Notes			
	The buffer must not overlap the top 8 MB of stolen memory.			
	Workaround			
The offset must be greater than 4K bytes, avoiding the first 4KB of stolen memory.				
Restriction				
The buffer must be 4K byte aligned.				
11:0	Reserved			
	Format:	MBZ		

FBC_CTL

FBC_CTL									
Register Space:	MMIO: 0/2/0								
Project:	BDW								
Default Value:	0x00000000								
Access:	R/W								
Size (in bits):	32								
Address:	43208h-4320Bh								
Name:	FBC Control								
ShortName:	FBC_CTL								
Valid Projects:	BDW								
Power:	Always on								
Reset:	soft								
Description									
FBC is tied to primary plane A.									
Programming Notes									
Frame Buffer Compression is only supported with surfaces up to 4096 pixels x 4096 lines. FBC is optimized to work best with surfaces up to 4096 pixels x 2048 lines.									
Restriction									
The contents of this register must not be changed, except the enable bit, while compression is enabled. Frame Buffer Compression is only supported with 16bpp and 32bpp 8:8:8 RGB plane source pixel formats. It is not supported with any other format. The 16bpp format requires the compression ratio to be set to 2:1 or 4:1.									
DWord	Bit	Description							
0	31	Enable FBC This bit is used to globally enable FBC function at the next Vertical Blank start. FBC should not be enabled when the pipe is disabled. <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Disable</td></tr> <tr> <td>1b</td><td>Enable</td></tr> </tbody> </table>		Value	Name	0b	Disable	1b	Enable
Value	Name								
0b	Disable								
1b	Enable								
Workaround									
Workaround (WaFbcExceedCdClockThreshold) : Do not enable FBC when the pipe pixel rate is greater than 95% of the CDCLK frequency. The pipe pixel rate is the port pixel rate multiplied by the pipe scaler down scale amount.									
Workaround (WaFbcAsynchFlipDisableFbcQueue) : Display register 420B0h bit 22 must be set to 1b for the entire time that Frame Buffer Compression is enabled.									

FBC_CTL

		FBC may intermittently fail to update some lines after an image change, causing stale data to appear. The stale data can be prevented by manually invalidating FBC after flips and enabling FBC. Manual invalidation sequence: For (i=0 to 127) { Write 0x50344 = (i«16) } The manual invalidation needs to happen in the frame that the image changes or FBC enables, between the start of vertical blank at the beginning of that frame and the start of vertical blank at the end of that frame. Recommended sequence: After submitting a flip or enabling FBC, wait for the next start of vblank (sync flips can alternatively wait for flip done), then perform the manual invalidation sequence.									
30:29	Reserved	Format: MBZ									
28	CPU Fence Enable	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="background-color: #d9e1f2; text-align: left; padding: 2px;">Value</th> <th style="background-color: #d9e1f2; text-align: left; padding: 2px;">Name</th> <th style="background-color: #d9e1f2; text-align: left; padding: 2px;">Description</th> </tr> </thead> <tbody> <tr> <td style="padding: 2px;">0b</td> <td style="padding: 2px;">No CPU Disp Buf</td> <td style="padding: 2px;">Display Buffer is not in a CPU fence. No modifications are allowed from CPU to the Display Buffer.</td> </tr> <tr> <td style="padding: 2px;">1b</td> <td style="padding: 2px;">CPU Disp Buf</td> <td style="padding: 2px;">Display Buffer exists in a CPU fence.</td> </tr> </tbody> </table>	Value	Name	Description	0b	No CPU Disp Buf	Display Buffer is not in a CPU fence. No modifications are allowed from CPU to the Display Buffer.	1b	CPU Disp Buf	Display Buffer exists in a CPU fence.
Value	Name	Description									
0b	No CPU Disp Buf	Display Buffer is not in a CPU fence. No modifications are allowed from CPU to the Display Buffer.									
1b	CPU Disp Buf	Display Buffer exists in a CPU fence.									
27:25	Reserved	Format: MBZ									
24:16	Reserved	Project: BDW									
15	Reserved										
14:11	Reserved	Format: MBZ									
10	Reserved										
9:8	Reserved										

FBC_CTL																	
	7:6	<p>Compression Limit</p> <p>This register sets a minimum limit on compression. This determines the maximum size of the compressed frame buffer. Display lines that do not meet the compression limit will not be compressed, so the best compression will be achieved with a 1:1 ratio.</p> <p>Compression Ratio 1, Pixel Format 16 bpp - Not Supported Compression Ratio 1, Pixel Format 32 bpp - Supported (CFB=FB) Compression Ratio 1/2, Pixel Format 16 bpp - Supported (CFB=FB) Compression Ratio 1/2, Pixel Format 32 bpp - Supported (CFB=1/2 FB) Compression Ratio 1/4, Pixel Format 16 bpp - Supported (CFB=1/2 FB) Compression Ratio 1/4, Pixel Format 32 bpp - Supported (CFB=1/4 FB)</p> <p>FB = Frame Buffer Size CFB = Compressed Frame Buffer Size</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>00b</td><td>1:1</td><td>Compressed buffer is the same size as the uncompressed buffer.</td></tr> <tr> <td>01b</td><td>2:1</td><td>Compressed buffer is one half the size of the uncompressed buffer.</td></tr> <tr> <td>10b</td><td>4:1</td><td>Compressed buffer is one quarter the size of the uncompressed buffer.</td></tr> <tr> <td>11b</td><td>Reserved</td><td>Reserved</td></tr> </tbody> </table>	Value	Name	Description	00b	1:1	Compressed buffer is the same size as the uncompressed buffer.	01b	2:1	Compressed buffer is one half the size of the uncompressed buffer.	10b	4:1	Compressed buffer is one quarter the size of the uncompressed buffer.	11b	Reserved	Reserved
Value	Name	Description															
00b	1:1	Compressed buffer is the same size as the uncompressed buffer.															
01b	2:1	Compressed buffer is one half the size of the uncompressed buffer.															
10b	4:1	Compressed buffer is one quarter the size of the uncompressed buffer.															
11b	Reserved	Reserved															
	5:4	<p>Write Back Watermark</p> <p>The compressed data write back engine waits for this number of entries to be ready before writing the data out to memory.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>00b</td><td>4</td><td>4 entries</td></tr> <tr> <td>01b</td><td>8</td><td>8 entries</td></tr> <tr> <td>10b</td><td>16</td><td>16 entries</td></tr> <tr> <td>11b</td><td>32</td><td>32 entries</td></tr> </tbody> </table>	Value	Name	Description	00b	4	4 entries	01b	8	8 entries	10b	16	16 entries	11b	32	32 entries
Value	Name	Description															
00b	4	4 entries															
01b	8	8 entries															
10b	16	16 entries															
11b	32	32 entries															
	3:0	<p>CPU Fence Number</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0000b</td><td>Fence 0</td></tr> </tbody> </table> <p>Restriction</p> <p>This field must be programmed to 0000b.</p>	Value	Name	0000b	Fence 0											
Value	Name																
0000b	Fence 0																

FBC_RT_BASE_ADDR_REGISTER

FBC_RT_BASE_ADDR_REGISTER - FBC_RT_BASE_ADDR_REGISTER											
Register Space: MMIO: 0/2/0 Project: BDW Source: RenderCS Default Value: 0x00000000 Access: R/W Size (in bits): 32											
Address: 07020h Valid Projects: [BDW]											
This Register is saved and restored as part of Context.											
DWord	Bit	Description									
0	31:12	FBC RT Base Address <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> <tr> <td>Format:</td><td>PPGraphicsAddress[31:12]</td></tr> </table> <p>4KB aligned Base Address as mapped in the PPGTT or in the GTT for the render target. This base address must be the one that is either front buffer or the back-buffer (a flip target). It must be programmed before any draw call binding that render target base address.</p>	Access:	R/W	Format:	PPGraphicsAddress[31:12]					
Access:	R/W										
Format:	PPGraphicsAddress[31:12]										
Reserved <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> <tr> <td>Format:</td><td>PBC</td></tr> </table>	Access:	R/W	Format:	PBC							
Access:	R/W										
Format:	PBC										
FBC Front Buffer Target <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> <tr> <td>Format:</td><td>Enable</td></tr> </table>	Project:	BDW	Access:	R/W	Format:	Enable					
Project:	BDW										
Access:	R/W										
Format:	Enable										
<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0h</td><td>[Default]</td><td>FBC is targeting the Back Buffer for compression. This buffer can be cached in the MLC/LLC, so a GFDT flush is required before FBC can begin compression.</td></tr> <tr> <td>1h</td><td></td><td>FBC is targeting the Font Buffer for compression. This buffer cannot be cached in the MLC/LLC. FBC compression can begin after any RC flush.</td></tr> </tbody> </table>			Value	Name	Description	0h	[Default]	FBC is targeting the Back Buffer for compression. This buffer can be cached in the MLC/LLC, so a GFDT flush is required before FBC can begin compression.	1h		FBC is targeting the Font Buffer for compression. This buffer cannot be cached in the MLC/LLC. FBC compression can begin after any RC flush.
Value	Name	Description									
0h	[Default]	FBC is targeting the Back Buffer for compression. This buffer can be cached in the MLC/LLC, so a GFDT flush is required before FBC can begin compression.									
1h		FBC is targeting the Font Buffer for compression. This buffer cannot be cached in the MLC/LLC. FBC compression can begin after any RC flush.									

FBC_RT_BASE_ADDR_REGISTER - FBC_RT_BASE_ADDR_REGISTER

	0	PPGTT Render Target Base Address Valid for FBC			
		Project:		BDW	
		Access:		R/W	
		Format:		Enable	
Value	Name	Description			Project
0h	[Default]	Base address in this register [31:12] is not valid and therefore FBC will not get any modifications from rendering.			BDW
1h		Base address in this register [31:12] is valid and HW needs to compare the current render target base address with this base address to provide modifications to FBC.			BDW

FBC_RT_BASE_ADDR_REGISTER_UPPER

FBC_RT_BASE_ADDR_REGISTER_UPPER - FBC_RT_BASE_ADDR_REGISTER_UPPER		
DWord	Bit	Description
0	31:16	Reserved Access: R/W Format: PBC
	15:0	FBC RT Base Address High Access: R/W Format: BaseAddress[47:32] <p>Must be set to modify corresponding data bit. Reads to this field returns zero. Upper 4KB aligned Base Address as mapped in the PPGTT or in the GTT for the render target. This base address must be the one that is either front buffer or the back-buffer (a flip target). It can be only programmed once per context.</p>
		Programming Notes It must be programmed before any draw call binding that render target base address.

FDI_RX_CTL

FDI_RX_CTL											
Register Space:	MMIO: 0/2/0										
Project:	DevLPT:H										
Default Value:	0x00000040										
Access:	R/W										
Size (in bits):	32										
Double Buffer Update Point:	Depends on bit										
Address:	F000Ch-F000Fh										
Name:	FDI A RX Control										
ShortName:	FDI_RX_CTL_A										
Power:	Always on										
Reset:	soft										
The FDI Receiver only operates in 8 bit per color mode. The FDI Receiver only operates in composite sync mode.											
DWord	Bit	Description									
0	31	FDI Rx Enable Disabling this port will put it in its lowest power state. <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Disable</td><td>Disable the FDI Rx interface</td></tr> <tr> <td>1b</td><td>Enable</td><td>Enable the FDI Rx interface</td></tr> </tbody> </table>	Value	Name	Description	0b	Disable	Disable the FDI Rx interface	1b	Enable	Enable the FDI Rx interface
Value	Name	Description									
0b	Disable	Disable the FDI Rx interface									
1b	Enable	Enable the FDI Rx interface									
30:28	Reserved Format: MBZ										
27	FS error correction enable This bit enables the Fill Start error correction over FDI. <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Disable</td><td>Disable FS Error Correction</td></tr> <tr> <td>1b</td><td>Enable</td><td>Enable FS Error Correction</td></tr> </tbody> </table>	Value	Name	Description	0b	Disable	Disable FS Error Correction	1b	Enable	Enable FS Error Correction	
Value	Name	Description									
0b	Disable	Disable FS Error Correction									
1b	Enable	Enable FS Error Correction									
26	FE error correction enable This bit enables the Fill End error correction over FDI. <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Disable</td><td>Disable FE Error Correction</td></tr> <tr> <td>1b</td><td>Enable</td><td>Enable FE Error Correction</td></tr> </tbody> </table>	Value	Name	Description	0b	Disable	Disable FE Error Correction	1b	Enable	Enable FE Error Correction	
Value	Name	Description									
0b	Disable	Disable FE Error Correction									
1b	Enable	Enable FE Error Correction									
25	FS error reporting enable This bit enables the FS error reporting over FDI. <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Disable</td><td>Disable FS Error Reporting</td></tr> <tr> <td>1b</td><td>Enable</td><td>Enable FS Error Reporting</td></tr> </tbody> </table>	Value	Name	Description	0b	Disable	Disable FS Error Reporting	1b	Enable	Enable FS Error Reporting	
Value	Name	Description									
0b	Disable	Disable FS Error Reporting									
1b	Enable	Enable FS Error Reporting									

FDI_RX_CTL														
24	FE error reporting enable This bit enables the FE error reporting over FDI.													
	<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Disable</td><td>Disable FE Error Reporting</td></tr> <tr> <td>1b</td><td>Enable</td><td>Enable FE Error Reporting</td></tr> </tbody> </table>	Value	Name	Description	0b	Disable	Disable FE Error Reporting	1b	Enable	Enable FE Error Reporting				
Value	Name	Description												
0b	Disable	Disable FE Error Reporting												
1b	Enable	Enable FE Error Reporting												
23:20	Reserved Format:	MBZ												
19	Port Width Selection These bits select the number of lanes to be enabled on the link. Port width change must be done as a part of mode set. Locked once port is enabled. Updates when the port is disabled then re-enabled													
	<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>x1 Mode</td><td>x1 Mode</td></tr> <tr> <td>1b</td><td>x2 Mode</td><td>x2 Mode</td></tr> <tr> <td>Others</td><td>Reserved</td><td>Reserved</td></tr> </tbody> </table>	Value	Name	Description	0b	x1 Mode	x1 Mode	1b	x2 Mode	x2 Mode	Others	Reserved	Reserved	
Value	Name	Description												
0b	x1 Mode	x1 Mode												
1b	x2 Mode	x2 Mode												
Others	Reserved	Reserved												
18:17	Reserved Format:	MBZ												
16	Polarity Reversal This bit allows FDI to work with polarity reversal. It must be set before the link is enabled.													
	<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Not Reversed</td><td>Polarity not reversed.</td></tr> <tr> <td>1b</td><td>Polarity Reversed</td><td>Polarity reversed.</td></tr> </tbody> </table>	Value	Name	Description	0b	Not Reversed	Polarity not reversed.	1b	Polarity Reversed	Polarity reversed.				
Value	Name	Description												
0b	Not Reversed	Polarity not reversed.												
1b	Polarity Reversed	Polarity reversed.												
15	Link reversal strap override FDI link automatically follows the DMI link reversal setting. This bit overrides that to the opposite of what DMI is set to. It must be set before the link is enabled in order to take effect.													
	<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Not Overriden</td><td>Link reversal strap not overriden</td></tr> <tr> <td>1b</td><td>Overriden</td><td>Link reversal strap overriden.</td></tr> </tbody> </table>	Value	Name	Description	0b	Not Overriden	Link reversal strap not overriden	1b	Overriden	Link reversal strap overriden.				
Value	Name	Description												
0b	Not Overriden	Link reversal strap not overriden												
1b	Overriden	Link reversal strap overriden.												
14	DMI Link reversal status Access:	RO												
	This bit reflects the DMI link reversal strap.													
	<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Not Reversed</td><td>Link not reversed</td></tr> <tr> <td>1b</td><td>Reversed</td><td>Link reversed.</td></tr> </tbody> </table>	Value	Name	Description	0b	Not Reversed	Link not reversed	1b	Reversed	Link reversed.				
Value	Name	Description												
0b	Not Reversed	Link not reversed												
1b	Reversed	Link reversed.												

FDI_RX_CTL															
13	FDI PLL enable Format: This bit enables the FDI PLL.	Enable													
Restriction															
After enabling the FDI PLL, software must wait for a warmup period before enabling the link. See the mode set sequence for more detail.															
12:11	Reserved Format:	MBZ													
10	FDI Auto Train This bit enables FDI auto-training on this port.	<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Disable</td><td>Disable FDI auto-training</td></tr> <tr> <td>1b</td><td>Enable</td><td>Enable FDI auto-training</td></tr> </tbody> </table>	Value	Name	Description	0b	Disable	Disable FDI auto-training	1b	Enable	Enable FDI auto-training				
Value	Name	Description													
0b	Disable	Disable FDI auto-training													
1b	Enable	Enable FDI auto-training													
9:8	Reserved														
7	Reserved														
6	Enhanced Framing Enable This bit selects enhanced framing. Locked once port is enabled. Updates when the port is disabled then re-enabled	<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Disable</td><td>Enhanced framing disabled</td></tr> <tr> <td>1b</td><td>Enable [Default]</td><td>Enhanced framing enabled</td></tr> </tbody> </table>	Value	Name	Description	0b	Disable	Enhanced framing disabled	1b	Enable [Default]	Enhanced framing enabled				
Value	Name	Description													
0b	Disable	Enhanced framing disabled													
1b	Enable [Default]	Enhanced framing enabled													
5	Reserved Format:	MBZ													
4	Rawclk to PCDCLK selection This bit switches PCH display clocking between the raw clock and PCDCLK.	<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Rawclk</td><td>Raw clock used</td></tr> <tr> <td>1b</td><td>PCDCLK</td><td>PCDCLK used</td></tr> </tbody> </table> <table border="1"> <thead> <tr> <th colspan="2">Restriction</th></tr> </thead> <tbody> <tr> <td colspan="2">This bit may be changed only at certain times. See the mode set sequence for more detail.</td></tr> </tbody> </table>	Value	Name	Description	0b	Rawclk	Raw clock used	1b	PCDCLK	PCDCLK used	Restriction		This bit may be changed only at certain times. See the mode set sequence for more detail.	
Value	Name	Description													
0b	Rawclk	Raw clock used													
1b	PCDCLK	PCDCLK used													
Restriction															
This bit may be changed only at certain times. See the mode set sequence for more detail.															
3:0	Reserved Format:	MBZ													

FDI_RX_IIR

FDI_RX_IIR											
DWord	Bit	Description									
0	31:0	<p>Interrupt Identity Bits</p> <p>This field holds the persistent values of the FDI_RX interrupt bits which are unmasked by the FDI_RX_IMR. Bits set in this register will propagate to the combined FDI_RX interrupt in the SDE_ISR. Bits set in this register will remain set (persist) until the interrupt condition is cleared by writing a '1' to the appropriate bits.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Condition Not Detected</td> <td>Interrupt Condition Not Detected</td> </tr> <tr> <td>1b</td> <td>Condition Detected</td> <td>Interrupt Condition Detected</td> </tr> </tbody> </table>	Value	Name	Description	0b	Condition Not Detected	Interrupt Condition Not Detected	1b	Condition Detected	Interrupt Condition Detected
Value	Name	Description									
0b	Condition Not Detected	Interrupt Condition Not Detected									
1b	Condition Detected	Interrupt Condition Detected									
		See the interrupt bit definition table to find the source event for each interrupt bit.									

FDI_RX_IMR

FDI_RX_IMR											
Register Space:	MMIO: 0/2/0										
Project:	DevLPT:H										
Default Value:	0x00000000										
Access:	R/W										
Size (in bits):	32										
Address:	F0018h-F001Bh										
Name:	FDI A RX Interrupt Mask										
ShortName:	FDI_RX_IMR_A										
Power:	Always on										
Reset:	soft										
See the interrupt bit definition table to find the source event for each interrupt bit.											
DWord	Bit	Description									
0	31:0	<p>Interrupt Mask Bits</p> <p>This field contains a bit mask which selects which FDI_RX events are reported in the FDI_RX_IIR.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Not Masked</td><td>Not Masked - will be reported in the FDI_RX_IIR</td></tr> <tr> <td>1b</td><td>Masked</td><td>Masked - will not be reported in the FDI_RX_IIR</td></tr> </tbody> </table>	Value	Name	Description	0b	Not Masked	Not Masked - will be reported in the FDI_RX_IIR	1b	Masked	Masked - will not be reported in the FDI_RX_IIR
Value	Name	Description									
0b	Not Masked	Not Masked - will be reported in the FDI_RX_IIR									
1b	Masked	Masked - will not be reported in the FDI_RX_IIR									

FDI_RX_MISC

FDI_RX_MISC											
Register Space: MMIO: 0/2/0 Project: DevLPT:H Default Value: 0x00200080 Access: R/W Size (in bits): 32											
Address: F0010h-F0013h Name: FDI A RX Miscellaneous ShortName: FDI_RX_MISC_A Power: Always on Reset: soft											
DWord	Bit	Description									
0	31:28	Reserved	Format: MBZ								
	27:26	Reserved	Default Value: 00h								
	25:24	Reserved	Default Value: 00h								
	23:22	Reserved	Format: MBZ								
	21:20	TP1 to TP2 Time	These bits select the number of link clocks to count before transitioning from TP1 to TP2 during auto training.								
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>10b</td><td>48 [Default]</td><td>48 clocks</td></tr> <tr> <td>11b</td><td>64</td><td>64 clocks</td></tr> </tbody> </table>	Value	Name	Description	10b	48 [Default]	48 clocks	11b	64	64 clocks
Value	Name	Description									
10b	48 [Default]	48 clocks									
11b	64	64 clocks									
Workaround											
This register must be written with the default TP1 to TP2 time before enabling FDI.											
19	Reserved	Format:	MBZ								

FDI_RX_MISC																													
	18:16	<p>Bit Lock Timeout Time These bits select the number of link clocks to count before timing out on bit lock during auto training.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>000b</td><td>128 [Default]</td><td>128 clocks</td></tr> <tr> <td>001b</td><td>256</td><td>256 clocks</td></tr> <tr> <td>010b</td><td>384</td><td>384 clocks</td></tr> <tr> <td>011b</td><td>512</td><td>512 clocks</td></tr> <tr> <td>100b</td><td>640</td><td>640 clocks</td></tr> <tr> <td>101b</td><td>768</td><td>768 clocks</td></tr> <tr> <td>110b</td><td>896</td><td>896 clocks</td></tr> <tr> <td>111b</td><td>1024</td><td>1024 clocks</td></tr> </tbody> </table>	Value	Name	Description	000b	128 [Default]	128 clocks	001b	256	256 clocks	010b	384	384 clocks	011b	512	512 clocks	100b	640	640 clocks	101b	768	768 clocks	110b	896	896 clocks	111b	1024	1024 clocks
Value	Name	Description																											
000b	128 [Default]	128 clocks																											
001b	256	256 clocks																											
010b	384	384 clocks																											
011b	512	512 clocks																											
100b	640	640 clocks																											
101b	768	768 clocks																											
110b	896	896 clocks																											
111b	1024	1024 clocks																											
	15:13	<p>Reserved</p> <table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ																									
Format:	MBZ																												
	12:0	<p>FDI Delay This field specifies latency as relative delay with respect to the dot clock required for active data over the FDI interface to reach the timing generator FIFO in the transcoder.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>80h</td><td>80h [Default]</td><td>Default</td></tr> <tr> <td>90h</td><td>90h</td><td>Required for all FDI configurations</td></tr> </tbody> </table> <p>Workaround</p> <p>Program 90h when FDI is used.</p>	Value	Name	Description	80h	80h [Default]	Default	90h	90h	Required for all FDI configurations																		
Value	Name	Description																											
80h	80h [Default]	Default																											
90h	90h	Required for all FDI configurations																											

FDI_RX_TUSIZE

FDI_RX_TUSIZE							
Register Space: MMIO: 0/2/0 Project: DevLPT:H Default Value: 0x7E000000 Access: R/W Size (in bits): 32							
Address: F0030h-F0033h Name: FDI A RX TU Size 1 ShortName: FDI_RX_TUSIZE_1_A Power: Always on Reset: soft							
Restriction							
The FDI Receiver TU size must be programmed to match the TU size used by the FDI Transmitter.							
DWord	Bit	Description					
0	31	Reserved <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Format:</td><td style="padding: 2px;">MBZ</td></tr> </table>	Format:	MBZ			
Format:	MBZ						
30:25	TU Size This field is the size of the transfer unit for FDI, minus one. <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%;">Value</th><th style="width: 50%;">Name</th></tr> </thead> <tbody> <tr> <td style="padding: 2px;">111111b</td><td style="padding: 2px;">63 [Default]</td></tr> <tr> <td style="padding: 2px;">[1,63]</td><td style="padding: 2px;"></td></tr> </tbody> </table>	Value	Name	111111b	63 [Default]	[1,63]	
Value	Name						
111111b	63 [Default]						
[1,63]							
24:0	Reserved <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Format:</td><td style="padding: 2px;">MBZ</td></tr> </table>	Format:	MBZ				
Format:	MBZ						

FDI Receiver Interrupt Bit Definition

FDI Receiver Interrupt Bit Definition				
DWord	Bit	Description		
0	31:12	Reserved <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ
Format:	MBZ			
11	FDI RX Bit Lock Timeout This indicates that bit lock timeout occurred.			
10	FDI RX Interlane Alignment This indicates all the lanes are properly inter-lane aligned.			
9	FDI RX Symbol Lock This indicates training pattern 2 was received successfully on all the enabled lanes.			
8	FDI RX Bit Lock This indicates training pattern 1 was received successfully on all the enabled lanes.			
7	FDI RX Training Pattern 2 Fail This indicates that the training pattern 2 has failed.			
6	FS Code Error This reports the Fill Start code missing condition.			
5	FE Code Error This reports the Fill End code missing condition.			
4	FDI RX High Symbol Error Rate This indicates the received symbol error rate is more than one error in 10^{10} symbols.			
3	Reserved <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ	
Format:	MBZ			
2	FDI RX Pixel FIFO Overflow This indicates the Pixel FIFO overflowed.			
1	FDI RX Cross Clock FIFO Overflow This indicates the cross clock symbol clock to display clock FIFO overflowed.			
0	FDI RX Symbol Queue overflow This indicates the symbol queue overflowed.			

Fence Control Register

MFCR - Fence Control Register										
Fence Control Register										
DWord	Bit	Description								
0	31	Fuse Override Lock <table border="1"> <tr> <td>Access:</td> <td>R/W Lock</td> </tr> <tr> <td colspan="2">SW Fuse Override Lock Bit</td></tr> </table>	Access:	R/W Lock	SW Fuse Override Lock Bit					
Access:	R/W Lock									
SW Fuse Override Lock Bit										
	30:24	ECORSVD <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td colspan="2">ECO purposes Reserved</td></tr> </table>	Project:	BDW	Access:	R/W	ECO purposes Reserved			
Project:	BDW									
Access:	R/W									
ECO purposes Reserved										
	23:22	GT VBOX DISABLE FUSE OVERRIDE <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Access:</td> <td>R/W Lock</td> </tr> <tr> <td colspan="2">SW GT Vbox Disable Fuse Override Bits</td></tr> </table>	Project:	BDW	Access:	R/W Lock	SW GT Vbox Disable Fuse Override Bits			
Project:	BDW									
Access:	R/W Lock									
SW GT Vbox Disable Fuse Override Bits										
	21:19	GT SUBSLICE DISABLE FUSE OVERRIDE <table border="1"> <tr> <td>Access:</td> <td>R/W Lock</td> </tr> <tr> <td colspan="2">SW GT SubSlice Disable Fuse Override Bits</td></tr> </table>	Access:	R/W Lock	SW GT SubSlice Disable Fuse Override Bits					
Access:	R/W Lock									
SW GT SubSlice Disable Fuse Override Bits										
	18:16	GT SLICE ENABLE FUSE OVERRIDE <table border="1"> <tr> <td>Default Value:</td> <td>111b</td> </tr> <tr> <td>Access:</td> <td>R/W Lock</td> </tr> <tr> <td colspan="2">SW GT Slice Enable Fuse Override Bits</td></tr> </table>	Default Value:	111b	Access:	R/W Lock	SW GT Slice Enable Fuse Override Bits			
Default Value:	111b									
Access:	R/W Lock									
SW GT Slice Enable Fuse Override Bits										
	15:5	RSVD <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO						
Access:	RO									
	4	Reserved								
	3	Reserved								
	2	Write/Read Port Block <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td colspan="2">0 - Dont Block the R/W port when Query is started.</td></tr> <tr> <td colspan="2">1 - Block the R/W port until the Memory Fence is completed.</td></tr> <tr> <td colspan="2">This is applicable for only Memory Fence.</td></tr> </table>	Access:	R/W	0 - Dont Block the R/W port when Query is started.		1 - Block the R/W port until the Memory Fence is completed.		This is applicable for only Memory Fence.	
Access:	R/W									
0 - Dont Block the R/W port when Query is started.										
1 - Block the R/W port until the Memory Fence is completed.										
This is applicable for only Memory Fence.										

MFCR - Fence Control Register

	1	LLC Query Enable		
		<table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>0 - Query for 16 Ways. 1 - Query for 32 Ways. No Flexing.</p>	Access:	R/W
Access:	R/W			
	0	Fence Controller GFDT Mode		
		<table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Fence Controller GFDT Mode. 0 - Single bit GFDT mode. 1 - Two bit GFDT mode.</p>	Access:	R/W
Access:	R/W			

FF Performance

FF_PERF - FF Performance														
DWord	Bit	Description												
0	31:16	<p>Mask</p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Access:</td> <td>WO</td> </tr> <tr> <td>Format:</td> <td>Mask[15:0]</td> </tr> </table> <p>Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)</p>	Project:	All	Access:	WO	Format:	Mask[15:0]						
Project:	All													
Access:	WO													
Format:	Mask[15:0]													
	15:11	<p>Reserved</p> <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Access:</td> <td>r/w</td> </tr> <tr> <td>Format:</td> <td>PBC</td> </tr> </table>	Project:	All	Access:	r/w	Format:	PBC						
Project:	All													
Access:	r/w													
Format:	PBC													
	10:8	<p>Throttle counter value</p> <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Access:</td> <td>r/w</td> </tr> <tr> <td>Format:</td> <td>Disable</td> </tr> </table> <p>Counter value defining how many clocks the interface needs to be slowed down.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>[Default]</td> <td>Masked by default.</td> </tr> </tbody> </table>	Project:	BDW	Access:	r/w	Format:	Disable	Value	Name	Description	0h	[Default]	Masked by default.
Project:	BDW													
Access:	r/w													
Format:	Disable													
Value	Name	Description												
0h	[Default]	Masked by default.												
	7:3	<p>Reserved</p> <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Access:</td> <td>r/w</td> </tr> <tr> <td>Format:</td> <td>PBC</td> </tr> </table>	Project:	BDW	Access:	r/w	Format:	PBC						
Project:	BDW													
Access:	r/w													
Format:	PBC													

FF_PERF - FF Performance											
	2	Enable throttling for SF-WM interface									
		<table border="1"> <tr> <td>Access:</td><td>r/w</td></tr> <tr> <td>Format:</td><td>Disable</td></tr> </table>	Access:	r/w	Format:	Disable					
Access:	r/w										
Format:	Disable										
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0h</td><td>Disable</td><td>No throttling</td></tr> <tr> <td>1h</td><td>Enable</td><td>Enable throttling in all SF-WM interfaces</td></tr> </tbody> </table>	Value	Name	Description	0h	Disable	No throttling	1h	Enable	Enable throttling in all SF-WM interfaces
Value	Name	Description									
0h	Disable	No throttling									
1h	Enable	Enable throttling in all SF-WM interfaces									
	1	Enable throttling for SF-SBE interface									
		<table border="1"> <tr> <td>Access:</td><td>r/w</td></tr> <tr> <td>Format:</td><td>Disable</td></tr> </table>	Access:	r/w	Format:	Disable					
Access:	r/w										
Format:	Disable										
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0h</td><td>Disable</td><td>No throttling</td></tr> <tr> <td>1h</td><td>Enable</td><td>Enable throttling in all SF-SBE interfaces</td></tr> </tbody> </table>	Value	Name	Description	0h	Disable	No throttling	1h	Enable	Enable throttling in all SF-SBE interfaces
Value	Name	Description									
0h	Disable	No throttling									
1h	Enable	Enable throttling in all SF-SBE interfaces									
	0	Enable throttling for CL-SF interface									
		<table border="1"> <tr> <td>Access:</td><td>r/w</td></tr> <tr> <td>Format:</td><td>Disable</td></tr> </table>	Access:	r/w	Format:	Disable					
Access:	r/w										
Format:	Disable										
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0h</td><td>Disable</td><td>No throttling</td></tr> <tr> <td>1h</td><td>Enable</td><td>Enable throttling in all CL-SF interfaces</td></tr> </tbody> </table>	Value	Name	Description	0h	Disable	No throttling	1h	Enable	Enable throttling in all CL-SF interfaces
Value	Name	Description									
0h	Disable	No throttling									
1h	Enable	Enable throttling in all CL-SF interfaces									

MSG_FIFO_MGSR - FIFO Messaging Register for Shadow Register Unit

MSG_FIFO_MGSR - FIFO Messaging Register for Shadow Register Unit

Register Space: MMIO: 0/2/0

Project: BDW

Default Value: 0x00000000

Size (in bits): 16

Address: 0803Ch

Message registers have bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16].

To set bit0, for example, the data would be 0x0001_0001.

To clear bit0, for example, the data would be 0x0001_0000.

Note that mask bit is the data bit offset + 16.

Message registers are protected from non-GT writes via the Message Channel.

DWord	Bit	Description	
0	15:1	Reserved	
		Project:	BDW
		Access:	RO
	0	Acknowledge that GT FIFO has been Blocked	
		Access:	R/W
		Acknowledge that GT FIFO has been Blocked. 1'b0: No meaning unless FIFO block request was sent (default). 1'b1: GT FIFO has been blocked. Note that the block request goes to MGSR, and MGSR responds to GPM with the blocked ack. Note that the unblock request goes to MGSR, and MBC responds to GPM with the unblocked ack (aka BOOT_FETCH_DONE). GPMunit self-clears this bit upon sampling.	

First Buffer Size and Start

FBSS - First Buffer Size and Start					
DWord	Bit	Description			
0	31:16	<p>First Virtual Buffer Base</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>First Virtual Buffer Base: Programmed by driver to allocate a memory space for performance data storage. The buffer size should be aligned to the size of the memory allocated so it naturally aligns to the base (i.e. for 128KB bit[16]=0, 256KB bit[17:16]=0, 512KB bit[18:16]=0). Signal - lpconf_lpfc_virtual_base0 [31:16].</p>	Access:	R/W	
Access:	R/W				
15:12	<p>First Buffer Size</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>First Buffer Size: Determines the allowed buffer size for performance data storage. 0000b: 64KB. 0001b: 128KB. 0010b: 256KB. 0011b: 512KB. ... 1111b: 2GB. Signal - lpconf_lpfc_buffer_size0 [3:0].</p>	Access:	R/W		
Access:	R/W				
11:3	<p>Reserved</p> <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Reserved.</p>	Project:	BDW	Access:	RO
Project:	BDW				
Access:	RO				

FBSS - First Buffer Size and Start														
	2	<p>Frame count and Draw call enable</p> <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Enables the replacement of a specific L3 performance counter value in the reported data with a 16-bit tag created from the concatenation of the "Frame Count" and "Draw Call Number" programmable bitfields in the "Frame Count and Draw Call Number" register.</p> <p>The exact counter replaced is dependent on the programmed value of the "Counter Enabling Selection" bitfield. The replaced counter is always the last one, except in the case only a single performance counter is enabled for reporting (in which no replacement occurs):</p> <table border="1"> <thead> <tr> <th>CNTRENSEL Value</th><th>Replaced Event Counter</th></tr> </thead> <tbody> <tr> <td>00</td><td>No Replacement</td></tr> <tr> <td>01</td><td>Counter 1</td></tr> <tr> <td>10</td><td>Counter 3</td></tr> <tr> <td>11</td><td>Counter 7</td></tr> </tbody> </table>	Access:	R/W	CNTRENSEL Value	Replaced Event Counter	00	No Replacement	01	Counter 1	10	Counter 3	11	Counter 7
Access:	R/W													
CNTRENSEL Value	Replaced Event Counter													
00	No Replacement													
01	Counter 1													
10	Counter 3													
11	Counter 7													
	1	Reserved												
	0	<p>Master Counter Enable</p> <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Master Counter Enable: This is the global enable for performance tracking. Once set, it kicks off all performance tracking mechanism.</p> <p>Signal - lpconf_lpfcc_master_cnt_en.</p> <p>This bit is used by all slices.</p>	Access:	R/W										
Access:	R/W													

Flexible EU Event Control 0

EU_PERF_CNT_CTL0 - Flexible EU Event Control 0						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Access:	R/W					
Size (in bits):	32					
Address:	0E458h					
This register configures flexible EU event 0/1. Please refer to the description of the flexible EU events for more details on supported events. Please note that this register is render context saved/restored.						
DWord	Bit	Description				
0	31:24	<p>Reserved</p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	All	Format:	MBZ
Project:	All					
Format:	MBZ					
23:20	<p>Fine Event Filter Select EU event 1</p> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>U4</td></tr> </table> <p>This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 1. Note that the fine event filter is logically applied after the coarse event filter.</p>	Project:	BDW	Format:	U4	
Project:	BDW					
Format:	U4					
19:16	<p>Coarse Event Filter Select EU event 1</p> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>U4</td></tr> </table> <p>This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 1. Note that the coarse event filter is logically applied before the fine event filter.</p>	Project:	BDW	Format:	U4	
Project:	BDW					
Format:	U4					
15:12	<p>Increment Event for EU event 1</p> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>U4</td></tr> </table> <p>This field controls which increment event provides the basis for flexible EU event 1.</p>	Project:	BDW	Format:	U4	
Project:	BDW					
Format:	U4					
11:8	<p>Fine Event Filter Select EU event 0</p> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>U4</td></tr> </table> <p>This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 0. Note that the fine event filter is logically applied after the coarse event filter.</p>	Project:	BDW	Format:	U4	
Project:	BDW					
Format:	U4					

EU_PERF_CNT_CTL0 - Flexible EU Event Control 0						
	7:4	<p>Coarse Event Filter Select EU event 0</p> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>U4</td></tr> </table> <p>This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 0. Note that the coarse event filter is logically applied before the fine event filter.</p>	Project:	BDW	Format:	U4
Project:	BDW					
Format:	U4					
	3:0	<p>Increment Event for EU event 0</p> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>U4</td></tr> </table> <p>This field controls which increment event provides the basis for flexible EU event 0.</p>	Project:	BDW	Format:	U4
Project:	BDW					
Format:	U4					

Flexible EU Event Control 1

EU_PERF_CNT_CTL1 - Flexible EU Event Control 1						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Access:	R/W					
Size (in bits):	32					
Address:	0E558h					
This register configures flexible EU event 2/3. Please refer to the description of the flexible EU events for more details on supported events. Please note that this register is render context saved/restored.						
DWord	Bit	Description				
0	31:24	<p>Reserved</p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	All	Format:	MBZ
Project:	All					
Format:	MBZ					
23:20	<p>Fine Event Filter Select EU event 3</p> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>U4</td></tr> </table> <p>This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 3. Note that the fine event filter is logically applied after the coarse event filter.</p>	Project:	BDW	Format:	U4	
Project:	BDW					
Format:	U4					
19:16	<p>Coarse Event Filter Select EU event 3</p> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>U4</td></tr> </table> <p>This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 3. Note that the coarse event filter is logically applied before the fine event filter.</p>	Project:	BDW	Format:	U4	
Project:	BDW					
Format:	U4					
15:12	<p>Increment Event for EU event 3</p> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>U4</td></tr> </table> <p>This field controls which increment event provides the basis for flexible EU event 3.</p>	Project:	BDW	Format:	U4	
Project:	BDW					
Format:	U4					
11:8	<p>Fine Event Filter Select EU event 2</p> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>U4</td></tr> </table> <p>This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 2. Note that the fine event filter is logically applied after the coarse event filter.</p>	Project:	BDW	Format:	U4	
Project:	BDW					
Format:	U4					

EU_PERF_CNT_CTL1 - Flexible EU Event Control 1						
	7:4	<p>Coarse Event Filter Select EU event 2</p> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>U4</td></tr> </table> <p>This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 2. Note that the coarse event filter is logically applied before the fine event filter.</p>	Project:	BDW	Format:	U4
Project:	BDW					
Format:	U4					
	3:0	<p>Increment Event for EU event 2</p> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>U4</td></tr> </table> <p>This field controls which increment event provides the basis for flexible EU event 2.</p>	Project:	BDW	Format:	U4
Project:	BDW					
Format:	U4					

Flexible EU Event Control 2

EU_PERF_CNT_CTL2 - Flexible EU Event Control 2						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Access:	R/W					
Size (in bits):	32					
Address:	0E658h					
<p>This register configures flexible EU event 4/5. Please refer to the description of the flexible EU events for more details on supported events. Please note that this register is render context saved/restored.</p>						
DWord	Bit	Description				
0	31:24	Reserved <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	All	Format:	MBZ
Project:	All					
Format:	MBZ					
23:20	Fine Event Filter Select EU event 5 <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>U4</td></tr> </table> <p>This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 5. Note that the fine event filter is logically applied after the coarse event filter.</p>	Project:	BDW	Format:	U4	
Project:	BDW					
Format:	U4					
19:16	Coarse Event Filter Select EU event 5 <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>U4</td></tr> </table> <p>This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 5. Note that the coarse event filter is logically applied before the fine event filter.</p>	Project:	BDW	Format:	U4	
Project:	BDW					
Format:	U4					
15:12	Increment Event for EU event 5 <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>U4</td></tr> </table> <p>This field controls which increment event provides the basis for flexible EU event 5.</p>	Project:	BDW	Format:	U4	
Project:	BDW					
Format:	U4					
11:8	Fine Event Filter Select EU event 4 <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>U4</td></tr> </table> <p>This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 4. Note that the fine event filter is logically applied after the coarse event filter.</p>	Project:	BDW	Format:	U4	
Project:	BDW					
Format:	U4					

EU_PERF_CNT_CTL2 - Flexible EU Event Control 2			
	7:4	Coarse Event Filter Select EU event 4	
		Project:	BDW
		Format:	U4
		This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 4. Note that the coarse event filter is logically applied before the fine event filter.	
	3:0	Increment Event for EU event 4	
		Project:	BDW
		Format:	U4
		This field controls which increment event provides the basis for flexible EU event 4.	

Flexible EU Event Control 3

EU_PERF_CNT_CTL3 - Flexible EU Event Control 3						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Access:	R/W					
Size (in bits):	32					
Address:	0E758h					
This register configures flexible EU event 6/7. Please refer to the description of the flexible EU events for more details on supported events. Please note that this register is render context saved/restored.						
DWord	Bit	Description				
0	31:24	<p>Reserved</p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	All	Format:	MBZ
Project:	All					
Format:	MBZ					
23:20	<p>Fine Event Filter Select EU event 7</p> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>U4</td></tr> </table> <p>This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 7. Note that the fine event filter is logically applied after the coarse event filter.</p>	Project:	BDW	Format:	U4	
Project:	BDW					
Format:	U4					
19:16	<p>Coarse Event Filter Select EU event 7</p> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>U4</td></tr> </table> <p>This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 7. Note that the coarse event filter is logically applied before the fine event filter.</p>	Project:	BDW	Format:	U4	
Project:	BDW					
Format:	U4					
15:12	<p>Increment Event for EU event 7</p> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>U4</td></tr> </table> <p>This field controls which increment event provides the basis for flexible EU event 7.</p>	Project:	BDW	Format:	U4	
Project:	BDW					
Format:	U4					
11:8	<p>Fine Event Filter Select EU event 6</p> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>U4</td></tr> </table> <p>This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 6. Note that the fine event filter is logically applied after the coarse event filter.</p>	Project:	BDW	Format:	U4	
Project:	BDW					
Format:	U4					

EU_PERF_CNT_CTL3 - Flexible EU Event Control 3						
	7:4	<p>Coarse Event Filter Select EU event 6</p> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>U4</td></tr> </table> <p>This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 6. Note that the coarse event filter is logically applied before the fine event filter.</p>	Project:	BDW	Format:	U4
Project:	BDW					
Format:	U4					
	3:0	<p>Increment Event for EU event 6</p> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>U4</td></tr> </table> <p>This field controls which increment event provides the basis for flexible EU event 6.</p>	Project:	BDW	Format:	U4
Project:	BDW					
Format:	U4					

Flexible EU Event Control 4

EU_PERF_CNT_CTL4 - Flexible EU Event Control 4						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Access:	R/W					
Size (in bits):	32					
Address:	0E45Ch					
This register configures flexible EU event 8/9. Please refer to the description of the flexible EU events for more details on supported events. Please note that this register is render context saved/restored.						
DWord	Bit	Description				
0	31:24	<p>Reserved</p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	All	Format:	MBZ
Project:	All					
Format:	MBZ					
23:20	<p>Fine Event Filter Select EU event 9</p> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>U4</td></tr> </table> <p>This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 9. Note that the fine event filter is logically applied after the coarse event filter.</p>	Project:	BDW	Format:	U4	
Project:	BDW					
Format:	U4					
19:16	<p>Coarse Event Filter Select EU event 9</p> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>U4</td></tr> </table> <p>This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 9. Note that the coarse event filter is logically applied before the fine event filter.</p>	Project:	BDW	Format:	U4	
Project:	BDW					
Format:	U4					
15:12	<p>Increment Event for EU event 9</p> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>U4</td></tr> </table> <p>This field controls which increment event provides the basis for flexible EU event 9.</p>	Project:	BDW	Format:	U4	
Project:	BDW					
Format:	U4					
11:8	<p>Fine Event Filter Select EU event 8</p> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>U4</td></tr> </table> <p>This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 8. Note that the fine event filter is logically applied after the coarse event filter.</p>	Project:	BDW	Format:	U4	
Project:	BDW					
Format:	U4					

EU_PERF_CNT_CTL4 - Flexible EU Event Control 4						
	7:4	<p>Coarse Event Filter Select EU event 8</p> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>U4</td></tr> </table> <p>This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 8. Note that the coarse event filter is logically applied before the fine event filter.</p>	Project:	BDW	Format:	U4
Project:	BDW					
Format:	U4					
	3:0	<p>Increment Event for EU event 8</p> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>U4</td></tr> </table> <p>This field controls which increment event provides the basis for flexible EU event 8.</p>	Project:	BDW	Format:	U4
Project:	BDW					
Format:	U4					

Flexible EU Event Control 5

EU_PERF_CNT_CTL5 - Flexible EU Event Control 5						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Access:	R/W					
Size (in bits):	32					
Address:	0E55Ch					
<p>This register configures flexible EU event 10/11. Please refer to the description of the flexible EU events for more details on supported events. Please note that this register is render context saved/restored.</p>						
DWord	Bit	Description				
0	31:24	Reserved <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	All	Format:	MBZ
Project:	All					
Format:	MBZ					
23:20	Fine Event Filter Select EU event 11 <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>U4</td></tr> </table> <p>This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 11. Note that the fine event filter is logically applied after the coarse event filter.</p>	Project:	BDW	Format:	U4	
Project:	BDW					
Format:	U4					
19:16	Coarse Event Filter Select EU event 11 <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>U4</td></tr> </table> <p>This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 11. Note that the coarse event filter is logically applied before the fine event filter.</p>	Project:	BDW	Format:	U4	
Project:	BDW					
Format:	U4					
15:12	Increment Event for EU event 11 <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>U4</td></tr> </table> <p>This field controls which increment event provides the basis for flexible EU event 11.</p>	Project:	BDW	Format:	U4	
Project:	BDW					
Format:	U4					
11:8	Fine Event Filter Select EU event 10 <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>U4</td></tr> </table> <p>This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 10. Note that the fine event filter is logically applied after the coarse event filter.</p>	Project:	BDW	Format:	U4	
Project:	BDW					
Format:	U4					

EU_PERF_CNT_CTL5 - Flexible EU Event Control 5						
	7:4	<p>Coarse Event Filter Select EU event 10</p> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>U4</td></tr> </table> <p>This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 10. Note that the coarse event filter is logically applied before the fine event filter.</p>	Project:	BDW	Format:	U4
Project:	BDW					
Format:	U4					
	3:0	<p>Increment Event for EU event 10</p> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>U4</td></tr> </table> <p>This field controls which increment event provides the basis for flexible EU event 10.</p>	Project:	BDW	Format:	U4
Project:	BDW					
Format:	U4					

Flexible EU Event Control 6

EU_PERF_CNT_CTL6 - Flexible EU Event Control 6						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Access:	R/W					
Size (in bits):	32					
Address:	0E65Ch					
This register configures flexible EU event 12/13. Please refer to the description of the flexible EU events for more details on supported events. Please note that this register is render context saved/restored.						
DWord	Bit	Description				
0	31:24	<p>Reserved</p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	All	Format:	MBZ
Project:	All					
Format:	MBZ					
23:20	<p>Fine Event Filter Select EU event 13</p> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>U4</td></tr> </table> <p>This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 13. Note that the fine event filter is logically applied after the coarse event filter.</p>	Project:	BDW	Format:	U4	
Project:	BDW					
Format:	U4					
19:16	<p>Coarse Event Filter Select EU event 13</p> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>U4</td></tr> </table> <p>This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 13. Note that the coarse event filter is logically applied before the fine event filter.</p>	Project:	BDW	Format:	U4	
Project:	BDW					
Format:	U4					
15:12	<p>Increment Event for EU event 13</p> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>U4</td></tr> </table> <p>This field controls which increment event provides the basis for flexible EU event 13.</p>	Project:	BDW	Format:	U4	
Project:	BDW					
Format:	U4					
11:8	<p>Fine Event Filter Select EU event 12</p> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>U4</td></tr> </table> <p>This field controls which fine event filter is applied to the coarsely filtered increment event when creating flexible EU event 12. Note that the fine event filter is logically applied after the coarse event filter.</p>	Project:	BDW	Format:	U4	
Project:	BDW					
Format:	U4					

EU_PERF_CNT_CTL6 - Flexible EU Event Control 6						
	7:4	<p>Coarse Event Filter Select EU event 12</p> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>U4</td></tr> </table> <p>This field controls which coarse event filter is applied to the selected increment event when creating flexible EU event 12. Note that the coarse event filter is logically applied before the fine event filter.</p>	Project:	BDW	Format:	U4
Project:	BDW					
Format:	U4					
	3:0	<p>Increment Event for EU event 12</p> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>U4</td></tr> </table> <p>This field controls which increment event provides the basis for flexible EU event 12.</p>	Project:	BDW	Format:	U4
Project:	BDW					
Format:	U4					

FORCE_TO_NONPRIV

FORCE_TO_NONPRIV - FORCE_TO_NONPRIV	
Register Space:	MMIO: 0/2/0
Project:	BDW
Default Value:	0x00002094
Access:	R/W
Size (in bits):	32
Address:	024D0h-024D3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_0_RCSUNIT
Address:	024D4h-024D7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_1_RCSUNIT
Address:	024D8h-024DBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_2_RCSUNIT
Address:	024DCh-024DFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_3_RCSUNIT
Address:	024E0h-024E3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_4_RCSUNIT
Address:	024E4h-024E7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_5_RCSUNIT
Address:	024E8h-024EBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_6_RCSUNIT
Address:	024ECh-024EFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_7_RCSUNIT
Address:	024F0h-024F3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_8_RCSUNIT
Address:	024F4h-024F7h
Name:	FORCE_TO_NONPRIV

FORCE_TO_NONPRIV - FORCE_TO_NONPRIV	
ShortName:	FORCE_TO_NONPRIV_9_RCSUNIT
Address:	024F8h-024FBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_10_RCSUNIT
Address:	024FCh-024FFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_11_RCSUNIT
Address:	124D0h-124D3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_0_VCSUNIT0
Address:	124D4h-124D7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_1_VCSUNIT0
Address:	124D8h-124DBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_2_VCSUNIT0
Address:	124DCh-124DFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_3_VCSUNIT0
Address:	124E0h-124E3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_4_VCSUNIT0
Address:	124E4h-124E7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_5_VCSUNIT0
Address:	124E8h-124EBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_6_VCSUNIT0
Address:	124ECh-124EFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_7_VCSUNIT0
Address:	124F0h-124F3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_8_VCSUNIT0
Address:	124F4h-124F7h

FORCE_TO_NONPRIV - FORCE_TO_NONPRIV	
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_9_VCSUNIT0
Address:	124F8h-124FBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_10_VCSUNIT0
Address:	124FCh-124FFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_11_VCSUNIT0
Address:	1A4D0h-1A4D3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_0_VECSUNIT
Address:	1A4D4h-1A4D7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_1_VECSUNIT
Address:	1A4D8h-1A4DBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_2_VECSUNIT
Address:	1A4DCh-1A4DFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_3_VECSUNIT
Address:	1A4E0h-1A4E3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_4_VECSUNIT
Address:	1A4E4h-1A4E7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_5_VECSUNIT
Address:	1A4E8h-1A4EBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_6_VECSUNIT
Address:	1A4ECh-1A4EFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_7_VECSUNIT
Address:	1A4F0h-1A4F3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_8_VECSUNIT

FORCE_TO_NONPRIV - FORCE_TO_NONPRIV	
Address:	1A4F4h-1A4F7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_9_VECSUNIT
Address:	1A4F8h-1A4FBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_10_VECSUNIT
Address:	1A4FCh-1A4FFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_11_VECSUNIT
Address:	1C4D0h-1C4D3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_0_VCSUNIT1
Address:	1C4D4h-1C4D7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_1_VCSUNIT1
Address:	1C4D8h-1C4DBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_2_VCSUNIT1
Address:	1C4DCh-1C4DFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_3_VCSUNIT1
Address:	1C4E0h-1C4E3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_4_VCSUNIT1
Address:	1C4E4h-1C4E7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_5_VCSUNIT1
Address:	1C4E8h-1C4EBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_6_VCSUNIT1
Address:	1C4ECh-1C4EFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_7_VCSUNIT1
Address:	1C4F0h-1C4F3h
Name:	FORCE_TO_NONPRIV

FORCE_TO_NONPRIV - FORCE_TO_NONPRIV	
ShortName:	FORCE_TO_NONPRIV_8_VCSUNIT1
Address:	1C4F4h-1C4F7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_9_VCSUNIT1
Address:	1C4F8h-1C4FBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_10_VCSUNIT1
Address:	1C4FCh-1C4FFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_11_VCSUNIT1
Address:	224D0h-224D3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_0_BCSUNIT
Address:	224D4h-224D7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_1_BCSUNIT
Address:	224D8h-224DBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_2_BCSUNIT
Address:	224DCh-224DFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_3_BCSUNIT
Address:	224E0h-224E3h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_4_BCSUNIT
Address:	224E4h-224E7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_5_BCSUNIT
Address:	224E8h-224EBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_6_BCSUNIT
Address:	224ECh-224EFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_7_BCSUNIT
Address:	224F0h-224F3h

FORCE_TO_NONPRIV - FORCE_TO_NONPRIV

Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_8_BCSUNIT
Address:	224F4h-224F7h
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_9_BCSUNIT
Address:	224F8h-224FBh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_10_BCSUNIT
Address:	224FCh-224FFh
Name:	FORCE_TO_NONPRIV
ShortName:	FORCE_TO_NONPRIV_11_BCSUNIT

These registers are privilege registers and are not allowed to be written from non-privilege batch buffer. These are global registers and power context save/restored.

Programming Notes

RCS_FORCE_TO_NONPRIV registers in render CS must be used to force the below registers to be treated as non-privileged by HW:

- 0xE100
- 0xB110
- 0x7010

DWord	Bit	Description						
0	31	Reserved <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Project:</td><td style="width: 50%;">BDW</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	BDW	Format:	MBZ		
Project:	BDW							
Format:	MBZ							
	30:26	Reserved <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Format:</td><td style="width: 50%;">MBZ</td></tr> </table>	Format:	MBZ				
Format:	MBZ							
	25:2	Non Privilege Register Address <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Format:</td><td style="width: 50%;">MmioAddress[25:2]</td></tr> </table>	Format:	MmioAddress[25:2]				
Format:	MmioAddress[25:2]							
Description								
This field contains the MMIO offset of a register. MMIO offset programmed in this field will be treated as a non-privilege register by render command streamer while processing register writes from a non-privilege batch buffer. This register provides programmability is to extend the non-privilege register table mentioned in MI_BATCH_BUFFER_START command in render command streamer.								
<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 33%;">Value</th><th style="width: 33%;">Name</th><th style="width: 33%;">Project</th></tr> </thead> <tbody> <tr> <td>825h</td><td>[Default]</td><td>BDW</td></tr> </tbody> </table>			Value	Name	Project	825h	[Default]	BDW
Value	Name	Project						
825h	[Default]	BDW						

FORCE_TO_NONPRIV - FORCE_TO_NONPRIV

	1:0	Reserved	Format:	MBZ
--	-----	-----------------	---------	-----

Force Wake Request for Multiple Threads with Mask

FORCE_WAKE - Force Wake Request for Multiple Threads with Mask

Register Space:	MMIO: 0/2/0			
Project:	BDW			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0A188h			
<p>[31:16] :Mask bits applied to [15:0] of same register. If mask is set to 1, corresponding bit in [15:0] is written. If mask is set to 0, corresponding bit in [15:0] is unaffected.</p> <p>Each bit of [15:0] acts as force wake to GT.</p> <p>0 = GT core can be powered down if no other force wake bits are set and all other C6 conditions are met.</p> <p>1 = GT core cannot be powered down.</p> <p>Note - these bits [15:0] need to have a corresponding mask set [31:16] to allow them to be written.</p> <p>The status of bits [15:0] are also sent to 0x130044[15:0] which is an always-on register that can be polled to verify the Force Wake status. Software must guarantee the following sequence when using Force Wake:</p> <ol style="list-style-type: none"> 1. Write 0xA188[n] ='1' with [n+16]='1', where [n] is used only by that particular code thread. 2. Read 0x130044[n] until it is '1'. 3. Perform any work that requires GT to be awake. 4. Write 0xA188[n] ='0' with [n+16]='1'. 5. Read 0x130044[n] until it is '0' sometime before writing 0xA188[n]='1' again. <p>The newly loaded Gfx driver must first initialize this register by clearing all bits (0xFFFF0000). Workaround for MGSRunIt</p>				
DWord	Bit	Description		
0	31:16	<p>Multiple Force Wake Mask</p> <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Mask bits applied to [15:0] of same register. If mask is set to 1, corresponding bit in [15:0] is written. If mask is set to 0, corresponding bit in [15:0] is unaffected.</p>	Access:	R/W
Access:	R/W			
15	<p>Force Wake Request for Thread 15</p> <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Thread 15 - When set with corresponding mask bit 31, GT core can not be powered down.</p>	Access:	R/W	
Access:	R/W			
14	<p>Force Wake Request for Thread 14</p> <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Thread 14 - When set with corresponding mask bit 30, GT core can not be powered down.</p>	Access:	R/W	
Access:	R/W			
13	<p>Force Wake Request for Thread 13</p> <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Thread 13 - When set with corresponding mask bit 29, GT core can not be powered down.</p>	Access:	R/W	
Access:	R/W			

FORCE_WAKE - Force Wake Request for Multiple Threads with Mask

	12	Force Wake Request for Thread 12	Access:	R/W
Thread 12 - When set with corresponding mask bit 28, GT core can not be powered down.				
	11	Force Wake Request for Thread 11	Access:	R/W
Thread 11 - When set with corresponding mask bit 27, GT core can not be powered down.				
	10	Force Wake Request for Thread 10	Access:	R/W
Thread 10 - When set with corresponding mask bit 26, GT core can not be powered down.				
	9	Force Wake Request for Thread 9	Access:	R/W
Thread 9 - When set with corresponding mask bit 25, GT core can not be powered down.				
	8	Force Wake Request for Thread 8	Access:	R/W
Thread 8 - When set with corresponding mask bit 24, GT core can not be powered down.				
	7	Force Wake Request for Thread 7	Access:	R/W
Thread 7 - When set with corresponding mask bit 23, GT core can not be powered down.				
	6	Force Wake Request for Thread 6	Access:	R/W
Thread 6 - When set with corresponding mask bit 22, GT core can not be powered down.				
	5	Force Wake Request for Thread 5	Access:	R/W
Thread 5 - When set with corresponding mask bit 21, GT core can not be powered down.				
	4	Force Wake Request for Thread 4	Access:	R/W
Thread 4 - When set with corresponding mask bit 20, GT core can not be powered down.				
	3	Force Wake Request for Thread 3	Access:	R/W
Thread 3 - When set with corresponding mask bit 19, GT core can not be powered down.				

FORCE_WAKE - Force Wake Request for Multiple Threads with Mask

	2	Force Wake Request for Thread 2
		Access: R/W
		Thread 2 - When set with corresponding mask bit 18, GT core can not be powered down.
	1	Force Wake Request for Thread 1
		Access: R/W
		Thread 1 - When set with corresponding mask bit 17, GT core can not be powered down.
	0	Force Wake Request for Thread 0
		Access: R/W
		Thread 0 - When set with corresponding mask bit 16, GT core can not be powered down.

Frame count and Draw call number

FCDCN - Frame count and Draw call number				
DWord	Bit	Description		
0	31:16	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
Access:	RO			
15:8	<p>Frame Number</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Frame number is the first of two reporting tags that software (i.e. driver) may populate in order to provide reference points during L3 performance reporting modes. Should the "Frame Count and Draw Call Enable" bit (FCDCE) in the "First Buffer Size and Start" register be set, LPFC will selectively replace one of the reporting events with this programmable tag (in addition to the "Draw Call Number" field below). Software may use this to provide reference points for L3 performance counts when parsing the resulting data stream to align reported counts to higher-level operations. The original incarnation called for software to increment this value with each frame, however, the field is generic and may be used for any tagging purpose.</p>	Access:	R/W	
Access:	R/W			
7:0	<p>Draw call number</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>The draw call number is the second programmable reporting tag provided by LPFC. With this second programmable tag, a more granular sampling boundary may be created by software, or it may be used to provide an alternative reference point for tracking L3 performance. The original incarnation called for software to increment this value with every draw call, but the field is generic and may be used for any similar purpose.</p>	Access:	R/W	
Access:	R/W			

FUSE_STRAP

FUSE_STRAP											
Register Space:		MMIO: 0/2/0									
Project:		BDW									
Source:		BSpec									
Default Value:		0x00000000									
Access:		RO									
Size (in bits):		32									
Address:		42014h-42017h									
Name:		Fuses and Straps									
ShortName:		FUSE_STRAP									
Power:		Always on									
Reset:		global									
This register provides readback of fuse and strap settings. These fuses are programmed by a message from PCU to display address 0x51000 MSG_FUSE, also known as Display Fuse State Message (DFSM).											
DWord	Bit	Description									
0	31	Internal Graphics Disable This bit indicates whether internal graphics capability is disabled. When disabled, iMPH hardware will prevent internal graphics from enabling. <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Enable</td><td>Internal Graphics Enabled</td></tr> <tr> <td>1b</td><td>Disable</td><td>Internal Graphics Disabled</td></tr> </tbody> </table>	Value	Name	Description	0b	Enable	Internal Graphics Enabled	1b	Disable	Internal Graphics Disabled
Value	Name	Description									
0b	Enable	Internal Graphics Enabled									
1b	Disable	Internal Graphics Disabled									
30	Internal Display Disable This bit indicates whether the internal display capability is disabled. This bit does not affect display hardware directly. <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Enable</td><td>Internal Display Enabled</td></tr> <tr> <td>1b</td><td>Disable</td><td>Internal Display Disabled</td></tr> </tbody> </table>	Value	Name	Description	0b	Enable	Internal Display Enabled	1b	Disable	Internal Display Disabled	
Value	Name	Description									
0b	Enable	Internal Display Enabled									
1b	Disable	Internal Display Disabled									
29	Reserved										
28	Display PipeC Disable This bit indicates whether the display pipe C capability is disabled. When disabled, display hardware will prevent the pipe C enable register bit from being set to 1b. <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Enable</td><td>Pipe C Capability Enabled</td></tr> <tr> <td>1b</td><td>Disable</td><td>Pipe C Capability Disabled</td></tr> </tbody> </table>	Value	Name	Description	0b	Enable	Pipe C Capability Enabled	1b	Disable	Pipe C Capability Disabled	
Value	Name	Description									
0b	Enable	Pipe C Capability Enabled									
1b	Disable	Pipe C Capability Disabled									
27	Reserved										
26	Display eDP Disable										

FUSE STRAP													
		This bit indicates whether the display embedded DisplayPort eDP DDIA capability is disabled. When disabled, display hardware will prevent the eDP DDIA enable register bit from being set to 1b and mask the eDP DDIA present strap.											
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Enable</td><td>eDP Capability Enabled</td></tr> <tr> <td>1b</td><td>Disable</td><td>eDP Capability Disabled</td></tr> </tbody> </table>	Value	Name	Description	0b	Enable	eDP Capability Enabled	1b	Disable	eDP Capability Disabled		
Value	Name	Description											
0b	Enable	eDP Capability Enabled											
1b	Disable	eDP Capability Disabled											
25		Reserved											
24		<p>Display CDCLK Limit</p> <p>This bit indicates whether the display CD clock frequency is limited to 450 MHz. When DISPLAY_CDCLK_LIMIT = 1, display hardware will ignore the LCPLL_CTL CD Frequency Select and only allow 450 MHz. From spare fuse bit 2.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>No Limit</td><td>CDCLK frequency not limited to 450 MHz</td></tr> <tr> <td>1b</td><td>Limit</td><td>CDCLK frequency limited to 450 MHz</td></tr> </tbody> </table>	Value	Name	Description	0b	No Limit	CDCLK frequency not limited to 450 MHz	1b	Limit	CDCLK frequency limited to 450 MHz		
Value	Name	Description											
0b	No Limit	CDCLK frequency not limited to 450 MHz											
1b	Limit	CDCLK frequency limited to 450 MHz											
23:22		<p>Display Spare</p> <p>Spare fuses for display. From spare fuses bits 1:0.</p>											
21		<p>CPU Internal SSC Enabled</p> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> </table> <p>This bit indicates if the CPU internal SSC modulator is enabled. Fuse name SSC_ssc_misc_config_EnableIntSscMod.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Not enabled</td><td>CPU internal SSC is disabled</td></tr> <tr> <td>1b</td><td>Enabled</td><td>CPU internal SSC is enabled</td></tr> </tbody> </table>	Project:	BDW	Value	Name	Description	0b	Not enabled	CPU internal SSC is disabled	1b	Enabled	CPU internal SSC is enabled
Project:	BDW												
Value	Name	Description											
0b	Not enabled	CPU internal SSC is disabled											
1b	Enabled	CPU internal SSC is enabled											
20		<p>Display WD Disable</p> <p>This bit indicates whether the display WD capability is disabled. When disabled, display hardware will prevent the pipe WD function enable register bit from being set to 1b.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Enable</td><td>WD Capability Enabled</td></tr> <tr> <td>1b</td><td>Disable</td><td>WD Capability Disabled</td></tr> </tbody> </table>	Value	Name	Description	0b	Enable	WD Capability Enabled	1b	Disable	WD Capability Disabled		
Value	Name	Description											
0b	Enable	WD Capability Enabled											
1b	Disable	WD Capability Disabled											
19:7		<p>Reserved</p> <table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ									
Format:	MBZ												
6		<p>Display RSB Enable</p> <p>This bit indicates whether the remote screen blanking feature is enabled in the display engine. When disabled, display hardware will prevent the remote screen blanking from being enabled.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Disable</td><td>RSB Capability Disabled</td></tr> <tr> <td>1b</td><td>Enable</td><td>RSB Capability Enabled</td></tr> </tbody> </table>	Value	Name	Description	0b	Disable	RSB Capability Disabled	1b	Enable	RSB Capability Enabled		
Value	Name	Description											
0b	Disable	RSB Capability Disabled											
1b	Enable	RSB Capability Enabled											
5:2		<p>Reserved</p> <table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ									
Format:	MBZ												

FUSE_STRAP										
0	1	Reserved								
	0	Display Audio Codec Disable This bit indicates whether the display audio codec capability is disabled. When disabled, display hardware will prevent the audio codec enable register bit from being set to 1b. <table border="1"><thead><tr><th>Value</th><th>Name</th><th>Description</th></tr></thead><tbody><tr><td>0b</td><td>Enable</td><td>Audio Codec Capability Enabled</td></tr><tr><td>1b</td><td>Disable</td><td>Audio Codec Capability Disabled</td></tr></tbody></table>	Value	Name	Description	0b	Enable	Audio Codec Capability Enabled	1b	Disable
Value	Name	Description								
0b	Enable	Audio Codec Capability Enabled								
1b	Disable	Audio Codec Capability Disabled								

FUSE_STRAP2

FUSE_STRAP2		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Address:	4201Ch-4201Fh	
Name:	Fuses and Straps 2	
ShortName:	FUSE_STRAP2	
Power:	Always on	
Reset:	global	
This register provides readback of fuse and strap settings. These fuses are programmed by a message from PCU to display address 0x51008 MSG_FUSE2, also known as Display Fuse State Message 2 (DFSM2).		
DWord	Bit	Description
0	31:29	Reserved
		Format: MBZ
	28:24	SSA_IWAPWMOD DISPLAY_SSA_IWAPWMOD[4:0] - Write Vccmin
	23:21	SSA_IWABIAS DISPLAY_SSA_IWABIAS[2:0] - Write Vccmin
	20	SSA_IWABIASENB DISPLAY_SSA_IWABIASENB - Write assist (active low)
	19	SSA_INBLEN DISPLAY_SSA_INBLEN - Write Vccmin
	18:15	SSA_INBLCAPMOD DISPLAY_SSA_INBLCAPMOD[3:0] - Write Vccmin
	14	SSA_INBLMODESEL DISPLAY_SSA_INBLMODESEL - Write Vccmin
	13:12	SSA_INBLPWMOD DISPLAY_SSA_INBLPWMOD[1:0] - Write Vccmin
	11:8	SSA_IRABIAS DISPLAY_SSA_IRABIAS[3:0] - Read Vccmin
	7:4	SSA_ISLPBIAS DISPLAY_SSA_ISLPBIAS[3:0] - Data retention
	3	SSA_ISLPEN DISPLAY_SSA_ISLPEN - Disable sleep
	2	SSA_IBITCELLSLP DISPLAY_SSA_IBITCELLSLP - Disable bitcell sleep

FUSE_STRAP2		
	1	SSA IWLSLP DISPLAY_SSA_IWLSLP - Disable wordline sleep
	0	SSA IBLSLP DISPLAY_SSA_IBLSLP - Disable bitline float sleep

FUSE_STRAP3

FUSE_STRAP3											
DWord	Bit	Description									
0	31:5	Reserved									
	4	ULT Mode This fuse is currently unused and should be ignored by software. <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td></td> </tr> <tr> <td>1b</td> <td></td> </tr> </tbody> </table>	Value	Name	0b		1b				
Value	Name										
0b											
1b											
	3	Reserved									
	2	LCPLL Unavail This bit specifies the availability of the LCPLL. <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Available</td> <td>LCPLL available</td> </tr> <tr> <td>1b</td> <td>Not available</td> <td>LCPLL not available</td> </tr> </tbody> </table>	Value	Name	Description	0b	Available	LCPLL available	1b	Not available	LCPLL not available
Value	Name	Description									
0b	Available	LCPLL available									
1b	Not available	LCPLL not available									
	1	Reference Clock Select This field indicates the Non-SSC reference clock frequency, which also indicates whether the CPU and PCH are in a single package or separate packages. <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>135 MHz</td> <td>Non-SSC reference is 135 MHz. CPU and PCH in separate packages.</td> </tr> <tr> <td>1b</td> <td>24 MHz</td> <td>Non-SSC reference is 24 MHz. CPU and PCH combined in a single package.</td> </tr> </tbody> </table>	Value	Name	Description	0b	135 MHz	Non-SSC reference is 135 MHz. CPU and PCH in separate packages.	1b	24 MHz	Non-SSC reference is 24 MHz. CPU and PCH combined in a single package.
Value	Name	Description									
0b	135 MHz	Non-SSC reference is 135 MHz. CPU and PCH in separate packages.									
1b	24 MHz	Non-SSC reference is 24 MHz. CPU and PCH combined in a single package.									
	0	DisplayPort A Present This bit specifies whether the port was present during initialization. The strap state can also be read in the DDI_BUF_CTL_A 0x64000 register bit 0. <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Not Present</td> <td>Port not present</td> </tr> <tr> <td>1b</td> <td>Present</td> <td>Port present</td> </tr> </tbody> </table>	Value	Name	Description	0b	Not Present	Port not present	1b	Present	Port present
Value	Name	Description									
0b	Not Present	Port not present									
1b	Present	Port present									

FUSE_STRAP4

FUSE_STRAP4		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Address:	42024h-42027h	
Name:	Fuses and Straps 4	
ShortName:	FUSE_STRAP4	
Power:	Always on	
Reset:	global	
This register provides readback of fuse and strap settings. These fuses are programmed by a message from PCU to display address 0x5100C MSG_FUSE3, also known as Display Fuse State Message 3 (DFSM3).		
DWord	Bit	Description
0	31:21	Reserved
		Format: MBZ
	20:11	DPF REDUNDANCY DISPLAY_DPF_REDUNDANCY[9:0] - column redundancy
	10:4	RF C DISPLAY_RF_C[6:0] - Write Vccmin
	3:0	RF IK DISPLAY_RF_IK[3:0] - Read Vccmin

FUSE_STRAP5

FUSE_STRAP5		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Address:	42028h-4202Bh	
Name:	Fuses and Straps 5	
ShortName:	FUSE_STRAP5	
Power:	Always on	
Reset:	global	
This register provides readback of fuse and strap settings. These fuses are programmed by a message from PCU to display address 0x51010 MSG_FUSE4, also known as Display Fuse State Message 4 (DFSM4).		
DWord	Bit	Description
0	31:30	Reserved Format: MBZ
	29:20	DDB3 REDUNDANCY DISPLAY_DDB3_REDUNDANCY[9:0] - 1 valid, 9 row index
	19:10	DDB2 REDUNDANCY DISPLAY_DDB2_REDUNDANCY[9:0] - 1 valid, 9 row index
	9:0	DDB1 REDUNDANCY DISPLAY_DDB1_REDUNDANCY[9:0] - 1 valid, 9 row index

FUSE_STRAP6

FUSE_STRAP6				
Register Space:	MMIO: 0/2/0			
Project:	BDW			
Default Value:	0x00000000			
Access:	RO			
Size (in bits):	32			
Address:	4202Ch-4202Fh			
Name:	Fuses and Straps 6			
ShortName:	FUSE_STRAP6			
Power:	Always on			
Reset:	global			
This register provides readback of fuse and strap settings. These fuses are programmed by a message from PCU to display address 0x51014 MSG_FUSE5, also known as Display Fuse State Message 5 (DFSM5).				
DWord	Bit	Description		
0	31:21	Reserved <table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ
Format:	MBZ			
20:0	IPS REDUNDANCY DISPLAY_IPS_REDUNDANCY[20:0] - column redundancy			

GAB Arbitration Programmable

GAB_AP - GAB ArbitrationProgrammable		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	040F0h	
DWord	Bit	Description
0	31:0	Reserved

GAB LRA 0

GAB_LRA_0 - GAB LRA 0						
DWord	Bit	Description				
0	31:29	Reserved <table border="1"> <tr> <td>Default Value:</td><td>000b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	000b	Access:	RO
Default Value:	000b					
Access:	RO					
28:24	GAB LRA1 Max <table border="1"> <tr> <td>Default Value:</td><td>11111b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Maximum value of programmable LRA1.</p>	Default Value:	11111b	Access:	R/W	
Default Value:	11111b					
Access:	R/W					
23:21	Reserved <table border="1"> <tr> <td>Default Value:</td><td>000b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	000b	Access:	RO	
Default Value:	000b					
Access:	RO					
20:16	GAB LRA1 Min <table border="1"> <tr> <td>Default Value:</td><td>10000b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Minimum value of programmable LRA1.</p>	Default Value:	10000b	Access:	R/W	
Default Value:	10000b					
Access:	R/W					
15:13	Reserved <table border="1"> <tr> <td>Default Value:</td><td>000b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	000b	Access:	RO	
Default Value:	000b					
Access:	RO					
12:8	GABLRA0 Max <table border="1"> <tr> <td>Default Value:</td><td>01111b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Maximum value of programmable LRA0.</p>	Default Value:	01111b	Access:	R/W	
Default Value:	01111b					
Access:	R/W					
7:5	Reserved <table border="1"> <tr> <td>Default Value:</td><td>000b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	000b	Access:	RO	
Default Value:	000b					
Access:	RO					
4:0	GABLRA0 Min <table border="1"> <tr> <td>Default Value:</td><td>00000b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Minimum value of programmable LRA0.</p>	Default Value:	00000b	Access:	R/W	
Default Value:	00000b					
Access:	R/W					

GAB LRA 1

GAB_LRA_1 - GAB LRA 1						
DWord	Bit	Description				
0	31:4	<p>Reserved</p> <table border="1"> <tr> <td>Default Value:</td><td>0000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	0000000h	Access:	RO
Default Value:	0000000h					
Access:	RO					
3:2	<p>BLB</p> <table border="1"> <tr> <td>Default Value:</td><td>00b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Which LRA should BLB use.</p>	Default Value:	00b	Access:	R/W	
Default Value:	00b					
Access:	R/W					
1:0	<p>BCS</p> <table border="1"> <tr> <td>Default Value:</td><td>01b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Which LRA should BCS use.</p>	Default Value:	01b	Access:	R/W	
Default Value:	01b					
Access:	R/W					

GAB unit Control Register

GAB_CTL_REG - GAB unit Control Register												
DWord	Bit	Description										
0	31:9	Reserved										
	8	Continue after Page Fault	<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>GAB Set</td> <td>Ipon receiving a page fault when requesting an address translation, GAB will set address bit 39 to 1 and continue.</td> </tr> <tr> <td>0</td> <td>GAB Hang</td> <td>GAB will hang on a page fault. Default = b0.</td> </tr> </tbody> </table>	Value	Name	Description	1	GAB Set	Ipon receiving a page fault when requesting an address translation, GAB will set address bit 39 to 1 and continue.	0	GAB Hang	GAB will hang on a page fault. Default = b0.
Value	Name	Description										
1	GAB Set	Ipon receiving a page fault when requesting an address translation, GAB will set address bit 39 to 1 and continue.										
0	GAB Hang	GAB will hang on a page fault. Default = b0.										
	7:6	PPGTT BCS TLB LRA MIN	<table border="1"> <tr> <td>Default Value:</td> <td>10b</td> </tr> <tr> <td colspan="2">TLB Depth Partitioning Register In PP GTT Mode.</td></tr> </table>	Default Value:	10b	TLB Depth Partitioning Register In PP GTT Mode.						
Default Value:	10b											
TLB Depth Partitioning Register In PP GTT Mode.												
	5:4	GAB write request priority signal value used in GAC arbitration	<table border="1"> <tr> <td>Default Value:</td> <td>11b</td> </tr> </table>	Default Value:	11b							
Default Value:	11b											
	3:2	GAB read only request priority signal value used in GAC arbitration	<table border="1"> <tr> <td>Default Value:</td> <td>11b</td> </tr> </table>	Default Value:	11b							
Default Value:	11b											
	1:0	GAB read request priority signal value used in GAC arbitration	<table border="1"> <tr> <td>Default Value:</td> <td>11b</td> </tr> </table>	Default Value:	11b							
Default Value:	11b											

GAC_GAM Arbitration Counters Register 0

ARB_GAC_GAM_REQCNTS0 - GAC_GAM Arbitration Counters Register 0		
Register Space:		MMIO: 0/2/0
Project:		BDW
Source:		RenderCS
Default Value:		0x00000000
Access:		R/W
Size (in bits):		32
Trusted Type:		1
Address:		043A8h
DWord	Bit	Description
0	31:22	Reserved
	21:16	Number of GAC WR requests to be accumulated before applying the arbitration
	15:14	Reserved
	13:8	Number of GAC R requests to be accumulated before applying the arbitration
	7:6	Reserved
	5:0	Number of GAC RO requests to be accumulated before applying the arbitration

GAC_GAM Arbitration Counters Register 1

ARB_GAC_GAM_REQCNTS1 - GAC_GAM Arbitration Counters Register 1		
Register Space:		MMIO: 0/2/0
Project:		BDW
Source:		RenderCS
Default Value:		0x00000000
Access:		R/W
Size (in bits):		32
Trusted Type:		1
Address:		043ACh
DWord	Bit	Description
0	31:22	Reserved
	21:16	Number of GAC WR requests to be accumulated before applying the arbitration
	15:14	Reserved
	13:8	Number of GAC R requests to be accumulated before applying the arbitration
	7:6	Reserved
	5:0	Number of GAC RO requests to be accumulated before applying the arbitration

GAC_GAM R Arbitration Register 0

ARB_R_GAC_GAM0 - GAC_GAM R Arbitration Register 0		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	043E0h	
DWord	Bit	Description
0	31:28	Reserved
	27	Priority for entry 1
	26:24	Goto field for entry 1 when request vector is 11b
	23:21	Goto field for entry 1 when request vector is 10b
	20:18	Goto field for entry 1 when request vector is 01b
	17:15	Goto field for entry 1 when request vector is 00b
	14:13	Reserved
	12	Priority for entry 0
	11:9	Goto field for entry 0 when request vector is 11b
	8:6	Goto field for entry 0 when request vector is 10b
	5:3	Goto field for entry 0 when request vector is 01b
	2:0	Goto field for entry 0 when request vector is 00b

GAC_GAM R Arbitration Register 1

ARB_R_GAC_GAM1 - GAC_GAM R Arbitration Register 1		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	043E4h	
DWord	Bit	Description
0	31:28	Reserved
	27	Priority for entry 3
	26:24	Goto field for entry 3 when request vector is 11b
	23:21	Goto field for entry 3 when request vector is 10b
	20:18	Goto field for entry 3 when request vector is 01b
	17:15	Goto field for entry 3 when request vector is 00b
	14:13	Reserved
	12	Priority for entry 2
	11:9	Goto field for entry 2 when request vector is 11b
	8:6	Goto field for entry 2 when request vector is 10b
	5:3	Goto field for entry 2 when request vector is 01b
	2:0	Goto field for entry 2 when request vector is 00b

GAC_GAM R Arbitration Register 2

ARB_R_GAC_GAM2 - GAC_GAM R Arbitration Register 2		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	043E8h	
DWord	Bit	Description
0	31:28	Reserved
	27	Priority for entry 5
	26:24	Goto field for entry 5 when request vector is 11b
	23:21	Goto field for entry 5 when request vector is 10b
	20:18	Goto field for entry 5 when request vector is 01b
	17:15	Goto field for entry 5 when request vector is 00b
	14:13	Reserved
	12	Priority for entry 4
	11:9	Goto field for entry 4 when request vector is 11b
	8:6	Goto field for entry 4 when request vector is 10b
	5:3	Goto field for entry 4 when request vector is 01b
	2:0	Goto field for entry 4 when request vector is 00b

GAC_GAM R Arbitration Register 3

ARB_R_GAC_GAM3 - GAC_GAM R Arbitration Register 3		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	043ECh	
DWord	Bit	Description
0	31:28	Reserved
	27	Priority for entry 7
	26:24	Goto field for entry 7 when request vector is 11b
	23:21	Goto field for entry 7 when request vector is 10b
	20:18	Goto field for entry 7 when request vector is 01b
	17:15	Goto field for entry 7 when request vector is 00b
	14:13	Reserved
	12	Priority for entry 6
	11:9	Goto field for entry 6 when request vector is 11b
	8:6	Goto field for entry 6 when request vector is 10b
	5:3	Goto field for entry 6 when request vector is 01b
	2:0	Goto field for entry 6 when request vector is 00b

GAC_GAM RO Arbitration Register 0

ARB_RO_GAC_GAM0 - GAC_GAM RO Arbitration Register 0		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	043D0h	
DWord	Bit	Description
0	31:28	Reserved
	27	Priority for entry 1
	26:24	Goto field for entry 1 when request vector is 11b
	23:21	Goto field for entry 1 when request vector is 10b
	20:18	Goto field for entry 1 when request vector is 01b
	17:15	Goto field for entry 1 when request vector is 00b
	14:13	Reserved
	12	Priority for entry 01
	11:9	Goto field for entry 01 when request vector is 11b
	8:6	Goto field for entry 01 when request vector is 10b
	5:3	Goto field for entry 01 when request vector is 01b
	2:0	Goto field for entry 01 when request vector is 00b

GAC_GAM RO Arbitration Register 1

ARB_RO_GAC_GAM1 - GAC_GAM RO Arbitration Register 1		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	043D4h	
DWord	Bit	Description
0	31:28	Reserved
	27	Priority for entry 3
	26:24	Goto field for entry 3 when request vector is 11b
	23:21	Goto field for entry 3 when request vector is 10b
	20:18	Goto field for entry 3 when request vector is 01b
	17:15	Goto field for entry 3 when request vector is 00b
	14:13	Reserved
	12	Priority for entry 2
	11:9	Goto field for entry 2 when request vector is 11b
	8:6	Goto field for entry 2 when request vector is 10b
	5:3	Goto field for entry 2 when request vector is 01b
	2:0	Goto field for entry 2 when request vector is 00b

GAC_GAM RO Arbitration Register 2

ARB_RO_GAC_GAM2 - GAC_GAM RO Arbitration Register 2		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	043D8h	
DWord	Bit	Description
0	31:28	Reserved
	27	Priority for entry 5
	26:24	Goto field for entry 5 when request vector is 11b
	23:21	Goto field for entry 5 when request vector is 10b
	20:18	Goto field for entry 5 when request vector is 01b
	17:15	Goto field for entry 5 when request vector is 00b
	14:13	Reserved
	12	Priority for entry 4
	11:9	Goto field for entry 4 when request vector is 11b
	8:6	Goto field for entry 4 when request vector is 10b
	5:3	Goto field for entry 4 when request vector is 01b
	2:0	Goto field for entry 4 when request vector is 00b

GAC_GAM RO Arbitration Register 3

ARB_RO_GAC_GAM3 - GAC_GAM RO Arbitration Register 3		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	043DCh	
DWord	Bit	Description
0	31:28	Reserved
	27	Priority for entry 7
	26:24	Goto field for entry 7 when request vector is 11b
	23:21	Goto field for entry 7 when request vector is 10b
	20:18	Goto field for entry 7 when request vector is 01b
	17:15	Goto field for entry 7 when request vector is 00b
	14:13	Reserved
	12	Priority for entry 6
	11:9	Goto field for entry 6 when request vector is 11b
	8:6	Goto field for entry 6 when request vector is 10b
	5:3	Goto field for entry 6 when request vector is 01b
	2:0	Goto field for entry 6 when request vector is 00b

GAC_GAM WR Arbitration Register 0

ARB_WR_GAC_GAM0 - GAC_GAM WR Arbitration Register 0		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	043F0h	
DWord	Bit	Description
0	31:28	Reserved
	27	Priority for entry 1
	26:24	Goto field for entry 1 when request vector is 11b
	23:21	Goto field for entry 1 when request vector is 10b
	20:18	Goto field for entry 1 when request vector is 01b
	17:15	Goto field for entry 1 when request vector is 00b
	14:13	Reserved
	12	Priority for entry 0
	11:9	Goto field for entry 0 when request vector is 11b
	8:6	Goto field for entry 0 when request vector is 10b
	5:3	Goto field for entry 0 when request vector is 01b
	2:0	Goto field for entry 0 when request vector is 00b

GAC_GAM WR Arbitration Register 1

ARB_WR_GAC_GAM1 - GAC_GAM WR Arbitration Register 1		
Register Space: MMIO: 0/2/0		
Project: BDW		
Source: RenderCS		
Default Value: 0x00000000		
Access: R/W		
Size (in bits): 32		
Trusted Type: 1		
Address: 043F4h		
DWord	Bit	Description
0	31:28	Reserved
	27	Priority for entry 3
	26:24	Goto field for entry 3 when request vector is 11b
	23:21	Goto field for entry 3 when request vector is 10b
	20:18	Goto field for entry 3 when request vector is 01b
	17:15	Goto field for entry 3 when request vector is 00b
	14:13	Reserved
	12	Priority for entry 2
	11:9	Goto field for entry 2 when request vector is 11b
	8:6	Goto field for entry 2 when request vector is 10b
	5:3	Goto field for entry 2 when request vector is 01b
	2:0	Goto field for entry 2 when request vector is 00b

GAC_GAM WR Arbitration Register 2

ARB_WR_GAC_GAM2 - GAC_GAM WR Arbitration Register 2		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	043F8h	
DWord	Bit	Description
0	31:28	Reserved
	27	Priority for entry 5
	26:24	Goto field for entry 5 when request vector is 11b
	23:21	Goto field for entry 5 when request vector is 10b
	20:18	Goto field for entry 5 when request vector is 01b
	17:15	Goto field for entry 5 when request vector is 00b
	14:13	Reserved
	12	Priority for entry 4
	11:9	Goto field for entry 4 when request vector is 11b
	8:6	Goto field for entry 4 when request vector is 10b
	5:3	Goto field for entry 4 when request vector is 01b
	2:0	Goto field for entry 4 when request vector is 00b

GAC_GAM WR Arbitration Register 3

ARB_WR_GAC_GAM3 - GAC_GAM WR Arbitration Register 3		
Register Space: MMIO: 0/2/0		
Project: BDW		
Source: RenderCS		
Default Value: 0x00000000		
Access: R/W		
Size (in bits): 32		
Trusted Type: 1		
Address: 043FCh		
DWord	Bit	Description
0	31:28	Reserved
	27	Priority for entry 7
	26:24	Goto field for entry 7 when request vector is 11b
	23:21	Goto field for entry 7 when request vector is 10b
	20:18	Goto field for entry 7 when request vector is 01b
	17:15	Goto field for entry 7 when request vector is 00b
	14:13	Reserved
	12	Priority for entry 6
	11:9	Goto field for entry 6 when request vector is 11b
	8:6	Goto field for entry 6 when request vector is 10b
	5:3	Goto field for entry 6 when request vector is 01b
	2:0	Goto field for entry 6 when request vector is 00b

GAM and SA Communication Register

GAMSACOMREG - GAM and SA Communication Register

Register Space:	MMIO: 0/2/0		
Project:	BDW		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	042A0h		
DWord	Bit	Description	
0	31:16	Mask Bits	
		Default Value:	0000h
		Access:	RO
	Mask Bits act as Write Enables for the bits[15:0] of this register.		
	15	GAM and SA Communication Register 15	
		Default Value:	0b
		Access:	R/W
For Future Use. This bit is self clear.			
14	GAM and SA Communication Register 14		
	Default Value:	0b	
	Access:	R/W	
For Future Use. This bit is self clear.			
13	GAM and SA Communication Register 13		
	Default Value:	0b	
	Access:	R/W	
For Future Use. This bit is self clear.			
12	GAM and SA Communication Register 12		
	Default Value:	0b	
	Access:	R/W	
For Future Use. This bit is self clear.			
11	GAM and SA Communication Register 11		
	Default Value:	0b	
	Access:	R/W	
For Future Use. This bit is self clear.			

GAMSACOMREG - GAM and SA Communication Register

	10	GAM and SA Communication Register 10				
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>For Future Use. This bit is self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
	9	GAM and SA Communication Register 9				
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>For Future Use. This bit is self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
	8	GAM and SA Communication Register 8				
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>For Future Use. This bit is self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
	7	GAM and SA Communication Register 7				
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>For Future Use. This bit is self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
	6	GAM and SA Communication Register 6				
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>For Future Use. This bit is self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
	5	GAM and SA Communication Register 5				
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>For Future Use. This bit is self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
	4	GAM and SA Communication Register 4				
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>For Future Use. This bit is self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
	3	GAM and SA Communication Register 3				
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>For Future Use. This bit is self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					

GAMSACOMREG - GAM and SA Communication Register

	2	GAM and SA Communication Register 2				
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Bit2 - Root Table Address Update Request. This bit is self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
	1	GAM and SA Communication Register 1				
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Bit1 - Queued Descriptor Request. This bit is self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
	0	GAM and SA Communication Register 0				
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Bit0 - Context Cache Invalidator Request. This bit is self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					

Gam Fub Done1 Lookup Register

DONE1_REG - Gam Fub Done1 Lookup Register								
DWord	Bit	Description						
0	31:0	Gam Fub Done1 Lookup Reg <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Default Value:</td><td style="padding: 2px;">00000000h</td></tr> <tr> <td style="padding: 2px;">Access:</td><td style="padding: 2px;">RO</td></tr> <tr> <td colspan="2" style="text-align: left; padding: 2px;">GAM Done1 signals.</td></tr> </table>	Default Value:	00000000h	Access:	RO	GAM Done1 signals.	
Default Value:	00000000h							
Access:	RO							
GAM Done1 signals.								

Gam Fub Done Lookup Register

DONE_REG - Gam Fub Done Lookup Register										
DWord	Bit	Description								
0	31:0	<p>Gam Fub Done Lookup Reg</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>31 CVS Credit Fifo is empty. 30 CVS TLB does not have any cycles. 29 Z Credit fifo is empty. 28 ZTLB does not have any cycles. 27 RCC Credit Fifo is empty. 26 RCC TLB does not have any cycles. 25 L3 Credit fifo is empty. 24 L3 TLB does not have any cycles. 23 VLF Credit fifo is empty. 22 VLF TLB does not have any cycles. 21 CASC Credit fifo empty. 20 CASC TLB does not have any cycles. 19 Miss Fub Done. 18 Read Stream Done. 17 Read Steam Fifo is empty. 16 Recycle Fifo in rstrm is empty. 15 TLB Pend Done. 14 TLB Pend PQ Array is done. 13 TLB pend PB Array is done. 12 Read route fub is done. 11 Gafm Data fifo is empty. 10 GAP data fifo is empty. 9 GAC data fifo is empty. 8 Wrdf is done with all the cycles. 7 Wrdf RID fifo is empty. 6 No hold from midarb to RTSTRM. 5 No hold from TLBPEND to MIDARB.</p> <table border="1"> <tr> <td>3 Tied to "1" - to be defined.</td></tr> <tr> <td>2 Fence FSM are IDLE.</td></tr> <tr> <td>1 Non PD Load Done.</td></tr> <tr> <td>0 Tied to "1" - to be defined.</td></tr> </table>	Default Value:	00000000h	Access:	RO	3 Tied to "1" - to be defined.	2 Fence FSM are IDLE.	1 Non PD Load Done.	0 Tied to "1" - to be defined.
Default Value:	00000000h									
Access:	RO									
3 Tied to "1" - to be defined.										
2 Fence FSM are IDLE.										
1 Non PD Load Done.										
0 Tied to "1" - to be defined.										

GAMMA_MODE

GAMMA_MODE		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Access:	Double Buffered	
Size (in bits):	32	
Double Buffer Update Point:	Start of vertical blank	
Address:	4A480h-4A483h	
Name:	Pipe A Gamma Mode	
ShortName:	GAMMA_MODE_A	
Valid Projects:	BDW	
Power:	Always on	
Reset:	soft	
Address:	4AC80h-4AC83h	
Name:	Pipe B Gamma Mode	
ShortName:	GAMMA_MODE_B	
Valid Projects:	BDW	
Power:	off/on	
Reset:	soft	
Address:	4B480h-4B483h	
Name:	Pipe C Gamma Mode	
ShortName:	GAMMA_MODE_C	
Valid Projects:	BDW	
Power:	off/on	
Reset:	soft	
DWord	Bit	Description
0	31:16	Reserved
	15	Reserved
		Project:
14:2	Reserved	

GAMMA_MODE																		
	1:0	Gamma Mode This field selects which mode the pipe palette/gamma correction logic works in. Other gamma units, such as in the planes, are unaffected by this bit.	<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>00b</td><td>8 bit</td><td>8-bit Legacy Palette Mode</td></tr> <tr> <td>01b</td><td>10 bit</td><td>10-bit Precision Palette Mode</td></tr> <tr> <td>10b</td><td>12 bit</td><td>12-bit Interpolated Gamma Mode</td></tr> <tr> <td>11b</td><td>Split</td><td>Split Gamma Mode (separate pipe gamma functions before and after pipe CSC)</td></tr> </tbody> </table>	Value	Name	Description	00b	8 bit	8-bit Legacy Palette Mode	01b	10 bit	10-bit Precision Palette Mode	10b	12 bit	12-bit Interpolated Gamma Mode	11b	Split	Split Gamma Mode (separate pipe gamma functions before and after pipe CSC)
Value	Name	Description																
00b	8 bit	8-bit Legacy Palette Mode																
01b	10 bit	10-bit Precision Palette Mode																
10b	12 bit	12-bit Interpolated Gamma Mode																
11b	Split	Split Gamma Mode (separate pipe gamma functions before and after pipe CSC)																

GAM Put Delay

GAM_PUT_DLY - GAM Put Delay		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0401Ch	
Number of clocks to wait between puts		
DWord	Bit	Description
0	31:0	GAM PUT DELAY
		Default Value: 0000000h
		Access: R/W

GAMT_DONE Register

GAMT_DONE - GAMT_DONE Register						
DWord	Bit	Description				
0	31:0	<p>GAMT_DONE Register</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p> 31: vebxtlb_all_done_f 30: cvstlb_all_done_f 29: ztlb_all_done_f 28: l3tlb_all_done_f 27: rcctlb_all_done_f 26: mfxtlb_all_done_f 25: vlftlb_all_done_f 24: bwgtlb_all_done_f 23: gamwrrb_all_done_f 22: mfxsl1tlb_all_done_f 21: vlfsl1tlb_all_done_f 20: bwgtlb_fifo_empty 19: l3tlb_fifo_empty 18: ztlb_fifo_empty 17: rcctlb_fifo_empty 16: cvstlb_fifo_empty 15: vebxtlb_fifo_empty 14: mfxtlb_fifo_empty 13: mfxsl1tlb_fifo_empty 12: vlfsl1tlb_fifo_empty 11: vlftlb_fifo_empty 10: wrdp_gafm_fifo_empty 9: wrdp_gap_fifo_empty 8: wrdp_gacfg_fifo_empty 7: wrdp_cs_fifo_empty 6: wrdp_vecs_fifo_empty 5: wrdp_oacs_fifo_empty 4: wrdp_gacv_fifo_empty 3: Tied to 1 2: Tied to 1 1: Tied to 1 0: Tied to 1 </p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

GAMT_ECO_REG_RO_IA

GAMT_ECO_REG_RO_IA - GAMT_ECO_REG_RO_IA						
Register Space: MMIO: 0/2/0						
Project: BDW						
Default Value: 0x00000000						
Size (in bits): 32						
Address: 04AB4h						
DWord	Bit	Description				
0	31:0	GAMTECO_REG_RO_IA <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Default Value:</td><td style="padding: 2px;">0000000h</td></tr> <tr> <td style="padding: 2px;">Access:</td><td style="padding: 2px;">RO</td></tr> </table> <p>This register is for ECO usage. RO register with IA Access Type on DEV reset.</p>	Default Value:	0000000h	Access:	RO
Default Value:	0000000h					
Access:	RO					

GAMT_ECO_REG_RW_IA

GAMT_ECO_REG_RW_IA - GAMT_ECO_REG_RW_IA						
Register Space: MMIO: 0/2/0						
Project: BDW						
Default Value: 0x0000AB1B						
Size (in bits): 32						
Address: 04AB0h						
Programmable Request Count - VEBX and BLT						
DWord	Bit	Description				
0	31:0	<p>GAMTECO_REG_RW_IA</p> <table border="1"> <tr> <td>Default Value:</td><td>0000AB1Bh</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Bit[31:16] = Reserved. Bit[15:8] = Number of max outstanding cycles (Misses and Hits not present) that can be allowed to potentially fault = 171. Bit[7:6] = Reserved. Bit[5:0] = Number of max outstanding misses that can be allowed to potentially fault = 27.</p>	Default Value:	0000AB1Bh	Access:	R/W
Default Value:	0000AB1Bh					
Access:	R/W					

GAMT Arbiter Mode Control

GAMTARBMODE - GAMT Arbiter Mode Control								
DWord	Bit	Description						
0	31:16	Mask Bits <table border="1"> <tr> <td>Default Value:</td> <td>0000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Default Value:	0000h	Access:	RO		
Default Value:	0000h							
Access:	RO							
	15	GAMT Arbiter Mode Control 15 <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>For Future Use</p>	Default Value:	0b	Access:	R/W		
Default Value:	0b							
Access:	R/W							
	14	GAMT Arbiter Mode Control 14 <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>0 - Cache the TLB even if there is a FAULT in GAMW read return. 1 - Don't Cache the TLB if there is a fault in GAMW return.</p>	Default Value:	0b	Project:	BDW	Access:	R/W
Default Value:	0b							
Project:	BDW							
Access:	R/W							
	13	GAMT Arbiter Mode Control 13 <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>0 - VEBXTLB clock gate enabled. 1 - VEBXTLB clock gate disabled.</p>	Default Value:	0b	Access:	R/W		
Default Value:	0b							
Access:	R/W							
	12	GAMT Arbiter Mode Control 12 <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>0 - MFXSL1TLB clock gate enabled. 1 - MFXSL1TLB clock gate disabled.</p>	Default Value:	0b	Access:	R/W		
Default Value:	0b							
Access:	R/W							
	11	GAMT Arbiter Mode Control 11 <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>0 - VLFSL1TLB clock gate enabled. 1 - VLFSL1TLB clock gate disabled.</p>	Default Value:	0b	Access:	R/W		
Default Value:	0b							
Access:	R/W							

GAMTARBMODE - GAMT Arbiter Mode Control

	10	GAMT Arbiter Mode Control 10		
		Default Value:	0b	
		Access:	R/W	
		0 - gamwrrb clock gate enabled. 1 - gamwrrb clock gate disabled.		
	9	GAMT Arbiter Mode Control 9		
		Default Value:	0b	
		Access:	R/W	
		Description		Project
		0 - BWGTLB clock gate enabled. 1 - BWGTLB clock gate disabled.		
	8	GAMT Arbiter Mode Control 8		
		Default Value:	0b	
		Access:	R/W	
		0 - VLFTLB clock gate enabled. 1 - VLFTLB clock gate disabled.		
	7	GAMT Arbiter Mode Control 7		
		Default Value:	0b	
		Access:	R/W	
		0 - MFXTLB clock gate enabled. 1 - MFXTLB clock gate disabled.		
	6	GAMT Arbiter Mode Control 6		
		Default Value:	0b	
		Access:	R/W	
		0 - RCCTLB clock gate enabled. 1 - RCCTLB clock gate disabled.		
	5	GAMT Arbiter Mode Control 5		
		Default Value:	0b	
		Access:	R/W	
		0 - L3TLB clock gate enabled. 1 - L3TLB clock gate disabled.		
		For DevBDW(all steppings) bit[5] needs to be set as a work-around due to recent gacb bug. To update bit 5, a value of 0x00200020 needs to be written.		

GAMTARBMODE - GAMT Arbiter Mode Control						
	4	GAMT Arbiter Mode Control 4 <table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>0 - ZTLB clock gate enabled. 1 - ZTLB clock gate disabled.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
	3	GAMT Arbiter Mode Control 3 <table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>0 - CVS clock gate enabled. 1 - CVS clock gate disabled.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
	2	GAMT Arbiter Mode Control 2 <table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>0 - No reg_hdc_inval_ack_force - take the value from client. 1 - reg_hdc_inval_ack_force - force value to 1 - disregard client value.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
	1	GAMT Arbiter Mode Control 1 <table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Bit [1]: Address Swizzling for Tiled Surfaces. This register location is updated via GFX Driver prior to enabling DRAM accesses. Driver needs to obtain the need for memory address swizzling via DRAM configuration registers and set the following bits (in Display Engine and Render/Media access streams). 0: No address Swizzling. 1: Address bit[1] needs to be swizzled for tiled surfaces.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
	0	GAMT Arbiter Mode Control 0 <table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Bit[0]: GAM to Bypass GTT Translation. GAM to Bypass GTT Translation and pass logical addresses through with 0's padded on the MSBs to form the Physical Address.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					

GAMW_ECO_BUS_RO_IA

GAMW_ECO_BUS_RO_IA - GAMW_ECO_BUS_RO_IA						
Register Space: MMIO: 0/2/0						
Project: BDW						
Default Value: 0x00000000						
Size (in bits): 32						
Address: 0408Ch						
DWord	Bit	Description				
0	31:0	<p>GAMWECO_BUS_RO_IA</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>This register is for ECO usage. RO register with IA Access Type on BUS reset.</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

GAMW_ECO_BUS_RW_IA

GAMW_ECO_BUS_RW_IA - GAMW_ECO_BUS_RW_IA						
Register Space: MMIO: 0/2/0						
Project: BDW						
Default Value: 0x00000000						
Size (in bits): 32						
Address: 04084h						
DWord	Bit	Description				
0	31:0	GAMWECO_BUS_RW_IA <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Default Value:</td><td style="padding: 2px;">0000000h</td></tr> <tr> <td style="padding: 2px;">Access:</td><td style="padding: 2px;">R/W</td></tr> </table> <p>This register is for ECO usage. RW register with IA Access Type on BUS reset.</p>	Default Value:	0000000h	Access:	R/W
Default Value:	0000000h					
Access:	R/W					

GAMW_ECO_DEV_RO_IA

GAMW_ECO_DEV_RO_IA - GAMW_ECO_DEV_RO_IA						
DWord	Bit	Description				
0	31:0	GAMWECO_DEV_RO_IA <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>This register is for ECO usage. RO register with IA Access Type on DEV reset.</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

GAMW_ECO_DEV_RW_IA

GAMW_ECO_DEV_RW_IA - GAMW_ECO_DEV_RW_IA		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04080h	
DWord	Bit	Description
0	31:0	GAMWECO_DEV_RW_IA Default Value: 00000000h Access: R/W

GAMW Power Context Save

PWRCTXSAVE - GAMW Power Context Save						
DWord	Bit	Description				
0	31:16	<p>Mask Bits</p> <table border="1"> <tr> <td>Default Value:</td> <td>0000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Mask Bits act as Write Enables for the bits[15:0] of this register.</p>	Default Value:	0000h	Access:	RO
Default Value:	0000h					
Access:	RO					
	15	<p>Extra Bits15</p> <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Extra Bits for future use.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
	14	<p>Extra Bits14</p> <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Extra Bits for future use.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
	13	<p>Extra Bits13</p> <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Extra Bits for future use.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
	12	<p>Extra Bits12</p> <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Extra Bits for future use.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
	11	<p>Extra Bits11</p> <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Extra Bits for future use.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
	10	<p>Extra Bits10</p> <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Extra Bits for future use.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					

PWRCTXSAVE - GAMW Power Context Save						
	9	<p>Power Context Save Request</p> <table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Power Context Save Bit[9]</p> <p>Power Context Save Request</p> <p>1'b0: Power context save is not being requested (default). 1'b1: Power context save is being requested. Unit needs to self-clear this bit upon sampling. This bit is self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
	8:0	<p>Power Context Save Quad Word Credits</p> <table border="1"> <tr> <td>Default Value:</td><td>000000000b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Power Context Save Bits[8:0]</p> <p>QWord Credits for Power Context Save Request</p> <p>An initial length packet is required per power context save session, but that packet does not consume a credit. See protocol description for more details.</p> <p>Minimum Credits = 1: Unit may send 1 QWord pair.</p> <p>Maximum Credits = 511: Unit may send 511 QWord pairs.</p> <p>A QWord pair is defined as a 32-bit register address and the corresponding 32-bits of register data.</p> <p>Only valid with PWRCTX_SAVE_REQ (Bit9).</p>	Default Value:	000000000b	Access:	R/W
Default Value:	000000000b					
Access:	R/W					

GARB Messaging Register for Boot Controller

MSG_GARB_MBC - GARB Messaging Register for Boot Controller

Register Space:	MMIO: 0/2/0
Project:	BDW
Default Value:	0x00000000
Size (in bits):	16
Address:	0801Ch
<p>Message registers have bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16].</p> <p>To set bit0, for example, the data would be 0x0001_0001.</p> <p>To clear bit0, for example, the data would be 0x0001_0000.</p> <p>Note that mask bit is the data bit offset + 16.</p> <p>Message registers are protected from non-GT writes via the Message Channel.</p>	

DWord	Bit	Description
0	15:7	Reserved Access: RO
	6	Fuse Download Done Indication Access: R/W <p>Fuse Download Done Indication. 1'b0: Fuse download is not complete yet (default). 1'b1: Fuse download is complete. GPMunit self-clears this bit upon sampling.</p>
	5	Boot Fetch Complete Indication Access: R/W <p>Boot Fetch Complete Indication. 1'b0: Boot Fetch is not complete yet (default). 1'b1: Boot Fetch is complete. GPMunit self-clears this bit upon sampling.</p>
	4	IDI Block Status Access: R/W <p>IDI Block Status. 1'b0: IDI interface is not blocked (default). 1'b1: IDI interface is blocked.</p>
	3	IDI Awake Status Access: R/W <p>IDI Awake Status. 1'b0: IDI interface is not ready (default). 1'b1: IDI interface is ready.</p>

MSG_GARB_MBC - GARB Messaging Register for Boot Controller

	2	Credit Active Status
		Access: R/W
		Credit Active Status. 1'b0: Send credit active deassert Event Bus Message on transition from 1'b1 => 1'b0 (default). 1'b1: Send credit active assert Event Bus Message on transition from 1'b0 => 1'b1.
	1	Global Arbitration Request
		Access: R/W
		Global Arbitration Request. 1'b0: No request (default). 1'b1: Request for arbitration. Full handshake requiring ack.
	0	Busy Indication
		Access: R/W
		Busy Indication. 1'b0: Idle (default). 1'b1: Busy. Full handshake requiring ack.

GARB Messaging Register for Clocking Unit

MSG_GARB_GCP - GARB Messaging Register for Clocking Unit

Register Space:	MMIO: 0/2/0			
Project:	BDW			
Default Value:	0x00000000			
Size (in bits):	16			
Address:	08024h			
<p>Message registers have bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16].</p> <p>To set bit0, for example, the data would be 0x0001_0001.</p> <p>To clear bit0, for example, the data would be 0x0001_0000.</p> <p>Note that mask bit is the data bit offset + 16.</p> <p>Message registers are protected from non-GT writes via the Message Channel.</p>				
DWord	Bit	Description		
0	15:3	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
Access:	RO			
2	GCP Request to send FLR Complete Message to SA via GAM <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>GCP Request to send FLR Complete Message to SA via GAM. 1'b0: No request (default). 1'b1: Send cycle on GA* Interface to address < address > with data < data >. GPM self-clears the request once it completes it. MBC needs to self-clear the acknowledgement once it sees it. GPM indicates a write cycle is complete once it puts it on the interface. GPM indicates a read cycle is complete once the read-return data comes back. GPMunit self-clears this bit upon sampling.</p>	Access:	R/W	
Access:	R/W			
1	Global Arbitration Request <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Global Arbitration Request. 1'b0: No request (default). 1'b1: Request for arbitration. Full handshake requiring ack.</p>	Access:	R/W	
Access:	R/W			
0	Busy Indication <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Busy Indication. 1'b0: Idle (default). 1'b1: Busy. Full handshake requiring ack.</p>	Access:	R/W	
Access:	R/W			

Gather Constants Not Consumed By RCS

GATHER_CONST_PRODUCE_COUNT - Gather Constants Not Consumed By RCS		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	0248Ch	
<p>This register keeps track of the outstanding Gather Constants produced by RS which are not yet consumed by Render Command Streamer. This register is part of the render context save and restore. This register should not be programmed by SW.</p>		
DWord	Bit	Description
0	31:0	Gather Constants Produce Count This register keeps track of the outstanding Gather Constants produced by RS which are not yet consumed by Render Command Streamer. This register is part of the render context save and restore.

GDR Per Client Write Drop Enables

WR_DROP_MODE - GDR Per Client Write Drop Enables								
DWord	Bit	Description						
0	31:0	<p>GDR Per Client Write Drop Enables</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>31 RSVD: Future use. 30 MBC write drop disable (0) or enable (1). 29 CS write drop disable (0) or enable (1). 28 SOL write drop disable (0) or enable (1). 27 RS write drop disable (0) or enable (1). 26 RCC write drop disable (0) or enable (1). 25 MSC write drop disable (0) or enable (1). 24 All L3 clients write drop disable (0) or enable (1). 23 STC write drop disable (0) or enable (1). 22 HIZ write drop disable (0) or enable (1). 21 RCZ write drop disable (0) or enable (1). 20 GAFS write drop disable (0) or enable (1). 19 GPM write drop disable (0) or enable (1). 18 GCP write drop disable (0) or enable (1). 17 VCS write drop disable (0) or enable (1). 16 BSP write drop disable (0) or enable (1). 15 VCR write drop disable (0) or enable (1). 14 VMX_RS write drop disable (0) or enable (1). 13 VMX_BS write drop disable (0) or enable (1). 12 VMX_RA write drop disable (0) or enable (1). 11 VMX_VDS write drop disable (0) or enable (1). 10 VLF_RS write drop disable (0) or enable (1). 9 VLF_FW write drop disable (0) or enable (1). 8 VECS write drop disable (0) or enable (1). 7 VEO write drop disable (0) or enable (1).</p> <table border="1"> <tr> <td>4 BCS write drop disable (0) or enable (1). 3 BLB write drop disable (0) or enable (1). 2 W_BSP write drop disable (0) or enable (1). 1 W_VMX_RS write drop disable (0) or enable (1). 0 W_VMX_BS write drop disable (0) or enable (1).</td><td></td></tr> </table>	Default Value:	00000000h	Access:	R/W	4 BCS write drop disable (0) or enable (1). 3 BLB write drop disable (0) or enable (1). 2 W_BSP write drop disable (0) or enable (1). 1 W_VMX_RS write drop disable (0) or enable (1). 0 W_VMX_BS write drop disable (0) or enable (1).	
Default Value:	00000000h							
Access:	R/W							
4 BCS write drop disable (0) or enable (1). 3 BLB write drop disable (0) or enable (1). 2 W_BSP write drop disable (0) or enable (1). 1 W_VMX_RS write drop disable (0) or enable (1). 0 W_VMX_BS write drop disable (0) or enable (1).								

GDR Write Drop

GDR_WR_DRP - GDR Write Drop		
Register Space: MMIO: 0/2/0		
Project: BDW		
Default Value: 0x00000000		
Size (in bits): 32		
Address: 04020h		
DWord	Bit	Description
0	31:0	GDR_WRITE_DROP Default Value: 00000000h Access: R/W

GFX Arbiter Client Priority Control

GFX_PRIO_CTRL - GFX Arbiter Client Priority Control						
DWord	Bit	Description				
0	31:27	<p>Read Rstrm Max Reject</p> <table border="1"> <tr> <td>Default Value:</td> <td>10001b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table>	Default Value:	10001b	Access:	R/W
Default Value:	10001b					
Access:	R/W					
26:21	<p>Extra Bits</p> <table border="1"> <tr> <td>Default Value:</td> <td>000000b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table>	Default Value:	000000b	Access:	R/W	
Default Value:	000000b					
Access:	R/W					
20:18	<p>sol_gam_priority</p> <table border="1"> <tr> <td>Default Value:</td> <td>010b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Client Priority Control Bits - Lowest Bit [18] is NOT Used.</p>	Default Value:	010b	Access:	R/W	
Default Value:	010b					
Access:	R/W					
17:15	<p>veo_gam_priority</p> <table border="1"> <tr> <td>Default Value:</td> <td>100b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Client Priority Control Bits - Lowest Bit [15] is NOT Used.</p>	Default Value:	100b	Access:	R/W	
Default Value:	100b					
Access:	R/W					
14:12	<p>vfw_gam_priority</p> <table border="1"> <tr> <td>Default Value:</td> <td>010b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Client Priority Control Bits - Lowest Bit [12] is NOT Used.</p>	Default Value:	010b	Access:	R/W	
Default Value:	010b					
Access:	R/W					
11:9	<p>gapc_gam_c_priority</p> <table border="1"> <tr> <td>Default Value:</td> <td>110b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Client Priority Control Bits - Lowest Bit [9] is NOT Used.</p>	Default Value:	110b	Access:	R/W	
Default Value:	110b					
Access:	R/W					
8:6	<p>gapc_gam_z_priority</p> <table border="1"> <tr> <td>Default Value:</td> <td>100b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Client Priority Control Bits - Lowest Bit [6] is NOT Used.</p>	Default Value:	100b	Access:	R/W	
Default Value:	100b					
Access:	R/W					

GFX_PRIO_CTRL - GFX Arbiter Client Priority Control

	5:3	gapc_gam_I3_priority		
		Default Value:	010b	
		Access:	R/W	
Client Priority Control Bits - Lowest Bit [3] is NOT Used.				
	2:0	csrvf_gam_priority		
		Default Value:	000b	
		Access:	R/W	
Client Priority Control Bits - Lowest Bit [0] is NOT Used.				

GFX Context Element Descriptor (High Part)

GFX_CTX_EDR_H - GFX Context Element Descriptor (High Part)

Register Space: MMIO: 0/2/0

Project: BDW

Default Value: 0x00000000

Size (in bits): 32

Address: 04404h

DWord	Bit	Description				
0	31:0	<p>GFX Context Element Descriptor (High Part)</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Bit[63:32] - Context ID: Context identification number assigned to separate this context from others. Context IDs need to be recycled in such a way that there cannot be two active contexts with the same ID. This is a unique identification number by which a context is identified and referenced.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

GFX Context Element Descriptor (Low Part)

GFX_CTX_EDR_L - GFX Context Element Descriptor (Low Part)						
DWord	Bit	Description				
0	31:0	<p>GFX Context Element Descriptor (Low Part)</p> <table border="1"> <tr> <td>Default Value:</td><td>00000009h</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Bit[31:12] - LRCA: Command Streamer Only.</p> <p>Bit[8] - Privileged Context / GTT vs PPGTT mode: Differs in legacy vs advanced context modes: In Legacy Context: Defines the page tables to be used. This is how page walker comes to know PPGTT vs GTT selection for the entire context. 0: Use Global GTT. 1: Use Per-Process GTT. In Advanced Context: Defines the privilege level for the context. 0: User mode context. 1: Supervisor mode context.</p> <p>Bit[5] - Deeper IA coherency Support: In Advanced Context: Defines the level of IA coherency. 0: IA coherency is provided at LLC level for all streams of GPU (i.e. Gen7.5 like mode). 1: IA coherency is provided at L3 level for EU data accesses of GPU.</p> <p>Bit[4] - A and D Support / 32 and 64b Address Support: Differs in legacy vs advanced context modes: In Legacy Context: Defines 32b vs 64b (48b canonical) addressing format: 0: 32b addressing format. 1: 64b (48b canonical) addressing format. In Advanced Context: Defines A and D bit support: 0: A and D bit management in page tables is NOT supported. 1: A and D bit management in page tables is supported.</p> <p>Bit[3] - Context Type: Legacy vs Advanced: Defines the context type 0: Advanced Context: Defines the rest of the advanced capabilities (i.e. OS page table support, fault models). Note that advanced context is not bounded to GPGPU. 1: Legacy Context: Defines the context as legacy mode which is similar to prior generations of Gen8. Note that: Bits [8:4] differs in functions when legacy vs advanced context modes are selected.</p> <p>Bit[2] - FR: Command streamer specific.</p> <p>Bit[1] - Scheduling Mode:</p>	Default Value:	00000009h	Access:	R/W
Default Value:	00000009h					
Access:	R/W					

GFX_CTX_EDR_L - GFX Context Element Descriptor (Low Part)

		<p>1: Indicates exelist mode of scheduling. 0: Indicates Ring Buffer mode of scheduling.</p> <p>Bit[0] - Valid: Indicates that element descriptor is valid. If GAM is programmed with an invalid descriptor, it continues but flags an error.</p>
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GFX Context Element Descriptor (Low Part)

GFX_CTX_EDR_L - GFX Context Element Descriptor (Low Part)						
DWord	Bit	Description				
0	31:0	<p>GFX Context Element Descriptor</p> <table border="1"> <tr> <td>Default Value:</td><td>00000009h</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Bit[31:12] - LRCA: Command Streamer Only.</p> <p>Bit[8] - Privileged Context / GTT vs PPGTT mode: Differs in legacy vs advanced context modes: In Legacy Context: Defines the page tables to be used. This is how page walker comes to know PPGTT vs GTT selection for the entire context. 0: Use Global GTT. 1: Use Per-Process GTT. In Advanced Context: Defines the privilege level for the context. 0: User mode context. 1: Supervisor mode context.</p> <p>Bit[5] - Deeper IA coherency Support: In Advanced Context: Defines the level of IA coherency. 0: IA coherency is provided at LLC level for all streams of GPU (i.e. Gen7.5 like mode). 1: IA coherency is provided at L3 level for EU data accesses of GPU.</p> <p>Bit[4] - A and D Support / 32 and 64b Address Support: Differs in legacy vs advanced context modes: In Legacy Context: Defines 32b vs 64b (48b canonical) addressing format: 0: 32b addressing format. 1: 64b (48b canonical) addressing format. In Advanced Context: Defines A and D bit support: 0: A and D bit management in page tables is NOT supported. 1: A and D bit management in page tables is supported.</p> <p>Bit[3] - Context Type: Legacy vs Advanced: Defines the context type 0: Advanced Context: Defines the rest of the advanced capabilities (i.e. OS page table support, fault models). Note that advanced context is not bounded to GPGPU. 1: Legacy Context: Defines the context as legacy mode which is similar to prior generations of Gen8. Note that: Bits [8:4] differs in functions when legacy vs advanced context modes are selected.</p> <p>Bit[2] - FR: Command streamer specific.</p> <p>Bit[1] - Scheduling Mode:</p>	Default Value:	00000009h	Access:	R/W
Default Value:	00000009h					
Access:	R/W					

GFX_CTX_EDR_L - GFX Context Element Descriptor (Low Part)

		<p>1: Indicates exelist mode of scheduling. 0: Indicates Ring Buffer mode of scheduling.</p> <p>Bit[0] - Valid: Indicates that element descriptor is valid. If GAM is programmed with an invalid descriptor, it continues but flags an error.</p>
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GFX Fault Counter

GFX_FAULT_CNTR - GFX Fault Counter		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	045A0h	
DWord	Bit	Description
0	31:0	GFX Fault Counter Default Value: 00000000h Access: RO

GFX Fixed Counter

GFX_FIXED_CNTR - GFX Fixed Counter		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	045A4h	
DWord	Bit	Description
0	31:0	GFX Fixed Counter
		Default Value: 00000000h
		Access: RO

GFX_PDP0/PML4/PASID Descriptor (High Part)

GFX_CTX_PDP0_H - GFX PDP0/PML4/PASID Descriptor (High Part)						
DWord	Bit	Description				
0	31:0	<p>GFX PDP0/PML4/PASID Descriptor (High Part)</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>PDP0/PML4/PASID: This register can contain three values which depend on the element descriptor definition. PASID[19:0]: Populated in the first 20bits of the register and selected when Advanced Context flag is set. PML4[38:12]: Pointer to base address of PML4 and selected when Legacy Context flag is set and 64b address support is selected. PDP0[38:12]: Pointer to one of the four page directory pointer (lowest) and defines the first 0-1GB of memory mapping. Note: This is a guest physical address.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

GFX_PDP0/PML4/PASID Descriptor (Low Part)

GFX_CTX_PDP0_L - GFX PDP0/PML4/PASID Descriptor (Low Part)						
DWord	Bit	Description				
0	31:0	<p>GFX PDP0/PML4/PASID Descriptor (Low Part)</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>PDP0/PML4/PASID: This register can contain three values which depend on the element descriptor definition. PASID[19:0]: Populated in the first 20 bits of the register and selected when Advanced Context flag is set. PML4[38:12]: Pointer to base address of PML4 and selected when Legacy Context flag is set and 64b address support is selected. PDP0[38:12]: Pointer to one of the four page directory pointer (lowest) and defines the first 0-1GB of memory mapping. Note: This is a guest physical address.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

GFX PDP1 Descriptor Register (High Part)

GFX_CTX_PDP1_H - GFX PDP1 Descriptor Register (High Part)						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04414h					
DWord	Bit	Description				
0	31:0	<p>GFX PDP1 Descriptor Register (High Part)</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Pointer to one of the four page directory pointer (lowest+1) and defines the first 1-2GB of memory mapping. Note: This is a guest physical address.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

GFX PDP1 Descriptor Register (Low Part)

GFX_CTX_PDP1_L - GFX PDP1 Descriptor Register (Low Part)						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04410h					
DWord	Bit	Description				
0	31:0	<p>GFX PDP1 Descriptor Register (Low Part)</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Pointer to one of the four page directory pointer (lowest+1) and defines the first 1-2GB of memory mapping. Note: This is a guest physical address.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

GFX PDP2 Descriptor Register (High Part)

GFX_CTX_PDP2_H - GFX PDP2 Descriptor Register (High Part)						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	0441Ch					
DWord	Bit	Description				
0	31:0	<p>GFX PDP2 Descriptor Register (High Part)</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Pointer to one of the four page directory pointer (lowest+2) and defines the first 2-3GB of memory mapping. Note: This is a guest physical address.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

GFX PDP2 Descriptor Register (Low Part)

GFX_CTX_PDP2_L - GFX PDP2 Descriptor Register (Low Part)						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04418h					
DWord	Bit	Description				
0	31:0	<p>GFX PDP2 Descriptor Register (Low Part)</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Pointer to one of the four page directory pointer (lowest+2) and defines the first 2-3GB of memory mapping. Note: This is a guest physical address.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

GFX PDP3 Descriptor Register (High Part)

GFX_CTX_PDP3_H - GFX PDP3 Descriptor Register (High Part)						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04424h					
DWord	Bit	Description				
0	31:0	<p>GFX PDP3 Descriptor Register (High Part)</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Pointer to one of the four page directory pointer (lowest+3) and defines the first 3-4GB of memory mapping. Note: This is a guest physical address.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

GFX PDP3 Descriptor Register (Low Part)

GFX_CTX_PDP3_L - GFX PDP3 DescriptorRegister(LowPart)						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04420h					
DWord	Bit	Description				
0	31:0	<p>GFX PDP3 Descriptor Register (Low Part)</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Pointer to one of the four page directory pointer (lowest+3) and defines the first 3-4GB of memory mapping. Note: This is a guest physical address.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

Global Capabilities, Minor and Major Version

GCAP_VMIN_VMAJ - Global Capabilities, Minor and Major Version

Register Space: MMIO: 0/3/0

Project: BDW

Default Value: 0x01002001

Access: RO

Size (in bits): 32

Address: 00000h-00003h

DWord	Bit	Description		
0	31:24	Major Version		
		Value	Name	Description
		01h	[Default]	Indicates major revision number 1 of the High Definition Audio specification, for specification version '1.0.' Should be reset to '01h'
		Programming Notes		
		Should be hardwired to "01h".		
0	23:16	Minor version		
		Value	Name	Description
		00h	[Default]	Indicates minor revision number 00h of the High Definition Audio specification, for specification version '1.0.' Reset to '00h'
		Programming Notes		
		Should be hardwired to "00h".		
0	15:12	Output Streams		
		Value	Name	Description
		0010b	[Default]	[All] A value of 0000b indicates that there are no Output Streams supported. A value of maximum 15 output streams are supported. [DevBDW] Three streams for BDW
		Programming Notes		
		Should be hardwired to "0010b".		
0	11:8	Input Streams		
		Value	Name	Description
		0000b		A value of 0000b indicates that there are no Input Streams supported. A maximum of 15 input streams are supported.
		Programming Notes		
		Should be hardwired to "0000b".		

GCAP_VMIN_VMAJ - Global Capabilities, Minor and Major Version

	7:3	BiDirectional Streams												
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0000b</td> <td></td> <td>A value of 0000b indicates that there are no Input Streams supported. A maximum of 15 input streams are supported.</td> </tr> </tbody> </table>	Value	Name	Description	0000b		A value of 0000b indicates that there are no Input Streams supported. A maximum of 15 input streams are supported.						
Value	Name	Description												
0000b		A value of 0000b indicates that there are no Input Streams supported. A maximum of 15 input streams are supported.												
		Programming Notes												
		Should be hardwired to "0000b".												
	2:1	Number of SDO Signal Software can enable the use of striping by setting the appropriate bit in the Stream Buffer Descriptor.												
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>01b</td> <td></td> <td>Indicates that two SDO lines are supported.</td> </tr> <tr> <td>10b</td> <td></td> <td>Indicates that four SDO lines are supported.</td> </tr> <tr> <td>11b</td> <td>Reserved</td> <td></td> </tr> </tbody> </table>	Value	Name	Description	01b		Indicates that two SDO lines are supported.	10b		Indicates that four SDO lines are supported.	11b	Reserved	
Value	Name	Description												
01b		Indicates that two SDO lines are supported.												
10b		Indicates that four SDO lines are supported.												
11b	Reserved													
	0	64 Addr Support												
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>1b</td> <td>[Default]</td> <td>Indicates that 64 bit addressing is supported by the controller for BDL addresses, data buffer addresses, and command buffer addresses.</td> </tr> <tr> <td>0b</td> <td></td> <td>Indicates that only 32-bit addressing is available. We support 64 bit addresses but the 64:39 are zeros.</td> </tr> </tbody> </table>	Value	Name	Description	1b	[Default]	Indicates that 64 bit addressing is supported by the controller for BDL addresses, data buffer addresses, and command buffer addresses.	0b		Indicates that only 32-bit addressing is available. We support 64 bit addresses but the 64:39 are zeros.			
Value	Name	Description												
1b	[Default]	Indicates that 64 bit addressing is supported by the controller for BDL addresses, data buffer addresses, and command buffer addresses.												
0b		Indicates that only 32-bit addressing is available. We support 64 bit addresses but the 64:39 are zeros.												
		Programming Notes												
		Must be hardwired to "1b".												

Global Control

GCTL - Global Control												
DWord	Bit	Description										
0	31:9	Reserved	Format: MBZ									
	8	UNSOL										
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disable [Default]</td> <td>Unsolicited responses are not accepted, and dropped on the floor.</td> </tr> <tr> <td>1b</td> <td>Enable</td> <td>Unsolicited Responses from the codecs are accepted by the controller and placed into the Response Input Ring Buffer.</td> </tr> </tbody> </table>		Value	Name	Description	0b	Disable [Default]	Unsolicited responses are not accepted, and dropped on the floor.	1b	Enable	Unsolicited Responses from the codecs are accepted by the controller and placed into the Response Input Ring Buffer.
Value	Name	Description										
0b	Disable [Default]	Unsolicited responses are not accepted, and dropped on the floor.										
1b	Enable	Unsolicited Responses from the codecs are accepted by the controller and placed into the Response Input Ring Buffer.										
		Programming Notes										
		This should be programmed to 1 by the driver.										
	7:2	Reserved	Format: MBZ									
	1	FCNTRL										
		Access:	R/W Set									
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disable [Default]</td> <td>Flush is completed</td> </tr> <tr> <td>1b</td> <td>Enable</td> <td>Flush Initiated</td> </tr> </tbody> </table>		Value	Name	Description	0b	Disable [Default]	Flush is completed	1b	Enable	Flush Initiated
Value	Name	Description										
0b	Disable [Default]	Flush is completed										
1b	Enable	Flush Initiated										
		Programming Notes										
		Writing a 1 to this bit initiates a flush. When the flush completion is received by the controller, hardware sets the Flush Status bit and clears this Flush Control bit. Before a flush cycle is initiated, the DMA Position Buffer must be programmed with a valid memory address by software, but the DMA Position Buffer bit 0 need not be set to enable the position reporting mechanism. Also, all streams must be stopped (the associated RUN bit must be 0). When the flush is initiated, the controller will flush pipelines to memory to guarantee that the hardware is ready to transition to a D3 state. Setting this bit is not a critical step in the power state transition if the content of the FIFOs is not critical.										

GCTL - Global Control

CRST				
	Value	Name	Description	
0	0b	Disable [Default]	Enter Reset State-Writing a 0 to this bit causes the Intel HD Audio controller to be reset. All state machines, FIFO's and non Suspend well memory mapped configuration registers (except ECAP and PCI Configuration Registers) in the controller will be reset. The Intel HD Audio link RESET# signal will be asserted and all other link signals will be driven to their "reset" values. After the hardware has completed sequencing into the reset state, it will report a 0 in this bit. Software must read a 0 from this bit to verify that the controller is in reset.	
	1b	Enable	Exit Reset State- Writing a 1 to this bit causes the controller to exit its reset state and de-assert the Intel HD Audio link RESET# signal. Software is responsible for setting/clearing this bit such that the minimum Intel HD Audio link RESET# signal assertion pulse width specification is met. When the controller hardware is ready to begin operation, it will report a 1 in this bit. Software must read a 1 from this bit before accessing any controller registers. The CRST# bit defaults to a 0 after hardware reset, therefore software needs to write a 1 to this bit to begin operation.	
Programming Notes				
	<p>Note that the CORB/RIRB RUN bits and all Stream RUN bits must be verified cleared to zero before CRST# is written to 0 (asserted) in order to assure a clean re-start. When setting or clearing CRST#, software must ensure that minimum link timing requirements (minimum RESET# assertion time, etc.) are met. When CRST# is 0 indicating that the controller is in reset, writes to all Intel HD Audio memory mapped registers are ignored as if the device is not present. The only exception is the Global Control register containing the CRST# bit itself. The Global Control register is write-able as a DWord, Word, or Byte even when CRST# is 0 if the byte enable for the byte containing the CRST# bit (Byte Enable 0) is active. If Byte Enable 0 is not active, writes to the Global Control register will be ignored when CRST# is 0. When CRST# is 0, reads to Intel HD Audio memory mapped registers will return their default value except for registers that are not reset with PLTRST# or on a D3hot -> D0 transition.</p>			

Global Invalidation Register

GLBLINVL - Global Invalidation Register						
DWord	Bit	Description				
0	31:3	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td colspan="2">Reserved.</td> </tr> </table>	Access:	RO	Reserved.	
Access:	RO					
Reserved.						
	2	<p>Cross sync read disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td colspan="2">lpconf_crs_sync_dis: Cross Sync Read Disable (CSRD). Cross Sync Read Disable (CSRD): Cross Sync Read Disable: upon a SYNC from HDC, follow with a write to cross SYNC Push and read to the same address. When set read is disabled.</td> </tr> </table>	Access:	R/W	lpconf_crs_sync_dis: Cross Sync Read Disable (CSRD). Cross Sync Read Disable (CSRD): Cross Sync Read Disable: upon a SYNC from HDC, follow with a write to cross SYNC Push and read to the same address. When set read is disabled.	
Access:	R/W					
lpconf_crs_sync_dis: Cross Sync Read Disable (CSRD). Cross Sync Read Disable (CSRD): Cross Sync Read Disable: upon a SYNC from HDC, follow with a write to cross SYNC Push and read to the same address. When set read is disabled.						
	1	<p>Disables hashing function</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td colspan="2">Disables hashing function (DISHF): Disables hashing function to generate bank_id[1:0] for L3\$ bank accessing, and forces the use of address[7:6] for bank_id[1:0]. 0: (default) Hash function enabled to generate L3\$ bank IDs. 1: L3\$ address[7:6] used as L3\$ bank IDs. lpconf_csr_l3bankidhashdis. (This bit needs to set corresponding bit lncf_csr_l3bankidhashdis in LNCF.)</td> </tr> </table>	Access:	R/W	Disables hashing function (DISHF): Disables hashing function to generate bank_id[1:0] for L3\$ bank accessing, and forces the use of address[7:6] for bank_id[1:0]. 0: (default) Hash function enabled to generate L3\$ bank IDs. 1: L3\$ address[7:6] used as L3\$ bank IDs. lpconf_csr_l3bankidhashdis. (This bit needs to set corresponding bit lncf_csr_l3bankidhashdis in LNCF.)	
Access:	R/W					
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	0	Reserved				

Global Status

GSTS - Global Status						
Register Space:	MMIO: 0/3/0					
Project:	BDW					
Default Value:	0x00000002					
Access:	R/W					
Size (in bits):	32					
Address:	00010h-00013h					
DWord	Bit	Description				
0	31:2	<p>Reserved</p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ		
Format:	MBZ					
	1	<p>FSTS</p> <table border="1"> <tr> <td>Default Value:</td> <td>0bh</td> </tr> <tr> <td>Access:</td> <td>R/WC</td> </tr> </table> <p>Programming Notes</p> <p>This bit is set to a 1 by the hardware to indicate that the flush cycle initiated when the FCNTRL bit was set has completed. Software must write a 1 to clear this bit before the next time FCNTRL is set.</p>	Default Value:	0bh	Access:	R/WC
Default Value:	0bh					
Access:	R/WC					
	0	<p>Reserved</p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ		
Format:	MBZ					

Global System Interrupt Routine

EU_GLOBAL_SIP - Global System Interrupt Routine

Register Space: MMIO: 0/2/0

Project: BDW

Default Value: 0x00000000

Access: R/W

Size (in bits): 32

Address: 0E42Ch

DWord	Bit	Description						
0	31:3	<p>Global SIP</p> <table border="1"> <tr> <td>Format:</td> <td>GraphicsAddress[31:3]</td> </tr> </table> <p>Specifies the base address for System Interrupt Routine that over-rides the SIP set by the state (STATE_SIP).</p>	Format:	GraphicsAddress[31:3]				
Format:	GraphicsAddress[31:3]							
	2:1	<p>Reserved</p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ				
Format:	MBZ							
	0	<p>Global SIP Enable</p> <p>The bit specifies if the System Routine starts from the Global SIP provided by the DW OR the SIP provided by the state (STATE_SIP)</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>SIP used is from STATE_EIP</td> </tr> <tr> <td>1</td> <td>SIP used is from MMIO register</td> </tr> </tbody> </table>	Value	Name	0	SIP used is from STATE_EIP	1	SIP used is from MMIO register
Value	Name							
0	SIP used is from STATE_EIP							
1	SIP used is from MMIO register							

GMBUS0

GMBUS0													
Register Space: MMIO: 0/2/0 Project: DevLPT Default Value: 0x00000000 Access: R/W Size (in bits): 32													
Address: C5100h-C5103h Name: GMBUS0 Clock/Port Select ShortName: GMBUS0 Power: Always on Reset: soft													
The GMBUS0 register controls the clock rate of the serial bus and the device the controller is connected to. This register should be configured before the first data valid bit is set.													
DWord	Bit	Description											
0	31:12	Reserved Format: MBZ											
	11	Reserved											
	10:8	GMBUS Rate Select These two bits select the rate that the GMBUS will run at. It also defines the AC timing parameters used. It should only be changed between transfers when the GMBUS is idle. <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>000b</td><td>100 KHz</td><td>100 KHz</td></tr> <tr> <td>001b</td><td>50 KHz</td><td>50 KHz</td></tr> <tr> <td>Others</td><td>Reserved</td><td>Reserved</td></tr> </tbody> </table>	Value	Name	Description	000b	100 KHz	100 KHz	001b	50 KHz	50 KHz	Others	Reserved
Value	Name	Description											
000b	100 KHz	100 KHz											
001b	50 KHz	50 KHz											
Others	Reserved	Reserved											
7:3	Reserved Format: MBZ												

GMBUS0

	2:0	Pin Pair Select This field selects a GMBUS pin pair for use in the GMBUS communication. Use the GPIO Pin Usage table above to determine which pin pairs are available for a particular device and the intended function of that pin pair. Note that it is not a straight forward mapping of port numbers to pair select numbers.
Value	Name	Description
000b	None	None (Disabled)
010b	DAC DDC	DDC for Analog monitor (VGA/CRT DAC)
100b	DDIC	DDC for HDMI/DVI port C
101b	DDIB	DDC for HDMI/DVI port B
110b	DDID	DDC for HDMI/DVI port D
111b	Reserved	Reserved

GMBUS1

GMBUS1															
Register Space:	MMIO: 0/2/0														
Project:	DevLPT														
Default Value:	0x00000000														
Access:	R/W Protect														
Size (in bits):	32														
Address:	C5104h-C5107h														
Name:	GMBUS1 Command/Status														
ShortName:	GMBUS1														
Power:	Always on														
Reset:	soft														
<p>This register lets the software indicate to the GMBUS controller the slave device address, register index, and indicate when the data write is complete. When the SW_CLR_INT bit is asserted, all writes to the GMBUS2, GMBUS3, and GMBUS4 registers are discarded. The GMBUS1 register writes to any other bit except the SW_CLR_INT are also lost. Reads to these registers always work normally regardless of the state of the SW_CLR_INT bit.</p>															
Workaround															
<p>On LP systems with ISCLK PLL shutdown enabled, display register C2020h bit 12 must be set to 1b before sending a GMBUS transaction. If no other feature requires register C2020h bit 12, it can be cleared to 0b after the GMBUS transaction is complete. To save power, register C2020h bit 12 must be cleared to 0b when internal graphics is put in the D3 device power state.</p>															
DWord	Bit	Description													
0	31	<p>Software Clear Interrupt</p> <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> <tr> <td colspan="2">(SW_CLR_INT) This bit must be clear for normal operation. Setting the bit then clearing it acts as local reset to the GMBUS controller. This bit is commonly used by software to clear a BUS_ERROR when a slave device delivers a NACK.</td></tr> </table> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Clear HW_RDY</td><td>If this bit is written as a zero when its current state is a one, will clear the HW_RDY bit and allows register writes to be accepted to the GMBUS registers (Write Protect Off). This bit is cleared to zero when an event causes the HW_RDY bit transition to occur.</td></tr> <tr> <td>1b</td><td>Assert HW_RDY</td><td>Asserted by software after servicing the GMBUS interrupt. Setting this bit causes the INT status bit to be cleared. Setting (1) this bit also asserts the HW_RDY bit (until this bit is written with a 0). When this bit is set, no writes to GMBUS registers will cause the contents to change with the exception of this bit which can be written.</td></tr> </tbody> </table>	Access:	R/W	(SW_CLR_INT) This bit must be clear for normal operation. Setting the bit then clearing it acts as local reset to the GMBUS controller. This bit is commonly used by software to clear a BUS_ERROR when a slave device delivers a NACK.		Value	Name	Description	0b	Clear HW_RDY	If this bit is written as a zero when its current state is a one, will clear the HW_RDY bit and allows register writes to be accepted to the GMBUS registers (Write Protect Off). This bit is cleared to zero when an event causes the HW_RDY bit transition to occur.	1b	Assert HW_RDY	Asserted by software after servicing the GMBUS interrupt. Setting this bit causes the INT status bit to be cleared. Setting (1) this bit also asserts the HW_RDY bit (until this bit is written with a 0). When this bit is set, no writes to GMBUS registers will cause the contents to change with the exception of this bit which can be written.
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GMBUS1

	30	Software Ready (SW_RDY) Data handshake bit used in conjunction with HW_RDY bit.																													
		<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="background-color: #d9e1f2;">Value</th><th style="background-color: #d9e1f2;">Name</th><th style="background-color: #d9e1f2;">Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>De-Assert</td><td>De-asserted via the assertion event for HW_RDY bit</td></tr> <tr> <td>1b</td><td>SW Assert</td><td>When asserted by software, results in de-assertion of HW_RDY bit</td></tr> </tbody> </table>			Value	Name	Description	0b	De-Assert	De-asserted via the assertion event for HW_RDY bit	1b	SW Assert	When asserted by software, results in de-assertion of HW_RDY bit																		
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1b	SW Assert	When asserted by software, results in de-assertion of HW_RDY bit																													
	29	Enable Timeout (ENT) Enables timeout for slave response. When this bit is enabled and the slave device response has exceeded the timeout period, the GMBUS Slave Stall Timeout Error interrupt bit is set.																													
		<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="background-color: #d9e1f2;">Value</th><th style="background-color: #d9e1f2;">Name</th><th style="background-color: #d9e1f2;">Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Disable</td><td>Disable timeout counter</td></tr> <tr> <td>1b</td><td>Enable</td><td>Enable timeout counter</td></tr> </tbody> </table>			Value	Name	Description	0b	Disable	Disable timeout counter	1b	Enable	Enable timeout counter																		
Value	Name	Description																													
0b	Disable	Disable timeout counter																													
1b	Enable	Enable timeout counter																													
	28	Reserved																													
		Format:		MBZ																											
	27:25	Bus Cycle Select GMBUS cycle will always consist of a START followed by Slave Address, followed by an optional read or write data phase. A read cycle with an index will consist of a START followed by a Slave Address a WRITE indication and the INDEX and then a RESTART with a Slave Address and an optional read data phase. The GMBUS cycle will terminate either with a STOP or by entering a wait state. The WAIT state is exited by generating a STOP or by starting another GMBUS cycle. This can only cause a STOP to be generated if a GMBUS cycle is generated, the GMBUS is currently in a data phase, or it is in a WAIT phase: Note that the three bits can be decoded as follows: 27 = STOP generated 26 = INDEX used 25 = Cycle ends in a WAIT																													
		<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="background-color: #d9e1f2;">Value</th><th style="background-color: #d9e1f2;">Name</th><th style="background-color: #d9e1f2;">Description</th></tr> </thead> <tbody> <tr> <td>000b</td><td>No cycle</td><td>No GMBUS cycle is generated</td></tr> <tr> <td>001b</td><td>No Index, No Stop, Wait</td><td>GMBUS cycle is generated without an INDEX, with no STOP, and ends with a WAIT</td></tr> <tr> <td>010b</td><td>Reserved</td><td>Reserved</td></tr> <tr> <td>011b</td><td>Index, No Stop, Wait</td><td>GMBUS cycle is generated with an INDEX, with no STOP, and ends with a WAIT</td></tr> <tr> <td>100b</td><td>Gen Stop</td><td>Generates a STOP if currently in a WAIT or after the completion of the current byte if active</td></tr> <tr> <td>101b</td><td>No Index, Stop</td><td>GMBUS cycle is generated without an INDEX and with a STOP</td></tr> <tr> <td>110b</td><td>Reserved</td><td>Reserved</td></tr> <tr> <td>111b</td><td>Index, Stop</td><td>GMBUS cycle is generated with an INDEX and with a STOP</td></tr> </tbody> </table>			Value	Name	Description	000b	No cycle	No GMBUS cycle is generated	001b	No Index, No Stop, Wait	GMBUS cycle is generated without an INDEX, with no STOP, and ends with a WAIT	010b	Reserved	Reserved	011b	Index, No Stop, Wait	GMBUS cycle is generated with an INDEX, with no STOP, and ends with a WAIT	100b	Gen Stop	Generates a STOP if currently in a WAIT or after the completion of the current byte if active	101b	No Index, Stop	GMBUS cycle is generated without an INDEX and with a STOP	110b	Reserved	Reserved	111b	Index, Stop	GMBUS cycle is generated with an INDEX and with a STOP
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110b	Reserved	Reserved																													
111b	Index, Stop	GMBUS cycle is generated with an INDEX and with a STOP																													
	24:16	Total Byte Count																													
		Format:		MBZ																											
		This determines the total number of bytes to be transferred during the DATA phase of a GMBUS cycle. The DATA phase can be prematurely terminated by generating a STOP while in the DATA phase (see Bus Cycle Select). Do not change the value of this field during GMBUS cycles transactions.																													

GMBUS1

	15:8	8 bit Slave Register Index (INDEX) This field specifies the 8-bits of index to be used for the generated bus write transaction or the index used for the WRITE portion of the WRITE/READ pair. It only has an effect if the enable Index bit is set. Do not change this field during a GMBUS transaction.																		
	7:0	Slave Address And Direction Bits 7:1 = 7-bit GMBUS Slave Address (SADDR): When a GMBUS cycle is to be generated using the Bus Cycle Select field, this field specifies the value of the slave address that is to be sent out. For use with 10-bit slave address devices, set this value to 11110XXb (where the last two bits (XX) are the two MSBs of the 10-bit address) and the slave direction bit to a write. This is followed by the first data byte being the 8 LSBs of the 10-bit slave address. Bit 0 = Slave Direction Bit: When a GMBUS cycle is to be generated based on the Bus Cycle Select, this bit determines if the operation will be a read or a write. A read operation with the index enabled will perform a write with just the index followed by a re-start and a read. A 1 indicates that a Read from the slave device operation is to be performed. A 0 indicates that a Write to the slave device operation is to be performed.																		
<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>00000001b</td><td>General</td><td>General Call Address</td></tr> <tr> <td>00000000b</td><td>Start</td><td>Start Bye</td></tr> <tr> <td>0000001Xb</td><td>CBUS</td><td>CBUS Address</td></tr> <tr> <td>11110XXXb</td><td>10-bit</td><td>10-Bit addressing</td></tr> <tr> <td>Others</td><td>Reserved</td><td>Reserved</td></tr> </tbody> </table>			Value	Name	Description	00000001b	General	General Call Address	00000000b	Start	Start Bye	0000001Xb	CBUS	CBUS Address	11110XXXb	10-bit	10-Bit addressing	Others	Reserved	Reserved
Value	Name	Description																		
00000001b	General	General Call Address																		
00000000b	Start	Start Bye																		
0000001Xb	CBUS	CBUS Address																		
11110XXXb	10-bit	10-Bit addressing																		
Others	Reserved	Reserved																		

GMBUS2

GMBUS2												
Register Space: MMIO: 0/2/0 Project: DevLPT Default Value: 0x00000800 Access: R/W Protect Size (in bits): 32												
Address: C5108h-C510Bh Name: GMBUS2 Status ShortName: GMBUS2 Power: Always on Reset: soft												
DWord	Bit	Description										
0	31:16	Reserved <table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ								
Format:	MBZ											
15	INUSE Software wishing to arbitrate for the GMBUS resource can poll this bit until it reads a zero and will then own usage of the GMBUS controller. This bit has no effect on the hardware, and is only used as semaphore among various independent software threads that don't know how to synchronize their use of this resource that may need to use the GMBUS logic. Writing a one to this bit is software's indication that the software use of this resource is now terminated and it is available for other clients. <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>GMBUS is Acquired</td><td>Read operation that contains a zero in this bit position indicates that the GMBUS engine is now acquired and the subsequent reads of this register will now have this bit set. Writing a 0 to this bit has no effect.</td></tr> <tr> <td>1b</td><td>GMBUS in Use</td><td>Read operation that contains a one for this bit indicates that the GMBUS is currently allocated to someone else and "In use". Once set, a write of a 1 to this bit indicates that the software has relinquished the GMBUS resource and will reset the value of this bit to a 0.</td></tr> </tbody> </table>	Value	Name	Description	0b	GMBUS is Acquired	Read operation that contains a zero in this bit position indicates that the GMBUS engine is now acquired and the subsequent reads of this register will now have this bit set. Writing a 0 to this bit has no effect.	1b	GMBUS in Use	Read operation that contains a one for this bit indicates that the GMBUS is currently allocated to someone else and "In use". Once set, a write of a 1 to this bit indicates that the software has relinquished the GMBUS resource and will reset the value of this bit to a 0.		
Value	Name	Description										
0b	GMBUS is Acquired	Read operation that contains a zero in this bit position indicates that the GMBUS engine is now acquired and the subsequent reads of this register will now have this bit set. Writing a 0 to this bit has no effect.										
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14	Hardware Wait Phase <table border="1"> <tr> <td>Access:</td><td>RO</td></tr> </table> (HW_WAIT_PHASE) Once in a WAIT_PHASE, the software can now choose to generate a STOP cycle or a repeated start (RESTART) cycle followed by another GMBUS transaction on the GMBUS. <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>No Wait</td><td>The GMBUS engine is not in a wait phase.</td></tr> <tr> <td>1b</td><td>Wait</td><td>Set when GMBUS engine is in wait phase. Wait phase is entered at the end of the current transaction when that transaction is selected not to terminate with a STOP.</td></tr> </tbody> </table>	Access:	RO	Value	Name	Description	0b	No Wait	The GMBUS engine is not in a wait phase.	1b	Wait	Set when GMBUS engine is in wait phase. Wait phase is entered at the end of the current transaction when that transaction is selected not to terminate with a STOP.
Access:	RO											
Value	Name	Description										
0b	No Wait	The GMBUS engine is not in a wait phase.										
1b	Wait	Set when GMBUS engine is in wait phase. Wait phase is entered at the end of the current transaction when that transaction is selected not to terminate with a STOP.										

GMBUS2

	13	Slave Stall Timeout Error									
		<table border="1"> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>This bit indicates that a slave stall timeout has occurred. It is tied to the Enable Timeout (ENT) bit.</p>	Access:	RO							
Access:	RO										
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>No Slave Timeout</td><td>No slave timeout has occurred</td></tr> <tr> <td>1b</td><td>Slave Timeout</td><td>A slave acknowledge timeout has occurred</td></tr> </tbody> </table>	Value	Name	Description	0b	No Slave Timeout	No slave timeout has occurred	1b	Slave Timeout	A slave acknowledge timeout has occurred
Value	Name	Description									
0b	No Slave Timeout	No slave timeout has occurred									
1b	Slave Timeout	A slave acknowledge timeout has occurred									
	12	GMBUS Interrupt Status									
		<table border="1"> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>This bit indicates that an event that causes a GMBUS interrupt has occurred.</p>	Access:	RO							
Access:	RO										
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Value	Name	Description									
0b	No Interrupt	The conditions that could cause a GMBUS interrupt have not occurred or this bit has been cleared by software assertion of the SW_CLR_INT bit.									
1b	Interrupt	GMBUS interrupt event occurred. This interrupt must have been one of the types enabled in the GMBUS4 register									
	11	Hardware Ready									
		<table border="1"> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>(HW_RDY) This provides a method of detecting when the current software client routine can proceed with the next step in a sequence of GMBUS operations. This data handshake bit is used in conjunction with the SW_RDY bit. When this bit is asserted by the GMBUS controller, it results in the de-assertion of the SW_RDY bit. This bit resumes to normal operation when the SW_CLR_INT bit is written to a 0.</p>	Access:	RO							
Access:	RO										
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>0</td><td>Condition required for assertion has not occurred or when this bit is a one and: - SW_RDY bit has been asserted - During a GMBUS read transaction, after the each read of the data register - During a GMBUS write transaction, after each write of the data register - SW_CLR_INT bit has been cleared</td></tr> <tr> <td>1b</td><td>1 [Default]</td><td>This bit is asserted under the following conditions: - After a reset or when the transaction is aborted by the setting of the SW_CLR_INT bit - When an active GMBUS cycle has terminated with a STOP - When during a GMBUS write transaction, the data register needs and can accept another four bytes of data - During a GMBUS read transaction, this bit is asserted when the data register has four bytes of new data or the read transaction DATA phase is complete and the data register contains the last few bytes of the read data</td></tr> </tbody> </table>	Value	Name	Description	0b	0	Condition required for assertion has not occurred or when this bit is a one and: - SW_RDY bit has been asserted - During a GMBUS read transaction, after the each read of the data register - During a GMBUS write transaction, after each write of the data register - SW_CLR_INT bit has been cleared	1b	1 [Default]	This bit is asserted under the following conditions: - After a reset or when the transaction is aborted by the setting of the SW_CLR_INT bit - When an active GMBUS cycle has terminated with a STOP - When during a GMBUS write transaction, the data register needs and can accept another four bytes of data - During a GMBUS read transaction, this bit is asserted when the data register has four bytes of new data or the read transaction DATA phase is complete and the data register contains the last few bytes of the read data
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0b	0	Condition required for assertion has not occurred or when this bit is a one and: - SW_RDY bit has been asserted - During a GMBUS read transaction, after the each read of the data register - During a GMBUS write transaction, after each write of the data register - SW_CLR_INT bit has been cleared									
1b	1 [Default]	This bit is asserted under the following conditions: - After a reset or when the transaction is aborted by the setting of the SW_CLR_INT bit - When an active GMBUS cycle has terminated with a STOP - When during a GMBUS write transaction, the data register needs and can accept another four bytes of data - During a GMBUS read transaction, this bit is asserted when the data register has four bytes of new data or the read transaction DATA phase is complete and the data register contains the last few bytes of the read data									

GMBUS2											
	10	NAK Indicator									
		<table border="1"> <tr> <td>Access:</td><td style="text-align: right;">RO</td></tr> </table>	Access:	RO							
Access:	RO										
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>No bus error</td><td>No bus error has been detected or SW_CLR_INT has been written as a zero since the last bus error</td></tr> <tr> <td>1b</td><td>No Ack</td><td>Set by hardware if any expected device acknowledge is not received from the slave within the timeout</td></tr> </tbody> </table>	Value	Name	Description	0b	No bus error	No bus error has been detected or SW_CLR_INT has been written as a zero since the last bus error	1b	No Ack	Set by hardware if any expected device acknowledge is not received from the slave within the timeout
Value	Name	Description									
0b	No bus error	No bus error has been detected or SW_CLR_INT has been written as a zero since the last bus error									
1b	No Ack	Set by hardware if any expected device acknowledge is not received from the slave within the timeout									
	9	GMBUS Active									
		<table border="1"> <tr> <td>Access:</td><td style="text-align: right;">RO</td></tr> </table> <p>(GA) This is a status bit that indicates whether the GMBUS controller is in an IDLE state or not.</p>	Access:	RO							
Access:	RO										
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Idle</td><td>The GMBUS controller is currently IDLE</td></tr> <tr> <td>1b</td><td>Active</td><td>This indicates that the bus is in START, ADDRESS, INDEX, DATA, WAIT, or STOP Phase. Set when GMBUS hardware is not IDLE.</td></tr> </tbody> </table>	Value	Name	Description	0b	Idle	The GMBUS controller is currently IDLE	1b	Active	This indicates that the bus is in START, ADDRESS, INDEX, DATA, WAIT, or STOP Phase. Set when GMBUS hardware is not IDLE.
Value	Name	Description									
0b	Idle	The GMBUS controller is currently IDLE									
1b	Active	This indicates that the bus is in START, ADDRESS, INDEX, DATA, WAIT, or STOP Phase. Set when GMBUS hardware is not IDLE.									
	8:0	Current Byte Count									
		<table border="1"> <tr> <td>Access:</td><td style="text-align: right;">RO</td></tr> </table> <p>Can be used to determine the number of bytes currently transmitted/received by the GMBUS controller hardware. Hardware sets it to zero at the start of a GMBUS transaction data transfer and incremented after the completion of each byte of the data phase. Note that because reads have internal storage, the byte count on a read operation may be ahead of the data that has been accepted from the data register.</p>	Access:	RO							
Access:	RO										

GMBUS3

GMBUS3		
Register Space:	MMIO: 0/2/0	
Project:	DevLPT	
Default Value:	0x00000000	
Access:	R/W Protect	
Size (in bits):	32	
Double Buffer	HW_RDY	
Update Point:		
Address:	C510Ch-C510Fh	
Name:	GMBUS3 Data Buffer	
ShortName:	GMBUS3	
Power:	Always on	
Reset:	soft	
<p>This is the data read/write register. This register is double buffered. Bit 0 is the first bit sent or read, bit 7 is the 8th bit sent or read, all the way through bit 31 being the 32nd bit sent or read. For GMBUS write operations with a non-zero byte count, this register should be written with the data before the GMBUS cycle is initiated. For byte counts that are greater than four bytes, this register will be written with subsequent data only after the HW_RDY status bit is set indicating that the register is now ready for additional data. For GMBUS read operations, software should wait until the HW_RDY bit indicates that the register contains the next set of valid read data before reading this register.</p>		
DWord	Bit	Description
0	31:24	Data Byte 3
	23:16	Data Byte 2
	15:8	Data Byte 1
	7:0	Data Byte 0

GMBUS4

GMBUS4		
Register Space: MMIO: 0/2/0 Project: DevLPT Default Value: 0x00000000 Access: R/W Size (in bits): 32		
Address: C5110h-C5113h Name: GMBUS4 Interrupt Mask ShortName: GMBUS4 Power: Always on Reset: soft		
DWord	Bit	Description
0	31:5	Reserved Format: MBZ
	4:0	Interrupt Mask This field specifies which GMBUS interrupt events may contribute to the setting of GMBUS interrupt status bit in the second level interrupt status register. For writes, the HW Ready (HWRDY) interrupt indicates that software can write the next DWORD. It does NOT mean that the transfer of data to the slave device has completed. The IDLE or HW wait interrupt may be used to detect the end of writing data to the slave device. The HWRDY interrupt may be used for gmbus write cycles only to detect when to write the next DWORD after the first two DWORDs have been written to GMBUS3. For reads, the HWRDY interrupt indicates the arrival of the next dword.
	Value	Name
	0b	
	0XXXXb	Slave stall TO Disable
	1XXXXb	Slave stall TO Enable
	X0XXXb	NAK Disable
	X1XXXb	NAK Enable
	XX0XXb	Idle Disable
	XX1XXb	Idle Enable
	XXX0Xb	HW Wait Disable
	XXX1Xb	HW Wait Enable
	XXXX0b	HW Ready Disable
	XXXX1b	HW Ready Enable

GMBUS5

GMBUS5			
Register Space: MMIO: 0/2/0 Project: DevLPT Default Value: 0x00000000 Access: R/W Size (in bits): 32			
Address: C5120h-C5123h Name: GMBUS5 2 Byte Index ShortName: GMBUS5 Power: Always on Reset: soft			
This register provides a method for the software indicate to the GMBUS controller the 2 byte device index.			
DWord	Bit	Description	
0	31	2 Byte Index Enable When this bit is asserted (1), then bits 15:0 are used as the index. Bits 15:8 are used in the first byte which is the most significant index bits. The slave index in the GMBUS1<15:8> are ignored. Bits 7:0 are used in the second byte which is the least significant index bits.	
	30:16	Reserved <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:
Format:	MBZ		
15:0	2 Byte Slave Index This is the 2 byte index used in all GMBUS accesses when bit 31 is asserted (1).		

GMCH Graphics Control

GGC_0_0_0_PCI - GMCH Graphics Control						
DWord	Bit	Description				
0	15:8	<p>Graphics Mode Select</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000101b</td> </tr> <tr> <td>Access:</td> <td>R/W Lock</td> </tr> </table> <p>This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics device in VGA (non-linear) and Native (linear) modes. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled. Hardware does not clear or set any of these bits automatically based on IGD being disabled/enabled. BIOS Requirement: BIOS must not set this field to 0h if IVD (bit 1 of this register) is 0.</p> <p>00h:0MB 01h:32MB 02h:64MB 03h:96MB 04h:128MB 05h:160MB (default) 06h:192MB 07h:224MB 08h:256MB 09h:288MB 0Ah:320MB 0Bh:352MB 0Ch:384MB 0Dh:416MB 0Eh:448MB 0Fh:480MB 10h:512MB 11h - 1Fh: Reserved 20h:1024MB 21h - 2Fh: Reserved 30h:1536MB 31h - 3Eh: Reserved 3Fh: 2016MB 40h - FFh: Reserved Hardware functionality in case of programming this value to Reserved is not guaranteed.</p>	Default Value:	00000101b	Access:	R/W Lock
Default Value:	00000101b					
Access:	R/W Lock					

GGC_0_0_0_PCI - GMCH Graphics Control

		GTT Graphics Memory Size	
7:6		Default Value:	00b
		Access:	R/W Lock
		<p>This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics Translation Table. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled. GSM is assumed to be a contiguous physical DRAM space with DSM, and BIOS needs to allocate a contiguous memory chunk. Hardware will derive the base of GSM from DSM only using the GSM size programmed in the register. Hardware functionality in case of programming this value to Reserved is not guaranteed.</p> <p>0x0: No Preallocated Memory 0x1: 2MB of Preallocated Memory 0x2: 4MB of Preallocated Memory 0x3: 8MB of Preallocated Memory</p>	
		Reserved	
		Format:	MBZ
5:3		Versatile Acceleration Mode Enable	
		Default Value:	0b
		Access:	R/W Lock
		<p>Enables the use of the iGFX engines for Versatile Acceleration. 1 - iGFX engines are in Versatile Acceleration Mode. Device 2 Class Code is 048000h. 0 - iGFX engines are in iGFX Mode. Device 2 Class Code is 030000h.</p>	
		IGD VGA Disable	
2		Default Value:	0b
		Access:	R/W Lock
		<p>0: Enable. Device 2 (IGD) claims VGA memory and IO cycles, the Sub-Class Code within Device 2 Class Code register is 00. 1: Disable. Device 2 (IGD) does not claim VGA cycles (Mem and IO), and the Sub- Class Code field within Device 2 function 0 Class Code register is 80. BIOS Requirement: BIOS must not set this bit to 0 if the GMS field pre-allocates no memory. This bit MUST be set to 1 if Device 2 is disabled either via a fuse or fuse override (CAPID0_A[IGD] = 1) or via a register (DEVEN[3] = 0).</p>	
		GGC Lock	
		Default Value:	0b
1		Access:	R/W Key Lock
		<p>When set to 1b, this bit will lock all bits in this register.</p>	

GO Messaging Register for GAMunit

MSG_GO_GAM - GO Messaging Register for GAMunit						
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x00000000 Size (in bits): 16 Address: 08028h						
Message registers have bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16]. To set bit0, for example, the data would be 0x0001_0001. To clear bit0, for example, the data would be 0x0001_0000. Note that mask bit is the data bit offset + 16. Message registers are protected from non-GT writes via the Message Channel. GA* Response to Allow Graphics Cycles to Read/Write from Memory. 1'b0: No gfx cycles allowed to memory (default). 1'b1: Allow gfx cycles to memory. GPM currently only ever sends the same GO request for all agents; either all is go=0, or all is go=1.						
DWord	Bit	Description				
0	15:7	Reserved <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Project:	BDW	Access:	RO
Project:	BDW					
Access:	RO					
6	GA* Response to Allow Wi-Di Graphics Cycles to Read/Write from Memory <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> <tr> <td colspan="2">[6] Controls Wi-Di Cycles (winunit).</td></tr> </table>	Access:	R/W	[6] Controls Wi-Di Cycles (winunit).		
Access:	R/W					
[6] Controls Wi-Di Cycles (winunit).						
5	Reserved					
4	GA* Response to Allow Blitter Graphics Cycles to Read/Write from Memory <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> <tr> <td colspan="2">[4] Controls Blitter Cycles (bcsunit).</td></tr> </table>	Access:	R/W	[4] Controls Blitter Cycles (bcsunit).		
Access:	R/W					
[4] Controls Blitter Cycles (bcsunit).						
3	GA* Response to Allow VEBox Graphics Cycles to Read/Write from Memory <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> <tr> <td colspan="2">[3] Controls VEBox Cycles (vecsunit).</td></tr> </table>	Access:	R/W	[3] Controls VEBox Cycles (vecsunit).		
Access:	R/W					
[3] Controls VEBox Cycles (vecsunit).						
2	GA* Response to Allow Media1 Graphics Cycles to Read/Write from Memory <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> <tr> <td colspan="2">[2] Controls Media1 Cycles (vcs1unit).</td></tr> </table>	Access:	R/W	[2] Controls Media1 Cycles (vcs1unit).		
Access:	R/W					
[2] Controls Media1 Cycles (vcs1unit).						
1	GA* Response to Allow Media0 Graphics Cycles to Read/Write from Memory <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> <tr> <td colspan="2">[1] Controls Media0 Cycles (vcs0unit).</td></tr> </table>	Access:	R/W	[1] Controls Media0 Cycles (vcs0unit).		
Access:	R/W					
[1] Controls Media0 Cycles (vcs0unit).						

MSG_GO_GAM - GO Messaging Register for GAMunit

	0	GA* Response to Allow Render Graphics Cycles to Read/Write from Memory
		Access: R/W [0] Controls Render Cycles (csunit).

Go Protocol GAM Request

GO_GAM_REQ - Go Protocol GAM Request								
DWord	Bit	Description						
0	31:16	Mask Bits <table border="1"> <tr> <td>Default Value:</td> <td>0000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Reserved.	Default Value:	0000h	Access:	RO		
Default Value:	0000h							
Access:	RO							
	15	GO_PROTOCOL_GAM_REQUEST15 <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> Go Protocol Request Reasons: 1'b0: Engine will NOT be resetting. 1'b1: Engine will be resetting (FLR/RC6 Enter or Soft Reset). Preparation for FLR (device) reset (cdevrst_b).	Default Value:	0b	Project:	BDW	Access:	R/W
Default Value:	0b							
Project:	BDW							
Access:	R/W							
	14	GO_PROTOCOL_GAM_REQUEST14 <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> Go Protocol Request Reasons: 1'b0: Engine will NOT be resetting. 1'b1: Engine will be resetting (FLR/RC6 Enter or Soft Reset). Preparation for Media1 reset (vcs1unit).	Default Value:	0b	Project:	BDW	Access:	R/W
Default Value:	0b							
Project:	BDW							
Access:	R/W							
	13	GO_PROTOCOL_GAM_REQUEST13 <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> Go Protocol Request Reasons: 1'b0: Engine will NOT be resetting. 1'b1: Engine will be resetting (FLR/RC6 Enter or Soft Reset). Preparation for Wi-Di reset (winunit).	Default Value:	0b	Project:	BDW	Access:	R/W
Default Value:	0b							
Project:	BDW							
Access:	R/W							

GO_GAM_REQ - Go Protocol GAM Request

		GO_PROTOCOL_GAM_REQUEST12						
	12	<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Go Protocol Request Reasons: 1'b0: Engine will NOT be resetting. 1'b1: Engine will be resetting (FLR/RC6 Enter or Soft Reset).</p>	Default Value:	0b	Project:	BDW	Access:	R/W
Default Value:	0b							
Project:	BDW							
Access:	R/W							
	11	<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Go Protocol Request Reasons: 1'b0: Engine will NOT be resetting. 1'b1: Engine will be resetting (FLR/RC6 Enter or Soft Reset). Preparation for Blitter reset (bcsunit).</p>	Default Value:	0b	Project:	BDW	Access:	R/W
Default Value:	0b							
Project:	BDW							
Access:	R/W							
	10	<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Go Protocol Request Reasons: 1'b0: Engine will NOT be resetting. 1'b1: Engine will be resetting (FLR/RC6 Enter or Soft Reset). Preparation for VEBox reset (vecsunit).</p>	Default Value:	0b	Project:	BDW	Access:	R/W
Default Value:	0b							
Project:	BDW							
Access:	R/W							
	9	<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Go Protocol Request Reasons: 1'b0: Engine will NOT be resetting. 1'b1: Engine will be resetting (FLR/RC6 Enter or Soft Reset). Preparation for Media0 reset (vcs0unit).</p>	Default Value:	0b	Project:	BDW	Access:	R/W
Default Value:	0b							
Project:	BDW							
Access:	R/W							
	8	<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Go Protocol Request Reasons: 1'b0: Engine will NOT be resetting. 1'b1: Engine will be resetting (FLR/RC6 Enter or Soft Reset). Preparation for Render reset (csunit).</p>	Default Value:	0b	Project:	BDW	Access:	R/W
Default Value:	0b							
Project:	BDW							
Access:	R/W							
	7	Reserved						

GO_GAM_REQ - Go Protocol GAM Request

		GO_PROTOCOL_GAM_REQUEST6				
	6	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Default Value:</td><td style="padding: 2px; text-align: right;">0b</td></tr> <tr> <td style="padding: 2px;">Access:</td><td style="padding: 2px; text-align: right;">R/W</td></tr> </table> <p>GPM to GAM Go Protocol Request. 0: No graphic cycles allowed to memory (default). 1: Allow graphic cycles to memory. Controls Wi-Di Cycles (winunit). GPM currently only ever sends the same GO request for all agents; either all is go=0, or all is go=1.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
	5	Reserved				
	4	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Default Value:</td><td style="padding: 2px; text-align: right;">0b</td></tr> <tr> <td style="padding: 2px;">Access:</td><td style="padding: 2px; text-align: right;">R/W</td></tr> </table> <p>GPM to GAM Go Protocol Request. 0: No graphic cycles allowed to memory (default). 1: Allow graphic cycles to memory. Controls Blitter Cycles (bcsunit). GPM currently only ever sends the same GO request for all agents; either all is go=0, or all is go=1.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
	3	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Default Value:</td><td style="padding: 2px; text-align: right;">0b</td></tr> <tr> <td style="padding: 2px;">Access:</td><td style="padding: 2px; text-align: right;">R/W</td></tr> </table> <p>GPM to GAM Go Protocol Request. 0: No graphic cycles allowed to memory (default). 1: Allow graphic cycles to memory. Controls VEBox Cycles (vecsunit). GPM currently only ever sends the same GO request for all agents; either all is go=0, or all is go=1.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
	2	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Default Value:</td><td style="padding: 2px; text-align: right;">0b</td></tr> <tr> <td style="padding: 2px;">Access:</td><td style="padding: 2px; text-align: right;">R/W</td></tr> </table> <p>GPM to GAM Go Protocol Request. 0: No graphic cycles allowed to memory (default). 1: Allow graphic cycles to memory. Controls Media1 Cycles (vcs1unit). GPM currently only ever sends the same GO request for all agents; either all is go=0, or all is go=1.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					

GO_GAM_REQ - Go Protocol GAM Request

		GO_PROTOCOL_GAM_REQUEST1				
	1	<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>GPM to GAM Go Protocol Request. 0: No graphic cycles allowed to memory (default). 1: Allow graphic cycles to memory. Controls Media0 Cycles (vcs0unit). GPM currently only ever sends the same GO request for all agents; either all is go=0, or all is go=1.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
	0	<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>GPM to GAM Go Protocol Request. 0: No graphic cycles allowed to memory (default). 1: Allow graphic cycles to memory. Controls Render Cycles (csunit). GPM currently only ever sends the same GO request for all agents; either all is go=0, or all is go=1.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					

GPA to HPA Translation Request

GPA2HPAR - GPA to HPA Translation Request						
DWord	Bit	Description				
0	31:16	Mask Bits <table border="1"> <tr> <td>Default Value:</td> <td>0000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Mask Bits act as Write Enables for the bits[15:0] of this register.</p>	Default Value:	0000h	Access:	RO
Default Value:	0000h					
Access:	RO					
	15	GPA to HPA Translation Request 15 <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>For Future Use. This bit is self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
	14	GPA to HPA Translation Request 14 <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>For Future Use. This bit is self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
	13	GPA to HPA Translation Request 13 <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>For Future Use. This bit is self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
	12	GPA to HPA Translation Request 12 <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>For Future Use. This bit is self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					

GPA2HPAR - GPA to HPA Translation Request

	11	GPA to HPA Translation Request 11
		Default Value: 0b Access: R/W
		For Future Use. This bit is self clear.
	10	GPA to HPA Translation Request 10
		Default Value: 0b Access: R/W
		For Future Use. This bit is self clear.
	9	GPA to HPA Translation Request 9
		Default Value: 0b Access: R/W
		For Future Use. This bit is self clear.
	8	GPA to HPA Translation Request 8
		Default Value: 0b Access: R/W
		For Future Use. This bit is self clear.
	7	GPA to HPA Translation Request 7
		Default Value: 0b Access: R/W
		For Future Use. This bit is self clear.
	6	GPA to HPA Translation Request 6
		Default Value: 0b Access: R/W
		For Future Use. This bit is self clear.
	5	GPA to HPA Translation Request 5
		Default Value: 0b Access: R/W
		For Future Use. This bit is self clear.

GPA2HPAR - GPA to HPA Translation Request

		GPA to HPA Translation Request 4				
	4	<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>For Future Use. This bit is self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
	3	GPA to HPA Translation Request 3 <table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>For Future Use. This bit is self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
	2	GPA to HPA Translation Request 2 <table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Bit[2]: A request for GPA to HPA translation. Note that GPA register should have been written prior to sending the message for the translation. Mask bit[18] needs to be enabled to program the register. This bit is self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
	1	GPA to HPA Translation Request 1 <table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>For Future Use. This bit is self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
	0	GPA to HPA Translation Request 0 <table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>For Future Use. This bit is self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					

GPA value for GPA to HPA Translation

GPA2HPAV - GPA value for GPA to HPA Translation						
DWord	Bit	Description				
0	31:0	<p>GPA value for GPA to HPA Translation</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>The GPA value of the page that requires the GPA=>HPA translation bits[39:12] map to [28:1] of the register.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

GPGPU Context Restore Request To TDL

GPGPU_CTX_RESTORE - GPGPU Context Restore Request To TDL	
Register Space:	MMIO: 0/2/0
Project:	BDW
Default Value:	0x00000000
Access:	WO
Size (in bits):	32
Address:	0E4CCh
Name:	GPGPU Context Restore Request To TDL Slice 0 SubSlice 0
ShortName:	GPGPU_CTX_RESTORE_S0_SS0
Valid Projects:	[BDW]
Address:	0E5CCh
Name:	GPGPU Context Restore Request To TDL Slice 0 SubSlice 1
ShortName:	GPGPU_CTX_RESTORE_S0_SS1
Valid Projects:	[BDW]
Address:	0E6CCh
Name:	GPGPU Context Restore Request To TDL Slice 0 SubSlice 2
ShortName:	GPGPU_CTX_RESTORE_S0_SS2
Valid Projects:	[BDW]
Address:	0E4DCh
Name:	GPGPU Context Restore Request To TDL Slice 1 SubSlice 0
ShortName:	GPGPU_CTX_RESTORE_S1_SS0
Valid Projects:	[BDW]
Address:	0E5DCh
Name:	GPGPU Context Restore Request To TDL Slice 1 SubSlice 1
ShortName:	GPGPU_CTX_RESTORE_S1_SS1
Valid Projects:	[BDW]
Address:	0E6DCh
Name:	GPGPU Context Restore Request To TDL Slice 1 SubSlice 2
ShortName:	GPGPU_CTX_RESTORE_S1_SS2
Valid Projects:	[BDW]
Address:	0E4ECh
Name:	GPGPU Context Restore Request To TDL Slice 2 SubSlice 0
ShortName:	GPGPU_CTX_RESTORE_S2_SS0
Valid Projects:	[BDW]
Address:	0E5ECh

GPGPU_CTX_RESTORE - GPGPU Context Restore Request To TDL

Name: GPGPU Context Restore Request To TDL Slice 2 SubSlice 1

ShortName: GPGPU_CTX_RESTORE_S2_SS1

Valid Projects: [BDW]

Address: 0E6ECh

Name: GPGPU Context Restore Request To TDL Slice 2 SubSlice 2

ShortName: GPGPU_CTX_RESTORE_S2_SS2

Valid Projects: [BDW]

DWord	Bit	Description	
0	31:0	Reserved Format:	MBZ

GPGPU Context Save Request To TDL

GPGPU_CTX_SAVE - GPGPU Context Save Request To TDL			
Register Space:	MMIO	0/2/0	
Project:	BDW		
Default Value:	0x00000000		
Access:	WO		
Size (in bits):	32		
Address:	0E4D8h		
Valid Projects:	[BDW]		
DWord	Bit	Description	
0	31:0	Reserved	
		Format:	MBZ

GPGPU Dispatch Dimension X

GPGPU_DISPATCHDIMX - GPGPU Dispatch Dimension X												
DWord	Bit	Description										
0	31:0	<p>Dispatch Dimension X</p> <table border="1"> <tr> <td>Format:</td> <td>U32</td> </tr> <tr> <td colspan="2">The number of thread groups to be dispatched in the X dimension (max x + 1).</td></tr> <tr> <th>Value</th><th>Name</th><th>Project</th></tr> <tr> <td>0, FFFFFFFFh</td><td></td><td>BDW</td></tr> </table>	Format:	U32	The number of thread groups to be dispatched in the X dimension (max x + 1).		Value	Name	Project	0, FFFFFFFFh		BDW
Format:	U32											
The number of thread groups to be dispatched in the X dimension (max x + 1).												
Value	Name	Project										
0, FFFFFFFFh		BDW										

GPGPU Dispatch Dimension Y

GPGPU_DISPATCHDIMY - GPGPU Dispatch Dimension Y												
Register Space: MMIO: 0/2/0 Project: BDW Source: RenderCS Default Value: 0x00000000 Access: R/W Size (in bits): 32												
Address: 02504h												
DWord	Bit	Description										
0	31:0	Dispatch Dimension Y <table border="1"> <tr> <td>Format:</td> <td>U32</td> </tr> <tr> <td colspan="2">The number of thread groups to be dispatched in the Y dimension (max y + 1)</td></tr> <tr> <th>Value</th><th>Name</th><th>Project</th></tr> <tr> <td>0, FFFFFFFFh</td><td></td><td>BDW</td></tr> </table>	Format:	U32	The number of thread groups to be dispatched in the Y dimension (max y + 1)		Value	Name	Project	0, FFFFFFFFh		BDW
Format:	U32											
The number of thread groups to be dispatched in the Y dimension (max y + 1)												
Value	Name	Project										
0, FFFFFFFFh		BDW										

GPGPU Dispatch Dimension Z

GPGPU_DISPATCHDIMZ - GPGPU Dispatch DimensionZ												
Register Space: MMIO: 0/2/0												
Project: BDW												
Source: RenderCS												
Default Value: 0x00000000												
Access: R/W												
Size (in bits): 32												
Address: 02508h												
DWord	Bit	Description										
0	31:0	<p>Dispatch Dimension Z</p> <table border="1"> <tr> <td>Format:</td> <td>U32</td> </tr> <tr> <td colspan="2">The number of thread groups to be dispatched in the Zdimension (max Z + 1)</td></tr> <tr> <th>Value</th><th>Name</th><th>Project</th></tr> <tr> <td>0, FFFFFFFFh</td><td></td><td>BDW</td></tr> </table>	Format:	U32	The number of thread groups to be dispatched in the Zdimension (max Z + 1)		Value	Name	Project	0, FFFFFFFFh		BDW
Format:	U32											
The number of thread groups to be dispatched in the Zdimension (max Z + 1)												
Value	Name	Project										
0, FFFFFFFFh		BDW										

GPIO_CTL

GPIO_CTL			
Register Space:	MMIO: 0/2/0		
Project:	DevLPT		
Default Value:	0x00000808		
Access:	R/W		
Size (in bits):	32		
Address:	C5010h-C5013h		
Name:	GPIO Control 0		
ShortName:	GPIO_CTL_0		
Valid Projects:	[DevLPT:H]		
Power:	Always on		
Reset:	soft		
Address:	C501Ch-C501Fh		
Name:	GPIO Control 3		
ShortName:	GPIO_CTL_3		
Power:	Always on		
Reset:	soft		
Address:	C5020h-C5023h		
Name:	GPIO Control 4		
ShortName:	GPIO_CTL_4		
Power:	Always on		
Reset:	soft		
Address:	C5024h-C5027h		
Name:	GPIO Control 5		
ShortName:	GPIO_CTL_5		
Valid Projects:	[DevLPT:H]		
Power:	Always on		
Reset:	soft		
The register controls a pair of pins that can be used for general purpose control, but usually is designated for specific functions according to the requirements of the device and the system that the device is in. Each pin of the two pin pair is designated as a clock or data for descriptive purposes. See the table at the beginning of this section to determine which pins/registers are supported and their intended functions. Board design variations are possible and would affect the usage of these pins. There are multiple instances of this register to support each of the GPIO pin pairs.			
DWord	Bit	Description	
0	31:13	Reserved	
		Format:	MBZ

GPIO_CTL

GPIO_CTL														
<p>12 GPIO Data In</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 33%;">Default Value:</td> <td colspan="2">Ub Undefined (read only depends on I/O pin)</td> </tr> <tr> <td>Access:</td> <td colspan="2">RO</td> </tr> </table> <p>This is the value that is sampled on the GPIO_Data pin as an input. This bit is undefined at reset.</p>			Default Value:	Ub Undefined (read only depends on I/O pin)		Access:	RO							
Default Value:	Ub Undefined (read only depends on I/O pin)													
Access:	RO													
<p>11 GPIO Data Value</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 33%;">Default Value:</td> <td colspan="2">1b</td> </tr> <tr> <td>Access:</td> <td colspan="2">R/W</td> </tr> </table> <p>This is the value that should be place on the GPIO Data pin as an output. This value is only written into the register if GPIO DATA MASK is also asserted. The value will appear on the pin if this data value is actually written to this register and the GPIO Data DIRECTION VALUE contains a value that will configure the pin as an output. The default of '1' mimics the I2C external pull-ups.</p>			Default Value:	1b		Access:	R/W							
Default Value:	1b													
Access:	R/W													
<p>10 GPIO Data Mask</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 33%;">Access:</td> <td colspan="2">WO</td> </tr> </table> <p>This is a mask bit to determine whether the GPIO DATA VALUE bit should be written into the register. This value is not stored and when read returns 0.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 33%;">Value</th> <th style="width: 33%;">Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>No Write</td> <td>Do NOT write GPIO Data Value bit</td> </tr> <tr> <td>1b</td> <td>Write</td> <td>Write GPIO Data Value bit.</td> </tr> </tbody> </table>			Access:	WO		Value	Name	Description	0b	No Write	Do NOT write GPIO Data Value bit	1b	Write	Write GPIO Data Value bit.
Access:	WO													
Value	Name	Description												
0b	No Write	Do NOT write GPIO Data Value bit												
1b	Write	Write GPIO Data Value bit.												
<p>9 GPIO Data Direction Value</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 33%;">Access:</td> <td colspan="2">R/W</td> </tr> </table> <p>This is the value that should be used to define the output enable of the GPIO Data pin. This value is only written into the register if GPIO Data DIRECTION MASK is also asserted. The value that will appear on the pin is defined by what is in the register for the GPIO DATA VALUE bit.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 33%;">Value</th> <th style="width: 33%;">Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Input</td> <td>Pin is configured as an input</td> </tr> <tr> <td>1b</td> <td>Output</td> <td>Pin is configured as an output</td> </tr> </tbody> </table>			Access:	R/W		Value	Name	Description	0b	Input	Pin is configured as an input	1b	Output	Pin is configured as an output
Access:	R/W													
Value	Name	Description												
0b	Input	Pin is configured as an input												
1b	Output	Pin is configured as an output												
<p>8 GPIO Data Direction Mask</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 33%;">Access:</td> <td colspan="2">WO</td> </tr> </table> <p>This is a mask bit to determine whether the GPIO Data DIRECTION VALUE bit should be written into the register. This value is not stored and when read always returns 0.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 33%;">Value</th> <th style="width: 33%;">Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>No Write</td> <td>Do NOT write GPIO Data Direction Value bit</td> </tr> <tr> <td>1b</td> <td>Write</td> <td>Write GPIO Data Direction Value bit</td> </tr> </tbody> </table>			Access:	WO		Value	Name	Description	0b	No Write	Do NOT write GPIO Data Direction Value bit	1b	Write	Write GPIO Data Direction Value bit
Access:	WO													
Value	Name	Description												
0b	No Write	Do NOT write GPIO Data Direction Value bit												
1b	Write	Write GPIO Data Direction Value bit												
<p>7:5 Reserved</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 33%;">Format:</td> <td colspan="2">MBZ</td> </tr> </table>			Format:	MBZ										
Format:	MBZ													

GPIO_CTL												
	4	GPIO Clock Data In										
		Default Value:	Ub Undefined (read only depends on I/O pin)									
		Access:	RO									
		This is the value that is sampled on the GPIO Clock pin as an input. This bit is undefined at reset.										
	3	GPIO Clock Data Value										
		Default Value:	1b									
		Access:	R/W									
		This is the value that should be place on the GPIO Clk pin as an output. This value is only written into the register if GPIO Clock DATA MASK is also asserted. The value will appear on the pin if this data value is actually written to this register and the GPIO Clock DIRECTION VALUE contains a value that will configure the pin as an output. The default of '1' mimics the I2C external pull-ups.										
	2	GPIO Clock Data Mask										
		Access:	WO									
		This is a mask bit to determine whether the GPIO Clock DATA VALUE bit should be written into the register. This value is not stored and when read always returns 0.										
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>No Write</td><td>Do NOT write GPIO Clock Data Value bit</td></tr> <tr> <td>1b</td><td>Write</td><td>Write GPIO Clock Data Value bit</td></tr> </tbody> </table>		Value	Name	Description	0b	No Write	Do NOT write GPIO Clock Data Value bit	1b	Write	Write GPIO Clock Data Value bit
Value	Name	Description										
0b	No Write	Do NOT write GPIO Clock Data Value bit										
1b	Write	Write GPIO Clock Data Value bit										
	1	GPIO Clock Direction Value										
		Access:	R/W									
		This is the value that should be used to define the output enable of the GPIO Clock pin. This value is only written into the register if GPIO Clock DIRECTION MASK is also asserted. The value that will appear on the pin is defined by what is in the register for the GPIO Clock DATA VALUE bit.										
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Input</td><td>Pin is configured as an input and the output driver is set to tri-state</td></tr> <tr> <td>1b</td><td>Output</td><td>Pin is configured as an output</td></tr> </tbody> </table>		Value	Name	Description	0b	Input	Pin is configured as an input and the output driver is set to tri-state	1b	Output	Pin is configured as an output
Value	Name	Description										
0b	Input	Pin is configured as an input and the output driver is set to tri-state										
1b	Output	Pin is configured as an output										
	0	GPIO Clock Direction Mask										
		Access:	WO									
		This is a mask bit to determine whether the GPIO Clock DIRECTION VALUE bit should be written into the register. This value is not stored and when read returns 0.										
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>No Update</td><td>Do NOT write GPIO Clock Direction Value bit</td></tr> <tr> <td>1b</td><td>Update</td><td>Write GPIO Clock Direction Value bit</td></tr> </tbody> </table>		Value	Name	Description	0b	No Update	Do NOT write GPIO Clock Direction Value bit	1b	Update	Write GPIO Clock Direction Value bit
Value	Name	Description										
0b	No Update	Do NOT write GPIO Clock Direction Value bit										
1b	Update	Write GPIO Clock Direction Value bit										

GPM Control Register in Bus Reset Domain with Lock bit

MISC_CTRL0 - GPM Control Register in Bus Reset Domain with Lock bit

Register Space: MMIO: 0/2/0

Project: BDW

Default Value: 0x05200000

Size (in bits): 32

Address: 0A180h

Lock bit ECOLOCK applies to all RW/L fields this register.

These bits are not reset on FLR (device reset).

DWord	Bit	Description	
0	31	Lock Bit	Access: R/W Lock
	30	Force CPD IA as Non-IA	Access: R/W Lock
		CPD IA = No clock changes for GT. CPD Non-IA = Clock is changing for GT. 1 = Treat a CPD IA as a CPD Non-IA during the CPD flows (as if clocks are changing). 0 = Treat a CPD IA normally (clocks are not changing) (default).	
	29	Reserved	
	28	CPD Core Status Register Access Enable	Access: R/W Lock
		0 = No Core Status Register reads or writes during CPD flow (including slice shutdown) (default). 1 = Core Status Register reads and writes occur during CPD enter/exit flows (including slice shutdown).	
	27	Reserved	
	26	RC6 FIFO Block Type When Requesting FIFO Block	Default Value: 1b Access: R/W Lock
		[26] = 0 RC6 FIFO Block Type is 'block-and-hold' (similar to CPD). MGSR is able to discern if fifo block is due to RC6 or CPD. When fifo is blocked, wait for it to become unblocked for read return data (cpd).	
		[26] = 1 RC6 FIFO Block Type is 'block-and-return-0s'. Indication to MGSR that we are doing a fifo block due to RC6 and not CPD. When fifo is blocked, DO NOT wait for it to become unblocked. Instead, immediately return all 0s (rcenter). PCU returns all 0s for a read when this bit is set and the fifo is blocked (default).	

MISC_CTRL0 - GPM Control Register in Bus Reset Domain with Lock bit

	25	CPD GAM GO Messaging Enable		
		<table border="1"> <tr> <td>Access:</td><td>R/W Lock</td></tr> </table> <p>0 = No GO Messages to GAM during CPD enter/exit flows (including slice shutdown) (default). 1 = GO Messages to GAM will occur during CPD enter/exit flows (including slice shutdown).</p>	Access:	R/W Lock
Access:	R/W Lock			
	Programmable Default for Software Render C-State Control Wish upon FLR			
		<table border="1"> <tr> <td>Default Value:</td><td>100b</td></tr> </table>	Default Value:	100b
Default Value:	100b			
		<table border="1"> <tr> <td>Access:</td><td>R/W Lock</td></tr> </table> <p>[24:22] = Corresponds to Software Render C-State Control (A094[18:16]). Default is 100b (RC6). 000b: RCO (this does not control clock gating). 001b: Reserved. 010b: RC1e (this does not control clock gating). 011b: Reserved. 100b: RC6 (default). 101b: Deep RC6. 110b: Deepest RC6. 111b: Reserved.</p>	Access:	R/W Lock
Access:	R/W Lock			
	21	Include idleness of all agents in RC6 qualification		
		<table border="1"> <tr> <td>Default Value:</td><td>1b</td></tr> </table>	Default Value:	1b
Default Value:	1b			
		<table border="1"> <tr> <td>Access:</td><td>R/W Lock</td></tr> </table> <p>[21] = 1 *CS Idleness, as well as CP/MBC/DT Idleness required for RC6 entry (default). [21] = 0 Only *CS Idleness required for RC6 entry.</p>	Access:	R/W Lock
Access:	R/W Lock			
	20	Reserved		
	19	Reserved		
	18:4	Reserved		
		<table border="1"> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Register bits that have no connection to design. Used to enable/disable changes to the design that were put in during the ECO process. pmcr_eco_bits[31:0].</p>	Access:	RO
Access:	RO			
	3:0	Reserved		
		<table border="1"> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Reserved.</p>	Access:	RO
Access:	RO			

GPU_Ticks_Counter

GPU_TICKS - GPU_Ticks_Counter						
DWord	Bit	Description				
0	31:0	<p>Considerations</p> <table border="1"> <tr> <td>Format:</td> <td>U32</td> </tr> <tr> <td colspan="2">This 32-bit field returns bits 31:0 of the GPU tick counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</td></tr> </table>	Format:	U32	This 32-bit field returns bits 31:0 of the GPU tick counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.	
Format:	U32					
This 32-bit field returns bits 31:0 of the GPU tick counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.						
Reading this register returns the live value of the GPU ticks counter that is sampled and included in the performance counter report header.						

Graphics Device Reset Control

GDRST - Graphics Device Reset Control								
DWord	Bit	Description						
0	31:8	<p>Reserved</p> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>RO</td></tr> <tr> <td colspan="2">Reserved</td></tr> </table>	Project:	BDW	Access:	RO	Reserved	
Project:	BDW							
Access:	RO							
Reserved								
	7	<p>Initiate Graphics Media1 soft reset</p> <table border="1"> <tr> <td>Access:</td><td>R/W Set</td></tr> </table> <p>Graphics Media 1 Soft-Reset Control: '1' : Initiate a graphics Vebox domain reset. - Cleared by CP once the reset is complete '0' : N/A - Once set, clearing of this bit has no effect on CP. Only CP can reset this bit. Note: This is a non-posted register.</p>	Access:	R/W Set				
Access:	R/W Set							
	6	<p>Initiate Graphics WIDI soft reset</p> <table border="1"> <tr> <td>Access:</td><td>R/W Set</td></tr> </table> <p>Graphics WIDI Soft-Reset Control (cwrst_b): '1' : Initiate a graphics Vebox domain reset. - Cleared by CP once the reset is complete '0' : N/A - Once set, clearing of this bit has no effect on CP. Only CP can reset this bit. Note: This is a non-posted register.</p>	Access:	R/W Set				
Access:	R/W Set							
	5	Reserved						
	4	<p>Initiate Graphics Vebox Soft Reset</p> <table border="1"> <tr> <td>Access:</td><td>R/W Set</td></tr> </table> <p>Graphics VEbox Soft-Reset Control: '1' : Initiate a graphics Vebox domain reset. - Cleared by CP once the reset is complete '0' : N/A - Once set, clearing of this bit has no effect on CP. Only CP can reset this bit. Note: This is a non-posted register.</p>	Access:	R/W Set				
Access:	R/W Set							

GDRST - Graphics Device Reset Control

	3	Initiate Graphics Blitter Soft Reset		
		<table border="1"> <tr> <td>Access:</td><td>R/W Set</td></tr> </table> <p>Graphics Blitter Soft-Reset Control: '1' : Initiate a graphics blitter domain reset. - Cleared by CP once the reset is complete '0' : N/A - Once set, clearing of this bit has no effect on CP. Only CP can reset this bit. Note: This is a non-posted register.</p>	Access:	R/W Set
Access:	R/W Set			
	2	Initiate Graphics Media Soft Reset		
		<table border="1"> <tr> <td>Access:</td><td>R/W Set</td></tr> </table> <p>Graphics Media Soft-Reset Control: '1' : Initiate a graphics media 0 domain reset. - Cleared by CP once the reset is complete '0' : N/A - Once set, clearing of this bit has no effect on CP. Only CP can reset this bit. Note: This is a non-posted register.</p>	Access:	R/W Set
Access:	R/W Set			
	1	Initiate Graphics Render Soft Reset		
		<table border="1"> <tr> <td>Access:</td><td>R/W Set</td></tr> </table> <p>Graphics Render Soft-Reset Control: '1' : Initiate a graphics render domain reset. - Cleared by CP once the reset is complete '0' : N/A - Once set, clearing of this bit has no effect on CP. Only CP can reset this bit. Note: This is a non-posted register.</p>	Access:	R/W Set
Access:	R/W Set			
	0	Initiate Graphics Full Soft Reset		
		<table border="1"> <tr> <td>Access:</td><td>R/W Set</td></tr> </table> <p>Graphics Full Soft-Reset Control: '1' : Initiate a full graphics reset (i.e., graphics render, media, and blitter reset). - Cleared by CP once the reset is complete '0' : N/A - Once set, clearing of this bit has no effect on CP. Only CP can reset this bit. Note: This is a non-posted register.</p>	Access:	R/W Set
Access:	R/W Set			

Graphics Memory Fence Table Register

FENCE - Graphics Memory Fence Table Register	
Register Space:	MMIO: 0/2/0
Project:	BDW
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Trusted Type:	1
Address:	100000h-100007h
Name:	FENCE_0
Valid Projects:	BDW
Address:	100008h-10000Fh
Name:	FENCE_1
Valid Projects:	BDW
Address:	100010h-100017h
Name:	FENCE_2
Valid Projects:	BDW
Address:	100018h-10001Fh
Name:	FENCE_3
Valid Projects:	BDW
Address:	100020h-100027h
Name:	FENCE_4
Valid Projects:	BDW
Address:	100028h-10002Fh
Name:	FENCE_5
Valid Projects:	BDW
Address:	100030h-100037h
Name:	FENCE_6
Valid Projects:	BDW
Address:	100038h-10003Fh
Name:	FENCE_7
Valid Projects:	BDW
Address:	100040h-100047h
Name:	FENCE_8
Valid Projects:	BDW
Address:	100048h-10004Fh

FENCE - Graphics Memory Fence Table Register	
Name:	FENCE_9
Valid Projects:	BDW
Address:	100050h-100057h
Name:	FENCE_10
Valid Projects:	BDW
Address:	100058h-10005Fh
Name:	FENCE_11
Valid Projects:	BDW
Address:	100060h-100067h
Name:	FENCE_12
Valid Projects:	BDW
Address:	100068h-10006Fh
Name:	FENCE_13
Valid Projects:	BDW
Address:	100070h-100077h
Name:	FENCE_14
Valid Projects:	BDW
Address:	100078h-10007Fh
Name:	FENCE_15
Valid Projects:	BDW
Address:	100080h-100087h
Name:	FENCE_16
Valid Projects:	BDW
Address:	100088h-10008Fh
Name:	FENCE_17
Valid Projects:	BDW
Address:	100090h-100097h
Name:	FENCE_18
Valid Projects:	BDW
Address:	100098h-10009Fh
Name:	FENCE_19
Valid Projects:	BDW
Address:	1000A0h-1000A7h
Name:	FENCE_20
Valid Projects:	BDW

FENCE - Graphics Memory Fence Table Register

Address: 1000A8h-1000AFh

Name: FENCE_21

Valid Projects: BDW

Address: 1000B0h-1000B7h

Name: FENCE_22

Valid Projects: BDW

Address: 1000B8h-1000BFh

Name: FENCE_23

Valid Projects: BDW

Address: 1000C0h-1000C7h

Name: FENCE_24

Valid Projects: BDW

Address: 1000C8h-1000CFh

Name: FENCE_25

Valid Projects: BDW

Address: 1000D0h-1000D7h

Name: FENCE_26

Valid Projects: BDW

Address: 1000D8h-1000DFh

Name: FENCE_27

Valid Projects: BDW

Address: 1000E0h-1000E7h

Name: FENCE_28

Valid Projects: BDW

Address: 1000E8h-1000EFh

Name: FENCE_29

Valid Projects: BDW

Address: 1000F0h-1000F7h

Name: FENCE_30

Valid Projects: BDW

Address: 1000F8h-1000FFh

Name: FENCE_31

Valid Projects: BDW

The graphics device performs address translation from linear space to tiled space for a CPU access to graphics memory (See Memory Interface Functions chapter for information on these memory layouts) using the fence registers. Note that the fence registers are used only for CPU accesses to gfx memory. Graphics

FENCE - Graphics Memory Fence Table Register

rendering/display pipelines use Per Surface Tiling (PST) parameters (found in SURFACE_STATE - see the Sampling Engine chapter) to access tiled gfx memory.

The intent of tiling is to locate graphics data that are close (in X and Y surface axes) in one physical memory page while still locating some amount of line oriented data sequentially in memory for display efficiency. All 3D rendering is done such that the QWords of any one span are all located in the same memory page, improving rendering performance. Applications view surfaces as linear, hence when the cpu access a surface that is tiled, the gfx hardware must perform linear to tiled address conversion and access the correct physical memory location(s) to get the data.

Tiled memory is supported for rendering and display surfaces located in graphics memory. A tiled memory surface is a surface that has a width and height that are subsets of the tiled region's pitch and height. The device maintains the constants required by the memory interface to perform the address translations. Each tiled region can have a different pitch and size. The CPU-memory interface needs the surface pitch and tile height to perform the address translation. It uses the GMAddr (PCI-BAR) offset address to compare with the fence start and end address, to determine if the rendering surface is tiled. The tiled address is generated based on the tile orientation determined from the matching fence register. Fence ranges are at least 4 KB aligned. Note that the fence registers are used only for CPU accesses to graphics memory.

A Tile represents 4 KB of memory. Tile height is 8 rows for X major tiles and 32 rows for Y major tiles. Tile Pitch is 512Bs for X major tiles and 128Bs for Y major tiles. The surface pitch is programmed in 128B units such that the pitch is an integer multiple of "tile pitch".

Engine restrictions on tile surface usage are detailed in Surface Placement Restrictions (Memory Interface Functions). Note that X major tiles can be used for Sampler, Color, Depth, motion compensation references and motion compensation destination, Display, Overlay, GDI Blt source and destination surfaces. Y major tiles can be used for Sampler, depth, color and motion compensation assuming they do not need to be displayed. GDI Blt operations, overlay and display cannot use Tiled Y orientations.

A "PST" graphics surface that will also be accessed via fence needs its base address to be tile row aligned.

Hardware handles the flushing of any pending cycles when software changes the fence upper/lower bounds.

Fence Table Registers occupy the address range specified above. Each Fence Table Register has the following format.

FENCE registers are not reset by a graphics reset. They will maintain their values unless a full reset is performed.

DWord	Bit	Description				
0	63:44	<p>Fence Upper Bound</p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>GraphicsAddress[31:12]</td></tr> </table> <p>Bits 31:12 of the ending Graphics Address of the fence region. Fence regions must be aligned to a 4KB page. This address represents the last 4KB page of the fence region (Upper Bound is included in the fence region).</p> <p>Graphics Address is the offset within GMADR space.</p>	Project:	All	Format:	GraphicsAddress[31:12]
Project:	All					
Format:	GraphicsAddress[31:12]					
<p>Reserved</p> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	BDW	Format:	MBZ		
Project:	BDW					
Format:	MBZ					

FENCE - Graphics Memory Fence Table Register

	42:32	<p>Fence Pitch</p> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>U10-1 Width in 128 bytes</td></tr> </table> <p>This field specifies the width (pitch) of the fence region in multiple of "tile width". For Tile X this field must be programmed to a multiple of 512B ("003" is the minimum value) and for Tile Y this field must be programmed to a multiple of 128B ("000" is the minimum value).</p> <p>000h = 128B 001h = 256B ... 3FFh = 128KB ... 7FFh = 256KB</p>	Project:	BDW	Format:	U10-1 Width in 128 bytes										
Project:	BDW															
Format:	U10-1 Width in 128 bytes															
	31:12	<p>Fence Lower Bound</p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>GraphicsAddress[31:12]</td></tr> </table> <p>Bits 31:12 of the starting Graphics Address of the fence region. Fence regions must be aligned to 4KB. This address represents the first 4KB page of the fence region (Lowe Bound is included in the fence region).</p> <p>Graphics Address is the offset within GMADR space.</p>	Project:	All	Format:	GraphicsAddress[31:12]										
Project:	All															
Format:	GraphicsAddress[31:12]															
	11:2	<p>Reserved</p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	All	Format:	MBZ										
Project:	All															
Format:	MBZ															
	1	<p>Tile Walk</p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> </table> <p>This field specifies the spatial ordering of QWords within tiles.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th><th>Project</th></tr> </thead> <tbody> <tr> <td>0h</td><td>MI_TILE_XMAJOR</td><td>Consecutive SWords (32 Bytes) sequenced in the X direction</td><td>All</td></tr> <tr> <td>1h</td><td>MI_TILE_YMAJOR</td><td>Consecutive OWords (16 Bytes) sequenced in the Y direction</td><td>All</td></tr> </tbody> </table>	Project:	All	Value	Name	Description	Project	0h	MI_TILE_XMAJOR	Consecutive SWords (32 Bytes) sequenced in the X direction	All	1h	MI_TILE_YMAJOR	Consecutive OWords (16 Bytes) sequenced in the Y direction	All
Project:	All															
Value	Name	Description	Project													
0h	MI_TILE_XMAJOR	Consecutive SWords (32 Bytes) sequenced in the X direction	All													
1h	MI_TILE_YMAJOR	Consecutive OWords (16 Bytes) sequenced in the Y direction	All													
	0	<p>Fence Valid</p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>MI_FenceValid</td></tr> </table> <p>This field specifies whether or not this fence register defines a fence region.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Project</th></tr> </thead> <tbody> <tr> <td>0h</td><td>MI_FENCE_INVALID</td><td>All</td></tr> <tr> <td>1h</td><td>MI_FENCE_VALID</td><td>All</td></tr> </tbody> </table>	Project:	All	Format:	MI_FenceValid	Value	Name	Project	0h	MI_FENCE_INVALID	All	1h	MI_FENCE_VALID	All	
Project:	All															
Format:	MI_FenceValid															
Value	Name	Project														
0h	MI_FENCE_INVALID	All														
1h	MI_FENCE_VALID	All														

Graphics Memory Range Address

GMADR_0_2_0_PCI - Graphics Memory Range Address						
DWord	Bit	Description				
0	63:39	<p>Reserved for Memory Base Address</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000000000000000000000000000b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>FLR Resettable Must be set to 0 since addressing above 512GB is not supported.</p>	Default Value:	00000000000000000000000000000000b	Access:	R/W
Default Value:	00000000000000000000000000000000b					
Access:	R/W					
0	38:32	<p>Memory Base Address</p> <table border="1"> <tr> <td>Default Value:</td> <td>0000000b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>FLR Resettable Set by the OS, these bits correspond to address signals [38:32].</p>	Default Value:	0000000b	Access:	R/W
Default Value:	0000000b					
Access:	R/W					
0	31	<p>4096 MB Address Mask</p> <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W Lock</td> </tr> </table> <p>FLR Resettable This bit is either part of the Memory Base Address (R/W) or part of the Address Mask (RO) depending on the value of MSAC.APSZ. RO and forced to 0 when MSAC.APSZ >= 4096MB. (i.e. MSAC.APSZ[4]=1)</p>	Default Value:	0b	Access:	R/W Lock
Default Value:	0b					
Access:	R/W Lock					
0	30	<p>2048 MB Address Mask</p> <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W Lock</td> </tr> </table> <p>FLR Resettable This bit is either part of the Memory Base Address (R/W) or part of the Address Mask (RO) depending on the value of MSAC.APSZ. RO and forced to 0 when MSAC.APSZ >= 2048MB. (i.e. MSAC.APSZ[3]=1)</p>	Default Value:	0b	Access:	R/W Lock
Default Value:	0b					
Access:	R/W Lock					
0	29	<p>1024 MB Address Mask</p> <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W Lock</td> </tr> </table> <p>FLR Resettable This bit is either part of the Memory Base Address (R/W) or part of the Address Mask (RO) depending on the value of MSAC.APSZ. RO and forced to 0 when MSAC.APSZ >= 1024MB. (i.e. MSAC.APSZ[2]=1)</p>	Default Value:	0b	Access:	R/W Lock
Default Value:	0b					
Access:	R/W Lock					

GMADR_0_2_0_PCI - Graphics Memory Range Address

	28	512MB Address Mask		
		Default Value:	0b	
		Access:	R/W Lock	
<p>FLR Resettable This bit is either part of the Memory Base Address (R/W) or part of the Address Mask (RO) depending on the value of MSAC.APSZ. RO and forced to 0 when MSAC.APSZ >= 512MB. (i.e. MSAC.APSZ[1]=1)</p>				
	27	256 MB Address Mask		
		Default Value:	0b	
		Access:	R/W Lock	
<p>FLR Resettable This bit is either part of the Memory Base Address (R/W) or part of the Address Mask (RO) depending on the value of MSAC.APSZ. RO and forced to 0 when MSAC.APSZ >= 256MB. (i.e. MSAC.APSZ[0]=1)</p>				
	26:4	Address Mask		
		Default Value:	0000000000000000000000000000000b	
		Access:	RO	
<p>Hardwired to 0s to indicate at least 128MB address range.</p>				
	3	Prefetchable Memory		
		Default Value:	1b	
		Access:	RO	
<p>Hardwired to 1 to enable prefetching.</p>				
	2:1	Memory Type		
		Default Value:	10b	
		Access:	RO	
<p>Hardwired to 2h to indicate 64 bit base address.</p>				
	0	Memory/IO Space		
		Default Value:	0b	
		Access:	RO	
<p>Hardwired to 0 to indicate memory space.</p>				

Graphics Mode Register

GFX_MODE - Graphics Mode Register							
Register Space: MMIO: 0/2/0 Project: BDW Source: RenderCS Default Value: 0x00000000 [BDW:GT1, BDW:GT2:G, BDW:GT2:H, BDW:GT3:H, BDW:GT3E:J] Size (in bits): 32 Trusted Type: 1							
Address: 0229Ch Valid Projects: [BDW]							
Description							
This register contains a control bit for the new execlist and 2-level PPGTT functions.							
DefaultValue = 00002800h							
DWord	Bit	Description					
0	31:16	<p>Mask Bits</p> <table border="1"> <tr> <td>Format:</td><td>Mask[15:0]</td></tr> <tr> <td colspan="2">Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)</td></tr> </table>	Format:	Mask[15:0]	Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)		
Format:	Mask[15:0]						
Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)							
15	<p>Execlist Enable</p> <table border="1"> <tr> <td>Mask:</td><td>MMIO#31</td></tr> <tr> <td colspan="2">When set, software can utilize the execlist registers to load a context into hardware. MI_SET_CONTEXT and MI_ARB_CHECK commands will be converted to NOOP if parsed. When this bit is clear, the Execlist mechanism cannot be used. The context must be loaded via MI_SET_CONTEXT and the ring must be loaded via MMIO access.</td></tr> </table>	Mask:	MMIO#31	When set, software can utilize the execlist registers to load a context into hardware. MI_SET_CONTEXT and MI_ARB_CHECK commands will be converted to NOOP if parsed. When this bit is clear, the Execlist mechanism cannot be used. The context must be loaded via MI_SET_CONTEXT and the ring must be loaded via MMIO access.			
Mask:	MMIO#31						
When set, software can utilize the execlist registers to load a context into hardware. MI_SET_CONTEXT and MI_ARB_CHECK commands will be converted to NOOP if parsed. When this bit is clear, the Execlist mechanism cannot be used. The context must be loaded via MI_SET_CONTEXT and the ring must be loaded via MMIO access.							
14	<p>Programming Notes</p> <p>This bit is <i>not</i> intended to be changed dynamically. Changing the value of this bit while rendering is in progress will have UNDEFINED results. This bit should be changed only <u>after a full reset</u> and <u>before</u> submitting <i>any</i> commands to the device.</p>						
13	<p>Reserved</p> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> </table> <p>Flush TLB invalidation Mode</p> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>U1</td></tr> </table> <p>This field controls the invalidation if the TLB cache inside the hardware. When enabled this bit limits the invalidation of the TLB only to batch buffer boundaries, to pipe_control commands which have the TLB invalidation bit set and sync flushes. If disabled, the TLB caches are flushed for every full flush of the pipeline.</p>	Project:	BDW	Project:	BDW	Format:	U1
Project:	BDW						
Project:	BDW						
Format:	U1						

GFX_MODE - Graphics Mode Register

	12	Reserved	Project:	All	
			Format:	MBZ	
	11	Reserved	Project:	BDW	
			Format:	MBZ	
	10	Reserved	Project:	All	
			Format:	MBZ	
	9	Per-Process GTT Enable	Project:	BDW	
			Format:	Enabled	
		Per-Process GTT Enable			
			Value	Name	Description
			0h	PPGTT Disable [Default]	When clear, the Global GTT will be used to translate memory access from designated commands and for commands that select the PPGTT as their translation space.
			1h	PPGTT Enable	When set, the PPGTT will be used to translate memory access from designated commands and for commands that select the PPGTT as their translation space.
			Programming Notes		
			<p>This bit is used for enabling PPGTT access in Ring Buffer mode of scheduling. Privilege field in context descriptor states the same in Execlist Mode of scheduling. This field should be set before programming PDP0/1/2/3 registers in order to set the PPGTT translation of memory access.</p> <p>Programming this bit doesn't enable or disable the PPGTT translation of memory access immediately; the change comes in to affect only when the Page Directory registers are programmed. Programming this bit must be followed by programming Page Directory Registers in order to enable or disable the PPGTT translation of memory access.</p>		
	8	Reserved	Project:	BDW	

GFX_MODE - Graphics Mode Register

	7	64Bit Virtual Addressing Enable																		
		Project:																		
		Format:																		
		Per-Process GTT Enable																		
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th colspan="3">Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>64Bit Virtual Addressing Disable [Default]</td> <td colspan="3">When clear indicates GFX operating in 32bit Virtual Addressing for PPGTT based memory access.</td></tr> <tr> <td>1h</td> <td>64Bit Virtual Addressing Enable</td> <td colspan="3">When Set indicates GFX operating in 64bit (48bit Canonical) Virtual Addressing for PPGTT based memory access.</td></tr> </tbody> </table>				Value	Name	Description			0h	64Bit Virtual Addressing Disable [Default]	When clear indicates GFX operating in 32bit Virtual Addressing for PPGTT based memory access.			1h	64Bit Virtual Addressing Enable	When Set indicates GFX operating in 64bit (48bit Canonical) Virtual Addressing for PPGTT based memory access.		
Value	Name	Description																		
0h	64Bit Virtual Addressing Disable [Default]	When clear indicates GFX operating in 32bit Virtual Addressing for PPGTT based memory access.																		
1h	64Bit Virtual Addressing Enable	When Set indicates GFX operating in 64bit (48bit Canonical) Virtual Addressing for PPGTT based memory access.																		
		<p style="text-align: center;">Programming Notes</p> <p>This bit is only valid when PPGTT is enabled in ring buffer mode of scheduling. Context Descriptor has a similar bit to control 64bit virtual addressing in execlist mode of scheduling. Whether this field is set or clear virtual addresses translated through GGTT are always 32Bit. This field should be programmed before enabling PPGTT access. When this field is not set or for GGTT virtual addresses, Graphics Address [47:32] field of any commands or register exercised by SW should be programmed to 0x0.</p>																		
	6:5	Reserved																		
		Project:			BDW															
	4	Reserved																		
		Project:			BDW															
	3:1	Reserved																		
		Project:			BDW															
		Format:			MBZ															
	0	Privilege Check Disable																		
		Project:			BDW															
		Format:			Enable															
		This field when set, disables Privilege Violation checks on non-privileged batch buffers. When set Privileged commands are allowed to be executed from non-privileged batch buffers.																		
		<p style="text-align: center;">Workaround</p> <p>Workaround : Irrespective of "Privilege Check Disable" bit set, HW enforces chained or second level batch buffer "Address Space Indicator" to be PPGTT if the parent batch buffer Address Space Indicator is PPGTT.</p>																		

Graphics System Event

GSE_0_2_0_PCI - Graphics System Event				
Register Space:	PCI: 0/2/0			
Project:	BDW			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	000E4h			
This register can be accessed by either Byte, Word, or Dword PCI config cycles. A write to this register will cause the Graphics System Event display interrupt if it is enabled and unmasked in the display interrupt registers.				
DWord	Bit	Description		
0	31:24	GSE Scratch Trigger 3		
		<table border="1"> <tr> <td>Default Value:</td><td>00000000b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table>	Default Value:	00000000b
Default Value:	00000000b			
Access:	R/W			
23:16	GSE Scratch Trigger 2			
	<table border="1"> <tr> <td>Default Value:</td><td>00000000b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table>	Default Value:	00000000b	Access:
Default Value:	00000000b			
Access:	R/W			
15:8	GSE Scratch Trigger 1			
	<table border="1"> <tr> <td>Default Value:</td><td>00000000b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table>	Default Value:	00000000b	Access:
Default Value:	00000000b			
Access:	R/W			
7:0	GSE Scratch Trigger 0			
	<table border="1"> <tr> <td>Default Value:</td><td>00000000b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table>	Default Value:	00000000b	Access:
Default Value:	00000000b			
Access:	R/W			

Graphics Translation Table Memory Mapped Range Address

GTTMMADR_0_2_0_PCI - Graphics Translation Table Memory Mapped Range Address

Register Space:	PCI: 0/2/0							
Project:	BDW							
Default Value:	0x00000004, 0x00000000							
Size (in bits):	64							
Address:	00010h							
<p>This register requests allocation for the combined Graphics Translation Table Modification Range and Memory Mapped Range. The range requires 16 MB combined for MMIO and Global GTT aperture, with 2MB of that used by MMIO, 6MB reserved, and 8MB used by GTT. GTTADDR will begin at (GTTMMADR + 8 MB) while the MMIO base address will be the same as GTTMMADR. The region between (GTTMMADR + 2MB) - (GTTMMADR + 8MB) is reserved. For the Global GTT, this range is defined as a memory BAR in graphics device config space. It is an alias into which software is required to write Page Table Entry values (PTEs). Software may read PTE values from the global Graphics Translation Table (GTT). PTEs cannot be written directly into the global GTT memory area. The device snoops writes to this region in order to invalidate any cached translations within the various TLB's implemented on-chip. The allocation is for 16MB and the base address is defined by bits [38:24]. Note: Per PCI enumeration requirements, to determine the size of a BAR software should write all 1s to the BAR, read it back and see how many of the lower bits read as 0 (meaning that they didn't take the 1s). This indicates the size of the BAR. In order for this to work bits 63 down to the size of the BAR need to be writable to 1s.</p>								
DWord	Bit	Description						
0	63:39	<p>Reserved for Memory Base Address</p> <table border="1"> <tr> <td>Default Value:</td><td>0000000000000000000000000000000b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> <tr> <td colspan="2">FLR Resettable Must be set to 0 since addressing above 512GB is not supported.</td></tr> </table>	Default Value:	0000000000000000000000000000000b	Access:	R/W	FLR Resettable Must be set to 0 since addressing above 512GB is not supported.	
Default Value:	0000000000000000000000000000000b							
Access:	R/W							
FLR Resettable Must be set to 0 since addressing above 512GB is not supported.								
38:24	<p>Memory Base Address Lower bits</p> <table border="1"> <tr> <td>Default Value:</td><td>0000000000000000b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> <tr> <td colspan="2">FLR Resettable Set by the OS, these bits correspond to address signals [38:24].</td></tr> </table>	Default Value:	0000000000000000b	Access:	R/W	FLR Resettable Set by the OS, these bits correspond to address signals [38:24].		
Default Value:	0000000000000000b							
Access:	R/W							
FLR Resettable Set by the OS, these bits correspond to address signals [38:24].								
23:4	<p>Address Mask</p> <table border="1"> <tr> <td>Default Value:</td><td>0000000000000000000000000000000b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> <tr> <td colspan="2">Hardwired to 0s to indicate at least 16MB address range.</td></tr> </table>	Default Value:	0000000000000000000000000000000b	Access:	RO	Hardwired to 0s to indicate at least 16MB address range.		
Default Value:	0000000000000000000000000000000b							
Access:	RO							
Hardwired to 0s to indicate at least 16MB address range.								
3	<p>Prefetchable Memory</p> <table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> <tr> <td colspan="2">Hardwired to 0 to prevent prefetching.</td></tr> </table>	Default Value:	0b	Access:	RO	Hardwired to 0 to prevent prefetching.		
Default Value:	0b							
Access:	RO							
Hardwired to 0 to prevent prefetching.								

GTTMMADR_0_2_0_PCI - Graphics Translation Table Memory Mapped Range Address

	2:1	Memory Type
		Default Value:
		Access:
Hardwired to 2h to indicate 64 bit base address.		
	0	Memory/IO Space
		Default Value:
		Access:
Hardwired to 0 to indicate memory space.		

GS Invocation Counter

GS_INVOCATION_COUNT - GS Invocation Counter		
Register Space: MMIO: 0/2/0 Project: BDW Source: RenderCS Default Value: 0x00000000, 0x00000000 Access: R/W Size (in bits): 64 Trusted Type: 1		
Address: 02328h		
This register stores the number of objects that are part of geometry shader threads. This register is part of the context save and restore.		
DWord	Bit	Description
0	63:32	GS Invocation Count UDW Number of objects that are dispatched as a geometry shader threads invoked by the GS stage. Updated only when Statistics Enable is set in GS_STATE (see the Geometry Shader Chapter in the 3D Volume.)
	31:0	GS Invocation Count LDW Number of objects that are dispatched as a geometry shader threads invoked by the GS stage. Updated only when Statistics Enable is set in GS_STATE (see the Geometry Shader Chapter in the 3D Volume.)

GS Primitives Counter

GS_PRIMITIVES_COUNT - GS Primitives Counter		
Register Space: MMIO: 0/2/0 Project: BDW Source: RenderCS Default Value: 0x00000000, 0x00000000 Access: R/W Size (in bits): 64 Trusted Type: 1		
Address: 02330h		
This register reflects the total number of primitives that have been output by the Geometry Shader stage. This register is part of the context save and restore.		
DWord	Bit	Description
0	63:32	GS Primitives Count UDW Total number of primitives output by the geometry stage. Updated only when Statistics Enable is set in GS_STATE (see the Geometry Shader Chapter in the 3D Volume.)
	31:0	GS Primitives Count LDW Total number of primitives output by the geometry stage. Updated only when Statistics Enable is set in GS_STATE (see the Geometry Shader Chapter in the 3D Volume.)

GT4 Mode Control Register

GT4MODECTL - GT4 Mode Control Register		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	09038h	
GT4 Mode Control Register		
DWord	Bit	Description
0	31:18	RSVD Access: R/W
	17:10	Reserved
	9:2	Reserved
	1:0	GT4 Mode Control Access: R/W GT4 Usage mode: 00b: Non-GT4. 01b: GT4 is used in Alternate Frame rendering Mode (AFR). 10b: Basic Split Frame rendering Mode (SFR). 11b: Complex Split Frame rendering Mode (SFR w/ CBR).

GTC_CPU_CTL

GTC_CPU_CTL								
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x0000010E Access: R/W Size (in bits): 32								
Address: 67000h-67003h Name: Global Time Code CPU Control ShortName: GTC_CPU_CTL Power: off/on Reset: soft								
DWord	Bit	Description						
0	31	GTC CPU Slave Enable This bit enables the slave GTC. When enabled, the slave uses periodic GTC messages received from PCH over CSYNC to update its GTC value. If this bit is set but the PCH GTC controller is disabled, the slave GTC runs independently with no forced synchronization to PCH GTC controller. <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Disable</td></tr> <tr> <td>1b</td><td>Enable</td></tr> </tbody> </table> <p>Restriction</p> <p>The DDA M/N settings must be programmed to valid values before enabling this bit.</p>	Value	Name	0b	Disable	1b	Enable
Value	Name							
0b	Disable							
1b	Enable							
30:29 Reserved								
28 Reserved								
27:25 Reserved								

GTC_CPU_CTL

	24	<p>Maintenance Phase Enable</p> <p>This bit is used to transition from lock acquisition to lock maintenance phase. The CPU GTC slave can generate an interrupt every time it receives a GTC update message from the PCH. Check for lock status by reading the slave lock field in the GTC_CPU_MISC register. Set this bit to 1b after making the determination that lock requirement has been satisfied. If it is determined that CPU GTC slave is no longer locked while in maintenance mode, clear this bit and attempt to achieve lock again.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Lock</td><td>Lock acquisition phase</td></tr> <tr> <td>1b</td><td>Maintain</td><td>Lock maintenance phase</td></tr> </tbody> </table> <p>Programming Notes</p> <p>Maintenance interval for sending GTC updates is 11ms instead of 10ms.</p>	Value	Name	Description	0b	Lock	Lock acquisition phase	1b	Maintain	Lock maintenance phase
Value	Name	Description									
0b	Lock	Lock acquisition phase									
1b	Maintain	Lock maintenance phase									
	23:21	Reserved									
	20:11	Reserved									
	10:1	<p>Reference Clock Freq</p> <table border="1"> <tr> <td>Default Value:</td> <td>1 0000 111b 135</td> </tr> </table> <p>This field is used to indicate the frequency of the reference clock used by the GTC slave and aux decoder. Hardware uses this value to divide down the GTC reference clock as needed to implement 1MHz aux signaling frequency. The input clock is the non-SSC reference. The frequency can be found in the FUSE_STRAP3 register.</p>	Default Value:	1 0000 111b 135							
Default Value:	1 0000 111b 135										
	0	Reserved									

GTC_CPU_DDA_M

GTC_CPU_DDA_M		
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x00000000 Access: R/W Size (in bits): 32		
Address: 67010h-67013h Name: Global Time Code CPU DDA M Value ShortName: GTC_CPU_DDA_M Power: off/on Reset: soft		
DWord	Bit	Description
0	31:24	Reserved
	23:0	GTC DDA M This field is the M value of the GTC DDA. The ratio of M to N programmed depends on the GTC reference clock. The DDA programmed values are related by the following formula: $1/(\text{accumulator increment}) = \text{Reference Clock} * \text{DDA_M} / \text{DDA_N}$.

GTC_CPU_DDA_N

GTC_CPU_DDA_N				
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x00000000 Access: R/W Size (in bits): 32				
Address: 67014h-67017h Name: Global Time Code CPU DDA N Value ShortName: GTC_CPU_DDA_N Power: off/on Reset: soft				
DWord	Bit	Description		
0	31:24	<p>GTC Accum Inc</p> <table border="1"> <tr> <td>Format:</td> <td>U7.1</td> </tr> </table> <p>This field is the GTC accumulator increment value in nanoseconds each time the DDA trips. It is programmed in 7.1 fixed point binary format where the LSB represents 0.5ns increment.</p>	Format:	U7.1
Format:	U7.1			
23:0	<p>GTC DDA N</p> <p>This field is the N value of the GTC DDA. The ratio of M to N programmed depends on the GTC reference clock and should not result in any accumulation error in any 10ms interval period. The DDA programmed values are related by the following formula: $1/(\text{accumulator increment}) = \text{Reference Clock} * \text{DDA_M} / \text{DDA_N}$.</p>			

GTC_CPU_IIR

GTC_CPU_IIR								
DWord	Bit	Description						
0	31:0	<p>Interrupt Identity Bits</p> <p>This field holds the persistent values of the GTC CPU interrupt bits which are unmasked by the GTC_CPU_IMR. Bits set in this register will propagate to the GTC_CPU interrupt in the Display Engine Miscellaneous Interrupts. Bits set in this register will remain set (persist) until the interrupt condition is cleared by writing a '1' to the appropriate bits.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Condition Not Detected</td> </tr> <tr> <td>1b</td> <td>Condition Detected</td> </tr> </tbody> </table>	Value	Name	0b	Condition Not Detected	1b	Condition Detected
Value	Name							
0b	Condition Not Detected							
1b	Condition Detected							
		See the GTC CPU interrupt bit definition to find the source event for each interrupt bit.						

GTC_CPU_IMR

GTC_CPU_IMR										
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x0000007F Access: R/W Size (in bits): 32										
Address: 67054h-67057h Name: Global Time Code CPU Interrupt Mask ShortName: GTC_CPU_IMR Power: off/on Reset: soft										
See the GTC CPU interrupt bit definition to find the source event for each interrupt bit.										
DWord	Bit	Description								
0	31:0	<p>Interrupt Mask Bits This field contains a bit mask which selects which GTC CPU events are reported int the GTC CPU IIR.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Not Masked</td></tr> <tr> <td>1b</td><td>Masked</td></tr> <tr> <td>00000007Fh</td><td>All interrupts masked [Default]</td></tr> </tbody> </table>	Value	Name	0b	Not Masked	1b	Masked	00000007Fh	All interrupts masked [Default]
Value	Name									
0b	Not Masked									
1b	Masked									
00000007Fh	All interrupts masked [Default]									

GTC_CPU_LOCAL_CURR

GTC_CPU_LOCAL_CURR		
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x00000000 Access: RO Size (in bits): 32		
Address: 67028h-6702Bh Name: Global Time Code CPU Local Current Value ShortName: GTC_CPU_LOCAL_CURR Power: off/on Reset: soft		
DWord	Bit	Description
0	31:0	GTC Local Current Value This field contains the last CPU GTC value sampled at the Aux sync point of the GTC update message received from PCH GTC controller.

GTC_CPU_LOCAL_PREV

GTC_CPU_LOCAL_PREV		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Address:	67030h-67033h	
Name:	Global Time Code CPU Local Previous Value	
ShortName:	GTC_CPU_LOCAL_PREV	
Power:	off/on	
Reset:	soft	
<hr/>		
DWord	Bit	Description
0	31:0	<p>GTC Local Previous Value</p> <p>This field contains the second to last CPU GTC value sampled at the Aux sync point of the GTC update message received from PCH GTC controller.</p>

GTC_CPU_MISC

GTC_CPU_MISC																	
DWord	Bit	Description															
0	31:24	Reserved															
	23:22	CPU GTC Lock Compare Value This field programs the threshold used to determine whether to set the lock status bit following comparison between the slave and master GTC values. <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>30ns</td> <td>Difference between master/slave is less than 30ns</td> </tr> <tr> <td>01b</td> <td>50ns [Default]</td> <td>Difference between master/slave is less than 50ns (default)</td> </tr> <tr> <td>10b</td> <td>100ns</td> <td>Difference between master/slave is less than 100ns</td> </tr> <tr> <td>11b</td> <td>200ns</td> <td>Difference between master/slave is less than 200ns</td> </tr> </tbody> </table>	Value	Name	Description	00b	30ns	Difference between master/slave is less than 30ns	01b	50ns [Default]	Difference between master/slave is less than 50ns (default)	10b	100ns	Difference between master/slave is less than 100ns	11b	200ns	Difference between master/slave is less than 200ns
Value	Name	Description															
00b	30ns	Difference between master/slave is less than 30ns															
01b	50ns [Default]	Difference between master/slave is less than 50ns (default)															
10b	100ns	Difference between master/slave is less than 100ns															
11b	200ns	Difference between master/slave is less than 200ns															
	21:16	Reserved															
	15:6	Reserved															
	5:0	Update Message Delay This field is the absolute delay in nanoseconds between the GTC aux sync point event in PCH and the corresponding sync point seen by the CPU GTC slave. It represents the delay between the GTC values in PCH and CPU due to fixed propagation delay of GTC update message. It is only applied to the GTC value sampled for audio. It is not factored directly in the CPU slave GTC update computation or reflected in the GTC local registers.															

GTC_CPU_REMOTE_CURR

GTC_CPU_REMOTE_CURR		
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x00000000 Access: RO Size (in bits): 32		
Address: 67024h-67027h Name: Global Time Code CPU Remote Current Value ShortName: GTC_CPU_REMOTE_CURR Power: off/on Reset: soft		
DWord	Bit	Description
0	31:0	GTC Remote Current Value This field contains the last PCH GTC value received via the GTC update message. It represents the value of the (remote) PCH GTC at the Aux sync point at time of transmission of the message over CSYNC. The PCH GTC controller sends periodic updates of its GTC value to the CPU GTC slave.

GTC_CPU_REMOTE_PREV

GTC_CPU_REMOTE_PREV		
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x00000000 Access: RO Size (in bits): 32		
Address: 6702Ch-6702Fh Name: Global Time Code CPU Remote Previous Value ShortName: GTC_CPU_REMOTE_PREV Power: off/on Reset: soft		
DWord	Bit	Description
0	31:0	GTC Remote Previous Value This field contains the second to last PCH GTC value received via the GTC update message. It represents the value of the (remote) PCH GTC at the Aux sync point at time of transmission of the message over CSYNC. The PCH GTC controller sends periodic updates of its GTC value to the CPU GTC slave.

GTC_CTL

GTC_CTL																				
Register Space: MMIO: 0/2/0 Project: DevLPT Default Value: 0x0400010E Access: R/W Size (in bits): 32																				
Address: E7000h-E7003h Name: Global Time Code Control ShortName: GTC_CTL Power: Always on Reset: soft																				
DWord	Bit	Description																		
0	31	<p>GTC Function Enable</p> <table border="1"> <thead> <tr> <th colspan="2">Description</th><th>Project</th></tr> </thead> <tbody> <tr> <td colspan="2">This bit enables the PCH GTC counter and periodic PCH update messages to the GTC slave in the CPU. Software must enable this bit before enabling GTC controller operation on a port with a GTC capable device.</td><td></td></tr> <tr> <td colspan="2">The GTC clock must be enabled in GTCLK_EN and warmed up for 40us prior to enabling GTC.</td><td>DevLPT:LP</td></tr> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> <tr> <td>0b</td><td>Disable</td><td>GTC Disabled</td></tr> <tr> <td>1b</td><td>Enable</td><td>GTC Enabled</td></tr> </tbody> </table> <p>Workaround</p> <p>On LP systems with ISCLK PLL shutdown enabled, display register C2020h bit 12 must be set to 1b before enabling GTC. If no other feature requires register C2020h bit 12, it can be cleared to 0b after GTC is disabled. To save power, register C2020h bit 12 must be cleared to 0b when internal graphics is put in the D3 device power state.</p>	Description		Project	This bit enables the PCH GTC counter and periodic PCH update messages to the GTC slave in the CPU. Software must enable this bit before enabling GTC controller operation on a port with a GTC capable device.			The GTC clock must be enabled in GTCLK_EN and warmed up for 40us prior to enabling GTC.		DevLPT:LP	Value	Name	Description	0b	Disable	GTC Disabled	1b	Enable	GTC Enabled
Description		Project																		
This bit enables the PCH GTC counter and periodic PCH update messages to the GTC slave in the CPU. Software must enable this bit before enabling GTC controller operation on a port with a GTC capable device.																				
The GTC clock must be enabled in GTCLK_EN and warmed up for 40us prior to enabling GTC.		DevLPT:LP																		
Value	Name	Description																		
0b	Disable	GTC Disabled																		
1b	Enable	GTC Enabled																		

GTC_CTL

	30:29	Master Select This field shall be set by software designate the GTC master. The PCH GTC controller is master by default; however it may designate an attached GTC device as the master. This occurs in response to request from designated GTC sink to act as master. Only one remote GTC sink may act as master. When operating as a slave, the GTC controller of the designated port will transition from writing GTCs periodically to the remote GTC sink to reading GTCs periodically from the remote GTC sink. The GTC controller must be returned to lock acquisition phase before changing this register field. Slave mode only															
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>00b</td><td>Master</td><td>GTC controller is master</td></tr> <tr> <td>01b</td><td>PortB</td><td>GTC controller is slave to GTC sink on port B</td></tr> <tr> <td>10b</td><td>PortC</td><td>GTC controller is slave to GTC sink on port C</td></tr> <tr> <td>11b</td><td>PortD</td><td>GTC controller is slave to GTC sink on port D</td></tr> </tbody> </table>	Value	Name	Description	00b	Master	GTC controller is master	01b	PortB	GTC controller is slave to GTC sink on port B	10b	PortC	GTC controller is slave to GTC sink on port C	11b	PortD	GTC controller is slave to GTC sink on port D
Value	Name	Description															
00b	Master	GTC controller is master															
01b	PortB	GTC controller is slave to GTC sink on port B															
10b	PortC	GTC controller is slave to GTC sink on port C															
11b	PortD	GTC controller is slave to GTC sink on port D															
	28	Reserved															
	27:26	CPU Update Interval This field programs the interval period used by GTC master to update the GTC slave in the CPU. During lock acquisition with remote GTC sink device software should program this value to 1ms or less. After remote sink lock done bit has been detected and at the time software enables maintenance phase enable bit, this bit should be set to 10ms.															
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>00b</td><td>0.5ms</td><td>Send update every 0.5ms</td></tr> <tr> <td>01b</td><td>1ms [Default]</td><td>Send update every 1ms</td></tr> <tr> <td>10b</td><td>2ms</td><td>Send update every 2ms</td></tr> <tr> <td>11b</td><td>10ms</td><td>Send update every 10ms</td></tr> </tbody> </table>	Value	Name	Description	00b	0.5ms	Send update every 0.5ms	01b	1ms [Default]	Send update every 1ms	10b	2ms	Send update every 2ms	11b	10ms	Send update every 10ms
Value	Name	Description															
00b	0.5ms	Send update every 0.5ms															
01b	1ms [Default]	Send update every 1ms															
10b	2ms	Send update every 2ms															
11b	10ms	Send update every 10ms															
	25:13	Reserved															
	12:11	Reserved															
		<table border="1"> <tr> <td>Project:</td><td>DevLPT:LP</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	DevLPT:LP	Format:	MBZ											
Project:	DevLPT:LP																
Format:	MBZ																
	12:11	Reserved															
		<table border="1"> <tr> <td>Project:</td><td>DevLPT:H</td></tr> </table>	Project:	DevLPT:H													
Project:	DevLPT:H																

GTC_CTL											
	10:1	Reference Clock Freq									
		<table border="1"> <thead> <tr> <th>Description</th><th>Project</th></tr> </thead> <tbody> <tr> <td>This field is used to indicate the frequency of the reference clock used by aux encoder/decoder to transmit update messages from PCH to CPU. Hardware shall use this value to divide down the GTC reference clock as needed to implement 1MHz aux signaling frequency.</td><td></td></tr> <tr> <td>Reference clock is 135 MHz</td><td>DevLPT:H</td></tr> <tr> <td>Reference clock is 96 MHz</td><td>DevLPT:LP</td></tr> </tbody> </table>	Description	Project	This field is used to indicate the frequency of the reference clock used by aux encoder/decoder to transmit update messages from PCH to CPU. Hardware shall use this value to divide down the GTC reference clock as needed to implement 1MHz aux signaling frequency.		Reference clock is 135 MHz	DevLPT:H	Reference clock is 96 MHz	DevLPT:LP	
Description	Project										
This field is used to indicate the frequency of the reference clock used by aux encoder/decoder to transmit update messages from PCH to CPU. Hardware shall use this value to divide down the GTC reference clock as needed to implement 1MHz aux signaling frequency.											
Reference clock is 135 MHz	DevLPT:H										
Reference clock is 96 MHz	DevLPT:LP										
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Project</th></tr> </thead> <tbody> <tr> <td>0001 0000 111b</td><td>135 MHz [Default]</td><td>DevLPT:H</td></tr> <tr> <td>0000 1100 000b</td><td>96 MHz [Default]</td><td>DevLPT:LP</td></tr> </tbody> </table>	Value	Name	Project	0001 0000 111b	135 MHz [Default]	DevLPT:H	0000 1100 000b	96 MHz [Default]	DevLPT:LP
Value	Name	Project									
0001 0000 111b	135 MHz [Default]	DevLPT:H									
0000 1100 000b	96 MHz [Default]	DevLPT:LP									
	0	Reserved									

GTC_DDA_M

GTC_DDA_M		
Register Space: MMIO: 0/2/0 Project: DevLPT Default Value: 0x00000000 Access: R/W Size (in bits): 32		
Address: E7010h-E7013h Name: Global Time Code DDA M Value ShortName: GTC_DDA_M Power: Always on Reset: soft		
DWord	Bit	Description
0	31:24	Reserved
	23:0	GTC DDA M This field is used to program the M value of the GTC DDA. The ratio of M to N programmed depends on the GTC reference clock. The DDA programmed values are related by the following formula: $1/(\text{accumulator increment}) = \text{Reference Clock} * \text{DDA_M} / \text{DDA_N}$

GTC_DDA_N

GTC_DDA_N						
DWord	Bit	Description				
0	31:26	<p>GTC Accum Inc</p> <table> <tr> <td>Format:</td> <td>U5.1</td> </tr> <tr> <td colspan="2">This field is used to program the GTC accumulator increment value in nanoseconds each time the DDA trips. It should be programmed in 5.1 fixed point binary format where the LSB represents 0.5ns increment.</td></tr> </table>	Format:	U5.1	This field is used to program the GTC accumulator increment value in nanoseconds each time the DDA trips. It should be programmed in 5.1 fixed point binary format where the LSB represents 0.5ns increment.	
Format:	U5.1					
This field is used to program the GTC accumulator increment value in nanoseconds each time the DDA trips. It should be programmed in 5.1 fixed point binary format where the LSB represents 0.5ns increment.						
25:24	Reserved					
23:0	<p>GTC DDA N</p> <p>This field is used to program the N value of the GTC DDA. The ratio of M to N programmed depends on the GTC reference clock and should not result in any accumulation error in any 10ms interval period. The DDA programmed values are related by the following formula: $1/(\text{accumulator increment}) = \text{Reference Clock} * \text{DDA_M} / \text{DDA_N}$</p>					

GTC_MISC

GTC_MISC																	
DWord	Bit	Description															
0	31:24	<p>GTC Lock Status</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>This field stores the history of the last 8 compare results to determine if GTC slave is tracking remote GTC master. The LSB indicates the most recent compare result. The MSB indicates the oldest compare result. The LSB is set if the difference between master and slave GTC is less than the GTC lock compare value. When a new comparison is complete, the LSB is updated with the result and the previous results are shifted towards the MSB and the old MSB is dropped.</p>	Access:	RO													
Access:	RO																
	23:22	<p>CPU GTC Lock Compare Value</p> <p>This field programs the threshold used to determine whether to set the lock status bit following comparison between the slave and master GTC values.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>30ns</td> <td>Difference between master/slave is less than 30ns</td> </tr> <tr> <td>01b</td> <td>50ns [Default]</td> <td>Difference between master/slave is less than 50ns</td> </tr> <tr> <td>10b</td> <td>100ns</td> <td>Difference between master/slave is less than 100ns</td> </tr> <tr> <td>11b</td> <td>200ns</td> <td>Difference between master/slave is less than 200ns</td> </tr> </tbody> </table>	Value	Name	Description	00b	30ns	Difference between master/slave is less than 30ns	01b	50ns [Default]	Difference between master/slave is less than 50ns	10b	100ns	Difference between master/slave is less than 100ns	11b	200ns	Difference between master/slave is less than 200ns
Value	Name	Description															
00b	30ns	Difference between master/slave is less than 30ns															
01b	50ns [Default]	Difference between master/slave is less than 50ns															
10b	100ns	Difference between master/slave is less than 100ns															
11b	200ns	Difference between master/slave is less than 200ns															
	21:12	<p>Reserved</p> <table border="1"> <tr> <td>Project:</td> <td>DevLPT:H</td> </tr> </table>	Project:	DevLPT:H													
Project:	DevLPT:H																
	21:12	<p>GTC Update Message Delay</p> <table border="1"> <tr> <td>Default Value:</td> <td>00110100b 52 nanoseconds</td> </tr> <tr> <td>Project:</td> <td>DevLPT:LP</td> </tr> </table> <p>In master mode this field is used to program the absolute delay in nanoseconds between the GTC at the aux sync point event in PCH and the corresponding GTC value at the capture point. It represents the delay between the GTC values at the aux sync point and capture point introduced due to synchronization and glitch suppression.</p>	Default Value:	00110100b 52 nanoseconds	Project:	DevLPT:LP											
Default Value:	00110100b 52 nanoseconds																
Project:	DevLPT:LP																

GTC_MISC				
	11:8	<p>Min Lock Duration</p> <table border="1"> <tr> <td>Default Value:</td><td>1010b 10ms</td></tr> </table> <p>This field determines the minimum duration in milliseconds of lock acquisition phase after which software is notified through interrupt. The GTC interrupt enable and mask register programming must be enabled beforehand. Software may also poll the interrupt identity bit in IIR.</p>	Default Value:	1010b 10ms
Default Value:	1010b 10ms			
	7:0	<p>Max Lock Timeout</p> <p>This field determines the minimum duration in 1ms increments of lock acquisition phase after which software is notified through interrupt that GTC was unable to achieve lock with remote GTC sync. Default programming of "0000" disables hardware timeout error notification.</p>		

GTC_PCH_IIR

GTC_PCH_IIR											
Register Space:	MMIO: 0/2/0										
Project:	DevLPT										
Default Value:	0x00000000										
Access:	R/WC										
Size (in bits):	32										
Address:	E7058h-E705Bh										
Name:	Global Time Code Interrupt Identity										
ShortName:	GTC_PCH_IIR										
Power:	Always on										
Reset:	soft										
See the GTC PCH interrupt bit definition table to find the source event for each interrupt bit.											
DWord	Bit	Description									
0	31:0	<p>Interrupt Identity Bits</p> <p>This field holds the persistent values of the GTC PCH interrupt bits which are unmasked by the GTC_PCH_IMR. Bits set in this register will propagate to the combined GTC_PCH interrupt in the SDE_ISR. Bits set in this register will remain set (persist) until the interrupt condition is cleared by writing a '1' to the appropriate bits.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Condition Not Detected</td><td>Interrupt Condition Not Detected</td></tr> <tr> <td>1b</td><td>Condition Detected</td><td>Interrupt Condition Detected</td></tr> </tbody> </table>	Value	Name	Description	0b	Condition Not Detected	Interrupt Condition Not Detected	1b	Condition Detected	Interrupt Condition Detected
Value	Name	Description									
0b	Condition Not Detected	Interrupt Condition Not Detected									
1b	Condition Detected	Interrupt Condition Detected									

GTC_PCH_IMR

GTC_PCH_IMR											
Register Space: MMIO: 0/2/0 Project: DevLPT Default Value: 0x00000000 Access: R/W Size (in bits): 32											
Address: E7054h-E7057h Name: Global Time Code Interrupt Mask ShortName: GTC_PCH_IMR Power: Always on Reset: soft											
See the GTC PCH interrupt bit definition table to find the source event for each interrupt bit.											
DWord	Bit	Description									
0	31:0	<p>Interrupt Mask Bits This field contains a bit mask which selects which GTC PCH events are reported in the GTC PCH IIR.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Not Masked</td><td>Not Masked - will be reported in the GTC_PCH_IIR</td></tr> <tr> <td>1b</td><td>Masked</td><td>Masked - will not be reported in the GTC_PCH_IIR</td></tr> </tbody> </table>	Value	Name	Description	0b	Not Masked	Not Masked - will be reported in the GTC_PCH_IIR	1b	Masked	Masked - will not be reported in the GTC_PCH_IIR
Value	Name	Description									
0b	Not Masked	Not Masked - will be reported in the GTC_PCH_IIR									
1b	Masked	Masked - will not be reported in the GTC_PCH_IIR									

GTC_PORT_CTL

GTC_PORT_CTL											
Register Space:	MMIO: 0/2/0										
Project:	DevLPT										
Default Value:	0x00000000										
Access:	R/W										
Size (in bits):	32										
Address:	E70B0h-E70B3h										
Name:	Global Time Code Port B Control										
ShortName:	GTC_PORT_CTL_B										
Power:	Always on										
Reset:	soft										
Address:	E70C0h-E70C3h										
Name:	Global Time Code Port C Control										
ShortName:	GTC_PORT_CTL_C										
Power:	Always on										
Reset:	soft										
Address:	E70D0h-E70D3h										
Name:	Global Time Code Port D Control										
ShortName:	GTC_PORT_CTL_D										
Power:	Always on										
Reset:	soft										
There is one instance of this register per port B, C, and D.											
DWord	Bit	Description									
0	31	<p>Port GTC Enable</p> <p>This bit enables the GTC controller to start lock acquisition phase with remote GTC sink connected to this port. The Maintenance_phase_enable bit must be initially written as '0' when this bit is set. This bit has no effect if the GTC controller is disabled.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Disable</td><td>GTC synchronization with remote sink disabled</td></tr> <tr> <td>1b</td><td>Enable</td><td>GTC synchronization with remote sink enabled</td></tr> </tbody> </table> <p>Programming Notes</p> <p>When this port is enabled software must use the associated GTC Update Complete interrupt to determine that a hardware periodic update was completed prior to initiating a read from GTC remote slave.</p>	Value	Name	Description	0b	Disable	GTC synchronization with remote sink disabled	1b	Enable	GTC synchronization with remote sink enabled
Value	Name	Description									
0b	Disable	GTC synchronization with remote sink disabled									
1b	Enable	GTC synchronization with remote sink enabled									

GTC_PORT_CTL												
		Restriction	Project									
		Restriction : Prior to the LPT:H:B1 and LPT:LP:A1 steppings, Global Time Code hardware initiated periodic updates to remote GTC slave is not supported.	DevLPT:H, EXCLUDE(LPT:H:A), EXCLUDE(LPT:H:B0), EXCLUDE(LPT:LP:A0)									
30:25	Reserved											
24	Maintenance Phase Enable This bit is used by software to transition from lock acquisition to lock maintenance phase. The GTC controller generates an interrupt at the end of the lock phase as determined by lock acquisition duration field. Software shall read the sink device GTC lock done bit. If set, software shall set this bit to '1' after first writing the GTC skew value to the RX GTC skew DPCD offset with GTC skew enable bit set to '1'.											
	<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Lock</td><td>Lock acquisition phase—the controller writes or reads GTC every 1ms</td></tr> <tr> <td>1b</td><td>Maintain</td><td>Lock maintenance phase—the controller writes or reads GTC every 10ms</td></tr> </tbody> </table>			Value	Name	Description	0b	Lock	Lock acquisition phase—the controller writes or reads GTC every 1ms	1b	Maintain	Lock maintenance phase—the controller writes or reads GTC every 10ms
Value	Name	Description										
0b	Lock	Lock acquisition phase—the controller writes or reads GTC every 1ms										
1b	Maintain	Lock maintenance phase—the controller writes or reads GTC every 10ms										
23:2	Reserved											
1	GTC Port TX Lock Done This bit indicates the GTC controller operating in slave mode has achieved lock with the remote GTC sink. This bit shall be written by software based on hardware compare results between GTC controller in slave mode and remote GTC master. This bit shall be cleared by software when GTC controller is returned to lock acquisition phase. Slave mode only											
	<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>NoLock</td><td>GTC TX slave not locked</td></tr> <tr> <td>1b</td><td>Lock</td><td>GTC TX slave lock achieved</td></tr> </tbody> </table>			Value	Name	Description	0b	NoLock	GTC TX slave not locked	1b	Lock	GTC TX slave lock achieved
Value	Name	Description										
0b	NoLock	GTC TX slave not locked										
1b	Lock	GTC TX slave lock achieved										
0	GTC Port RX Lock Done This bit indicates the remote GTC sink has achieved lock. This bit shall be written by software after reading remote GTC sink DPCD register. This bit shall be cleared by software when GTC controller is reset from lock maintenance mode to lock acquisition mode or when the controller is disabled.											
	<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>NoLock</td><td>GTC RX slave not locked</td></tr> <tr> <td>1b</td><td>Lock</td><td>GTC RX slave lock achieved</td></tr> </tbody> </table>			Value	Name	Description	0b	NoLock	GTC RX slave not locked	1b	Lock	GTC RX slave lock achieved
Value	Name	Description										
0b	NoLock	GTC RX slave not locked										
1b	Lock	GTC RX slave lock achieved										

GTC_PORT_RX_CURR

GTC_PORT_RX_CURR		
Register Space:	MMIO: 0/2/0	
Project:	DevLPT	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Address:	E70B4h-E70B7h	
Name:	Global Time Code Port B RX Current Value	
ShortName:	GTC_PORT_RX_CURR_B	
Power:	Always on	
Reset:	soft	
Address:	E70C4h-E70C7h	
Name:	Global Time Code Port C RX Current Value	
ShortName:	GTC_PORT_RX_CURR_C	
Power:	Always on	
Reset:	soft	
Address:	E70D4h-E70D7h	
Name:	Global Time Code Port D RX Current Value	
ShortName:	GTC_PORT_RX_CURR_D	
Power:	Always on	
Reset:	soft	
There is one instance of this register per port B, C, and D.		
DWord	Bit	Description
0	31:0	GTC Port RX Current This field contains the remote sink GTC value at the Aux sync point of the response message from the remote GTC sink. It is updated by hardware following a read of the remote sink GTC DPCD register.

GTC_PORT_TX_CURR

GTC_PORT_TX_CURR		
Register Space:	MMIO: 0/2/0	
Project:	DevLPT	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Address:	E70B8h-E70BBh	
Name:	Global Time Code Port B TX Current Value	
ShortName:	GTC_PORT_TX_CURR_B	
Power:	Always on	
Reset:	soft	
Address:	E70C8h-E70CBh	
Name:	Global Time Code Port C TX Current Value	
ShortName:	GTC_PORT_TX_CURR_C	
Power:	Always on	
Reset:	soft	
Address:	E70D8h-E70DBh	
Name:	Global Time Code Port D TX Current Value	
ShortName:	GTC_PORT_TX_CURR_D	
Power:	Always on	
Reset:	soft	
There is one instance of this register per port B, C, and D.		
DWord	Bit	Description
0	31:0	<p>GTC Port TX Current</p> <p>This field contains the local GTC value sampled at the Aux sync point of the response message from remote GTC sink following software read of remote sink GTC DPCD register when PCH GTC controller is operating as master. When PCH GTC controller is operating as a slave this field contains the local GTC value sampled at the Aux sync point of the response message. In both master and slave mode this register is updated by hardware.</p>

GTC_SLAVE_RX_PREV

GTC_SLAVE_RX_PREV		
Register Space: MMIO: 0/2/0 Project: DevLPT Default Value: 0x00000000 Access: RO Size (in bits): 32		
Address: E7078h-E707Bh Name: Global Time Code RX Previous Value ShortName: GTC_SLAVE_RX_PREV Power: Always on Reset: soft		
DWord	Bit	Description
0	31:0	GTC RX Previous This field contains the previous GTC value read from remote GTC sink. It is transferred from the GTC_PORT_RX_VALUE register of port designated as master when the current value is updated. This register is valid only when GTC controller is operating as a slave to remote GTC master. Slave mode only

GTC_SLAVE_TX_PREV

GTC_SLAVE_TX_PREV		
Register Space: MMIO: 0/2/0 Project: DevLPT Default Value: 0x00000000 Access: RO Size (in bits): 32		
Address: E707Ch-E707Fh Name: Global Time Code TX Previous Value ShortName: GTC_SLAVE_TX_PREV Power: Always on Reset: soft		
DWord	Bit	Description
0	31:0	<p>GTC TX Previous</p> <p>This field contains the previous local GTC value sampled at Aux sync point. It is transferred from the GTC_PORT_TX_VALUE register of port designated as master when the current value is updated. This register is valid only when GTC controller is operating as a slave to remote GTC master. Slave mode only</p>

GTCLK_EN

GTCLK_EN								
DWord	Bit	Description						
0	31:1	Reserved Format: MBZ						
	0	GTC Clock Enable This field controls the GTC clock enable. <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disable</td> </tr> <tr> <td>1b</td> <td>Enable</td> </tr> </tbody> </table> Programming Notes The GTC clock must be enabled for at least 40us prior to enabling GTC. The clock must be kept enabled until after GTC is disabled.	Value	Name	0b	Disable	1b	Enable
Value	Name							
0b	Disable							
1b	Enable							

GTC PCH Interrupt Bit Definition

GTC PCH Interrupt Bit Definition				
DWord	Bit	Description		
0	31:27	Reserved <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ
Format:	MBZ			
26	Reserved			
25	GTC Lock Loss PCH GTC has lost lock with a remote GTC sink. The difference between the local and remote GTC has exceeded programmed threshold.			
24:19	Reserved <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ	
Format:	MBZ			
18	Reserved			
17	GTC Aux Rx Error portD An aux channel error occurred during PCH GTC transfer with remote GTC sink attached to this port.			
16	GTC Update Complete portD A hardware initiated GTC update has completed with a sink attached to this port. This may be either a write of PCH GTC master to remote GTC slave or a read of the GTC of a remote master.			
15:11	Reserved <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ	
Format:	MBZ			
10	Reserved			
9	GTC Aux Rx Error portC An aux channel error occurred during PCH GTC transfer with remote GTC sink attached to this port.			
8	GTC Update Complete portC A hardware initiated GTC update has completed with a sink attached to this port. This may be either a write of PCH GTC master to remote GTC slave or a read of the GTC of a remote master.			
7:3	Reserved <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ	
Format:	MBZ			
2	Reserved			
1	GTC Aux Rx Error portB An aux channel error occurred during PCH GTC transfer with remote GTC sink attached to this port..			

GTC PCH Interrupt Bit Definition		
	0	GTC Update Complete portB A hardware initiated GTC update has completed with a sink attached to this port. This may be either a write of PCH GTC master to remote GTC slave or a read of the GTC of a remote master.

GT Force Awake

GTFORCEAWAKE_0_2_0_GTTMMADR-GTForceAwake			
Register Space:	MMIO: 0/2/0		
Project:	BDW		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	130090h		
FLR Resettable			
DWord	Bit	Description	
0	0	Force Awake Default Value: 0b Access: R/W	
This field is no longer used. The multiple force wake mechanism has replaced it. Refer to MULTIFORCEWAKE 0xA188 register description for the usage.			

GT Function Level Reset Control Message

FLRCTLMSG - GT Function Level Reset Control Message				
Register Space: MMIO: 0/2/0				
Project: BDW				
Default Value: 0x00000000				
Size (in bits): 32				
Address: 08100h				
GT FLR Control Register				
DWord	Bit	Description		
0	31:16	<p>Message Mask</p> <table border="1"> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Message Mask In order to write to bits 15:0, the corresponding message mask bits must be written. For example, for bit 14 to be set, bit 30 needs to be 1 : 40004000</p>	Access:	RO
Access:	RO			
15:1	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Reserved</p>	Access:	RO	
Access:	RO			
0	<p>Initiate GT Function Level Reset Message</p> <table border="1"> <tr> <td>Access:</td><td>R/W Set</td></tr> </table> <p>GT Function Level Reset (FLR) 1: Initiate GT FLR - This is a Non-Posted message to reset Render, Media, Blitter and GTI-Device domains. - This bit is cleared by the CPunit upon completion of the reset.</p>	Access:	R/W Set	
Access:	R/W Set			

GT Interrupt 0 Definition

GT Interrupt 0 Definition		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	44300h-4430Fh	
Name:	GT 0 Interrupts	
ShortName:	GT_0_INTERRUPT	
Valid Projects:	BDW	
Power:	Always on	
Reset:	soft	
<p>This table indicates which events are mapped to each bit of the GT Interrupt 0 registers.</p> <p>Bits 15:0 are used for Render CS.</p> <p>Bits 31:16 are used for Blitter CS.</p> <p>The IER enabled Render Interrupt IIR (sticky) bits are ORed together to generate the Render Interrupts Pending bit in the Master Interrupt Control register.</p> <p>The IER enabled Blitter Interrupt IIR (sticky) bits are ORed together to generate the Blitter Interrupts Pending bit in the Master Interrupt Control register.</p> <p>0x44300 = ISR 0x44304 = IMR 0x44308 = IIR 0x4430C = IER</p>		
DWord	Bit	Description
0	31	Spare 31
	30	Spare 30
	29	Spare 29
	28	Spare 28
	27	BCS Wait On Semaphore
	26	Spare 26
	25	Spare 25
	24	BCS Context Switch Interrupt
	23	Spare 23
	22	Spare 22
		Project: BDW
	21	Spare 21
	20	BCS MI Flush DW Notify
	19	BCS Error Interrupt
	18	Spare 18

GT Interrupt 0 Definition

17	Spare 17	
16	BCS MI User Interrupt	
15	Spare 15	
14	Spare 14	Project: <input type="text"/> BDW
13	Spare 13	
12	Spare 12	
11	CS Wait On Semaphore	
10	CS L3 Counter Save	
9	Spare 9	Project: <input type="text"/> BDW
8	CS Context Switch Interrupt	
7	Page Fault Interrupt This interrupt is for handling Legacy Page Fault interface for all Command Streamers [BCS, RCS, VCS, VECS]. When Fault Repair Mode is enabled, Interrupt mask register value is not looked at to generate interrupt due to page fault. Please refer to vol1c "page fault support" section for more details.	
6	CS Watchdog Counter Expired	
5	L3 Parity Error	Project: <input type="text"/> BDW
4	CS PIPE_CONTROL Notify	
3	CS Error Interrupt	
2	Spare 2	
1	Reserved	
0	CS MI User Interrupt	

GT INTERRUPT 0 ENABLE REGISTER

GT_INTERRUPT0_IER - GT INTERRUPT 0 ENABLE REGISTER

Register Space: MMIO: 0/2/0

Project: BDW

Default Value: 0x00000000

Size (in bits): 32

Address: 4430Ch-4430Fh

This table indicates which events are mapped to each bit of the GT Interrupt 0 registers. Bits 15:0 are used for Render CS. Bits 31:16 are used for Blitter CS.

The IER enabled Render Interrupt IIR (sticky) bits are ORed together to generate the Render Interrupts Pending bit in the Master Interrupt Control register.

The IER enabled Blitter Interrupt IIR (sticky) bits are ORed together to generate the Blitter Interrupts Pending bit in the Master Interrupt Control register.

DWord	Bit	Description
0	31	UNUSED0 Access: R/W
	30	UNUSED1 Access: R/W
	29	UNUSED2 Access: R/W
	28	UNUSED3 Access: R/W
	27	BCS_WAIT_ON_SEMAPHORE Access: R/W BCS wait on semaphore
	26	UNUSED4 Access: R/W
	25	UNUSED5 Access: R/W
	24	BCS_CTX_SWITCH_INTERRUPT Access: R/W BCS context switch interrupt
	23	UNUSED6 Access: R/W
	22	UNUSED7 Access: R/W

GT_INTERRUPT0_IER - GT INTERRUPT 0 ENABLE REGISTER

	21	UNUSED8	Access:	R/W
	20	BCS_MI_FLUSH_DWNOTIFY	Access:	R/W
		BCS MI flush DW notify		
	19	BCS_ERROR_INTERRUPT	Access:	R/W
		BCS error interrupt		
	18	UNUSED9	Access:	R/W
	17	UNUSED10	Access:	R/W
	16	BCS_MI_USER_INTERRUPT	Access:	R/W
		BCS MI user interrupt		
	15	UNUSED11	Access:	R/W
	14	UNUSED12	Access:	R/W
	13	UNUSED13	Access:	R/W
	12	UNUSED14	Access:	R/W
	11	CS_WAIT_ON_SEMAPHORE	Access:	R/W
		CS wait on semaphore		
	10	CS_L3_COUNTER_SAVE	Access:	R/W
		CS L3 counter save		
	9	UNUSED15	Access:	R/W
	8	CS_CTX_SWITCH_INTERRUPT	Access:	R/W
		CS context switch interrupt		

GT_INTERRUPTO_IER - GT INTERRUPT 0 ENABLE REGISTER

	PAGE_FAULT_ERROR
7	Access: R/W this interrupt is for handling legacy page fault interface for all command streamer (BCS, VCS, RCS, VECS). when fault repair mode is enabled, interrupt mask register value is not looked at to generate interrupt due to page fault. please refer to vol1c BDW 'page fault support' section for more details.
CS_WATCHDOG_COUNTER_EXPIRED	
6	Access: R/W CS watchdog counter expired
L3PARITYERROR	
5	Access: R/W L3 parity error
CS_PIPE_CONTROL_NOTIFY	
4	Access: R/W CS pipe control notify
CS_ERROR_INTERRUPT	
3	Access: R/W CS error interrupt
UNUSED17	
2	Access: R/W
Reserved	
CS_MI_USER_INTERRUPT	
0	Access: R/W CS context switch interrupt

GT INTERRUPT 0 IDENTITY REGISTER

GT_INTERRUPT0_IIR - GT INTERRUPT 0 IDENTITY REGISTER		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	44308h-4430Bh	
<p>This table indicates which events are mapped to each bit of the GT Interrupt 0 registers. Bits 15:0 are used for Render CS. Bits 31:16 are used for Blitter CS.</p> <p>The IER enabled Render Interrupt IIR (sticky) bits are ORed together to generate the Render Interrupts Pending bit in the Master Interrupt Control register.</p> <p>The IER enabled Blitter Interrupt IIR (sticky) bits are ORed together to generate the Blitter Interrupts Pending bit in the Master Interrupt Control register.</p>		
DWord	Bit	Description
0	31	UNUSED0
	Access:	R/W One Clear
	30	UNUSED1
	Access:	R/W One Clear
	29	UNUSED2
	Access:	R/W One Clear
	28	UNUSED3
	Access:	R/W One Clear
	27	BCS_WAIT_ON_SEMAPHORE
	Access:	R/W One Clear
BCS wait on semaphore		
0	26	UNUSED4
	Access:	R/W One Clear
	25	UNUSED5
	Access:	R/W One Clear
	24	BCS_CTX_SWITCH_INTERRUPT
	Access:	R/W One Clear
	BCS context switch interrupt	
	23	UNUSED6
	Access:	R/W One Clear
	22	UNUSED7
Access:		
R/W One Clear		

GT_INTERRUPT0_IIR - GT INTERRUPT 0 IDENTITY REGISTER

	21 UNUSED8
	Access: R/W One Clear
	20 BCS_MI_FLUSH_DWNNOTIFY
	Access: R/W One Clear
	BCS MI flush DW notify
	19 BCS_ERROR_INTERRUPT
	Access: R/W One Clear
	BCS error interrupt
	18 UNUSED9
	Access: R/W One Clear
	17 UNUSED10
	Access: R/W One Clear
	16 BCS_MI_USER_INTERRUPT
	Access: R/W One Clear
	BCS MI user interrupt
	15 UNUSED11
	Access: R/W One Clear
	14 UNUSED12
	Access: R/W One Clear
	13 UNUSED13
	Access: R/W One Clear
	12 UNUSED14
	Access: R/W One Clear
	11 CS_WAIT_ON_SEMAPHORE
	Access: R/W One Clear
	CS wait on semaphore
	10 CS_L3_COUNTER_SAVE
	Access: R/W One Clear
	CS L3 counter save
	9 UNUSED15
	Access: R/W One Clear
	8 CS_CTX_SWITCH_INTERRUPT
	Access: R/W One Clear
	CS context switch interrupt

GT_INTERRUPT0_IIR - GT INTERRUPT 0 IDENTITY REGISTER

	PAGE_FAULT_ERROR		
7	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px;">R/W One Clear</td> </tr> </table> <p>this interrupt is for handling legacy page fault interface for all command streamer (BCS, VCS, RCS, VECS). when fault repair mode is enabled, interrupt mask register value is not looked at to generate interrupt due to page fault. please refer to vol1c BDW 'page fault support' section for more details.</p>	Access:	R/W One Clear
Access:	R/W One Clear		
CS_WATCHDOG_COUNTER_EXPIRED			
6	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px;">R/W One Clear</td> </tr> </table> <p>CS watchdog counter expired</p>	Access:	R/W One Clear
Access:	R/W One Clear		
L3PARITYERROR			
5	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px;">R/W One Clear</td> </tr> </table> <p>L3 parity error</p>	Access:	R/W One Clear
Access:	R/W One Clear		
CS_PIPE_CONTROL_NOTIFY			
4	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px;">R/W One Clear</td> </tr> </table> <p>CS pipe control notify</p>	Access:	R/W One Clear
Access:	R/W One Clear		
CS_ERROR_INTERRUPT			
3	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px;">R/W One Clear</td> </tr> </table> <p>CS error interrupt</p>	Access:	R/W One Clear
Access:	R/W One Clear		
UNUSED17			
2	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px;">R/W One Clear</td> </tr> </table>	Access:	R/W One Clear
Access:	R/W One Clear		
Reserved			
CS_MI_USER_INTERRUPT			
0	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px;">R/W One Clear</td> </tr> </table> <p>CS context switch interrupt</p>	Access:	R/W One Clear
Access:	R/W One Clear		

GT INTERRUPT 0 MASK REGISTER

GT_INTERRUPT0_IMR - GT INTERRUPT 0 MASK REGISTER		
DWord	Bit	Description
0	31	UNUSED0 Access: R/W
	30	UNUSED1 Access: R/W
	29	UNUSED2 Access: R/W
	28	UNUSED3 Access: R/W
	27	BCS_WAIT_ON_SEMAPHORE Default Value: 1b Access: R/W BCS wait on semaphore
	26	UNUSED4 Access: R/W
	25	UNUSED5 Access: R/W
	24	BCS_CTX_SWITCH_INTERRUPT Default Value: 1b Access: R/W BCS context switch interrupt
	23	UNUSED6 Access: R/W

GT_INTERRUPT0_IMR - GT INTERRUPT 0 MASK REGISTER

	22	UNUSED7	Access:	R/W
	21	UNUSED8	Access:	R/W
	20	BCS_MI_FLUSH_DWNOTIFY	Default Value:	1b
			Access:	R/W
			BCS MI flush DW notify	
	19	BCS_ERROR_INTERRUPT	Default Value:	1b
			Access:	R/W
			BCS error interrupt	
	18	UNUSED9	Access:	R/W
	17	UNUSED10	Access:	R/W
	16	BCS_MI_USER_INTERRUPT	Default Value:	1b
			Access:	R/W
			BCS MI user interrupt	
	15	UNUSED11	Access:	R/W
	14	UNUSED12	Access:	R/W
	13	UNUSED13	Access:	R/W
	12	UNUSED14	Access:	R/W
	11	CS_WAIT_ON_SEMAPHORE	Default Value:	1b
			Access:	R/W
			CS wait on semaphore	

GT_INTERRUPTO_IMR - GT INTERRUPT 0 MASK REGISTER

	10	CS_L3_COUNTER_SAVE		
		Default Value:	1b	
		Access:	R/W	
CS L3 counter save				
	9	UNUSED15		
		Access:	R/W	
	8	CS_CTX_SWITCH_INTERRUPT		
		Default Value:	1b	
		Access:	R/W	
CS context switch interrupt				
	7	PAGE_FAULT_ERROR		
		Default Value:	1b	
		Access:	R/W	
this interrupt is for handling legacy page fault interface for all command streamer (BCS, VCS, RCS, VECS). when fault repair mode is enabled, interrupt mask register value is not looked at to generate interrupt due to page fault. please refer to vol1c BDW 'page fault support' section for more details.				
	6	CS_WATCHDOG_COUNTER_EXPIRED		
		Default Value:	1b	
		Access:	R/W	
CS watchdog counter expired				
	5	L3PARITYERROR		
		Default Value:	1b	
		Access:	R/W	
L3 parity error				
	4	CS_PIPE_CONTROL_NOTIFY		
		Default Value:	1b	
		Access:	R/W	
CS pipe control notify				
	3	CS_ERROR_INTERRUPT		
		Default Value:	1b	
		Access:	R/W	
CS error interrupt				

GT_INTERRUPT0_IMR - GT INTERRUPT 0 MASK REGISTER			
	2	UNUSED17	
		Access:	R/W
	1	Reserved	
	0	CS_MI_USER_INTERRUPT	
		Default Value:	1b
		Access:	R/W
CS context switch interrupt			

GT INTERRUPT 0 STATUS REGISTER

GT_INTERRUPT0_ISR - GT INTERRUPT 0 STATUS REGISTER

Register Space: MMIO: 0/2/0

Project: BDW

Default Value: 0x00000000

Size (in bits): 32

Address: 44300h-44303h

This table indicates which events are mapped to each bit of the GT Interrupt 0 registers. Bits 15:0 are used for Render CS. Bits 31:16 are used for Blitter CS.

The IER enabled Render Interrupt IIR (sticky) bits are ORed together to generate the Render Interrupts Pending bit in the Master Interrupt Control register.

The IER enabled Blitter Interrupt IIR (sticky) bits are ORed together to generate the Blitter Interrupts Pending bit in the Master Interrupt Control register.

DWord	Bit	Description
0	31	UNUSED0 Access: RO
	30	UNUSED1 Access: RO
	29	UNUSED2 Access: RO
	28	UNUSED3 Access: RO
	27	BCS_WAIT_ON_SEMAPHORE Access: RO BCS wait on semaphore
	26	UNUSED4 Access: RO
	25	UNUSED5 Access: RO
	24	BCS_CTX_SWITCH_INTERRUPT Access: RO BCS context switch interrupt
	23	UNUSED6 Access: RO
	22	UNUSED7 Access: RO

GT_INTERRUPT0_ISR - GT INTERRUPT 0 STATUS REGISTER

	21	UNUSED8	Access:	RO
	20	BCS_MI_FLUSH_DWNNOTIFY	Access:	RO
		BCS MI flush DW notify		
	19	BCS_ERROR_INTERRUPT	Access:	RO
		BCS error interrupt		
	18	UNUSED9	Access:	RO
	17	UNUSED10	Access:	RO
	16	BCS_MI_USER_INTERRUPT	Access:	RO
		BCS MI user interrupt		
	15	UNUSED11	Access:	RO
	14	UNUSED12	Access:	RO
	13	UNUSED13	Access:	RO
	12	UNUSED14	Access:	RO
	11	CS_WAIT_ON_SEMAPHORE	Access:	RO
		CS wait on semaphore		
	10	CS_L3_COUNTER_SAVE	Access:	RO
		CS L3 counter save		
	9	UNUSED15	Access:	RO

GT_INTERRUPT0_ISR - GT INTERRUPT 0 STATUS REGISTER

	8	CS_CTX_SWITCH_INTERRUPT	Access:	RO
		CS context switch interrupt		
	7	PAGE_FAULT_ERROR	Access:	RO
		this interrupt is for handling legacy page fault interface for all command streamer (BCS, VCS, RCS, VECS). when fault repair mode is enabled, interrupt mask register value is not looked at to generate interrupt due to page fault. please refer to vol1c BDW 'page fault support' section for more details.		
	6	CS_WATCHDOG_COUNTER_EXPIRED	Access:	RO
		CS watchdog counter expired		
	5	L3PARITYERROR	Access:	RO
		L3 parity error		
	4	CS_PIPE_CONTROL_NOTIFY	Access:	RO
		CS pipe control notify		
	3	CS_ERROR_INTERRUPT	Access:	RO
		CS error interrupt		
	2	UNUSED17	Access:	RO
	1	Reserved		
	0	CS_MI_USER_INTERRUPT	Access:	RO
		CS context switch interrupt		

GT Interrupt 1 Definition

GT Interrupt 1 Definition		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	44310h-4431Fh	
Name:	GT 1 Interrupts	
ShortName:	GT_1_INTERRUPT	
Valid Projects:	BDW	
Power:	Always on	
Reset:	soft	
This table indicates which events are mapped to each bit of the GT Interrupt 1 registers. Bits 15:0 are used for VCS1. Bits 31:16 are used for VCS2. The VCS1 Interrupt IIR (sticky) bits are ORed together to generate the VCS1 Interrupts Pending bit in the Master Interrupt Control register. The VCS2 Interrupt IIR (sticky) bits are ORed together to generate the VCS2 Interrupts Pending bit in the Master Interrupt Control register. 0x44310 = ISR 0x44314 = IMR 0x44318 = IIR 0x4431C = IER		
DWord	Bit	Description
0	31	Spare 31
	30	Spare 30
	29	Spare 29
	28	Spare 28
	27	VCS2 Wait On Semaphore
	26	Spare 26
	25	Reserved
		Project: BDW
	24	VCS2 Context Switch Interrupt
	23	Spare 23
	22	VCS2 Watchdog Counter Expired
	21	Reserved
	20	VCS2 MI Flush DW Notify
	19	VCS2 Error Interrupt
	18	Spare 18

GT Interrupt 1 Definition		
	17	Spare 17
	16	VCS2 MI User Interrupt
	15	Spare 15
	14	Spare 14
	13	Spare 13
	12	Spare 12
	11	VCS1 Wait On Semaphore
	10	Spare 10
	9	Reserved
		Project: BDW
	8	VCS1 Context Switch Interrupt
	7	Spare 7
	6	VCS1 Watchdog Counter Expired
	5	Reserved
	4	VCS1 MI Flush DW Notify
	3	VCS1 Error Interrupt
	2	Spare 2
	1	Spare 1
	0	VCS1 MI User Interrupt

GT INTERRUPT1 ENABLE REGISTER

GT_INTERRUPT1_IER - GT INTERRUPT1 ENABLE REGISTER		
DWord	Bit	Description
0	31	UNUSED0 Access: R/W
	30	UNUSED1 Access: R/W
	29	UNUSED2 Access: R/W
	28	UNUSED3 Access: R/W
	27	VCS2_WAIT_ON_SEMAPHORE Access: R/W VCS2 wait on semaphore
	26	UNUSED4 Access: R/W
	25	Reserved
	24	VCS2_CTX_SWITCH_INTERRUPT Access: R/W VCS2 context switch interrupt
	23	UNUSED5 Access: R/W
	22	VCS2_WATCHDOG_COUNTER_EXPIRED Access: R/W VCS2 watchdog counter expired

GT_INTERRUPT1_IER - GT INTERRUPT1 ENABLE REGISTER

	21	Reserved	
	20	VCS2_MI_FLUSH_DWNOTIFY	
		Access:	R/W
		VCS2 MI flush DW notify	
	19	VCS2_ERROR_INTERRUPT	
		Access:	R/W
		VCS2 error interrupt	
	18	UNUSED6	
		Access:	R/W
	17	UNUSED7	
		Access:	R/W
	16	VCS2_MI_USER_INTERRUPT	
		Access:	R/W
		VCS2 MI user interrupt	
	15	UNUSED8	
		Access:	R/W
	14	UNUSED9	
		Access:	R/W
	13	UNUSED10	
		Access:	R/W
	12	UNUSED11	
		Access:	R/W
	11	VCS1_WAIT_ON_SEMAPHORE	
		Access:	R/W
		VCS1 wait on semaphore	
	10	UNUSED12	
		Access:	R/W
	9	Reserved	
	8	VCS1_CTX_SWITCH_INTERRUPT	
		Access:	R/W
		VCS1 context switch interrupt	
	7	UNUSED13	
		Access:	R/W

GT_INTERRUPT1_IER - GT INTERRUPT1 ENABLE REGISTER

	6	VCS1_WATCHDOG_COUNTER_EXPIRED
		Access: R/W VCS1 watchdog counter expired
	5	Reserved
	4	VCS1_MI_FLUSH_DWNOTIFY
		Access: R/W VCS1 MI flush DW notify
	3	VCS1_ERROR_INTERRUPT
		Access: R/W VCS1 error interrupt
	2	UNUSED14
		Access: R/W
	1	UNUSED15
		Access: R/W
	0	VCS1_MI_USER_INTERRUPT
		Access: R/W VCS1 MI user interrupt

GT INTERRUPT1 IDENTITY REGISTER

GT_INTERRUPT1_IIR - GT INTERRUPT1 IDENTITY REGISTER

Register Space: MMIO: 0/2/0

Project: BDW

Default Value: 0x00000000

Size (in bits): 32

Address: 44318h-4431Bh

This table indicates which events are mapped to each bit of the GT Interrupt 0 registers. Bits 15:0 are used for VCS1. Bits 31:16 are used for VCS2.

The IER enabled VCS1 Interrupt IIR (sticky) bits are ORed together to generate the VCS1 Interrupts Pending bit in the Master Interrupt Control register.

The IER enabled VCS2 Interrupt IIR (sticky) bits are ORed together to generate the VCS2 Interrupt Pending bit in the Master Interrupt Control register.

DWord	Bit	Description
0	31	UNUSED0 Access: R/W One Clear
	30	UNUSED1 Access: R/W One Clear
	29	UNUSED2 Access: R/W One Clear
	28	UNUSED3 Access: R/W One Clear
	27	VCS2_WAIT_ON_SEMAPHORE Access: R/W One Clear VCS2 wait on semaphore
	26	UNUSED4 Access: R/W One Clear
	25	Reserved
	24	VCS2_CTX_SWITCH_INTERRUPT Access: R/W One Clear VCS2 context switch interrupt
	23	UNUSED5 Access: R/W One Clear
	22	VCS2_WATCHDOG_COUNTER_EXPIRED Access: R/W One Clear VCS2 watchdog counter expired

GT_INTERRUPT1_IIR - GT INTERRUPT1 IDENTITY REGISTER

	21	Reserved	
	20	VCS2_MI_FLUSH_DWNOTIFY	
		Access:	R/W One Clear
		VCS2 MI flush DW notify	
	19	VCS2_ERROR_INTERRUPT	
		Access:	R/W One Clear
		VCS2 error interrupt	
	18	UNUSED6	
		Access:	R/W One Clear
	17	UNUSED7	
		Access:	R/W One Clear
	16	VCS2_MI_USER_INTERRUPT	
		Access:	R/W One Clear
		VCS2 MI user interrupt	
	15	UNUSED8	
		Access:	R/W One Clear
	14	UNUSED9	
		Access:	R/W One Clear
	13	UNUSED10	
		Access:	R/W One Clear
	12	UNUSED11	
		Access:	R/W One Clear
	11	VCS1_WAIT_ON_SEMAPHORE	
		Access:	R/W One Clear
		VCS1 wait on semaphore	
	10	UNUSED12	
		Access:	R/W One Clear
	9	Reserved	
	8	VCS1_CTX_SWITCH_INTERRUPT	
		Access:	R/W One Clear
		VCS1 context switch interrupt	
	7	UNUSED13	
		Access:	R/W One Clear

GT_INTERRUPT1_IIR - GT INTERRUPT1 IDENTITY REGISTER

	6	VCS1_WATCHDOG_COUNTER_EXPIRED		
		<table border="1"> <tr> <td>Access:</td> <td>R/W One Clear</td> </tr> </table> <p>VCS1 watchdog counter expired</p>	Access:	R/W One Clear
Access:	R/W One Clear			
	5	Reserved		
	4	VCS1_MI_FLUSH_DWNOTIFY		
		<table border="1"> <tr> <td>Access:</td> <td>R/W One Clear</td> </tr> </table> <p>VCS1 MI flush DW notify</p>	Access:	R/W One Clear
Access:	R/W One Clear			
	3	VCS1_ERROR_INTERRUPT		
		<table border="1"> <tr> <td>Access:</td> <td>R/W One Clear</td> </tr> </table> <p>VCS1 error interrupt</p>	Access:	R/W One Clear
Access:	R/W One Clear			
	2	UNUSED14		
		<table border="1"> <tr> <td>Access:</td> <td>R/W One Clear</td> </tr> </table>	Access:	R/W One Clear
Access:	R/W One Clear			
	1	UNUSED15		
		<table border="1"> <tr> <td>Access:</td> <td>R/W One Clear</td> </tr> </table>	Access:	R/W One Clear
Access:	R/W One Clear			
	0	VCS1_MI_USER_INTERRUPT		
		<table border="1"> <tr> <td>Access:</td> <td>R/W One Clear</td> </tr> </table> <p>VCS1 MI user interrupt</p>	Access:	R/W One Clear
Access:	R/W One Clear			

GT INTERRUPT1 MASK REGISTER

GT_INTERRUPT1_IMR - GT INTERRUPT1 MASK REGISTER		
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x09590959 Size (in bits): 32		
Address: 44314h-44317h		
This table indicates which events are mapped to each bit of the GT Interrupt 0 registers. Bits 15:0 are used for VCS1. Bits 31:16 are used for VCS2. The IER enabled VCS1 Interrupt IIR (sticky) bits are ORed together to generate the VCS1 Interrupt Pending bit in the Master Interrupt Control register. The IER enabled VCS2 Interrupt IIR (sticky) bits are ORed together to generate the VCS2 Interrupt Pending bit in the Master Interrupt Control register.		
DWord	Bit	Description
0	31	UNUSED0 Access: R/W
	30	UNUSED1 Access: R/W
	29	UNUSED2 Access: R/W
	28	UNUSED3 Access: R/W
	27	VCS2_WAIT_ON_SEMAPHORE Default Value: 1b Access: R/W VCS2 wait on semaphore
	26	UNUSED4 Access: R/W
	25	Reserved
	24	VCS2_CTX_SWITCH_INTERRUPT Default Value: 1b Access: R/W VCS2 context switch interrupt
	23	UNUSED5 Access: R/W

GT_INTERRUPT1_IMR - GT INTERRUPT1 MASK REGISTER

	22	VCS2_WATCHDOG_COUNTER_EXPIRED
		Default Value:
		Access:
		VCS2 watchdog counter expired
	21	Reserved
	20	VCS2_MI_FLUSH_DWNOTIFY
		Default Value:
		Access:
		VCS2 MI flush DW notify
	19	VCS2_ERROR_INTERRUPT
		Default Value:
		Access:
		VCS2 error interrupt
	18	UNUSED6
		Access:
	17	UNUSED7
		Access:
	16	VCS2_MI_USER_INTERRUPT
		Default Value:
		Access:
		VCS2 MI user interrupt
	15	UNUSED8
		Access:
	14	UNUSED9
		Access:
	13	UNUSED10
		Access:
	12	UNUSED11
		Access:
	11	VCS1_WAIT_ON_SEMAPHORE
		Default Value:
		Access:
		VCS1 wait on semaphore

GT_INTERRUPT1_IMR - GT INTERRUPT1 MASK REGISTER		
10	UNUSED12	
	Access:	R/W
9	Reserved	
8	VCS1_CTX_SWITCH_INTERRUPT	
	Default Value:	1b
	Access:	R/W
	VCS1 context switch interrupt	
7	UNUSED13	
	Access:	R/W
6	VCS1_WATCHDOG_COUNTER_EXPIRED	
	Default Value:	1b
	Access:	R/W
	VCS1 watchdog counter expired	
5	Reserved	
4	VCS1_MI_FLUSH_DWNOTIFY	
	Default Value:	1b
	Access:	R/W
	VCS1 MI flush DW notify	
3	VCS1_ERROR_INTERRUPT	
	Default Value:	1b
	Access:	R/W
	VCS1 error interrupt	
2	UNUSED14	
	Access:	R/W
1	UNUSED15	
	Access:	R/W
0	VCS1_MI_USER_INTERRUPT	
	Default Value:	1b
	Access:	R/W
	VCS1 MI user interrupt	

GT INTERRUPT1 STATUS REGISTER

GT_INTERRUPT1_ISR - GT INTERRUPT1 STATUS REGISTER		
DWord	Bit	Description
0	31	UNUSED0 Access: RO
	30	UNUSED1 Access: RO
	29	UNUSED2 Access: RO
	28	UNUSED3 Access: RO
	27	VCS2_WAIT_ON_SEMAPHORE Access: RO VCS2 wait on semaphore
	26	UNUSED4 Access: RO
	25	Reserved
	24	VCS2_CTX_SWITCH_INTERRUPT Access: RO VCS2 context switch interrupt
	23	UNUSED5 Access: RO
	22	VCS2_WATCHDOG_COUNTER_EXPIRED Access: RO VCS2 watchdog counter expired

GT_INTERRUPT1_ISR - GT INTERRUPT1 STATUS REGISTER

	21	Reserved	
	20	VCS2_MI_FLUSH_DWNOTIFY	
		Access:	RO
		VCS2 MI flush DW notify	
	19	VCS2_ERROR_INTERRUPT	
		Access:	RO
		VCS2 error interrupt	
	18	UNUSED6	
		Access:	RO
	17	UNUSED7	
		Access:	RO
	16	VCS2_MI_USER_INTERRUPT	
		Access:	RO
		VCS2 MI user interrupt	
	15	UNUSED8	
		Access:	RO
	14	UNUSED9	
		Access:	RO
	13	UNUSED10	
		Access:	RO
	12	UNUSED11	
		Access:	RO
	11	VCS1_WAIT_ON_SEMAPHORE	
		Access:	RO
		VCS1 wait on semaphore	
	10	UNUSED12	
		Access:	RO
	9	Reserved	
	8	VCS1_CTX_SWITCH_INTERRUPT	
		Access:	RO
		VCS1 context switch interrupt	
	7	UNUSED13	
		Access:	RO

GT_INTERRUPT1_ISR - GT INTERRUPT1 STATUS REGISTER

	6	VCS1_WATCHDOG_COUNTER_EXPIRED	
		Access:	RO
		VCS1 watchdog counter expired	
	5	Reserved	
	4	VCS1_MI_FLUSH_DWNOTIFY	
		Access:	RO
		VCS1 MI flush DW notify	
	3	VCS1_ERROR_INTERRUPT	
		Access:	RO
		VCS1 error interrupt	
	2	UNUSED14	
		Access:	RO
	1	UNUSED15	
		Access:	RO
	0	VCS1_MI_USER_INTERRUPT	
		Access:	RO
		VCS1 MI user interrupt	

GT Interrupt 2 Definition

GT Interrupt 2 Definition		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	44320h-4432Fh	
Name:	GT 2 Interrupts	
ShortName:	GT_2_INTERRUPT	
Valid Projects:	BDW	
Power:	Always on	
Reset:	soft	
This table indicates which events are mapped to each bit of the GT Interrupt 2 registers. Bits 15:0 are used for GTPM. The IER enabled GTPM Interrupt IIR (sticky) bits are ORed together to generate the GTPM Interrupts Pending bit in the Master Interrupt Control register. 0x44320 = ISR 0x44324 = IMR 0x44328 = IIR 0x4432C = IER		
DWord	Bit	Description
0	31	Reserved
	30	Reserved
	29	Reserved
	28	Reserved
	27	Reserved
	26	Reserved
	25	Reserved
	24	Reserved
	23	Reserved
	22	Reserved
	21	Reserved
	20	Reserved
	19	Reserved
	18	Reserved
	17	Reserved
	16	Reserved
	15	Spare 15

GT Interrupt 2 Definition

	14	Spare 14
	13	Unslice Frequency Control Up Interrupt
	12	Unslice Frequency Control Down Interrupt
	11	NFADFL Frequency Up Interrupt
	10	NFADFL Frequency Down Interrupt
	9	Reserved
	8	GTPM Engines Idle Interrupt
	7	GTPM Uncore to Core Trap Interrupt
	6	GTPM Render Frequency Downwards Timeout During RC6 Interrupt
	5	GTPM Render P-State Up Threshold Interrupt
	4	GTPM Render P-State Down Threshold Interrupt
	3	Spare 3
	2	GTPM Render Geyserville Up Evaluation Interval Interrupt
	1	GTPM Render Geyserville Down Evaluation Interval Interrupt
	0	Spare 0

GT Interrupt 3 Definition

GT Interrupt 3 Definition		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	44330h-4433Fh	
Name:	GT 3 Interrupts	
ShortName:	GT_3_INTERRUPT	
Valid Projects:	BDW	
Power:	Always on	
Reset:	soft	
This table indicates which events are mapped to each bit of the GT Interrupt 3 registers. Bits 15:0 are used for VEBox. Bits 31:28 are used for OACS. The VEBox Interrupt IIR (sticky) bits are ORed together to generate the VEBox Interrupts Pending bit in the Master Interrupt Control register. 0x44330 = ISR 0x44334 = IMR 0x44338 = IIR 0x4433C = IER		
DWord	Bit	Description
0	31	Spare 31
	30	Spare 30
	29	Spare 29
	28	Performance Monitoring Buffer Half-Full Interrupt For internal trigger (timer event based) reporting, this interrupt is generated if the report buffer crosses the half full limit.
	27	Spare 27
	26	Spare 26
	25	Spare 25
	24	Spare 24
	23	Spare 23
	22	Spare 22
	21	Spare 21 Project: BDW
	20	Spare 20 Project: BDW
	19	Spare 19

GT Interrupt 3 Definition

	18	Spare 18
	17	Reserved
	16	Reserved
	15	Spare 15
	14	Spare 14
	13	Spare 13
	12	Spare 12
	11	VECS Wait On Semaphore
	10	Spare 10
	9	Spare 9
	8	VECS Context Switch Interrupt
	7	Spare 7
	6	Spare 6 Project: <input type="text"/> BDW
	5	Spare 5
	4	VECS MI Flush DW Notify
	3	VECS Error Interrupt
	2	Spare 2
	1	Spare 1
	0	VECS MI User Interrupt

GT INTERRUPT3 ENABLE REGISTER

GT_INTERRUPT3_IER - GT INTERRUPT3 ENABLE REGISTER		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	4433Ch-4433Fh	
This table indicates which events are mapped to each bit of the GT interrupt 3 register. Bits 15:0 are VEDBOX and bits 31:28 ARE OACS. The VEDBOX Interrupt IIR sticky bits are ORed together to generate VEDBOX interrupt pending bit in the master interrupt control register.		
DWord	Bit	Description
0	31:29	UNUSED0 Access: R/W
	28	Reserved
	27:17	UNUSED1 Access: R/W
	16	Reserved
	15:12	UNUSED2 Access: R/W
	11	VECS_WAIT_SEMAPHORE Access: R/W VECS wait on semaphore
	10:9	UNUSED3 Access: R/W
	8	VECS_CTX_SWITCH_INT Access: R/W VECS context switch interrupt
	7:5	UNUSED4 Access: R/W
	4	VECS_MI_FLUSH_DWNNOTIFY Access: R/W VECS MI Flush DW Notify
	3	VECS_ERR_INT Access: R/W VECS error interrupt

GT_INTERRUPT3_IER - GT INTERRUPT3 ENABLE REGISTER

	2:1	UNUSED5
		Access: R/W
	0	VECS_MI_USER_INT
		Access: R/W VECS MI user interrupt

GT INTERRUPT3 IDENTITY REGISTER

GT_INTERRUPT3_IIR - GT INTERRUPT3 IDENTITY REGISTER

Register Space: MMIO: 0/2/0

Project: BDW

Default Value: 0x00000000

Size (in bits): 32

Address: 44338h-4433Bh

This table indicates which events are mapped to each bit of the GT interrupt 3 register.

Bits 15:0 are VEDBOX and Bits 31:28 ARE OACS. the VEDBOX Interrupt IIR sticky bits are Ored together to generate VEDBOX interrupt pending bit in the master interrupt control register.

DWord	Bit	Description
0	31:29	UNUSED0 Access: R/W One Clear
	28	Reserved
	27:17	UNUSED1 Access: R/W One Clear
	16	Reserved
	15:12	UNUSED2 Access: R/W One Clear
	11	VECS_WAIT_SEMAPHORE Access: R/W One Clear VECS wait on semaphore
	10:9	UNUSED3 Access: R/W One Clear
	8	VECS_CTX_SWITCH_INT Access: R/W One Clear VECS context switch interrupt
	7:5	UNUSED4 Access: R/W One Clear
	4	VECS_MI_FLUSH_DWNNOTIFY Access: R/W One Clear VECS MI Flush DW Notify
	3	VECS_ERR_INT Access: R/W One Clear VECS error interrupt

GT_INTERRUPT3_IIR - GT INTERRUPT3 IDENTITY REGISTER

	2:1	UNUSED5
		Access: R/W One Clear
	0	VECS_MI_USER_INT
		Access: R/W One Clear VECS MI user interrupt

GT INTERRUPT3 MASK REGISTER

GT_INTERRUPT3_IMR - GT INTERRUPT3 MASK REGISTER		
DWord	Bit	Description
0	31:29	UNUSED0
		Access: R/W
	28	Reserved
	27:17	UNUSED1
		Access: R/W
	16	Reserved
	15:12	UNUSED2
		Access: R/W
	11	VECS_WAIT_SEMAPHORE
		Default Value: 1b
		Access: R/W
		VECS wait on semaphore
10:9	10:9	UNUSED3
		Access: R/W
	8	VECS_CTX_SWITCH_INT
		Default Value: 1b
7:5	7:5	UNUSED4
		Access: R/W
	4	VECS_MI_FLUSH_DWNNOTIFY
		Default Value: 1b
		Access: R/W
		VECS MI Flush DW Notify

GT_INTERRUPT3_IMR - GT INTERRUPT3 MASK REGISTER

	3	VECS_ERR_INT
		Default Value: 1b Access: R/W VECS error interrupt
	2:1	UNUSED5
		Access: R/W
	0	VECS_MI_USER_INT
		Default Value: 1b Access: R/W VECS MI user interrupt

GT INTERRUPT3 STATUS REGISTER

GT_INTERRUPT3_ISR - GT INTERRUPT3 STATUS REGISTER		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	44330h-44333h	
This table indicates which events are mapped to each bit of the GT interrupt 3 register. Bits 15:0 are VEDBOX and Bits 31:28 ARE OACS. the VEDBOX Interrupt IIR sticky bits are Ored together to generate VEDBOX interrupt pending bit in the master interrupt control register.		
DWord	Bit	Description
0	31:29	UNUSED0 Access: RO
	28	Reserved
	27:17	UNUSED1 Access: RO
	16	Reserved
	15:12	UNUSED2 Access: RO
	11	VECS_WAIT_SEMAPHORE Access: RO VECS wait on semaphore
	10:9	UNUSED3 Access: RO
	8	VECS_CTX_SWITCH_INT Access: RO VECS context switch interrupt
	7:5	UNUSED4 Access: RO
	4	VECS_MI_FLUSH_DWNNOTIFY Access: RO VECS MI Flush DW Notify
	3	VECS_ERR_INT Access: RO VECS error interrupt

GT_INTERRUPT3_ISR - GT INTERRUPT3 STATUS REGISTER

	2:1	UNUSED5
		Access: RO
	0	VECS_MI_USER_INT
		Access: RO VECS MI user interrupt

GT Mode Register

GT_MODE - GT Mode Register													
Register Space: MMIO: 0/2/0 Project: BDW Source: RenderCS Default Value: 0x00000000 [BDW] Access: R/W Size (in bits): 32 Trusted Type: 1													
Address: 07008h Valid Projects: [BDW]													
This Register is used to control the 6EU and 12EU configuration for GT. Writing 0x01FF01FF to this register enables the 6EU mode.													
DWord	Bit	Description											
0	31:16	Mask <table border="1"> <tr> <td>Access:</td><td>WO</td></tr> <tr> <td>Format:</td><td>Mask[15:0]</td></tr> </table> <p>Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)</p>	Access:	WO	Format:	Mask[15:0]							
Access:	WO												
Format:	Mask[15:0]												
EU Local Thread Checking Enable <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>r/w</td></tr> </table> <p>This field configures the EU local thread checking. If enable the stateless access will be checked against the local thread's scratch space size and start address.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0h</td><td>Disable [Default]</td><td>EU local thread checking is disabled.</td></tr> <tr> <td>1h</td><td>Enable</td><td>EU local thread checking is enabled.</td></tr> </tbody> </table>	Project:	BDW	Access:	r/w	Value	Name	Description	0h	Disable [Default]	EU local thread checking is disabled.	1h	Enable	EU local thread checking is enabled.
Project:	BDW												
Access:	r/w												
Value	Name	Description											
0h	Disable [Default]	EU local thread checking is disabled.											
1h	Enable	EU local thread checking is enabled.											
14:13	SFR mode <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>r/w</td></tr> <tr> <td>Format:</td><td>U2</td></tr> </table> <p>This field must be zero when not in GT4(SFR) configuration i.e GTB_rendermode fuse set to SFR.</p>	Project:	BDW	Access:	r/w	Format:	U2						
Project:	BDW												
Access:	r/w												
Format:	U2												
Reserved <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>r/w</td></tr> <tr> <td>Format:</td><td>PBC</td></tr> </table>	Project:	BDW	Access:	r/w	Format:	PBC							
Project:	BDW												
Access:	r/w												
Format:	PBC												
11	Reserved												

GT_MODE - GT Mode Register

	10	16X16 Cross Slice Hash Disable															
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>r/w</td></tr> <tr> <td>Format:</td><td>U1</td></tr> </table> <p>This field allows to control pixel block hashing across slices.</p>	Project:	BDW	Access:	r/w	Format:	U1									
Project:	BDW																
Access:	r/w																
Format:	U1																
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0h</td><td>Enable [Default]</td><td>16X16 Checkerboard hashing enabled across slices</td></tr> <tr> <td>1h</td><td>Disable</td><td>16X16 Checkerboard hashing disabled across slices</td></tr> </tbody> </table>	Value	Name	Description	0h	Enable [Default]	16X16 Checkerboard hashing enabled across slices	1h	Disable	16X16 Checkerboard hashing disabled across slices						
Value	Name	Description															
0h	Enable [Default]	16X16 Checkerboard hashing enabled across slices															
1h	Disable	16X16 Checkerboard hashing disabled across slices															
	9	WIZ Hashing Mode High Bit															
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>r/w</td></tr> <tr> <td>Format:</td><td>U1</td></tr> </table> <p>This field adds additional hashing modes in combination with the WIZ Hashing Mode field. The Value column in the table below refers to this field (high bit) and the WIZ Hashing Mode field (low bit). This field is don't care if the Hashing Disable bit is set.</p>	Project:	BDW	Access:	r/w	Format:	U1									
Project:	BDW																
Access:	r/w																
Format:	U1																
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0h</td><td>[Default]</td><td>8x8 Checkerboard hashing</td></tr> <tr> <td>1h</td><td></td><td>8x4 Checkerboard hashing</td></tr> <tr> <td>2h</td><td></td><td>16x4 Checkerboard hashing</td></tr> <tr> <td>3h</td><td></td><td>Reserved</td></tr> </tbody> </table>	Value	Name	Description	0h	[Default]	8x8 Checkerboard hashing	1h		8x4 Checkerboard hashing	2h		16x4 Checkerboard hashing	3h		Reserved
Value	Name	Description															
0h	[Default]	8x8 Checkerboard hashing															
1h		8x4 Checkerboard hashing															
2h		16x4 Checkerboard hashing															
3h		Reserved															
		Programming Notes															
		8x4 hashing preferred for when msaa enabled															
	8	Reserved															
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>r/w</td></tr> <tr> <td>Format:</td><td>PBC</td></tr> </table>	Project:	BDW	Access:	r/w	Format:	PBC									
Project:	BDW																
Access:	r/w																
Format:	PBC																
	7	WIZ Hashing Mode															
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>r/w</td></tr> <tr> <td>Format:</td><td>U1</td></tr> </table>	Project:	BDW	Access:	r/w	Format:	U1									
Project:	BDW																
Access:	r/w																
Format:	U1																
		Description															
		This field configures the Hashing mode in Windower. This field is don't care if the Hashing Disable bit is set.															
		The WIZ Hashing Mode High Bit field is combined with this field to enable additional modes.															

GT_MODE - GT Mode Register

	6:3	Reserved	
		Project:	BDW
		Access:	r/w
		Format:	PBC
	2	Reserved	
		Project:	BDW*:A, :*:B
		Access:	r/w
		Format:	PBC
	1:0	Reserved	
		Project:	BDW
		Access:	r/w
		Format:	PBC

GTSCRATCH

GTSCRATCH		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	4F100h-4F11Fh	
Name:	GT Scratchpad	
ShortName:	GTSCRATCH_*	
Valid Projects:	BDW	
Power:	Always on	
Reset:	soft	
There are 8 instances of this register format.		
Restriction		
These registers are used by hardware and must not be used by software.		
DWord	Bit	Description
0	31:0	GT Scratchpad GT Scratchpad

GT Scratch Pad 1

GTSP1_0_2_0_GTTMMADR - GT Scratch Pad 1						
Multiple Force Wake						
DWord	Bit	Description				
0	31:0	<p>GT scratch pad</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000000000000000000000000000b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>FLR Resettable [31:16] are reserved. [15:0] Multiple Force Wake: GT programs this field with the multiple force wake status. Software reads this field to find the status. Refer to MULTIFORCEWAKE 0xA188 register description for the usage.</p>	Default Value:	00000000000000000000000000000000b	Access:	R/W
Default Value:	00000000000000000000000000000000b					
Access:	R/W					

GT Scratch Pad 2

GTSP2_0_2_0_GTTMMADR - GT Scratch Pad 2						
Register Space: MMIO: 0/2/0						
Project: BDW						
Default Value: 0x00000000						
Size (in bits): 32						
Address: 130048h						
FLR Resettable Scratchpad register can be R/W by both driver and GT.						
DWord	Bit	Description				
0	31:0	GT scratch pad <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Default Value:</td><td style="padding: 2px;">00000000000000000000000000000000b</td></tr> <tr> <td style="padding: 2px;">Access:</td><td style="padding: 2px;">R/W</td></tr> </table>	Default Value:	00000000000000000000000000000000b	Access:	R/W
Default Value:	00000000000000000000000000000000b					
Access:	R/W					

GT Scratch Pad 3

GTSP3_0_2_0_GTTMMADR - GT Scratch Pad 3			
Register Space: MMIO: 0/2/0			
Project: BDW			
Default Value: 0x00000000			
Size (in bits): 32			
Address: 13004Ch			
FLR Resettable Scratchpad register can be R/W by both driver and GT.			
DWord	Bit	Description	
0	31:0	GT scratch pad	
		Default Value:	00000000000000000000000000000000b
		Access:	R/W

GT Scratch Pad 4

GTSP4_0_2_0_GTTMMADR - GT Scratch Pad 4			
Register Space:	MMIO: 0/2/0		
Project:	BDW		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	130050h		
FLR Resettable Scratchpad register can be R/W by both driver and GT.			
DWord	Bit	Description	
0	31:0	GT scratch pad	
		Default Value:	00000000000000000000000000000000b
		Access:	R/W

GT Scratch Pad 5

GTSP5_0_2_0_GTTMMADR - GT Scratch Pad 5			
Register Space: MMIO: 0/2/0			
Project: BDW			
Default Value: 0x00000000			
Size (in bits): 32			
Address: 130054h			
FLR Resettable Scratchpad register can be R/W by both driver and GT.			
DWord	Bit	Description	
0	31:0	GT scratch pad	
		Default Value:	00000000000000000000000000000000b
		Access:	R/W

GT Scratch Pad 6

GTSP6_0_2_0_GTTMMADR - GT Scratch Pad 6			
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x00000000 Size (in bits): 32			
Address: 130058h			
FLR Resettable Scratchpad register can be R/W by both driver and GT.			
DWord	Bit	Description	
0	31:0	GT scratch pad Default Value: 00000000000000000000000000000000b Access: R/W	

GTT Cache Enable

GTT_CACHE_EN - GTT CacheEnable																																																				
Register Space: MMIO: 0/2/0 Project: BDW 0x00000000 [BDW:GT1, BDW:GT2, BDW:GT3:H, BDW:GT3E] Size (in bits): 32																																																				
Address: 04024h Enable GTT Cache for respective client(s), A0: Must program/observed this to all 0 due to Big Pages Bug 1898112																																																				
DWord	Bit	Description																																																		
0	31:0	<p>GTT Cache Enable for CS</p> <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> <tr> <td colspan="2">Enable GTT Caching for all the client(s) below:</td></tr> <tr> <td colspan="2">31: BLIT Engine (overrides individual enables of the units)</td></tr> <tr> <td colspan="2">30: VEBX Engine (overrides individual enables of the units)</td></tr> <tr> <td colspan="2">29: MFX Engine (overrides individual enables of the units)</td></tr> <tr> <td colspan="2">28: GFX Engine (overrides individual enables of the units)</td></tr> <tr> <td colspan="2">27-15: Reserved</td></tr> <tr> <td colspan="2">14: VM Cunit</td></tr> <tr> <td colspan="2">13: VL Funit</td></tr> <tr> <td colspan="2">12: BLB unit</td></tr> <tr> <td colspan="2">11: VF Wunit</td></tr> <tr> <td colspan="2">10: VE Ounit</td></tr> <tr> <td colspan="2">9: HI Zunit</td></tr> <tr> <td colspan="2">8: RCZ unit</td></tr> <tr> <td colspan="2">7: RCC unit</td></tr> <tr> <td colspan="2">6: ISC unit</td></tr> <tr> <td colspan="2">5: DC unit</td></tr> <tr> <td colspan="2">4: MT unit</td></tr> <tr> <td colspan="2">3: SOL unit</td></tr> <tr> <td colspan="2">2: VF unit</td></tr> <tr> <td colspan="2">1: RS unit</td></tr> <tr> <td colspan="2">0: CS unit</td></tr> <tr> <th>Value</th><th>Name</th><th>Project</th></tr> <tr> <td>00000000h</td><td>[Default]</td><td>BDW</td></tr> </table>	Access:	R/W	Enable GTT Caching for all the client(s) below:		31: BLIT Engine (overrides individual enables of the units)		30: VEBX Engine (overrides individual enables of the units)		29: MFX Engine (overrides individual enables of the units)		28: GFX Engine (overrides individual enables of the units)		27-15: Reserved		14: VM Cunit		13: VL Funit		12: BLB unit		11: VF Wunit		10: VE Ounit		9: HI Zunit		8: RCZ unit		7: RCC unit		6: ISC unit		5: DC unit		4: MT unit		3: SOL unit		2: VF unit		1: RS unit		0: CS unit		Value	Name	Project	00000000h	[Default]	BDW
Access:	R/W																																																			
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2: VF unit																																																				
1: RS unit																																																				
0: CS unit																																																				
Value	Name	Project																																																		
00000000h	[Default]	BDW																																																		

Hardware Scratch Read Write

HSRW_0_2_0_PCI - Hardware Scratch Read Write						
DWord	Bit	Description				
0	15:0	<p>Reserved R/W</p> <table border="1"> <tr> <td>Default Value:</td><td>0000000000000000b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>FLR Resettable Reserved for future usage.</p>	Default Value:	0000000000000000b	Access:	R/W
Default Value:	0000000000000000b					
Access:	R/W					

Hardware Status Mask Register

HWSTAM - Hardware Status Mask Register						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Source:	RenderCS					
Default Value:	0xFFFFFFFF					
Access:	R/W, RO					
Size (in bits):	32					
Trusted Type:	1					
Address:	02098h					
<p>The HWSTAM register has the same format as the Interrupt Control Registers. The bits in this register are mask bits that prevent the corresponding bits in the Interrupt Status Register from generating a Hardware Status Write (PCI write cycle). Any unmasked interrupt bit (HWSTAM bit set to 0) will allow the Interrupt Status Register to be written to the ISR location (within the memory page specified by the Hardware Status Page Address Register) when that Interrupt Status Register bit changes state.</p>						
Programming Notes						
<ul style="list-style-type: none"> • To write the interrupt to the HWSP, the corresponding IMR bit must also be clear (enabled). • At most 1 bit can be unmasked at any given time. 						
DWord	Bit	Description				
0	31:0	<p>Hardware Status Mask Register Value</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Default Value:</td><td style="padding: 2px;">FFFFFFFh</td></tr> <tr> <td style="padding: 2px;">Format:</td><td style="padding: 2px;">Array of Masks</td></tr> </table> <p>Refer to the Interrupt Control Register section for bit definitions. Reserved bits are RO.</p>	Default Value:	FFFFFFFh	Format:	Array of Masks
Default Value:	FFFFFFFh					
Format:	Array of Masks					

Hardware Status Page Address Register

HWS_PGA - Hardware Status Page Address Register				
Register Space:	MMIO: 0/2/0			
Project:	BDW			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Trusted Type:	1			
Address:	02080h-02083h			
Name:	Hardware Status Page Address Register			
ShortName:	HWS_PGA_RCSUNIT			
Address:	12080h-12083h			
Name:	Hardware Status Page Address Register			
ShortName:	HWS_PGA_VCSUNIT0			
Address:	1A080h-1A083h			
Name:	Hardware Status Page Address Register			
ShortName:	HWS_PGA_VECSUNIT			
Address:	1C080h-1C083h			
Name:	Hardware Status Page Address Register			
ShortName:	HWS_PGA_VCSUNIT1			
Address:	22080h-22083h			
Name:	Hardware Status Page Address Register			
ShortName:	HWS_PGA_BCSUNIT			
Description				
This register is used to program the 4 KB-aligned System Memory address of the Hardware Status Page used to report hardware status into (typically cacheable) System Memory.				
The address in this register is translated using the Global GTT in memory. The mapping type of the GTT entry determines the snoop nature of the transaction to memory.				
DWord	Bit	Description		
0	31:12	<p>Address</p> <table border="1"> <tr> <td>Format:</td><td>GraphicsAddress[31:12]</td></tr> </table> <p>This field is used by SW to specify Bits 31:12 of the 4 KB-aligned System Memory address of the 4 KB page known as the Hardware Status Page. The Global GTT is used to map this page from the graphics virtual address to physical address.</p> <p>Programming Notes</p> <p>If the Per-Process Virtual Address Space and Exec List Enable bit is set, HW requires that the status page is programmed to allow for the context switch status to be reported.</p>	Format:	GraphicsAddress[31:12]
Format:	GraphicsAddress[31:12]			

HWS_PGA - Hardware Status Page Address Register

	11:0	Reserved	Format:	MBZ
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HBLANK

HBLANK		
Register Space: MMIO: 0/2/0 Project: DevLPT:H Default Value: 0x00000000 Access: R/W Size (in bits): 32		
Address: E0004h-E0007h Name: Transcoder A Horizontal Blank ShortName: TRANS_HBLANK_A Power: Always on Reset: soft		
DWord	Bit	Description
0	31:29	Reserved Format: MBZ
	28:16	Horizontal Blank End This field specifies Horizontal Blank End position relative to the horizontal active display start. The minimum horizontal blank size is 32 pixels. This register must always be programmed to the same value as the Horizontal Total.
	15:13	Reserved Format: MBZ
	12:0	Horizontal Blank Start This field specifies the Horizontal Blank Start position relative to the horizontal active display start. This register must always be programmed to the same value as the Horizontal Active.

HDC TLB REQUEST CONTROL REGISTER

HDCTLB_REQ_CTRL - HDC TLB REQUEST CONTROL REGISTER			
Register Space:	MMIO: 0/2/0		
Default Value:	0x00000000		
Size (in bits):	32		
This is a basic register template			
DWord	Bit	Description	
0	31:19	Reserved	
		Default Value:	000000000000000b
		Access:	RO

Header Type

HDR2_0_2_0_PCI - Header Type			
DWord	Bit	Description	
0	7	Multi Function Status	
		Default Value: Access:	0b RO
Indicates if the device is a Multi-Function Device. The Value of this register is hardwired to 0, internal graphics is a single function.			
	6:0	Header Code	
		Default Value: Access:	0000000b RO
This is a 7-bit value that indicates the Header Code for the IGD. This code is hardwired to the value 00h, indicating a type 0 configuration space format.			

HOTPLUG_CTL

HOTPLUG_CTL											
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x00000000 Access: R/W Size (in bits): 32											
Address: 44030h-44033h Name: Hot Plug Control ShortName: HOTPLUG_CTL Power: Always on Reset: soft											
DWord	Bit	Description									
0	31:5	Reserved									
	4	DDI A HPD Input Enable <p>This field enables the hot plug detection for port A. This is independent of whether the port is enabled or not.</p> <p>On systems that have the CPU and PCH in the same package, the DDI A HPD input is connected to the PCH, and the DDI A HPD input must be enabled in both the North Display Engine Registers HOTPLUG_CTL and the South Display Engine Registers SHOTPLUG_CTL.</p> <p>On systems that have the CPU and PCH in separate packages, the DDI A HPD input is connected to the CPU, and the DDI A HPD input must be enabled in only the North Display Engine Registers HOTPLUG_CTL.</p> <p>The fuse register FUSE_STRAP3 has a field that indicates the package type.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Disable</td><td>Hot plugs cannot be detected.</td></tr> <tr> <td>1b</td><td>Enable</td><td>Hot plugs can be detected.</td></tr> </tbody> </table>	Value	Name	Description	0b	Disable	Hot plugs cannot be detected.	1b	Enable	Hot plugs can be detected.
Value	Name	Description									
0b	Disable	Hot plugs cannot be detected.									
1b	Enable	Hot plugs can be detected.									
	3:2	Reserved									

HOTPLUG_CTL														
1:0	DDI A HPD Status													
	Access:	R/WC												
<p>This field reflects the hot plug detect status on port A. This bit is used for either monitor hotplug/unplug or for notification of a sink event. When HPD input is enabled and either a long or short pulse is detected, one of these bits will set and the hotplug IIR will be set (if unmasked in the IMR). The hotplug ISR gives the live state of the HPD pin. These are sticky bits, cleared by writing 1s to both of them. The short pulse duration is programmed in HPD_PULSE_CNT.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>00b</td><td>Not Detected</td><td>Digital port hot plug event not detected</td></tr> <tr> <td>1Xb</td><td>Long Pulse</td><td>Digital port long pulse hot plug event detected</td></tr> <tr> <td>X1b</td><td>Short Pulse</td><td>Digital port short pulse hot plug event detected</td></tr> </tbody> </table> <p>Programming Notes</p> <p>Due to the possibility of back to back HPD events it is recommended that software filters the value read from the ISR.</p>			Value	Name	Description	00b	Not Detected	Digital port hot plug event not detected	1Xb	Long Pulse	Digital port long pulse hot plug event detected	X1b	Short Pulse	Digital port short pulse hot plug event detected
Value	Name	Description												
00b	Not Detected	Digital port hot plug event not detected												
1Xb	Long Pulse	Digital port long pulse hot plug event detected												
X1b	Short Pulse	Digital port short pulse hot plug event detected												

HPD_FILTER_CNT

HPD_FILTER_CNT				
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x000001F2 Access: R/W Size (in bits): 32				
Address: 44038h-4403Bh Name: HPD Filter count ShortName: HPD_FILTER_CNT Power: Always on Reset: global				
This register is on the chip reset, not the FLR reset.				
Restriction				
This register must be programmed properly before enabling DDI HPD detection.				
DWord	Bit	Description		
0	31:17	Reserved <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Format:</td> <td style="padding: 2px;">MBZ</td> </tr> </table>	Format:	MBZ
Format:	MBZ			
16:0	HPD Filter Count <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Default Value:</td> <td style="padding: 2px;">001F2h 500 microseconds</td> </tr> </table> <p>These bits define the duration of the filter for DDI HPD. The value is in number of microseconds minus 2.</p>	Default Value:	001F2h 500 microseconds	
Default Value:	001F2h 500 microseconds			

HPD_PULSE_CNT

HPD_PULSE_CNT				
Register Space:	MMIO: 0/2/0			
Project:	BDW			
Default Value:	0x000007CE			
Access:	R/W			
Size (in bits):	32			
Address:	44034h-44037h			
Name:	HPD Pulse count			
ShortName:	HPD_PULSE_CNT			
Power:	Always on			
Reset:	global			
This register is on the chip reset, not the FLR reset.				
Restriction				
This register must be programmed properly before enabling DDI HPD detection.				
DWord	Bit	Description		
0	31:17	Reserved <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Format:</td><td style="padding: 2px; width: 10%;">MBZ</td></tr> </table>	Format:	MBZ
Format:	MBZ			
16:0	DP ShortPulse Count <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Default Value:</td><td style="padding: 2px; width: 10%;">007CEh 2000 microseconds</td></tr> </table> <p style="margin-top: 2px;">These bits define the duration of the pulse defined as a short pulse for DisplayPort HPD. The value is in number of microseconds minus 2.</p>	Default Value:	007CEh 2000 microseconds	
Default Value:	007CEh 2000 microseconds			

HS Invocation Counter

HS_INVOCATION_COUNT - HS Invocation Counter		
Register Space: MMIO: 0/2/0 Project: BDW Source: RenderCS Default Value: 0x00000000, 0x00000000 Access: R/W Size (in bits): 64 Trusted Type: 1		
Address: 02300h		
This register stores the number of patch objects processed by the HS unit. E.g., A PATCHLIST_2 topology with 6 vertices would cause this counter to increment by 3 (there are 3 2-vertex patch objects in that topology). This register is part of the context save and restore.		
DWord	Bit	Description
0	63:32	HS Invocation Count UDW Number of patch objects processed by the HS stage. Updated only when HS Enable and HS Statistics Enable are set in 3DSTATE_HS
	31:0	HS Invocation Count LDW Number of patch objects processed by the HS stage. Updated only when HS Enable and HS Statistics Enable are set in 3DSTATE_HS

HSYNC

HSYNC					
Register Space:	MMIO: 0/2/0				
Project:	DevLPT:H				
Default Value:	0x00000000				
Access:	R/W				
Size (in bits):	32				
Address:	E0008h-E000Bh				
Name:	Transcoder A Horizontal Sync				
ShortName:	TRANS_HSYNC_A				
Power:	Always on				
Reset:	soft				
DWord	Bit	Description			
0	31:29	Reserved Format: MBZ			
	28:16	Horizontal Sync End This field specifies the Horizontal Sync End position relative to the horizontal active display start. It is programmed with HorizontalActive+FrontPorch+Sync-1. This value must be greater than the horizontal sync start and less than Horizontal Total. <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center; background-color: #e0e0ff;">Value</th><th style="text-align: center; background-color: #e0e0ff;">Name</th></tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td><td></td></tr> </tbody> </table>	Value	Name	0b
Value	Name				
0b					
15:13	Reserved Format: MBZ				
12:0	Horizontal Sync Start This field specifies the Horizontal Sync Start position relative to the horizontal active display start. It is programmed with HorizontalActive+FrontPorch-1. This value must be greater than Horizontal Active. <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center; background-color: #e0e0ff;">Value</th><th style="text-align: center; background-color: #e0e0ff;">Name</th></tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td><td></td></tr> </tbody> </table>	Value	Name	0b	
Value	Name				
0b					

HTOTAL

HTOTAL			
Register Space: MMIO: 0/2/0 Project: DevLPT:H Default Value: 0x00000000 Access: R/W Size (in bits): 32			
Address: E0000h-E0003h Name: Transcoder A Horizontal Total ShortName: TRANS_HTOTAL_A Power: Always on Reset: soft			
DWord	Bit	Description	
0	31:29	Reserved	Format: MBZ
	28:16	Horizontal Total This field specifies Horizontal Total size. This should be equal to the sum of the horizontal active and the horizontal blank sizes. This field is programmed to the number of pixels desired minus one. This register must always be programmed to the same value as the Horizontal Blank End.	
	15:12	Reserved	Format: MBZ
	11:0	Horizontal Active This field specifies Horizontal Active Display size. Note that the first horizontal active display pixel is considered pixel number 0. This field is programmed to the number of pixels desired minus one. The minimum horizontal active display size is 64 pixels. This register must always be programmed to the same value as the Horizontal Blank Start.	

HW RC allow calculation results

RC_STATUS3 - HW RC allow calculation results						
DWord	Bit	Description				
0	31:28	<p>PM Allow</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>pmcr_allow_store[3:0].</td> <td></td> </tr> </table>	Access:	R/W	pmcr_allow_store[3:0].	
Access:	R/W					
pmcr_allow_store[3:0].						
27:0	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO			
Access:	RO					

IA32_MTRR_FIX4K_C0000_High

MTRR_FIX4K_C0000_H - IA32_MTRR_FIX4K_C0000_High						
DWord	Bit	Description				
0	31:0	<p>Range0 to Range7 Memory Type</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Bit[63:56]: Identifies the memory type 00h-FFh of range#7. Bit[55:48]: Identifies the memory type 00h-FFh of range#6. Bit[47:40]: Identifies the memory type 00h-FFh of range#5. Bit[39:32]: Identifies the memory type 00h-FFh of range#4.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

IA32_MTRR_FIX4K_C0000_Low

MTRR_FIX4K_C0000_L - IA32_MTRR_FIX4K_C0000 Low						
DWord	Bit	Description				
0	31:0	<p>Range0 to Range7 Memory Type</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Bit[31:24]: Identifies the memory type 00h-FFh of range#3. Bit[23:16]: Identifies the memory type 00h-FFh of range#2. Bit[15:8]: Identifies the memory type 00h-FFh of range#1. Bit[7:0]: Identifies the memory type 00h-FFh of range#0.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

IA32_MTRR_FIX4K_C8000_High

MTRR_FIX4K_C8000_H - IA32_MTRR_FIX4K_C8000_High						
DWord	Bit	Description				
0	31:0	<p>Range0 to Range7 Memory Type</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Bit[63:56]: Identifies the memory type 00h-FFh of range#7. Bit[55:48]: Identifies the memory type 00h-FFh of range#6. Bit[47:40]: Identifies the memory type 00h-FFh of range#5. Bit[39:32]: Identifies the memory type 00h-FFh of range#4.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

IA32_MTRR_FIX4K_C8000_Low

MTRR_FIX4K_C8000_L - IA32_MTRR_FIX4K_C8000_Low						
DWord	Bit	Description				
0	31:0	<p>Range0 to Range7 Memory Type</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Bit[31:24]: Identifies the memory type 00h-FFh of range#3. Bit[23:16]: Identifies the memory type 00h-FFh of range#2. Bit[15:8]: Identifies the memory type 00h-FFh of range#1. Bit[7:0]: Identifies the memory type 00h-FFh of range#0.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

IA32_MTRR_FIX4K_D0000_High

MTRR_FIX4K_D0000_H - IA32_MTRR_FIX4K_D0000_High						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	0F14Ch					
Fixed MTRR to identify (D0000-D8000h)						
DWord	Bit	Description				
0	31:0	<p>Range0 to Range7 Memory Type</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Bit[63:56]: Identifies the memory type 00h-FFh of range#7. Bit[55:48]: Identifies the memory type 00h-FFh of range#6. Bit[47:40]: Identifies the memory type 00h-FFh of range#5. Bit[39:32]: Identifies the memory type 00h-FFh of range#4.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

IA32_MTRR_FIX4K_D0000_Low

MTRR_FIX4K_D0000_L - IA32_MTRR_FIX4K_D0000_Low						
Register Space:	MMIO	0/2/0				
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	OF148h					
Fixed MTRR to identify (D0000-D8000h)						
DWord	Bit	Description				
0	31:0	<p>Range0 to Range7 Memory Type</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Bit[31:24]: Identifies the memory type 00h-FFh of range#3. Bit[23:16]: Identifies the memory type 00h-FFh of range#2. Bit[15:8]: Identifies the memory type 00h-FFh of range#1. Bit[7:0]: Identifies the memory type 00h-FFh of range#0.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

IA32_MTRR_FIX4K_D8000_High

MTRR_FIX4K_D8000_H - IA32_MTRR_FIX4K_D8000_High								
Register Space: MMIO: 0/2/0								
Project: BDW								
Default Value: 0x00000000								
Size (in bits): 32								
Address: 0F154h								
Fixed MTRR to identify (D8000-E0000h)								
DWord	Bit	Description						
0	31:0	<p>Range0 to Range7 Memory Type</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> <tr> <td colspan="2">Bit[63:56]: Identifies the memory type 00h-FFh of range#7. Bit[55:48]: Identifies the memory type 00h-FFh of range#6. Bit[47:40]: Identifies the memory type 00h-FFh of range#5. Bit[39:32]: Identifies the memory type 00h-FFh of range#4.</td></tr> </table>	Default Value:	00000000h	Access:	R/W	Bit[63:56]: Identifies the memory type 00h-FFh of range#7. Bit[55:48]: Identifies the memory type 00h-FFh of range#6. Bit[47:40]: Identifies the memory type 00h-FFh of range#5. Bit[39:32]: Identifies the memory type 00h-FFh of range#4.	
Default Value:	00000000h							
Access:	R/W							
Bit[63:56]: Identifies the memory type 00h-FFh of range#7. Bit[55:48]: Identifies the memory type 00h-FFh of range#6. Bit[47:40]: Identifies the memory type 00h-FFh of range#5. Bit[39:32]: Identifies the memory type 00h-FFh of range#4.								

IA32_MTRR_FIX4K_D8000_Low

MTRR_FIX4K_D8000_L - IA32_MTRR_FIX4K_D8000_Low						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	0F150h					
Fixed MTRR to identify (D8000-E0000h)						
DWord	Bit	Description				
0	31:0	<p>Range0 to Range7 Memory Type</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Bit[31:24]: Identifies the memory type 00h-FFh of range#3. Bit[23:16]: Identifies the memory type 00h-FFh of range#2. Bit[15:8]: Identifies the memory type 00h-FFh of range#1. Bit[7:0]: Identifies the memory type 00h-FFh of range#0.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

IA32_MTRR_FIX4K_E0000_High

MTRR_FIX4K_E0000_H - IA32_MTRR_FIX4K_E0000_High						
DWord	Bit	Description				
0	31:0	<p>Range0 to Range7 Memory Type</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Bit[63:56]: Identifies the memory type 00h-FFh of range#7. Bit[55:48]: Identifies the memory type 00h-FFh of range#6. Bit[47:40]: Identifies the memory type 00h-FFh of range#5. Bit[39:32]: Identifies the memory type 00h-FFh of range#4.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

IA32_MTRR_FIX4K_E0000_Low

MTRR_FIX4K_E0000_L - IA32_MTRR_FIX4K_E0000 Low						
DWord	Bit	Description				
0	31:0	<p>Range0 to Range7 Memory Type</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Bit[31:24]: Identifies the memory type 00h-FFh of range#3. Bit[23:16]: Identifies the memory type 00h-FFh of range#2. Bit[15:8]: Identifies the memory type 00h-FFh of range#1. Bit[7:0]: Identifies the memory type 00h-FFh of range#0.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

IA32_MTRR_FIX4K_E8000_High

MTRR_FIX4K_E8000_H - IA32_MTRR_FIX4K_E8000_High						
DWord	Bit	Description				
0	31:0	<p>Range0 to Range7 Memory Type</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Bit[63:56]: Identifies the memory type 00h-FFh of range#7. Bit[55:48]: Identifies the memory type 00h-FFh of range#6. Bit[47:40]: Identifies the memory type 00h-FFh of range#5. Bit[39:32]: Identifies the memory type 00h-FFh of range#4.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

IA32_MTRR_FIX4K_E8000_Low

MTRR_FIX4K_E8000_L - IA32_MTRR_FIX4K_E8000_Low						
DWord	Bit	Description				
0	31:0	<p>Range0 to Range7 Memory Type</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Bit[31:24]: Identifies the memory type 00h-FFh of range#3. Bit[23:16]: Identifies the memory type 00h-FFh of range#2. Bit[15:8]: Identifies the memory type 00h-FFh of range#1. Bit[7:0]: Identifies the memory type 00h-FFh of range#0.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

IA32_MTRR_FIX4K_F0000_High

MTRR_FIX4K_F0000_H - IA32_MTRR_FIX4K_F0000_High						
DWord	Bit	Description				
0	31:0	<p>Range0 to Range7 Memory Type</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Bit[63:56]: Identifies the memory type 00h-FFh of range#7. Bit[55:48]: Identifies the memory type 00h-FFh of range#6. Bit[47:40]: Identifies the memory type 00h-FFh of range#5. Bit[39:32]: Identifies the memory type 00h-FFh of range#4.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

IA32_MTRR_FIX4K_F0000_Low

MTRR_FIX4K_F0000_L - IA32_MTRR_FIX4K_F0000_Low						
DWord	Bit	Description				
0	31:0	<p>Range0 to Range7 Memory Type</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Bit[31:24]: Identifies the memory type 00h-FFh of range#3. Bit[23:16]: Identifies the memory type 00h-FFh of range#2. Bit[15:8]: Identifies the memory type 00h-FFh of range#1. Bit[7:0]: Identifies the memory type 00h-FFh of range#0.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

IA32_MTRR_FIX4K_F8000_High

MTRR_FIX4K_F8000_H - IA32_MTRR_FIX4K_F8000_High						
DWord	Bit	Description				
0	31:0	<p>Range0 to Range7 Memory Type</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Bit[63:56]: Identifies the memory type 00h-FFh of range#7. Bit[55:48]: Identifies the memory type 00h-FFh of range#6. Bit[47:40]: Identifies the memory type 00h-FFh of range#5. Bit[39:32]: Identifies the memory type 00h-FFh of range#4.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

IA32_MTRR_FIX4K_F8000_Low

MTRR_FIX4K_F8000_L - IA32_MTRR_FIX4K_F8000_Low						
DWord	Bit	Description				
0	31:0	<p>Range0 to Range7 Memory Type</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Bit[31:24]: Identifies the memory type 00h-FFh of range#3. Bit[23:16]: Identifies the memory type 00h-FFh of range#2. Bit[15:8]: Identifies the memory type 00h-FFh of range#1. Bit[7:0]: Identifies the memory type 00h-FFh of range#0.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

IA32_MTRR_FIX16K_80000_High

MTRR_FIX16K_80000_H - IA32_MTRR_FIX16K_80000_High						
DWord	Bit	Description				
0	31:0	<p>Range0 to Range7 Memory Type</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Bit[63:56]: Identifies the memory type 00h-FFh of range#7. Bit[55:48]: Identifies the memory type 00h-FFh of range#6. Bit[47:40]: Identifies the memory type 00h-FFh of range#5. Bit[39:32]: Identifies the memory type 00h-FFh of range#4.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

IA32_MTRR_FIX16K_80000_Low

MTRR_FIX16K_80000_L - IA32_MTRR_FIX16K_80000_Low						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	0F128h					
Fixed MTRR to identify 512K-768K of the main memory (80000-A0000h).						
DWord	Bit	Description				
0	31:0	<p>Range0 to Range7 Memory Type</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Bit[31:24]: Identifies the memory type 00h-FFh of range#3. Bit[23:16]: Identifies the memory type 00h-FFh of range#2. Bit[15:8]: Identifies the memory type 00h-FFh of range#1. Bit[7:0]: Identifies the memory type 00h-FFh of range#0</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

IA32_MTRR_FIX16K_A0000_High

MTRR_FIX16K_A0000_H - IA32_MTRR_FIX16K_A0000_High						
DWord	Bit	Description				
0	31:0	<p>Range0 to Range7 Memory Type</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Bit[63:56]: Identifies the memory type 00h-FFh of range#7. Bit[55:48]: Identifies the memory type 00h-FFh of range#6. Bit[47:40]: Identifies the memory type 00h-FFh of range#5. Bit[39:32]: Identifies the memory type 00h-FFh of range#4.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

IA32_MTRR_FIX16K_A0000_Low

MTRR_FIX16K_A0000_L - IA32_MTRR_FIX16K_A0000_Low						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	0F130h					
Fixed MTRR to identify 768K-1024K of the main memory (A0000-C0000h).						
DWord	Bit	Description				
0	31:0	<p>Range0 to Range7 Memory Type</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Bit[31:24]: Identifies the memory type 00h-FFh of range#3. Bit[23:16]: Identifies the memory type 00h-FFh of range#2. Bit[15:8]: Identifies the memory type 00h-FFh of range#1. Bit[7:0]: Identifies the memory type 00h-FFh of range#0.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

IA32_MTRR_FIX64K_00000_High

MTRR_FIX64K_00000_H - IA32_MTRR_FIX64K_00000_High						
DWord	Bit	Description				
0	31:0	<p>Range0 to Range7 Memory Type</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Bit[63:56]: Identifies the memory type 00h-FFh of range#7. Bit[55:48]: Identifies the memory type 00h-FFh of range#6. Bit[47:40]: Identifies the memory type 00h-FFh of range#5. Bit[39:32]: Identifies the memory type 00h-FFh of range#4.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

IA32_MTRR_FIX64K_00000_Low

MTRR_FIX64K_00000_L-IA32MTRRFIX64K_00000Low						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	0F120h					
Fixed MTRR to identify 0-512K of the main memory (0-80000h).						
DWord	Bit	Description				
0	31:0	<p>Range0 to Range7 Memory Type</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Bit[31:24]: Identifies the memory type 00h-FFh of range#3. Bit[23:16]: Identifies the memory type 00h-FFh of range#2. Bit[15:8]: Identifies the memory type 00h-FFh of range#1. Bit[7:0]: Identifies the memory type 00h-FFh of range#0.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

IA32_MTRR_PHYSBASE0_H - IA32 MTRR PHYSBASE0 High

MTRR_PHYSBASE0_H - IA32 MTRR PHYSBASE0 High				
Register Space:	MMIO: 0/2/0			
Project:	BDW			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0F184h			
Variable MTRR0				
DWord	Bit	Description		
0	31:7	Reserved		
		<table border="1"> <tr> <td>Default Value:</td><td>00000000000000000000000000000000b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	00000000000000000000000000000000b
Default Value:	00000000000000000000000000000000b			
Access:	RO			
	6:0	PhysBase		
		<table border="1"> <tr> <td>Default Value:</td><td>0000000b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Physical Base address[38:32] of the variable MTRR.</p>	Default Value:	0000000b
Default Value:	0000000b			
Access:	R/W			

IA32_MTRR_PHYSBASE0_L - IA32_MTRR_PHYSBASE0 Low

MTRR_PHYSBASE0_L - IA32_MTRR_PHYSBASE0 Low						
Register Space: MMIO: 0/2/0						
Project: BDW						
Default Value: 0x00000000						
Size (in bits): 32						
Address: 0F180h						
Variable MTRR0						
DWord	Bit	Description				
0	31:12	<p>PhysBase</p> <table border="1"> <tr> <td>Default Value:</td><td>00000h</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Physical Base address[31:0] of the variable MTRR.</p>	Default Value:	00000h	Access:	R/W
Default Value:	00000h					
Access:	R/W					
11:8	<p>Reserved</p> <table border="1"> <tr> <td>Default Value:</td><td>0000b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	0000b	Access:	RO	
Default Value:	0000b					
Access:	RO					
7:0	<p>Memory Type</p> <table border="1"> <tr> <td>Default Value:</td><td>00h</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Identifies the memory type 00h-FFh.</p>	Default Value:	00h	Access:	R/W	
Default Value:	00h					
Access:	R/W					

IA32_MTRR_PHYSBASE1_H - IA32 MTRR PHYSBASE1 High

MTRR_PHYSBASE1_H - IA32 MTRR PHYSBASE1 High				
Register Space: MMIO: 0/2/0				
Project: BDW				
Default Value: 0x00000000				
Size (in bits): 32				
Address: 0F194h				
Variable MTRR1				
DWord	Bit	Description		
0	31:7	Reserved		
		<table border="1"> <tr> <td>Default Value:</td><td>00000000000000000000000000000000b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	00000000000000000000000000000000b
Default Value:	00000000000000000000000000000000b			
Access:	RO			
	6:0	PhysBase		
		<table border="1"> <tr> <td>Default Value:</td><td>0000000b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Physical Base address[38:32] of the variable MTRR.</p>	Default Value:	0000000b
Default Value:	0000000b			
Access:	R/W			

IA32_MTRR_PHYSBASE1_L - IA32 MTRR PHYSBASE1 Low

MTRR_PHYSBASE1_L - IA32 MTRR PHYSBASE1 Low						
Variable MTRR1						
DWord	Bit	Description				
0	31:12	<p>PhysBase</p> <table border="1"> <tr> <td>Default Value:</td><td>00000h</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Physical Base address[31:0] of the variable MTRR.</p>	Default Value:	00000h	Access:	R/W
Default Value:	00000h					
Access:	R/W					
11:8	<p>Reserved</p> <table border="1"> <tr> <td>Default Value:</td><td>0000b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	0000b	Access:	RO	
Default Value:	0000b					
Access:	RO					
7:0	<p>Memory Type</p> <table border="1"> <tr> <td>Default Value:</td><td>00h</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Identifies the memory type 00h-FFh.</p>	Default Value:	00h	Access:	R/W	
Default Value:	00h					
Access:	R/W					

IA32_MTRR_PHYSBASE2_H - IA32 MTRR PHYSBASE2 High

MTRR_PHYSBASE2_H - IA32 MTRR PHYSBASE2 High				
Register Space:	MMIO: 0/2/0			
Project:	BDW			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0F1A4h			
Variable MTRR2				
DWord	Bit	Description		
0	31:7	Reserved		
		<table border="1"> <tr> <td>Default Value:</td><td>00000000000000000000000000000000b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	00000000000000000000000000000000b
Default Value:	00000000000000000000000000000000b			
Access:	RO			
	6:0	PhysBase		
		<table border="1"> <tr> <td>Default Value:</td><td>0000000b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Physical Base address[38:32] of the variable MTRR.</p>	Default Value:	0000000b
Default Value:	0000000b			
Access:	R/W			

IA32_MTRR_PHYSBASE2_L - IA32 MTRR PHYSBASE2 Low

MTRR_PHYSBASE2_L - IA32 MTRR PHYSBASE2 Low						
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x00000000 Size (in bits): 32						
Address: 0F1A0h						
Variable MTRR2						
DWord	Bit	Description				
0	31:12	<p>PhysBase</p> <table border="1"> <tr> <td>Default Value:</td><td>00000h</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Physical Base address[31:0] of the variable MTRR.</p>	Default Value:	00000h	Access:	R/W
Default Value:	00000h					
Access:	R/W					
11:8	<p>Reserved</p> <table border="1"> <tr> <td>Default Value:</td><td>0000b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	0000b	Access:	RO	
Default Value:	0000b					
Access:	RO					
7:0	<p>Memory Type</p> <table border="1"> <tr> <td>Default Value:</td><td>00h</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Identifies the memory type 00h-FFh.</p>	Default Value:	00h	Access:	R/W	
Default Value:	00h					
Access:	R/W					

IA32_MTRR_PHYSBASE3_H - IA32 MTRR PHYSBASE3 High

MTRR_PHYSBASE3_H - IA32 MTRR PHYSBASE3 High				
Register Space:	MMIO: 0/2/0			
Project:	BDW			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0F1B4h			
Variable MTRR3				
DWord	Bit	Description		
0	31:7	Reserved		
		<table border="1"> <tr> <td>Default Value:</td><td>00000000000000000000000000000000b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	00000000000000000000000000000000b
Default Value:	00000000000000000000000000000000b			
Access:	RO			
	6:0	PhysBase		
		<table border="1"> <tr> <td>Default Value:</td><td>0000000b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Physical Base address[38:32] of the variable MTRR.</p>	Default Value:	0000000b
Default Value:	0000000b			
Access:	R/W			

IA32_MTRR_PHYSBASE3_L - IA32_MTRR_PHYSBASE3 Low

MTRR_PHYSBASE3_L - IA32_MTRR_PHYSBASE3 Low						
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x00000000 Size (in bits): 32						
Address: 0F1B0h						
Variable MTRR3						
DWord	Bit	Description				
0	31:12	<p>PhysBase</p> <table border="1"> <tr> <td>Default Value:</td><td>00000h</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Physical Base address[31:0] of the variable MTRR.</p>	Default Value:	00000h	Access:	R/W
Default Value:	00000h					
Access:	R/W					
11:8	<p>Reserved</p> <table border="1"> <tr> <td>Default Value:</td><td>0000b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	0000b	Access:	RO	
Default Value:	0000b					
Access:	RO					
7:0	<p>Memory Type</p> <table border="1"> <tr> <td>Default Value:</td><td>00h</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Identifies the memory type 00h-FFh.</p>	Default Value:	00h	Access:	R/W	
Default Value:	00h					
Access:	R/W					

IA32_MTRR_PHYSBASE4_H - IA32 MTRR PHYSBASE4 High

MTRR_PHYSBASE4_H - IA32 MTRR PHYSBASE4 High				
Register Space:	MMIO: 0/2/0			
Project:	BDW			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0F1C4h			
Variable MTRR4				
DWord	Bit	Description		
0	31:7	Reserved		
		<table border="1"> <tr> <td>Default Value:</td><td>00000000000000000000000000000000b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	00000000000000000000000000000000b
Default Value:	00000000000000000000000000000000b			
Access:	RO			
	6:0	PhysBase		
		<table border="1"> <tr> <td>Default Value:</td><td>0000000b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Physical Base address[38:32] of the variable MTRR.</p>	Default Value:	0000000b
Default Value:	0000000b			
Access:	R/W			

IA32_MTRR_PHYSBASE4_L - IA32 MTRR PHYSBASE4 Low

MTRR_PHYSBASE4_L - IA32 MTRR PHYSBASE4 Low						
Register Space: MMIO: 0/2/0						
Project: BDW						
Default Value: 0x00000000						
Size (in bits): 32						
Address: 0F1C0h						
Variable MTRR4						
DWord	Bit	Description				
0	31:12	<p>PhysBase</p> <table border="1"> <tr> <td>Default Value:</td><td>00000h</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Physical Base address[31:0] of the variable MTRR.</p>	Default Value:	00000h	Access:	R/W
Default Value:	00000h					
Access:	R/W					
11:8	<p>Reserved</p> <table border="1"> <tr> <td>Default Value:</td><td>0000b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	0000b	Access:	RO	
Default Value:	0000b					
Access:	RO					
7:0	<p>Memory Type</p> <table border="1"> <tr> <td>Default Value:</td><td>00h</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Identifies the memory type 00h-FFh</p>	Default Value:	00h	Access:	R/W	
Default Value:	00h					
Access:	R/W					

IA32_MTRR_PHYSBASE5_H - IA32 MTRR PHYSBASE5 High

MTRR_PHYSBASE5_H - IA32 MTRR PHYSBASE5 High				
Register Space:	MMIO: 0/2/0			
Project:	BDW			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0F1D4h			
Variable MTRR5				
DWord	Bit	Description		
0	31:7	Reserved		
		<table border="1"> <tr> <td>Default Value:</td><td>00000000000000000000000000000000b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	00000000000000000000000000000000b
Default Value:	00000000000000000000000000000000b			
Access:	RO			
	6:0	PhysBase		
		<table border="1"> <tr> <td>Default Value:</td><td>0000000b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Physical Base address[38:32] of the variable MTRR.</p>	Default Value:	0000000b
Default Value:	0000000b			
Access:	R/W			

IA32_MTRR_PHYSBASE5_L - IA32 MTRR PHYSBASE5 Low

MTRR_PHYSBASE5_L - IA32 MTRR PHYSBASE5 Low						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	0F1D0h					
Variable MTRR5						
DWord	Bit	Description				
0	31:12	<p>PhysBase</p> <table border="1"> <tr> <td>Default Value:</td><td>00000h</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Physical Base address[31:0] of the variable MTRR.</p>	Default Value:	00000h	Access:	R/W
Default Value:	00000h					
Access:	R/W					
11:8	<p>Reserved</p> <table border="1"> <tr> <td>Default Value:</td><td>0000b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	0000b	Access:	RO	
Default Value:	0000b					
Access:	RO					
7:0	<p>Memory Type</p> <table border="1"> <tr> <td>Default Value:</td><td>00h</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Identifies the memory type 00h-FFh.</p>	Default Value:	00h	Access:	R/W	
Default Value:	00h					
Access:	R/W					

IA32_MTRR_PHYSBASE6_H - IA32 MTRR PHYSBASE6 High

MTRR_PHYSBASE6_H - IA32 MTRR PHYSBASE6 High				
Register Space:	MMIO: 0/2/0			
Project:	BDW			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0F1E4h			
Variable MTRR6				
DWord	Bit	Description		
0	31:7	Reserved		
		<table border="1"> <tr> <td>Default Value:</td><td>00000000000000000000000000000000b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	00000000000000000000000000000000b
Default Value:	00000000000000000000000000000000b			
Access:	RO			
	6:0	PhysBase		
		<table border="1"> <tr> <td>Default Value:</td><td>0000000b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Physical Base address[38:32] of the variable MTRR.</p>	Default Value:	0000000b
Default Value:	0000000b			
Access:	R/W			

IA32_MTRR_PHYSBASE6_L - IA32_MTRR_PHYSBASE6 Low

MTRR_PHYSBASE6_L - IA32_MTRR_PHYSBASE6 Low						
Variable MTRR6						
DWord	Bit	Description				
0	31:12	<p>PhysBase</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Physical Base address[31:0] of the variable MTRR.</p>	Default Value:	00000h	Access:	R/W
Default Value:	00000h					
Access:	R/W					
11:8	<p>Reserved</p> <table border="1"> <tr> <td>Default Value:</td> <td>0000b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Default Value:	0000b	Access:	RO	
Default Value:	0000b					
Access:	RO					
7:0	<p>Memory Type</p> <table border="1"> <tr> <td>Default Value:</td> <td>00h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Identifies the memory type 00h-FFh.</p>	Default Value:	00h	Access:	R/W	
Default Value:	00h					
Access:	R/W					

IA32_MTRR_PHYSBASE7_H - IA32 MTRR PHYSBASE7 High

MTRR_PHYSBASE7_H - IA32 MTRR PHYSBASE7 High				
Register Space:	MMIO: 0/2/0			
Project:	BDW			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0F1F4h			
Variable MTRR7				
DWord	Bit	Description		
0	31:7	Reserved		
		<table border="1"> <tr> <td>Default Value:</td><td>00000000000000000000000000000000b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	00000000000000000000000000000000b
Default Value:	00000000000000000000000000000000b			
Access:	RO			
	6:0	PhysBase		
		<table border="1"> <tr> <td>Default Value:</td><td>0000000b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Physical Base address[38:32] of the variable MTRR.</p>	Default Value:	0000000b
Default Value:	0000000b			
Access:	R/W			

IA32_MTRR_PHYSBASE7_L - IA32_MTRR_PHYSBASE7 Low

MTRR_PHYSBASE7_L - IA32_MTRR_PHYSBASE7 Low						
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x00000000 Size (in bits): 32						
Address: 0F1F0h						
Variable MTRR7						
DWord	Bit	Description				
0	31:12	<p>PhysBase</p> <table border="1"> <tr> <td>Default Value:</td><td>00000h</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Physical Base address[31:0] of the variable MTRR.</p>	Default Value:	00000h	Access:	R/W
Default Value:	00000h					
Access:	R/W					
11:8	<p>Reserved</p> <table border="1"> <tr> <td>Default Value:</td><td>0000b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	0000b	Access:	RO	
Default Value:	0000b					
Access:	RO					
7:0	<p>Memory Type</p> <table border="1"> <tr> <td>Default Value:</td><td>00h</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Identifies the memory type 00h-FFh.</p>	Default Value:	00h	Access:	R/W	
Default Value:	00h					
Access:	R/W					

IA32_MTRR_PHYSBASE8_H - IA32 MTRR PHYSBASE8 High

MTRR_PHYSBASE8_H - IA32 MTRR PHYSBASE8 High				
Register Space:	MMIO: 0/2/0			
Project:	BDW			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0F204h			
Variable MTRR8				
DWord	Bit	Description		
0	31:7	Reserved		
		<table border="1"> <tr> <td>Default Value:</td><td>00000000000000000000000000000000b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	00000000000000000000000000000000b
Default Value:	00000000000000000000000000000000b			
Access:	RO			
	6:0	PhysBase		
		<table border="1"> <tr> <td>Default Value:</td><td>0000000b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Physical Base address[38:32] of the variable MTRR.</p>	Default Value:	0000000b
Default Value:	0000000b			
Access:	R/W			

IA32_MTRR_PHYSBASE8_L - IA32_MTRR_PHYSBASE8 Low

MTRR_PHYSBASE8_L - IA32_MTRR_PHYSBASE8 Low						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	0F200h					
Variable MTRR8						
DWord	Bit	Description				
0	31:12	PhysBase				
		<table border="1"> <tr> <td>Default Value:</td><td>00000h</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Physical Base address[31:0] of the variable MTRR</p>	Default Value:	00000h	Access:	R/W
Default Value:	00000h					
Access:	R/W					
11:8	Reserved					
0	7:0	<table border="1"> <tr> <td>Default Value:</td><td>0000b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	0000b	Access:	RO
Default Value:	0000b					
Access:	RO					
Memory Type						
	<table border="1"> <tr> <td>Default Value:</td><td>00h</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Identifies the memory type 00h-FFh.</p>	Default Value:	00h	Access:	R/W	
Default Value:	00h					
Access:	R/W					

IA32_MTRR_PHYSBASE9_H - IA32 MTRR PHYSBASE9 High

MTRR_PHYSBASE9_H - IA32 MTRR PHYSBASE9 High				
Register Space:	MMIO: 0/2/0			
Project:	BDW			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0F214h			
Variable MTRR9				
DWord	Bit	Description		
0	31:7	Reserved		
		<table border="1"> <tr> <td>Default Value:</td><td>00000000000000000000000000000000b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	00000000000000000000000000000000b
Default Value:	00000000000000000000000000000000b			
Access:	RO			
	6:0	PhysBase		
		<table border="1"> <tr> <td>Default Value:</td><td>0000000b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Physical Base address[38:32] of the variable MTRR.</p>	Default Value:	0000000b
Default Value:	0000000b			
Access:	R/W			

IA32_MTRR_PHYSBASE9_L - IA32 MTRR PHYSBASE9 Low

MTRR_PHYSBASE9_L - IA32 MTRR PHYSBASE9 Low						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	0F210h					
Variable MTRR9						
DWord	Bit	Description				
0	31:12	<p>PhysBase</p> <table border="1"> <tr> <td>Default Value:</td><td>00000h</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Physical Base address[31:0] of the variable MTRR.</p>	Default Value:	00000h	Access:	R/W
Default Value:	00000h					
Access:	R/W					
11:8	<p>Reserved</p> <table border="1"> <tr> <td>Default Value:</td><td>0000b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	0000b	Access:	RO	
Default Value:	0000b					
Access:	RO					
7:0	<p>Memory Type</p> <table border="1"> <tr> <td>Default Value:</td><td>00h</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Identifies the memory type 00h-FFh.</p>	Default Value:	00h	Access:	R/W	
Default Value:	00h					
Access:	R/W					

IA32_MTRR_PHYSMASK0_H - IA32 MTRR PHYSMASK0 High

MTRR_PHYSMASK0_H - IA32 MTRR PHYSMASK0 High				
Register Space: MMIO: 0/2/0				
Project: BDW				
Default Value: 0x00000000				
Size (in bits): 32				
Address: 0F18Ch				
Variable MTRR0				
DWord	Bit	Description		
0	31:7	Reserved		
		<table border="1"> <tr> <td>Default Value:</td><td>00000000000000000000000000000000b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	00000000000000000000000000000000b
Default Value:	00000000000000000000000000000000b			
Access:	RO			
	6:0	PhysMask		
		<table border="1"> <tr> <td>Default Value:</td><td>0000000b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Physical MASK for the address[38:32] of the variable MTRR.</p>	Default Value:	0000000b
Default Value:	0000000b			
Access:	R/W			

IA32_MTRR_PHYSMASK0_L - IA32_MTRR_PHYSMASK0 Low

MTRR_PHYSMASK0_L - IA32_MTRR_PHYSMASK0 Low				
Register Space:	MMIO: 0/2/0			
Project:	BDW			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0F188h			
Variable MTRR0				
DWord	Bit	Description		
0	31:12	PhysMask		
		<table border="1"> <tr> <td>Default Value:</td><td>00000h</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Physical MASK for the address[31:0] of the variable MTRR.</p>	Default Value:	00000h
Default Value:	00000h			
Access:	R/W			
Valid <table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Valid bit showing that MTRR decode is active.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b			
Access:	R/W			
	10:0	Reserved		
		<table border="1"> <tr> <td>Default Value:</td><td>00000000000b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	00000000000b
Default Value:	00000000000b			
Access:	RO			

IA32_MTRR_PHYSMASK1_H - IA32 MTRR PHYSMASK1 High

MTRR_PHYSMASK1_H - IA32 MTRR PHYSMASK1 High				
Register Space: MMIO: 0/2/0				
Project: BDW				
Default Value: 0x00000000				
Size (in bits): 32				
Address: 0F19Ch				
Variable MTRR1				
DWord	Bit	Description		
0	31:7	Reserved		
		<table border="1"> <tr> <td>Default Value:</td><td>00000000000000000000000000000000b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	00000000000000000000000000000000b
Default Value:	00000000000000000000000000000000b			
Access:	RO			
	6:0	PhysMask		
		<table border="1"> <tr> <td>Default Value:</td><td>0000000b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Physical MASK for the address[38:32] of the variable MTRR.</p>	Default Value:	0000000b
Default Value:	0000000b			
Access:	R/W			

IA32_MTRR_PHYSMASK1_L - IA32 MTRR PHYSMASK1 Low

MTRR_PHYSMASK1_L - IA32 MTRR PHYSMASK1 Low				
Register Space:	MMIO: 0/2/0			
Project:	BDW			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0F198h			
Variable MTRR1				
DWord	Bit	Description		
0	31:12	PhysMask		
		<table border="1"> <tr> <td>Default Value:</td><td>00000h</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Physical MASK for the address[31:0] of the variable MTRR.</p>	Default Value:	00000h
Default Value:	00000h			
Access:	R/W			
Valid <table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Valid bit showing that MTRR decode is active.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b			
Access:	R/W			
	10:0	Reserved		
		<table border="1"> <tr> <td>Default Value:</td><td>00000000000b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	00000000000b
Default Value:	00000000000b			
Access:	RO			

IA32_MTRR_PHYSMASK2_H - IA32 MTRR PHYSMASK2 High

MTRR_PHYSMASK2_H - IA32 MTRR PHYSMASK2 High				
Register Space: MMIO: 0/2/0				
Project: BDW				
Default Value: 0x00000000				
Size (in bits): 32				
Address: 0F1ACh				
Variable MTRR2				
DWord	Bit	Description		
0	31:7	Reserved		
		<table border="1"> <tr> <td>Default Value:</td><td>00000000000000000000000000000000b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	00000000000000000000000000000000b
Default Value:	00000000000000000000000000000000b			
Access:	RO			
	6:0	PhysMask		
		<table border="1"> <tr> <td>Default Value:</td><td>0000000b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Physical MASK for the address[38:32] of the variable MTRR.</p>	Default Value:	0000000b
Default Value:	0000000b			
Access:	R/W			

IA32_MTRR_PHYSMASK2_L - IA32_MTRR_PHYSMASK2 Low

MTRR_PHYSMASK2_L - IA32_MTRR_PHYSMASK2 Low		
Variable MTRR2		
DWord	Bit	Description
0	31:12	PhysMask
		Default Value: 00000h Access: R/W Physical MASK for the address[31:0] of the variable MTRR.
		Valid
11	11	Default Value: 0b Access: R/W Valid bit showing that MTRR decode is active.
		Reserved
		Default Value: 00000000000b Access: RO

IA32_MTRR_PHYSMASK3_H - IA32 MTRR PHYSMASK3 High

MTRR_PHYSMASK3_H - IA32 MTRR PHYSMASK3 High				
Register Space: MMIO: 0/2/0				
Project: BDW				
Default Value: 0x00000000				
Size (in bits): 32				
Address: 0F1BCh				
Variable MTRR3				
DWord	Bit	Description		
0	31:7	Reserved		
		<table border="1"> <tr> <td>Default Value:</td><td>00000000000000000000000000000000b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	00000000000000000000000000000000b
Default Value:	00000000000000000000000000000000b			
Access:	RO			
	6:0	PhysMask		
		<table border="1"> <tr> <td>Default Value:</td><td>0000000b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Physical MASK for the address[38:32] of the variable MTRR.</p>	Default Value:	0000000b
Default Value:	0000000b			
Access:	R/W			

IA32_MTRR_PHYSMASK3_L - IA32 MTRR PHYSMASK3 Low

MTRR_PHYSMASK3_L - IA32 MTRR PHYSMASK3 Low				
Register Space:	MMIO: 0/2/0			
Project:	BDW			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0F1B8h			
Variable MTRR3				
DWord	Bit	Description		
0	31:12	PhysMask		
		<table border="1"> <tr> <td>Default Value:</td><td>00000h</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Physical MASK for the address[31:0] of the variable MTRR.</p>	Default Value:	00000h
Default Value:	00000h			
Access:	R/W			
Valid <table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Valid bit showing that MTRR decode is active.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b			
Access:	R/W			
	10:0	Reserved		
		<table border="1"> <tr> <td>Default Value:</td><td>00000000000b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	00000000000b
Default Value:	00000000000b			
Access:	RO			

IA32_MTRR_PHYSMASK4_H - IA32 MTRR PHYSMASK4 High

MTRR_PHYSMASK4_H - IA32 MTRR PHYSMASK4 High				
Register Space: MMIO: 0/2/0				
Project: BDW				
Default Value: 0x00000000				
Size (in bits): 32				
Address: 0F1CCh				
Variable MTRR4				
DWord	Bit	Description		
0	31:7	Reserved		
		<table border="1"> <tr> <td>Default Value:</td><td>00000000000000000000000000000000b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	00000000000000000000000000000000b
Default Value:	00000000000000000000000000000000b			
Access:	RO			
	6:0	PhysMask		
		<table border="1"> <tr> <td>Default Value:</td><td>0000000b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Physical MASK for the address[38:32] of the variable MTRR.</p>	Default Value:	0000000b
Default Value:	0000000b			
Access:	R/W			

IA32_MTRR_PHYSMASK4_L - IA32_MTRR_PHYSMASK4 Low

MTRR_PHYSMASK4_L - IA32 MTRR PHYSMASK4 Low				
Register Space:	MMIO: 0/2/0			
Project:	BDW			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0F1C8h			
Variable MTRR4				
DWord	Bit	Description		
0	31:12	PhysMask		
		<table border="1"> <tr> <td>Default Value:</td><td>00000h</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Physical MASK for the address[31:0] of the variable MTRR.</p>	Default Value:	00000h
Default Value:	00000h			
Access:	R/W			
Valid <table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Valid bit showing that MTRR decode is active.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b			
Access:	R/W			
	10:0	Reserved		
		<table border="1"> <tr> <td>Default Value:</td><td>00000000000b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	00000000000b
Default Value:	00000000000b			
Access:	RO			

IA32_MTRR_PHYSMASK5_H - IA32 MTRR PHYSMASK5 High

MTRR_PHYSMASK5_H - IA32 MTRR PHYSMASK5 High				
Register Space: MMIO: 0/2/0				
Project: BDW				
Default Value: 0x00000000				
Size (in bits): 32				
Address: 0F1DCh				
Variable MTRR5				
DWord	Bit	Description		
0	31:7	Reserved		
		<table border="1"> <tr> <td>Default Value:</td><td>00000000000000000000000000000000b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	00000000000000000000000000000000b
Default Value:	00000000000000000000000000000000b			
Access:	RO			
	6:0	PhysMask		
		<table border="1"> <tr> <td>Default Value:</td><td>0000000b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Physical MASK for the address[38:32] of the variable MTRR.</p>	Default Value:	0000000b
Default Value:	0000000b			
Access:	R/W			

IA32_MTRR_PHYSMASK5_L - IA32 MTRR PHYSMASK5 Low

MTRR_PHYSMASK5_L - IA32 MTRR PHYSMASK5 Low		
Variable MTRR5		
DWord	Bit	Description
0	31:12	PhysMask
		Default Value: 00000h Access: R/W Physical MASK for the address[31:0] of the variable MTRR.
		Valid Default Value: 0b Access: R/W Valid bit showing that MTRR decode is active.
	10:0	Reserved
		Default Value: 00000000000b Access: RO

IA32_MTRR_PHYSMASK6_H - IA32 MTRR PHYSMASK6 High

MTRR_PHYSMASK6_H - IA32 MTRR PHYSMASK6 High				
Register Space: MMIO: 0/2/0				
Project: BDW				
Default Value: 0x00000000				
Size (in bits): 32				
Address: 0F1ECh				
Variable MTRR6				
DWord	Bit	Description		
0	31:7	Reserved		
		<table border="1"> <tr> <td>Default Value:</td><td>00000000000000000000000000000000b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	00000000000000000000000000000000b
Default Value:	00000000000000000000000000000000b			
Access:	RO			
	6:0	PhysMask		
		<table border="1"> <tr> <td>Default Value:</td><td>0000000b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Physical MASK for the address[38:32] of the variable MTRR.</p>	Default Value:	0000000b
Default Value:	0000000b			
Access:	R/W			

IA32_MTRR_PHYSMASK6_L - IA32 MTRR PHYSMASK6 Low

MTRR_PHYSMASK6_L - IA32 MTRR PHYSMASK6 Low				
Register Space:	MMIO: 0/2/0			
Project:	BDW			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0F1E8h			
Variable MTRR6				
DWord	Bit	Description		
0	31:12	PhysMask		
		<table border="1"> <tr> <td>Default Value:</td><td>00000h</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Physical MASK for the address[31:0] of the variable MTRR.</p>	Default Value:	00000h
Default Value:	00000h			
Access:	R/W			
Valid <table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Valid bit showing that MTRR decode is active.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b			
Access:	R/W			
	10:0	Reserved		
		<table border="1"> <tr> <td>Default Value:</td><td>00000000000b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	00000000000b
Default Value:	00000000000b			
Access:	RO			

IA32_MTRR_PHYSMASK7_H - IA32 MTRR PHYSMASK7 High

MTRR_PHYSMASK7_H - IA32 MTRR PHYSMASK7 High				
Register Space: MMIO: 0/2/0				
Project: BDW				
Default Value: 0x00000000				
Size (in bits): 32				
Address: 0F1FCh				
Variable MTRR7				
DWord	Bit	Description		
0	31:7	Reserved		
		<table border="1"> <tr> <td>Default Value:</td><td>00000000000000000000000000000000b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	00000000000000000000000000000000b
Default Value:	00000000000000000000000000000000b			
Access:	RO			
	6:0	PhysMask		
		<table border="1"> <tr> <td>Default Value:</td><td>0000000b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Physical MASK for the address[38:32] of the variable MTRR.</p>	Default Value:	0000000b
Default Value:	0000000b			
Access:	R/W			

IA32_MTRR_PHYSMASK7_L - IA32_MTRR_PHYSMASK7 Low

MTRR_PHYSMASK7_L - IA32_MTRR_PHYSMASK7 Low		
Variable MTRR7		
DWord	Bit	Description
0	31:12	PhysMask
		Default Value: 00000h Access: R/W Physical MASK for the address[31:0] of the variable MTRR.
		Valid Default Value: 0b Access: R/W Valid bit showing that MTRR decode is active.
	10:0	Reserved
		Default Value: 00000000000b Access: RO

IA32_MTRR_PHYSMASK8_H - IA32 MTRR PHYSMASK8 High

MTRR_PHYSMASK8_H - IA32 MTRR PHYSMASK8 High				
Register Space: MMIO: 0/2/0				
Project: BDW				
Default Value: 0x00000000				
Size (in bits): 32				
Address: 0F20Ch				
Variable MTRR8				
DWord	Bit	Description		
0	31:7	Reserved		
		<table border="1"> <tr> <td>Default Value:</td><td>00000000000000000000000000000000b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	00000000000000000000000000000000b
Default Value:	00000000000000000000000000000000b			
Access:	RO			
	6:0	PhysMask		
		<table border="1"> <tr> <td>Default Value:</td><td>0000000b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Physical MASK for the address[38:32] of the variable MTRR.</p>	Default Value:	0000000b
Default Value:	0000000b			
Access:	R/W			

IA32_MTRR_PHYSMASK8_L - IA32 MTRR PHYSMASK8 Low

MTRR_PHYSMASK8_L - IA32 MTRR PHYSMASK8 Low		
Variable MTRR8		
DWord	Bit	Description
0	31:12	PhysMask
		Default Value: 00000h Access: R/W Physical MASK for the address[31:0] of the variable MTRR.
		Valid
11	11	Default Value: 0b Access: R/W Valid bit showing that MTRR decode is active.
		Reserved
		Default Value: 00000000000b Access: RO

IA32_MTRR_PHYSMASK9_H - IA32 MTRR PHYSMASK9 High

MTRR_PHYSMASK9_H - IA32 MTRR PHYSMASK9 High				
Register Space: MMIO: 0/2/0				
Project: BDW				
Default Value: 0x00000000				
Size (in bits): 32				
Address: 0F21Ch				
Variable MTRR9				
DWord	Bit	Description		
0	31:7	Reserved		
		<table border="1"> <tr> <td>Default Value:</td><td>00000000000000000000000000000000b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	00000000000000000000000000000000b
Default Value:	00000000000000000000000000000000b			
Access:	RO			
	6:0	PhysMask		
		<table border="1"> <tr> <td>Default Value:</td><td>0000000b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Physical MASK for the address[38:32] of the variable MTRR.</p>	Default Value:	0000000b
Default Value:	0000000b			
Access:	R/W			

IA32_MTRR_PHYSMASK9_L - IA32 MTRR PHYSMASK9 Low

MTRR_PHYSMASK9_L - IA32 MTRR PHYSMASK9 Low				
Register Space:	MMIO: 0/2/0			
Project:	BDW			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0F218h			
Variable MTRR9				
DWord	Bit	Description		
0	31:12	PhysMask		
		<table border="1"> <tr> <td>Default Value:</td><td>00000h</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Physical MASK for the address[31:0] of the variable MTRR.</p>	Default Value:	00000h
Default Value:	00000h			
Access:	R/W			
Valid <table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Valid bit showing that MTRR decode is active.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b			
Access:	R/W			
	10:0	Reserved		
		<table border="1"> <tr> <td>Default Value:</td><td>00000000000b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	00000000000b
Default Value:	00000000000b			
Access:	RO			

IA Vertices Count

IA_VERTICES_COUNT - IA Vertices Count		
Register Space: MMIO: 0/2/0 Project: BDW Source: RenderCS Default Value: 0x00000000, 0x00000000 Access: R/W Size (in bits): 64 Trusted Type: 1		
Address: 02310h Valid Projects: BDW		
This register stores the count of vertices processed by VF. This register is part of the context save and restore.		
DWord	Bit	Description
0	63:32	IA Vertices Count Report UDW Total number of vertices fetched by the VF stage. This count is updated for every input vertex as long as Statistics Enable is set in VF_STATE (see the Vertex Fetch Chapter in the 3D Volume.)
	31:0	IA Vertices Count Report LDW Total number of vertices fetched by the VF stage. This count is updated for every input vertex as long as Statistics Enable is set in VF_STATE (see the Vertex Fetch Chapter in the 3D Volume.)

IDI Cacheable Register

IDICA - IDI Cacheable Register				
DWord	Bit	Description		
0	31:30	<p>LLCWBCA</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO 00b.</p>	Access:	R/W
Access:	R/W			
29:28	<p>LLCPRFCA</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO 00b.</p>	Access:	R/W	
Access:	R/W			
27:26	<p>LLCPCCA</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO 00b.</p>	Access:	R/W	
Access:	R/W			
25:24	<p>LLCPDCA</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO 00b.</p>	Access:	R/W	
Access:	R/W			
23:22	<p>CLFCA</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO 00b.</p>	Access:	R/W	
Access:	R/W			
21:20	<p>POCA</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO 00b.</p>	Access:	R/W	
Access:	R/W			
19:18	<p>ITMCA</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO 00b.</p>	Access:	R/W	
Access:	R/W			

IDICA - IDI Cacheable Register

	17:16	WCILFCA	Access:	R/W
NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO 00b.				
	15:14	WILCA	Access:	R/W
NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO 00b. CANNOT BE FLEXED.				
	13:12	WCILCA	Access:	R/W
>NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO 00b. CANNOT BE FLEXED.				
	11:10	WBMCA	Access:	R/W
NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO 00b.				
	9:8	RFOCA	Access:	R/W
NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO 00b.				
	7:6	PORINCA	Access:	R/W
NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO 00b.				
	5:4	PRDCA	Access:	R/W
NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO 00b.				
	3:2	DRDCA	Access:	R/W
00b: Whatever the logic decides (so force feature is disabled) - Default. 01b: Always drive 0. 10b: Always drive 1. 11b: Reserved.				
	1:0	CRDCA	Access:	R/W
00b: Whatever the logic decides (so force feature is disabled) - Default. 01b: Always drive 0. 10b: Always drive 1. 11b: Reserved.				

IDI Control register

IDICR - IDI Control register						
DWord	Bit	Description				
0	31:23	<p>Spares</p> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>ECO purposes and Reserved.</p>	Project:	BDW	Access:	R/W
Project:	BDW					
Access:	R/W					
	22	<p>eDRAM Fill Flag Disable</p> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>C2Ureq.Misc[0] controls the eDRAM fill flag for the surfaces that are allocated to eLLC only. This particular bit disables use of this new control. 0b : eDRAM fill flag is enabled 1b : eDRAM fill flag is disabled</p>	Project:	BDW	Access:	R/W
Project:	BDW					
Access:	R/W					
	21:16	<p>IDI HASH MASK</p> <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>IDI HASH MASK: When a corresponding bit is set, the address line going into HASH for CBO ID calculation is forced to logic0.</p> <p>21=> Address Bit[11] 20=> Address Bit[10] 19=> Address Bit[9] 18=> Address Bit[8] 17=> Address Bit[7] 16=> Address Bit[6]</p> <p>Note: It is required for GFX Driver to set [19:16] to 1 when eDRAM configuration is enabled.</p>	Access:	R/W		
Access:	R/W					
	15	<p>GFX Data regulation</p> <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>BGF data regulation for incoming streams with chunkID detection.</p>	Access:	R/W		
Access:	R/W					
	14:10	Reserved				
	9	<p>RSVD</p> <table border="1"> <tr> <td>Access:</td><td>RO</td></tr> </table>	Access:	RO		
Access:	RO					

IDICR - IDI Control register

	8	Push Write Enable				
		<table border="1"> <tr> <td>Default Value:</td><td>1b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table>	Default Value:	1b	Access:	R/W
Default Value:	1b					
Access:	R/W					
		<p>Push Write Enable: Push writes are a new mechanism to deliver write data to Uncore. It provides two advantages. 1) Reduced TAG pass requirements 2) Only way to allocate into eLLC without going thru LLC.</p> <p>The downside is the fact that push writes are weakly ordered which means a synchronizing event is required to guarantee consistency of data.</p>				
Snoop Request control						
	7	<table border="1"> <tr> <td>Default Value:</td><td>1b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>1: Snoop is allowed only when there are no Pending response. 0: Means after every 24 u2c response we allow one snoop request to bypass.</p>	Default Value:	1b	Access:	R/W
Default Value:	1b					
Access:	R/W					
	6:4	LRUHint <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>000b: No LRUHint command sent to uncore. It is reserved. 001b: If LRUHint is asserted from SQ with a read or write command, IDI dispatcher chooses to send an LlcPrefData. 101b: If LRUHint is asserted from SQ with a read or write command, IDI dispatcher chooses to send an LLCPrefCode command on the C2U request channel. 010b: If LRUHint is asserted from SQ with a read/write command, IDI dispatcher chooses to send an LlcPrefRFO command on the C2U request channel. 011b: If LRUHint is asserted from SQ with a read, IDI dispatcher chooses to send LlcPrefData command on the C2U request channel. If LRUHint is asserted from SQ with a write, IDI dispatcher chooses to send LlcPrefRFO command on the C2U request channel. 111b: If LRUHint is asserted from SQ with a read, IDI dispatcher chooses to send LLCPrefCode command on the C2U request channel. If LRUHint is asserted from SQ with a write, IDI dispatcher chooses to send LlcPrefRFO command on the C2U request channel.</p>	Access:	R/W		
Access:	R/W					
	3	RSVD				
	2	Resport 1 disable <table border="1"> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>0: Default value - Both the Response ports on the BGF side are enabled. 1: Rsp Port1 Disable - Response Port1 is disable on the BGF Side.</p>	Access:	RO		
Access:	RO					

IDICR - IDI Control register

	1:0	SQ Grant Counter	
		Default Value:	01b
		Access:	R/W
SQ grant counter - 2-bit grant counter for SQ requests			
00b: 1 grant. 01b: 2 grants. 10b: 4 grants. 11b: 8 grants.			

IDI HASH Mask Register

DRBIDI3 - IDI HASH Mask Register

Register Space: MMIO: 0/2/0
 Project: BDW
 Default Value: 0x00000000 [BDW]
 Size (in bits): 32

Address: 01948h

DWord	Bit	Description						
0	31:10	Reserved <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>RO</td></tr> <tr> <td>Reserved</td><td></td></tr> </table>	Project:	BDW	Access:	RO	Reserved	
Project:	BDW							
Access:	RO							
Reserved								
	9:8	Reserved						
	7:6	Reserved <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>RO</td></tr> <tr> <td>Reserved</td><td></td></tr> </table>	Project:	BDW	Access:	RO	Reserved	
Project:	BDW							
Access:	RO							
Reserved								
	5:0	IDI HASH MASK <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>When corresponding MASK bit is set, the masked address bit going into HASH calculator is forced to be logic0.</p> <p>21=> Address Bit[11] 20=> Address Bit[10] 19=> Address Bit[9] 18=> Address Bit[8] 17=> Address Bit[7] 16=> Address Bit[6]</p> <p>For Gen8 with 128MB eDRAM eLLC, bits[5:0] should be set to 001111 (matching 9008[21:16] IDI hash mask)</p>	Access:	R/W				
Access:	R/W							

IDI Look up Register

IDILK2 - IDI Look up Register						
DWord	Bit	Description				
0	31:30	Spares <table border="1"> <tr> <td>Access:</td> <td>R/W Lock</td> </tr> </table>	Access:	R/W Lock		
Access:	R/W Lock					
	29	Spares1 <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Access:</td> <td>R/W Lock</td> </tr> </table> <p>Reserved for Slice 5.</p>	Project:	BDW	Access:	R/W Lock
Project:	BDW					
Access:	R/W Lock					
	28	Colloc bit for Slice 5 <table border="1"> <tr> <td>Access:</td> <td>R/W Lock</td> </tr> </table> <p>Co-located indicates that the Collocated Cbo should receive this request.</p>	Access:	R/W Lock		
Access:	R/W Lock					
	27	Direction bit for Slice 5 <table border="1"> <tr> <td>Access:</td> <td>R/W Lock</td> </tr> </table> <p>In Half ring uncore topologies this indicates if the 1: Going Up. 0: Going Down.</p>	Access:	R/W Lock		
Access:	R/W Lock					
	26	Polarity bit for Slice 5 <table border="1"> <tr> <td>Access:</td> <td>R/W Lock</td> </tr> </table> <p>Polarity based on the current core Slice ID and the Destination Cbo ID - should this request be sent to the rings in Even or Odd cycles (this is basically the Distance between the source and destination). 1 - Even. 0 - Odd.</p>	Access:	R/W Lock		
Access:	R/W Lock					
	25	For Me for Slice 5 <table border="1"> <tr> <td>Access:</td> <td>R/W Lock</td> </tr> </table> <p>The next slice the Target of this request (MyNeighbourId == DestCbold).</p>	Access:	R/W Lock		
Access:	R/W Lock					

IDILK2 - IDI Look up Register

	24	Spares2	
		Project:	BDW
		Access:	R/W Lock
Reserved for Slice 4.			
	23	Colloc bit for Slice 4	
		Access:	R/W Lock
Co-located indicates that the Collocated Cbo should receive this request.			
	22	Direction bit for Slice 4	
		Access:	R/W Lock
In Half ring uncore topologies this indicates if the 1: Going Up. 0: Going Down.			
	21	Polarity Bit for Slice 4	
		Access:	R/W Lock
Polarity based on the current core Slice ID and the Destination Cbo ID - should this request be sent to the rings in Even or Odd cycles (this is basically the Distance between the source and destination). 1 - Even. 0 - Odd.			
	20	For Me bit for Slice 4	
		Access:	R/W Lock
The next slice the Target of this request (MyNeighbourId == DestCbold).			
	19	Spare for Slice 3	
		Project:	BDW
		Access:	R/W Lock
Reserved for Slice 3.			
	18	Colloc bit for Slice 3	
		Access:	R/W Lock
Co-located indicates that the Collocated Cbo should receive this request.			
	17	Direction bit for S3	
		Access:	R/W Lock
In Half ring uncore topologies this indicates if the 1: Going Up. 0: Going Down.			

IDILK2 - IDI Look up Register

	16	Polarity Bit for Slice 3				
		<table border="1"> <tr> <td>Access:</td><td>R/W Lock</td></tr> </table> <p>Polarity based on the current core Slice ID and the Destination Cbo ID - should this request be sent to the rings in Even or Odd cycles (this is basically the Distance between the source and destination). 1 - Even. 0 - Odd.</p>	Access:	R/W Lock		
Access:	R/W Lock					
For Me Bit for Slice 3						
	15	<table border="1"> <tr> <td>Access:</td><td>R/W Lock</td></tr> </table> <p>The next slice the Target of this request (MyNeigbourId == DestCbold).</p>	Access:	R/W Lock		
Access:	R/W Lock					
Spare for Slice 2						
	14	<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>R/W Lock</td></tr> </table> <p>Reserved for Slice 2.</p>	Project:	BDW	Access:	R/W Lock
Project:	BDW					
Access:	R/W Lock					
Colloc bit for Slice 2						
	13	<table border="1"> <tr> <td>Access:</td><td>R/W Lock</td></tr> </table> <p>Co-located indicates that the Collocated Cbo should receive this request.</p>	Access:	R/W Lock		
Access:	R/W Lock					
Direction Bit for Slice 2						
	12	<table border="1"> <tr> <td>Access:</td><td>R/W Lock</td></tr> </table> <p>In Half ring uncore topologies this indicates if the 1: Going Up. 0: Going Down.</p>	Access:	R/W Lock		
Access:	R/W Lock					
Polarity Bit for Slice 2						
	11	<table border="1"> <tr> <td>Access:</td><td>R/W Lock</td></tr> </table> <p>Polarity based on the current core Slice ID and the Destination Cbo ID - should this request be sent to the rings in Even or Odd cycles (this is basically the Distance between the source and destination). 1 - Even. 0 - Odd.</p>	Access:	R/W Lock		
Access:	R/W Lock					
For me Bit for Slice 2						
	10	<table border="1"> <tr> <td>Access:</td><td>R/W Lock</td></tr> </table> <p>The next slice the Target of this request (MyNeigbourId == DestCbold).</p>	Access:	R/W Lock		
Access:	R/W Lock					
Spare for Slice 1						
	9	<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>R/W Lock</td></tr> </table> <p>Reserved for Slice 1.</p>	Project:	BDW	Access:	R/W Lock
Project:	BDW					
Access:	R/W Lock					

IDILK2 - IDI Look up Register

	8	Colloc Bit for Slice 1				
		<table border="1"> <tr> <td>Access:</td><td>R/W Lock</td></tr> </table> <p>Co-located indicates that the Collocated Cbo should receive this request.</p>	Access:	R/W Lock		
Access:	R/W Lock					
Direction Bit for Slice 1						
	7	<table border="1"> <tr> <td>Access:</td><td>R/W Lock</td></tr> </table> <p>In Half ring uncore topologies this indicates if the 1: Going Up. 0: Going Down.</p>	Access:	R/W Lock		
Access:	R/W Lock					
Polarity Bit for Slice 1						
	6	<table border="1"> <tr> <td>Access:</td><td>R/W Lock</td></tr> </table> <p>Polarity based on the current core Slice ID and the Destination Cbo ID - should this request be sent to the rings in Even or Odd cycles (this is basically the Distance between the source and destination). 1 - Even. 0 - Odd.</p>	Access:	R/W Lock		
Access:	R/W Lock					
For Me Bit for Slice 1						
	5	<table border="1"> <tr> <td>Access:</td><td>R/W Lock</td></tr> </table> <p>The next slice the Target of this request (MyNeigbourId == DestCbOld).</p>	Access:	R/W Lock		
Access:	R/W Lock					
Spare for Slice 0						
	4	<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>R/W Lock</td></tr> </table> <p>Reserved for Slice 0.</p>	Project:	BDW	Access:	R/W Lock
Project:	BDW					
Access:	R/W Lock					
Colloc Bit for Slice 0						
	3	<table border="1"> <tr> <td>Access:</td><td>R/W Lock</td></tr> </table> <p>Co-located indicates that the Collocated Cbo should receive this request.</p>	Access:	R/W Lock		
Access:	R/W Lock					
Direction Bit in Slice0						
	2	<table border="1"> <tr> <td>Access:</td><td>R/W Lock</td></tr> </table> <p>Direction bit for Slice0: In Half ring uncore topologies this indicates if the request needs to be driven on the Up going (1) or the down (0) going ring direction. For Full ring it indicates Clock-wise (1) or counter clock-wise directions. 1: Going Up. 0: Going Down.</p>	Access:	R/W Lock		
Access:	R/W Lock					

IDILK2 - IDI Look up Register				
	1	<p>Polarity Bit for Slice 0</p> <table border="1"> <tr> <td>Access:</td><td>R/W Lock</td></tr> </table> <p>Polarity based on the current core Slice ID and the Destination Cbo ID - should this request be sent to the rings in Even or Odd cycles (this is basically the Distance between the source and destination).</p> <p>1 - Even. 0 - Odd.</p>	Access:	R/W Lock
Access:	R/W Lock			
0	<p>For Me bit for Slice0</p> <table border="1"> <tr> <td>Access:</td><td>R/W Lock</td></tr> </table> <p>The next slice the Target of this request (MyNeigbourId == DestCb0ld).</p>	Access:	R/W Lock	
Access:	R/W Lock			

IDILook up Table register

IDILK1 - IDILook up Table register						
DWord	Bit	Description				
0	31:20	Spares <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Access:</td> <td>R/W Lock</td> </tr> </table>	Project:	BDW	Access:	R/W Lock
Project:	BDW					
Access:	R/W Lock					
	19:15	GT Logical ID <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Access:</td> <td>R/W Lock</td> </tr> </table> <p>Logical ID for GT.</p>	Project:	BDW	Access:	R/W Lock
Project:	BDW					
Access:	R/W Lock					
	14	Spares1 <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Access:</td> <td>R/W Lock</td> </tr> </table> <p>Reserved for SA slice.</p>	Project:	BDW	Access:	R/W Lock
Project:	BDW					
Access:	R/W Lock					
	13	Colloc bit for SA Slice <table border="1"> <tr> <td>Access:</td> <td>R/W Lock</td> </tr> </table> <p>Co-located indicates that the Collocated Cbo should receive this request.</p>	Access:	R/W Lock		
Access:	R/W Lock					
	12	Direction Bit for SA <table border="1"> <tr> <td>Access:</td> <td>R/W Lock</td> </tr> </table> <p>In Half ring uncore topologies this indicates if the request needs to be driven on the Up going (1) or the down (0) going ring direction. For Full ring it indicates Clock-wise (1) or counter clock-wise directions. 1: Going Up. 0: Going Down.</p>	Access:	R/W Lock		
Access:	R/W Lock					
	11	Polarity bit for SA Slice <table border="1"> <tr> <td>Access:</td> <td>R/W Lock</td> </tr> </table> <p>Polarity based on the current core Slice ID and the Destination Cbo ID - should this request be sent to the rings in Even or Odd cycles (this is basically the Distance between the source and destination). 1 - Even. 0 - Odd.</p>	Access:	R/W Lock		
Access:	R/W Lock					

IDILK1 - IDILook up Table register

	10	For Me bit for SA		
		<table border="1"> <tr> <td>Access:</td><td>R/W Lock</td></tr> </table> <p>The next slice the Target of this request (MyNeigbourId == DestCb0ld).</p>	Access:	R/W Lock
Access:	R/W Lock			
Number of LLC SA Slices				
	9:5	<table border="1"> <tr> <td>Access:</td><td>R/W Lock</td></tr> </table> <p>Number of Slice information in the system. This register contains the number of LLC cache slices on the RING. Default: 0000b.</p>	Access:	R/W Lock
Access:	R/W Lock			
Colocated Slice ID for GT				
	4:0	<table border="1"> <tr> <td>Access:</td><td>R/W Lock</td></tr> </table> <p>This register contains the ID of the slice that is servicing GT's co-located cycles. The default is for slice0 to service GT.</p>	Access:	R/W Lock
Access:	R/W Lock			

IDI MESSAGES

IDIMSG - IDI MESSAGES						
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x00000000 Size (in bits): 32						
Address: 08500h						
IDI Message Register						
DWord	Bit	Description				
0	31:16	Mask Bits <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td colspan="2">Reserved.</td> </tr> </table>	Access:	RO	Reserved.	
	Access:	RO				
	Reserved.					
	15:13	RSVD <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO		
	Access:	RO				
	12	MCHECK COMPLETE <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td colspan="2">iMPH writes to this bit to initiate MCHECK COMPLETE Routine (PPPE flow). MBCunit will clear this bit once the PPPE flow is complete</td> </tr> </table>	Access:	R/W	iMPH writes to this bit to initiate MCHECK COMPLETE Routine (PPPE flow). MBCunit will clear this bit once the PPPE flow is complete	
	Access:	R/W				
	iMPH writes to this bit to initiate MCHECK COMPLETE Routine (PPPE flow). MBCunit will clear this bit once the PPPE flow is complete					
	11	Spare <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td colspan="2">Spare Messaging Bit with self-clear.</td> </tr> </table>	Access:	R/W	Spare Messaging Bit with self-clear.	
	Access:	R/W				
Spare Messaging Bit with self-clear.						
10	MBC Busy ACK <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td colspan="2">1 - Busy ACK from GPMunit(Non-Idle). 0 - Non Busy ACK from Gpmunit (Idle). This bit is valid only if 26th Bit is set.</td> </tr> </table>	Access:	R/W	1 - Busy ACK from GPMunit(Non-Idle). 0 - Non Busy ACK from Gpmunit (Idle). This bit is valid only if 26th Bit is set.		
Access:	R/W					
1 - Busy ACK from GPMunit(Non-Idle). 0 - Non Busy ACK from Gpmunit (Idle). This bit is valid only if 26th Bit is set.						
9	Reserved					
8	Reserved					
7	RSVD <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO			
Access:	RO					
6	Request to Block IDI <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td colspan="2">Block and Unblock IDI Request - usually done during CPD Entry and Exits. This is valid only if 22nd bit is set. Block IDI - CPD Entry = 1. Unblock IDI CPD Exit = 0.</td> </tr> </table>	Access:	R/W	Block and Unblock IDI Request - usually done during CPD Entry and Exits. This is valid only if 22nd bit is set. Block IDI - CPD Entry = 1. Unblock IDI CPD Exit = 0.		
Access:	R/W					
Block and Unblock IDI Request - usually done during CPD Entry and Exits. This is valid only if 22nd bit is set. Block IDI - CPD Entry = 1. Unblock IDI CPD Exit = 0.						

IDIMSG - IDI MESSAGES		
	5	Unblock MMIO ack Access: R/W Unblock MMIO ACK coming from SA. This is valid only if 21st bit is set.
	4	Mbcunit Arbitration request/Release ACK Access: R/W Arbitration request is sent during the MAE update. The ack is received from GPMunit. This is valid only if 20th bit is set. Arb req ack = 1. Arb release ack = 0.
	3	IDI Shutdown request Access: R/W IDI Shutdown Request from GPM to MBCunit. This is valid only if the 19th bit is set.
	2	IDI Wakeup Message Access: R/W IDI wakeup message from PM to MBCunit. This is valid only if 18th bit is set.
	1	Credit Active De-assertreq ACK Access: R/W Credit Active De-assertreq ACK - GPMunit sends to the MBCunit. This is valid only if the 17th bit of this register is set.
	0	RSVD Project: BDW Access: RO

IDI Self Snoop Register

IDISLFSNP - IDI Self Snoop Register				
DWord	Bit	Description		
0	31:30	LLCWBSNP <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>00b: Whatever the logic decides (so force feature is disabled) - Default. 01b: Always drive 0. 10b: Always drive 1. 11b: Reserved.</p>	Access:	R/W
Access:	R/W			
	29:28	LLCPRFOSNP <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO 00b. CANNOT BE FLEXED.</p>	Access:	R/W
Access:	R/W			
	27:26	LLCPCSNP <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO 00b. CANNOT BE FLEXED.</p>	Access:	R/W
Access:	R/W			
	25:24	LLCPDSNP <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO 00b. CANNOT BE FLEXED.</p>	Access:	R/W
Access:	R/W			
	23:22	CLFCA <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO 00b. CANNOT BE FLEXED.</p>	Access:	R/W
Access:	R/W			
	21:20	POCA <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO 00b. CANNOT BE FLEXED.</p>	Access:	R/W
Access:	R/W			
	19:18	ITMSNP <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>00b: Whatever the logic decides (so force feature is disabled) - Default. 01b: Always drive 0. 10b: Always drive 1. 11b: Reserved.</p>	Access:	R/W
Access:	R/W			
	17:16	WCILFSNP		

IDISLFSNP - IDI Self Snoop Register			
		Access:	R/W
NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO 00b. CANNOT BE FLEXED.			
15:14	WILSNP	Access:	R/W
NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO 00b. CANNOT BE FLEXED.			
13:12	WCILSNP	Access:	R/W
NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO 00b. CANNOT BE FLEXED.			
11:10	WBMSNP	Access:	R/W
NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO 00b. CANNOT BE FLEXED.			
9:8	RFOSNP	Access:	R/W
00b: Whatever the logic decides (so force feature is disabled) - Default. 01b: Always drive 0. 10b: Always drive 1. 11b: Reserved.			
7:6	PORINSNP	Access:	R/W
NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO 00b. CANNOT BE FLEXED.			
5:4	PRDSNP	Access:	R/W
NOTE - THIS SHOULD ALWAYS BE PROGRAMMED TO 00b. CANNOT BE FLEXED.			
3:2	DRDSNP	Access:	R/W
00b: Whatever the logic decides (so force feature is disabled) - Default. 01b: Always drive 0. 10b: Always drive 1. 11b: Reserved.			
1:0	CRDSP	Access:	R/W
00b: Whatever the logic decides (so force feature is disabled) - Default. 01b: Always drive 0. 10b: Always drive 1. 11b: Reserved.			

IDLE Messaging Register for Blitter Engine

MSG_IDLE_BCS - IDLE Messaging Register for Blitter Engine

Register Space: MMIO: 0/2/0

Project: BDW

Default Value: 0x00000000

Size (in bits): 16

Address: 0800Ch

Message registers have bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16].

To set bit0, for example, the data would be 0x0001_0001.

To clear bit0, for example, the data would be 0x0001_0000.

Note that mask bit is the data bit offset + 16.

Message registers are protected from non-GT writes via the Message Channel.

DWord	Bit	Description
0	15:11	Reserved Access: RO
	10:9	Reserved Project: BDW Access: RO
	8:6	Reserved Access: RO
	5	Flush and Block Acknowledgement Access: R/W Flush and Block Acknowledgement. 1'b0: Not flushed and blocked (default). 1'b1: Unit has flushed and blocked its pipeline.
	4	Preparation for Reset Acknowledgement Access: R/W Go Acknowledgement. 1'b0: Go=0 Ack (default). 1'b1: Go=1 Ack. Requirement is that when Go=0 request is sent, the agent has to indicate busy before sending the Go=0 acknowledgement. It can only go idle again once Go=1 is received.

MSG_IDLE_BCS - IDLE Messaging Register for Blitter Engine

	3:0	Idle Messaging	
		Access: Idle Messaging. Bit[3]. Secondary Pipe Clock Gating. 1'b0: Secondary pipe clock must be on (default). 1'b1: Secondary pipe clock may be gated. Only used by Render CS on DevBDW for the Fixed Function DOP. Bit[2]. Primary Pipe Clock Gating. 1'b0: Primary pipe clock must be on (default). 1'b1: Primary pipe clock may be gated. Bit[1]. C6 Allowed. 1'b0: Do not allow GT to enter C6 (default). 1'b1: GT may enter C6. Bit[0]. Idle Indication. 1'b0: Pipe is busy (default). 1'b1: Pipe is idle. ** See the Valid Combinations for Idle Messaging Table.	R/W

IDLE Messaging Register for Media0 Engine

MSG_IDLE_VCS0 - IDLE Messaging Register for Media0 Engine

Register Space: MMIO: 0/2/0

Project: BDW

Default Value: 0x00000000

Size (in bits): 16

Address: 08004h

Message registers have bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16].

To set bit0, for example, the data would be 0x0001_0001.

To clear bit0, for example, the data would be 0x0001_0000.

Note that mask bit is the data bit offset + 16.

Message registers are protected from non-GT writes via the Message Channel.

DWord	Bit	Description
0	15:11	Reserved Access: RO
	10:9	Reserved Project: BDW Access: RO
	8:6	Reserved Access: RO
	5	Flush and Block Acknowledgement Access: R/W Flush and Block Acknowledgement. 1'b0: Not flushed and blocked (default). 1'b1: Unit has flushed and blocked its pipeline.
	4	Preparation for Reset Acknowledgement Access: R/W Go Acknowledgement. 1'b0: Go=0 Ack (default). 1'b1: Go=1 Ack. Requirement is that when Go=0 request is sent, the agent has to indicate busy before sending the Go=0 acknowledgement. It can only go idle again once Go=1 is received.

MSG_IDLE_VCS0 - IDLE Messaging Register for Media0 Engine

	3:0	Idle Messaging	
		Access: Idle Messaging. Bit[3]. Secondary Pipe Clock Gating. 1'b0: Secondary pipe clock must be on (default). 1'b1: Secondary pipe clock may be gated. Only used by Render CS on BDW for the Fixed Function DOP. Bit[2]. Primary Pipe Clock Gating. 1'b0: Primary pipe clock must be on (default). 1'b1: Primary pipe clock may be gated. Bit[1]. C6 Allowed. 1'b0: Do not allow GT to enter C6 (default). 1'b1: GT may enter C6. Bit[0]. Idle Indication. 1'b0: Pipe is busy (default). 1'b1: Pipe is idle. ** See the Valid Combinations for Idle Messaging Table.	R/W

IDLE Messaging Register for Media1 Engine

MSG_IDLE_VCS1 - IDLE Messaging Register for Media1 Engine

Register Space: MMIO: 0/2/0

Project: BDW

Default Value: 0x00000000

Size (in bits): 16

Address: 08008h

Message registers have bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16].

To set bit0, for example, the data would be 0x0001_0001.

To clear bit0, for example, the data would be 0x0001_0000.

Note that mask bit is the data bit offset + 16.

Message registers are protected from non-GT writes via the Message Channel.

DWord	Bit	Description
0	15:11	Reserved Access: RO
	10:9	Reserved Project: BDW Access: RO
	8:6	Reserved Access: RO
	5	Flush and Block Acknowledgement Access: R/W Flush and Block Acknowledgement. 1'b0: Not flushed and blocked (default). 1'b1: Unit has flushed and blocked its pipeline.
	4	Preparation for Reset Acknowledgement Access: R/W Go Acknowledgement. 1'b0: Go=0 Ack (default). 1'b1: Go=1 Ack. Requirement is that when Go=0 request is sent, the agent has to indicate busy before sending the Go=0 acknowledgement. It can only go idle again once Go=1 is received.

MSG_IDLE_VCS1 - IDLE Messaging Register for Media1 Engine

	3:0	Idle Messaging	
		Access:	R/W
		Idle Messaging. Bit[3]. Secondary Pipe Clock Gating. 1'b0: Secondary pipe clock must be on (default). 1'b1: Secondary pipe clock may be gated. Only used by Render CS on BDW for the Fixed Function DOP. Bit[2]. Primary Pipe Clock Gating. 1'b0: Primary pipe clock must be on (default). 1'b1: Primary pipe clock may be gated. Bit[1]. C6 Allowed. 1'b0: Do not allow GT to enter C6 (default). 1'b1: GT may enter C6. Bit[0]. Idle Indication. 1'b0: Pipe is busy (default). 1'b1: Pipe is idle.	
		** See the Valid Combinations for Idle Messaging Table.	

IDLE Messaging Register for Render Engine

MSG_IDLE_CS - IDLE Messaging Register for Render Engine					
DWord	Bit	Description			
0	31:16	<p>Context Save Mask</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>When context save is in progress, mask is forced to particular value to save off messages that need to be retained across an RC6 event.</p> <p>Currently for this register, the following fields are context saved and restored for an RC6 event: [7] GPGPU_ACTIVE. [6] MEDIA_ACTIVE.</p>	Access:	R/W	
Access:	R/W				
15:9	<p>Reserved</p> <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Project:	BDW	Access:	RO
Project:	BDW				
Access:	RO				
7	<p>GPGPU Active Load Indication</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Active Load Indication - bits[7:6] of this register.</p> <p>2'b00: Render load is being executed (default).</p> <p>2'b01: Media load is being executed.</p> <p>2'b10: GPGPU load is being executed.</p> <p>2'b11: Undefined.</p> <p>GPMunit self-clears this bit upon sampling.</p>	Access:	R/W		
Access:	R/W				

MSG_IDLE_CS - IDLE Messaging Register for Render Engine

	6	Media Active Load Indication	
		Access:	R/W
		<p>Active Load Indication - bits[7:6] of this register.</p> <p>2'b00: Render load is being executed (default).</p> <p>2'b01: Media load is being executed.</p> <p>2'b10: GPGPU load is being executed.</p> <p>2'b11: Undefined.</p> <p>GPMunit self-clears this bit upon sampling.</p>	
	5	Flush and Block Acknowledgement	
		Access:	R/W
		<p>Flush and Block Acknowledgement.</p> <p>1'b0: Not flushed and blocked (default).</p> <p>1'b1: Unit has flushed and blocked its pipeline.</p>	
	4	Preparation for Reset Acknowledgement	
		Access:	R/W
		<p>Go Acknowledgement.</p> <p>1'b0: Go=0 Ack (default).</p> <p>1'b1: Go=1 Ack.</p> <p>Requirement is that when Go=0 request is sent, the agent has to indicate busy before sending the Go=0 acknowledgement. It can only go idle again once Go=1 is received.</p>	
	3:0	Idle Messaging	
		Access:	R/W
		<p>Idle Messaging.</p> <p>Bit[3].</p> <p>Secondary Pipe Clock Gating.</p> <p>1'b0: Secondary pipe clock must be on (default).</p> <p>1'b1: Secondary pipe clock may be gated.</p> <p>Only used by Render CS on BDW for the Fixed Function DOP.</p> <p>Bit[2].</p> <p>Primary Pipe Clock Gating.</p> <p>1'b0: Primary pipe clock must be on (default).</p> <p>1'b1: Primary pipe clock may be gated.</p> <p>Bit[1].</p> <p>C6 Allowed.</p> <p>1'b0: Do not allow GT to enter C6 (default).</p> <p>1'b1: GT may enter C6.</p> <p>Bit[0].</p> <p>Idle Indication.</p> <p>1'b0: Pipe is busy (default).</p> <p>1'b1: Pipe is idle.</p> <p>** See the Valid Combinations for Idle Messaging Table.</p>	

IDLE Messaging Register for VEBox

MSG_IDLE_VECS - IDLE Messaging Register for VEBox		
DWord	Bit	Description
0	15:11	Reserved Access: RO
	10:9	Reserved Project: BDW Access: RO
	8:6	Reserved Access: RO
	5	Flush and Block Acknowledgement Access: R/W Flush and Block Acknowledgement. 1'b0: Not flushed and blocked (default). 1'b1: Unit has flushed and blocked its pipeline.
	4	Preparation for Reset Acknowledgement Access: R/W Go Acknowledgement. 1'b0: Go=0 Ack (default). 1'b1: Go=1 Ack. Requirement is that when Go=0 request is sent, the agent has to indicate busy before sending the Go=0 acknowledgement. It can only go idle again once Go=1 is received.

MSG_IDLE_VECS - IDLE Messaging Register for VEBox

	3:0	Idle Messaging	
		Access:	R/W
		Idle Messaging. Bit[3]. Secondary Pipe Clock Gating. 1'b0: Secondary pipe clock must be on (default). 1'b1: Secondary pipe clock may be gated. Only used by Render CS on BDW for the Fixed Function DOP. Bit[2]. Primary Pipe Clock Gating. 1'b0: Primary pipe clock must be on (default). 1'b1: Primary pipe clock may be gated. Bit[1]. C6 Allowed. 1'b0: Do not allow GT to enter C6 (default). 1'b1: GT may enter C6. Bit[0]. Idle Indication. 1'b0: Pipe is busy (default). 1'b1: Pipe is idle.	
		** See the Valid Combinations for Idle Messaging Table	

IDLE Messaging Register for Wi-Di

MSG_IDLE_WIN - IDLE Messaging Register for Wi-Di					
DWord	Bit	Description			
0	15:6	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO				
5	<p>Reserved</p> <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Project:	BDW	Access:	RO
Project:	BDW				
Access:	RO				
4	<p>Preparation for Reset Acknowledgement</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Go Acknowledgement. 1'b0: Go=0 Ack (default). 1'b1: Go=1 Ack. Requirement is that when Go=0 request is sent, the agent has to indicate busy before sending the Go=0 acknowledgement. It can only go idle again once Go=1 is received.</p>	Access:	R/W		
Access:	R/W				

MSG_IDLE_WIN - IDLE Messaging Register for Wi-Di

	3:0	Idle Messaging	
		Access:	R/W
		<p>Idle Messaging.</p> <p>Bit[3].</p> <p>Secondary Pipe Clock Gating.</p> <p>1'b0: Secondary pipe clock must be on (default).</p> <p>1'b1: Secondary pipe clock may be gated.</p> <p>Only used by Render CS on BDW for the Fixed Function DOP.</p> <p>Bit[2].</p> <p>Primary Pipe Clock Gating.</p> <p>1'b0: Primary pipe clock must be on (default).</p> <p>1'b1: Primary pipe clock may be gated.</p> <p>Bit[1].</p> <p>C6 Allowed.</p> <p>1'b0: Do not allow GT to enter C6 (default).</p> <p>1'b1: GT may enter C6.</p> <p>Bit[0].</p> <p>Idle Indication.</p> <p>1'b0: Pipe is busy (default).</p> <p>1'b1: Pipe is idle.</p> <p>** See the Valid Combinations for Idle Messaging Table.</p>	

Idle Switch Delay

IDLEDLY - Idle Switch Delay					
Register Space: MMIO: 0/2/0 Project: BDW Source: RenderCS Default Value: 0x00000000 Access: R/W Size (in bits): 32					
Address: 0223Ch					
The IDLEDLY register contains an Idle Delay field which specifies the minimum number of microseconds allowed for command streamer to wait before a context is switched out leading to IDLE state in Execlist mode, i.e following this context switch there is no active element available in HW to execute. A default value of 0, means that by default, there is no restriction to wait on a context switch leading to IDLE. This register has no significance when Execlists are not enabled.					
DWord	Bit	Description			
0	31:21	Reserved <table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ	
	Format:	MBZ			
20:0	IDLE Delay <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U21</td></tr> </table> <p>Minimum number of micro-seconds allowed</p>	Project:	All	Format:	U21
Project:	All				
Format:	U21				

Immediate Command Output Interface

ICOI - Immediate Command Output Interface				
DWord	Bit	Description		
0	31:0	<p>Immediate Command Write</p> <table border="1"> <tr> <td>Default Value:</td> <td>0h</td> </tr> </table> <p>Programming Notes</p> <p>The command to be sent to the codec via the Immediate Command mechanism is written to this register. The command stored in this register is sent out over the link during the next available frame after a 1 is written to the ICB bit.</p>	Default Value:	0h
Default Value:	0h			

Immediate Command Status

ICS - Immediate Command Status													
DWord	Bit	Description											
0	31:2	<p>Reserved</p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ									
Format:	MBZ												
	1	<p>Immediate Result Valid</p> <table border="1"> <tr> <td>Access:</td> <td>R/WC</td> </tr> </table> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Response_Read [Default]</td> <td>See ProgrammingNotes</td> </tr> <tr> <td>1b</td> <td>Response_Available</td> <td>See ProgrammingNotes</td> </tr> </tbody> </table> <p>Programming Notes</p> <p>This bit is set to a '1' by hardware when a new response is latched into the IRR register. This is a status flag indicating that software may read the response from the Immediate Response register. Software must clear this bit (by writing a one to it) before issuing a new command so that the software may determine when a new response has arrived.</p>	Access:	R/WC	Value	Name	Description	0b	Response_Read [Default]	See ProgrammingNotes	1b	Response_Available	See ProgrammingNotes
Access:	R/WC												
Value	Name	Description											
0b	Response_Read [Default]	See ProgrammingNotes											
1b	Response_Available	See ProgrammingNotes											
	0	<p>Immediate Command Busy</p> <table border="1"> <tr> <td>Access:</td> <td>R/W Set</td> </tr> </table> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Command_Done [Default]</td> <td>See ProgrammingNotes</td> </tr> <tr> <td>1b</td> <td>Command_Available</td> <td>See ProgrammingNotes</td> </tr> </tbody> </table> <p>Programming Notes</p> <p>When this bit is read as a 0 it indicates that a new command may be issued using the Immediate Command mechanism. When this bit transitions from a 0 to a 1 (via software writing a 1), the controller issues the command currently stored in the Immediate Command register to the codec over the link. When the corresponding response is latched into the Immediate Response register, the controller hardware sets the IRV flag and clears the ICB bit back to 0. Note: While the CORB/RIRB mechanism is operating an Immediate Command must not be issued, otherwise the responses conflict. This must be enforced by software.</p>	Access:	R/W Set	Value	Name	Description	0b	Command_Done [Default]	See ProgrammingNotes	1b	Command_Available	See ProgrammingNotes
Access:	R/W Set												
Value	Name	Description											
0b	Command_Done [Default]	See ProgrammingNotes											
1b	Command_Available	See ProgrammingNotes											

Immediate Response Input Interface

IRII - Immediate Response Input Interface				
DWord	Bit	Description		
0	31:0	<p>Immediate Response Read</p> <table border="1"> <tr> <td>Default Value:</td> <td>0h</td> </tr> </table> <p>This register contains the response received from a codec resulting from a command sent via the Immediate Command mechanism. If multiple codecs responded in the same frame, there is no guarantee as to which response will be latched. Therefore broadcast-type commands must not be issued via the Immediate Command mechanism.</p>	Default Value:	0h
Default Value:	0h			

Indirect Context Pointer

INDIRECT_CTX - Indirect Context Pointer	
Register Space:	MMIO: 0/2/0
Project:	BDW
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
Address:	021C4h-021C7h
Name:	Indirect Context Pointer
ShortName:	INDIRECT_CTX_RCSUNIT
Address:	121C4h-121C7h
Name:	Indirect Context Pointer
ShortName:	INDIRECT_CTX_VCSUNIT0
Address:	1A1C4h-1A1C7h
Name:	Indirect Context Pointer
ShortName:	INDIRECT_CTX_VECSUNIT
Address:	1C1C4h-1C1C7h
Name:	Indirect Context Pointer
ShortName:	INDIRECT_CTX_VCSUNIT1
Address:	221C4h-221C7h
Name:	Indirect Context Pointer
ShortName:	INDIRECT_CTX_BCSUNIT
This register is used to program the indirect address to be executed between CS and SVG engine context if enabled. This will only get executed due to regular context save/restore and not during power restore. This register is part of the execution list context and will be executed per context. Only supported if execution list is enabled. There is no preempting workloads within this context.	
Programming Notes	
The following commands are not supported within Render CS indirect context:	
Command Name	
MI_WAIT_FOR_EVENT	RenderCS
MI_SEMAPHORE_SIGNAL	
MI_ARB_CHECK	
MI_RS_CONTROL	
MI_REPORT_HEAD	
MI_URB_ATOMIC_ALLOC	

INDIRECT_CTX - Indirect Context Pointer

MI_SUSPEND_FLUSH
MI_TOPOLOGY_FILTER
MI_RS_CONTEXT
MI_SET_CONTEXT
MI_URB_CLEAR
MI_SEMAPHORE_WAIT in Memory Poll Mode is not supported.
MI_BATCH_BUFFER_START
MI_CONDITIONAL_BATCH_BUFFER_END
MEDIA_OBJECT_WALKER
GPGPU_WALKER
3DPRIMITIVE
3DSTATE_BINDING_TABLE_POINTERS_VS
3DSTATE_BINDING_TABLE_POINTERS_HS
3DSTATE_BINDING_TABLE_POINTERS_DS
3DSTATE_BINDING_TABLE_POINTERS_GS
3DSTATE_BINDING_TABLE_POINTERS_PS
3DSTATE_GATHER_CONSTANT_VS
3DSTATE_GATHER_CONSTANT_GS
3DSTATE_GATHER_CONSTANT_HS
3DSTATE_GATHER_CONSTANT_DS
3DSTATE_GATHER_CONSTANT_PS
3DSTATE_DX9_CONSTANTF_VS
3DSTATE_DX9_CONSTANTF_HS
3DSTATE_DX9_CONSTANTF_DS
3DSTATE_DX9_CONSTANTF_GS
3DSTATE_DX9_CONSTANTF_PS
3DSTATE_DX9_CONSTANTI_VS
3DSTATE_DX9_CONSTANTI_HS
3DSTATE_DX9_CONSTANTI_DS
3DSTATE_DX9_CONSTANTI_GS
3DSTATE_DX9_CONSTANTI_PS
3DSTATE_DX9_CONSTANTB_VS
3DSTATE_DX9_CONSTANTB_HS
3DSTATE_DX9_CONSTANTB_DS
3DSTATE_DX9_CONSTANTB_GS
3DSTATE_DX9_CONSTANTB_PS

INDIRECT_CTX - Indirect Context Pointer

3DSTATE_DX9_LOCAL_VALID_VS
3DSTATE_DX9_LOCAL_VALID_DS
3DSTATE_DX9_LOCAL_VALID_HS
3DSTATE_DX9_LOCAL_VALID_GS
3DSTATE_DX9_LOCAL_VALID_PS
3DSTATE_DX9_GENERATE_ACTIVE_VS
3DSTATE_DX9_GENERATE_ACTIVE_HS
3DSTATE_DX9_GENERATE_ACTIVE_DS
3DSTATE_DX9_GENERATE_ACTIVE_GS
3DSTATE_DX9_GENERATE_ACTIVE_PS
3DSTATE_BINDING_TABLE_EDIT_VS
3DSTATE_BINDING_TABLE_EDIT_GS
3DSTATE_BINDING_TABLE_EDIT_HS
3DSTATE_BINDING_TABLE_EDIT_DS
3DSTATE_BINDING_TABLE_EDIT_PS
3DSTATE_CONSTANT_VS
3DSTATE_CONSTANT_GS
3DSTATE_CONSTANT_PS
3DSTATE_CONSTANT_HS
3DSTATE_CONSTANT_DS
MI_BATCH_BUFFER_END

DWord	Bit	Description					
0	31:6	Indirect CS Context Address <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Format:</td> <td style="padding: 2px;">GraphicsAddress[31:6]</td> </tr> </table> <p>Pointer to the Context in memory to be executed as a batch.</p>	Format:	GraphicsAddress[31:6]			
Format:	GraphicsAddress[31:6]						
5:0	Size of Indirect CS Context <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Format:</td> <td style="padding: 2px; text-align: right;">U6</td> </tr> </table> <p>This is the size of the Indirect Context for CS. This size supports up to 63 cache lines worth of commands where a cache line is 64B. If programmed to zero then the indirect fetch of the CS context is disabled.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="background-color: #d9e1f2; text-align: center; padding: 2px;">Value</th> <th style="background-color: #d9e1f2; text-align: center; padding: 2px;">Name</th> </tr> </thead> <tbody> <tr> <td style="padding: 2px; text-align: center;">[0,63]</td> <td></td> </tr> </tbody> </table>	Format:	U6	Value	Name	[0,63]	
Format:	U6						
Value	Name						
[0,63]							

Instruction Parser Mode Register

INSTPM - Instruction Parser Mode Register

Register Space:	MMIO: 0/2/0
Project:	BDW
Source:	RenderCS 0x00004080 [BDW:GT1, BDW:GT1.5, BDW:GT2:H, BDW:GT3:H, BDW:GT3E:J]
Access:	R/W, RO
Size (in bits):	32
Trusted Type:	1
Address:	020C0h

The INSTPM register is used to control the operation of the Instruction Parser. Certain classes of instructions can be disabled (ignored) - often useful for detecting performance bottlenecks. Also, Synchronizing Flush operations can be initiated - useful for ensuring the completion (vs. only parsing) of rendering instructions.

Programming Notes

- If an instruction type is disabled, the parser will read those instructions but not process them.
- Error checking will be performed even if the instruction is ignored.
- All Reserved bits are implemented.
- This Register is saved and restored as part of Context.

DWord	Bit	Description						
0	31:16	<p>Mask Bits</p> <table border="1"> <tr> <td>Format:</td> <td>Mask[15:0]</td> </tr> </table> <p>Masks: These bits serve as write enables for bits 15:0. If this register is written with any of these bits clear the corresponding bit in the field 15:0 will not be modified. Reading these bits always returns 0s.</p>	Format:	Mask[15:0]				
Format:	Mask[15:0]							
	15	<p>Reserved</p> <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	BDW	Access:	RO	Format:	MBZ
Project:	BDW							
Access:	RO							
Format:	MBZ							

INSTPM - Instruction Parser Mode Register

	14	Replay Mode											
		Project:		BDW									
		Format:		U1									
		This field controls the granularity of the replay mechanism when coming back into a previously preempted context.											
		<table border="1" style="width: 100%;"> <thead> <tr> <th style="background-color: #d9e1f2;">Value</th> <th style="background-color: #d9e1f2;">Name</th> <th style="background-color: #d9e1f2;">Description</th> </tr> </thead> <tbody> <tr> <td>1h</td> <td>Object Level Preemption [Default]</td> <td>Object Level. Preemption is done on an Object Level Boundary in VF. Objects send down by VF are completely rendered. Pipeline is flushed before switching to the next context. On resubmission of the context VF starts parsing from the object where it got preempted last time.</td> </tr> <tr> <td>0h</td> <td></td> <td>Drawcall Level. Pipeline is flushed before switching to the next context. Commands parsed are committed to completing before a context switch.</td> </tr> </tbody> </table>			Value	Name	Description	1h	Object Level Preemption [Default]	Object Level. Preemption is done on an Object Level Boundary in VF. Objects send down by VF are completely rendered. Pipeline is flushed before switching to the next context. On resubmission of the context VF starts parsing from the object where it got preempted last time.	0h		Drawcall Level. Pipeline is flushed before switching to the next context. Commands parsed are committed to completing before a context switch.
Value	Name	Description											
1h	Object Level Preemption [Default]	Object Level. Preemption is done on an Object Level Boundary in VF. Objects send down by VF are completely rendered. Pipeline is flushed before switching to the next context. On resubmission of the context VF starts parsing from the object where it got preempted last time.											
0h		Drawcall Level. Pipeline is flushed before switching to the next context. Commands parsed are committed to completing before a context switch.											
		Programming Notes											
		This bit must be set to 0 prior to any 3DPRIMITVE using trifan, polygon, lineloop or quadstrip topology.											
		This bit must be set to 0 prior to any 3DPRIMITVE using linestrip_adjacency and 3dstate_GS.enable is set to 1.											
	13	Reserved											
		Project:		BDW									
		Format:		Must Be One									
	12	Reserved											
		Project:		BDW									
	11	CLFLUSH Toggle											
		Project:		BDW									
		Access:		RO									
		Format:		U1									
		This bit changes polarity each time the MI_CLFLUSH command completes. This bit is Read Only.											
	10	Reserved											
	9:8	Reserved											
		Project:		BDW									
		Format:		MBZ									

INSTPM - Instruction Parser Mode Register

	7	Force Sync Command Ordering						
		<table border="1"> <tr> <td>Default Value:</td><td>1b</td></tr> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>Enable</td></tr> </table>	Default Value:	1b	Project:	BDW	Format:	Enable
Default Value:	1b							
Project:	BDW							
Format:	Enable							
		<p>By default, driver/OS synchronization commands (MI_STORE_DATA_IMM, for instance) can execute out of order with respect to 3D state and 3D primitive commands. When set, this bit forces ordering of these commands. See section 3.2.2 for a list of these commands.</p>						
	6	CONSTANT_BUFFER Address Offset Disable						
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>Disable</td></tr> </table>	Project:	BDW	Format:	Disable		
Project:	BDW							
Format:	Disable							
		<p>When this bit is clear, the 3DSTATE_CONSTANT_* Buffers' Starting Address is used as a DynamicStateOffset. That is, it serves as an offset from the Dynamic State Base Address. Accesses will be subject to Dynamic State bounds checking. When this bit is set, the 3DSTATE_CONSTANT_* Buffers' Starting Address is used as a true GraphicsAddress (not an offset). No bounds checking will be performed during access.</p>						
	5	Reserved						
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	BDW	Format:	MBZ		
Project:	BDW							
Format:	MBZ							
	4	Reserved						
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> </table>	Project:	BDW				
Project:	BDW							
	3	Media Instruction Disable						
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>U1</td></tr> </table>	Project:	BDW	Format:	U1		
Project:	BDW							
Format:	U1							
		<p>This bit instructs the Renderer instruction parser to parse and error-check Media instructions, but not execute them. Format = Disable</p>						
	2	3D Rendering Instruction Disable						
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>U1</td></tr> </table>	Project:	BDW	Format:	U1		
Project:	BDW							
Format:	U1							
		<p>This bit instructs the Renderer instruction parser to parse and error-check 3D Rendering instructions, but not execute them. This bit must always be set by software if 3D State Instruction Disable is set. Setting this bit without setting 3D State Instruction Disable is allowed.</p>						
		<p>Format = Disable</p>						
	1	3D State Instruction Disable						
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>Disable</td></tr> </table>	Project:	BDW	Format:	Disable		
Project:	BDW							
Format:	Disable							
	0	Texture Palette Load Instruction Disable						
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>U1</td></tr> </table>	Project:	BDW	Format:	U1		
Project:	BDW							
Format:	U1							
		<p>This bit instructs the Renderer instruction parser to parse and error-check Texture Palette Load instructions, but not execute them. Format = Disable</p>						

Internal GAM State

INTSTATE - Internal GAM State		
DWord	Bit	Description
0	31:0	Reserved

Interrupt Control

INTCTL - Interrupt Control										
Register Space: MMIO: 0/3/0 Project: BDW Default Value: 0x00000000 Access: R/W Size (in bits): 32										
DWord	Bit	Description								
0	31	Global Interrupt Enable								
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Disable [Default]</td> <td>GIE is disabled</td> </tr> <tr> <td>1h</td> <td>Enable</td> <td>GIE is enabled</td> </tr> </tbody> </table>		Value	Name	Description	0h	Disable [Default]	GIE is disabled	1h
Value	Name	Description								
0h	Disable [Default]	GIE is disabled								
1h	Enable	GIE is enabled								
<p>Programming Notes</p> <p>Global bit to enable device interrupt generation. When set to 1 the Intel HD Audio function is enabled to generate an interrupt. This control is in addition to any bits in the bus specific address space, such as the Interrupt Enable bit in the PCI Configuration Space. This bit is not affected by controller reset.</p>										
	30	Controller Interrupt Enable								
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Disable [Default]</td> <td>CIE is disabled</td> </tr> <tr> <td>1h</td> <td>Enable</td> <td>CIE is enabled</td> </tr> </tbody> </table>		Value	Name	Description	0h	Disable [Default]	CIE is disabled	1h
Value	Name	Description								
0h	Disable [Default]	CIE is disabled								
1h	Enable	CIE is enabled								
<p>Programming Notes</p> <p>This bit Enables the general interrupt for controller functions. When set to 1 (and GIE is enabled), the controller generates an interrupt when the CIS bit gets set. This bit is not affected by controller reset.</p>										
	29:3	Reserved								
		Format:	MBZ							

INTCTL - Interrupt Control

2:0	Stream Interrupt Enable <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Project:</td><td style="padding: 2px;">BDW</td></tr> </table> <table border="1" style="width: 100%; border-collapse: collapse; margin-top: 10px;"> <thead> <tr> <th style="text-align: center; padding: 2px;">Value</th><th style="text-align: center; padding: 2px;">Name</th><th style="text-align: center; padding: 2px;">Description</th></tr> </thead> <tbody> <tr> <td style="padding: 2px;">000b</td><td style="padding: 2px;">Disable [Default]</td><td style="padding: 2px;">All stream interrupts disabled</td></tr> <tr> <td style="padding: 2px;">001b</td><td style="padding: 2px;">Stream 1 Enable</td><td style="padding: 2px;">Output Stream 1 interrupt enabled</td></tr> <tr> <td style="padding: 2px;">010b</td><td style="padding: 2px;">Stream 2 Enable</td><td style="padding: 2px;">Output Stream 2 interrupt enabled</td></tr> <tr> <td style="padding: 2px;">100b</td><td style="padding: 2px;">Stream 3 Enable</td><td style="padding: 2px;">Output Stream 3 interrupt enabled</td></tr> <tr> <td style="padding: 2px;">111b</td><td style="padding: 2px;">All Enabled</td><td style="padding: 2px;">All streams enabled</td></tr> </tbody> </table> <div style="background-color: #e0e0ff; padding: 5px; margin-top: 10px; text-align: center;"> Programming Notes </div> <p style="margin-left: 20px;">When set to 1 the individual Streams are enabled to generate an interrupt when the corresponding stream status bits get set. A stream interrupt will be caused as a result of a buffer with IOC=1 in the BDL entry being completed, or as a result of a FIFO error (underrun or overrun) occurring. Control over the generation of each of these sources is in the associated Stream Descriptor. The streams are numbered and the SIE bits assigned sequentially, based on their order in the register set. Bit 0: Output Stream 1 Bit 1: Output Stream 2 Bit 2 : Output Stream 3</p>	Project:	BDW	Value	Name	Description	000b	Disable [Default]	All stream interrupts disabled	001b	Stream 1 Enable	Output Stream 1 interrupt enabled	010b	Stream 2 Enable	Output Stream 2 interrupt enabled	100b	Stream 3 Enable	Output Stream 3 interrupt enabled	111b	All Enabled	All streams enabled
Project:	BDW																				
Value	Name	Description																			
000b	Disable [Default]	All stream interrupts disabled																			
001b	Stream 1 Enable	Output Stream 1 interrupt enabled																			
010b	Stream 2 Enable	Output Stream 2 interrupt enabled																			
100b	Stream 3 Enable	Output Stream 3 interrupt enabled																			
111b	All Enabled	All streams enabled																			

Interrupt Line

INTRILINE_0_2_0_PCI - Interrupt Line						
Register Space: PCI: 0/2/0						
Project: BDW						
Default Value: 0x00000000						
Size (in bits): 8						
Address: 0003Ch						
<p>This register is used to communicate interrupt line routing information. The device itself does not use this value, rather it is used by device drivers and operating systems to determine priority and vector information.</p>						
DWord	Bit	Description				
0	7:0	<p>Interrupt Connection</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Used to communicate interrupt line routing information. POST software writes the routing information into this register as it initializes and configures the system. The value in this register indicates to which input of the system interrupt controller the device's interrupt pin is connected.</p>	Default Value:	00000000b	Access:	R/W
Default Value:	00000000b					
Access:	R/W					

Interrupt Line and Interrupt Pin

INTLN_INTPN - Interrupt Line and Interrupt Pin						
DWord	Bit	Description				
0	31:12	Reserved <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ		
Format:	MBZ					
	11:8	Interrupt Pin <table border="1"> <tr> <td>Default Value:</td> <td>01h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Interrupt Pin A</p>	Default Value:	01h	Access:	RO
Default Value:	01h					
Access:	RO					
	7:0	Interrupt Line <table border="1"> <tr> <td>Default Value:</td> <td>00h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Indicates to software the interrupt line that the interrupt pin is connected to. This register is not affected by FLR.</p>	Default Value:	00h	Access:	R/W
Default Value:	00h					
Access:	R/W					

Interrupt Mask Register

IMR - Interrupt Mask Register

Register Space: MMIO: 0/2/0

Project: BDW

Source: RenderCS

Default Value: 0xFFFFFFFF

Access: R/W, RO

Size (in bits): 32

Address: 020A8h

The IMR register is used by software to control which Interrupt Status Register bits are masked or unmasked. Unmasked bits will be reported in the IIR, possibly triggering a CPU interrupt, and will persist in the IIR until cleared by software. Masked bits will not be reported in the IIR and therefore cannot generate CPU interrupts.

DWord	Bit	Description												
0	31:0	<p>Interrupt Mask Bits</p> <p>Format: InterruptMask[32] Refer to the Interrupt Control Register section for bit definitions.</p> <p>This field contains a bit mask which selects which interrupt bits (from the ISR) are reported in the IIR. Reserved bits in the Interrupt Control Register are RO.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>FFFF FFFFh</td> <td>[Default]</td> <td></td> </tr> <tr> <td>0h</td> <td>Not Masked</td> <td>Will be reported in the IIR</td> </tr> <tr> <td>1h</td> <td>Masked</td> <td>Will not be reported in the IIR</td> </tr> </tbody> </table>	Value	Name	Description	FFFF FFFFh	[Default]		0h	Not Masked	Will be reported in the IIR	1h	Masked	Will not be reported in the IIR
Value	Name	Description												
FFFF FFFFh	[Default]													
0h	Not Masked	Will be reported in the IIR												
1h	Masked	Will not be reported in the IIR												

Interrupt Pin

INTRPIN_0_2_0_PCI - InterruptPin							
DWord	Bit	Description					
0	7:0	Interrupt Pin <table border="1"> <tr> <td>Default Value:</td><td>00000001b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>As a single function device, the IGD specifies INTA# as its interrupt pin. Hardwired to 01h = INTA#.</p>	Default Value:	00000001b	Access:	RO	
Default Value:	00000001b						
Access:	RO						

Interrupt Status

INTSTS - Interrupt Status										
Register Space: MMIO: 0/3/0 Project: BDW Default Value: 0x00000000 Access: R/W Variant Size (in bits): 32										
Address: 00024h-00027h										
DWord	Bit	Description								
0	31	Global Interrupt Status								
		<table border="1"> <tr> <td>Access:</td><td>RO</td></tr> </table>		Access:	RO					
Access:	RO									
<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Off [Default]</td><td>Interrupt off</td></tr> <tr> <td>1b</td><td>On</td><td>Interrupt on</td></tr> </tbody> </table>		Value	Name	Description	0b	Off [Default]	Interrupt off	1b	On	Interrupt on
Value	Name	Description								
0b	Off [Default]	Interrupt off								
1b	On	Interrupt on								
Programming Notes										
This bit is an OR of all of the interrupt status bits in this register.										
0	30	Controller Interrupt Status								
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Off [Default]</td><td>Interrupt off</td></tr> <tr> <td>1b</td><td>On</td><td>Interrupt on</td></tr> </tbody> </table>		Value	Name	Description	0b	Off [Default]	Interrupt off	1b
Value	Name	Description								
0b	Off [Default]	Interrupt off								
1b	On	Interrupt on								
Programming Notes										
		Status of general controller interrupt. A 1 indicates that an interrupt condition occurred due to a Response Interrupt, a Response Buffer Overrun Interrupt, CORB Memory Error Interrupt, Error Present Interrupt (Intel Reserved), or a SDIN State Change event. The exact cause can be determined by interrogating other registers. Note that a HW interrupt will not be generated unless the corresponding enable bit is set. This bit is an OR of all of the stated interrupt status bits for this register.								
0	29:3	Reserved								
		<table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>		Format:	MBZ					
Format:	MBZ									

INTSTS - Interrupt Status

		Stream Interrupt Status 3									
	2	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Project:</td><td style="padding: 2px;">BDW</td></tr> </table>	Project:	BDW							
Project:	BDW										
Programming Notes											
<p>A '1' indicates that an interrupt condition occurred on the corresponding Stream. Note that a HW interrupt will not be generated unless the corresponding enable bit is set. This bit is an OR of all of an individual stream's interrupt status bits. The streams are numbered and the SIS bits assigned sequentially, based on their order in the register set. Bit 2: Output Stream 3</p>											
	1	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Value</td><td style="padding: 2px;">Name</td><td style="padding: 2px;">Description</td></tr> <tr> <td style="padding: 2px;">0</td><td style="padding: 2px;">Off [Default]</td><td style="padding: 2px;">Stream interrupt off</td></tr> <tr> <td style="padding: 2px;">1</td><td style="padding: 2px;">On</td><td style="padding: 2px;">Stream interrupt On</td></tr> </table>	Value	Name	Description	0	Off [Default]	Stream interrupt off	1	On	Stream interrupt On
Value	Name	Description									
0	Off [Default]	Stream interrupt off									
1	On	Stream interrupt On									
Programming Notes											
<p>A '1' indicates that an interrupt condition occurred on the corresponding Stream. Note that a HW interrupt will not be generated unless the corresponding enable bit is set. This bit is an OR of all of an individual stream's interrupt status bits. The streams are numbered and the SIS bits assigned sequentially, based on their order in the register set. Bit 1: Output Stream 2</p>											
	0	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Value</td><td style="padding: 2px;">Name</td><td style="padding: 2px;">Description</td></tr> <tr> <td style="padding: 2px;">0</td><td style="padding: 2px;">Off [Default]</td><td style="padding: 2px;">Stream interrupt off</td></tr> <tr> <td style="padding: 2px;">1</td><td style="padding: 2px;">On</td><td style="padding: 2px;">Stream interrupt On</td></tr> </table>	Value	Name	Description	0	Off [Default]	Stream interrupt off	1	On	Stream interrupt On
Value	Name	Description									
0	Off [Default]	Stream interrupt off									
1	On	Stream interrupt On									
Programming Notes											
<p>A '1' indicates that an interrupt condition occurred on the corresponding Stream. Note that a HW interrupt will not be generated unless the corresponding enable bit is set. This bit is an OR of all of an individual stream's interrupt status bits. The streams are numbered and the SIS bits assigned sequentially, based on their order in the register set. Bit 0: Output Stream 1</p>											

I/O Base Address

IOBAR_0_2_0_PCI - I/O Base Address						
Register Space:	PCI: 0/2/0					
Project:	BDW					
Default Value:	0x00000001					
Size (in bits):	32					
Address:	00020h					
<p>This register provides the Base offset of the I/O registers within Device #2. Bits 15:6 are programmable allowing the I/O Base to be located anywhere in 16bit I/O Address Space. Bits 2:1 are fixed and return zero; bit 0 is hardwired to a one indicating that 8 bytes of I/O space are decoded. Access to the 8Bs of IO space is allowed in PM state D0 when IO Enable (PCICMD bit 0) set. Access is disallowed in PM states D1-D3 or if IO Enable is clear or if Device #2 is turned off or if Internal graphics is disabled through the fuse or fuse override mechanisms.</p> <p>Note that access to this IO BAR is independent of VGA functionality within Device #2. If accesses to this IO bar is allowed then all 8, 16 or 32 bit IO cycles from IA cores that falls within the 8B are claimed.</p>						
DWord	Bit	Description				
0	15:6	<p>IO Base Address</p> <table border="1"> <tr> <td>Default Value:</td><td>0000000000b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>FLR Resettable Set by the OS, these bits correspond to address signals [15:6].</p>	Default Value:	0000000000b	Access:	R/W
Default Value:	0000000000b					
Access:	R/W					
<p>Reserved</p> <table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ				
Format:	MBZ					
2:1	<p>Memory Type</p> <table border="1"> <tr> <td>Default Value:</td><td>00b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Hardwired to 0s to indicate 32-bit address.</p>	Default Value:	00b	Access:	RO	
Default Value:	00b					
Access:	RO					
<p>Memory/IO Space</p> <table border="1"> <tr> <td>Default Value:</td><td>1b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Hardwired to "1" to indicate IO space.</p>	Default Value:	1b	Access:	RO		
Default Value:	1b					
Access:	RO					

IPS_CTL

IPS_CTL								
Register Space:	MMIO: 0/2/0							
Project:	BDW							
Default Value:	0x00000000							
Access:	Double Buffered							
Size (in bits):	32							
Double Buffer Update Point:	Start of vertical blank OR pipe disabled							
Address:	43408h-4340Bh							
Name:	IPS Control							
ShortName:	IPS_CTL							
Valid Projects:	BDW							
Power:	Always on							
Reset:	soft							
IPS is tied to the pipe A output before the panel fitter.								
Programming Notes								
IPS increases the number of pixels that can be pre-fetched during the vertical blank and reduces how quickly the palette/gamma can be programmed. This can make it difficult to program palette/gamma seamlessly while IPS is enabled.								
Restriction								
IPS is only supported with pipe pixel formats of 8:8:8 or less.								
This register is normally under hardware control. Hardware will dynamically enable and disable IPS as needed. Software must use the GT Driver Mailbox to control IPS instead of writing this register. Follow the programming sequence in the Intermediate Pixel Storage overview section.								
DWord	Bit	Description						
0	31	<p>Enable IPS</p> <p>This bit is used to enable the IPS function.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Disable</td></tr> <tr> <td>1b</td><td>Enable</td></tr> </tbody> </table> <p>Workaround</p> <p>Do not enable IPS when the pipe pixel rate is greater than 95% of the CDCLK frequency. The pipe pixel rate is the port pixel rate multiplied by the pipe scaler down scale amount.</p>	Value	Name	0b	Disable	1b	Enable
Value	Name							
0b	Disable							
1b	Enable							

IPS_CTL	
	Restriction
	IPS must be enabled and disabled following the sequence in the Intermediate Pixel Storage overview section. See programming note above about controlling IPS through the GT Driver Mailbox.
30:27	Spare 30 27 Bit 30 indicates that IPS is under hardware control. Bits 29:27 are spares.
26:24	Reserved
23:21	Spare 23 21 Spare bits
20	Reserved
19:6	Spare 19 6 Spare bits
5	Reserved
4	Reserved
3	Reserved
2	Reserved
1	Reserved
0	Reserved

IPS_STATUS

IPS_STATUS			
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x00000000 Access: R/WC Size (in bits): 32			
Address: 43410h-43413h Name: IPS Status ShortName: IPS_STATUS Valid Projects: BDW Power: Always on Reset: soft			
DWord	Bit	Description	
0	31	Full Frame	Access: R/WC
		This field is tied to 0.	
	30	Pixel Count Mismatch	Access: R/WC
		This bit is set if the wrong number of pixels is decompressed for a line. Write 1b to to clear the bit.	
29:12	29:12	Reserved	Format: MBZ
	11:0	Last Comp Amount	Access: RO
		This field is tied to 0.	

KCR GAM slave counter High part

KCR_CTR_SLAVE_H - KCR GAM slave counter High part								
Register Space:	MMIO: 0/2/0							
Project:	BDW							
Default Value:	0x00000000							
Size (in bits):	32							
Address:	0482Ch							
DWord	Bit	Description						
0	31:0	<p>KCR Slave Counter High</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> <tr> <td colspan="2">Slave High counter[63:32] for KCR</td></tr> </table>	Default Value:	00000000h	Access:	R/W	Slave High counter[63:32] for KCR	
Default Value:	00000000h							
Access:	R/W							
Slave High counter[63:32] for KCR								

KCR GAM slave counter Low part

KCR_CTR_SLAVE_L-KCRGAMslavecounterLowpart						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04828h					
DWord	Bit	Description				
0	31:0	<p>KCR Slave Counter Low</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Slave Low counter[31:0] for KCR</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

L3 Bank Status

L3STAT - L3 Bank Status						
DWord	Bit	Description				
0	31	<p>L3 Fill Access Status bit</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>This register is Hardware Set and Clear. Set condition: set when the first command is seen on LTCC-LTCD interface. Reset condition: reset when the first Pipeline Flush command is seen on the LTCC-LTCD interface. Reset condition: This Flag will be reset only if we have atleast 1 modified line in the cache written by DC client.</p>	Access:	RO		
Access:	RO					
	30:0	<p>Reserved</p> <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Project:	BDW	Access:	RO
Project:	BDW					
Access:	RO					

L3CD Error Status register 1

L3CDERRST - L3CD Error Status register 1						
DWord	Bit	Description				
0	31:25	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO		
Access:	RO					
	24	<p>Double bit ECC error detected</p> <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W One Clear</td> </tr> </table> <p>Indicates if bank detected a double bit ECC error. When ltcd_lbcf_ecc_2bit_err_valid is set.</p>	Default Value:	0b	Access:	R/W One Clear
Default Value:	0b					
Access:	R/W One Clear					
	23:14	<p>Parity row address error</p> <table border="1"> <tr> <td>Default Value:</td> <td>0000000000b</td> </tr> <tr> <td>Access:</td> <td>R/W One Clear</td> </tr> </table> <p>Data array address which has parity B1. Report the data array address which has the Error. ltcd_lbcf_parity_err_rownum[9:0]. Once set by HW, it can be cleared only by MMIO Write of 1 to this register bit 13. Driver needs to write 1 to clear this bit.</p>	Default Value:	0000000000b	Access:	R/W One Clear
Default Value:	0000000000b					
Access:	R/W One Clear					
	13	<p>Parity Error Valid</p> <table border="1"> <tr> <td>Access:</td> <td>R/W One Clear</td> </tr> </table> <p>Parity Error valid. Report the Parity Error. ltcd_lbcf_parity_err_valid. Once set by HW, it can be cleared only by MMIO Write of 1 to this register bit 13. Driver needs to write 1 to clear this bit. when ltcd_lbcf_parity_err_valid is asserted, lbcf generates interrupt to ltiseql lbcf_ltiseql_parity_intr.</p>	Access:	R/W One Clear		
Access:	R/W One Clear					
	12:11	<p>Parity error bank number</p> <table border="1"> <tr> <td>Access:</td> <td>R/W One Clear</td> </tr> </table> <p>bank number which has parity error. Report the bank no. which has the Error. ltcd_lbcf_parity_err_banknum[1:0]. Once set by HW, it can be cleared only by MMIO Write of 1 to this register bit 13. Driver needs to write 1 to clear this bit.</p>	Access:	R/W One Clear		
Access:	R/W One Clear					

L3CDERRST - L3CD Error Status register 1

	10:8	Parity Error sub-bank no	
		Access:	R/W One Clear
Parity Error in sub bank: ltcd0_lbcf_parity_err_subbanknum[2:0]. Once set by HW, it can be cleared only by MMIO Write of 1 to this register bit 13. Driver needs to write 1 to clear this bit.			
	7	Parity report enable	
		Default Value:	1b
		Access:	R/W
Parity report enable (LCPRTYRPTEN): lbcf_csr_lc_parity_report_en. This is the parity reporting enable, by default it is enabled. When enabled parity is reported by ltcd to sarb. When disabled by driver, ltcd should not send out any parity error to SARB. Driver needs to write 1 to clear this bit.			
	6:0	Reserved	
		Access:	RO

L3 Control Register

L3CNTLREG - L3 Control Register																											
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x00000000 [BDW] Access: R/W Size (in bits): 32 Address: 07034h																											
Programming Notes The L3 allocation programming should assign all ways of the cache with no left over ways. Refer to L3 section for the recommended settings.																											
Any L3 configuration change that reduces the data cache allocation when strong IA coherency is used requires the full flush of L3 prior to the programming update. An explicit or implicit flush of L3 (DC Flush) through the command streamer doesn't result in flushing/invalidating the IA Coherent lines from L3. However this can be achieved by setting the " Pipe line flush Coherent lines " control bit in the "L3SQCREG4" register.																											
SLM comes up in an in-consistent state post reconfiguration and must be initialized by the driver for proper parity generation																											
DWord	Bit	Description																									
0	31:25	All L3 Client Pool <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> Number of ways allocated for the all client pool. This is a combined pool for all clients. <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th><th>Project</th></tr> </thead> <tbody> <tr> <td>[0h,40h]</td><td></td><td>Increments of 4KB</td><td>BDW:GT1</td></tr> <tr> <td>[0h,40h]</td><td></td><td>Increments of 8KB</td><td>BDW:GT2</td></tr> <tr> <td>[0h,40h]</td><td></td><td>Increments of 16KB</td><td>BDW:GT3</td></tr> <tr> <td>30h</td><td>[Default]</td><td></td><td>BDW</td></tr> </tbody> </table>		Project:	All	Access:	R/W	Value	Name	Description	Project	[0h,40h]		Increments of 4KB	BDW:GT1	[0h,40h]		Increments of 8KB	BDW:GT2	[0h,40h]		Increments of 16KB	BDW:GT3	30h	[Default]		BDW
Project:	All																										
Access:	R/W																										
Value	Name	Description	Project																								
[0h,40h]		Increments of 4KB	BDW:GT1																								
[0h,40h]		Increments of 8KB	BDW:GT2																								
[0h,40h]		Increments of 16KB	BDW:GT3																								
30h	[Default]		BDW																								
		Programming Notes When this field is non-zero, DC Way Assignment and Read Only Client Pool should be 0KB. Odd number values are not allowed. Please refer to L3 Section with Allocation and Programming for recommended settings.																									

L3CNTLREG - L3 Control Register																					
	24:18	DC Way Assignment																			
		<table border="1"> <tr> <td>Project:</td><td>All</td><td></td><td></td></tr> <tr> <td>Access:</td><td>R/W</td><td></td><td></td></tr> </table>				Project:	All			Access:	R/W										
Project:	All																				
Access:	R/W																				
		Number of ways allocated for DC. Note this allocation is only for DC data types.																			
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th><th>Project</th></tr> </thead> <tbody> <tr> <td>[0h,40h]</td><td>0KB-256KB</td><td>Increments of 4KB</td><td>BDW:GT1</td></tr> <tr> <td>[0h,40h]</td><td>0KB-512KB</td><td>Increments of 8KB</td><td>BDW:GT2</td></tr> <tr> <td>[0h,40h]</td><td>0KB-1024KB</td><td>Increments of 16KB</td><td>BDW:GT3</td></tr> </tbody> </table>				Value	Name	Description	Project	[0h,40h]	0KB-256KB	Increments of 4KB	BDW:GT1	[0h,40h]	0KB-512KB	Increments of 8KB	BDW:GT2	[0h,40h]	0KB-1024KB	Increments of 16KB	BDW:GT3
Value	Name	Description	Project																		
[0h,40h]	0KB-256KB	Increments of 4KB	BDW:GT1																		
[0h,40h]	0KB-512KB	Increments of 8KB	BDW:GT2																		
[0h,40h]	0KB-1024KB	Increments of 16KB	BDW:GT3																		
		Programming Notes																			
		Note: This field must be 0KB if All L3 Client Pool is non-zero. Odd number values are not allowed. Please refer to L3 HAS for valid programming values																			
	17:11	Read Only Client Pool																			
		<table border="1"> <tr> <td>Project:</td><td>All</td><td></td><td></td></tr> <tr> <td>Access:</td><td>R/W</td><td></td><td></td></tr> </table>				Project:	All			Access:	R/W										
Project:	All																				
Access:	R/W																				
		Number of ways allocated for Read Only L3 clients. This is a combined pool for all Read Only clients.																			
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th><th>Project</th></tr> </thead> <tbody> <tr> <td>[0h,40h]</td><td>0KB-256KB</td><td>Increments of 4KB</td><td>BDW:GT1</td></tr> <tr> <td>[0h,40h]</td><td>0KB-512KB</td><td>Increments of 8KB</td><td>BDW:GT2</td></tr> <tr> <td>[0h,40h]</td><td>0KB-1024KB</td><td>Increments of 16KB</td><td>BDW:GT3</td></tr> </tbody> </table>				Value	Name	Description	Project	[0h,40h]	0KB-256KB	Increments of 4KB	BDW:GT1	[0h,40h]	0KB-512KB	Increments of 8KB	BDW:GT2	[0h,40h]	0KB-1024KB	Increments of 16KB	BDW:GT3
Value	Name	Description	Project																		
[0h,40h]	0KB-256KB	Increments of 4KB	BDW:GT1																		
[0h,40h]	0KB-512KB	Increments of 8KB	BDW:GT2																		
[0h,40h]	0KB-1024KB	Increments of 16KB	BDW:GT3																		
		Programming Notes																			
		Note: This field must be 0KB if All L3 Client Pool is non-zero. Odd number values are not allowed. Please refer to L3 HAS for valid programming values																			
	10	Reserved																			
		<table border="1"> <tr> <td>Access:</td><td>R/W</td><td></td><td></td></tr> <tr> <td>Format:</td><td>PBC</td><td></td><td></td></tr> </table>				Access:	R/W			Format:	PBC										
Access:	R/W																				
Format:	PBC																				

L3CNTLREG - L3 Control Register																										
	9	<p>Error Detection Behavior Control</p> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> <tr> <td>Format:</td><td>Enable</td></tr> </table> <p>The L3 error detection can be enabled to hang the GPU on a non-recoverable error due to SER type events. Such option will be used when corresponding context has data consistency requirements. Once error detection is enabled, s/w has to initialize URB or SLM to all 0's (based on usage model) prior to execution of the workload. Initialization is required to clean up the error detection logic and syndrome tracking.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0h</td><td>[Default]</td><td>RTL does not hang on parity errors or double bit error</td></tr> <tr> <td>1h</td><td></td><td>RTL enforces a hang on parity errors or double bit error</td></tr> </tbody> </table>	Project:	BDW	Access:	R/W	Format:	Enable	Value	Name	Description	0h	[Default]	RTL does not hang on parity errors or double bit error	1h		RTL enforces a hang on parity errors or double bit error									
Project:	BDW																									
Access:	R/W																									
Format:	Enable																									
Value	Name	Description																								
0h	[Default]	RTL does not hang on parity errors or double bit error																								
1h		RTL enforces a hang on parity errors or double bit error																								
	8	<p>GPGPU L3 Credit Mode Enable</p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> <tr> <td>Format:</td><td>Enable</td></tr> </table> <p>This bit is required to be enabled under GPGPU workloads to provide the MAX latency coverage from L3 cache. It will override the registers 0xB100[18:14] and 0xB100[23:19], to 0 and the maximum value respectively.</p>	Project:	All	Access:	R/W	Format:	Enable																		
Project:	All																									
Access:	R/W																									
Format:	Enable																									
	7:1	<p>URB Allocation</p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Number of ways allocated for URB usage</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th><th>Project</th></tr> </thead> <tbody> <tr> <td>[0h,40h]</td><td></td><td>Increments of 4KB</td><td>BDW:GT1</td></tr> <tr> <td>[0h,40h]</td><td></td><td>Increments of 8KB</td><td>BDW:GT2</td></tr> <tr> <td>[0h,40h]</td><td></td><td>Increments of 16KB</td><td>BDW:GT3</td></tr> <tr> <td>30h</td><td>[Default]</td><td></td><td>BDW</td></tr> </tbody> </table> <p>Programming Notes</p> <p>Odd number values are not allowed. Please refer to L3 HAS for valid programming values</p>	Project:	All	Access:	R/W	Value	Name	Description	Project	[0h,40h]		Increments of 4KB	BDW:GT1	[0h,40h]		Increments of 8KB	BDW:GT2	[0h,40h]		Increments of 16KB	BDW:GT3	30h	[Default]		BDW
Project:	All																									
Access:	R/W																									
Value	Name	Description	Project																							
[0h,40h]		Increments of 4KB	BDW:GT1																							
[0h,40h]		Increments of 8KB	BDW:GT2																							
[0h,40h]		Increments of 16KB	BDW:GT3																							
30h	[Default]		BDW																							
	0	<p>SLM Mode Enable</p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> <tr> <td>Format:</td><td>Enable</td></tr> </table> <p>When enabled, a 64KB (per bank) region of L3 is reserved for SLM.</p>	Project:	All	Access:	R/W	Format:	Enable																		
Project:	All																									
Access:	R/W																									
Format:	Enable																									

L3 Control Register1

L3CNTLREG1 - L3 Control Register1

Register Space:	MMIO: 0/2/0
Project:	BDW 0x8C47FF80 [BDW]
Size (in bits):	32
Address:	0B10Ch

DWord	Bit	Description												
0	31:28	Data Fifo Depth Control <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td colspan="2">Data Fifo Depth Control (TS mode).</td> </tr> <tr> <td colspan="2">Value cannot be zero for normal operation. lbcf_csr_lc_datafifo_depth[3:0].</td> </tr> <tr> <th>Value</th><th>Name</th><th>Project</th></tr> <tr> <td>1000b</td><td>[Default]</td><td>BDW</td></tr> </table>	Access:	R/W	Data Fifo Depth Control (TS mode).		Value cannot be zero for normal operation. lbcf_csr_lc_datafifo_depth[3:0].		Value	Name	Project	1000b	[Default]	BDW
Access:	R/W													
Data Fifo Depth Control (TS mode).														
Value cannot be zero for normal operation. lbcf_csr_lc_datafifo_depth[3:0].														
Value	Name	Project												
1000b	[Default]	BDW												
27:24		Data Clock off time <table border="1"> <tr> <td>Default Value:</td> <td>1100b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td colspan="2">Data Clock off time (DATACLKOFF): Data Clock off time - Data block is shut off after these many number of clocks programmed in this register bits. lbcf_csr_lc_dataclkoff_time[3:0]. Min value to be 4'h100. It should be between 4'h4 : 4'hf.</td> </tr> </table>	Default Value:	1100b	Access:	R/W	Data Clock off time (DATACLKOFF): Data Clock off time - Data block is shut off after these many number of clocks programmed in this register bits. lbcf_csr_lc_dataclkoff_time[3:0]. Min value to be 4'h100. It should be between 4'h4 : 4'hf.							
Default Value:	1100b													
Access:	R/W													
Data Clock off time (DATACLKOFF): Data Clock off time - Data block is shut off after these many number of clocks programmed in this register bits. lbcf_csr_lc_dataclkoff_time[3:0]. Min value to be 4'h100. It should be between 4'h4 : 4'hf.														
23:20		TAG CLK OFF TIME <table border="1"> <tr> <td>Default Value:</td> <td>0100b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <th colspan="2">Description</th> </tr> <tr> <td colspan="2">TAG CLK OFF TIME (TAGCLKOFF): TAG Clock Off time. This is the time, which Clock gating Logic checks before it turns off the clock. lbcf_csr_lc_tagclkoff_time[3:0]. Value can be between 4'h4 - 4'hf.</td> </tr> <tr> <td colspan="2">Workaround is as follows: B10Ch, bits [23:20] programmed to 1000b (applicable to C0 also). So, program the tag clock off timer to 8 clocks as permanent work around to fix the issue found in clock gating when all the Invalidations line up(cs_*) in the same clock and a L3 cache access is seen during the 3rd invalidation and after the clocks are gated.</td> </tr> </table>	Default Value:	0100b	Access:	R/W	Description		TAG CLK OFF TIME (TAGCLKOFF): TAG Clock Off time. This is the time, which Clock gating Logic checks before it turns off the clock. lbcf_csr_lc_tagclkoff_time[3:0]. Value can be between 4'h4 - 4'hf.		Workaround is as follows: B10Ch, bits [23:20] programmed to 1000b (applicable to C0 also). So, program the tag clock off timer to 8 clocks as permanent work around to fix the issue found in clock gating when all the Invalidations line up(cs_*) in the same clock and a L3 cache access is seen during the 3rd invalidation and after the clocks are gated.			
Default Value:	0100b													
Access:	R/W													
Description														
TAG CLK OFF TIME (TAGCLKOFF): TAG Clock Off time. This is the time, which Clock gating Logic checks before it turns off the clock. lbcf_csr_lc_tagclkoff_time[3:0]. Value can be between 4'h4 - 4'hf.														
Workaround is as follows: B10Ch, bits [23:20] programmed to 1000b (applicable to C0 also). So, program the tag clock off timer to 8 clocks as permanent work around to fix the issue found in clock gating when all the Invalidations line up(cs_*) in the same clock and a L3 cache access is seen during the 3rd invalidation and after the clocks are gated.														

L3CNTLREG1 - L3 Control Register1

	19	L3 Aging Disable Bit								
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>L3 Aging Disable Bit (L3AGDIS): Aging Disable. <code>lbcf_csr_lc_agingdis.</code></p>	Default Value:	0b	Access:	R/W				
Default Value:	0b									
Access:	R/W									
	18:15	Fill aging								
		<table border="1"> <tr> <td>Default Value:</td><td>1111b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Fill aging (L3AGF): Aging Counter for Fill. <code>lbcf_csr_lc_fill_aging_cnt[3:0].</code> If bit B103.19 is 0 then this register value has to be nonzero.</p>	Default Value:	1111b	Access:	R/W				
Default Value:	1111b									
Access:	R/W									
	14:11	Aging Counter for Read 1 Port								
		<table border="1"> <tr> <td>Default Value:</td><td>1111b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Aging Counter for Read 1 Port (L3AGR1): Aging Counter for Read 1 Port. <code>lbcf_csr_lc_r1_aging_cnt[3:0].</code> If bit B103.19 is 0 then this register value has to be nonzero.</p>	Default Value:	1111b	Access:	R/W				
Default Value:	1111b									
Access:	R/W									
	10:7	L3 Aging Counter for R0								
		<table border="1"> <tr> <td>Default Value:</td><td>1111b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>L3 Aging Counter for R0 (L3AGR0): Aging Counter for R0 Port. <code>lbcf_csr_lc_r0_aging_cnt[3:0].</code> If bit B103.19 is 0 then this register value has to be nonzero.</p>	Default Value:	1111b	Access:	R/W				
Default Value:	1111b									
Access:	R/W									
	6:0	Reserved								
		<table border="1"> <tr> <td>Default Value:</td><td>000000b</td></tr> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>RO</td></tr> <tr> <td>Reserved.</td><td></td></tr> </table>	Default Value:	000000b	Project:	BDW	Access:	RO	Reserved.	
Default Value:	000000b									
Project:	BDW									
Access:	RO									
Reserved.										

L3 LRA 0

L3_LRA_0 - L3 LRA 0						
DWord	Bit	Description				
0	31:30	<p>L3</p> <table border="1"> <tr> <td>Default Value:</td> <td>00b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Which LRA should L3 use.</p>	Default Value:	00b	Access:	R/W
Default Value:	00b					
Access:	R/W					
29:20	<p>L3 LRA1 Min</p> <table border="1"> <tr> <td>Default Value:</td> <td>0011100000b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Minimum value of programmable LRA1.</p>	Default Value:	0011100000b	Access:	R/W	
Default Value:	0011100000b					
Access:	R/W					
19:10	<p>L3 LRA0 Max</p> <table border="1"> <tr> <td>Default Value:</td> <td>0011011111b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Maximum value of programmable LRA0.</p>	Default Value:	0011011111b	Access:	R/W	
Default Value:	0011011111b					
Access:	R/W					
9:0	<p>L3 LRA0 Min</p> <table border="1"> <tr> <td>Default Value:</td> <td>0000000000b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Minimum value of programmable LRA0.</p>	Default Value:	0000000000b	Access:	R/W	
Default Value:	0000000000b					
Access:	R/W					

L3 LRA 0 GPGPU

L3_LRA_0_GPGPU - L3 LRA 0 GPGPU								
DWord	Bit	Description						
0	31:30	L3 GPGPU <table border="1"> <tr> <td>Default Value:</td><td>00b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> <tr> <td colspan="2">Which LRA should L3 use.</td></tr> </table>	Default Value:	00b	Access:	R/W	Which LRA should L3 use.	
Default Value:	00b							
Access:	R/W							
Which LRA should L3 use.								
29:20	L3 LRA1 Min GPGPU <table border="1"> <tr> <td>Default Value:</td><td>0001010000b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> <tr> <td colspan="2">Minimum value of programmable LRA1.</td></tr> </table>	Default Value:	0001010000b	Access:	R/W	Minimum value of programmable LRA1.		
Default Value:	0001010000b							
Access:	R/W							
Minimum value of programmable LRA1.								
19:10	L3 LRA0 Max GPGPU <table border="1"> <tr> <td>Default Value:</td><td>0001001111b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> <tr> <td colspan="2">Maximum value of programmable LRA0.</td></tr> </table>	Default Value:	0001001111b	Access:	R/W	Maximum value of programmable LRA0.		
Default Value:	0001001111b							
Access:	R/W							
Maximum value of programmable LRA0.								
9:0	L3 LRA0 Min GPGPU <table border="1"> <tr> <td>Default Value:</td><td>0000000000b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> <tr> <td colspan="2">Minimum value of programmable LRA0.</td></tr> </table>	Default Value:	0000000000b	Access:	R/W	Minimum value of programmable LRA0.		
Default Value:	0000000000b							
Access:	R/W							
Minimum value of programmable LRA0.								

L3 LRA 1

L3_LRA_1 - L3 LRA 1						
DWord	Bit	Description				
0	31:30	<p>DC</p> <table border="1"> <tr> <td>Default Value:</td> <td>01b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Which LRA should DC use.</p>	Default Value:	01b	Access:	R/W
Default Value:	01b					
Access:	R/W					
29:20	<p>L3 LRA2 Max</p> <table border="1"> <tr> <td>Default Value:</td> <td>1001111111b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Maximum value of programmable LRA2.</p>	Default Value:	1001111111b	Access:	R/W	
Default Value:	1001111111b					
Access:	R/W					
19:10	<p>L3 LRA2 Min</p> <table border="1"> <tr> <td>Default Value:</td> <td>0111000000b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Minimum value of programmable LRA2.</p>	Default Value:	0111000000b	Access:	R/W	
Default Value:	0111000000b					
Access:	R/W					
9:0	<p>L3 LRA1 Max</p> <table border="1"> <tr> <td>Default Value:</td> <td>0110111111b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Maximum value of programmable LRA1.</p>	Default Value:	0110111111b	Access:	R/W	
Default Value:	0110111111b					
Access:	R/W					

L3 LRA 1 GPGPU

L3_LRA_1_GPGPU - L3 LRA 1 GPGPU						
DWord	Bit	Description				
0	31:30	<p>DC GPGPU</p> <table border="1"> <tr> <td>Default Value:</td> <td>01b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Which LRA should DC use.</p>	Default Value:	01b	Access:	R/W
Default Value:	01b					
Access:	R/W					
29:20	<p>L3 LRA2 Max GPGPU</p> <table border="1"> <tr> <td>Default Value:</td> <td>1001111111b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Maximum value of programmable LRA2.</p>	Default Value:	1001111111b	Access:	R/W	
Default Value:	1001111111b					
Access:	R/W					
19:10	<p>L3 LRA2 Min GPGPU</p> <table border="1"> <tr> <td>Default Value:</td> <td>1000011100b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Minimum value of programmable LRA2.</p>	Default Value:	1000011100b	Access:	R/W	
Default Value:	1000011100b					
Access:	R/W					
9:0	<p>L3 LRA1 Max GPGPU</p> <table border="1"> <tr> <td>Default Value:</td> <td>1000011011b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Maximum value of programmable LRA1.</p>	Default Value:	1000011011b	Access:	R/W	
Default Value:	1000011011b					
Access:	R/W					

L3 LRA 2

L3_LRA_2 - L3 LRA 2				
DWord	Bit	Description		
0	31:2	Reserved		
		<table border="1"> <tr> <td>Default Value:</td><td>00000000000000000000000000000000b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	00000000000000000000000000000000b
Default Value:	00000000000000000000000000000000b			
Access:	RO			
	1:0	Texture		
		<table border="1"> <tr> <td>Default Value:</td><td>10b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Which LRA should Texture use.</p>	Default Value:	10b
Default Value:	10b			
Access:	R/W			

L3 LRA 2 GPGPU

L3_LRA_2_GPGPU - L3 LRA 2 GPGPU				
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x00000002 Size (in bits): 32				
Address: 04DD8h				
DWord	Bit	Description		
0	31:2	Reserved		
		<table border="1"> <tr> <td>Default Value:</td><td>00000000000000000000000000000000b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	00000000000000000000000000000000b
Default Value:	00000000000000000000000000000000b			
Access:	RO			
	1:0	Texture GPGPU		
		<table border="1"> <tr> <td>Default Value:</td><td>10b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Which LRA should Texture use.</p>	Default Value:	10b
Default Value:	10b			
Access:	R/W			

L3 LRA 0 3D

L3_LRA_0_3D - L3 LRA 0 3D						
DWord	Bit	Description				
0	31:30	<p>L3 3D</p> <table border="1"> <tr> <td>Default Value:</td> <td>00b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Which LRA should L3 use.</p>	Default Value:	00b	Access:	R/W
Default Value:	00b					
Access:	R/W					
29:20	<p>L3 LRA1 Min 3D</p> <table border="1"> <tr> <td>Default Value:</td> <td>0001010000b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Minimum value of programmable LRA1.</p>	Default Value:	0001010000b	Access:	R/W	
Default Value:	0001010000b					
Access:	R/W					
19:10	<p>L3 LRA0 Max 3D</p> <table border="1"> <tr> <td>Default Value:</td> <td>0001001111b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Maximum value of programmable LRA0.</p>	Default Value:	0001001111b	Access:	R/W	
Default Value:	0001001111b					
Access:	R/W					
9:0	<p>L3 LRA0 Min 3D</p> <table border="1"> <tr> <td>Default Value:</td> <td>0000000000b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Minimum value of programmable LRA0.</p>	Default Value:	0000000000b	Access:	R/W	
Default Value:	0000000000b					
Access:	R/W					

L3 LRA 1 3D

L3_LRA_1_3D - L3 LRA 1 3D		
DWord	Bit	Description
0	31:30	DC 3D Default Value: 01b Access: R/W Which LRA should DC use.
		L3 LRA2 Max 3D Default Value: 1001111111b Project: BDW, :GT2:B Access: R/W Maximum value of programmable LRA2.
	19:10	L3 LRA2 Min 3D Default Value: 0010110100b Access: R/W Minimum value of programmable LRA2.
		L3 LRA1 Max 3D Default Value: 0010110011b Access: R/W Maximum value of programmable LRA1.

L3 LRA 2 3D

L3_LRA_2_3D - L3 LRA 2 3D				
Register Space:	MMIO: 0/2/0			
Project:	BDW			
Default Value:	0x00000002			
Size (in bits):	32			
Address:	04A18h			
DWord	Bit	Description		
0	31:2	Reserved		
		<table border="1"> <tr> <td>Default Value:</td><td>00000000000000000000000000000000b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	00000000000000000000000000000000b
Default Value:	00000000000000000000000000000000b			
Access:	RO			
	1:0	Texture 3D		
		<table border="1"> <tr> <td>Default Value:</td><td>10b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Which LRA should Texture use.</p>	Default Value:	10b
Default Value:	10b			
Access:	R/W			

L3 Messaging Register

MSG_L3_LPFC - L3 Messaging Register				
DWord	Bit	Description		
0	15:2	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
Access:	RO			
1	<p>Acknowledge that L3 Unblock Completed</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Acknowledge that L3 Unblock Completed. 1'b0: L3 unblock not complete yet (default). 1'b1: L3 unblock has completed. GPMunit self-clears this bit upon sampling.</p>	Access:	R/W	
Access:	R/W			
0	<p>Acknowledge that L3 Flush and Block Completed</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Acknowledge that L3 Flush and Block Completed. 1'b0: L3 flush and block not complete yet (default). 1'b1: L3 flush and block has completed. GPMunit self-clears this bit upon sampling.</p>	Access:	R/W	
Access:	R/W			

L3 SLM Register

L3SLMREG - L3 SLM Register

Register Space: MMIO: 0/2/0

Project: BDW

Default Value: 0x40000000

Size (in bits): 32

Address: 0B110h

DWord	Bit	Description				
0	31	<p>Disable Periodic SLM/SQ slot allocation</p> <table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Disable Periodic SLM/SQ slot allocation: When cfg_lslm_livelock_fairarb_dis=1 lslm unit always has the higher priority and lslm_lsqc_block to lsqcunit is asserted as long as there are requests in SLM FIFO. lbcf_csr_lslm_livelock_fairarb_dis.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
30:26	LSLM_SQ_PENDING_MAX	<table border="1"> <tr> <td>Default Value:</td><td>10000b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>If lslmunit has read data to be sent to lcbrunit this cfg register specifies the maximum number of clocks for which LSLMunit can block SQ request from being sent o lcbrunit. Default value = 8. Value cannot be zero. lbcf_csr_lslm_sqpend_max[4:0].</p>	Default Value:	10000b	Access:	R/W
Default Value:	10000b					
Access:	R/W					
25	LSLM address disable	<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>0 - Enable b2b addr matching fix. lslmunit should not block the cycle in fifo if there is a match in the pipeline. 1 - Disable b2b addr matching fix. lslmunit should block the cycle in fifo if there is a match in the pipeline. lbcf_csr_lslm_same_addr_dis. Default = 0.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
24:0	Reserved	<table border="1"> <tr> <td>Access:</td><td>RO</td></tr> </table>	Access:	RO		
Access:	RO					

L3 SQC register 4

L3SQCREG4 - L3 SQC register 4						
DWord	Bit	Description				
0	31	Reserved				
	30	L3SQ URB Read CAM Match Disable <table border="1"> <tr> <td>Default Value:</td><td>1b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>L3SQ URB Read CAM Match Disable (SQRURBRDCAMDIS): Disables the L3SQ Cam Match ability for URB Reads. By disabling, this allows a performance mode where URB reads are not dependent upon one another but only on any previous URB writes to the same address. This allows many URB reads to the same cacheline at any given time instead of serializing the requests. 1 = URB Read CAM matching is disabled; multiple URB reads to the same cacheline are allowed to be concurrent (default). 0 = URB Read CAM matching is enabled; multiple URB reads to the same cacheline are serialized. lbcf_csr_lsqc_urbrdcam_dis.</p>	Default Value:	1b	Access:	R/W
Default Value:	1b					
Access:	R/W					
	29:28	Traffic regulation in LSQC for URB lookup traffic <table border="1"> <tr> <td>Default Value:</td><td>00b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Traffic regulation in LSQC for URB lookup traffic (URB lookups are issued to ltcc these many clocks apart). 00b - Continuous. 01b - 4 clocks apart. 10b - 8 clocks apart. 11b - 16 clocks apart. lbcf_lsqc_urb_traffic.</p>	Default Value:	00b	Access:	R/W
Default Value:	00b					
Access:	R/W					
	27	LQSC RO PERF DIS <table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Default: 0. when set, RO performance mode is disabled and all Reads proceed only after Parent recycles. lbcf_csr_lsqc_roperf_dis.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					

L3SQCREG4 - L3 SQC register 4

	26	Order Cam Snp Reject				
		<table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
		<p>Default: 0. when set, all slots resulting in matches to.snp addr result in snprsp as REJECT instead of MISS. lbcf_csr_lsqc_ordercam_snpreject.</p>				
	25	LQSC RW PERF DIS				
		<table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
		<p>Default: 0. 0: Performance mode is enabled. when set, Rd to RW performance mode is disabled and all cycles proceed only after Parent recycles.</p>				
		<p>lbcf_csr_lsqc_rwperf_dis.</p>				
	24	LSQC read rtrn local crdt pre-consume disable				
		<table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
		<p>0 - Default, LSQD consumes the LNE local slicecredit when read return pending. 1 - LSQD consumes read rtrn credit in the clock it is ready to send read return data. lbcf_csr_lsqd_rdtrn_prcrdt_dis.</p>				
	23	LSQC Mem Write sqcam HITM response disable				
		<table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
		<p>0 - Default. 1 - This disables any Memory Write from cache with HitM tag response to respond for SQCAMs. lbcf_csr_lsqc_sqcam_l3tagrsphitm_dis.</p>				
	22	Non-IA coherent atomics enable				
		<table border="1"> <tr> <td>Default Value:</td> <td>1b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table>	Default Value:	1b	Access:	R/W
Default Value:	1b					
Access:	R/W					
		<p>0: Atomics in GTI. 1: Atomics in L3 (non-IA atomic) (default). lbcf_csr_lsqc_glblatmcs_l3. Value of this bit should be same as LNCF register bit 0xb008[0]. Value of this bit should be same as LBCF register bit 0xb11c[8].</p>				

L3SQCREG4 - L3 SQC register 4

	21	Pipe line flush Coherent lines		
		Default Value:	0b	
		Project:	BDW	
		Access:	R/W	
		1: Treat pipeline flush as invalidating even coherent lines along with non coherent lines . 0: Flush invalidates non coherent lines only. lbcf_csr_lsqc_pipeflush_coh.		
	20:0	Reserved		
		Project:	BDW	
		Access:	RO	

L3 SQC registers 1

L3SQCREG1 - L3 SQC registers 1						
DWord	Bit	Description				
0	31:24	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Reserved.</td> <td></td> </tr> </table>	Access:	RO	Reserved.	
Access:	RO					
Reserved.						
	23:19	<p>L3SQ General Priority Credit Initialization</p> <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>L3SQ General Priority Credit Initialization (SQGPCI): Number of general and high priority credits that SQ presents to L3 Arbiter blocks. This inherently also determines the depth of the SQ; reduce the number of credits and SQ uses fewer slots. Any value not listed here is considered Reserved. Gen priority credits is always greater than high priority credits. When this register is programmed through KMD, the crclk DOP clk gating should be disabled before the programming and be enabled ~100 clocks after the programming is done.</p> <p>Value # General Credits</p> <p>00000b 0 00001b 2 00010b 4 00011b 6 00100b 8 00101b 10 00110b 12 00111b 14 01000b 16 01001b</p>	Project:	BDW	Access:	R/W
Project:	BDW					
Access:	R/W					

L3SQCREG1 - L3 SQC registers 1

18	
01010b	
20	
01011b	
22	
01100b	
24 (default)	
01101b	
26	
01110b	
28	
01111b	
30	
10000b	
32	

Other values are not possible.
For BDW Need to go up to 32 credits.
lbcf_csr_lsqc_gen_credit_init[4:0].

Value	Name	Project
01100b	[Default]	BDW

18:14 L3SQ High Priority Credit Initialization

Default Value:	00100b
Project:	BDW
Access:	R/W

L3SQ High Priority Credit Initialization (SQHPCI):

Number of general and high priority credits that SQ presents to L3 Arbiter blocks. This inherently also determines the depth of the SQ; reduce the number of credits and SQ uses fewer slots.

Any value not listed here is considered Reserved.

gen priority credits is always greater than high priority credits.

When this register is programmed through KMD, the crclk DOP clk gating should be disabled before the programming and be enabled ~100 clocks after the programming is done.

Value

High Pri Credits

00000b	
0	
00001b	
2	
00010b	
4	
00011b	
6	
00100b	
8 (default)	
00101b	
10	

L3SQCREG1 - L3 SQC registers 1						
		00110b 12 00111b 14 01000b 16 01001b 18 01010b 20 01011b 22 01100b 24 01101b 26 01110b 28 01111b 30 10000b 32 Other values are not possible. lbcf_csr_lsqc_hp_credit_init[4:0]. lbcf_csr_lsqc_hp_credit_init[4:0] ++ lbcf_csr_lsqc_gen_credit_init[4:0] should always be less than or equal to 32.				
	13:10	Reserved <table border="1"> <tr> <td>Access:</td><td>RO</td></tr> <tr> <td colspan="2">Reserved.</td></tr> </table>	Access:	RO	Reserved.	
Access:	RO					
Reserved.						
	9	L3SQ Read Once Enable for Sampler Client <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> <tr> <td colspan="2">L3SQ Read Once Enable for Sampler Client (SQROE): Enables Read Once indications to L3 Cache from SQ. Once enabled, any reads from Sampler client (MT) are sent as Read Once. 0 = (default) Reads from Sampler clients issue Read to L3 Cache. 1 = Reads from Sampler clients issue Read Once to L3 Cache. lbcf_csr_sampler_readonce_en.</td></tr> </table>	Access:	R/W	L3SQ Read Once Enable for Sampler Client (SQROE): Enables Read Once indications to L3 Cache from SQ. Once enabled, any reads from Sampler client (MT) are sent as Read Once. 0 = (default) Reads from Sampler clients issue Read to L3 Cache. 1 = Reads from Sampler clients issue Read Once to L3 Cache. lbcf_csr_sampler_readonce_en.	
Access:	R/W					
L3SQ Read Once Enable for Sampler Client (SQROE): Enables Read Once indications to L3 Cache from SQ. Once enabled, any reads from Sampler client (MT) are sent as Read Once. 0 = (default) Reads from Sampler clients issue Read to L3 Cache. 1 = Reads from Sampler clients issue Read Once to L3 Cache. lbcf_csr_sampler_readonce_en.						
	8:6	Reserved <table border="1"> <tr> <td>Access:</td><td>RO</td></tr> <tr> <td colspan="2">Reserved.</td></tr> </table>	Access:	RO	Reserved.	
Access:	RO					
Reserved.						

L3SQCREG1 - L3 SQC registers 1				
	5:3	<p>L3SQ Outstanding L3 Fills</p> <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>L3SQ Outstanding L3 Fills (SQOUTSL3F): Identifies the number of L3 Fills that can be outstanding before SQ throttles the fill requests to L3 Cache. This is not an exact limit, but instead it is used as a threshold to throttling. Once the fill count is greater than or equal to the threshold, then no fills are issued until the fill responses are received to bring the outstanding count back below the threshold. 000b = (default) No limit. 001b = 1 fill. 010b = 2 fills. 011b = 4 fills. 100b = 8 fills. 101b = 16 fills. 11Xb = Reserved. lbcf_csr_lsqc_outs_fill[2:0].</p>	Access:	R/W
Access:	R/W			
	2:0	<p>L3SQ Outstanding L3 Lookups</p> <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>L3SQ Outstanding L3 Lookups (SQOUTSL3L): Identifies the number of L3 lookups that can be outstanding before SQ throttles the lookup requests to L3 Cache. This is not an exact limit, but instead it is used as a threshold to throttling. once the lookup count is greater than or equal to the threshold, then no lookups are issued until the lookup responses are received to bring the outstanding count back below the threshold. 000b = (default) No limit. 001b = 1 lookup. 010b = 2 lookups. 011b = 4 lookups. 100b = 8 lookups. 101b = 16 lookups. 11Xb = Reserved. lbcf_csr_lsqc_outs_lookup[2:0].</p>	Access:	R/W
Access:	R/W			

L3 SQC registers 2

L3SQCREG2 - L3 SQC registers 2				
DWord	Bit	Description		
0	31:17	Reserved Access: RO Reserved.		
	16	L3SQ Priority Selection Disable Access: R/W <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center; background-color: #e0e0ff;">Description</th> </tr> </thead> <tbody> <tr> <td>L3SQ Priority Selection Disable (SQPRIDIS): Enables the use of priority selection based on client ID decodes. If disabled, all cycles in SQ are treated as same priority. 0 = (default) Priority selection is enabled. 1 = Priority selection is disabled. Should not be set when RO perf mode is enabled (by default this is enabled which is bit[27] of B118-B11Bh). lbcf_csr_priority_cnt_disable.</td> </tr> </tbody> </table>	Description	L3SQ Priority Selection Disable (SQPRIDIS): Enables the use of priority selection based on client ID decodes. If disabled, all cycles in SQ are treated as same priority. 0 = (default) Priority selection is enabled. 1 = Priority selection is disabled. Should not be set when RO perf mode is enabled (by default this is enabled which is bit[27] of B118-B11Bh). lbcf_csr_priority_cnt_disable.
Description				
L3SQ Priority Selection Disable (SQPRIDIS): Enables the use of priority selection based on client ID decodes. If disabled, all cycles in SQ are treated as same priority. 0 = (default) Priority selection is enabled. 1 = Priority selection is disabled. Should not be set when RO perf mode is enabled (by default this is enabled which is bit[27] of B118-B11Bh). lbcf_csr_priority_cnt_disable.				
	15	L3SQ Priority 3 Pool Count Disable Access: R/W <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center; background-color: #e0e0ff;">Description</th> </tr> </thead> <tbody> <tr> <td>L3SQ Priority 3 Pool Count Disable (SQPRI3CNTDIS): When set, priority3 pool becomes unlimited. And priority3 pool count value should not be used in reset of the remaining counters. 0 = (default) Priority 3 pool count is enabled. 1 = Priority 3 pool count is disabled. Should not be set when RO perf mode is enabled (by default this is enabled which is bit[27] of B118-B11Bh). lbcf_csr_priority3_cnt_disable.</td> </tr> </tbody> </table>	Description	L3SQ Priority 3 Pool Count Disable (SQPRI3CNTDIS): When set, priority3 pool becomes unlimited. And priority3 pool count value should not be used in reset of the remaining counters. 0 = (default) Priority 3 pool count is enabled. 1 = Priority 3 pool count is disabled. Should not be set when RO perf mode is enabled (by default this is enabled which is bit[27] of B118-B11Bh). lbcf_csr_priority3_cnt_disable.
Description				
L3SQ Priority 3 Pool Count Disable (SQPRI3CNTDIS): When set, priority3 pool becomes unlimited. And priority3 pool count value should not be used in reset of the remaining counters. 0 = (default) Priority 3 pool count is enabled. 1 = Priority 3 pool count is disabled. Should not be set when RO perf mode is enabled (by default this is enabled which is bit[27] of B118-B11Bh). lbcf_csr_priority3_cnt_disable.				

L3SQCREG2 - L3 SQC registers 2

	14:12	L3SQ Priority 3 Pool Counter						
		<table border="1"> <tr> <td>Default Value:</td><td>100b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>L3SQ Priority 3 Pool Counter (SQPRI3CNT): The count of cycles is selected from priority3 pool before switching to other priority pools. Count is used as the power of 2. 000b = 1 request. 001b = 2 requests. 010b = 4 requests. 011b = 8 requests. ... 111b = 128 requests. <code>lbcf_csr_priority3_cnt[2:0]</code>.</p>	Default Value:	100b	Access:	R/W		
Default Value:	100b							
Access:	R/W							
	11	L3SQ Priority 2 Pool Count Disable						
		<table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table>	Access:	R/W				
Access:	R/W							
		<table border="1"> <thead> <tr> <th>Description</th><th>Project</th></tr> </thead> <tbody> <tr> <td>L3SQ Priority 2 Pool Count Disable (SQPRI2CNTDIS): When set, priority2 pool becomes unlimited. And priority2 pool count value should not be used in reset of the remaining counters. 0 = (default) Priority 2 pool count is enabled. 1 = Priority 2 pool count is disabled. Should not be set when RO perf mode is enabled (by default this is enabled which is bit[27] of B118-B11Bh). <code>lbcf_csr_priority2_cnt_disable</code>.</td><td></td></tr> <tr> <td>As a workaround if this bit is set to 1 then the following bits in register B108-B10B should have identical values 29:28, 27:26, 25:24, 23:22, 21:20, 19:18, 17:16, 15:14, 13:12, 11:10, 9:8, 7:6, 5:4, 3:2, 1:0.</td><td>BDW</td></tr> </tbody> </table>	Description	Project	L3SQ Priority 2 Pool Count Disable (SQPRI2CNTDIS): When set, priority2 pool becomes unlimited. And priority2 pool count value should not be used in reset of the remaining counters. 0 = (default) Priority 2 pool count is enabled. 1 = Priority 2 pool count is disabled. Should not be set when RO perf mode is enabled (by default this is enabled which is bit[27] of B118-B11Bh). <code>lbcf_csr_priority2_cnt_disable</code> .		As a workaround if this bit is set to 1 then the following bits in register B108-B10B should have identical values 29:28, 27:26, 25:24, 23:22, 21:20, 19:18, 17:16, 15:14, 13:12, 11:10, 9:8, 7:6, 5:4, 3:2, 1:0.	BDW
Description	Project							
L3SQ Priority 2 Pool Count Disable (SQPRI2CNTDIS): When set, priority2 pool becomes unlimited. And priority2 pool count value should not be used in reset of the remaining counters. 0 = (default) Priority 2 pool count is enabled. 1 = Priority 2 pool count is disabled. Should not be set when RO perf mode is enabled (by default this is enabled which is bit[27] of B118-B11Bh). <code>lbcf_csr_priority2_cnt_disable</code> .								
As a workaround if this bit is set to 1 then the following bits in register B108-B10B should have identical values 29:28, 27:26, 25:24, 23:22, 21:20, 19:18, 17:16, 15:14, 13:12, 11:10, 9:8, 7:6, 5:4, 3:2, 1:0.	BDW							
	10:8	L3SQ Priority 2 Pool Counter						
		<table border="1"> <tr> <td>Default Value:</td><td>101b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table>	Default Value:	101b	Access:	R/W		
Default Value:	101b							
Access:	R/W							
		<p>L3SQ Priority 2 Pool Counter (SQPRI2CNT): The count of cycles is selected from priority2 pool before switching to other priority pools. Count is used as the power of 2. 000b = 1 request. 001b = 2 requests. 010b = 4 requests. 011b = 8 requests. ... 111b = 128 requests. <code>lbcf_csr_priority2_cnt[2:0]</code>.</p>						

L3SQCREG2 - L3 SQC registers 2										
	7	L3SQ Priority 1 Pool Count Disable <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> <tr> <th>Description</th><th>Project</th></tr> <tr> <td> L3SQ Priority 1 Pool Count Disable (SQPRI1CNTDIS): When set, priority1 pool becomes unlimited. And priority1 pool count value should not be used in reset of the remaining counters. 0 = (default) Priority 1 pool count is enabled. 1 = Priority 1 pool count is disabled. Should not be set when RO perf mode is enabled (by default this is enabled which is bit[27] of B118-B11Bh). <code>lbcf_csr_priority1_cnt_disable.</code> </td><td></td></tr> <tr> <td>As a workaround if this bit is set to 1 then the following bits in register B108-B10B should have identical values 29:28, 27:26, 25:24, 23:22, 21:20, 19:18, 17:16, 15:14, 13:12, 11:10, 9:8, 7:6, 5:4, 3:2, 1:0.</td><td>BDW</td></tr> </table>	Access:	R/W	Description	Project	L3SQ Priority 1 Pool Count Disable (SQPRI1CNTDIS): When set, priority1 pool becomes unlimited. And priority1 pool count value should not be used in reset of the remaining counters. 0 = (default) Priority 1 pool count is enabled. 1 = Priority 1 pool count is disabled. Should not be set when RO perf mode is enabled (by default this is enabled which is bit[27] of B118-B11Bh). <code>lbcf_csr_priority1_cnt_disable.</code>		As a workaround if this bit is set to 1 then the following bits in register B108-B10B should have identical values 29:28, 27:26, 25:24, 23:22, 21:20, 19:18, 17:16, 15:14, 13:12, 11:10, 9:8, 7:6, 5:4, 3:2, 1:0.	BDW
Access:	R/W									
Description	Project									
L3SQ Priority 1 Pool Count Disable (SQPRI1CNTDIS): When set, priority1 pool becomes unlimited. And priority1 pool count value should not be used in reset of the remaining counters. 0 = (default) Priority 1 pool count is enabled. 1 = Priority 1 pool count is disabled. Should not be set when RO perf mode is enabled (by default this is enabled which is bit[27] of B118-B11Bh). <code>lbcf_csr_priority1_cnt_disable.</code>										
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	6:4	L3SQ Priority 1 Pool Counter <table border="1"> <tr> <td>Default Value:</td><td>110b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> <tr> <td> L3SQ Priority 1 Pool Counter (SQPRI1CNT): The count of cycles is selected from priority1 pool before switching to other priority pools. Count is used as the power of 2. 000b = 1 request. 001b = 2 requests. 010b = 4 requests. 011b = 8 requests. ... 111b = 128 requests. <code>lbcf_csr_priority1_cnt[2:0].</code> </td><td></td></tr> </table>	Default Value:	110b	Access:	R/W	L3SQ Priority 1 Pool Counter (SQPRI1CNT): The count of cycles is selected from priority1 pool before switching to other priority pools. Count is used as the power of 2. 000b = 1 request. 001b = 2 requests. 010b = 4 requests. 011b = 8 requests. ... 111b = 128 requests. <code>lbcf_csr_priority1_cnt[2:0].</code>			
Default Value:	110b									
Access:	R/W									
L3SQ Priority 1 Pool Counter (SQPRI1CNT): The count of cycles is selected from priority1 pool before switching to other priority pools. Count is used as the power of 2. 000b = 1 request. 001b = 2 requests. 010b = 4 requests. 011b = 8 requests. ... 111b = 128 requests. <code>lbcf_csr_priority1_cnt[2:0].</code>										
	3	L3SQ Priority 0 Pool Count Disable <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> <tr> <th>Description</th><th>Project</th></tr> <tr> <td> L3SQ Priority 0 Pool Count Disable (SQPRI0CNTDIS): When set, priority0 pool becomes unlimited. And priority0 pool count value should not be used in reset of the remaining counters. 0 = (default) Priority 0 pool count is enabled. 1 = Priority 0 pool count is disabled. Should not be set when RO perf mode is enabled (by default this is enabled which is bit[27] of B118-B11Bh). <code>lbcf_csr_priority0_cnt_disable.</code> </td><td></td></tr> <tr> <td>As a workaround if this bit is set to 1 then the following bits in register B108-B10B should have identical values 29:28, 27:26, 25:24, 23:22, 21:20, 19:18, 17:16, 15:14, 13:12, 11:10, 9:8, 7:6, 5:4, 3:2, 1:0.</td><td></td></tr> </table>	Access:	R/W	Description	Project	L3SQ Priority 0 Pool Count Disable (SQPRI0CNTDIS): When set, priority0 pool becomes unlimited. And priority0 pool count value should not be used in reset of the remaining counters. 0 = (default) Priority 0 pool count is enabled. 1 = Priority 0 pool count is disabled. Should not be set when RO perf mode is enabled (by default this is enabled which is bit[27] of B118-B11Bh). <code>lbcf_csr_priority0_cnt_disable.</code>		As a workaround if this bit is set to 1 then the following bits in register B108-B10B should have identical values 29:28, 27:26, 25:24, 23:22, 21:20, 19:18, 17:16, 15:14, 13:12, 11:10, 9:8, 7:6, 5:4, 3:2, 1:0.	
Access:	R/W									
Description	Project									
L3SQ Priority 0 Pool Count Disable (SQPRI0CNTDIS): When set, priority0 pool becomes unlimited. And priority0 pool count value should not be used in reset of the remaining counters. 0 = (default) Priority 0 pool count is enabled. 1 = Priority 0 pool count is disabled. Should not be set when RO perf mode is enabled (by default this is enabled which is bit[27] of B118-B11Bh). <code>lbcf_csr_priority0_cnt_disable.</code>										
As a workaround if this bit is set to 1 then the following bits in register B108-B10B should have identical values 29:28, 27:26, 25:24, 23:22, 21:20, 19:18, 17:16, 15:14, 13:12, 11:10, 9:8, 7:6, 5:4, 3:2, 1:0.										

L3SQCREG2 - L3 SQC registers 2

	2:0	L3SQ Priority 0 Pool Counter
		Default Value:
		111b
		Access:
L3SQ Priority 0 Pool Counter (SQPRI0CNT): The count of cycles is selected from priority0 pool before switching to other priority pools. Count is used as the power of 2. 000b = 1 request. 001b = 2 requests. 010b = 4 requests. 011b = 8 requests. ... 111b = (default) 128 requests. <code>lbcf_csr_priority0_cnt[2:0]</code> .		

L3 SQC registers 3

L3SQCREG3 - L3 SQC registers 3				
DWord	Bit	Description		
0	31:30	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Reserved.</p>	Access:	RO
Access:	RO			
	29:28	SOLunit Priority Value <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>SOLunit Priority Value (SQSOLPRIVAL): Identifies the priority value for all cycles that are initiated by SOLunit. Priority is used in the L3 Super Queue (L3SQ). 00b = Priority 0 (default). 01b = Priority 1. 10b = Priority 2. 11b = Priority 3. lbcf_csr_sol_priority[1:0].</p>	Access:	R/W
Access:	R/W			
	27:26	GSunit Priority Value <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>GSunit Priority Value (SQGSPRIVAL): Identifies the priority value for all cycles that are initiated by GSunit. Priority is used in the L3 Super Queue (L3SQ). 00b = Priority 0 (default). 01b = Priority 1. 10b = Priority 2. 11b = Priority 3. lbcf_csr_gs_priority[1:0].</p>	Access:	R/W
Access:	R/W			
	25:24	TEunit Priority Value <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>TEunit Priority Value (SQTEPRIVAL): Identifies the priority value for all cycles that are initiated by TEunit. Priority is used in the L3 Super Queue (L3SQ). 00b = Priority 0 (default). 01b = Priority 1. 10b = Priority 2. 11b = Priority 3. lbcf_csr_te_priority[1:0].</p>	Access:	R/W
Access:	R/W			

L3SQCREG3 - L3 SQC registers 3				
	23:22	CLunit Priority Value		
		<table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>CLunit Priority Value (SQCLPRIVAL): Identifies the priority value for all cycles that are initiated by CLunit. Priority is used in the L3 Super Queue (L3SQ). 00b = Priority 0 (default). 01b = Priority 1. 10b = Priority 2. 11b = Priority 3. lbcf_csr_cl_priority[1:0].</p>	Access:	R/W
Access:	R/W			
	21:20	TSunit Priority Value		
		<table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>TSunit Priority Value (SQTSPRIVAL): Identifies the priority value for all cycles that are initiated by TSunit. Priority is used in the L3 Super Queue (L3SQ). 00b = Priority 0 (default). 01b = Priority 1. 10b = Priority 2. 11b = Priority 3. lbcf_csr_ts_priority[1:0].</p>	Access:	R/W
Access:	R/W			
	19:18	SFunit Priority Value		
		<table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>SFunit Priority Value (SQSFPRIVAL): Identifies the priority value for all cycles that are initiated by SFunit. Priority is used in the L3 Super Queue (L3SQ). 00b = Priority 0 (default). 01b = Priority 1. 10b = Priority 2. 11b = Priority 3. lbcf_csr_sf_priority[1:0].</p>	Access:	R/W
Access:	R/W			
	17:16	SVSM Priority Value		
		<table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>SVSM Priority Value (SQSVSMPRIVAL): Identifies the priority value for all cycles that are initiated by SVSM. Priority is used in the L3 Super Queue (L3SQ). 00b = Priority 0 (default). 01b = Priority 1. 10b = Priority 2. 11b = Priority 3. lbcf_csr_svsm_priority[1:0].</p>	Access:	R/W
Access:	R/W			

L3SQCREG3 - L3 SQC registers 3

	15:14	SARB Priority Value	
		Access:	R/W
<p>SARB Priority Value (SQSARBPRIVAL): Identifies the priority value for all cycles that are initiated by State Arbiter (SARB). Priority is used in the L3 Super Queue (L3SQ).</p> <p>00b = Priority 0 (default). 01b = Priority 1. 10b = Priority 2. 11b = Priority 3. lbcf_csr_sarb_priority[1:0].</p>			
	13:12	SBE Priority Value	
		Default Value:	01b
		Access:	R/W
<p>SBE Priority Value (SQSBEPRALVAL): Identifies the priority value for all cycles that are initiated by SBE. Priority is used in the L3 Super Queue (L3SQ).</p> <p>00b = Priority 0. 01b = Priority 1 (default). 10b = Priority 2. 11b = Priority 3. lbcf_csr_sbe_priority[1:0].</p>			
	11:10	IC\$ Priority Value	
		Default Value:	10b
		Access:	R/W
<p>IC\$ Priority Value (SQICPRIVAL): Identifies the priority value for all cycles that are initiated by Instruction Cache (IC\$). Priority is used in the L3 Super Queue (L3SQ).</p> <p>00b = Priority 0. 01b = Priority 1. 10b = Priority 2 (default). 11b = Priority 3. lbcf_csr_ic_priority[1:0].</p>			
	9:8	TDL Priority Value	
		Default Value:	10b
		Access:	R/W
<p>TDL Priority Value (SQTDLPRIVAL): Identifies the priority value for all cycles that are initiated by TDL. Priority is used in the L3 Super Queue (L3SQ).</p> <p>00b = Priority 0. 01b = Priority 1. 10b = Priority 2 (default). 11b = Priority 3. lbcf_csr_tdl_priority[1:0].</p>			

L3SQCREG3 - L3 SQC registers 3			
	7:6	DCunit Priority Value	
		Default Value:	10b
		Access:	R/W
		DCunit Priority Value (SQDCPRIVAL): Identifies the priority value for all cycles that are initiated by DC. Priority is used in the L3 Super Queue (L3SQ). 00b = Priority 0. 01b = Priority 1. 10b = Priority 2 (default). 11b = Priority 3. lbcf_csr_dc_priority[1:0].	
	5:4	DAPR Priority Value	
		Default Value:	11b
		Access:	R/W
		DAPR Priority Value (SQDAPRPRIVAL): Identifies the priority value for all cycles that are initiated by DAPR. Priority is used in the L3 Super Queue (L3SQ). 00b = Priority 0. 01b = Priority 1. 10b = Priority 2. 11b = Priority 3 (default). lbcf_csr_dapr_priority[1:0].	
	3:2	MTunit Priority Value	
		Default Value:	11b
		Access:	R/W
		MTunit Priority Value (SQMTPRIVAL): Identifies the priority value for all cycles that are initiated by Sampler (MT). Priority is used in the L3 Super Queue (L3SQ). 00b = Priority 0. 01b = Priority 1. 10b = Priority 2. 11b = Priority 3 (default). lbcf_csr_mt_priority[1:0].	

L3SQCREG3 - L3 SQC registers 3

	1:0	LSQCunit Priority Value
		Default Value: 11b Access: R/W
		<p>LSQCunit Priority Value (SQPRIVAL): Identifies the priority value for all cycles that are initiated by Super Queue (L3 Evictions). Priority is used in the L3 Super Queue (L3SQ).</p> <p>00b = Priority 0. 01b = Priority 1. 10b = Priority 2. 11b = Priority 3 (default). lbcf_csr_lsqc_priority[1:0].</p>

LBCF config save msg

LBCFCSR - LBCF config save msg				
DWord	Bit	Description		
0	31:10	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
Access:	RO			
	9:0	<p>Context save bit</p> <table border="1"> <tr> <td>Access:</td> <td>R/W Hardware Clear</td> </tr> </table> <p>Bit[9]: Power Context Save Request. 0: Power context save is not being requested (default). 1: Power context save is being requested. Unit needs to self-clear this bit upon sampling.</p> <p>Bits[8:0]: QWord Credits for Power Context Save Request. Minimum Credits = 1: Unit may send 1 QWord pair (enough for first LRI at least). Maximum Credits = 511: Unit may send 511 QWord pairs. A QWord pair is defined as a 32-bit register address and the corresponding 32-bits of register data. Note that the LRI header and END commands are 64-bits each (32-bit command followed by 32-bit NOOP) and consumes one QWord credit. Only valid with PWRCTX_SAVE_REQ (Bit9).</p>	Access:	R/W Hardware Clear
Access:	R/W Hardware Clear			

LBCF DPF Error log register 0

LBCFPM00 - LBCF DPF Error log register 0				
Register Space:	MMIO: 0/2/0			
Project:	BDW			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0B130h			
Slice0 Bank 0 subbank0 Error log register				
DWord	Bit	Description		
0	31:21	<p>Row Number for Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. lbcf_sb0_error_addr1[9:0].</p>	Access:	R/W
Access:	R/W			
20:17	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
16	<p>Valid Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The Address located in field 31:21 is valid. lbcf_sb0_valid_error1.</p>	Access:	R/W	
Access:	R/W			
15:5	<p>Row Number for Error0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. lbcf_sb0_error_addr0[9:0].</p>	Access:	R/W	
Access:	R/W			
4:1	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	<p>Valid Error 0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The address located in field 15:5 is valid. lbcf_sb0_valid_error0.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 1

LBCFPM01 - LBCF DPF Error log register 1				
Slice0 Bank 0 subbank1 Error log register				
DWord	Bit	Description		
0	31:21	<p>Row Number for Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. lbcf_sb1_error_addr1[9:0].</p>	Access:	R/W
Access:	R/W			
20:17	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
16	<p>Valid Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The Address located in field 31:21 is valid. lbcf_sb1_error_addr0[9:0].</p>	Access:	R/W	
Access:	R/W			
15:5	<p>Row Number for Error0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. lbcf_sb1_error_addr0[9:0].</p>	Access:	R/W	
Access:	R/W			
4:1	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	<p>Valid Error 0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The address located in field 15:5 is valid. lbcf_sb1_valid_error0.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 2

LBCFPM02 - LBCF DPF Error log register 2						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	0B138h					
Slice0 Bank0 Subbank 2 Error log register						
DWord	Bit	Description				
0	31:21	Row Number for Error 1 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td colspan="2">Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. lbcf_sb2_error_addr1[9:0].</td></tr> </table>	Access:	R/W	Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. lbcf_sb2_error_addr1[9:0].	
Access:	R/W					
Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. lbcf_sb2_error_addr1[9:0].						
20:17	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO			
Access:	RO					
16	Valid Error 1 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td colspan="2">Valid Error: The Address located in field 31:21 is valid. lbcf_sb2_valid_error1.</td></tr> </table>	Access:	R/W	Valid Error: The Address located in field 31:21 is valid. lbcf_sb2_valid_error1.		
Access:	R/W					
Valid Error: The Address located in field 31:21 is valid. lbcf_sb2_valid_error1.						
15:5	Row Number for Error0 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td colspan="2">Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. lbcf_sb2_error_addr0[9:0].</td></tr> </table>	Access:	R/W	Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. lbcf_sb2_error_addr0[9:0].		
Access:	R/W					
Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. lbcf_sb2_error_addr0[9:0].						
4:1	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO			
Access:	RO					
0	Valid Error 0 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td colspan="2">Valid Error: The address located in field 15:5 is valid. lbcf_sb2_valid_error0.</td></tr> </table>	Access:	R/W	Valid Error: The address located in field 15:5 is valid. lbcf_sb2_valid_error0.		
Access:	R/W					
Valid Error: The address located in field 15:5 is valid. lbcf_sb2_valid_error0.						

LBCF DPF Error log register 3

LBCFPM03 - LBCF DPF Error log register 3				
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x00000000 Size (in bits): 32				
Address: 0B13Ch				
Slice0 Bank0 subbank3 Error log register				
DWord	Bit	Description		
0	31:21	Row Number for Error 1 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. lbcf_sb3_error_addr1[9:0].</p>	Access:	R/W
Access:	R/W			
20:17	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
16	Valid Error 1 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The Address located in field 31:21 is valid. lbcf_sb3_valid_error1.</p>	Access:	R/W	
Access:	R/W			
15:5	Row Number for Error0 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. lbcf_sb3_error_addr0[9:0].</p>	Access:	R/W	
Access:	R/W			
4:1	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	Valid Error 0 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The address located in field 15:5 is valid. lbcf_sb3_valid_error0.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 4

LBCFERRLOG01 - LBCF DPF Error log register 4				
DWord	Bit	Description		
0	31:21	Row Number for Error 1 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 0 Bank 1 Error log register 00.</p>	Access:	R/W
Access:	R/W			
20:17	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
16	Valid Error 1 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid. Slice 0 Bank 1 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
15:5	Row Number for Error0 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 0 Bank 1 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	Valid Error 0 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is valid. Slice 0 Bank 1 Error log register 00.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 5

LBCFERRLOG02 - LBCF DPF Error log register 5				
Register Space: MMIO: 0/2/0				
Project: BDW				
Default Value: 0x00000000				
Size (in bits): 32				
Address: 0B144h				
Slice 0 Bank 1 Subbank1 Error log register				
DWord	Bit	Description		
0	31:21	<p>Row Number for Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 0 Bank 1 Error log register 00.</p>	Access:	R/W
Access:	R/W			
20:17	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
16	<p>Valid Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The Address located in field 31:21 is valid. Slice 0 Bank 1 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
15:5	<p>Row Number for Error0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 0 Bank 1 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	<p>Valid Error 0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The address located in field 15:5 is valid</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 6

LBCFERRLOG03 - LBCF DPF Error log register 6				
DWord	Bit	Description		
0	31:21	Row Number for Error 1 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 0 Bank 1 Error log register 00.</p>	Access:	R/W
Access:	R/W			
20:17	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
16	Valid Error 1 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 0 Bank 1 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
15:5	Row Number for Error0 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 0 Bank 1 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	Valid Error 0 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The address located in field 15:5 is valid. Slice 0 Bank 1 Error log register 00.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 7

LBCFERRLOG04 - LBCF DPF Error log register 7				
DWord	Bit	Description		
0	31:21	<p>Row Number for Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 0 Bank 1 Error log register 00.</p>	Access:	R/W
Access:	R/W			
20:17	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
16	<p>Valid Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The Address located in field 31:21 is valid. Slice 0 Bank 1 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
15:5	<p>Row Number for Error0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 0 Bank 1 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	<p>Valid Error 0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The address located in field 15:5 is valid. Slice 0 Bank 1 Error log register 00.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 8

LBCFERRLOG05 - LBCF DPF Error log register 8				
DWord	Bit	Description		
0	31:21	<p>Row Number for Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank.</p> <p>The number of rows varies between 4K vs. 8K/16K subbanks which requires 10 bits vs 11 bits respectively.</p> <p>This field contains the row# with the error.</p> <p>Slice 0 Bank 2 Error log register 00.</p>	Access:	R/W
Access:	R/W			
	20:17	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
Access:	RO			
	16	<p>Valid Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 16:5 is valid and</p> <p>Slice 0 Bank 2 Error log register 00.</p>	Access:	R/W
Access:	R/W			
	16:5	<p>Row Number for Error0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 16:5 is valid and</p> <p>Slice 0 Bank 2 Error log register 00.</p>	Access:	R/W
Access:	R/W			
	4:1	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
Access:	RO			
	0	<p>Valid Error 0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 16:5 is valid.</p> <p>Slice 0 Bank 2 Error log register 00.</p>	Access:	R/W
Access:	R/W			

LBCF DPF Error log register 9

LBCFERRLOG06 - LBCF DPF Error log register 9				
Slice 0 Bank 2 subbank1 Error log register				
DWord	Bit	Description		
0	31:21	<p>Row Number for Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank.</p> <p>The number of rows varies between 4K vs. 8K/16K subbanks which requires 10 bits vs 11 bits respectively.</p> <p>This field contains the row# with the error.</p> <p>Slice 0 Bank 2 Error log register 00.</p>	Access:	R/W
Access:	R/W			
	20:17	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
Access:	RO			
	16	<p>Valid Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid.</p> <p>Slice 0 Bank 2 Error log register 00.</p>	Access:	R/W
Access:	R/W			
	15:5	<p>Row Number for Error0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank.</p> <p>Slice 0 Bank 2 Error log register 00.</p>	Access:	R/W
Access:	R/W			
	4:1	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
Access:	RO			
	0	<p>Valid Error 0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is valid.</p>	Access:	R/W
Access:	R/W			

LBCF DPF Error log register 10

LBCFERRLOG07 - LBCF DPF Error log register 10				
DWord	Bit	Description		
0	31:21	<p>Row Number for Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank.</p> <p>The number of rows varies between 4K vs. 8K/16K subbanks which requires 10 bits vs. 11 bits respectively.</p> <p>This field contains the row# with the error.</p> <p>Slice 0 Bank 2 Error log register 00.</p>	Access:	R/W
Access:	R/W			
	20:17	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
Access:	RO			
	16	<p>Valid Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid.</p> <p>Slice 0 Bank 2 Error log register 00.</p>	Access:	R/W
Access:	R/W			
	15:5	<p>Row Number for Error0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank.</p> <p>Slice 0 Bank 2 Error log register 00.</p>	Access:	R/W
Access:	R/W			
	4:1	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
Access:	RO			
	0	<p>Valid Error 0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is valid.</p> <p>Slice 0 Bank 2 Error log register 00.</p>	Access:	R/W
Access:	R/W			

LBCF DPF Error log register 11

LBCFERRLOG08 - LBCF DPF Error log register 11				
DWord	Bit	Description		
0	31:21	<p>Row Number for Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank.</p> <p>The number of rows varies between 4K vs. 8K/16K subbanks which requires 10 bits vs. 11 bits respectively.</p> <p>This field contains the row# with the error.</p> <p>Slice 0 Bank 2 Error log register 00.</p>	Access:	R/W
Access:	R/W			
	20:17	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
Access:	RO			
	16	<p>Valid Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid.</p> <p>Slice 0 Bank 2 Error log register 00.</p>	Access:	R/W
Access:	R/W			
	15:5	<p>Row Number for Error0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank.</p> <p>Slice 0 Bank 2 Error log register 00.</p>	Access:	R/W
Access:	R/W			
	4:1	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
Access:	RO			
	0	<p>Valid Error 0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is valid.</p> <p>Slice 0 Bank 2 Error log register 00.</p>	Access:	R/W
Access:	R/W			

LBCF DPF Error log register 12

LBCFERRLOG09 - LBCF DPF Error log register 12				
DWord	Bit	Description		
0	31:21	Row Number for Error 1 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 0 Bank 3 Error log register 00.</p>	Access:	R/W
Access:	R/W			
20:17	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
16	Valid Error 1 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid. Slice 0 Bank 3 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
15:5	Row Number for Error0 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 0 Bank 3 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	Valid Error 0 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is valid. Slice 0 Bank 3 Error log register 00.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 13

LBCFERRLOG10 - LBCF DPF Error log register 13				
DWord	Bit	Description		
0	31:21	<p>Row Number for Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 0 Bank 3 Error log register 00.</p>	Access:	R/W
Access:	R/W			
20:17	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
16	<p>Valid Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid. Slice 0 Bank 3 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
15:5	<p>Row Number for Error0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 0 Bank 3 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	<p>Valid Error 0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is valid.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 14

LBCFERRLOG11 - LBCF DPF Error log register 14				
DWord	Bit	Description		
0	31:21	Row Number for Error 1 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 0 Bank 3 Error log register 00.</p>	Access:	R/W
Access:	R/W			
20:17	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
16	Valid Error 1 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid. Slice 0 Bank 3 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
15:5	Row Number for Error0 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 0 Bank 3 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	Valid Error 0 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is valid. Slice 0 Bank 3 Error log register 00.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 15

LBCFERRLOG12 - LBCF DPF Error log register 15				
DWord	Bit	Description		
0	31:21	<p>Row Number for Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 0 Bank 3 Error log register 00.</p>	Access:	R/W
Access:	R/W			
20:17	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
16	<p>Valid Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid. Slice 0 Bank 3 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
15:5	<p>Row Number for Error0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 0 Bank 3 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	<p>Valid Error 0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is valid. Slice 0 Bank 3 Error log register 00.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 16

LBCFERRLOG13 - LBCF DPF Error log register 16				
DWord	Bit	Description		
0	31:21	Row Number for Error 1 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 bank 1 Error log register 00.</p>	Access:	R/W
Access:	R/W			
20:17	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
16	Valid Error 1 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid. Slice 1 bank 1 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
15:5	Row Number for Error0 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 bank 1 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	Valid Error 0 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is valid. Slice 1 bank 1 Error log register 00.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 17

LBCFERRLOG14 - LBCF DPF Error log register 17				
DWord	Bit	Description		
0	31:21	<p>Row Number for Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 bank 1 Error log register 00.</p>	Access:	R/W
Access:	R/W			
20:17	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
16	<p>Valid Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid. Slice 1 bank 1 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
15:5	<p>Row Number for Error0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 bank 1 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	<p>Valid Error 0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is valid.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 18

LBCFERRLOG15 - LBCF DPF Error log register 18				
DWord	Bit	Description		
0	31:21	Row Number for Error 1 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 bank 1 Error log register 00.</p>	Access:	R/W
Access:	R/W			
20:17	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
16	Valid Error 1 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid. Slice 1 bank 1 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
15:5	Row Number for Error0 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 bank 1 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	Valid Error 0 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is valid. Slice 1 bank 1 Error log register 00.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 19

LBCFERRLOG16 - LBCF DPF Error log register 19				
DWord	Bit	Description		
0	31:21	<p>Row Number for Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 bank 1 Error log register 00.</p>	Access:	R/W
Access:	R/W			
20:17	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
16	<p>Valid Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid. Slice 1 bank 1 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
15:5	<p>Row Number for Error0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 bank 1 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	<p>Valid Error 0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is valid. Slice 1 bank 1 Error log register 00.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 20

LBCFERRLOG17 - LBCF DPF Error log register 20				
DWord	Bit	Description		
0	31:21	Row Number for Error 1 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 bank 0 Error log register 00.</p>	Access:	R/W
Access:	R/W			
20:17	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
16	Valid Error 1 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid. Slice 1 bank 0 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
15:5	Row Number for Error0 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 bank 0 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	Valid Error 0 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is valid. Slice 1 bank 0 Error log register 00.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 21

LBCFERRLOG18 - LBCF DPF Error log register 21				
DWord	Bit	Description		
0	31:21	<p>Row Number for Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 bank 0 Error log register 00.</p>	Access:	R/W
Access:	R/W			
20:17	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
16	<p>Valid Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid. Slice 1 bank 0 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
15:5	<p>Row Number for Error0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 bank 0 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	<p>Valid Error 0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is valid.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 22

LBCFERRLOG19 - LBCF DPF Error log register 22				
DWord	Bit	Description		
0	31:21	Row Number for Error 1 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 bank 0 Error log register 00.</p>	Access:	R/W
Access:	R/W			
20:17	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
16	Valid Error 1 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid. Slice 1 bank 0 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
15:5	Row Number for Error0 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 bank 0 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	Valid Error 0 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is valid. Slice 1 bank 0 Error log register 00.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 23

LBCFERRLOG20 - LBCF DPF Error log register 23				
DWord	Bit	Description		
0	31:21	<p>Row Number for Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 bank 0 Error log register 00.</p>	Access:	R/W
Access:	R/W			
20:17	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
16	<p>Valid Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid. Slice 1 bank 0 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
15:5	<p>Row Number for Error0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 bank 0 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	<p>Valid Error 0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is valid. Slice 1 bank 0 Error log register 00.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 24

LBCFERRLOG21 - LBCF DPF Error log register 24				
DWord	Bit	Description		
0	31:21	Row Number for Error 1 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 bank 2 Error log register 00.</p>	Access:	R/W
Access:	R/W			
20:17	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
16	Valid Error 1 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid. Slice 1 bank 2 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
15:5	Row Number for Error0 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 bank 2 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	Valid Error 0 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is valid. Slice 1 bank 2 Error log register 00.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 25

LBCFERRLOG22 - LBCF DPF Error log register 25				
DWord	Bit	Description		
0	31:21	<p>Row Number for Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 bank 2 Error log register 00.</p>	Access:	R/W
Access:	R/W			
20:17	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
16	<p>Valid Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid. Slice 1 bank 2 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
15:5	<p>Row Number for Error0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 bank 2 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	<p>Valid Error 0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is valid.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 26

LBCFERRLOG23 - LBCF DPF Error log register 26				
DWord	Bit	Description		
0	31:21	Row Number for Error 1 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 bank 2 Error log register 00.</p>	Access:	R/W
Access:	R/W			
20:17	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
16	Valid Error 1 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid. Slice 1 bank 2 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
15:5	Row Number for Error0 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 bank 2 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	Valid Error 0 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is valid. Slice 1 bank 2 Error log register 00.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 27

LBCFERRLOG24 - LBCF DPF Error log register 27				
DWord	Bit	Description		
0	31:21	<p>Row Number for Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 bank 2 Error log register 00.</p>	Access:	R/W
Access:	R/W			
20:17	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
16	<p>Valid Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid. Slice 1 bank 2 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
15:5	<p>Row Number for Error0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 bank 2 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	<p>Valid Error 0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is valid. Slice 1 bank 2 Error log register 00.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 28

LBCFERRLOG25 - LBCF DPF Error log register 28				
DWord	Bit	Description		
0	31:21	<p>Row Number for Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 Bank 3 Error log register 00.</p>	Access:	R/W
Access:	R/W			
20:17	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
16	<p>Valid Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid. Slice 1 Bank 3 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
15:5	<p>Row Number for Error0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 Bank 3 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	<p>Valid Error 0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is valid. Slice 1 Bank 3 Error log register 00.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 29

LBCFERRLOG26 - LBCF DPF Error log register 29				
DWord	Bit	Description		
0	31:21	<p>Row Number for Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 Bank 3 Error log register 00.</p>	Access:	R/W
Access:	R/W			
20:17	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
16	<p>Valid Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid. Slice 1 Bank 3 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
15:5	<p>Row Number for Error0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 Bank 3 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	<p>Valid Error 0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is valid.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 30

LBCFERRLOG27 - LBCF DPF Error log register 30				
DWord	Bit	Description		
0	31:21	Row Number for Error 1 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 Bank 3 Error log register 00.</p>	Access:	R/W
Access:	R/W			
20:17	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
16	Valid Error 1 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid. Slice 1 Bank 3 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
15:5	Row Number for Error0 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 Bank 3 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	Valid Error 0 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is valid. Slice 1 Bank 3 Error log register 00.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 31

LBCFERRLOG28 - LBCF DPF Error log register 31				
DWord	Bit	Description		
0	31:21	<p>Row Number for Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 Bank 3 Error log register 00.</p>	Access:	R/W
Access:	R/W			
20:17	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
16	<p>Valid Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid. Slice 1 Bank 3 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
15:5	<p>Row Number for Error0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 1 Bank 3 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	<p>Valid Error 0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is valid. Slice 1 Bank 3 Error log register 00.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 32

LBCFERRLOG29 - LBCF DPF Error log register 32				
DWord	Bit	Description		
0	31:21	Row Number for Error 1 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 0 Error log register 00.</p>	Access:	R/W
Access:	R/W			
20:17	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
16	Valid Error 1 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid. Slice 2 Bank 0 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
15:5	Row Number for Error0 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 0 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	Valid Error 0 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is valid. Slice 2 Bank 0 Error log register 00.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 33

LBCFERRLOG30 - LBCF DPF Error log register 33				
DWord	Bit	Description		
0	31:21	<p>Row Number for Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 0 Error log register 00.</p>	Access:	R/W
Access:	R/W			
20:17	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
16	<p>Valid Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid. Slice 2 Bank 0 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
15:5	<p>Row Number for Error0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 0 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	<p>Valid Error 0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is valid.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 34

LBCFERRLOG31 - LBCF DPF Error log register 34				
DWord	Bit	Description		
0	31:21	Row Number for Error 1 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 0 Error log register 00.</p>	Access:	R/W
Access:	R/W			
20:17	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
16	Valid Error 1 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid. Slice 2 Bank 0 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
15:5	Row Number for Error0 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 0 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	Valid Error 0 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is valid. Slice 2 Bank 0 Error log register 00.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 35

LBCFERRLOG32 - LBCF DPF Error log register 35				
DWord	Bit	Description		
0	31:21	<p>Row Number for Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 0 Error log register 00.</p>	Access:	R/W
Access:	R/W			
20:17	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
16	<p>Valid Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid. Slice 2 Bank 0 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
15:5	<p>Row Number for Error0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 0 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	<p>Valid Error 0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is valid. Slice 2 Bank 0 Error log register 00.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 36

LBCFERRLOG33 - LBCF DPF Error log register 36				
DWord	Bit	Description		
0	31:21	Row Number for Error 1 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 1 Error log register 00.</p>	Access:	R/W
Access:	R/W			
20:17	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
16	Valid Error 1 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid. Slice 2 Bank 1 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
15:5	Row Number for Error0 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 1 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	Valid Error 0 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is valid. Slice 2 Bank 1 Error log register 00.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 37

LBCFERRLOG34 - LBCF DPF Error log register 37				
DWord	Bit	Description		
0	31:21	<p>Row Number for Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 1 Error log register 00.</p>	Access:	R/W
Access:	R/W			
20:17	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
16	<p>Valid Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid. Slice 2 Bank 1 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
15:5	<p>Row Number for Error0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 1 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	<p>Valid Error 0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is valid.</p>	Access:	R/W	
Access:	R/W			

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LBCFERRLOG35 - LBCF DPF Error log register 38				
DWord	Bit	Description		
0	31:21	Row Number for Error 1 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 1 Error log register 00.</p>	Access:	R/W
Access:	R/W			
20:17	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
16	Valid Error 1 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid. Slice 2 Bank 1 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
15:5	Row Number for Error0 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 1 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	Valid Error 0 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is valid. Slice 2 Bank 1 Error log register 00.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 39

LBCFERRLOG36 - LBCF DPF Error log register 39				
DWord	Bit	Description		
0	31:21	<p>Row Number for Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 1 Error log register 00.</p>	Access:	R/W
Access:	R/W			
20:17	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
16	<p>Valid Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid. Slice 2 Bank 1 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
15:5	<p>Row Number for Error0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 1 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	<p>Valid Error 0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is valid. Slice 2 Bank 1 Error log register 00.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 40

LBCFERRLOG37 - LBCF DPF Error log register 40				
DWord	Bit	Description		
0	31:21	<p>Row Number for Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 2 Error log register 00.</p>	Access:	R/W
Access:	R/W			
20:17	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
16	<p>Valid Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid. Slice 2 Bank 2 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
15:5	<p>Row Number for Error0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 2 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	<p>Valid Error 0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is valid. Slice 2 Bank 2 Error log register 00.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 41

LBCFERRLOG38 - LBCF DPF Error log register 41				
DWord	Bit	Description		
0	31:21	<p>Row Number for Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 2 Error log register 00.</p>	Access:	R/W
Access:	R/W			
20:17	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
16	<p>Valid Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid. Slice 2 Bank 2 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
15:5	<p>Row Number for Error0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 2 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	<p>Valid Error 0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is valid.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 42

LBCFERRLOG39 - LBCF DPF Error log register 42				
DWord	Bit	Description		
0	31:21	Row Number for Error 1 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 2 Error log register 00.</p>	Access:	R/W
Access:	R/W			
	20:17	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
Access:	RO			
	16	Valid Error 1 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid. Slice 2 Bank 2 Error log register 00.</p>	Access:	R/W
Access:	R/W			
	15:5	Row Number for Error0 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 2 Error log register 00.</p>	Access:	R/W
Access:	R/W			
	4:1	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
Access:	RO			
	0	Valid Error 0 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is valid. Slice 2 Bank 2 Error log register 00.</p>	Access:	R/W
Access:	R/W			

LBCF DPF Error log register 43

LBCFERRLOG40 - LBCF DPF Error log register 43				
DWord	Bit	Description		
0	31:21	<p>Row Number for Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 2 Error log register 00.</p>	Access:	R/W
Access:	R/W			
20:17	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
16	<p>Valid Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid. Slice 2 Bank 2 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
15:5	<p>Row Number for Error0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 2 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	<p>Valid Error 0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is valid. Slice 2 Bank 2 Error log register 00.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 44

LBCFERRLOG41 - LBCF DPF Error log register 44				
DWord	Bit	Description		
0	31:21	Row Number for Error 1 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 3 Error log register 00.</p>	Access:	R/W
Access:	R/W			
20:17	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
16	Valid Error 1 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid. Slice 2 Bank 3 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
15:5	Row Number for Error0 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. and Slice 2 Bank 3 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	Valid Error 0 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is validcorresponding logical 16KB group should bypass this row. Slice 2 Bank 3 Error log register 00.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 45

LBCFERRLOG42 - LBCF DPF Error log register 45				
DWord	Bit	Description		
0	31:21	<p>Row Number for Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 3 Error log register 00.</p>	Access:	R/W
Access:	R/W			
20:17	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
16	<p>Valid Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid. Slice 2 Bank 3 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
15:5	<p>Row Number for Error0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 3 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	<p>Valid Error 0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is valid.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 46

LBCFERRLOG43 - LBCF DPF Error log register 46				
DWord	Bit	Description		
0	31:21	Row Number for Error 1 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 3 Error log register 00.</p>	Access:	R/W
Access:	R/W			
20:17	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
16	Valid Error 1 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid. Slice 2 Bank 3 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
15:5	Row Number for Error0 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 3 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	Valid Error 0 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is valid. Slice 2 Bank 3 Error log register 00.</p>	Access:	R/W	
Access:	R/W			

LBCF DPF Error log register 47

LBCFERRLOG44 - LBCF DPF Error log register 47				
DWord	Bit	Description		
0	31:21	<p>Row Number for Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error1: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 3 Error log register 00.</p>	Access:	R/W
Access:	R/W			
20:17	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
16	<p>Valid Error 1</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 31:21 is valid. Slice 2 Bank 3 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
15:5	<p>Row Number for Error0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Row Number for Error0: The physical row Addr where the parity error has been detected in SLM Bank. Slice 2 Bank 3 Error log register 00.</p>	Access:	R/W	
Access:	R/W			
4:1	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			
0	<p>Valid Error 0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Valid Error: The error located in field 15:5 is valid. Slice 2 Bank 3 Error log register 00.</p>	Access:	R/W	
Access:	R/W			

LBS config bits

LBSREG - LBS config bits								
Register Space: MMIO: 0/2/0 Project: BDW 0x46000000 [BDW:GT1, BDW:GT2, BDW:GT3:H, BDW:GT3E] Size (in bits): 32								
Address: 0B124h								
Config Bits for LBS unit								
DWord	Bit	Description						
0	31:27	<p>Retry timer for lookup into LSQC</p> <table border="1"> <tr> <td>Default Value:</td><td>01000b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Time between receiving Reject Response from LSQC and doing a snoop lookup request again onto LSQUnit. 00000b: 0 clocks. 00001b: 1 clocks. 00010b: 2 clocks. ... 01000b: 8 clocks (default value). ... 11111b: 32 clocks. lbcf_retry_timer[4:0].</p>	Default Value:	01000b	Access:	R/W		
Default Value:	01000b							
Access:	R/W							
	26	<p>Recycle parent faster in R/W perf mode</p> <table border="1"> <tr> <td>Default Value:</td><td>1b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Arc into recycle as soon as parent becomes eligible to be recycled. 0: Disabled (recycle possible only when parent is recycled). 1: Enabled (default). lbcf_csr_lsqc_rwperf_quickrec.</p>	Default Value:	1b	Access:	R/W		
Default Value:	1b							
Access:	R/W							
	25	<p>Perf mode for Writes to same address</p> <table border="1"> <tr> <td>Default Value:</td><td>1b</td></tr> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Performance improvement for writes to same address in L3: 0 - Performance mode is not enabled. 1 - Performance mode is enabled (default). lbcf_csr_lsqc_earlyrec.</p>	Default Value:	1b	Project:	BDW	Access:	R/W
Default Value:	1b							
Project:	BDW							
Access:	R/W							
	24:0	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td><td>RO</td></tr> </table>	Access:	RO				
Access:	RO							

LCPLL_CTL

LCPLL_CTL								
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x00000000 Access: R/W Size (in bits): 32								
Address: 130040h-130043h Name: LCPLL Control ShortName: LCPLL_CTL Power: Always on Reset: global								
This register is also known as GT Scratchpad 0 or GTSP0. The LC PLL drives the display core clock (CDCLK) and the core display 2X clock (CD2XCLK). The LC PLL can drive the DDI ports at certain fixed frequencies. The LC PLL will automatically adjust for the reference frequency based on the reference select straps. This register is not reset by the device 2 FLR.								
DWord	Bit	Description						
0	31	PLL Disable This bit will enable or disable the PLL.						
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Enable</td></tr> <tr> <td>1b</td><td>Disable</td></tr> </tbody> </table>	Value	Name	0b	Enable	1b	Disable
Value	Name							
0b	Enable							
1b	Disable							
	30	Restriction After reset, this must not be changed while CD and CD2X clocks are in use.						
		<table border="1"> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>This read only bit indicates the status of the PLL lock.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Not locked or not enabled</td></tr> <tr> <td>1b</td><td>Locked</td></tr> </tbody> </table>	Access:	RO	Value	Name	0b	Not locked or not enabled
Access:	RO							
Value	Name							
0b	Not locked or not enabled							
1b	Locked							

LCPLL_CTL																	
	29:28	<p>Reference Select Select between PLL references.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>00b</td><td>Non-SSC</td><td>Non-Spread reference</td></tr> <tr> <td>01b</td><td>Reserved</td><td>Reserved</td></tr> </tbody> </table> <p>Restriction This must not be changed while this PLL is enabled.</p>	Value	Name	Description	00b	Non-SSC	Non-Spread reference	01b	Reserved	Reserved						
Value	Name	Description															
00b	Non-SSC	Non-Spread reference															
01b	Reserved	Reserved															
	27:26	<p>CD Frequency Select Select between frequencies for CD clock. CD2X clock is always twice the frequency of CD clock. When the fuse DISPLAY_CDCLK_LIMIT = 1, display hardware will ignore the CD Frequency Select and use 450 MHz.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>00b</td><td>450 MHz</td><td>450 MHz CD clock</td></tr> <tr> <td>01b</td><td>540 MHz</td><td>540 MHz CD clock</td></tr> <tr> <td>10b</td><td>337.5 MHz</td><td>337.5 MHz CD clock</td></tr> <tr> <td>11b</td><td>675 MHz</td><td>675 MHz CD clock</td></tr> </tbody> </table> <p>Workaround Do not use DisplayPort with CDCLK 337.5 MHz, audio enabled, port width x4, and link rate HBR2 (5.4 GHz), or else there may be audio corruption or screen corruption.</p> <p>Restriction The 675 MHz CD clock frequency is not supported on ULX. ULX requires extra cooling to support the 540 MHz CD clock frequency. ULT requires extra cooling to support the 675 MHz CD clock frequency. The CD clock frequency should only be changed by following the Display Sequences for Changing CD Clock Frequency.</p>	Value	Name	Description	00b	450 MHz	450 MHz CD clock	01b	540 MHz	540 MHz CD clock	10b	337.5 MHz	337.5 MHz CD clock	11b	675 MHz	675 MHz CD clock
Value	Name	Description															
00b	450 MHz	450 MHz CD clock															
01b	540 MHz	540 MHz CD clock															
10b	337.5 MHz	337.5 MHz CD clock															
11b	675 MHz	675 MHz CD clock															
	25	<p>CD Clock Disable This bit will enable or disable the CD clock for the Display Engine.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Enable</td></tr> <tr> <td>1b</td><td>Disable</td></tr> </tbody> </table>	Value	Name	0b	Enable	1b	Disable									
Value	Name																
0b	Enable																
1b	Disable																
	24	<p>Root CD2X Clock Disable This bit will enable or disable the root of the CD2X clock for the Display Engine. This is the source of both the CD2X and CD clock within display.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Enable</td></tr> <tr> <td>1b</td><td>Disable</td></tr> </tbody> </table>	Value	Name	0b	Enable	1b	Disable									
Value	Name																
0b	Enable																
1b	Disable																

LCPLL_CTL											
23	CD2X Clock Disable This bit will enable or disable the CD2X clock for the Display Engine.										
	<table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Enable</td></tr> <tr> <td>1b</td><td>Disable</td></tr> </tbody> </table>	Value	Name	0b	Enable	1b	Disable				
Value	Name										
0b	Enable										
1b	Disable										
22	Reserved										
21	CD Source Select This bit selects the source for CD clock.										
	<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>LCPLL</td><td>CD clock source is LCPLL</td></tr> <tr> <td>1b</td><td>Fclk</td><td>CD clock source is Fclk</td></tr> </tbody> </table>	Value	Name	Description	0b	LCPLL	CD clock source is LCPLL	1b	Fclk	CD clock source is Fclk	
Value	Name	Description									
0b	LCPLL	CD clock source is LCPLL									
1b	Fclk	CD clock source is Fclk									
	Restriction										
	This field should only be changed as part of the display sequence for package C8.										
20	CD Source Switching										
	Access:	RO									
	This read only bit indicates when the CD clock source switch from LCPLL to Fclk is in progress.										
	<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Not in progress</td><td>CD clock source switch to Fclk not in progress</td></tr> <tr> <td>1b</td><td>In progress</td><td>CD clock source switch to Fclk in progress</td></tr> </tbody> </table>	Value	Name	Description	0b	Not in progress	CD clock source switch to Fclk not in progress	1b	In progress	CD clock source switch to Fclk in progress	
Value	Name	Description									
0b	Not in progress	CD clock source switch to Fclk not in progress									
1b	In progress	CD clock source switch to Fclk in progress									
19	CD Source Fclk										
	Access:	RO									
	This read only bit indicates when the CD clock source switch from LCPLL to Fclk is done.										
	<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Not done</td><td>CD clock source switch to Fclk not done</td></tr> <tr> <td>1b</td><td>Done</td><td>CD clock source switch to Fclk done</td></tr> </tbody> </table>	Value	Name	Description	0b	Not done	CD clock source switch to Fclk not done	1b	Done	CD clock source switch to Fclk done	
Value	Name	Description									
0b	Not done	CD clock source switch to Fclk not done									
1b	Done	CD clock source switch to Fclk done									
18:0	Reserved										
	Format:	MBZ									

LINKM

LINKM				
Register Space:	MMIO: 0/2/0			
Project:	BDW			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Address:	60040h-60043h			
Name:	Transcoder A Link M Value 1			
ShortName:	TRANS_LINKM1_A			
Valid Projects:	BDW			
Power:	off/on			
Reset:	soft			
Address:	61040h-61043h			
Name:	Transcoder B Link M Value 1			
ShortName:	TRANS_LINKM1_B			
Valid Projects:	BDW			
Power:	off/on			
Reset:	soft			
Address:	62040h-62043h			
Name:	Transcoder C Link M Value 1			
ShortName:	TRANS_LINKM1_C			
Valid Projects:	BDW			
Power:	off/on			
Reset:	soft			
Address:	6F040h-6F043h			
Name:	Transcoder EDP Link M Value 1			
ShortName:	TRANS_LINKM1_EDP			
Valid Projects:	BDW			
Power:	Always on			
Reset:	soft			
Description				
There is one instance of this register for each transcoder A/B/C/EDP. This register is double buffered to update on the next MSA after LINKN is written.				
DWord	Bit	Description		
0	31:24	Reserved		
		Format: MBZ		

LINKM		
	23:0	Link M value This field is the link M value for external transmission in the Main Stream Attributes.

LINKN

LINKN				
Register Space:	MMIO: 0/2/0			
Project:	BDW			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Address:	60044h-60047h			
Name:	Transcoder A Link N Value 1			
ShortName:	TRANS_LINKN1_A			
Valid Projects:	BDW			
Power:	off/on			
Reset:	soft			
Address:	61044h-61047h			
Name:	Transcoder B Link N Value 1			
ShortName:	TRANS_LINKN1_B			
Valid Projects:	BDW			
Power:	off/on			
Reset:	soft			
Address:	62044h-62047h			
Name:	Transcoder C Link N Value 1			
ShortName:	TRANS_LINKN1_C			
Valid Projects:	BDW			
Power:	off/on			
Reset:	soft			
Address:	6F044h-6F047h			
Name:	Transcoder EDP Link N Value 1			
ShortName:	TRANS_LINKN1_EDP			
Valid Projects:	BDW			
Power:	Always on			
Reset:	soft			
Description				
There is one instance of this register for each transcoder A/B/C/EDP. This register is double buffered to update on the next MSA after written. Writes to this register arm M/N registers for this transcoder.				
DWord	Bit	Description		
0	31:24	Reserved		
		Format: MBZ		

LINKN		
	23:0	Link N value This field is the link N value for external transmission in the Main Stream Attributes and VB-ID.

LNCF config save msg

LNCFCSR - LNCF config save msg				
DWord	Bit	Description		
0	31:10	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
Access:	RO			
	9:0	<p>Context save bit</p> <table border="1"> <tr> <td>Access:</td> <td>R/W Hardware Clear</td> </tr> </table> <p>Bit[9]. Power Context Save Request 0: Power context save is not being requested (default). 1: Power context save is being requested. Unit needs to self-clear this bit upon sampling. Bits[8:0]. QWord Credits for Power Context Save Request. Minimum Credits = 1: Unit may send 1 QWord pair (enough for first LRI at least). Maximum Credits = 511: Unit may send 511 QWord pairs. A QWord pair is defined as a 32-bit register address and the corresponding 32-bits of register data. Note that the LRI header and END commands are 64-bits each (32-bit command followed by 32-bit NOOP) and consume one QWord credit. Only valid with PWRCTX_SAVE_REQ (Bit9).</p>	Access:	R/W Hardware Clear
Access:	R/W Hardware Clear			

Load Indirect Base Vertex

3DPRIM_BASE_VERTEX - Load Indirect Base Vertex				
DWord	Bit	Description		
0	31:0	Base Vertex <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td style="padding: 2px;">Format:</td> <td style="padding: 2px;">S31</td> </tr> </table> <p>This register is used to store the Base Vertex of the 3D_PRIMITIVE command when Load Indirect Enable is set.</p>	Format:	S31
Format:	S31			

Load Indirect Instance Count

3DPRIM_INSTANCE_COUNT - Load Indirect Instance Count		
Register Space: MMIO: 0/2/0		
Project:	BDW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	02438h-0243Bh	
Valid Projects:	BDW	
DWord	Bit	Description
0	31:0	Instance Count This register is used to store the Instance Count of the 3D_PRIMITIVE command when Load Indirect Enable is set.

Load Indirect Start Instance

3DPRIM_START_INSTANCE - Load Indirect Start Instance				
DWord	Bit	Description		
0	31:0	<p>Start Vertex</p> <table border="1"> <tr> <td>Format:</td> <td>U32</td> </tr> </table> <p>This register is used to store the Start Instance of the 3D_PRIMITIVE command when Load Indirect Enable is set.</p>	Format:	U32
Format:	U32			

Load Indirect Start Vertex

3DPRIM_START_VERTEX - Load Indirect Start Vertex				
DWord	Bit	Description		
0	31:0	<p>Start Vertex</p> <table border="1"> <tr> <td>Format:</td> <td>U32</td> </tr> </table> <p>This register is used to store the Start Vertex of the 3D_PRIMITIVE command when Load Indirect Enable is set.</p>	Format:	U32
Format:	U32			

Load Indirect Vertex Count

3DPRIM_VERTEX_COUNT - Load Indirect Vertex Count				
DWord	Bit	Description		
0	31:0	Vertex Count <table border="1"> <tr> <td>Format:</td> <td>U32</td> </tr> </table> <p>This register is used to store the Vertex Count of the 3D_PRIMITIVE command when Load Indirect Enable is set.</p>	Format:	U32
Format:	U32			

LPFC control register

LPFCCNTL - LPFC control register					
DWord	Bit	Description			
0	31	<p>LPFC enable signal</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>LPPC event collection enable signal. Incf_lpfc_cnt_en.</p>	Access:	R/W	
Access:	R/W				
30:0	<p>Reserved</p> <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Reserved.</p>	Project:	BDW	Access:	RO
Project:	BDW				
Access:	RO				

LTCD Error Injection Register

LBCFERR - LTCD Error Injection Register								
DWord	Bit	Description						
0	31:25	Reserved <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Project:	BDW	Access:	RO		
Project:	BDW							
Access:	RO							
	24	LTISEQSL parity error interrupt <table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Parity error interrupt to LTISEQ Slice.</p>	Default Value:	0b	Project:	BDW	Access:	R/W
Default Value:	0b							
Project:	BDW							
Access:	R/W							
	23	Bank hang on parity disable <table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table>	Default Value:	0b	Project:	BDW	Access:	R/W
Default Value:	0b							
Project:	BDW							
Access:	R/W							
	22	Parity Error Injection Enable <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>0: Disable parity error injection. 1: Enable parity error injection. lbcf_parity_err_inject_en. Do not Enable this when ECC Error injection is enabled.</p>	Project:	BDW	Access:	R/W		
Project:	BDW							
Access:	R/W							
	21	Double Bit Error injection <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>0: Default No error injected. 1: Double bit error is injected. lbcf_ecc_2bit_err_inject. Single bit Error Injection and double bit error injection are mutually exclusive. Do not Enable this when Parity Error injection is enabled.</p>	Project:	BDW	Access:	R/W		
Project:	BDW							
Access:	R/W							

LBCFERR - LTCD Error Injection Register

	20	Single Bit Error injection				
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>0: Default No error injected. 1: Single bit error is injected. <code>lbcf_ecc_1bit_err_inject</code>. Single bit Error Injection and double bit error injection are mutually exclusive. Do not Enable this when Parity Error injection is enabled.</p>	Project:	BDW	Access:	R/W
Project:	BDW					
Access:	R/W					
	19	ECC Error Injection Enable				
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>0: Disable ECC error injection. 1: Enable ECC error injection. <code>lbcf_ecc_err_inject_en</code>. Do not Enable this when Parity Error injection is enabled.</p>	Project:	BDW	Access:	R/W
Project:	BDW					
Access:	R/W					
	18:4	Row address for error injection				
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Row address for which error is injected. For ECC error injection, the same row address is overloaded to inject ECC error for that particular row address. SLM configuration. For Address: Rowaddress [16:7] is applicable for SLM banks and Parity injection is enabled and Rowaddress[18:7] is applicable for ECC (for both NonSLM/SLM banks). Sub bank is applicable only for Parity injection. Only Subbank 0, 1, 2, 3 are supported and are only related to SLM Banks (4KB). Total 12 bits address. Bits 18:7: Row address. Bits 6:4: Sub-Bank number. <code>lbcf_parity_err_inject_rowaddr[9:0]</code>. <code>lbcf_parity_err_inject_subbank[2:0]</code>. 16:7 - For SLM parity only. <code>lbcf_parity_err_inject_rowaddr[9:0]</code>. <code>lbcf_ecc_err_inject_rowaddr[11:0]</code>. For ECC error injection, the same row address is overloaded to inject ECC error for that particular row address.</p>	Project:	BDW	Access:	R/W
Project:	BDW					
Access:	R/W					

LBCFERR - LTCD Error Injection Register

	3:2	Bank ID for error injection				
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table>	Project:	BDW	Access:	R/W
Project:	BDW					
Access:	R/W					
		<p>00b: Inject in Bank 0. 01b: Inject in Bank 1. 10b: Inject in Bank 2. 11b: Inject in Bank 3 (error injection not supported for SLM bank3). <code>lbcf_err_inject_bankid[1:0]</code>.</p>				
	1:0	Slice ID for Error injection				
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table>	Project:	BDW	Access:	R/W
Project:	BDW					
Access:	R/W					
		<p>00b: Inject error in Slice 0. 01b: Inject error in Slice 1. 10b: Inject error in Slice 2. <code>lbcf_err_inject_sliceid</code>.</p>				

Main Graphic Arbiter Error Report

ERROR - Main Graphic Arbiter Error Report								
DWord	Bit	Description						
0	31	Reserved Error Bits 31 <table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> <tr> <td>Future Use.</td><td></td></tr> </table>	Default Value:	0b	Access:	R/W	Future Use.	
Default Value:	0b							
Access:	R/W							
Future Use.								
	30	Reserved Error Bits 30 <table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> <tr> <td>Future Use.</td><td></td></tr> </table>	Default Value:	0b	Access:	R/W	Future Use.	
Default Value:	0b							
Access:	R/W							
Future Use.								
	29	Reserved Error Bits 29 <table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> <tr> <td>Future Use.</td><td></td></tr> </table>	Default Value:	0b	Access:	R/W	Future Use.	
Default Value:	0b							
Access:	R/W							
Future Use.								
	28	Reserved Error Bits 28 <table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> <tr> <td>Future Use.</td><td></td></tr> </table>	Default Value:	0b	Access:	R/W	Future Use.	
Default Value:	0b							
Access:	R/W							
Future Use.								
	27	Reserved Error Bits 27 <table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> <tr> <td>Future Use.</td><td></td></tr> </table>	Default Value:	0b	Access:	R/W	Future Use.	
Default Value:	0b							
Access:	R/W							
Future Use.								
	26	Reserved Error Bits 26 <table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> <tr> <td>Future Use.</td><td></td></tr> </table>	Default Value:	0b	Access:	R/W	Future Use.	
Default Value:	0b							
Access:	R/W							
Future Use.								

ERROR - Main Graphic Arbiter Error Report

	25	Reserved Error Bits 25	
		Default Value:	0b
		Access:	R/W
		Future Use.	
	24	Reserved Error Bits 24	
		Default Value:	0b
		Access:	R/W
		Future Use.	
	23	Reserved Error Bits 23	
		Default Value:	0b
		Access:	R/W
		Future Use.	
	22	Reserved Error Bits 22	
		Default Value:	0b
		Access:	R/W
		Future Use.	
	21	Reserved Error Bits 21	
		Default Value:	0b
		Access:	R/W
		Future Use.	
	20	Reserved Error Bits 20	
		Default Value:	0b
		Access:	R/W
		Future Use.	
	19	Reserved Error Bits 19	
		Default Value:	0b
		Access:	R/W
		Future Use.	
	18	Reserved Error Bits 18	
		Default Value:	0b
		Access:	R/W
		Future Use.	

ERROR - Main Graphic Arbiter Error Report

	17	Reserved Error Bits 17	Default Value:	0b
		Access:		R/W
		Future Use.		
	16	Reserved Error Bits 16	Default Value:	0b
		Access:		R/W
		Future Use.		
	15	Reserved Error Bits 15	Default Value:	0b
		Access:		R/W
		ctx_fault_ctxt_not_prsmt_err - The Present (P) field in the context-entry used to process the DMA request is Clear.		
	14	Reserved Error Bits 14	Default Value:	0b
		Access:		R/W
		ctx_fault_root_not_prsmt_err - The present (UP/LP) field in the root-entry used to process the untranslated request with PASID is 0.		
	13	Reserved Error Bits 13	Default Value:	0b
		Access:		R/W
		ctx_fault_pasid_not_prsnt_err - PASID Table entry to be used does not have the PRESENT flag set. This means the PASID entry is not valid.		
	12	Reserved Error Bits 12	Default Value:	0b
		Access:		R/W
		ctx_fault_pasid_ovflw_err - PASID Table size in extended context entry defines the number of PASIDs that will be supported. If hardware receives a PASID number outside the supported boundary, report as an error.		
	11	Reserved Error Bits 11	Default Value:	0b
		Access:		R/W
		ctx_fault_pasid_dis_err - Submission of advanced context where the PASID field is not enabled in the extended context entry.		

ERROR - Main Graphic Arbiter Error Report

		Reserved Error Bits 10
	10	Default Value: 0b Access: R/W
		rstrm_fault_nowb_atomic_err - All page table accesses in advanced context with A/D bits are considered as atomic operations in WB space. However if the memory type for the page table accesses come out as anything but WB, that is an error.
	9	Reserved
	8	Unloaded PD Error
		Default Value: 0b Access: R/W
		The Cache Line containing a PD entry being accessed, was marked as invalid in the last PD load cycle.
	7	Reserved Error Bits 7
		Default Value: 0b Access: R/W
		Future Use.
	6	Reserved
	5	Reserved
	4	Reserved
	3	Reserved
	2	Invalid Page Directory Entry Error
		Default Value: 0b Access: R/W
		PD entry's valid bit is 0.
	1	Reserved
	0	TLB Page Fault Error
		Default Value: 0b Access: R/W
		A TLB Page's GTT translation generated a page fault (GTT entry not valid).

Main Graphic Arbiter Error Report 2

ERROR_2 - Main Graphic Arbiter Error Report2						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	040A4h					
DWord	Bit	Description				
0	31:0	<p>Main Graphic Arbiter Error Report 2</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Bit [31:6] - Reserved. Bit [5:0] - tlbpPEND_REG_FAULTCNT[5:0].</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Main Graphic Arbiter Error Report 3

ERROR_3 - Main Graphic Arbiter Error Report 3							
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x00000000 [BDW] Size (in bits): 32							
Address: 040A8h This register is used to report different error conditions. Error bits are writable.							
DWord	Bit	Description					
0	31:16	Reserved <table border="1"> <tr> <td>Default Value:</td><td>0000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	0000h	Access:	RO	
Default Value:	0000h						
Access:	RO						
15	Error3 Bits 15 <table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> Future Use.	Default Value:	0b	Access:	R/W		
Default Value:	0b						
Access:	R/W						
14	Error3 Error Bits 14 <table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> Future Use.	Default Value:	0b	Access:	R/W		
Default Value:	0b						
Access:	R/W						
13	Error3 Error Bits 13 <table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> Future Use.	Default Value:	0b	Access:	R/W		
Default Value:	0b						
Access:	R/W						
12	Error3 Error Bits 12 <table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> Future Use.	Default Value:	0b	Access:	R/W		
Default Value:	0b						
Access:	R/W						
11	Error3 Error Bits 11 <table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> invalid_varmtrr_overlap_memtype_rd.	Default Value:	0b	Project:	BDW	Access:	R/W
Default Value:	0b						
Project:	BDW						
Access:	R/W						

ERROR_3 - Main Graphic Arbiter Error Report 3

	10	Error3 Error Bits 10						
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table>	Default Value:	0b	Project:	BDW	Access:	R/W
Default Value:	0b							
Project:	BDW							
Access:	R/W							
		invalid_varmtrr_overlap_memtype_wr.						
	9	Error3 Error Bits 9						
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table>	Default Value:	0b	Project:	BDW	Access:	R/W
Default Value:	0b							
Project:	BDW							
Access:	R/W							
		invalid_default_memtype_value_rd.						
	8	Error3 Error Bits 8						
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table>	Default Value:	0b	Project:	BDW	Access:	R/W
Default Value:	0b							
Project:	BDW							
Access:	R/W							
		invalid_default_memtype_value_wr.						
	7	Error3 Error Bits 7						
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table>	Default Value:	0b	Project:	BDW	Access:	R/W
Default Value:	0b							
Project:	BDW							
Access:	R/W							
		invalid_varmtrr_memtype_value_rd.						
	6	Error3 Error Bits 6						
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table>	Default Value:	0b	Project:	BDW	Access:	R/W
Default Value:	0b							
Project:	BDW							
Access:	R/W							
		invalid_varmtrr_memtype_value_wr.						
	5	Error3 Error Bits 5						
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table>	Default Value:	0b	Project:	BDW	Access:	R/W
Default Value:	0b							
Project:	BDW							
Access:	R/W							
		invalid_fixedmtrr_memtype_value_rd.						

ERROR_3 - Main Graphic Arbiter Error Report 3

	4	Error3 Error Bits 4						
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>invalid_fixedmtrr_memtype_value_wr.</p>	Default Value:	0b	Project:	BDW	Access:	R/W
Default Value:	0b							
Project:	BDW							
Access:	R/W							
	3	Error3 Error Bits 3						
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>gttc_internal_error.</p>	Default Value:	0b	Project:	BDW	Access:	R/W
Default Value:	0b							
Project:	BDW							
Access:	R/W							
	2	Error3 Error Bits 2						
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table>	Default Value:	0b	Project:	BDW	Access:	R/W
Default Value:	0b							
Project:	BDW							
Access:	R/W							
	1	Error3 Error Bits 1						
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>tlbpend_internal_error.</p>	Default Value:	0b	Access:	R/W		
Default Value:	0b							
Access:	R/W							
	0	Error3 Error Bits 0						
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>reg_wrid_internal_error.</p>	Default Value:	0b	Access:	R/W		
Default Value:	0b							
Access:	R/W							

Main Graphic Arbiter Error Report Register

GFX_ARB_ERROR_RPT - Main Graphic Arbiter Error Report Register

Register Space:	MMIO: 0/2/0	
Project:	BDW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	040A0h	
This register is used to report error conditions. Error bits are writable.		
DWord	Bit	Description
0	31:16	Reserved Format: MBZ
	15:9	Reserved
	8	Unloaded PD Error The Cache Line containing a PD entry being accessed was marked as invalid in the last PD load cycle.
	7	Hardware Status Page VTD Translation Error HWSP's VTD translation generated an error. (HPA is not accessible for DMA read or write.)
	6	Page Directory Entry VTD Translation Error PD entry's VTD translation generated an error. (HPA is not accessible for DMA read or write.)
	5	Context Page VTD Translation Error A Context Page's VTD translation generated an error. (HPA is not accessible for DMA read or write.)
	4	TLB Page VTD Translation Error A TLB Page's VTD translation generated an error. (HPA is not accessible for DMA read or write.)
	3	Hardware Status Page Fault Error HWSP's GTT translation generated a page fault (GTT entry not valid).
	2	Invalid Page Directory entry error PD entry's valid bit is 0.
	1	Context Page Fault Error A Context Page's GTT translation generated a page fault (GTT entry not valid).
	0	TLB Page Fault Error A TLB Page's GTT translation generated a page fault (GTT entry not valid).

MASTER_INT_CTL

MASTER_INT_CTL												
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x00000000 Access: R/W, RO Size (in bits): 32												
Address: 44200h-44203h Name: Master Interrupt Control ShortName: MASTER_INT_CTL Valid Projects: BDW Power: Always on Reset: soft												
This register has the master enable for graphics interrupts and gives an overview of what interrupts are pending. An interrupt pending bit will read 1b while one or more interrupts of that category are set (IIR) and enabled (IER). All Pending Interrupts are ORed together to generate the combined interrupt. The combined interrupt is ANDed with the Master Interrupt enable to create the master enabled interrupt. The master enabled interrupt goes to PCI device 2 interrupt processing. The master interrupt enable must be set before any of these interrupts will propagate to PCI device 2 interrupt processing.												
DWord	Bit	Description										
0	31	Master Interrupt Enable <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> <tr> <td colspan="2">This is the master control for graphics interrupts. This must be enabled for any of these interrupts to propagate to PCI device 2 interrupt processing.</td></tr> <tr> <td align="center">Value</td><td align="center">Name</td></tr> <tr> <td>0b</td><td>Master interrupt disable</td></tr> <tr> <td>1b</td><td>Master interrupt enable</td></tr> </table>	Access:	R/W	This is the master control for graphics interrupts. This must be enabled for any of these interrupts to propagate to PCI device 2 interrupt processing.		Value	Name	0b	Master interrupt disable	1b	Master interrupt enable
Access:	R/W											
This is the master control for graphics interrupts. This must be enabled for any of these interrupts to propagate to PCI device 2 interrupt processing.												
Value	Name											
0b	Master interrupt disable											
1b	Master interrupt enable											
PCU Interrupts Pending <table border="1"> <tr> <td>Access:</td><td>RO</td></tr> <tr> <td colspan="2" rowspan="2">This field indicates if interrupts of this category are pending.</td></tr> </table>	Access:	RO	This field indicates if interrupts of this category are pending.									
Access:	RO											
This field indicates if interrupts of this category are pending.												
		Reserved										
24	Audio Codec Interrupts Pending <table border="1"> <tr> <td>Access:</td><td>RO</td></tr> <tr> <td colspan="2" rowspan="2">This field indicates if interrupts of this category are pending.</td></tr> </table>	Access:	RO	This field indicates if interrupts of this category are pending.								
Access:	RO											
This field indicates if interrupts of this category are pending.												

MASTER_INT_CTL		
23	DE PCH Interrupts Pending	Access: RO This field indicates if interrupts of this category are pending. The PCH Display interrupt is configured through the SDE interrupt registers.
22	DE Misc Interrupts Pending	Access: RO This field indicates if interrupts of this category are pending.
21	Reserved	
20	DE Port Interrupts Pending	Access: RO This field indicates if interrupts of this category are pending.
19	Reserved	
18	DE Pipe C Interrupts Pending	Access: RO This field indicates if interrupts of this category are pending.
17	DE Pipe B Interrupts Pending	Access: RO This field indicates if interrupts of this category are pending.
16	DE Pipe A Interrupts Pending	Access: RO This field indicates if interrupts of this category are pending.
15:8	Reserved	
7	Reserved	
6	VEBox Interrupts Pending	Access: RO This field indicates if interrupts of this category are pending.
5	Reserved	
4	GTPM Interrupts Pending	Access: RO This field indicates if interrupts of this category are pending.

MASTER_INT_CTL				
	3	VCS2 Interrupts Pending		
<table border="1"> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>This field indicates if interrupts of this category are pending.</p>			Access:	RO
Access:	RO			
	2	VCS1 Interrupts Pending		
<table border="1"> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>This field indicates if interrupts of this category are pending.</p>			Access:	RO
Access:	RO			
	1	Blitter Interrupts Pending		
<table border="1"> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>This field indicates if interrupts of this category are pending.</p>			Access:	RO
Access:	RO			
	0	Render Interrupts Pending		
<table border="1"> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>This field indicates if interrupts of this category are pending.</p>			Access:	RO
Access:	RO			

Master Latency Timer

MLT2_0_2_0_PCI - Master Latency Timer								
DWord	Bit	Description						
0	7:0	<p>Master Latency Timer Count Value</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> <tr> <td colspan="2">Hardwired to 0s.</td></tr> </table>	Default Value:	00000000b	Access:	RO	Hardwired to 0s.	
Default Value:	00000000b							
Access:	RO							
Hardwired to 0s.								
The IGD does not support the programmability of the master latency timer because it does not perform bursts.								

Master start timer

MASTIMER - Master start timer						
DWord	Bit	Description				
0	31:0	<p>Master start timer value</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000000000000000000000000001b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Master Start Timer (MSTSTTMR). Ipcfg_Ipfcc_master_start_timer [31:0]. So many clocks are expired before starting the rest of the counters. Time to wait is 256 * value clocks. Value for this register cannot be 0.</p>	Default Value:	00000000000000000000000000000001b	Access:	R/W
Default Value:	00000000000000000000000000000001b					
Access:	R/W					

Maximum Latency

MAXLAT_0_2_0_PCI - MaximumLatency			
Register Space: PCI: 0/2/0			
Project: BDW			
Default Value: 0x00000000			
Size (in bits): 8			
Address: 0003Fh			
The Integrated Graphics Device has no requirement for the settings of Latency Timers.			
DWord	Bit	Description	
0	7:0	Maximum Latency Value	
		Default Value:	00000000b
		Access:	RO
		Hardwired to 0s because the IGD has no specific requirements for how often it needs to access the PCI bus.	

Max Outstanding Pending TLB Requests 0

GFX_PEND_TLB_0 - Max Outstanding Pending TLB Requests 0			
DWord	Bit	Description	
0		TEX Limit Enable Bit	
		Default Value:	0b
		Access:	R/W
This bit is used to enable the pending TLB requests limitation function for the Texture Cache. When set, the number of internal pending read requests which require a TLB read does not exceed the programmed counter value.			
30		Reserved	
		Default Value:	0b
		Access:	RO
29:24		TEX TLB Limit Count	
		Default Value:	000000b
		Access:	R/W
This is the MAX number of Allowed internal pending read requests which require a TLB read.			
23		DC Limit Enable Bit	
		Default Value:	0b
		Access:	R/W
This bit is used to enable the pending TLB requests limitation function for the Instruction Cache. When set, the number of internal pending read requests which require a TLB read does not exceed the programmed counter value.			
22		Reserved	
		Default Value:	0b
		Access:	RO
21:16		DC TLB Limit Count	
		Default Value:	000000b
		Access:	R/W
This is the MAX number of Allowed internal pending read requests which require a TLB read.			

GFX_PEND_TLB_0 - Max Outstanding Pending TLB Requests 0

	15	VF Limit Enable Bit				
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
		This bit is used to enable the pending TLB requests limitation function for the Vertex Fetch. When set, the number of internal pending read requests which require a TLB read does not exceed the programmed counter value.				
	14	Reserved				
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	0b	Access:	RO
Default Value:	0b					
Access:	RO					
	13:8	VF TLB Limit Count				
		<table border="1"> <tr> <td>Default Value:</td><td>000000b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table>	Default Value:	000000b	Access:	R/W
Default Value:	000000b					
Access:	R/W					
		This is the MAX number of Allowed internal pending read requests which require a TLB read.				
	7	VMC Limit Enable bit				
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
		This bit is used to enable the pending TLB requests limitation function for the Video Motion Compensation. When set, the number of internal pending read requests which require a TLB read does not exceed the programmed counter value.				
	6	Reserved				
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	0b	Access:	RO
Default Value:	0b					
Access:	RO					
	5:0	VMC TLB Limit Count				
		<table border="1"> <tr> <td>Default Value:</td><td>000000b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table>	Default Value:	000000b	Access:	R/W
Default Value:	000000b					
Access:	R/W					
		This is the MAX number of Allowed internal pending read requests which require a TLB read.				

Max Outstanding Pending TLB Requests 1

GFX_PEND_TLB_1 - Max Outstanding Pending TLB Requests 1						
DWord	Bit	Description				
0	31	<p>SOL Limit Enable Bit</p> <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>This bit is used to enable the pending TLB requests limitation function for the SOL. When set, the number of internal pending read requests which require a TLB read does not exceed the programmed counter value.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
	30	<p>Reserved</p> <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Default Value:	0b	Access:	RO
Default Value:	0b					
Access:	RO					
	29:24	<p>SOL TLB Limit Count</p> <table border="1"> <tr> <td>Default Value:</td> <td>000000b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>This is the MAX number of Allowed internal pending read requests which require a TLB read.</p>	Default Value:	000000b	Access:	R/W
Default Value:	000000b					
Access:	R/W					
	23	<p>L3 Limit Enable Bit</p> <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>This bit is used to enable the pending TLB requests limitation function for the L3. When set, the number of internal pending read requests which require a TLB read does not exceed the programmed counter value.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
	22	<p>Reserved</p> <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Default Value:	0b	Access:	RO
Default Value:	0b					
Access:	RO					
	21:16	<p>L3 TLB Limit Count</p> <table border="1"> <tr> <td>Default Value:</td> <td>000000b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>This is the MAX number of Allowed internal pending read requests which require a TLB read.</p>	Default Value:	000000b	Access:	R/W
Default Value:	000000b					
Access:	R/W					

GFX_PEND_TLB_1 - Max Outstanding Pending TLB Requests 1

	15	RCZ Limit Enable Bit				
		Default Value:	0b			
		Access:	R/W			
		This bit is used to enable the pending TLB requests limitation function for the Render Depth Cache. When set, the number of internal pending read requests which require a TLB read does not exceed the programmed counter value.				
	14	Reserved				
		Default Value:	0b			
		Access:	RO			
	13:8	RCZ TLB Limit Count				
		Default Value:	000000b			
		Access:	R/W			
		RCZ TLB Limit Count Project: All Format: U6				
		This is the MAX number of Allowed internal pending read requests which require a TLB read.				
	7	RCC Limit Enable bit				
		Default Value:	0b			
		Access:	R/W			
		This bit is used to enable the pending TLB requests limitation function for the Render Color Cache. When set, the number of internal pending read requests which require a TLB read does not exceed the programmed counter value.				
	6	Reserved				
		Default Value:	0b			
		Access:	RO			
	5:0	RCC TLB Limit Count				
		Default Value:	000000b			
		Access:	R/W			
		This is the MAX number of Allowed internal pending read requests which require a TLB read.				

Max Outstanding Pending TLB Requests 2

GFX_PEND_TLB_2 - Max Outstanding Pending TLB Requests 2						
DWord	Bit	Description				
0	31:16	Reserved <table border="1"> <tr> <td>Default Value:</td><td>0000000000000000b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table>	Default Value:	0000000000000000b	Access:	R/W
Default Value:	0000000000000000b					
Access:	R/W					
	15	BLT Limit Enable Bit <table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>This bit is used to enable the pending TLB requests limitation function for the Blitter engine. When set, the number of internal pending read requests which require a TLB read does not exceed the programmed counter value.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
	14	Reserved <table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
	13:8	BLT TLB Limit Count <table border="1"> <tr> <td>Default Value:</td><td>000000b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>BLT TLB Limit Count Project: All Format: U6 This is the MAX number of Allowed internal pending read requests which require a TLB read.</p>	Default Value:	000000b	Access:	R/W
Default Value:	000000b					
Access:	R/W					
	7	Reserved				
	6	Reserved <table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
	5:0	Reserved				

Max Outstanding Pending TLB Requests 3

GFX_PEND_TLB_3 - Max Outstanding Pending TLB Requests 3						
DWord	Bit	Description				
0	31	<p>VEBX Limit Enable Bit</p> <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>This bit is used to enable the pending TLB requests limitation function for the VEBX engine. When set, the number of internal pending read requests which require a TLB read does not exceed the programmed counter value.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
	30	<p>Reserved</p> <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
	29:24	<p>VEBX TLB Limit Count</p> <table border="1"> <tr> <td>Default Value:</td> <td>000000b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>This is the MAX number of Allowed internal pending read requests which require a TLB read.</p>	Default Value:	000000b	Access:	R/W
Default Value:	000000b					
Access:	R/W					
	23	<p>MFX1 Limit Enable Bit</p> <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>This bit is used to enable the pending TLB requests limitation function for the Media1 engine. When set, the number of internal pending read requests which require a TLB read does not exceed the programmed counter value.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
	22	<p>Reserved</p> <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
	21:16	<p>MFX1 TLB Limit Count</p> <table border="1"> <tr> <td>Default Value:</td> <td>000000b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>This is the MAX number of Allowed internal pending read requests which require a TLB read.</p>	Default Value:	000000b	Access:	R/W
Default Value:	000000b					
Access:	R/W					

GFX_PEND_TLB_3 - Max Outstanding Pending TLB Requests 3

	15	MFX0 Limit Enable Bit	Default Value:	0b
		Access:		R/W
	This bit is used to enable the pending TLB requests limitation function for the Media0 engine. When set, the number of internal pending read requests which require a TLB read does not exceed the programmed counter value.			
	14	Reserved	Default Value:	0b
		Access:		R/W
	13:8	MFX0 TLB Limit Count	Default Value:	000000b
		Access:		R/W
	MFX0 TLB Limit Count Project: All Format: U6 This is the MAX number of Allowed internal pending read requests which require a TLB read.			
	7	GFX Limit Enable bit	Default Value:	0b
		Access:		R/W
	This bit is used to enable the pending TLB requests limitation function for the Render engine. When set, the number of internal pending read requests which require a TLB read does not exceed the programmed counter value.			
	6	Reserved	Default Value:	0b
		Access:		R/W
	5:0	GFX TLB Limit Count	Default Value:	000000b
		Access:		R/W
	This is the MAX number of Allowed internal pending read requests which require a TLB read.			

MAX Requests Allowed - GAM

GFX_MAX_REQ_COUNT - MAX Requests Allowed - GAM						
Programmable Request Count - GAM						
DWord	Bit	Description				
0	31:26	<p>GAP Writes Max Request Limit Count</p> <table border="1"> <tr> <td>Default Value:</td> <td>010000b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>This is the MAX number of Allowed Write Requests Count - These counters keep track of the accepted write requests from all GAP clients (RCZ, HiZ, Stc, RCC, L3). Minimum count value must be = 1.</p>	Default Value:	010000b	Access:	R/W
Default Value:	010000b					
Access:	R/W					
	25:20	<p>CVS Max Request Limit Count</p> <table border="1"> <tr> <td>Default Value:</td> <td>111111b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>This is the MAX number of Allowed Requests Count - These counters keep track of the accepted requests from each client. Requests are counted, regardless of kind of cycle (Miss/Hit/Present). Minimum count value must be = 1.</p>	Default Value:	111111b	Access:	R/W
Default Value:	111111b					
Access:	R/W					
	19	<p>Reserved</p> <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Default Value:	0b	Access:	RO
Default Value:	0b					
Access:	RO					
	18:13	<p>L3 Max Request Limit Count</p> <table border="1"> <tr> <td>Default Value:</td> <td>010000b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>This is the MAX number of Allowed Requests Count - These counters keep track of the accepted requests from each client. Requests are counted, regardless of kind of cycle (Miss/Hit/Present). Minimum count value must be = 1.</p>	Default Value:	010000b	Access:	R/W
Default Value:	010000b					
Access:	R/W					
	12	<p>Reserved</p> <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Default Value:	0b	Access:	RO
Default Value:	0b					
Access:	RO					

GFX_MAX_REQ_COUNT - MAX Requests Allowed - GAM							
	11:6	Z Request Limit Count					
<table border="1"> <tr> <td>Default Value:</td><td>000100b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>This is the MAX number of Allowed Requests Count - These counters keep track of the accepted requests from each client. Requests are counted, regardless of kind of cycle (Miss/Hit/Present). Minimum count value must be = 1.</p>				Default Value:	000100b	Access:	R/W
Default Value:	000100b						
Access:	R/W						
	5:0	RCC Request Limit Count					
<table border="1"> <tr> <td>Default Value:</td><td>000001b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>This is the MAX number of Allowed Requests Count - These counters keep track of the accepted requests from each client. Requests are counted, regardless of kind of cycle (Miss/Hit/Present). Minimum count value must be = 1.</p>				Default Value:	000001b	Access:	R/W
Default Value:	000001b						
Access:	R/W						

MAX Requests Allowed - MFX

MEDIA_MAX_REQ_COUNT - MAX Requests Allowed - MFX						
Programmable Request Count - MFX						
DWord	Bit	Description				
0	31:24	<p>GFX Max Request Limit Count</p> <table border="1"> <tr> <td>Default Value:</td> <td>00010000b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>This is the MAX number of Allowed Requests Count - These counters keep track of the accepted requests from each engine. Requests are counted, regardless of kind of cycle (Miss/Hit/Present). Minimum count value must be = 1.</p>	Default Value:	00010000b	Access:	R/W
Default Value:	00010000b					
Access:	R/W					
	23:16	<p>MFX Max Request Limit Count</p> <table border="1"> <tr> <td>Default Value:</td> <td>00100000b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>This is the MAX number of Allowed Requests Count - These counters keep track of the accepted requests from each engine. Requests are counted, regardless of kind of cycle (Miss/Hit/Present). Minimum count value must be = 1.</p>	Default Value:	00100000b	Access:	R/W
Default Value:	00100000b					
Access:	R/W					
	15:14	<p>Reserved</p> <table border="1"> <tr> <td>Default Value:</td> <td>00b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Default Value:	00b	Access:	RO
Default Value:	00b					
Access:	RO					
	13:8	<p>VLF Max Request Limit Count</p> <table border="1"> <tr> <td>Default Value:</td> <td>010000b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>This is the MAX number of Allowed Requests Count - These counters keep track of the accepted requests from each client. Requests are counted, regardless of kind of cycle (Miss/Hit/Present). Minimum count value must be = 1.</p>	Default Value:	010000b	Access:	R/W
Default Value:	010000b					
Access:	R/W					
	7:6	<p>Reserved</p> <table border="1"> <tr> <td>Default Value:</td> <td>00b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Default Value:	00b	Access:	RO
Default Value:	00b					
Access:	RO					

MEDIA_MAX_REQ_COUNT - MAX Requests Allowed - MFX			
	5:0	MFX Max Request Limit Count	
		Default Value:	100000b
		Access:	R/W
This is the MAX number of Allowed Requests Count - These counters keep track of the accepted requests from each client. Requests are counted, regardless of kind of cycle (Miss/Hit/Present). Minimum count value must be = 1.			

MAX Requests Allowed - VEBX and BLT

VEBX_BLIT_MAX_REQ_COUNT - MAX Requests Allowed - VEBX and BLT			
Register Space:		MMIO: 0/2/0	
Project:		BDW	
Default Value:		0x08081020	
Size (in bits):		32	
Address:		04AA8h	
Programmable Request Count - VEBX and BLT			
DWord	Bit	Description	
0	31:24	BLT Max Request Limit Count	
		Default Value:	00001000b
	23:16	Access:	R/W
		This is the MAX number of Allowed Requests Count - These counters keep track of the accepted requests from each engine. Requests are counted, regardless of kind of cycle (Miss/Hit/Present).	
	15:8	VEBX Max Request Limit Count	
		Default Value:	00001000b
	7:0	Access:	R/W
		This is the MAX number of Allowed Requests Count - These counters keep track of the accepted requests from each engine. Requests are counted, regardless of kind of cycle (Miss/Hit/Present).	
	7:0	VLF1 Max Request Limit Count	
		Default Value:	00010000b
	7:0	Access:	R/W
		This is the MAX number of Allowed Requests Count - These counters keep track of the accepted requests from each engine. Requests are counted, regardless of kind of cycle (Miss/Hit/Present).	
	7:0	MFX1 Max Request Limit Count	
		Default Value:	00100000b
	7:0	Access:	R/W
		This is the MAX number of Allowed Requests Count - These counters keep track of the accepted requests from each engine. Requests are counted, regardless of kind of cycle (Miss/Hit/Present).	

MBC Control Register

MBCTL - MBC Control Register											
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x00010000 Size (in bits): 32											
Address: 0907Ch											
MBC Control Register											
DWord	Bit	Description									
0	31:17	ECORSVD <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> <tr> <td colspan="2">ECO purposes Reserved</td></tr> </table>	Project:	BDW	Access:	R/W	ECO purposes Reserved				
	Project:	BDW									
	Access:	R/W									
	ECO purposes Reserved										
	16	16	VCR Fuse Writes as Posted <table border="1"> <tr> <td>Default Value:</td><td>1b</td></tr> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> <tr> <td colspan="2">BDW - Non-posted fuse fetching is NOT supported starting on BDW project. Only posted is allowed (the default). 0 - MBCunit sends VCR Fuse Writes as Non-posted. 1 - MBCunit sends VCR Fuse Writes as posted. Non-posted write mode is not supported in Broadwell</td></tr> </table>	Default Value:	1b	Project:	BDW	Access:	R/W	BDW - Non-posted fuse fetching is NOT supported starting on BDW project. Only posted is allowed (the default). 0 - MBCunit sends VCR Fuse Writes as Non-posted. 1 - MBCunit sends VCR Fuse Writes as posted. Non-posted write mode is not supported in Broadwell	
		Default Value:	1b								
		Project:	BDW								
		Access:	R/W								
		BDW - Non-posted fuse fetching is NOT supported starting on BDW project. Only posted is allowed (the default). 0 - MBCunit sends VCR Fuse Writes as Non-posted. 1 - MBCunit sends VCR Fuse Writes as posted. Non-posted write mode is not supported in Broadwell									
15:8		RSVD	<table border="1"> <tr> <td>Access:</td><td>RO</td></tr> </table>	Access:	RO						
Access:		RO									
7		Disable Wait for SQempty in MAE	<table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> <tr> <td colspan="2">0 - Wait for SQempty for MAE update Flow. 1 - MBC MAE update FSM does not wait for the SQempty to complete the FSM.</td></tr> </table>	Access:	R/W	0 - Wait for SQempty for MAE update Flow. 1 - MBC MAE update FSM does not wait for the SQempty to complete the FSM.					
Access:		R/W									
0 - Wait for SQempty for MAE update Flow. 1 - MBC MAE update FSM does not wait for the SQempty to complete the FSM.											
6	Reserved										
5	RSVD	<table border="1"> <tr> <td>Access:</td><td>RO</td></tr> </table>	Access:	RO							
Access:	RO										
4	RSVD										
3	RSVD										
2	RSVD										

MBCTL - MBC Control Register		
	4	MBC Driver Boot Enable Access: R/W Config bit for driver managed boot kick off. 1 - Enable Boot Fetch without any PM interaction. 0 - Default (no action). This Bit is cleared by the Hardware once the Boot fetch is complete.
	3	Context Fetch Needed Access: R/W Context Fetch Needed for Power Exits. 0 - Context Fetch Not Needed. 1 - Context Fetch Needed for Power Exits (CPD Entry).
	2	BME Update Enable Access: R/W BME update Enable: 0 - Default BME Update is not Enabled. MBC ignores all the BME updates from SA. 1- BME update is Enabled.
	1	MAE Update Enable Access: R/W MAE update Enable: 0 - Default MAE Update is not Enabled. MBC ignores all the MAE updates from SA. 1 - MAE update is Enabled. MBC responds to the MAE updates.
	0	RSVD Access: RO

Media 1 TLB Control Register

M1TCR - Media 1 TLB Control Register						
DWord	Bit	Description				
0	31:1	Reserved <table border="1"> <tr> <td>Default Value:</td><td>00000000000000000000000000000000b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	00000000000000000000000000000000b	Access:	RO
Default Value:	00000000000000000000000000000000b					
Access:	RO					
	0	Invalidate TLBs on the corresponding Engine <table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>SW writes 1 to invalidate the TLBs for the associated engine and HW clears the bit when invalidation is complete. To ensure proper invalidation of the TLBs, SW has to ensure the corresponding engine's HW pipeline is flushed and cleared from all its memory accesses. Otherwise HW cannot guarantee the proper invalidation for TLBs. This bit is self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					

Media 2 TLB Control Register

M2TCR - Media 2 TLB Control Register		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04268h	
DWord	Bit	Description
0	31:1	Reserved
		Default Value:
	0	Invalidate TLBs on the corresponding Engine
		Default Value:
		Access:
		R/W
		SW writes 1 to invalidate the TLBs for the associated engine and HW clears the bit when invalidation is complete. To ensure proper invalidation of the TLBs, SW has to ensure the corresponding engine's HW pipeline is flushed and cleared from all its memory accesses. Otherwise HW cannot guarantee the proper invalidation for TLBs. This bit is self clear.

Message Address

MA_0_2_0_PCI - Message Address						
DWord	Bit	Description				
0	31:2	<p>Message Address</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000000000000000000000000000b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>FLR Resettable Used by system software to assign an MSI address to the device. The device handles an MSI by writing the padded contents of the MD register to this address.</p>	Default Value:	00000000000000000000000000000000b	Access:	R/W
Default Value:	00000000000000000000000000000000b					
Access:	R/W					
<p>Force Dword Align</p> <table border="1"> <tr> <td>Default Value:</td> <td>00b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Hardwired to 0 so that addresses assigned by system software are always aligned on a DWORD address boundary.</p>	Default Value:	00b	Access:	RO		
Default Value:	00b					
Access:	RO					

Message Control

MC_0_2_0_PCI - Message Control						
DWord	Bit	Description				
0	7	<p>64 Bit Capable</p> <table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Hardwired to 0 to indicate that the function does not implement the upper 32 bits of the Message address register and is incapable of generating a 64-bit memory address.</p>	Default Value:	0b	Access:	RO
Default Value:	0b					
Access:	RO					
6:4	<p>Multiple Message Enable</p> <table border="1"> <tr> <td>Default Value:</td><td>000b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>FLR Resettable System software programs this field to indicate the actual number of messages allocated to this device. This number will be equal to or less than the number actually requested. Value: Number of requests 000: 1 001: 2 010: 4 011: 8 100: 16 101: 32 110: Reserved 111: Reserved</p>	Default Value:	000b	Access:	R/W	
Default Value:	000b					
Access:	R/W					
3:1	<p>Multiple Message Capable</p> <table border="1"> <tr> <td>Default Value:</td><td>000b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>System Software reads this field to determine the number of messages being requested by this device. Hardwired to 000b to indicate number of requests is 1.</p>	Default Value:	000b	Access:	RO	
Default Value:	000b					
Access:	RO					
0	<p>MSI Enable</p> <table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Controls the ability of this device to generate MSIs.</p>	Default Value:	0b	Access:	R/W	
Default Value:	0b					
Access:	R/W					

Message Data

MD_0_2_0_PCI - MessageData						
DWord	Bit	Description				
0	15:0	<p>Message Data</p> <table border="1"> <tr> <td>Default Value:</td><td>0000000000000000b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>FLR Resettable Base message data pattern assigned by system software and used to handle an MSI from the device. When the device must generate an interrupt request, it writes a 32-bit value to the memory address specified in the MA register. The upper 16 bits are always set to 0. The lower 16 bits are supplied by this register.</p>	Default Value:	0000000000000000b	Access:	R/W
Default Value:	0000000000000000b					
Access:	R/W					

Message Register

MSGREG - Message Register						
DWord	Bit	Description				
0	31:16	Mask Bits <table border="1"> <tr> <td>Default Value:</td><td>0000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> Reserved.	Default Value:	0000h	Access:	RO
Default Value:	0000h					
Access:	RO					
15	GO_PROTOCOL_GAM_REQUEST15 <table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> Reserved.	Default Value:	0b	Access:	R/W	
Default Value:	0b					
Access:	R/W					
14	GO_PROTOCOL_GAM_REQUEST14 <table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> Reserved.	Default Value:	0b	Access:	R/W	
Default Value:	0b					
Access:	R/W					
13	GO_PROTOCOL_GAM_REQUEST13 <table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> Reserved.	Default Value:	0b	Access:	R/W	
Default Value:	0b					
Access:	R/W					
12	GO_PROTOCOL_GAM_REQUEST12 <table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> Reserved.	Default Value:	0b	Access:	R/W	
Default Value:	0b					
Access:	R/W					
11	GO_PROTOCOL_GAM_REQUEST11 <table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> Reserved.	Default Value:	0b	Access:	R/W	
Default Value:	0b					
Access:	R/W					

MSGREG - Message Register

	10	GO_PROTOCOL_GAM_REQUEST10
		Default Value:
		Access:
		Reserved.
	9	GO_PROTOCOL_GAM_REQUEST9
		Default Value:
		Access:
		Reserved.
	8	GO_PROTOCOL_GAM_REQUEST8
		Default Value:
		Access:
		Reserved.
	7	GO_PROTOCOL_GAM_REQUEST7
		Default Value:
		Access:
		Reserved.
	6	GO_PROTOCOL_GAM_REQUEST6
		Default Value:
		Access:
		Reserved.
	5	GO_PROTOCOL_GAM_REQUEST5
		Default Value:
		Access:
		Reserved.
	4	GO_PROTOCOL_GAM_REQUEST4
		Default Value:
		Access:
		Reserved.
	3	GO_PROTOCOL_GAM_REQUEST3
		Default Value:
		Access:
		Reserved.

MSGREG - Message Register								
	2	GO_PROTOCOL_GAM_REQUEST2 <table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> <tr> <td colspan="2">Reserved.</td></tr> </table>	Default Value:	0b	Access:	R/W	Reserved.	
Default Value:	0b							
Access:	R/W							
Reserved.								
	1	GO_PROTOCOL_GAM_REQUEST1 <table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> <tr> <td colspan="2">Reserved.</td></tr> </table>	Default Value:	0b	Access:	R/W	Reserved.	
Default Value:	0b							
Access:	R/W							
Reserved.								
	0	GO_PROTOCOL_GAM_REQUEST0 <table border="1"> <tr> <td>Default Value:</td><td>1b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> <tr> <td colspan="2">0 - GPM to GAM Busy Ack Indication. 1 - GPM to GAM Idle Ack Indication.</td></tr> </table>	Default Value:	1b	Access:	R/W	0 - GPM to GAM Busy Ack Indication. 1 - GPM to GAM Idle Ack Indication.	
Default Value:	1b							
Access:	R/W							
0 - GPM to GAM Busy Ack Indication. 1 - GPM to GAM Idle Ack Indication.								

Message Signaled Interrupts Capability ID

MSI_CAPID_0_2_0_PCI - Message Signaled Interrupts Capability ID		
Register Space:	PCI: 0/2/0	
Project:	BDW	
Default Value:	0x0000D005	
Size (in bits):	16	
Address:	00090h	
When a device supports MSI it can generate an interrupt request to the processor by writing a predefined data item (a message) to a predefined memory address.		
DWord	Bit	Description
0	15:8	Reserved
		Default Value: 11010000b
		Access: RO
	7:0	Capability ID
		Default Value: 00000101b
		Access: RO
This field is hardwired to the value 05h to identify the CAP_ID as being for MSI registers.		

Messaging Register for GPMunit

MSG_GPM - Messaging Register for GPMunit

Register Space: MMIO: 0/2/0

Project: BDW

Default Value: 0x00000000

Size (in bits): 32

Address: 00C00h

Message registers have bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16].

To set bit0, for example, the data would be 0x0001_0001.

To clear bit0, for example, the data would be 0x0001_0000.

Note that mask bit is the data bit offset + 16. Message registers are protected from non-GT writes via the Message Channel.

DWord	Bit	Description	
0	31:16	Reserved	Access: RO
	15	GPM Messages Bit 15 Placeholder for GPM Messages. RPMunit could self-clear these bits upon sampling.	Access: R/W
	14	GPM Messages Bit 14 Placeholder for GPM Messages. RPMunit could self-clear these bits upon sampling.	Access: R/W
	13	GPM Messages Bit 13 Placeholder for GPM Messages. RPMunit could self-clear these bits upon sampling.	Access: R/W
	12	GPM Messages Bit 12 Placeholder for GPM Messages. RPMunit could self-clear these bits upon sampling.	Access: R/W
	11	GPM Messages Bit 11 Placeholder for GPM Messages. RPMunit could self-clear these bits upon sampling.	Access: R/W

MSG_GPM - Messaging Register for GPMunit						
	10	GPM Messages Bit 10 <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Placeholder for GPM Messsages. RPMunit could self-clear these bits upon sampling.</p>	Access:	R/W		
Access:	R/W					
	9	GPM Messages Bit 9 <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Placeholder for GPM Messsages. RPMunit could self-clear these bits upon sampling.</p>	Access:	R/W		
Access:	R/W					
	8	GPM Messages Bit 8 <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Placeholder for GPM Messsages. RPMunit could self-clear these bits upon sampling.</p>	Access:	R/W		
Access:	R/W					
	7	GPM Messages Bit 7 <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Placeholder for GPM Messsages RPMunit could self-clear these bits upon sampling.</p>	Project:	BDW	Access:	R/W
Project:	BDW					
Access:	R/W					
	6	GPM Messages Bit 6 <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Placeholder for GPM Messsages. RPMunit could self-clear these bits upon sampling.</p>	Project:	BDW	Access:	R/W
Project:	BDW					
Access:	R/W					
	5	GPM Messages Bit 5 <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Placeholder for GPM Messsages. RPMunit could self-clear these bits upon sampling.</p>	Project:	BDW	Access:	R/W
Project:	BDW					
Access:	R/W					
	4	Request to send CPD Exit Ack Message on EventBus (U2C) <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Request from GPMunit for RPMunit to send CPD_EXIT_ACK message on the Eventbus. RPMunit self-clears this bit upon sampling.</p>	Access:	R/W		
Access:	R/W					

MSG_GPM - Messaging Register for GPMunit				
	3	<p>Request to send CPD Enter Ack Message on EventBus (U2C)</p> <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Request from GPMunit for RPMunit to send CPD_ENTER_ACK message on the Eventbus. RPMunit self-clears this bit upon sampling.</p>	Access:	R/W
Access:	R/W			
	2	<p>Request to send Credit Active Deassert Message on EventBus (U2C)</p> <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Request from GPMunit for RPMunit to send CREDIT_ACTIVE_DEASSERT message on the Eventbus. RPMunit self-clears this bit upon sampling.</p>	Access:	R/W
Access:	R/W			
	1	<p>Request to send Credit Active Assert Message on EventBus (U2C)</p> <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Request from GPMunit for RPMunit to send CREDIT_ACTIVE_ASSERT message on the Eventbus. RPMunit self-clears this bit upon sampling.</p>	Access:	R/W
Access:	R/W			
	0	<p>Request to send IDI Shutdown Ack Message on EventBus (U2C)</p> <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Request from GPMunit for RPMunit to send IDI_SHUTDOWN_ACK message on the Eventbus. RPMunit self-clears this bit upon sampling.</p>	Access:	R/W
Access:	R/W			

Messaging Register for MDRBunit

MSG_MDRB - Messaging Register for MDRBunit					
DWord	Bit	Description			
0	31:16	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO				
15:2	<p>MDRB Messages</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Placeholder for MDRB Messages. MDRBunit could self-clear these bits upon sampling.</p>	Access:	R/W		
Access:	R/W				
1	<p>RFO Enable/Disable Ack for RPM (internal) RFO Request</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>RFO Enable/Disable Ack for Internal RFO Request. Enable Ack = 1'b1 Disable Ack = 1'b0</p>	Access:	R/W		
Access:	R/W				
0	<p>RFO Enable/Disable Ack for U2C (Evtentbus) RFO Request</p> <table border="1"> <tr> <td>Default Value:</td> <td>1b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>RFO Enable/Disable Ack for U2C RFO Request. Enable Ack = 1'b1 Disable Ack = 1'b0</p>	Default Value:	1b	Access:	R/W
Default Value:	1b				
Access:	R/W				

Messaging Register for MGSRunit

MSG_MGSR - Messaging Register for MGSRunit				
DWord	Bit	Description		
0	31:16	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
Access:	RO			
15:0	<p>MGSR Messages</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Placeholder for MGSR Messages. MGSRunit could self-clear these bits upon sampling.</p>	Access:	R/W	
Access:	R/W			

MFC_AVC CABAC INSERTION COUNT

AVC CABAC INSERTION COUNT - MFC_AVC CABAC INSERTION COUNT		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Source:	VideoCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	128ACh	
Valid Projects:	[BDW]	
Address:	1C8ACh	
Valid Projects:	[BDW:GT3]	
This register stores the count in bytes of CABAC ZERO_WORD insertion . It is primarily provided for statistical data gathering.		
DWord	Bit	Description
0	31:0	MFC AVC Cabac Insertion Count Total number of bytes in the bitstream output before for the CABAC zero word insertion. This count is updated each time when the insertion count is incremented.

MFC_AVC Bitstream Decoding Front-End Parsing Logic Error Counter

MFC_VIN_AVD_ERROR_CNTR - MFC_AVC Bitstream Decoding Front-End Parsing Logic Error Counter		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Source:	VideoCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	12804h	
Valid Projects:	[BDW]	
Address:	1C804h	
Valid Projects:	[BDW:GT3]	
DWord	Bit	Description
0 avd_error_flagsR[31:0]	31:0	Reserved Format: _____ MBZ

MFC Image Status Control

MFC_IMAGE_STATUS_CONTROL - MFC Image Status Control					
Register Space:	MMIO: 0/2/0				
Project:	BDW				
Source:	VideoCS				
Default Value:	0x00000000				
Access:	RO				
Size (in bits):	32				
Trusted Type:	1				
Address:	128B8h				
Valid Projects:	[BDW]				
Address:	1C8B8h				
Valid Projects:	[BDW:GT3]				
This register stores the suggested data for next frame in multi-pass.					
DWord	Bit	Description			
0	31:24	Cumulative slice delta QP			
	23:16	QP Value suggested slice QP delta value for frame level Rate control. This value can be +ve or -ve			
	15	QP-Polarity Change Cumulative slice delta QP polarity change.			
	14:13	Num-Pass Polarity Change Number of passes after cumulative slice delta QP polarity changes.			
	12	Reserved <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	BDW	Format:
Project:	BDW				
Format:	MBZ				
11:8	Total Num-Pass				
7:4	Reserved <table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ		
Format:	MBZ				
3	Reserved <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	BDW	Format:	MBZ
Project:	BDW				
Format:	MBZ				
2	Panic Panic triggered to avoid too big packed file.				
1	Frame Bit Count Frame Bit count over-run/under-run flag				
0	Max Conformance Flag Max Macroblock conformance flag or Frame Bit count over-run/under-run				

MFC Image Status Mask

MFC_IMAGE_STATUS_MASK - MFC Image Status Mask		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Source:	VideoCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	128B4h	
Valid Projects:	[BDW]	
Address:	1C8B4h	
Valid Projects:	[BDW:GT3]	
This register stores the image status(flags).		
DWord	Bit	Description
0	31:0	Control Mask Control Mask for dynamic frame repeat.

MFC QP Status Count

MFC_QUP_CT - MFC QP Status Count						
Register Space: MMIO: 0/2/0 Project: BDW Source: VideoCS Default Value: 0x00000000 Access: RO Size (in bits): 32 Trusted Type: 1						
Address: 128BCh Valid Projects: [BDW]						
Address: 1C8BCh Valid Projects: [BDW:GT3]						
This register stores the suggested QP COUNTS in multi-pass.						
DWord	Bit	Description				
0	31:24	Cumulative QP Adjust <table border="1"> <tr> <td>Format:</td><td>U8</td></tr> <tr> <td colspan="2">Cumulative QP adjustment after multiple passes. If there is no need to multi-pass, this value would be zero. (This is in sign magnitude form).</td></tr> </table>	Format:	U8	Cumulative QP adjustment after multiple passes. If there is no need to multi-pass, this value would be zero. (This is in sign magnitude form).	
Format:	U8					
Cumulative QP adjustment after multiple passes. If there is no need to multi-pass, this value would be zero. (This is in sign magnitude form).						
23:0	Cumulative QP <table border="1"> <tr> <td>Format:</td><td>U24</td></tr> <tr> <td colspan="2">Cumulative QP for all MB of a Frame (Can be used for computing average QP).</td></tr> </table>	Format:	U24	Cumulative QP for all MB of a Frame (Can be used for computing average QP).		
Format:	U24					
Cumulative QP for all MB of a Frame (Can be used for computing average QP).						

MFD Error Status

MFD_ERROR_STATUS - MFD Error Status				
Register Space: MMIO: 0/2/0 Project: BDW Source: VideoCS Default Value: 0x00000000 Access: RO Size (in bits): 32 Trusted Type: 1				
Address: 12800h		Valid Projects: [BDW]		
Address: 1C800h		Valid Projects: [BDW:GT3]		
This register stores the error status flags and count reports by the bit-stream decoder. This register is not part of hardware context save and restore. Driver should read the content prior to starting a new batch/frame.				
DWord	Bit	Description		
0	31:20	Reserved <table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table> <p>This field is currently reserved</p>	Format:	MBZ
Format:	MBZ			
19:16	AVC Short Format Error Flags <table border="1"> <tr> <td>Exists If:</td><td>// AVC Short Format == True</td></tr> </table> <p>Bit-stream error detected by VLD short format bit-stream decoder. These flags are reset at the beginning of a frame and updated until starting of another frame.</p> <ul style="list-style-type: none"> [19] – Slice Type SE Error Flag – Invalid Slice Type SE [18] – MMCO SE Error Flag – Invalid memory management control operation SE. MMCO Loop does not end (mmco control != 0) even after all MMCO SEs are decoded OR MMCO SEs are still being decoded and MMCO SE loop end (mmco control == 0) is hit [17] – Reordering IDC Error Flag – Syntax Element modification_of_pic_nums_idc >= 6 OR modification_of_pic_nums_idc != 3 (end of reordering loop) but reordering count has already hit maximum value [16] – Premature bitstream end is hit before finishing slice header decode 	Exists If:	// AVC Short Format == True	
Exists If:	// AVC Short Format == True			
15:0	Bit-stream Error flags <table border="1"> <tr> <td>Exists If:</td><td>// AVC CAVLC, AVC CABAC, VC1 and MPEG2 == True</td></tr> </table> <p>Bitstream error detected by the VLD bit-stream decoder. These flags are reset at the beginning of a frame and updated until starting of another frame.</p> <ul style="list-style-type: none"> AVC CAVLC: Please refer to AVC CAVLC table for each bit field AVC CABAC: Please refer to AVC CABAC table for each bit field VC1: Please refer to VC1 table for each bit field MPEG2: Please refer to MPEG2 table for each bit field 	Exists If:	// AVC CAVLC, AVC CABAC, VC1 and MPEG2 == True	
Exists If:	// AVC CAVLC, AVC CABAC, VC1 and MPEG2 == True			

MFD Picture Parameter

MFD_PICTURE_PARAM - MFD Picture Parameter			
Register Space: MMIO: 0/2/0 Project: BDW Source: VideoCS Default Value: 0x00000000 Access: R/W Size (in bits): 32 Trusted Type: 1			
Address: 12820h Valid Projects: [BDW]			
Address: 1C820h Valid Projects: [BDW:GT3]			
DWord	Bit	Description	
0	31:0	Reserved	Format: MBZ

MFX_Memory_Latency_Count1

MFX_LAT_CT1 - MFX_Memory_Latency_Count1		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Source:	VideoCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	12870h	
Valid Projects:	[BDW]	
Address:	1C870h	
Valid Projects:	[BDW:GT3]	
This register stores the max and min memory latency counts reported on reference read requests. This register is not part of hardware context save and restore.		
DWord	Bit	Description
0	31:24	Max Request Count This field indicates the maximum number of requests allowed by the memory sub-system channel.
	23:16	Current Request Count This field indicates the number of requests currently outstanding in the memory sub-system. This field should report with a value of zero at the end of frame; otherwise the motion compensation engine is most likely hung waiting for read data to be returned from sub-system.
	15:8	MFX Reference picture read request - Max Latency Count in 8xMedia clock cycles This field reports the maximum memory latency count on all reference reads requested by the motion compensation engine.
	7:0	MFX Reference picture read request - Min Latency Count in 8xMedia clock cycles This field reports the minimum memory latency count on all reference reads requested by the motion compensation engine.

MFX0 Context Element Descriptor (High Part)

MFX0_CTX_EDR_H - MFX0 Context Element Descriptor (High Part)						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04444h					
DWord	Bit	Description				
0	31:0	MFX0 Context Element Descriptor (High Part)				
		<table border="1"><tr><td>Default Value:</td><td>00000000h</td></tr><tr><td>Access:</td><td>R/W</td></tr></table>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

MFX0 Context Element Descriptor (Low Part)

MFX0_CTX_EDR_L - MFX0 Context Element Descriptor (Low Part)						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000009					
Size (in bits):	32					
Address:	04440h					
DWord	Bit	Description				
0	31:0	MFX0 Context Element Descriptor (Low Part)				
		<table border="1"><tr><td>Default Value:</td><td>00000009h</td></tr><tr><td>Access:</td><td>R/W</td></tr></table>	Default Value:	00000009h	Access:	R/W
Default Value:	00000009h					
Access:	R/W					

MFX0 Context Element Descriptor (Low Part)

MFX0_CTX_EDR_L - MFX0 Context Element Descriptor (Low Part)						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000009					
Size (in bits):	32					
Address:	04440h					
DWord	Bit	Description				
0	31:0	MFX0 Context Element Descriptor <table border="1"><tr><td>Default Value:</td><td>00000009h</td></tr><tr><td>Access:</td><td>R/W</td></tr></table>	Default Value:	00000009h	Access:	R/W
Default Value:	00000009h					
Access:	R/W					

MFX0 Fault Counter

MFX0_FAULT_CNTR - MFX0 Fault Counter						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	045A8h					
DWord	Bit	Description				
0	31:0	MFX0 Fault Counter				
		<table border="1"><tr><td>Default Value:</td><td>00000000h</td></tr><tr><td>Access:</td><td>RO</td></tr></table>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

MFX0 Fixed Counter

MFX0_FIXED_CNTR - MFX0 Fixed Counter						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	045ACh					
DWord	Bit	Description				
0	31:0	MFX0 Fixed Counter <table border="1"><tr><td>Default Value:</td><td>0000000h</td></tr><tr><td>Access:</td><td>RO</td></tr></table>	Default Value:	0000000h	Access:	RO
Default Value:	0000000h					
Access:	RO					

MFX0_PDP0/PML4/PASID Descriptor (High Part)

MFX0_CTX_PDP0_H - MFX0_PDP0/PML4/PASID Descriptor (High Part)		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0444Ch	
DWord	Bit	Description
0	31:0	MFX0_PDP0/PML4/PASID Descriptor (High Part)
		Default Value: 00000000h
		Access: R/W

MFX0_PDP0/PML4/PASID Descriptor (Low Part)

MFX0_CTX_PDP0_L - MFX0_PDP0/PML4/PASID Descriptor (Low Part)						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04448h					
DWord	Bit	Description				
0	31:0	MFX0_PDP0/PML4/PASID Descriptor (Low Part)				
		<table border="1"><tr><td>Default Value:</td><td>00000000h</td></tr><tr><td>Access:</td><td>R/W</td></tr></table>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

MFX0 PDP1 Descriptor Register (High Part)

MFX0_CTX_PDP1_H - MFX0 PDP1 Descriptor Register (High Part)		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04454h	
DWord	Bit	Description
0	31:0	MFX0 PDP1 Descriptor Register (High Part)
		Default Value: 00000000h
		Access: R/W

MFX0 PDP1 Descriptor Register (Low Part)

MFX0_CTX_PDP1_L - MFX0 PDP1 Descriptor Register (Low Part)		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04450h	
DWord	Bit	Description
0	31:0	MFX0 PDP1 Descriptor Register (Low Part)
		Default Value: 00000000h
		Access: R/W

MFX0 PDP2 Descriptor Register (High Part)

MFX0_CTX_PDP2_H - MFX0 PDP2 Descriptor Register (High Part)		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0445Ch	
DWord	Bit	Description
0	31:0	MFX0 PDP2 Descriptor Register (High Part)
		Default Value: 00000000h
		Access: R/W

MFX0 PDP2 Descriptor Register (Low Part)

MFX0_CTX_PDP2_L - MFX0 PDP2 Descriptor Register (Low Part)		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04458h	
DWord	Bit	Description
0	31:0	MFX0 PDP2 Descriptor Register (Low Part)
		Default Value: 00000000h
		Access: R/W

MFX0 PDP3 Descriptor Register (High Part)

MFX0_CTX_PDP3_H - MFX0 PDP3 Descriptor Register (High Part)		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04464h	
DWord	Bit	Description
0	31:0	MFX0 PDP3 Descriptor Register (High Part)
		Default Value: 00000000h
		Access: R/W

MFX0 PDP3 Descriptor Register (Low Part)

MFX0_CTX_PDP3_L - MFX0 PDP3 Descriptor Register (Low Part)		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04460h	
DWord	Bit	Description
0	31:0	MFX0 PDP3 Descriptor Register (Low Part)
		Default Value: 00000000h
		Access: R/W

MFX1 Context Element Descriptor (High Part)

MFX1_CTX_EDR_H - MFX1 Context Element Descriptor (High Part)						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04484h					
DWord	Bit	Description				
0	31:0	MFX1 Context Element Descriptor (High Part)				
		<table border="1"><tr><td>Default Value:</td><td>00000000h</td></tr><tr><td>Access:</td><td>R/W</td></tr></table>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

MFX1 Context Element Descriptor (Low Part)

MFX1_CTX_EDR_L - MFX1 Context Element Descriptor (Low Part)						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000009					
Size (in bits):	32					
Address:	04480h					
DWord	Bit	Description				
0	31:0	MFX1 Context Element Descriptor (Low Part)				
		<table border="1"><tr><td>Default Value:</td><td>00000009h</td></tr><tr><td>Access:</td><td>R/W</td></tr></table>	Default Value:	00000009h	Access:	R/W
Default Value:	00000009h					
Access:	R/W					

MFX1 Context Element Descriptor (Low Part)

MFX1_CTX_EDR_L - MFX1 Context Element Descriptor (Low Part)						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000009					
Size (in bits):	32					
Address:	04480h					
DWord	Bit	Description				
0	31:0	MFX1 Context Element Descriptor <table border="1"><tr><td>Default Value:</td><td>00000009h</td></tr><tr><td>Access:</td><td>R/W</td></tr></table>	Default Value:	00000009h	Access:	R/W
Default Value:	00000009h					
Access:	R/W					

MFX1 Fault Counter

MFX1_FAULT_CNTR - MFX1 Fault Counter		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	045B0h	
DWord	Bit	Description
0	31:0	MFX1 Fault Counter
		Default Value: 00000000h
		Access: RO

MFX1 Fixed Counter

MFX1_FIXED_CNTR - MFX1 Fixed Counter		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	045B4h	
DWord	Bit	Description
0	31:0	MFX1 Fixed Counter
		Default Value: 00000000h
		Access: RO

MFX1_PDP0/PML4/PASID Descriptor (High Part)

MFX1_CTX_PDP0_H - MFX1_PDP0/PML4/PASID Descriptor (High Part)		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0448Ch	
DWord	Bit	Description
0	31:0	MFX1_PDP0/PML4/PASID Descriptor (High Part)
		Default Value: 00000000h
		Access: R/W

MFX1_PDP0/PML4/PASID Descriptor (Low Part)

MFX1_CTX_PDP0_L - MFX1_PDP0/PML4/PASID Descriptor (Low Part)						
DWord	Bit	Description				
0	31:0	MFX1_PDP0/PML4/PASID Descriptor (Low Part) <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

MFX1 PDP1 Descriptor Register (High Part)

MFX1_CTX_PDP1_H - MFX1 PDP1 Descriptor Register (High Part)		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04494h	
DWord	Bit	Description
0	31:0	MFX1 PDP1 Descriptor Register (High Part)
		Default Value: 00000000h
		Access: R/W

MFX1 PDP1 Descriptor Register (Low Part)

MFX1_CTX_PDP1_L - MFX1 PDP1 Descriptor Register (Low Part)		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04490h	
DWord	Bit	Description
0	31:0	MFX1 PDP1 Descriptor Register (Low Part)
		Default Value: 00000000h
		Access: R/W

MFX1 PDP2 Descriptor Register (High Part)

MFX1_CTX_PDP2_H - MFX1 PDP2 Descriptor Register (High Part)		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0449Ch	
DWord	Bit	Description
0	31:0	MFX1 PDP2 Descriptor Register (High Part)
		Default Value: 00000000h
		Access: R/W

MFX1 PDP2 Descriptor Register (Low Part)

MFX1_CTX_PDP2_L - MFX1 PDP2 Descriptor Register (Low Part)		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	04498h	
DWord	Bit	Description
0	31:0	MFX1 PDP2 Descriptor Register (Low Part)
		Default Value: 00000000h
		Access: R/W

MFX1 PDP3 Descriptor Register (High Part)

MFX1_CTX_PDP3_H - MFX1 PDP3 Descriptor Register (High Part)		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	044A4h	
DWord	Bit	Description
0	31:0	MFX1 PDP3 Descriptor Register (High Part)
		Default Value: 00000000h
		Access: R/W

MFX1 PDP3 Descriptor Register (Low Part)

MFX1_CTX_PDP3_L - MFX1 PDP3 Descriptor Register (Low Part)		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	044A0h	
DWord	Bit	Description
0	31:0	MFX1 PDP3 Descriptor Register (Low Part)
		Default Value: 00000000h
		Access: R/W

MFX Frame BitStream SE/BIN Count

MFX_SE-BIN_CT - MFX Frame BitStream SE/BIN Count		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Source:	VideoCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	1286Ch	
Valid Projects:	[BDW]	
Address:	1C86Ch	
Valid Projects:	[BDW:GT3]	
This register stores the number of BINs (AVC CABAC) and SEs (CAVLD, VLD) decoded in a frame. This register is not part of hardware context save and restore.		
DWord	Bit	Description
0	31:0	MFX Frame Bit-stream SE/BIN Count Total number of BINs/SEs decoded in current frame. This number is used with frame performance count to derive Bin/clk or SE/clk.

MFX Frame Macroblock Count

MFX_MB_COUNT - MFX Frame Macroblock Count

Register Space:	MMIO: 0/2/0
Project:	BDW
Source:	VideoCS
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1

Address: 12868h

Valid Projects: [BDW]

Address: 1C868h

Valid Projects: [BDW:GT3]

This register stores the number of Macro-blocks decoded/encoded in current frame. This register is not part of hardware context save and restore.

DWord	Bit	Description				
0	31:20	MBZ <table border="1"> <tr> <td>Exists If:</td> <td>// JPEG == True</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table> <p>This field is currently reserved</p>	Exists If:	// JPEG == True	Format:	MBZ
Exists If:	// JPEG == True					
Format:	MBZ					
Intra MB Count <table border="1"> <tr> <td>Exists If:</td> <td>// AVC CAVLC, AVC CABAC, VC1 and MPEG2 == True</td> </tr> <tr> <td>Format:</td> <td>U16</td> </tr> </table>	Exists If:	// AVC CAVLC, AVC CABAC, VC1 and MPEG2 == True	Format:	U16		
Exists If:	// AVC CAVLC, AVC CABAC, VC1 and MPEG2 == True					
Format:	U16					
19:0	JPEG Block Count <table border="1"> <tr> <td>Exists If:</td> <td>// JPEG == True</td> </tr> <tr> <td>Format:</td> <td>U20</td> </tr> </table> <p>This 20-bit field indicates the number of 8x8 blocks within the JPEG frame. This field is clear at the start of decoding a new frame.</p>	Exists If:	// JPEG == True	Format:	U20	
Exists If:	// JPEG == True					
Format:	U20					
Number of MB Concealment <table border="1"> <tr> <td>Exists If:</td> <td>// AVC CAVLC, AVC CABAC, VC1 and MPEG2 == True</td> </tr> </table> <p>This 16-bit field indicates the number of MB is concealed by hardware. This field is clear at the start of decoding a new frame.</p>	Exists If:	// AVC CAVLC, AVC CABAC, VC1 and MPEG2 == True				
Exists If:	// AVC CAVLC, AVC CABAC, VC1 and MPEG2 == True					

MFX Frame Motion Comp Miss Count

MFX_MISS_CT - MFX Frame Motion Comp Miss Count				
Register Space: MMIO: 0/2/0 Project: BDW Source: VideoCS Default Value: 0x00000000 Access: RO Size (in bits): 32 Trusted Type: 1				
Address: 12888h Valid Projects: [BDW]				
Address: 1C888h Valid Projects: [BDW:GT3]				
This register stores the total number of cacheline hits occurred in the motion compensation cache per frame. This register is not part of hardware context save and restore.				
DWord	Bit	Description		
0	31:0	MFX Frame Motion Comp cache miss Count <table border="1"> <tr> <td>Format:</td><td>U32</td></tr> </table> Total number of CL misses occurred in the 12KB cache of the motion compensation engine per frame. This number is used along with MFX Frame Motion Comp Read Count to derive motion comp cache miss/hit ratio.	Format:	U32
Format:	U32			

MFX Frame Motion Comp Read Count

MFX_READ_CT - MFX Frame Motion Comp Read Count		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Source:	VideoCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	12484h	
This register stores the total number of reference picture read requests made by the Motion Compensation engine per frame. This register is not part of hardware context save and restore.		
DWord	Bit	Description
0	31:20	Reserved
		Format: MBZ
	19:0	MFX Frame Motion Comp CL read request Count Total number of reference picture read requests by the motion compensation engine per frame.

MFX Frame Performance Count

MFX_FRAME_PERFORMANCE_CT - MFX Frame PerformanceCount		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Source:	VideoCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	12860h	
Valid Projects:	[BDW]	
Address:	1C860h	
Valid Projects:	[DevBDW:GT3, DevBDW:GT4]	
This register stores the number of clock cycles spent decoding/encoding the current frame. This register is not part of hardware context save and restore.		
DWord	Bit	Description
0	31:0	MFX Frame Performance Counter Total number of clocks between frame start and frame end. This counter is incremented on cmclk

MFX Frame Row-Stored/BitStream Read Count

MFX_ROW-PER-BS_COUNT - MFX Frame Row-Stored/BitStream Read Count		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Source:	VideoCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	12880h	
Valid Projects:	[BDW]	
Address:	1C880h	
Valid Projects:	[BDW:GT3]	
This register stores the total number of row-stored/bit-stream read requests made by the pre-fetch engine per frame. This register is not part of hardware context save and restore.		
DWord	Bit	Description
0	31:16	Reserved Format: MBZ
	15:0	MFX row-stored/bit-stream read request Count Total number of row-stored/bit-stream read requests sent by the memory pre-fetch engine per frame.

MFX LRA 0

MFX_LRA_0 - MFX LRA 0						
DWord	Bit	Description				
0	31:24	MFX LRA1 Max <table border="1"> <tr> <td>Default Value:</td><td>01111111b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> Maximum value of programmable LRA1.	Default Value:	01111111b	Access:	R/W
Default Value:	01111111b					
Access:	R/W					
23:16	MFX LRA1 Min <table border="1"> <tr> <td>Default Value:</td><td>01000000b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> Minimum value of programmable LRA1.	Default Value:	01000000b	Access:	R/W	
Default Value:	01000000b					
Access:	R/W					
15:8	MFX LRA0 Max <table border="1"> <tr> <td>Default Value:</td><td>00111111b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> Maximum value of programmable LRA0.	Default Value:	00111111b	Access:	R/W	
Default Value:	00111111b					
Access:	R/W					
7:0	MFX LRA0 Min <table border="1"> <tr> <td>Default Value:</td><td>00000000b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> Minimum value of programmable LRA0.	Default Value:	00000000b	Access:	R/W	
Default Value:	00000000b					
Access:	R/W					

MFX LRA 1

MFX_LRA_1 - MFX LRA 1						
DWord	Bit	Description				
0	31:24	<p>MFX LRA3 Max</p> <table border="1"> <tr> <td>Default Value:</td><td>11111111b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Maximum value of programmable LRA3.</p>	Default Value:	11111111b	Access:	R/W
Default Value:	11111111b					
Access:	R/W					
23:16	<p>MFX LRA3 Min</p> <table border="1"> <tr> <td>Default Value:</td><td>11000000b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Minimum value of programmable LRA3.</p>	Default Value:	11000000b	Access:	R/W	
Default Value:	11000000b					
Access:	R/W					
15:8	<p>MFX LRA2 Max</p> <table border="1"> <tr> <td>Default Value:</td><td>10111111b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Maximum value of programmable LRA2.</p>	Default Value:	10111111b	Access:	R/W	
Default Value:	10111111b					
Access:	R/W					
7:0	<p>MFX LRA2 Min</p> <table border="1"> <tr> <td>Default Value:</td><td>10000000b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Minimum value of programmable LRA2.</p>	Default Value:	10000000b	Access:	R/W	
Default Value:	10000000b					
Access:	R/W					

MFX LRA 2

MFX_LRA_2 - MFX LRA 2						
DWord	Bit	Description				
0	31:8	Reserved <table border="1"> <tr> <td>Default Value:</td><td>000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	000000h	Access:	RO
Default Value:	000000h					
Access:	RO					
7:6	VCS LRA <table border="1"> <tr> <td>Default Value:</td><td>00b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Which LRA should VCS use.</p>	Default Value:	00b	Access:	R/W	
Default Value:	00b					
Access:	R/W					
5:4	VMX LRA <table border="1"> <tr> <td>Default Value:</td><td>01b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Which LRA should VMX use.</p>	Default Value:	01b	Access:	R/W	
Default Value:	01b					
Access:	R/W					
3:2	VMC LRA <table border="1"> <tr> <td>Default Value:</td><td>10b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Which LRA should VMC use.</p>	Default Value:	10b	Access:	R/W	
Default Value:	10b					
Access:	R/W					
1:0	VCR LRA <table border="1"> <tr> <td>Default Value:</td><td>11b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Which LRA should VCRSL1 use.</p>	Default Value:	11b	Access:	R/W	
Default Value:	11b					
Access:	R/W					

MFX LRA SL1 0

MFX_LRA_SL1_0 - MFX LRA SL1 0						
DWord	Bit	Description				
0	31:24	<p>MFX SL1 LRA1 Max</p> <table border="1"> <tr> <td>Default Value:</td><td>01111111b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Maximum value of programmable LRA1.</p>	Default Value:	01111111b	Access:	R/W
Default Value:	01111111b					
Access:	R/W					
23:16	<p>MFX SL1 LRA1 Min</p> <table border="1"> <tr> <td>Default Value:</td><td>01000000b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Minimum value of programmable LRA1.</p>	Default Value:	01000000b	Access:	R/W	
Default Value:	01000000b					
Access:	R/W					
15:8	<p>MFX SL1 LRA0 Max</p> <table border="1"> <tr> <td>Default Value:</td><td>00111111b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Maximum value of programmable LRA0.</p>	Default Value:	00111111b	Access:	R/W	
Default Value:	00111111b					
Access:	R/W					
7:0	<p>MFX SL1 LRA0 Min</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Minimum value of programmable LRA0.</p>	Default Value:	00000000b	Access:	R/W	
Default Value:	00000000b					
Access:	R/W					

MFX LRA SL1 1

MFX_LRA_SL1_1 - MFX LRA SL1 1						
DWord	Bit	Description				
0	31:24	MFX SL1 LRA3 Max <table border="1"> <tr> <td>Default Value:</td><td>11111111b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> Maximum value of programmable LRA3.	Default Value:	11111111b	Access:	R/W
Default Value:	11111111b					
Access:	R/W					
23:16	MFX SL1 LRA3 Min <table border="1"> <tr> <td>Default Value:</td><td>11000000b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> Minimum value of programmable LRA3.	Default Value:	11000000b	Access:	R/W	
Default Value:	11000000b					
Access:	R/W					
15:8	MFX SL1 LRA2 Max <table border="1"> <tr> <td>Default Value:</td><td>10111111b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> Maximum value of programmable LRA2.	Default Value:	10111111b	Access:	R/W	
Default Value:	10111111b					
Access:	R/W					
7:0	MFX SL1 LRA2 Min <table border="1"> <tr> <td>Default Value:</td><td>10000000b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> Minimum value of programmable LRA2.	Default Value:	10000000b	Access:	R/W	
Default Value:	10000000b					
Access:	R/W					

MFX LRA SL1 2

MFX_LRA_SL1_2 - MFX LRA SL1 2						
DWord	Bit	Description				
0	31:8	Reserved <table border="1"> <tr> <td>Default Value:</td><td>000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	000000h	Access:	RO
Default Value:	000000h					
Access:	RO					
	7:6	VCSSL1 LRA <table border="1"> <tr> <td>Default Value:</td><td>00b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> Which LRA should VCSSL1 use.	Default Value:	00b	Access:	R/W
Default Value:	00b					
Access:	R/W					
	5:4	VMXSL1 LRA <table border="1"> <tr> <td>Default Value:</td><td>01b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> Which LRA should VMXSL1 use.	Default Value:	01b	Access:	R/W
Default Value:	01b					
Access:	R/W					
	3:2	VMCSL1 LRA <table border="1"> <tr> <td>Default Value:</td><td>10b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> Which LRA should VMCSL1 use.	Default Value:	10b	Access:	R/W
Default Value:	10b					
Access:	R/W					
	1:0	VCRSL1 LRA <table border="1"> <tr> <td>Default Value:</td><td>11b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> Which LRA should VCRSL1 use.	Default Value:	11b	Access:	R/W
Default Value:	11b					
Access:	R/W					

MFX Memory Latency Count2

MFX_LAT_CT2 - MFX Memory Latency Count2		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Source:	VideoCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	12874h	
Valid Projects:	[BDW]	
Address:	1C874h	
Valid Projects:	[BDW:GT3]	
This register stores the accumulative memory latency count on reference picture read requests. This register is not part of hardware context save and restore.		
DWord	Bit	Description
0	31:26	Reserved
		Format: MBZ
	25:0	MFX Reference picture read request - Accumulative Memory Latency Count for the entire frame in 8xMedia clock cycles
		The accumulative memory latency count of all reference reads requested by motion compensative engine per frame. This number is used with MFX Frame Motion Comp Read Count to derive average memory latency.

MFX Memory Latency Count3

MFX_LAT_CT3 - MFX Memory Latency Count3		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Source:	VideoCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	12878h	
Valid Projects:	[BDW]	
Address:	1C878h	
Valid Projects:	[BDW:GT3]	
<p>This register stores the max and min memory latency counts reported on row-stored/bit-stream read requests. Max and current requests into memory sub-system engine. This register is not part of hardware context save and restore.</p>		
DWord	Bit	Description
0	31:24	Max Request Count This field indicates the maximum number of requests allowed by the memory sub-system channel.
	23:16	Current Request Count This field indicates the number of requests currently outstanding in the memory sub-system. This field should report with a value of zero at the end of frame; otherwise the pre-fetch engine most likely hung waiting for read data to be returned from sub-system.
	15:8	MFX row-stored/bit-stream read request - Max Latency Count in 8xMedia clock cycles This field reports the maximum memory latency count on all row-stored/bit-stream reads requested by the memory pre-fetch engine.
	7:0	MFX row-stored/bit-stream read request - Min Latency Count in 8xMedia clock cycles This field reports the minimum memory latency count on all row-stored/bit-stream reads requested by the memory pre-fetch engine.

MFX Memory Latency Count4

MFX_LAT_CT4 - MFX Memory Latency Count4		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Source:	VideoCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	1287Ch	
Valid Projects:	[BDW]	
Address:	1C87Ch	
Valid Projects:	[BDW:GT3]	
This register stores the accumulative memory latency count on row-stored/bit-stream read requests. This register is not part of hardware context save and restore.		
DWord	Bit	Description
0	31:26	Reserved
	25:0	MFX row-stored/bit-stream read request - Accumulative Memory Latency Count for the entire frame in 8xMedia clock cycles The accumulative memory latency count of all row-stored/bit-stream reads requested by prefetch engine per frame. This number is used with Frame row-stored/bit-stream memory read count to derive average memory latency.

MFX Pipeline Status Flags

MFX_STATUS_FLAGS - MFX Pipeline Status Flags								
Register Space:	MMIO: 0/2/0							
Project:	BDW							
Source:	VideoCS							
Default Value:	0x00000000							
Access:	RO							
Size (in bits):	32							
Trusted Type:	1							
Address:	12838h							
Valid Projects:	[BDW]							
Address:	1C838h							
Valid Projects:	[BDW:GT3]							
This register stores the various pipeline status flags. This register is not part of hardware context save and restore.								
DWord	Bit	Description						
0	31:17	Reserved						
		Format: MBZ						
	16	MFX Active Frame decoding/encoding is in progress. Set on frame_start; clear on frame_end.						
	15:10	Reserved						
		Format: MBZ						
	9	Streamout Enable						
	8	Reserved						
	7	Post Deblocking Mode Enable						
	6	Pre Deblocking Mode Enable						
	5	Decoder Mode Select						
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0</td><td>Configure the MFD Engine for VLD Mode</td></tr> <tr> <td>1</td><td>Configure the MFD Engine for IT Mode</td></tr> </tbody> </table>	Value	Name	0	Configure the MFD Engine for VLD Mode	1	Configure the MFD Engine for IT Mode
Value	Name							
0	Configure the MFD Engine for VLD Mode							
1	Configure the MFD Engine for IT Mode							
	4	Codec Select						
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0</td><td>Decode</td></tr> <tr> <td>1</td><td>Encode</td></tr> </tbody> </table>	Value	Name	0	Decode	1	Encode
Value	Name							
0	Decode							
1	Encode							

MFX_STATUS_FLAGS - MFX Pipeline Status Flags

	3:2	Video Mode										
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>MPEG2</td> </tr> <tr> <td>01b</td> <td>VC1</td> </tr> <tr> <td>10b</td> <td>AVC</td> </tr> <tr> <td>11b</td> <td>JPEG</td> </tr> </tbody> </table>	Value	Name	00b	MPEG2	01b	VC1	10b	AVC	11b	JPEG
Value	Name											
00b	MPEG2											
01b	VC1											
10b	AVC											
11b	JPEG											
	1	Decoder Short Format Mode										
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td></td> <td>AVC/VC1 Short Format Mode is in use</td> </tr> <tr> <td>1</td> <td></td> <td>AVC/VC1 Long Format Mode is in use</td> </tr> </tbody> </table>	Value	Name	Description	0		AVC/VC1 Short Format Mode is in use	1		AVC/VC1 Long Format Mode is in use	
Value	Name	Description										
0		AVC/VC1 Short Format Mode is in use										
1		AVC/VC1 Long Format Mode is in use										
	0	Stitch Mode										
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td></td> <td>Not in Stitch Mode</td> </tr> <tr> <td>1b</td> <td></td> <td>In the Special Stitch Mode</td> </tr> </tbody> </table>	Value	Name	Description	0b		Not in Stitch Mode	1b		In the Special Stitch Mode	
Value	Name	Description										
0b		Not in Stitch Mode										
1b		In the Special Stitch Mode										

MFX Slice Performance Count

MFX_SLICE_PERFORM_CT - MFX Slice Performance Count		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Source:	VideoCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	12864h	
Valid Projects:	[BDW]	
Address:	1C864h	
Valid Projects:	[BDW:GT3]	
This register stores the number of clock cycles spent decoding/encoding the current slice. This register is not part of hardware context save and restore.		
DWord	Bit	Description
0	31:0	MFX Frame Performance Count Total number of clocks between slice start and slice end. This count is incremented on crm_clk

MGSR2GAM Message Register

MGSR2GAM_MSGREG - MGSR2GAM Message Register						
DWord	Bit	Description				
0	31:16	Mask Bits <table border="1"> <tr> <td>Default Value:</td><td>0000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Mask Bits act as Write Enables for the bits[15:0] of this register.</p>	Default Value:	0000h	Access:	RO
Default Value:	0000h					
Access:	RO					
	15	MGSR2GAM Message Register 15 <table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>For Future Use. This bit is self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
	14	MGSR2GAM Message Register 14 <table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>For Future Use. This bit is self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
	13	MGSR2GAM Message Register 13 <table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>For Future Use. This bit is self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
	12	MGSR2GAM Message Register 12 <table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>For Future Use. This bit is self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					

MGSR2GAM_MSGREG - MGSR2GAM Message Register

	11	MGSR2GAM Message Register 11				
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>For Future Use. This bit is self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
	10	MGSR2GAM Message Register 10				
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>For Future Use. This bit is self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
	9	MGSR2GAM Message Register 9				
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>For Future Use. This bit is self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
	8	MGSR2GAM Message Register 8				
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>For Future Use. This bit is self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
	7	MGSR2GAM Message Register 7				
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>For Future Use. This bit is self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
	6	MGSR2GAM Message Register 6				
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>For Future Use. This bit is self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
	5	MGSR2GAM Message Register 5				
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>For Future Use. This bit is self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					

MGSR2GAM_MSGREG - MGSR2GAM Message Register

	4	MGSR2GAM Message Register 4				
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>For Future Use. This bit is self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
	3	MGSR2GAM Message Register 3				
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>For Future Use. This bit is self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
	2	MGSR2GAM Message Register 2				
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>For Future Use. This bit is self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
	1	MGSR2GAM Message Register 1				
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>For Future Use. This bit is self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
	0	MGSR2GAM Message Register 0				
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Bit0 - Tail Update Ack Message. This bit is self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					

MGSR Control Register 1

SHADOWREG1 - MGSR Control Register 1

Register Space: MMIO: 0/2/0
 Project: BDW
 0x00000002 [BDW]
 Size (in bits): 32

Address: 00E04h-00E07h

DWord	Bit	Description	
0	31:16	Mask Bits	Access: RO Mask bits applied to [15:0] of same register. If mask is set to 1, corresponding bit in [15:0] is written. If mask is set to 0, corresponding bit in [15:0] is unaffected.
	15:9	Reserved	Access: RO
	8	Force Wake	Default Value: 0b Access: R/WC block GT wakeup
	7:2	Reserved	Project: BDW Access: RO
	1	RC6 model	Default Value: 1b Access: R/WC Set RC6 mode (1) or CPD(0)
	0	GT unblock	Default Value: 0b Access: R/WC GT unblock (1) or block (0)

Minimum Grant

MINGNT_0_2_0_PCI - Minimum Grant						
Register Space: PCI: 0/2/0						
Project: BDW						
Default Value: 0x00000000						
Size (in bits): 8						
Address: 0003Eh						
The Integrated Graphics Device has no requirement for the settings of Latency Timers.						
DWord	Bit	Description				
0	7:0	Minimum Grant Value <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Default Value:</td><td style="padding: 2px;">00000000b</td></tr> <tr> <td style="padding: 2px;">Access:</td><td style="padding: 2px;">RO</td></tr> </table> <p>Hardwired to 0s because the IGD does not burst as a PCI compliant master.</p>	Default Value:	00000000b	Access:	RO
Default Value:	00000000b					
Access:	RO					

Mirror for ARAT LSB

MIRROR_ARAT_LSB - MirrorforARATLSB				
Register Space: MMIO: 0/2/0				
Project: BDW				
Default Value: 0x00000000				
Size (in bits): 32				
Address: 0A530h				
DWord	Bit	Description		
0	31:0	<p>Mirror ARAT LSB Values</p> <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Mirrors arat[31:0], except during context restore when restored value needs to be captured.</p>	Access:	R/W
Access:	R/W			

Mirror for ARAT MSB and ARAT Armed Status

MIRROR_ARAT_MSB - Mirror for ARAT MSB and ARAT Armed Status						
DWord	Bit	Description				
0	31	Mirror ARAT Armed Status <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> Mirrors arat_armed, except during context restore when restored value needs to be captured.	Project:	BDW	Access:	R/W
Project:	BDW					
Access:	R/W					
23:0	Mirror ARAT MSB Values <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> Mirrors arat[55:32], except during context restore when restored value needs to be captured.	Access:	R/W			
Access:	R/W					

Mirror of Base Data of Stolen Memory

BDSM_0_2_0_PCI - Mirror of Base Data of Stolen Memory				
Register Space: PCI: 0/2/0				
Project: BDW				
Default Value: 0x00000000				
Size (in bits): 32				
Address: 0005Ch				
This register contains the base address of graphics data stolen DRAM memory.				
DWord	Bit	Description		
0	31:20	Graphics Base of Stolen Memory		
		<table border="1"> <tr> <td>Default Value:</td><td>0000000000000b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>This register contains bits 31 to 20 of the base address of stolen DRAM memory. BIOS determines the base of graphics stolen memory by subtracting the graphics stolen memory size from TOLUD.</p>	Default Value:	0000000000000b
Default Value:	0000000000000b			
Access:	RO			
<table border="1"> <tr> <td>19:1</td><td>Reserved</td></tr> <tr> <td></td><td>Format: MBZ</td></tr> </table>	19:1	Reserved		Format: MBZ
19:1	Reserved			
	Format: MBZ			
	0	Lock		
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>This bit will lock all writeable settings in this register, including itself.</p>	Default Value:	0b
Default Value:	0b			
Access:	RO			

Mirror of Capabilities A

CAPID0_A_0_2_0_PCI - Mirror of Capabilities A		
DWord	Bit	Description
0	31	Display HD Audio Disable Default Value: 0b Access: RO 0: Display HD Audio Enabled 1: Display HD Audio Disabled
	30	PEG12 Disable Default Value: 0b Access: RO
	29	PEG11 Disable Default Value: 0b Access: RO
	28	PEG10 Disable Default Value: 0b Access: RO
	27	PCI Express Link Width Upconfig Disable Default Value: 0b Access: RO
	26	DMI Width Default Value: 0b Access: RO
	25	ECC Disable Default Value: 0b Access: RO
	24	Force DRAM ECC Enabled Default Value: 0b Access: RO

CAPID0_A_0_2_0_PCI - Mirror of Capabilities A

	23	VTd Disable	Default Value:	0b	
		Access:		RO	
		0: Enable VTd 1: Disable VTd			
	22	DMI Gen 2 Disable	Default Value:	0b	
		Access:		RO	
	21	PEG Gen 2 Disable	Default Value:	0b	
		Access:		RO	
	20:19	DDR Size	Default Value:	00b	
		Access:		RO	
	18	Bclk overclocking disable	Default Value:	0b	
		Access:		RO	
	17	Disable 1N Mode	Default Value:	0b	
		Access:		RO	
	16	Full ULT Fuse Read Disable	Default Value:	0b	
		Access:		RO	
	15	Camarillo Device Disable	Default Value:	0b	
		Access:		RO	
	14	2 DIMMS per Channel Disable	Default Value:	0b	
		Access:		RO	
	13	X2APIC Enabled	Default Value:	0b	
		Access:		RO	
	12	Performance Dual Channel Disable	Default Value:	0b	
		Access:		RO	

CAPID0_A_0_2_0_PCI - Mirror of Capabilities A

	11	Internal Graphics Disable				
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	0b	Access:	RO
Default Value:	0b					
Access:	RO					
		<p>0b: There is a graphics engine within this CPU. Internal Graphics Device (Device 2) is enabled and all of its memory and I/O spaces are accessible. Configuration cycles to Device 2 will be completed within the CPU. All non-SMM memory and IO accesses to VGA will be handled based on Memory and IO enables of Device 2 and IO registers within Device 2 and VGA Enable of the PCI to PCI bridge control (If PCI Express GFX attach is supported). A selected amount of Graphics Memory space is pre-allocated from the main memory based on Graphics Mode Select (GMS in the GGC Register). Graphics Memory is pre-allocated above TSEG Memory. 1b: There is no graphics engine within this CPU. Internal Graphics Device (Device 2) and all of its memory and I/O functions are disabled. Configuration cycle targeted to Device 2 will be passed on. All non-SMM memory and IO accesses to VGA will be handled based on VGA Enable of the PCI to PCI bridge control. Device 2 is disabled and hidden.</p>				
	10	Reserved				
	9:8	Capability Device ID				
		<table border="1"> <tr> <td>Default Value:</td><td>00b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	00b	Access:	RO
Default Value:	00b					
Access:	RO					
	7:4	Compatibility Rev ID				
		<table border="1"> <tr> <td>Default Value:</td><td>0000b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	0000b	Access:	RO
Default Value:	0000b					
Access:	RO					
		This is an 8-bit value that indicates the revision identification number for the Host Device 0.				
	3	DDR Overclocking				
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	0b	Access:	RO
Default Value:	0b					
Access:	RO					
	2	IA Overclocking Enabled by SKU				
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	0b	Access:	RO
Default Value:	0b					
Access:	RO					
	1	DDR Write VRef				
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	0b	Access:	RO
Default Value:	0b					
Access:	RO					
	0	DDR3L Enable				
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	0b	Access:	RO
Default Value:	0b					
Access:	RO					

Mirror of Capabilities B

CAPID0_B_0_2_0_PCI - Mirror of Capabilities B		
DWord	Bit	Description
0	31	SPARE31
		Default Value: 0b
		Access: RO
	30	IA Overclocking DSKU Control Disable
		Default Value: 0b
		Access: RO
	29	IA Overclocking Enable
		Default Value: 0b
		Access: RO
	28	SMT Capability
		Default Value: 0b
		Access: RO
27:25	Cache Size Capability	
	Default Value: 000b	
24	24	SPARE24
		Default Value: 0b
		Access: RO
	23:21	DDR3 Maximum Frequency Capability with 100 Memory
		Default Value: 000b
		Access: RO
	20	Gen3 Disable Fuse for PCIe PEG Controllers
		Default Value: 0b
		Access: RO
19	Package Type	
	Default Value: 0b	
	Access: RO	

CAPID0_B_0_2_0_PCI - Mirror of Capabilities B

	18	Additive Graphics Enabled
		Default Value:
		Access:
0 - Additive Graphics Disabled 1- Additive Graphics Enabled		
	17	Additive Graphics Capable
		Default Value:
		Access:
0 - Capable of Additive Graphics 1 - Not capable of Additive Graphics		
	16	Primary PEG Port x16 Disable
		Default Value:
		Access:
	15:12	SPARE15_12
		Default Value:
		Access:
	11	Reserved
	10:8	SPARE10_8
		Default Value:
		Access:
	7	Reserved
	6:4	DDR3 Maximum Frequency Capability
		Default Value:
		Access:
	3	SPARE3
		Default Value:
		Access:
	2	DDR4 Enable
		Default Value:
		Access:
	1	Dual PEG Force x1 when VGA Enabled
		Default Value:
		Access:
	0	Single PEG Force x1 when VGA Enabled
		Default Value:
		Access:

Mirror of Device Enable

DEVEN0_0_2_0_PCI - Mirror of Device Enable		
DWord	Bit	Description
0	14	Chap Enable
		Default Value:
		Access:
	13:8	Reserved
		Format:
	7	Device 4 Enable
		Default Value:
		Access:
	6	Reserved
		Format:
	5	Device 3 enable for Display HD Audio
		Default Value:
		Access: 0: Bus 0 Device 3 is disabled and hidden 1: Bus 0 Device 3 is enabled and visible
	4	Internal Graphics Engine
		Default Value:
		Access: 0: Bus 0 Device 2 is disabled and hidden 1: Bus 0 Device 2 is enabled and visible This bit will be set to 0b and remain 0b if Device 2 capability is disabled.
	3	PEG10 Enable
		Default Value:
	2	Access:
		PEG11 Enable
		Default Value:
		Access:

DEVENO_0_2_0_PCI - Mirror of Device Enable			
	1	PEG12 Enable	
		Default Value:	1b
	0	Host Bridge	
		Default Value:	1b
		Access:	RO

Mirror of DSMBASE

DSMB - Mirror of DSMBASE			
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x00000000 Size (in bits): 32			
DSM Base			
DWord	Bit	Description	
0	31:20	DSM Base Lower 32 Bits	
		Access:	RO
This register contains bits 31 to 20 of the base address of stolen DRAM memory. BIOS determines the base of graphics stolen memory by subtracting the graphics stolen memory size (PCI Device 0 offset 52 bits 6:4) from TOLUD (PCI Device 0 offset BC bits 31:20).			
	19:0	Spares	
		Access:	RO

Mirror of EMRR Base LSB

EMRRBASE_LSB - Mirror of EMRR Base LSB						
Mirror of EMRR Base						
DWord	Bit	Description				
0	31:12	<p>EMRR Base LSB</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>EMRR Base Value.</td> <td></td> </tr> </table>	Access:	RO	EMRR Base Value.	
Access:	RO					
EMRR Base Value.						
11:0	<p>Spares</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO			
Access:	RO					

Mirror of EMRR Base MSB

EMRRBASE_MSB - Mirror of EMRR Base MSB				
Register Space:	MMIO: 0/2/0			
Project:	BDW			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	09204h			
Mirror of EMRR Base				
DWord	Bit	Description		
0	31:7	<p>Spares</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
Access:	RO			
6:0	<p>EMRR Base MSB</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>EMRR Base Value.</p>	Access:	RO	
Access:	RO			

Mirror of EU Disable Fuses - Register0

MIRROR_EU_DISABLE0 - Mirror of EU Disable Fuses - Register0						
DWord	Bit	Description				
0	31:0	<p>EU Disable Fuses</p> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Slice0 - Subslice0 = Register0[7:0] Slice0 - Subslice1 = Register0[15:8] Slice0 - Subslice2 = Register0[23:16] Slice1 - Subslice0 = Register0[31:24] Slice1 - Subslice1 = Register1[7:0] Slice1 - Subslice2 = Register1[15:8] Slice2 - Subslice0 = Register1[23:16] Slice2 - Subslice1 = Register1[31:24] Slice2 - Subslice2 = Register2[7:0]</p>	Project:	BDW	Access:	RO
Project:	BDW					
Access:	RO					

Mirror of EU Disable Fuses - Register1

MIRROR_EU_DISABLE1 - Mirror of EU DisableFuses-Register1						
DWord	Bit	Description				
0	31:0	<p>EU Disable Fuses</p> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Slice0 - Subslice0 = Register0[7:0] Slice0 - Subslice1 = Register0[15:8] Slice0 - Subslice2 = Register0[23:16] Slice1 - Subslice0 = Register0[31:24] Slice1 - Subslice1 = Register1[7:0] Slice1 - Subslice2 = Register1[15:8] Slice2 - Subslice0 = Register1[23:16] Slice2 - Subslice1 = Register1[31:24] Slice2 - Subslice2 = Register2[7:0]</p>	Project:	BDW	Access:	RO
Project:	BDW					
Access:	RO					

Mirror of EU Disable Fuses - Register2

MIRROR_EU_DISABLE2 - Mirror of EU Disable Fuses - Register2						
DWord	Bit	Description				
0	31:8	Spare <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Project:	BDW	Access:	RO
Project:	BDW					
Access:	RO					
7:0	EU Disable Fuses <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p> Slice0 - Subslice0 = Register0[7:0] Slice0 - Subslice1 = Register0[15:8] Slice0 - Subslice2 = Register0[23:16] Slice1 - Subslice0 = Register0[31:24] Slice1 - Subslice1 = Register1[7:0] Slice1 - Subslice2 = Register1[15:8] Slice2 - Subslice0 = Register1[23:16] Slice2 - Subslice1 = Register1[31:24] Slice2 - Subslice2 = Register2[7:0] </p>	Project:	BDW	Access:	RO	
Project:	BDW					
Access:	RO					

Mirror of FUSE1 Control DW

FUSE1 - Mirror of FUSE1 Control DW		
DWord	Bit	Description
0	31:19	Spares Project: BDW Access: RO
	18	Reserved
	17:16	Spares1 Access: RO
	15	Authentication Bypass Access: RO
	14	Reserved
	13	Spares2 Access: RO
	12	Reserved
	11	Render Disable Access: RO
	10:9	Spares3 Access: RO
	8	VME IME Enable Access: RO
	7	VME CRE Enable Access: RO
	6:5	Media Decode Access: RO Applicable to Media - Fuse to disable VIN from processing media_objs or turn off the entire crclk tree trunk.
	4	Disable GT3 Slice Shutdown Access: RO N/A -- Not used by GT hardware: This fuse is actually enforced by the PCU; it is reflected here for driver information only.

FUSE1 - Mirror of FUSE1 Control DW

	3	Reserved	
	2	Spares4	Access: RO
	1:0	Media Encode	Access: RO Applicable to Media - One fuse to disable VIN from processing Pak_obj. Second fuse to disable VME.

Mirror of FUSE2 Control DW

FUSE2 - Mirror of FUSE2 Control DW						
DWord	Bit	Description				
0	31:29	<p>GT SKU Fuse</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>GT SKU Fuse Bits See project specific configuration table for possible values.</p>	Access:	RO		
Access:	RO					
	28	<p>Spares</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO		
Access:	RO					
	27:25	<p>GT Slice Enable Fuse</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Slice Enables Bit25 - Slice0 Enable Bit26 - Slice1 Enable Bit27 - Slice2 Enable See project specific configuration table for possible values.</p>	Access:	RO		
Access:	RO					
	24	<p>Spares1</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO		
Access:	RO					
	23:21	<p>GT Subslice Disable Fuse</p> <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Subslice Disable: 000b = All subslices enabled (GT2/3/4) 001b = Subslice 0 disabled (GT1) 010b = Subslice 1 disabled (GT1) 100b = Subslice 2 disabled (GT1) 110b = Subslice 1 and 2 disabled (Emulation Only)</p>	Project:	BDW	Access:	RO
Project:	BDW					
Access:	RO					
	20	<p>Spares2</p> <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Project:	BDW	Access:	RO
Project:	BDW					
Access:	RO					

FUSE2 - Mirror of FUSE2 Control DW

	19:18	GT VDBox and VEBox Configuration Fuse
		Access: RO VDBox and VEbox Configurations: 00b = Both VDBOXes and VBOXEs enabled 01b = VDBOX1 and VBOX1 enabled (GT1,2) 10b = VDBOX0 and VBOX0 enabled (GT1,2) See project specific configuration table for possible values.
	17:16	Spares3
		Access: RO
	15:0	Cabability Fuse
		Access: RO

Mirror of Global Command Register

GCMD - Mirror of Global Command Register

Register Space: MMIO: 0/2/0

Project: BDW

Default Value: 0x00000000

Size (in bits): 32

Address: 090CCh

DWord	Bit	Description		
0	31	<p>Translation Enable</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Software writes to this field to request hardware to enable/disable DMA-remapping hardware. 0: Disable DMA-remapping hardware. 1: Enable DMA-remapping hardware.</p> <p>Hardware reports the status of the translation enable operation through the TES field in the Global Status register.</p> <p>Before enabling (or re-enabling) DMA-remapping hardware through this field, software must:</p> <ul style="list-style-type: none"> • Setup the DMA-remapping structures in memory. • Flush the write buffers (through WBF field), if write buffer flushing is reported as required. • Set the root-entry table pointer in hardware (through SRTP field). • Perform global invalidation of the context-cache and global invalidation of IOTLB • If advanced fault logging supported, setup fault log pointer (through SFL field) and enable advanced fault logging (through EAFL field). <p>Refer to Section 9 for detailed software requirements.</p> <p>There may be active DMA requests in the platform when software updates this field. Hardware must enable or disable remapping logic only at deterministic transaction boundaries, so that any in-flight transaction is either subject to remapping or not at all.</p> <p>Hardware implementations supporting DMA draining must drain any in-flight translated DMA read/write requests queued within the root complex before completing the translation enable command and reflecting the status of the command through the TES field in the GSTS_REG.</p> <p>Value returned on read of this field is undefined.</p>	Access:	RO
Access:	RO			
	30	<p>Set Root Table Pointer</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Software sets this field to set/update the root-entry table pointer used by hardware. The root-entry table pointer is specified through the Root-entry Table Address register.</p> <p>Hardware reports the status of the "root table pointer set" operation through the RTPS field in the Global Status register.</p> <p>The root table pointer set operation must be performed before enabling or re-enabling (after disabling) DMA remapping through the TE field.</p> <p>After a "root table pointer set" operation, software must globally invalidate the context cache and then globally invalidate the IOTLB. This is required to ensure hardware uses only the remapping structures referenced by the new root table pointer, and not any stale cached entries.</p>	Access:	RO
Access:	RO			

GCMD - Mirror of Global Command Register				
		While DMA remapping is active, software may update the root table pointer through this field. However, to ensure valid in-flight DMA requests are deterministically remapped, software must ensure that the structures referenced by the new root table pointer are programmed to provide the same remapping results as the structures referenced by the previous root-table pointer. Clearing this bit has no effect. The value returned on a read of this field is undefined.		
29	Set Fault Log	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td><td style="padding: 2px; text-align: right;">RO</td></tr> </table> <p>This field is valid only for implementations supporting advanced fault logging. Software sets this field to request hardware to set/update the fault-log pointer used by hardware. The fault-log pointer is specified through Advanced Fault Log register. Hardware reports the status of the fault log set operation through the FLS field in the Global Status register. The fault log pointer must be set before enabling advanced fault logging (through EAFL field). Once advanced fault logging is enabled, the fault log pointer may be updated through this field while DMA remapping is active. Clearing this bit has no effect. The value returned on read of this field is undefined.</p>	Access:	RO
Access:	RO			
28	Enable Fault Logging	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td><td style="padding: 2px; text-align: right;">RO</td></tr> </table> <p>This field is valid only for implementations supporting advanced fault logging. Software writes to this field to request hardware to enable or disable advanced fault logging. 0: Disable advanced fault logging. In this case, translation faults are reported through the Fault Recording registers. 1: Enable use of memory-resident fault log. When enabled, translation faults are recorded in the memory-resident log. The fault log pointer must be set in hardware (through SFL field) before enabling advanced fault logging. Hardware reports the status of the advanced fault logging enable operation through the AFLS field in the Global Status register. Value returned on read of this field is undefined.</p>	Access:	RO
Access:	RO			
27	Write Buffer Flush	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td><td style="padding: 2px; text-align: right;">RO</td></tr> </table> <p>This bit is valid only for implementations requiring write buffer flushing. Software sets this field to request hardware to flush the root-complex internal write buffers. This is done to ensure any updates to the memory-resident remapping structures are not held in any internal write posting buffers. Refer to Section 11.1 for details on write-buffer flushing requirements. Hardware reports the status of the write buffer flushing operation through the WBFS field in the Global Status register. Clearing this bit has no effect. Value returned on read of this field is undefined.</p>	Access:	RO
Access:	RO			

GCMD - Mirror of Global Command Register

26	Queued Invalidations Enable			
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px; text-align: right;">RO</td> </tr> </table>	Access:	RO	
Access:	RO			
	<p>This field is valid only for implementations supporting queued invalidations.</p> <p>Software writes to this field to enable or disable queued invalidations.</p> <p>0: Disable queued invalidations.</p> <p>1: Enable use of queued invalidations.</p> <p>Hardware reports the status of queued invalidation enable operation through QIES field in the Global Status register.</p> <p>Refer to Section 6.2.2 for software requirements for enabling/disabling queued invalidations.</p> <p>The value returned on a read of this field is undefined.</p>			
25	Interrupt Remapping Enable			
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px; text-align: right;">RO</td> </tr> </table>	Access:	RO	
Access:	RO			
	<p>This field is valid only for implementations supporting interrupt remapping.</p> <p>0: Disable interrupt-remapping hardware</p> <p>1: Enable interrupt-remapping hardware</p> <p>Hardware reports the status of the interrupt remapping enable operation through the IRES field in the Global Status register.</p> <p>There may be active interrupt requests in the platform when software updates this field. Hardware must enable or disable interrupt-remapping logic only at deterministic transaction boundaries, so that any in-flight interrupts are either subject to remapping or not at all.</p> <p>Hardware implementations must drain any in-flight interrupt requests queued in the Root-Complex before completing the interrupt-remapping enable command and reflecting the status of the command through the IRES field in the Global Status register.</p> <p>The value returned on a read of this field is undefined.</p>			
24	Set Interrupt Remap Table Pointer			
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px; text-align: right;">RO</td> </tr> </table>	Access:	RO	
Access:	RO			
	<p>This field is valid only for implementations supporting interrupt-remapping.</p> <p>Software sets this field to set/update the interrupt remapping table pointer used by hardware. The interrupt remapping table pointer is specified through the Interrupt Remapping Table Address register.</p> <p>Hardware reports the status of the interrupt remapping table pointer set operation through the IRTPS field in the Global Status register.</p> <p>The interrupt remap table pointer set operation must be performed before enabling or re-enabling (after disabling) interrupt-remapping hardware through the IRE field.</p> <p>After an interrupt remap table pointer set operation, software must globally invalidate the interrupt entry cache. This is required to ensure hardware uses only the interrupt-remapping entries referenced by the new interrupt remap table pointer, and not any stale cached entries.</p> <p>While interrupt remapping is active, software may update the interrupt remapping table pointer through this field. However, to ensure valid in-flight interrupt requests are deterministically remapped, software must ensure that the structures referenced by the new interrupt remap table pointer are programmed to provide the same remapping results as the structures referenced by the previous interrupt remap table pointer.</p> <p>Clearing this bit has no effect. The value returned on a read of this field is undefined.</p>			

GCMD - Mirror of Global Command Register

	23	Compatibility Format Interrupt	
		Access:	RO
<p>This field is valid only for Intel(R)64 implementations supporting interrupt-remapping. Software writes to this field to enable or disable Compatibility Format interrupts on Intel(R)64 platforms. The value in this field is effective only when interrupt-remapping is enabled and Legacy Interrupt Mode is active.</p> <p>0: Block Compatibility format interrupts.</p> <p>1: Process Compatibility format interrupts as pass-through (bypass interrupt remapping). Hardware reports the status of updating this field through the CFIS field in the Global Status register.</p> <p>Refer to Section 5.4.1 for details on Compatibility Format interrupt requests.</p> <p>The value returned on a read of this field is undefined.</p> <p>This field is not implemented on Itanium(TM) implementations.</p>			
	22:0	Spares	
		Access:	RO

Mirror of GMCH Graphics Control

MGGC0_0_2_0_PCI - Mirror of GMCH Graphics Control						
DWord	Bit	Description				
0	15:8	<p>Graphics Mode Select</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000101b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics device in VGA (non-linear) and Native (linear) modes. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled. Hardware does not clear or set any of these bits automatically based on IGD being disabled/enabled. BIOS Requirement: BIOS must not set this field to 0h if IVD (bit 1 of this register) is 0. 00h:0MB 01h:32MB 02h:64MB 03h:96MB 04h:128MB 05h:160MB (default) 06h:192MB 07h:224MB 08h:256MB 09h:288MB 0Ah:320MB 0Bh:352MB 0Ch:384MB 0Dh:416MB 0Eh:448MB 0Fh:480MB 10h:512MB 11h - 1Fh: Reserved 20h:1024MB 21h - 2Fh: Reserved 30h:1536MB 31h - 3Eh: Reserved 3Fh: 2016MB 40h - FFh: Reserved Hardware functionality in case of programming this value to Reserved is not guaranteed.</p>	Default Value:	00000101b	Access:	RO
Default Value:	00000101b					
Access:	RO					

MGGC0_0_2_0_PCI - Mirror of GMCH Graphics Control

	7:6	GTT Graphics Memory Size				
		<table border="1"> <tr> <td>Default Value:</td><td>00b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	00b	Access:	RO
Default Value:	00b					
Access:	RO					
		<p>This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics Translation Table. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled. GSM is assumed to be a contiguous physical DRAM space with DSM, and BIOS needs to allocate a contiguous memory chunk. Hardware will derive the base of GSM from DSM only using the GSM size programmed in the register. Hardware functionality in case of programming this value to Reserved is not guaranteed.</p> <p>0x0: No Preallocated Memory 0x1: 2MB of Preallocated Memory 0x2: 4MB of Preallocated Memory 0x3: 8MB of Preallocated Memory</p>				
	5:3	Reserved				
		<table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ		
Format:	MBZ					
	2	Versatile Acceleration Mode Enable				
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	0b	Access:	RO
Default Value:	0b					
Access:	RO					
		<p>Enables the use of the iGFX engines for Versatile Acceleration.</p> <p>1 - iGFX engines are in Versatile Acceleration Mode. Device 2 Class Code is 048000h. 0 - iGFX engines are in iGFX Mode. Device 2 Class Code is 030000h.</p>				
	1	IGD VGA Disable				
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	0b	Access:	RO
Default Value:	0b					
Access:	RO					
		<p>0: Enable. Device 2 (IGD) claims VGA memory and IO cycles, the Sub-Class Code within Device 2 Class Code register is 00.</p> <p>1: Disable. Device 2 (IGD) does not claim VGA cycles (Mem and IO), and the Sub- Class Code field within Device 2 function 0 Class Code register is 80.</p> <p>BIOS Requirement: BIOS must not set this bit to 0 if the GMS field pre-allocates no memory. This bit MUST be set to 1 if Device 2 is disabled either via a fuse or fuse override (CAPID0_A[IGD] = 1) or via a register (DEVEN[3] = 0).</p>				
	0	GGC Lock				
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	0b	Access:	RO
Default Value:	0b					
Access:	RO					
		<p>When set to 1b, this bit will lock all bits in this register.</p>				

Mirror of GMCH Graphics Control Register

MGGC - Mirror of GMCH Graphics Control Register

Register Space:	MMIO: 0/2/0			
Project:	BDW			
Default Value:	0x00000300			
Size (in bits):	32			
Address:	09094h			
Mirror of GMCH Graphics Control Register				
DWord	Bit	Description		
0	31:16	Spares		
		<table border="1"> <tr> <td>Access:</td><td>RO</td></tr> </table>	Access:	RO
Access:	RO			
15:8	Graphics Mode Select			
	<table border="1"> <tr> <td>Default Value:</td><td>3h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	3h	Access:
Default Value:	3h			
Access:	RO			
<p>This field selects the amount of Main Memory that is pre-allocated to support the Internal Graphics device in VGA (non-linear) and Native (linear) modes. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled.</p> <p>0h: No memory pre-allocated. Device 2 (IGD) does not claim VGA cycles (Mem and IO), and the Sub-Class Code field within Device 2 function 0 Class Code register is 80.</p> <p>1h-4h: Reserved.</p> <p>5h-Dh: DVMT (UMA) mode, memory pre-allocated for frame buffer, in quantities as shown in the Encoding table.</p> <p>Eh-Fh: Reserved.</p> <p>NOTE: This register is locked and becomes Read Only when the D_LCK bit in the SMRAMC register is set. This register is also LT lockable.</p> <p>Hardware does not clear or set any of these bits automatically based on IGD being disabled/enabled.</p> <p>BIOS Requirement: BIOS must not set this field to 0h if IVD (bit 1 of this register) is 0.</p>				
GTT Graphics Memory Size				
<table border="1"> <tr> <td>Access:</td><td>RO</td></tr> </table>	Access:	RO		
Access:	RO			
<p>This field selects the amount of Main Memory that is pre-allocated to support the Internal Graphics Translation Table. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled.</p> <p>GSM is assumed to be a contiguous physical DRAM space with DSM, and BIOS needs to allocate a contiguous memory chunk. Hardware derives the base of GSM from DSM only using the GSM size programmed in the register.</p> <p>0h: No memory pre-allocated. GTT cycles (Mem and IO) are not claimed.</p> <p>1h: 2 MB of memory pre-allocated for GTT.</p> <p>2h: 4 MB of memory pre-allocated for GTT.</p> <p>3h: 8 MB of memory pre-allocated for GTT.</p> <p>Hardware functionality in case of programming this value to Reserved is not guaranteed.</p>				

MGGC - Mirror of GMCH Graphics Control Register

		This register is locked and becomes Read Only when the D_LCK bit in the SMRAMC register is set.		
5:3	Spares2	<table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
Access:	RO			
2	Versatile Acceleration Mode Enable	<table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Enables the use of the iGFX engines for Versatile Acceleration. 1 - iGFX engines are in Versatile Acceleration Mode. Device 2 Class Code is 048000h. 0 - iGFX engines are in iGFX Mode. Device 2 Class Code is 030000h.</p>	Access:	RO
Access:	RO			
1	IGD VGA Disable	<table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>0: Enable. Device 2 (IGD) claims VGA memory and IO cycles, the Sub-Class Code within Device 2 Class Code register is 00. 1: Disable. Device 2 (IGD) does not claim VGA cycles (Mem and IO), and the Sub-Class Code field within Device 2 function 0 Class Code register is 80. BIOS Requirement: BIOS must not set this bit to 0 if the GMS field (bits 6:4 of this register) pre-allocates no memory. This bit MUST be set to 1 if Device 2 is disabled either via a fuse or fuse override (CAPID0[46] = 1) or via a register (DEVEN[3] = 0). This register is locked by LT lock.</p>	Access:	RO
Access:	RO			
0	Spares3	<table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
Access:	RO			

Mirror of Graphics Translation Table and Memory Mapped Range Address

GTTMMADR LSB - Mirror of Graphics Translation Table and Memory Mapped Range Address

Register Space: MMIO: 0/2/0

Project: BDW

Default Value: 0x00000000

Size (in bits): 32

Address: 09124h

This register requests allocation for the combined Graphics Translation Table Modification Range and Memory Mapped Range. The range requires 4 MB combined for MMIO and Global GTT aperture, with 2MB of that used by MMIO and 2MB used by GTT. GTTADR begins at (GTTMMADR + 2 MB) while the MMIO base address is the same as GTTMMADR.

For the Global GTT, this range is defined as a memory BAR in graphics device config space. It is an alias into which software is required to write Page Table Entry values (PTEs). Software may read PTE values from the global Graphics Translation Table (GTT). PTEs cannot be written directly into the global GTT memory area.

The device snoops writes to this region in order to invalidate any cached translations within the various TLBs implemented on-chip. There are some exceptions to this - see GTT-TLB in the Programming Interface chapter. The allocation is for 4MB and the base address is defined by bits [38:22].

DWord	Bit	Description				
0	31:22	<p>Memory Base Address (LSB - 31:22 of 38:22)</p> <table border="1"> <tr> <td>Access:</td><td>RO</td></tr> <tr> <td colspan="2">Set by the OS, these bits correspond to address signals [38:22]. 4MB combined for MMIO and Global GTT table aperture (2MB for MMIO and 2 MB for GTT).</td></tr> </table>	Access:	RO	Set by the OS, these bits correspond to address signals [38:22]. 4MB combined for MMIO and Global GTT table aperture (2MB for MMIO and 2 MB for GTT).	
Access:	RO					
Set by the OS, these bits correspond to address signals [38:22]. 4MB combined for MMIO and Global GTT table aperture (2MB for MMIO and 2 MB for GTT).						
21:4	<p>Spares</p> <table border="1"> <tr> <td>Access:</td><td>RO</td></tr> </table>	Access:	RO			
Access:	RO					
3	<p>Prefetchable Memory</p> <table border="1"> <tr> <td>Access:</td><td>RO</td></tr> <tr> <td colspan="2">Hardwired to 0 to prevent prefetching.</td></tr> </table>	Access:	RO	Hardwired to 0 to prevent prefetching.		
Access:	RO					
Hardwired to 0 to prevent prefetching.						
2:1	<p>Memory Type</p> <table border="1"> <tr> <td>Access:</td><td>RO</td></tr> <tr> <td colspan="2">00b: To indicate 32 bit base address. 01b: Reserved. 10b: To indicate 64 bit base address. 11b: Reserved.</td></tr> </table>	Access:	RO	00b: To indicate 32 bit base address. 01b: Reserved. 10b: To indicate 64 bit base address. 11b: Reserved.		
Access:	RO					
00b: To indicate 32 bit base address. 01b: Reserved. 10b: To indicate 64 bit base address. 11b: Reserved.						
0	<p>Memory I/O Space</p> <table border="1"> <tr> <td>Access:</td><td>RO</td></tr> <tr> <td colspan="2">Hardwired to 0 to indicate memory space.</td></tr> </table>	Access:	RO	Hardwired to 0 to indicate memory space.		
Access:	RO					
Hardwired to 0 to indicate memory space.						

Mirror of Graphics Translation Table and Memory Mapped Range Address UDW

GTTMMADR_MSB - Mirror of Graphics Translation Table and Memory Mapped Range Address UDW				
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x00000000 Size (in bits): 32				
Address: 09128h				
This register requests allocation for the combined Graphics Translation Table Modification Range and Memory Mapped Range. The range requires 4 MB combined for MMIO and Global GTT aperture, with 2MB of that used by MMIO and 2MB used by GTT. GTTADR begins at (GTTMMADR + 2 MB) while the MMIO base address is the same as GTTMMADR. For the Global GTT, this range is defined as a memory BAR in graphics device config space. It is an alias into which software is required to write Page Table Entry values (PTEs). Software may read PTE values from the global Graphics Translation Table (GTT). PTEs cannot be written directly into the global GTT memory area. The device snoops writes to this region in order to invalidate any cached translations within the various TLBs implemented on-chip. There are some exceptions to this - see GTT-TLB in the Programming Interface chapter. The allocation is for 4MB and the base address is defined by bits [38:22].				
DWord	Bit	Description		
0	31:7	Spares <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
Access:	RO			
6:0	Memory Base Address (MSB - 38:32 of 38:22) <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Set by the OS, these bits correspond to address signals [38:22]. 4MB combined for MMIO and Global GTT table aperture (2MB for MMIO and 2 MB for GTT).	Access:	RO	
Access:	RO			

Mirror of GSMBASE

GSMB - Mirror of GSMBASE				
Register Space:	MMIO: 0/2/0			
Project:	BDW			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	090A4h			
<p>This register contains the base address of stolen DRAM memory for the GTT. BIOS determines the base of GTT stolen memory by subtracting the GTT graphics stolen memory size (PCI Device 0 offset 52 bits 11:8) from the Graphics Base of Data Stolen Memory (PCI Device 0 offset B0 bits 31:20).</p>				
DWord	Bit	Description		
0	31:20	GSM Base <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px; text-align: right;">RO</td> </tr> </table> <p>This register contains the base address of stolen DRAM memory for the GTT. BIOS determines the base of GTT stolen memory by subtracting the GTT graphics stolen memory size (PCI Device 0 offset 52 bits 11:8) from the Graphics Base of Data Stolen Memory (PCI Device 0 offset B0 bits 31:23).</p>	Access:	RO
Access:	RO			
19:0	Spares <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px; text-align: right;">RO</td> </tr> </table>	Access:	RO	
Access:	RO			

Mirror of PCICMD MAE/BME

PCICMD - Mirror of PCICMD MAE/BME			
DWord	Bit	Description	
0	31:11	Spare	Access: R/W
	10	Interrupt Disable This bit disables the device from asserting INTx#. 0: Enable the assertion of this device's INTx# signal. 1: Disable the assertion of this device's INTx# signal. DO_INTx messages are not sent to DMI. GSA Implementation: When 1, blocks the sending of an MSI interrupt and blocks the sending of a Line interrupt. (The interrupt status is not blocked from being reflected in the INTSTS bit.) When 0, permits the sending of an MSI interrupt or Line interrupt.	Access: R/W
	9	Fast Back to Back Not Implemented. Hardwired to 0.	Access: R/W
	8	SERR Enable Not Implemented. Hardwired to 0.	Access: R/W
	7	Address/Data Stepping Enable Not Implemented. Hardwired to 0.	Access: R/W
	6	Parity Error Enable Not Implemented. Hardwired to 0. Since the IGD belongs to the category of devices that does not corrupt programs or data in system memory or hard drives, the IGD ignores any parity error that it detects and continues with normal operation.	Access: R/W

PCICMD - Mirror of PCICMD MAE/BME

		Video Pallette Snooping		
	5	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px; text-align: right;">R/W</td> </tr> </table> <p>This bit is hardwired to 0 to disable snooping.</p>	Access:	R/W
Access:	R/W			
	4	Memory Write and Invalidate Enable <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px; text-align: right;">R/W</td> </tr> </table> <p>Hardwired to 0. The IGD does not support memory write and invalidate commands.</p>	Access:	R/W
Access:	R/W			
	3	Special Cycle Enable <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px; text-align: right;">R/W</td> </tr> </table> <p>This bit is hardwired to 0. The IGD ignores Special cycles.</p>	Access:	R/W
Access:	R/W			
	2	Bus Master Enable <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px; text-align: right;">R/W</td> </tr> </table> <p>0: Disable IGD bus mastering. 1: Enable the IGD to function as a PCI compliant master. GSA Implementation: When 0, blocks the sending of MSI interrupts. When 1, permits the sending of above. (Note: See descriptions of the INTDIS, MSE, and INTSTS bits.)</p>	Access:	R/W
Access:	R/W			
	1	Memory Access Enable <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px; text-align: right;">R/W</td> </tr> </table> <p>This bit controls the IGD's response to memory space accesses. 0: Disable. 1: Enable.</p>	Access:	R/W
Access:	R/W			
	0	I/O Access Enable <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px; text-align: right;">R/W</td> </tr> </table> <p>This bit controls the IGD's response to I/O space accesses. 0: Disable. 1: Enable.</p>	Access:	R/W
Access:	R/W			

Misc Clocking / Reset Control Registers

MISCCPCTL - Misc Clocking / Reset Control Registers										
DWord	Bit	Description								
0	31:8	<p>Bonus ECO bits</p> <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td colspan="2">Bonus ECO bits</td></tr> </table>	Project:	BDW	Access:	R/W	Bonus ECO bits			
Project:	BDW									
Access:	R/W									
Bonus ECO bits										
	7	<p>DOP clock gating enable for VEbox clks</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td colspan="2">Controls the Enabling of the DOP-level Vebox (cvclk) Clock Gating via PM event messages</td></tr> <tr> <td>1</td><td>Clock gating is enabled</td></tr> <tr> <td>0</td><td>Clock gating is disabled</td></tr> </table>	Access:	R/W	Controls the Enabling of the DOP-level Vebox (cvclk) Clock Gating via PM event messages		1	Clock gating is enabled	0	Clock gating is disabled
Access:	R/W									
Controls the Enabling of the DOP-level Vebox (cvclk) Clock Gating via PM event messages										
1	Clock gating is enabled									
0	Clock gating is disabled									
	6	<p>DOP clock gating enable for Media clocks</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td colspan="2">Controls the Enabling of the DOP-level Media (cmclk) Clock Gating via PM event messages</td></tr> <tr> <td>1</td><td>Clock gating is enabled</td></tr> <tr> <td>0</td><td>Clock gating is disabled</td></tr> </table>	Access:	R/W	Controls the Enabling of the DOP-level Media (cmclk) Clock Gating via PM event messages		1	Clock gating is enabled	0	Clock gating is disabled
Access:	R/W									
Controls the Enabling of the DOP-level Media (cmclk) Clock Gating via PM event messages										
1	Clock gating is enabled									
0	Clock gating is disabled									
	5	<p>DOp clock gate enable for Media1 Clocks</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td colspan="2">Controls the Enabling of the DOP-level Render (cmclk for 2nd media block) Clock Gating via PM event messages</td></tr> <tr> <td>1</td><td>Clock gating is enabled</td></tr> <tr> <td>0</td><td>Clock gating is disabled</td></tr> </table>	Access:	R/W	Controls the Enabling of the DOP-level Render (cmclk for 2nd media block) Clock Gating via PM event messages		1	Clock gating is enabled	0	Clock gating is disabled
Access:	R/W									
Controls the Enabling of the DOP-level Render (cmclk for 2nd media block) Clock Gating via PM event messages										
1	Clock gating is enabled									
0	Clock gating is disabled									
	4	Reserved								
	3	<p>DOP Clock gating Enable for Widi clocks</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td colspan="2">Controls the Enabling of the DOP-level Render (cwclk) Clock Gating via PM event messages</td></tr> <tr> <td>1</td><td>Clock gating is enabled</td></tr> <tr> <td>0</td><td>Clock gating is disabled</td></tr> </table>	Access:	R/W	Controls the Enabling of the DOP-level Render (cwclk) Clock Gating via PM event messages		1	Clock gating is enabled	0	Clock gating is disabled
Access:	R/W									
Controls the Enabling of the DOP-level Render (cwclk) Clock Gating via PM event messages										
1	Clock gating is enabled									
0	Clock gating is disabled									

MISCCPCTL - Misc Clocking / Reset Control Registers

	2	DOP clock gating Enable for Fix clocks (cfclk)	Access:	R/W
Controls the Enabling of the DOP-level Render (cfclk/cf2xclk) Clock Gating via PM event messages 1 - Clock gating is enabled 0 - Clock gating is disabled				
	1	L1 Clock Ungate Enabling Control During Reset	Default Value:	1b
			Access:	R/W
Control to enable/disable L1 clock gating during soft resets and FLR reset processing '1' : disable L1 clock gating during soft resets and FLR '0' : enable L1 clock gating during soft resets and FLR (default op)				
	0	DOP Clock Gating Enable for Render Clocks	Access:	R/W
Controls the Enabling of the DOP-level Render (crclk/cr2xclk) Clock Gating via PM event messages 1 - Clock gating is enabled 0 - Clock gating is disabled				

MISC CTX control register

MISCCTXCTL - MISC CTX control register				
DWord	Bit	Description		
0	31:1	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
Access:	RO			
0	Context Restore ACK indication from Csunit <table border="1"> <tr> <td>Access:</td> <td>R/W Set</td> </tr> </table> <p>Context Restore ACK indication from Csunit 1'b1 : Csunit has completed restoring CPunits address space Once set, CPunit hardware clears this bit after sending the ctx save ack done message to CS 1'b0 : Csunit has NOT completed restoring CPunits address space</p>	Access:	R/W Set	
Access:	R/W Set			

Misc Reset Control Register

RSTCTL - Misc Reset Control Register						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	09420h					
Miscellaneous reset control registers.(Not Ctx save on BDW A0 for slice shutdown)						
DWord	Bit	Description				
0	31:4	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td colspan="2">Reserved</td></tr> </table>	Access:	RO	Reserved	
Access:	RO					
Reserved						
3:2	<p>Reset Staggering Period Control</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td colspan="2">Reset assertion staggering period between reset domains during FLR and soft-resets: 00: 6 csclk staggering reset assertion staggering 01: 12 cs clocks 10: 18 cs clocks 11: 24 cs clocks</td></tr> </table>	Access:	R/W	Reset assertion staggering period between reset domains during FLR and soft-resets: 00: 6 csclk staggering reset assertion staggering 01: 12 cs clocks 10: 18 cs clocks 11: 24 cs clocks		
Access:	R/W					
Reset assertion staggering period between reset domains during FLR and soft-resets: 00: 6 csclk staggering reset assertion staggering 01: 12 cs clocks 10: 18 cs clocks 11: 24 cs clocks						
1:0	<p>Reset Residency Control</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td colspan="2">Reset assertion residency period for FLR and soft-resets. "00" : 8 cs clocks "01" : 16 cs clocks "10" : 32 cs clocks "11" : 64 cs clocks</td></tr> </table>	Access:	R/W	Reset assertion residency period for FLR and soft-resets. "00" : 8 cs clocks "01" : 16 cs clocks "10" : 32 cs clocks "11" : 64 cs clocks		
Access:	R/W					
Reset assertion residency period for FLR and soft-resets. "00" : 8 cs clocks "01" : 16 cs clocks "10" : 32 cs clocks "11" : 64 cs clocks						

MISR Determinism Control Registers with Lock bit

MISR_CTRL0 - MISR Determinism Control Registers with Lock bit						
DWord	Bit	Description				
0	31	<p>Lock for MISR Control Registers</p> <table border="1"> <tr> <td>Access:</td> <td>R/W Lock</td> </tr> </table> <p>Controls whether MISR control registers are writeable. 0: Registers are writeable. 1: Registers are blocked. Lock bit cannot be cleared without cold reset (i.e., writing a 0 after having written a 1 does not clear the lock).</p>	Access:	R/W Lock		
Access:	R/W Lock					
	30:11	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO		
Access:	RO					
	10:8	<p>Reserved</p> <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Project:	BDW	Access:	RO
Project:	BDW					
Access:	RO					
	7:1	<p>MISR Core Ratio Override Value</p> <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Access:</td> <td>R/W Lock</td> </tr> </table> <p>Used for deterministic signature generation for MISR. Overrides internal core ratio[6:0]. Lock bit MISRCONTROL_LOCK applies to this register.</p>	Project:	BDW	Access:	R/W Lock
Project:	BDW					
Access:	R/W Lock					
	0	<p>Reserved</p>				

Mode Register for GAB

GAB_MODE - Mode Register for GAB		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Source:	BlitterCS	
Default Value:	0x00000000	
Access:	r/w	
Size (in bits):	32	
Address:	220A0h-220A3h	
The GAB_MODE register contains information that controls configurations in the GAB.		
DWord	Bit	Description
0	31:16	Mask Access: WO Format: Mask
	15:6	Reserved Read/Write
	5:3	BLB Arbitration Priority Format: U3
	2:0	BCS Arbitration Priority Format: U3

Mode Register for GAC

GAC_MODE - Mode Register for GAC						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Source:	VideoCS					
Default Value:	0x00000000 [BDW]					
Access:	r/w					
Size (in bits):	32					
Address:	120A0h-120A3h					
ShortName:	GAC_MODE					
Valid Projects:	[BDW]					
Address:	1C0A0h-1C0A3h					
ShortName:	GAC_MODE1					
Valid Projects:	[BDW:GT3]					
The GAC_MODE register contains information that controls configurations in the GAC.						
DWord	Bit	Description				
0	31:16	Mask <table border="1"> <tr> <td>Access:</td><td>WO</td></tr> <tr> <td>Format:</td><td>Mask</td></tr> </table>	Access:	WO	Format:	Mask
Access:	WO					
Format:	Mask					
15:1	Reserved <table border="1"> <tr> <td>Access:</td><td>r/w</td></tr> </table>	Access:	r/w			
Access:	r/w					
0	Reserved <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>r/w</td></tr> </table>	Project:	BDW	Access:	r/w	
Project:	BDW					
Access:	r/w					

Mode Register for GAFS

GAFS_MODE - Mode Register for GAFS						
DWord	Bit	Description				
0	31:16	<p>Mask Bits</p> <table border="1"> <tr> <td>Access:</td> <td>WO</td> </tr> <tr> <td>Format:</td> <td>Mask</td> </tr> </table> <p>Masks: These bits serve as write enables for bits 15:0. If this register is written with any of these bits clear the corresponding bit in the field 15:0 will not be modified. Reading these bits always returns 0s.</p>	Access:	WO	Format:	Mask
Access:	WO					
Format:	Mask					
	15:11	<p>Reserved</p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ		
Format:	MBZ					
	10	<p>Reserved</p> <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	BDW	Format:	MBZ
Project:	BDW					
Format:	MBZ					
	9	<p>Reserved</p>				
	8:2	<p>Reserved</p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ		
Format:	MBZ					
	1:0	<p>Reserved</p> <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	BDW	Format:	MBZ
Project:	BDW					
Format:	MBZ					

MSI Cap ID and Message Control

MID_MMIC - MSI Cap ID and Message Control							
DWord	Bit	Description					
0	31:24	<p>Reserved</p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ			
Format:	MBZ						
23	<p>64b Address Capability</p> <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td colspan="2">32 bit message address.</td></tr> </table>	Default Value:	0b	Access:	RO	32 bit message address.	
Default Value:	0b						
Access:	RO						
32 bit message address.							
22:20	<p>Multiple Message Enable</p> <table border="1"> <tr> <td>Default Value:</td> <td>000b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td colspan="2">Hardwired to 0 (there is only 1 message).</td></tr> </table>	Default Value:	000b	Access:	RO	Hardwired to 0 (there is only 1 message).	
Default Value:	000b						
Access:	RO						
Hardwired to 0 (there is only 1 message).							
19:17	<p>Multiple Message Capable</p> <table border="1"> <tr> <td>Default Value:</td> <td>000b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td colspan="2">Hardwired to 0 (there is only 1 message).</td></tr> </table>	Default Value:	000b	Access:	RO	Hardwired to 0 (there is only 1 message).	
Default Value:	000b						
Access:	RO						
Hardwired to 0 (there is only 1 message).							
16	<p>MSI Enable</p> <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W Variant</td> </tr> <tr> <td colspan="2">If set an MSI is generated instead of INTx#. MSI Cap ID and Message Control</td></tr> </table>	Default Value:	0b	Access:	R/W Variant	If set an MSI is generated instead of INTx#. MSI Cap ID and Message Control	
Default Value:	0b						
Access:	R/W Variant						
If set an MSI is generated instead of INTx#. MSI Cap ID and Message Control							
15:8	<p>Next Capability</p> <table border="1"> <tr> <td>Default Value:</td> <td>70h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td colspan="2">Points to the PCI Express capability structure. MSI Cap ID and Message Control</td></tr> </table>	Default Value:	70h	Access:	RO	Points to the PCI Express capability structure. MSI Cap ID and Message Control	
Default Value:	70h						
Access:	RO						
Points to the PCI Express capability structure. MSI Cap ID and Message Control							

MID_MMC - MSI Cap ID and Message Control

Cap ID		
Default Value:		05h
Access:		RO
Indicates that this pointer is a MSI capability.		

MSI Message Base Address

MMA - MSI Message Base Address						
DWord	Bit	Description				
0	31:2	Message Lower Address				
		<table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> <tr> <td colspan="2">Lower Address used for MSI Message.</td></tr> </table>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					
Lower Address used for MSI Message.						
1:0	Reserved					
<table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ				
Format:	MBZ					

MSI Message Data

MMD - MSI Message Data					
DWord	Bit	Description			
0	31:16	Reserved <table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ	
Format:	MBZ				
15:0	Message Data <table border="1"> <tr> <td>Default Value:</td><td>0000h</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Data used for MSI Message.</p>	Default Value:	0000h	Access:	R/W
Default Value:	0000h				
Access:	R/W				

MTRR Capability Register 0

MTRR_CR_0 - MTRR Capability Register 0			
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x0000050A Size (in bits): 32			
Address: 0F100h			
Register to define MTRR - range register capabilities.			
DWord	Bit	Description	
0	31:11	Reserved	
		Default Value:	0000000000000000000000000000000b
		Access:	RO
	10	Write Combining Support	
		Default Value:	1b
		Access:	RO
0: Write Combining (WC) memory type is not supported. 1: Write Combining (WC) memory type is supported. GFX Implementation: More details on memory type section however WC support in GFX looks like streamlining non-cacheable accesses. This is the existing UC concept used in GFX architecture.			
9	9	Reserved	
		Default Value:	0b
8	9		
	8	Fixed Range MTRRs Support	
		Default Value:	1b
		Access:	RO
		0: No Fixed range MTRRs are supported. 1: Fixed Range MTRRs (IA32_MTRR_FIX64K_00000 through IA32_MTRR_FIX4K_0F8000) are supported.	
7:0	7:0	Variable Range MTRR Count	
		Default Value:	0Ah
		Access:	RO
Indicates the number of variable ranges implemented.			

MTRR Capability Register 1

MTRR_CR_1 - MTRR Capability Register1						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	0F104h					
Register to define MTRR - range register capabilities						
DWord	Bit	Description				
0	31:0	<p>MTRR Capability Register 1 Reserved</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Bit[63:32]: Reserved.</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

MTRR Default Type Register 0

MTRR_DT_0 - MTRR Default Type Register 0			
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x00000000 Size (in bits): 32			
Address: 0F108h			
Register to define MTRR - range register capabilities.			
DWord	Bit	Description	
0	31:12	Reserved	
		Default Value:	00000000000000000000000000000000b
		Access:	RO
	11	Reserved	
	10	Fixed Range MTRR Enable/Disable	
		Default Value:	0b
		Access:	R/W
0: Disable fixed-range MTRRs. 1: Enable fixed-range MTRRs. When the fixed-range MTRRs are enabled, they take priority over the variable-range MTRRs when overlaps in ranges occur. If the fixed-range MTRRs are disabled, the variable range MTRRs can still be used and can map the range ordinarily covered by the fixed-range MTRRs. GFX Implementation: GFX uses this field as a specific enable/disable for fixed range MTRRs.			
9:8	Reserved		
		Default Value:	00b
		Access:	RO
7:0	Default Memory Type		
		Default Value:	00h
		Access:	R/W
Indicates default memory type used for physical memory address ranges that do not have a memory type specified for them by an MTRR. Legal values for this field are 0, 1, 4, 5, and 6. GFX Implementation: GFX uses this field to assign memory regions that are not assigned as part of the fixed and variable range registers.			

MTRR Default Type Register 1

MTRR_DT_1 - MTRR Default TypeRegister1								
Register Space:	MMIO: 0/2/0							
Project:	BDW							
Default Value:	0x00000000							
Size (in bits):	32							
Address:	0F10Ch							
Register to define MTRR - range register capabilities.								
DWord	Bit	Description						
0	31:0	<p>MTRR Default Type Register 1 Reserved</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> <tr> <td colspan="2">Bit[63:32]: Reserved.</td></tr> </table>	Default Value:	00000000h	Access:	RO	Bit[63:32]: Reserved.	
Default Value:	00000000h							
Access:	RO							
Bit[63:32]: Reserved.								

MT Virtual Page Address Registers

MTTLB_VA - MT Virtual Page Address Registers						
Register Space: MMIO: 0/2/0						
Project:	BDW					
Source:	RenderCS					
Default Value:	0x00000000					
Access:	RO					
Size (in bits):	32					
Trusted Type:	1					
Address:	04800h-04803h					
DWord	Bit	Description				
0	31:12	Address <table border="1"> <tr> <td>Format:</td><td>GraphicsAddress[31:12]</td></tr> <tr> <td colspan="2">Page virtual address.</td></tr> </table>	Format:	GraphicsAddress[31:12]	Page virtual address.	
Format:	GraphicsAddress[31:12]					
Page virtual address.						
11:0	Reserved <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	BDW	Format:	MBZ	
Project:	BDW					
Format:	MBZ					

Multi Size Aperture Control

MSAC_0_2_0_PCI - Multi Size Aperture Control						
DWord	Bit	Description				
0	7:5	<p>Reserved R/W</p> <table border="1"> <tr> <td>Default Value:</td> <td>000b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Scratch Bits</p>	Default Value:	000b	Access:	R/W
Default Value:	000b					
Access:	R/W					
4	<p>Aperture Size Bit 4</p> <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W Key</td> </tr> </table>	Default Value:	0b	Access:	R/W Key	
Default Value:	0b					
Access:	R/W Key					
3	<p>Aperture Size Bit 3</p> <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W Key</td> </tr> </table>	Default Value:	0b	Access:	R/W Key	
Default Value:	0b					
Access:	R/W Key					
2	<p>Aperture Size Bit 2</p> <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W Key</td> </tr> </table>	Default Value:	0b	Access:	R/W Key	
Default Value:	0b					
Access:	R/W Key					
1	<p>Aperture Size Bit 1</p> <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W Key</td> </tr> </table>	Default Value:	0b	Access:	R/W Key	
Default Value:	0b					
Access:	R/W Key					
0	<p>Aperture Size Bit 0</p> <table border="1"> <tr> <td>Default Value:</td> <td>1b</td> </tr> <tr> <td>Access:</td> <td>R/W Key</td> </tr> </table>	Default Value:	1b	Access:	R/W Key	
Default Value:	1b					
Access:	R/W Key					

NDE_RSTWRN_OPT

NDE_RSTWRN_OPT								
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x00000000 Access: R/W Size (in bits): 32								
Address: 46408h-4640Bh Name: North Display Reset Warn Options ShortName: NDE_RSTWRN_OPT Valid Projects: BDW Power: Always on Reset: global								
This register is used to control the display behavior on receiving a Reset Warning.								
DWord	Bit	Description						
0	31:7	Reserved						
		Format:	MBZ					
	6	Reserved	BDW					
	5	Reserved						
	4	RST PCH Handshake En	This field enables the handshake with PCH display when processing the reset. This applies to all types of DE resets. By default it is disabled and the north display will not wait for south display to acknowledge the reset.					
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Disable</td></tr> <tr> <td>1b</td><td>Enable</td></tr> </tbody> </table>	Value	Name	0b	Disable	1b	Enable
Value	Name							
0b	Disable							
1b	Enable							
3:0	Reserved	<table border="1"> <thead> <tr> <th>Restriction</th><th>Project</th></tr> </thead> <tbody> <tr> <td>BIOS must set this to 1b after the PCH display BDF has been enabled and before enabling any function in the PCH display. The PCH display BDF is enabled by setting 0:31:0 Root Complex Base Address + 0x3428 bit 0 = 1b.</td><td>BDW</td></tr> </tbody> </table>	Restriction	Project	BIOS must set this to 1b after the PCH display BDF has been enabled and before enabling any function in the PCH display. The PCH display BDF is enabled by setting 0:31:0 Root Complex Base Address + 0x3428 bit 0 = 1b.	BDW		
Restriction	Project							
BIOS must set this to 1b after the PCH display BDF has been enabled and before enabling any function in the PCH display. The PCH display BDF is enabled by setting 0:31:0 Root Complex Base Address + 0x3428 bit 0 = 1b.	BDW							

NOP Identification Register

NOPIID - NOP Identification Register							
Register Space:	MMIO: 0/2/0						
Project:	BDW						
Source:	RenderCS						
Default Value:	0x00000000						
Size (in bits):	32						
Trusted Type:	1						
Address:	02094h						
<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center; background-color: #e0e0ff;">Description</th> <th style="text-align: center; background-color: #e0e0ff;">Project</th> </tr> </thead> <tbody> <tr> <td>Access: RW</td> <td>BDW</td> </tr> <tr> <td>The NOPID register contains the Noop Identification value specified by the last MI_NOOP instruction that enabled this register to be updated.</td> <td></td> </tr> </tbody> </table>		Description	Project	Access: RW	BDW	The NOPID register contains the Noop Identification value specified by the last MI_NOOP instruction that enabled this register to be updated.	
Description	Project						
Access: RW	BDW						
The NOPID register contains the Noop Identification value specified by the last MI_NOOP instruction that enabled this register to be updated.							
DWord	Bit	Description					
0	31:22	Reserved <table border="1" style="margin-left: 20px; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Format:</td> <td style="padding: 2px;">MBZ</td> </tr> </table>	Format:	MBZ			
	Format:	MBZ					
21:0	Reserved						

OA Interrupt Mask Register

OA_IMR - OA Interrupt Mask Register			
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0xFFFFFFFF Access: R/W Size (in bits): 32 Address: 02B20h			
The OAIMR register is used by software to control whether OA generates an interrupt or not.			
DWord	Bit	Description	
0	31:29	Reserved	
		Default Value:	7h
		Format:	PBC
	28	Mask Bit	
		Value	Name
		0h	Not Masked
		1h	Masked [Default]
	27:0	Reserved	
		Default Value:	FFFFFFFh
		Format:	PBC

OA TLB Control Register

OTCR - OA TLB Control Register						
DWord	Bit	Description				
0	31:1	<p>Reserved</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000000000000000000000000000b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	00000000000000000000000000000000b	Access:	RO
Default Value:	00000000000000000000000000000000b					
Access:	RO					
	0	<p>Invalidate TLBs on the corresponding Engine</p> <table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>SW writes 1 to invalidate the TLBs for the associated engine and HW clears the bit when invalidation is complete. To ensure proper invalidation of the TLBs, SW has to ensure the corresponding engine's HW pipeline is flushed and cleared from all its memory accesses. Otherwise HW cannot guarantee the proper invalidation for TLBs. This bit is self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					

Observation Architecture Buffer

OABUFFER - Observation Architecture Buffer																																
Register Space: MMIO: 0/2/0 Project: BDW 0x00000001 [BDW] Size (in bits): 32																																
Address: 02B14h Valid Projects: [BDW] Access: R/W																																
This register is used to program the OA unit.																																
Programming Notes																																
This MMIO must be set before the OATAILPTR register and set after the OAHEADPTR register. This is to enable proper functionality of the overflow bit.																																
DWord	Bit	Description																														
0	31:6	Report Buffer Offset <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 15%;">Format:</td><td>GraphicsAddress[31:6]</td></tr> <tr> <td colspan="2">This field specifies 64B aligned GFX MEM address where the chap counter values are reported.</td></tr> </table>	Format:	GraphicsAddress[31:6]	This field specifies 64B aligned GFX MEM address where the chap counter values are reported.																											
Format:	GraphicsAddress[31:6]																															
This field specifies 64B aligned GFX MEM address where the chap counter values are reported.																																
5:3	Inter Trigger Report Buffer Size <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Project:</td><td>BDW</td></tr> <tr> <td colspan="2">This field indicates the size of report buffer for time/event-based report trigger mechanisms. This field is programmed in terms of multiple of 128KB.</td></tr> </table> <table border="1" style="width: 100%; border-collapse: collapse; margin-top: 5px;"> <thead> <tr> <th style="width: 15%;">Value</th><th style="width: 45%;">Name</th><th style="width: 40%;">Description</th></tr> </thead> <tbody> <tr><td>0h</td><td>128 KB [Default]</td><td>All context considered</td></tr> <tr><td>1h</td><td>256 KB</td><td></td></tr> <tr><td>2h</td><td>512 KB</td><td></td></tr> <tr><td>3h</td><td>1 MB</td><td></td></tr> <tr><td>4h</td><td>2 MB</td><td></td></tr> <tr><td>5h</td><td>4 MB</td><td></td></tr> <tr><td>6h</td><td>8 MB</td><td></td></tr> <tr><td>7h</td><td>16 MB</td><td></td></tr> </tbody> </table>	Project:	BDW	This field indicates the size of report buffer for time/event-based report trigger mechanisms. This field is programmed in terms of multiple of 128KB.		Value	Name	Description	0h	128 KB [Default]	All context considered	1h	256 KB		2h	512 KB		3h	1 MB		4h	2 MB		5h	4 MB		6h	8 MB		7h	16 MB	
Project:	BDW																															
This field indicates the size of report buffer for time/event-based report trigger mechanisms. This field is programmed in terms of multiple of 128KB.																																
Value	Name	Description																														
0h	128 KB [Default]	All context considered																														
1h	256 KB																															
2h	512 KB																															
3h	1 MB																															
4h	2 MB																															
5h	4 MB																															
6h	8 MB																															
7h	16 MB																															
2	OA Report Trigger Select <table border="1" style="width: 100%; border-collapse: collapse; margin-top: 5px;"> <thead> <tr> <th style="width: 25%;">Value</th><th style="width: 25%;">Name</th><th style="width: 50%;">Description</th></tr> </thead> <tbody> <tr><td>0</td><td></td><td>Level Report trigger</td></tr> <tr><td>1</td><td></td><td>Edge Report trigger</td></tr> </tbody> </table>	Value	Name	Description	0		Level Report trigger	1		Edge Report trigger																						
Value	Name	Description																														
0		Level Report trigger																														
1		Edge Report trigger																														

OABUFFER - Observation Architecture Buffer

	1	Disable Overrun Mode																
		<table border="1"> <tr> <td>Project:</td><td colspan="2">BDW</td></tr> <tr> <td>Format:</td><td colspan="2">Enable</td></tr> </table>			Project:	BDW		Format:	Enable									
Project:	BDW																	
Format:	Enable																	
		<p>This field defines the mode of reporting for internal trigger/timer based reporting. When this bit is set, overrun does not lose reports but stops reporting. Based on the head and tail pointer, when HW detects room for the report, it would resume reporting to the buffer. This mode would not set the over-run bit in the register. When this mode bit is reset, buffer overrun can happen and lose the reports while setting the buffer over-run bit.</p>																
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0h</td><td>Disable [Default]</td></tr> <tr> <td>1h</td><td>Enable</td></tr> </tbody> </table>		Value	Name	0h	Disable [Default]	1h	Enable	<table border="1"> <thead> <tr> <th colspan="2">Description</th></tr> </thead> <tbody> <tr> <td>Counter gets written out on regular intervals, defined by the Timer Period</td><td></td></tr> <tr> <td>Counter does not get written out on regular interval</td><td></td></tr> </tbody> </table>			Description		Counter gets written out on regular intervals, defined by the Timer Period		Counter does not get written out on regular interval	
Value	Name																	
0h	Disable [Default]																	
1h	Enable																	
Description																		
Counter gets written out on regular intervals, defined by the Timer Period																		
Counter does not get written out on regular interval																		
	0	Memory Select PPGTT/GGTT Access																
		<table border="1"> <tr> <td>Project:</td><td colspan="2">BDW</td></tr> </table>			Project:	BDW												
Project:	BDW																	
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0h</td><td>PPGTT</td></tr> <tr> <td>1h</td><td>GGTT [Default]</td></tr> </tbody> </table>			Value	Name	0h	PPGTT	1h	GGTT [Default]								
Value	Name																	
0h	PPGTT																	
1h	GGTT [Default]																	
		<p style="text-align: center;">Programming Notes</p> <p>When each context has its own Per Process GTT, this field should be always set to GGTT.</p>																

Observation Architecture Control

OACONTROL - Observation Architecture Control													
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x00000000 Access: R/W Size (in bits): 32													
Address: 02B00h Valid Projects: [BDW]													
This register controls global OA functionality, report format, interrupt steering and context filtering.													
DWord	Bit	Description											
0	31:6	Reserved <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>PBC</td></tr> </table>	Project:	BDW	Format:	PBC							
Project:	BDW												
Format:	PBC												
	5	Interrupt Steering Bit <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> </table> <p>When reset, OACS unit sends the interrupt message to Display Engine as config writes on GAM interface.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0h</td><td>DE [Default]</td><td>To display engine via GAM</td></tr> <tr> <td>1h</td><td>Reserved</td><td></td></tr> </tbody> </table>	Project:	BDW	Value	Name	Description	0h	DE [Default]	To display engine via GAM	1h	Reserved	
Project:	BDW												
Value	Name	Description											
0h	DE [Default]	To display engine via GAM											
1h	Reserved												
	4:2	Counter Select <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>Performance Counter Report Format</td></tr> </table> <p>This field selects which performance counter report format to use, please refer to Performance Counter Report Formats section for more details on the structure of the format.</p>	Project:	BDW	Format:	Performance Counter Report Format							
Project:	BDW												
Format:	Performance Counter Report Format												
	1	Specific Context Enable <table border="1"> <tr> <td>Format:</td><td>Enable</td></tr> </table> <p>Description</p> <p>Enables counters to work on a context specific workload. The context is given by bits 31:12. OA unit level clock gating must be ENABLED when using specific ContextID feature.</p> <p>When "Specific Context Enable" bit is set to '1' in OACONTROL register, Boolean/Threshold report trigger function gets enabled only for the selected context. When "Specific Context Enable" bit is set to '0' in OACONTROL register, Boolean/Threshold report trigger function gets enabled for all contexts.</p> <p>Timer Based Report logic is not sensitive to "Specific Context Enable" bit programmed in OACONTROL register.</p>	Format:	Enable									
Format:	Enable												

OACONTROL - Observation Architecture Control

<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0h</td><td>Disable [Default]</td><td>All contexts are considered</td></tr> <tr> <td>1h</td><td>Enable</td><td>Only the contexts with the Select Context ID field in OACTXID are considered</td></tr> </tbody> </table>			Value	Name	Description	0h	Disable [Default]	All contexts are considered	1h	Enable	Only the contexts with the Select Context ID field in OACTXID are considered
Value	Name	Description									
0h	Disable [Default]	All contexts are considered									
1h	Enable	Only the contexts with the Select Context ID field in OACTXID are considered									
Workaround											
<p>Workaround : Render engine pulls down Context ID match during lite restore flows irrespective of Context ID match. This results in OA freezing during the lite restore flows when Specific Context Enable is set missing to count the events occurring during lite restore window.</p> <p>This needs to be work around either by</p> <ul style="list-style-type: none"> • Specific Context Enable must not be set. Or • Lite restore must be disabled in render engine by setting Force PD Restore in the context descriptor on context submission. 											
0	Performance Counter Enable <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>Enable</td></tr> </table> <p>Global performance counter enable. If clear, no counting will occur. MI_REPORT_PERF_COUNT is undefined when clear.</p>		Project:	All	Format:	Enable					
Project:	All										
Format:	Enable										
	Programming Notes										
	<p>When this bit is set, OABUFFER, OAHEADPTR and OATAILPTR must be programmed correctly to ensure report triggers due to Context Switch and GO transition happen correctly.</p>										

Observation Architecture Control Context ID

OACTXID - Observation Architecture ControlContextID		
Register Space: MMIO: 0/2/0 Project: BDW Source: RenderCS Default Value: 0x00000000 Access: R/W Size (in bits): 32		
Address: 02364h		
This register has the context details when Specific context Enable is set. This register is implemented in render command streamer and render context save/restored. This register should be initialized by SW appropriately on the very first submission of a context when OA is enabled.		
DWord	Bit	Description
0	31:0	Select Context ID Specifies the context ID of the one context that affects the performance counters when "Specific Context Enable" bit is set. All other contexts are ignored. Ring Buffer Mode of Scheduling: Bits[31:12] represent the CCID and bits [11:0] must be zero. Exelist mode of scheduling: Bits[31:0] represent the context id.

Observation Architecture Control per Context

OACTXCONTROL - Observation Architecture Control per Context										
Register Space: MMIO: 0/2/0 Project: BDW Source: RenderCS Default Value: 0x00000000 Access: R/W Size (in bits): 32										
Address: 02360h										
This register is implemented in render command streamer and render context save/restored. This register should be initialized by SW appropriately on the very first submission of a context when OA is enabled.										
DWord	Bit	Description								
0	30:8	<p>Reserved</p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ						
	Format:	MBZ								
7:2	<p>Timer Period</p> <table border="1"> <tr> <td>Format:</td> <td>Select</td> </tr> </table> <p>Specifies the period of the timer strobe as a function of the minimum TIME_STAMP resolution. The period is determined by selecting a specified bit from the TIME_STAMP register as follows: StrobePeriod = MinimumTimeStampPeriod * 2 (TimerPeriod + 1) The exponent is defined by this field.</p> <p>Note: The TIME_STAMP is not reset at start time so the phase of the strobe is not synchronized with the enable of the OA unit. This could result in approximately a full StrobePeriod elapsing prior to the first trigger. Usage for this mechanism should be time based periodic triggering, typically.</p>	Format:	Select							
Format:	Select									
1	1	<p>Timer Enable</p> <table border="1"> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>Description</p> <p>This field enables the timer logic to output a periodic strobe, as defined by the Timer Period. When disabled the timer output is not asserted. Users should be aware that the timer-based report logic and the Boolean report trigger logic are logically OR'd together with no buffering of report triggers. This implies that only one performance counter report will be generated for clocks where both the timer-based report logic and the Boolean report trigger logic trigger a performance counter report.</p> <p>Timer Based Report logic is not sensitive to "Specific Context Enable" bit programmed in OACONTROL register.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0h</td><td>Disable[Default]</td><td>Counter does not get written out on regular interval</td></tr> </tbody> </table>	Format:	Enable	Value	Name	Description	0h	Disable[Default]	Counter does not get written out on regular interval
	Format:	Enable								
	Value	Name	Description							
0h	Disable[Default]	Counter does not get written out on regular interval								

OACTXCONTROL - Observation Architecture Control per Context

		1h	Enable	Counter gets written out on regular intervals, defined by the Timer Period													
	0	Counter Stop-Resume Mechanism															
		Format: <input type="text"/> Select															
		Description															
		Counter stop-resume mechanism: signal name: cs_oa_perfcntr_freeze															
		<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: left; padding: 2px;">Value</th> <th style="text-align: left; padding: 2px;">Name</th> <th style="text-align: left; padding: 2px;">Description</th> <th style="text-align: left; padding: 2px;">Technologies</th> </tr> </thead> <tbody> <tr> <td style="padding: 2px;">0h</td> <td style="padding: 2px;">[Default]</td> <td style="padding: 2px;">Reserved</td> <td style="padding: 2px;"></td> </tr> <tr> <td style="padding: 2px;">1h</td> <td style="padding: 2px;"></td> <td style="padding: 2px;">resume counting for all counters</td> <td style="padding: 2px;"></td> </tr> </tbody> </table>				Value	Name	Description	Technologies	0h	[Default]	Reserved		1h		resume counting for all counters	
Value	Name	Description	Technologies														
0h	[Default]	Reserved															
1h		resume counting for all counters															

Observation Architecture Head Pointer

OAHEADPTR - Observation Architecture Head Pointer				
DWord	Bit	Description		
0	31:6	<p>Head Pointer Virtual address of the internal trigger based buffer that is updated by software after consuming reports from the report buffer. This pointer must be updated by SW only when using time or event-based report triggering.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="text-align: center; padding: 2px;">Programming Notes</td></tr> <tr> <td style="padding: 2px;">SW must ensure that Head Pointer and the Tail Pointer match before enabling internally triggered performance counter reporting.</td></tr> </table>	Programming Notes	SW must ensure that Head Pointer and the Tail Pointer match before enabling internally triggered performance counter reporting.
Programming Notes				
SW must ensure that Head Pointer and the Tail Pointer match before enabling internally triggered performance counter reporting.				
<p>Reserved</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Format:</td><td style="width: 30%;">PBC</td></tr> </table>			Format:	PBC
Format:	PBC			

Observation Architecture Report Trigger 2

OAREPORTTRIG2 - Observation Architecture Report Trigger 2

Register Space: MMIO: 0/2/0

Project: BDW

Default Value: 0x00000000

Access: R/W

Size (in bits): 32

Address: 02744h

Description

This register controls some of the Boolean logic defining Boolean/threshold report trigger 0. The bit definitions in this register refer to the stages in the report trigger block diagram in the Performance Counter Reporting section.

Report triggers generated from OAREPORTTRIG 1-4 and OAREPORTTRIG 5-8 are ORed to form a new report trigger. Report trigger behavior can be derived by programming these two sets of OA REPORT registers with the same value. Users should be aware that while programming Timer based and Threshold Counter based triggers simultaneously for internal reporting, they should be programmed such way that they are not consecutively triggered. If programmed simultaneously, RTL pulse detection logic will have problem when these triggers occur in consecutive clock cycles.

DWord	Bit	Description				
0	31	Report Trigger Enable				
		<table border="1"> <tr> <td>Format:</td> <td>Enable</td> </tr> </table>			Format:	Enable
Format:	Enable					
		Description				
		Enable Boolean/threshold report trigger 0. Users should be aware that the timer-based report logic and the Boolean report trigger logic are logically OR'd together with no buffering of report triggers. This implies that only one performance counter report will be generated for clocks where both the timer-based report logic and the Boolean report trigger logic trigger a performance counter report.				
		When "Specific Context Enable" bit set to '1' in OACONTROL register, Boolean/Threshold report trigger function gets enabled only for the selected context. When "Specific Context Enable" bit set to '0' in OACONTROL register, Boolean/Threshold report trigger function gets enabled for all contexts.				
	30:24	Reserved				
		<table border="1"> <tr> <td>Format:</td> <td>PBC</td> </tr> </table>			Format:	PBC
Format:	PBC					
	23	Threshold Enable				
		<table border="1"> <tr> <td>Format:</td> <td>Enable</td> </tr> </table>			Format:	Enable
Format:	Enable					
		Enable the threshold compare logic within the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).				

OAREPORTTRIG2 - Observation Architecture Report Trigger 2

	22	Invert D Enable 0	Format:	Enable	Invert the specified signal at the D stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	21	Invert C Enable 1	Format:	Enable	Invert the specified signal at the C stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	20	Invert C Enable 0	Format:	Enable	Invert the specified signal at the C stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	19	Invert B Enable 3	Format:	Enable	Invert the specified signal at the B stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	18	Invert B Enable 2	Format:	Enable	Invert the specified signal at the B stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	17	Invert B Enable 1	Format:	Enable	Invert the specified signal at the B stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	16	Invert B Enable 0	Format:	Enable	Invert the specified signal at the B stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	15	Invert A Enable 15	Format:	Enable	Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).

OAREPORTTRIG2 - Observation Architecture Report Trigger 2

	14	Invert A Enable 14	Format:	Enable	Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	13	Invert A Enable 13	Format:	Enable	Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	12	Invert A Enable 12	Format:	Enable	Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	11	Invert A Enable 11	Format:	Enable	Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	10	Invert A Enable 10	Format:	Enable	Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	9	Invert A Enable 9	Format:	Enable	Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	8	Invert A Enable 8	Format:	Enable	Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	7	Invert A Enable 7	Format:	Enable	Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).

OAREPORTTRIG2 - Observation Architecture Report Trigger 2

	6	Invert A Enable 6	Format:	Enable	Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	5	Invert A Enable 5	Format:	Enable	Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	4	Invert A Enable 4	Format:	Enable	Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	3	Invert A Enable 3	Format:	Enable	Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	2	Invert A Enable 2	Format:	Enable	Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	1	Invert A Enable 1	Format:	Enable	Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	0	Invert A Enable 0	Format:	Enable	Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).

Observation Architecture Report Trigger 6

OAREPORTTRIG6 - Observation Architecture Report Trigger 6

Register Space: MMIO: 0/2/0

Project: BDW

Default Value: 0x00000000

Access: R/W

Size (in bits): 32

Address: 02754h

Description

This register controls some of the Boolean logic defining Boolean/threshold report trigger 1. Note that Boolean report triggers 0 and 1 are logically OR'd together without buffering, this implies that only one performance counter report will be generated for clocks where both Boolean report triggers evaluate true. The bit definitions in this register refer to the stages in the report trigger block diagram in the Performance Counter Reporting section.

Report triggers generated from OAREPORTTRIG 1-4 and OAREPORTTRIG 5-8 are ORed to form a new report trigger. Report trigger behavior can be derived by programming these two sets of OA REPORT registers with the same value. Users should be aware that while programming Timer based and Threshold Counter based triggers simultaneously for internal reporting, they should be programmed such way that they are not consecutively triggered. If programmed simultaneously, RTL pulse detection logic will have problem when these triggers occur in consecutive clock cycles.

DWord	Bit	Description						
0	31	<p>Report Trigger Enable</p> <table border="1"> <thead> <tr> <th colspan="2">Description</th> </tr> </thead> <tbody> <tr> <td colspan="2">Enable Boolean/threshold report trigger 0. Users should be aware that the timer-based report logic and the Boolean report trigger logic are logically OR'd together with no buffering of report triggers. This implies that only one performance counter report will be generated for clocks where both the timer-based report logic and the Boolean report trigger logic trigger a performance counter report.</td> </tr> <tr> <td colspan="2">When "Specific Context Enable" bit set to '1' in OACONTROL register, Boolean/Threshold report trigger function gets enabled only for the selected context. When "Specific Context Enable" bit set to '0' in OACONTROL register, Boolean/Threshold report trigger function gets enabled for all contexts.</td> </tr> </tbody> </table>	Description		Enable Boolean/threshold report trigger 0. Users should be aware that the timer-based report logic and the Boolean report trigger logic are logically OR'd together with no buffering of report triggers. This implies that only one performance counter report will be generated for clocks where both the timer-based report logic and the Boolean report trigger logic trigger a performance counter report.		When "Specific Context Enable" bit set to '1' in OACONTROL register, Boolean/Threshold report trigger function gets enabled only for the selected context. When "Specific Context Enable" bit set to '0' in OACONTROL register, Boolean/Threshold report trigger function gets enabled for all contexts.	
Description								
Enable Boolean/threshold report trigger 0. Users should be aware that the timer-based report logic and the Boolean report trigger logic are logically OR'd together with no buffering of report triggers. This implies that only one performance counter report will be generated for clocks where both the timer-based report logic and the Boolean report trigger logic trigger a performance counter report.								
When "Specific Context Enable" bit set to '1' in OACONTROL register, Boolean/Threshold report trigger function gets enabled only for the selected context. When "Specific Context Enable" bit set to '0' in OACONTROL register, Boolean/Threshold report trigger function gets enabled for all contexts.								
	30:24	<p>Reserved</p> <table border="1"> <tr> <td>Format:</td> <td>PBC</td> </tr> </table>	Format:	PBC				
Format:	PBC							
	23	<p>Threshold Enable</p> <p>Enable the threshold compare logic within the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).</p>						
	22	<p>Invert D Enable 0</p> <p>Invert the specified signal at the D stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).</p>						

OAREPORTTRIG6 - Observation Architecture Report Trigger 6

	21	Invert C Enable 1 Invert the specified signal at the C stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	20	Invert C Enable 0 Invert the specified signal at the C stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	19	Invert B Enable 3 Invert the specified signal at the B stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	18	Invert B Enable 2 Invert the specified signal at the B stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	17	Invert B Enable 1 Invert the specified signal at the B stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	16	Invert B Enable 0 Invert the specified signal at the B stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	15	Invert A Enable 15 Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	14	Invert A Enable 14 Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	13	Invert A Enable 13 Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	12	Invert A Enable 12 Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	11	Invert A Enable 11 Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	10	Invert A Enable 10 Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	9	Invert A Enable 9 Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	8	Invert A Enable 8 Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).

OAREPORTTRIG6 - Observation Architecture Report Trigger 6

	7	Invert A Enable 7 Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	6	Invert A Enable 6 Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	5	Invert A Enable 5 Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	4	Invert A Enable 4 Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	3	Invert A Enable 3 Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	2	Invert A Enable 2 Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	1	Invert A Enable 1 Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	0	Invert A Enable 0 Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).

Observation Architecture Report Trigger Counter

OARPTTRIG_COUNTER - Observation Architecture Report Trigger Counter		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	02B1Ch	
This register provides status of report trigger threshold count 1 and 2. This register is for HW internal purpose and power context save/restored. This register must not be programmed by SW.		
DWord	Bit	Description
0	31:16	Report Trig Threshold Count 1 Status
		Programming Notes
This field is for HW internal use to context save/restore rpt trigger threshold count 1. It always indicates current value of HW's internal report trigger count. SW should not program these bits.		
	15:0	Report Trig Threshold count 2 status
		Programming Notes
This field is for HW internal use to context save/restore rpt trigger threshold count 2. It always indicates current value of HW's internal report trigger count. SW should not program these bits.		

Observation Architecture Start Trigger 5

OASTARTTRIG5 - Observation Architecture Start Trigger 5			
DWord	Bit	Description	
0	31:16	Reserved	
		Project: BDW Format: PBC	
	15:0	Threshold Value	
		Format: U16	
Programming Notes			
		Threshold value for the compare logic within the start trigger logic for B7-B4 counters.	

Observation Architecture Start Trigger Counter

OASTARTTRIG_COUNTER - Observation Architecture Start Trigger Counter		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	02B18h	
This register provides status of start trigger threshold count 1 and 2. This register is for HW internal purpose.		
DWord	Bit	Description
0	31:16	<p>Start Trig Threshold Count 1 Status</p> <p>Programming Notes</p> <p>This field is for HW internal use to context save/restore start trigger threshold count 1. It always indicates current value of HW's internal start trigger count. SW should not program these bits.</p>
	15:0	<p>Start Trig Threshold count 2 status</p> <p>Programming Notes</p> <p>This field is for HW internal use to context save/restore start trigger threshold count 2. It always indicates current value of HW's internal start trigger count. SW should not program these bits.</p>

Observation Architecture Status Register

OASTATUS - Observation Architecture Status Register

Register Space: MMIO: 0/2/0

Project: BDW

Default Value: 0x00030000

Access: R/W

Size (in bits): 32

Address: 02B08h

This register provides status of report buffer and overflow conditions as well as status of some flags which hardware needs for internal purpose. Software should not program these status bits.

DWord	Bit	Description							
0	31:22	Reserved							
		Default Value:	0						
		Format:	PBC						
Start Trigger Flag 1									
<table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0</td><td>[Default]</td></tr> <tr> <td>1</td><td></td></tr> </tbody> </table>				Value	Name	0	[Default]	1	
Value	Name								
0	[Default]								
1									
Programming Notes									
This bit is for HW internal use to context save /restore Start Trigger 1 occurrence On RC6 entry. Software should not program this bit.									
Start Trigger Flag 2									
<table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0</td><td>[Default]</td></tr> <tr> <td>1</td><td></td></tr> </tbody> </table>				Value	Name	0	[Default]	1	
Value	Name								
0	[Default]								
1									
Programming Notes									
This bit is for HW internal use to context save /restore Start Trigger 2 occurrence On RC6 entry. Software should not program this bit.									
Report Trigger Flag 1									
<table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0</td><td>[Default]</td></tr> <tr> <td>1</td><td></td></tr> </tbody> </table>				Value	Name	0	[Default]	1	
Value	Name								
0	[Default]								
1									
Programming Notes									
This bit is for HW internal use to context save /restore Report Trigger 1 occurrence On RC6 entry. Software should not program this bit.									

OASTATUS - Observation Architecture Status Register

	18	Report Trigger Flag 2				
			Value	Name		
		0	[Default]			
		1				
	Programming Notes					
	This bit is for HW internal use to context save /restore Report Trigger 2 occurrence On RC6 entry. Software should not program this bit.					
	17	Tail Pointer Wrap Flag				
		Format:	U1			
			Value	Name		
		0				
		1	[Default]			
	Programming Notes					
	This bit is for HW internal use to context save /restore Tail Pointer Wrap Flag. SW should not program this bit. This bit gets programmed only when Tail Pointer Wrap Mask bit is set.					
	16	Head Pointer Wrap Flag				
		Format:	U1			
			Value	Name		
		0				
		1	[Default]			
	Programming Notes					
	This bit is for HW internal use to context save /restore Head Pointer Wrap Flag. SW should not program this bit. This bit gets programmed only when Head Pointer Wrap Mask bit is set.					
	15:6	Reserved				
		Default Value:	0			
		Format:	PBC			
	5	Reserved				
		Default Value:	0			
		Format:	PBC			
	4	Reserved				
		Default Value:	0			
		Format:	PBC			
	3	Reserved				

OASTATUS - Observation Architecture Status Register

	2	Counter Overflow						
		Format: Select						
<p>This bit is set if any of the counters overflows. This bit can be reset by SW by either soft reset or writing a 1 to it.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0</td><td>[Default]</td></tr> <tr> <td>1</td><td></td></tr> </tbody> </table>			Value	Name	0	[Default]	1	
Value	Name							
0	[Default]							
1								
	1	Buffer Overflow						
		This bit is set when the Tail-pointer - Head pointer > max internal trigger buffer size						
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0h</td><td>[Default]</td></tr> <tr> <td>1</td><td></td></tr> </tbody> </table>	Value	Name	0h	[Default]	1	
Value	Name							
0h	[Default]							
1								
	0	Report Lost Error						
		Format: Enable						
		<p>This bit is set if the Report Trigger due to "Internal Report Trigger-1", "Internal Report Trigger-2" or "Timer Triggered" to write out the counter values is dropped, while there is an ongoing report in progress. The report request is ignored and the counter continue to count.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0</td><td>[Default]</td></tr> <tr> <td>1</td><td></td></tr> </tbody> </table>	Value	Name	0	[Default]	1	
Value	Name							
0	[Default]							
1								
		Programming Notes						
		This bit can be reset by SW by either soft reset or writing a 1 to it.						

Observation Architecture Tail Pointer

OATAILPTR - Observation Architecture Tail Pointer				
Register Space:	MMIO: 0/2/0			
Project:	BDW			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Address:	02B10h			
This register allows software to program tail pointer and also indicates current tail pointer value.				
DWord	Bit	Description		
0	31:6	Tail Pointer Virtual address of the internal trigger based buffer that is updated for every 64B cacheline write to memory when reporting via internal report trigger. This pointer will not be updated for MI_REPORT_PERF_COUNT command based writes.		
		<table border="1"> <thead> <tr> <th>Programming Notes</th><th>Project</th></tr> </thead> <tbody> <tr> <td>Before enabling internally triggered performance counter reporting, SW must ensure that this address matches the Report Buffer Offset programmed in OABUFFER register (i.e. tail pointer must start at the beginning of the report buffer). SW must ensure that Tail pointer and the Head Pointer match before enabling internally triggered performance counter reporting.</td><td>BDW</td></tr> </tbody> </table>	Programming Notes	Project
Programming Notes	Project			
Before enabling internally triggered performance counter reporting, SW must ensure that this address matches the Report Buffer Offset programmed in OABUFFER register (i.e. tail pointer must start at the beginning of the report buffer). SW must ensure that Tail pointer and the Head Pointer match before enabling internally triggered performance counter reporting.	BDW			
	5:0	Reserved		
		<table border="1"> <tr> <td>Format:</td><td>PBC</td></tr> </table>	Format:	PBC
Format:	PBC			

Output/Input Stream Payload Capability

OUTSTRMPAY_INSTRMPAY - Output/Input Stream Payload Capability											
Register Space: MMIO: 0/3/0 Project: BDW Default Value: 0x00000030 Access: RO Size (in bits): 32											
Address: 00018h-0001Bh											
DWord	Bit	Description									
0	31:16	INSTRMPAY <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0000h</td><td>[Default]</td><td>0 word</td></tr> <tr> <td>1-00FFh</td><td></td><td>1 word payload - 255 word payload</td></tr> </tbody> </table> <p>Programming Notes</p> <p>Input Stream Payload Capability (INSTRMPAY): Indicates maximum number of words per frame for any single input stream. This measurement is in 16 bit word quantities per 48 kHz frame. 24 Words (48B) is the maximum supported, therefore a value of 18h is reported in this register. Software must ensure that a format which would cause more words per frame than indicated is not programmed into the Input Stream Descriptor register.</p>	Value	Name	Description	0000h	[Default]	0 word	1-00FFh		1 word payload - 255 word payload
Value	Name	Description									
0000h	[Default]	0 word									
1-00FFh		1 word payload - 255 word payload									
	15:0	OUTSTRMPAY <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0-00FFh</td><td></td><td>0 words - 255 word payload</td></tr> <tr> <td>0030h</td><td>[Default]</td><td></td></tr> </tbody> </table>	Value	Name	Description	0-00FFh		0 words - 255 word payload	0030h	[Default]	
Value	Name	Description									
0-00FFh		0 words - 255 word payload									
0030h	[Default]										

Output Payload and Input payload Capability

OUTPAY_INPAY - Output Payload and Input payload Capability

Register Space:	MMIO: 0/3/0										
Project:	BDW										
Default Value:	0x003C001D										
Access:	RO										
Size (in bits):	32										
Address:	00004h-00007h										
DWord	Bit	Description									
0	31:16	<p>Input Payload</p> <p>Indicates the total input payload available on the link. This does not include bandwidth used for command and control. This measurement is in 16-bit Word quantities per 48-kHz frame. The default link clock speed of 24.000 MHz provides 500 bits per frame, or 31.25 Words. 36 bits (2.25 Words) are used for command and control, leaving 29 words for payload. This measurement is on a per-codec basis.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>003Ch</td><td>[Default]</td><td></td></tr> <tr> <td>0-FFh</td><td></td><td>0000h: 0 Words 0001h: 1 Word payload ... 0003Ch: 60 Word payload [Default] ... 00FFh: 255 Word payload</td></tr> </tbody> </table>	Value	Name	Description	003Ch	[Default]		0-FFh		0000h: 0 Words 0001h: 1 Word payload ... 0003Ch: 60 Word payload [Default] ... 00FFh: 255 Word payload
Value	Name	Description									
003Ch	[Default]										
0-FFh		0000h: 0 Words 0001h: 1 Word payload ... 0003Ch: 60 Word payload [Default] ... 00FFh: 255 Word payload									
	15:0	<p>Output payload</p> <p>Indicates the total output payload available on the link. This does not include bandwidth used for command and control. This measurement is in 16-bit Word quantities per 48-kHz frame. The default link clock speed of 24.000 MHz (the data is double pumped) provides 1000 bits per frame, or 62.5 Words in total. Forty bits (2.5 Words) are used for command and control, leaving 60 Words available for data payload. Note that this value does not reflect any bandwidth increase due to support for multiple SDO lines.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>001Dh</td><td>[Default]</td><td></td></tr> <tr> <td>0-FFh</td><td>OUTPAY</td><td>0000h: 0 Words 0001h: 1 Word payload ... 003Ch: 60 Word payload ... 00FFh: 255 Word payload</td></tr> </tbody> </table>	Value	Name	Description	001Dh	[Default]		0-FFh	OUTPAY	0000h: 0 Words 0001h: 1 Word payload ... 003Ch: 60 Word payload ... 00FFh: 255 Word payload
Value	Name	Description									
001Dh	[Default]										
0-FFh	OUTPAY	0000h: 0 Words 0001h: 1 Word payload ... 003Ch: 60 Word payload ... 00FFh: 255 Word payload									

Output Stream Descriptor Buffer Descriptor List Pointer Lower

SBDPL - Output Stream Descriptor Buffer Descriptor List Pointer Lower		
Register Space: MMIO: 0/3/0 Project: BDW Default Value: 0x00000000 Access: R/W Size (in bits): 32		
Address:		00098h-0009Bh
Name:		Output Stream Descriptor 1 Buffer Descriptor List Pointer Lower
ShortName:		SBDPL_1
Address:		000B8h-000BBh
Name:		Output Stream Descriptor 2 Buffer Descriptor List Pointer Lower
ShortName:		SBDPL_2
Address:		000D8h-000DBh
Name:		Output Stream Descriptor 3 Buffer Descriptor List Pointer Lower
ShortName:		SBDPL_3
DWord	Bit	Description
0	31:7	Buffer Descriptor List Lower Base Address
		Default Value: 0000000h Access: R/W Variant
	6:1	BDLLBASE LOWER BITS Default Value: 00h Access: RO Hardwired to 0. Forces alignment on 128B boundaries.
0	0	Reserved

Output Stream Descriptor Buffer Descriptor List Pointer Upper

SDBDPU - Output Stream Descriptor Buffer Descriptor List Pointer Upper		
Register Space: MMIO: 0/3/0 Project: BDW Default Value: 0x00000000 Access: R/W Size (in bits): 32		
Address:		0009Ch-0009Fh
Name:		Output Stream Descriptor 1 Buffer Descriptor List Pointer Upper
ShortName:		SDBDPU_1
Address:		000BCh-000BFh
Name:		Output Stream Descriptor 2 Buffer Descriptor List Pointer Upper
ShortName:		SDBDPU_2
Address:		000DCh-000DFh
Name:		Output Stream Descriptor 3 Buffer Descriptor List Pointer Upper
ShortName:		SDBDPU_3
DWord	Bit	Description
0	31:0	Buffer Descriptor List Upper Base Address Upper 32-bit address of the Buffer Descriptor List. This value should only be modified when the RUN bit is '0' or the DMA transfer may be corrupted.

Output Stream Descriptor Control and Status

SDCTL_STS - Output Stream Descriptor Control and Status												
Register Space: MMIO: 0/3/0 Project: BDW Default Value: 0x00040000 Access: R/W Size (in bits): 32												
Address:		00080h-00083h										
Name:		Output Stream Descriptor 1 Control and Status										
ShortName:		SDCTL_STS_1										
Address:		000A0h-000A3h										
Name:		Output Stream Descriptor 2 Control and Status										
ShortName:		SDCTL_STS_2										
Address:		000C0h-000C3h										
Name:		Output Stream Descriptor 3 Control and Status										
ShortName:		SDCTL_STS_3										
DWord	Bit	Description										
0	31:30	Reserved <table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ								
Format:	MBZ											
29	FIFO Ready <table border="1"> <tr> <td>Access:</td><td>RO Variant</td></tr> </table> <p>For output streams, the controller hardware will set this bit to a 1 while the output DMA FIFO contains enough data to maintain the stream on then link. This bit defaults to 0 on reset because the FIFO is cleared on a reset.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Disable [Default]</td><td>See Description</td></tr> <tr> <td>1b</td><td>Enable</td><td>See Description</td></tr> </tbody> </table>	Access:	RO Variant	Value	Name	Description	0b	Disable [Default]	See Description	1b	Enable	See Description
Access:	RO Variant											
Value	Name	Description										
0b	Disable [Default]	See Description										
1b	Enable	See Description										
28	Descriptor Error <table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Hardwired to '0'. No memory errors are tracked.</p>	Default Value:	0b	Access:	RO							
Default Value:	0b											
Access:	RO											

SDCTL_STS - Output Stream Descriptor Control and Status

	FIFO Error													
27	Default Value: Access:	0b R/WC												
	Programming Notes													
	Set when a FIFO error occurs. Bit is cleared by writing a 1 to this bit position. This bit is set even if an interrupt is not enabled. For an output stream, this indicates a FIFO under run when there are still buffers to send. The hardware should not transmit anything on the link for the associated stream if there is not valid data to send.													
26	Buffer Completion Interrupt Status													
	Default Value: Access:	0b R/WC												
	Programming Notes													
	This bit is set to 1 by the hardware after the last sample of a buffer has been processed, AND if the Interrupt on Completion (IOC) bit is set in the command byte of the buffer descriptor. It remains active until software clears it by writing a 1 to this bit position.													
25:24	Reserved													
	Format:	MBZ												
23:20	Stream Number													
	Access:	R/W												
	This value reflects the Tag associated with the data being transferred on the link. When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.													
	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> <th style="text-align: center;">Description</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0000b</td> <td>Reserved [Default]</td> <td>Indicates Unused</td> </tr> <tr> <td style="text-align: center;">0001b</td> <td>Stream 1</td> <td></td> </tr> <tr> <td style="text-align: center;">0010b-1111b</td> <td>Stream 2- Stream 15</td> <td></td> </tr> </tbody> </table>		Value	Name	Description	0000b	Reserved [Default]	Indicates Unused	0001b	Stream 1		0010b-1111b	Stream 2- Stream 15	
Value	Name	Description												
0000b	Reserved [Default]	Indicates Unused												
0001b	Stream 1													
0010b-1111b	Stream 2- Stream 15													
19	Bidirectional Direction Control													
	Default Value: Access:	0b RO												
	This bit is only meaningful for Bidirectional streams. Therefore this bit is hardwired to 0.													
18	Traffic Priority													
	Default Value: Access:	1b RO												
	Hardwired to 1 indicating that all streams will use VC1 if it is enabled throughout the PCI Express registers.													

SDCTL_STS - Output Stream Descriptor Control and Status

	17:16	Stripe Control											
		Default Value:	00b										
		Access:	RO										
For output streams it controls the number of SDO signals to stripe data across. Only one SDO is supported in dHDA. Therefore it is hardwired to 0's.													
	15:5	Reserved	Format:	MBZ									
	4	Error Interrupt Enable											
		Access:	R/W										
Implemented as RW but no functionality as memory errors are not tracked.													
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Disable [Default]</td> <td>See Description</td> </tr> <tr> <td>1h</td> <td>Enable</td> <td>See Description</td> </tr> </tbody> </table>	Value	Name	Description	0h	Disable [Default]	See Description	1h	Enable	See Description		
Value	Name	Description											
0h	Disable [Default]	See Description											
1h	Enable	See Description											
	3	FIFO Error Interrupt Enable											
		Access:	R/W										
This bit controls whether the occurrence of a FIFO error (under-run for output) will cause an interrupt or not. If this bit is not set, bit 3 in the Status register will be set, but the interrupt will not occur. Either way, the samples will be dropped.													
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Disable [Default]</td> <td>See Description</td> </tr> <tr> <td>1h</td> <td>Enable</td> <td>See Description</td> </tr> </tbody> </table>	Value	Name	Description	0h	Disable [Default]	See Description	1h	Enable	See Description		
Value	Name	Description											
0h	Disable [Default]	See Description											
1h	Enable	See Description											
	2	Interrupt On Completion Enable											
		Access:	R/W										
This bit controls whether or not an interrupt occurs when a buffer completes with the IOC bit set in its descriptor. If this bit is not set, bit 2 in the Status register will be set, but the interrupt will not occur.													
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Disable [Default]</td> <td>See Description</td> </tr> <tr> <td>1h</td> <td>Enable</td> <td>See Description</td> </tr> </tbody> </table>	Value	Name	Description	0h	Disable [Default]	See Description	1h	Enable	See Description		
Value	Name	Description											
0h	Disable [Default]	See Description											
1h	Enable	See Description											

SDCTL_STS - Output Stream Descriptor Control and Status

	1	Stream Run										
		Access:	R/W									
<p>When set to 1 the DMA engine associated with this output stream will be enabled to transfer data in the main memory to FIFO. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this output stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped.</p>												
<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0h</td><td>Disable [Default]</td><td>See Description</td></tr> <tr> <td>1h</td><td>Enable</td><td>See Description</td></tr> </tbody> </table>				Value	Name	Description	0h	Disable [Default]	See Description	1h	Enable	See Description
Value	Name	Description										
0h	Disable [Default]	See Description										
1h	Enable	See Description										
Programming Notes												
<p>Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.</p>												
	0	Stream Reset										
		Default Value:	0b									
		Access:	R/W Variant									
Programming Notes												
<p>Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.</p>												

Output Stream Descriptor Cyclic Buffer Length

SDCBL - Output Stream Descriptor Cyclic Buffer Length										
DWord	Bit	Description								
0	31:0	<p>Cyclic Buffer Length</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td colspan="2">): Indicates the number of bytes in the complete cyclic buffer. CBL must represent an integer number of samples. Link Position in Buffer (LPIB) will be reset when it reaches this value.</td> </tr> <tr> <td align="center" colspan="2">Programming Notes</td></tr> <tr> <td align="center" colspan="2">Software may only write to this register after Global Reset, Controller Reset, or Stream Reset has occurred. This value should only be modified when the RUN bit is '0'. Once the RUN bit has been set to enable the engine, software must not write to this register until after the next reset is asserted, or transfers may be corrupted.</td></tr> </table>	Default Value:	00000000h): Indicates the number of bytes in the complete cyclic buffer. CBL must represent an integer number of samples. Link Position in Buffer (LPIB) will be reset when it reaches this value.		Programming Notes		Software may only write to this register after Global Reset, Controller Reset, or Stream Reset has occurred. This value should only be modified when the RUN bit is '0'. Once the RUN bit has been set to enable the engine, software must not write to this register until after the next reset is asserted, or transfers may be corrupted.	
Default Value:	00000000h									
): Indicates the number of bytes in the complete cyclic buffer. CBL must represent an integer number of samples. Link Position in Buffer (LPIB) will be reset when it reaches this value.										
Programming Notes										
Software may only write to this register after Global Reset, Controller Reset, or Stream Reset has occurred. This value should only be modified when the RUN bit is '0'. Once the RUN bit has been set to enable the engine, software must not write to this register until after the next reset is asserted, or transfers may be corrupted.										

Output Stream Descriptor FIFO Data and Format

SDFIFOD_FMT - Output Stream Descriptor FIFO Data and Format																					
Register Space: MMIO: 0/3/0 Project: BDW Default Value: 0x000000C0 Access: R/W Size (in bits): 32																					
Address:		00090h-00093h																			
Name:		Output Stream Descriptor 1 FIFO Data and Format																			
ShortName:		SDFIFOD_FMT_1																			
Address:		000B0h-000B3h																			
Name:		Output Stream Descriptor 2 FIFO Data and Format																			
ShortName:		SDFIFOD_FMT_2																			
Address:		000D0h-000D3h																			
Name:		Output Stream Descriptor 3 FIFO Data and Format																			
ShortName:		SDFIFOD_FMT_3																			
DWord	Bit	Description																			
0	31	Reserved <table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ																	
Format:	MBZ																				
30	Sample Base Rate <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0h</td><td>48 [Default]</td><td>48 kHz</td></tr> <tr> <td>1h</td><td>44.1</td><td>44.1 kHz</td></tr> </tbody> </table>	Access:	R/W	Value	Name	Description	0h	48 [Default]	48 kHz	1h	44.1	44.1 kHz									
Access:	R/W																				
Value	Name	Description																			
0h	48 [Default]	48 kHz																			
1h	44.1	44.1 kHz																			
29:27	Sample Base Rate Multiple <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>000b</td><td>[Default]</td><td>48 kHz/44.1 kHz or less</td></tr> <tr> <td>001b</td><td>x2</td><td>96 kHz, 88.2 kHz, 32 kHz</td></tr> <tr> <td>010b</td><td>x3</td><td>144 kHz</td></tr> <tr> <td>011b</td><td>x4</td><td>192 kHz, 176.4 kHz</td></tr> <tr> <td>100b-111b</td><td>Reserved</td><td>N/A</td></tr> </tbody> </table>	Access:	R/W	Value	Name	Description	000b	[Default]	48 kHz/44.1 kHz or less	001b	x2	96 kHz, 88.2 kHz, 32 kHz	010b	x3	144 kHz	011b	x4	192 kHz, 176.4 kHz	100b-111b	Reserved	N/A
Access:	R/W																				
Value	Name	Description																			
000b	[Default]	48 kHz/44.1 kHz or less																			
001b	x2	96 kHz, 88.2 kHz, 32 kHz																			
010b	x3	144 kHz																			
011b	x4	192 kHz, 176.4 kHz																			
100b-111b	Reserved	N/A																			

SDFIFOD_FMT - Output Stream Descriptor FIFO Data and Format

	26:24	Sample Base Rate Divisor				
		Access:		R/W		
Value		Name	Description			
000b		Divide by 1 [Default]	48 kHz, 44.1 kHz			
001b		Divide by 2	24 kHz, 22.05 kHz			
010b		Divide by 3	16 kHz, 32 kHz			
011b		Divide by 4	11.025 kHz)			
100b		Divide by 5	9.6 kHz			
101b		Divide by 6	8 kHz			
110b		Divide by 7	6.875 kHz			
111b		Divide by 8	6 kHz			
	23	Reserved				
		Format:		MBZ		
	22:20	Bits per Sample				
		Access:		R/W		
Value		Name	Description			
000b		8 bits [Default]	The data will be packed in memory in 8-bit containers on 16-bit boundaries			
0001b		16 bits	The data will be packed in memory in 16-bit containers on 16-bit boundaries			
010b		20 bits	The data will be packed in memory in 32-bit containers on 32-bit boundaries			
011b		24 bits	The data will be packed in memory in 32-bit containers on 32-bit boundaries			
100b		32 bits	The data will be packed in memory in 32-bit containers on 32-bit boundaries			
101b-111b		Reserved	N/A			
	19:16	Number of Channels				
		Access:		R/W		
Number of channels in each frame of the stream.						
Value		Name	Description			
0000b-1111b		1-16	0000b = 1 channel in each frame of the stream. [Default] 0001b = 2 channels in each frame of the stream. ... 1111b = 16 channels in each frame of the stream.			

SDFIFOD_FMT - Output Stream Descriptor FIFO Data and Format

	15:0	FIFO Size	
		Default Value:	00C0h
		Access:	R/W Variant
Indicates the maximum number of bytes that could be fetched by the controller at one time. This is the maximum number of bytes that may have been DMA'd into memory but not yet transmitted on the link, and is also the maximum possible value that the PICB count will increase by at one time. It depends on what the Stream parameters are programmed as default.			

Output Stream Descriptor Last Valid Index

SDLVI - Output Stream Descriptor Last Valid Index					
Register Space: MMIO: 0/3/0 Project: BDW Default Value: 0x00000000 Access: R/W Size (in bits): 32					
Address:		0008Ch-0008Fh			
Name:		Output Stream Descriptor 1 Last Valid Index			
ShortName:		SDLVI_1			
Address:		000ACh-000AFh			
Name:		Output Stream Descriptor 2 Last Valid Index			
ShortName:		SDLVI_2			
Address:		000CCh-000CFh			
Name:		Output Stream Descriptor 3 Last Valid Index			
ShortName:		SDLVI_3			
DWord	Bit	Description			
0	31:8	Reserved <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ	
Format:	MBZ				
7:0	Last Valid Index <table border="1"> <tr> <td>Default Value:</td> <td>00h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Programming Notes</p> <p>The value written to this register indicates the index for the last valid Buffer Descriptor in the BDL. After the controller has processed this descriptor, it will wrap back to the first descriptor in the list and continue processing. LVI must be at least 1; i.e., there must be at least two valid entries in the buffer descriptor list before DMA operations can begin. This value should only be modified when the RUN bit is '0'.</p>	Default Value:	00h	Access:	R/W
Default Value:	00h				
Access:	R/W				

Output Stream Descriptor Link Position in Current Buffer

SDLPIB - Output Stream Descriptor Link Position in Current Buffer			
Register Space: MMIO: 0/3/0 Project: BDW Default Value: 0x00000000 Access: RO Variant Size (in bits): 32			
Address:		00084h-00087h	
Name:		Output Stream Descriptor 1 Link Position in Current Buffer	
ShortName:		SDLPIB_1	
Address:		000A4h-000A7h	
Name:		Output Stream Descriptor 2 Link Position in Current Buffer	
ShortName:		SDLPIB_2	
Address:		000C4h-000C7h	
Name:		Output Stream Descriptor 3 Link Position in Current Buffer	
ShortName:		SDLPIB_3	
DWord	Bit	Description	
0	31:0	cLink Position in Buffer Default Value: 00000000h Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register and then wrap to 0.	

Output Stream Descriptor Link Position in Current Buffer Alias

SDLPIBA - Output Stream Descriptor Link Position in Current Buffer Alias								
Register Space: MMIO: 0/3/0 Project: BDW Default Value: 0x00000000 Access: RO Variant Size (in bits): 32								
Address:		02084h-02087h						
Name:		Output Stream Descriptor 1 Link Position in Current Buffer Alias						
ShortName:		SDLPIBA_1						
Address:		020A4h-020A7h						
Name:		Output Stream Descriptor 2 Link Position in Current Buffer Alias						
ShortName:		SDLPIBA_2						
Address:		020C4h-020C7h						
Name:		Output Stream Descriptor 3 Link Position in Current Buffer Alias						
ShortName:		SDLPIBA_3						
DWord	Bit	Description						
0	31:0	Link Position in Buffer Alias This is an alias of the corresponding LPIB register. Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register and then wrap to 0. <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0h</td><td>Disable [Default]</td></tr> <tr> <td>1h</td><td>Enable</td></tr> </tbody> </table>	Value	Name	0h	Disable [Default]	1h	Enable
Value	Name							
0h	Disable [Default]							
1h	Enable							

Outstanding Page Request Allocation

OPRA_0_2_0_PCI - Outstanding Page Request Allocation						
DWord	Bit	Description				
0	31:0	<p>Outstanding Page Request Allocation</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000000000000000000000000000b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>This register contains the number of outstanding page request messages the associated Page Request Interface is allowed to issue.</p>	Default Value:	00000000000000000000000000000000b	Access:	R/W
Default Value:	00000000000000000000000000000000b					
Access:	R/W					

Outstanding Page Request Capacity

OPRC_0_2_0_PCI - Outstanding Page Request Capacity						
Register Space: PCI: 0/2/0 Project: BDW Default Value: 0x00008000 Size (in bits): 32						
Address: 00308h						
Page Request Extended Capability reports support for page-faults on Device-2, compliant to PCI-Express ATS 1.1 Specification						
DWord	Bit	Description				
0	31:0	Outstanding Page Request Capacity <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 15%;">Default Value:</td><td>00000000000000001000000000000000b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>This register contains the number of outstanding page request messages the associated Page Request Interface physically supports. This is the upper limit on the number of pages that can be usefully allocated to the Page Request Interface. Hardwired to 32,768 requests.</p>	Default Value:	00000000000000001000000000000000b	Access:	RO
Default Value:	00000000000000001000000000000000b					
Access:	RO					

PAGE_FAULT_MODE

PAGE_FAULT_MODE - PAGE_FAULT_MODE								
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x00000000 Size (in bits): 32								
Address: 0E454h Name: PAGE_FAULT_MODE ShortName: PAGE_FAULT_MODE Valid Projects: [BDW]								
This is a basic register template								
DWord	Bit	Description						
0	31:8	Reserved						
		Default Value: 0000000000000000b Access: RO						
	7:6	FAULT_MODE						
		Project: BDW Access: R/W						
Fault Model: Applicable only in advanced context "00": Fault & Hang "01": Reserved "10": Reserved "11": Reserved								
	5:0	<table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>00b</td><td>[Default]</td></tr> <tr> <td>01b</td><td></td></tr> </tbody> </table>	Value	Name	00b	[Default]	01b	
Value	Name							
00b	[Default]							
01b								
Reserved								
Project:	BDW							

Page Directory Pointer Descriptor - PDP0/PML4/PASID

PDP0 - Page Directory Pointer Descriptor - PDP0/PML4/PASID

Register Space:	MMIO: 0/2/0
Project:	BDW
Default Value:	0x00000000, 0x00000000
Access:	R/W
Size (in bits):	64
Address:	02270h-02277h
Name:	Page Directory Pointer Descriptor - PDP0/PML4/PASID
ShortName:	PDP0_RCSUNIT
Address:	12270h-12277h
Name:	Page Directory Pointer Descriptor - PDP0/PML4/PASID
ShortName:	PDP0_VCSUNIT0
Address:	1A270h-1A277h
Name:	Page Directory Pointer Descriptor - PDP0/PML4/PASID
ShortName:	PDP0_VECSUNIT
Address:	1C270h-1C277h
Name:	Page Directory Pointer Descriptor - PDP0/PML4/PASID
ShortName:	PDP0_VCSUNIT1
Address:	22270h-22277h
Name:	Page Directory Pointer Descriptor - PDP0/PML4/PASID
ShortName:	PDP0_BCSUNIT
PDP0/PML4/PASID: This register can contain three values which depend on the element descriptor definition.	
PASID[19:0]: Populated in the first 20bits of the register and selected when Advanced Context flag is set in the element descriptor in execlist mode of submission. This is not valid in ring buffer mode of scheduling.	
PML4[38:12]: Pointer to base address of PML4 and selected when Legacy Context flag is set and 64b address support is selected. PDP0[38:12]: Pointer to one of the four page directory pointer (lowest) and defines the first 0-1GB of memory mapping. This is valid when Legacy Context Flag is set and 64bit virtual addressing is not supported. <i>Note: This is a guest physical address.</i>	

Programming Notes

Execlist Based Scheduling: SW should update PDP0/12/3 registers in context image with proper values before submitting the context to HW in execlist mode of scheduling. HW restores these registers as part of context restore to set the PPGTT access accordingly. PPGTT is always enabled in advanced context mode of execlist based scheduling and can be disabled only in legacy context mode. Privilege Access Bit in Element Descriptor controls the PPGTT enabling in legacy context mode.

PDP0 - Page Directory Pointer Descriptor - PDP0/PML4/PASID

Ring Buffer Based Scheduling: A write via MMIO to PDP0_DESCRIPTOR (lower Dword) triggers the Page Directory Restore in HW when PPGTT is enabled. SW should ensure PDP1/2/3 registers are programmed appropriately prior to programming PDP0. PDP0_DESCRIPTOR lower dword should be programmed at the end. Per-Process GTT Enable Bit in GFX_MODE register controls the PPGTT enabling and disabling. Programming Per-Process GTT Enable Bit in GFX_MODE register doesn't enable/disable the PPGTT translation of memory access immediately; the change comes in to affect only when the Page Directory registers are programmed. Programming Per-Process GTT Enable Bit in GFX_MODE register bit must be followed by programming Page Directory Registers in order to enable or disable the PPGTT translation of memory access. PDP* DESCRIPTOR registers must always be programmed through MI_LOAD_REGISTER_IMMEDIATE command in ring buffer with PDP0_DESCRIPTOR lower dword written at the end. PDP0/12/3 registers are context save restored. PDP descriptors are power context save restored in VCS, BCS and VECS engines. PDP descriptors are context save restored per render context in RCS and must be programmed following MI_SET_CONTEXT command, in case of PDP descriptors programmed without context set (MI_SET_CONTEXT) will get lost on C6 entry/exit. PDP descriptor registers should be programmed after ensuring the pipe is completely flushed and TLB's invalidated.

DWord	Bit	Description	
0	63	PD Load Busy	
		Project:	BDW
		Access:	RO
		Format:	Valid
		This read-only field gets set when PDP0 is written to indicating Page Directory Restore activity is in progress and will get reset once the activity is completed.	
	62:0	PDP0 Descriptor	
		Project:	BDW

Page Directory Pointer Descriptor - PDP1

PDP1 - Page Directory Pointer Descriptor - PDP1		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000, 0x00000000	
Access:	R/W	
Size (in bits):	64	
Address:	02278h-0227Fh	
Name:	Page Directory Pointer Descriptor - PDP1	
ShortName:	PDP1_RCSUNIT	
Address:	12278h-1227Fh	
Name:	Page Directory Pointer Descriptor - PDP1	
ShortName:	PDP1_VCSUNIT0	
Address:	1A278h-1A27Fh	
Name:	Page Directory Pointer Descriptor - PDP1	
ShortName:	PDP1_VECSUNIT	
Address:	1C278h-1C27Fh	
Name:	Page Directory Pointer Descriptor - PDP1	
ShortName:	PDP1_VCSUNIT1	
Address:	22278h-2227Fh	
Name:	Page Directory Pointer Descriptor - PDP1	
ShortName:	PDP1_BCSUNIT	
PDP1[38:12]: Pointer to one of the four page directory pointer (lowest+1) and defines the first 1-2GB of memory mapping. This is valid when Legacy Context Flag is set and 64bit virtual addressing is not supported.		
<i>Note: This is a guest physical address.</i>		
DWord	Bit	Description
0	63:0	PDP1 Descriptor

Page Directory Pointer Descriptor - PDP2

PDP2 - Page Directory Pointer Descriptor - PDP2		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000, 0x00000000	
Access:	R/W	
Size (in bits):	64	
Address:	02280h-02287h	
Name:	Page Directory Pointer Descriptor - PDP2	
ShortName:	PDP2_RCSUNIT	
Address:	12280h-12287h	
Name:	Page Directory Pointer Descriptor - PDP2	
ShortName:	PDP2_VCSUNIT0	
Address:	1A280h-1A287h	
Name:	Page Directory Pointer Descriptor - PDP2	
ShortName:	PDP2_VECSUNIT	
Address:	1C280h-1C287h	
Name:	Page Directory Pointer Descriptor - PDP2	
ShortName:	PDP2_VCSUNIT1	
Address:	22280h-22287h	
Name:	Page Directory Pointer Descriptor - PDP2	
ShortName:	PDP2_BCSUNIT	
PDP2[38:12]: Pointer to one of the four page directory pointer (lowest+2) and defines the first 2-3GB of memory mapping. This is valid when Legacy Context Flag is set and 64bit virtual addressing is not supported. <i>Note: This is a guest physical address.</i>		
DWord	Bit	Description
0	63:0	PDP2 Descriptor

Page Directory Pointer Descriptor - PDP3

PDP3 - Page Directory Pointer Descriptor - PDP3		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000, 0x00000000	
Access:	R/W	
Size (in bits):	64	
Address:	02288h-0228Fh	
Name:	Page Directory Pointer Descriptor - PDP3	
ShortName:	PDP3_RCSUNIT	
Address:	12288h-1228Fh	
Name:	Page Directory Pointer Descriptor - PDP3	
ShortName:	PDP3_VCSUNIT0	
Address:	1A288h-1A28Fh	
Name:	Page Directory Pointer Descriptor - PDP3	
ShortName:	PDP3_VECSUNIT	
Address:	1C288h-1C28Fh	
Name:	Page Directory Pointer Descriptor - PDP3	
ShortName:	PDP3_VCSUNIT1	
Address:	22288h-2228Fh	
Name:	Page Directory Pointer Descriptor - PDP3	
ShortName:	PDP3_BCSUNIT	
PDP3[38:12]: Pointer to one of the four page directory pointer (lowest+3) and defines the first 3-4GB of memory mapping. This is valid when Legacy Context Flag is set and 64bit virtual addressing is not supported.		
<i>Note: This is a guest physical address.</i>		
DWord	Bit	Description
0	63:0	PDP3 Descriptor

Page Request Control

PR_CTRL_0_2_0_PCI - Page Request Control						
DWord	Bit	Description				
0	1	<p>Reset</p> <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>When the Enable field is clear, or is being cleared in the same register update that sets this field, writing a 1b to this field, clears the associated implementation dependent page request credit Counter and pending request state for the associated Page Request Interface. No action is initiated if this field is written to 0b or if this field is written with any value when the PRE field is set. Processor graphics does not use this field, and hardwires it as read-only (0).</p>	Default Value:	0b	Access:	RO
Default Value:	0b					
Access:	RO					
0	<p>Page-Request Enable</p> <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>When Set, indicates that the page request interface on the endpoint is allowed to make page requests. If both this field and the Stopped field in Page Request Status register are Clear, then the Page request interface will not issue new page requests, but has outstanding page requests for which page responses is not yet received. When this field transitions from 0 to 1, all the status fields in the Page-Request Status register are cleared. Enabling a page request interface that has not successfully stopped has indeterminate results.</p>	Default Value:	0b	Access:	R/W	
Default Value:	0b					
Access:	R/W					

Page Request Extended Capability Header

PR_EXTCAP_0_2_0_PCI - Page Request Extended Capability Header					
DWord	Bit	Description			
0	31:20	Next Capability Offset			
		<table border="1"> <tr> <td>Default Value:</td><td>00000000000000b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>This is a hardwired pointer to the next item in the capabilities list. Value 000h indicates that this is the end of the PCI-Express Extended capability Linked List.</p>	Default Value:	00000000000000b	Access:
Default Value:	00000000000000b				
Access:	RO				
19:16	Version <table border="1"> <tr> <td>Default Value:</td><td>0001b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Hardwired to capability version 1.</p>	Default Value:	0001b	Access:	RO
Default Value:	0001b				
Access:	RO				
	15:0	Capability ID			
		<table border="1"> <tr> <td>Default Value:</td><td>0000000000010011b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Hardwired to the Page Request Extended Capability ID</p>	Default Value:	0000000000010011b	Access:
Default Value:	0000000000010011b				
Access:	RO				

Page Request Queue Address Register 0

PAGEREQ_QADDR_0 - Page Request Queue Address Register 0						
DWord	Bit	Description				
0	31:12	<p>Page Request Queue Base Register</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>This field points to the base of 4KB aligned invalidation request queue. Hardware may ignore and not implement bits 63:HAW, where HAW is the host address width. Reads of this field return the value that was last programmed to it.</p>	Default Value:	00000h	Access:	R/W
Default Value:	00000h					
Access:	R/W					
	11:3	<p>Reserved</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Default Value:	00000000b	Access:	RO
Default Value:	00000000b					
Access:	RO					
	2:0	<p>Queue Size</p> <table border="1"> <tr> <td>Default Value:</td> <td>000b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>This field specifies the size of the page request queue. A value of X in this field indicates a page request queue of (2X) 4KB pages. The number of entries in the invalidation queue is 2(X+8).</p>	Default Value:	000b	Access:	R/W
Default Value:	000b					
Access:	R/W					

Page Request Queue Address Register 1

PAGEREQ_QADDR_1 - Page Request Queue Address Register1						
DWord	Bit	Description				
0	31:0	<p>Page Request Queue Base Register</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>This field points to the base of 4KB aligned invalidation request queue. Hardware may ignore and not implement bits 63:HAW, where HAW is the host address width. Reads of this field return the value that was last programmed to it.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

Page Request Queue Head Register 0

PAGEREQ_QHEAD_0 - Page Request Queue Head Register 0			
Register Space: MMIO: 0/2/0			
Project: BDW			
Default Value: 0x00000000			
Size (in bits): 32			
Address: 0F0C0h			
Register indicating the page request queue head.			
DWord	Bit	Description	
0	31:19	Reserved	
		Default Value:	000000000000000b
		Access:	RO
	18:4	Queue Head	
		Default Value:	000000000000000b
		Access:	R/W
Specifies the offset (128-bit aligned) to the page request queue for the command that is processed next by software. GFX implementation: GFX has to read the content of the Head pointer as tail pointer gets close to it to prevent overflows in page request queue.			
	3:0	Reserved	
		Default Value:	0h
		Access:	RO

Page Request Queue Head Register 1

PAGEREQ_QHEAD_1 - Page Request Queue Head Register1								
Register Space:	MMIO: 0/2/0							
Project:	BDW							
Default Value:	0x00000000							
Size (in bits):	32							
Address:	0F0C4h							
Register indicating the page request queue head.								
DWord	Bit	Description						
0	31:0	Page Request Queue Head Register 1 Reserved <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> <tr> <td colspan="2">Bit[63:32]: Reserved.</td></tr> </table>	Default Value:	00000000h	Access:	RO	Bit[63:32]: Reserved.	
Default Value:	00000000h							
Access:	RO							
Bit[63:32]: Reserved.								

Page Request Queue Tail Register 0

PAGEREQ_QTAIL_0 - Page Request Queue Tail Register 0						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	0F0C8h					
Register indicating the page request queue tail.						
DWord	Bit	Description				
0	31:1	<p>Queue Tail</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000000000000000000000000000b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Bit[31:19]: Reserved. Bit[18:4]: Specifies the offset (128-bit aligned) to the page request queue for the request that is written next by hardware. GFX Implementation: GT manages the tail pointer value as part of page requests. The value can be acquired as part of the RC6 exit. Bit[3:1]: Reserved.</p>	Default Value:	00000000000000000000000000000000b	Access:	R/W
Default Value:	00000000000000000000000000000000b					
Access:	R/W					
0	0	<p>Valid Bit</p> <table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>This bit can only be cleared by SW, which also clears the other fields.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					

Page Request Queue Tail Register 1

PAGEREQ_QTAIL_1 - Page Request QueueTailRegister1								
Register Space: MMIO: 0/2/0								
DWord	Bit	Description						
0	31:0	Page Request Queue Tail Register 1 Reserved <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> <tr> <td colspan="2">Bit[63:32]: Reserved.</td></tr> </table>	Default Value:	00000000h	Access:	RO	Bit[63:32]: Reserved.	
Default Value:	00000000h							
Access:	RO							
Bit[63:32]: Reserved.								

Page Request Status

PR_STATUS_0_2_0_PCI - Page Request Status						
DWord	Bit	Description				
0	8	<p>Stopped</p> <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>When this field is Set, the associated page request interface has stopped issuing additional Page requests and that all previously issued Page requests have completed. When this field is clear the associate Page request interface either has not stopped or has stopped issuing new Page requests but has outstanding Page requests.</p>	Default Value:	0b	Access:	RO
Default Value:	0b					
Access:	RO					
7:2	<p>Reserved</p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ			
Format:	MBZ					
1	<p>Unexpected Page Request Group Index</p> <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W One Clear</td> </tr> </table> <p>When Set, indicates the function received a PRG response message containing a PRG index that has no matching request, a response failure. This field is Set by the Function and cleared when a 1b is written to the field.</p>	Default Value:	0b	Access:	R/W One Clear	
Default Value:	0b					
Access:	R/W One Clear					
0	<p>Response Failure</p> <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W One Clear</td> </tr> </table> <p>When Set, indicates the function received a PRG response message indicating a response failure. The function expects no further response from the host (any received are ignored). This field is Set by the Function and cleared when a 1b is written to this field.</p>	Default Value:	0b	Access:	R/W One Clear	
Default Value:	0b					
Access:	R/W One Clear					

PAK_Stream-Out Report (Errors)

PAK_ERR - PAK_Stream-Out Report (Errors)		
DWord	Bit	Description
0	31:22	Reserved Format: MBZ
	21	Incorrect IntraMBFlag in I-slice(AVCf)
	20	Out of Range Symbol Code(AVC/mpeg2)
	19	Incorrect MBType(AVC/mpeg2)
	18	Motion Vectors are not inside the frame boundary(mpeg2)
	17	Scale code is zero(mpeg2)
	16	Incorrect DCTtype for given motionType(mpeg2)
	15:8	MB Y-position This field indicates Macro Block(MB) Y- position where an error occurred while encoding.
	7:0	MB X-position This field indicates Macro Block(MB) X- position where an error occurred while encoding.

PAK_Stream-Out Report (Warnings)

PAK_WARN - PAK_Stream-Out Report (Warnings)		
DWord	Bit	Description
0	31:22	Reserved
		Project: All
		Format: MBZ
	21	Skip Run > 8192 (AVC)
	20	Incorrect SkipMB (AVC and mpeg2)
	19	Incorrect MV difference for dual-prime MB (mpeg2)
	18	End of Slice signal missing on last MB of a Row(mpeg2)
	17	Incorrect DCT type for field picture
	16	MVs are not within defined range by fcode
15:8	MB Y-position	
	MB X-position	

PAK Report Running Status

PAK_REPORT_STAT - PAK Report Running Status										
Register Space: MMIO: 0/2/0 Project: BDW Source: VideoCS Default Value: 0x00000000 Access: RO Size (in bits): 32 Trusted Type: 1										
Address:		128ECh								
Valid Projects:		[BDW]								
Address: 1C8ECh Valid Projects: [BDW:GT3]										
DWord	Bit	Description								
0	31:1	Reserved								
	0	PAK Status <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0</td><td></td><td>PAK engine is IDLE</td></tr> <tr> <td>1</td><td></td><td>PAK engine is currently generating bit stream.</td></tr> </tbody> </table>	Value	Name	Description	0		PAK engine is IDLE	1	
Value	Name	Description								
0		PAK engine is IDLE								
1		PAK engine is currently generating bit stream.								

PAL_EXT_GC_MAX

PAL_EXT_GC_MAX					
Register Space:		MMIO: 0/2/0			
Project:		BDW			
Default Value:		0x0007FFFF, 0x0007FFFF, 0x0007FFFF			
Access:		R/W			
Size (in bits):		96			
Address: 4A420h-4A42Bh Name: Pipe A Extended Gamma Correction Max ShortName: PAL_EXT_GC_MAX_A_* Valid Projects: BDW Power: Always on Reset: soft					
Address: 4AC20h-4AC2Bh Name: Pipe B Extended Gamma Correction Max ShortName: PAL_EXT_GC_MAX_B_* Valid Projects: BDW Power: off/on Reset: soft					
Address: 4B420h-4B42Bh Name: Pipe C Extended Gamma Correction Max ShortName: PAL_EXT_GC_MAX_C_* Valid Projects: BDW Power: off/on Reset: soft					
DWord	Bit	Description			
0	31:19	Reserved			
		Format:	MBZ		
	18:0	Red Ext Max GC Point			
		Default Value:	11111111111111111111b		
		Format:	U3.16		
		The extended point for red color channel gamma correction. This value is represented in a 3.16 format with 3 integer and 16 fractional bits.			
1	31:19	Reserved			
		Format:	MBZ		

PAL_EXT_GC_MAX			
	18:0	Green Ext Max GC Point	
		Default Value:	11111111111111111111b
		Format:	U3.16
The extended point for green color channel gamma correction. This value is represented in a 3.16 format with 3 integer and 16 fractional bits.			
2	31:19	Reserved	Format: MBZ
	18:0	Blue Ext Max GC Point	
		Default Value:	11111111111111111111b
		Format:	U3.16
	The extended point for blue color channel gamma correction. This value is represented in a 3.16 format with 3 integer and 16 fractional bits.		

PAL_GC_MAX

PAL_GC_MAX			
Register Space:		MMIO: 0/2/0	
Project:		BDW	
Default Value:		0x00010000, 0x00010000, 0x00010000	
Access:		R/W	
Size (in bits):		96	
Address:		4A410h-4A41Bh	
Name:		Pipe A Gamma Correction Max	
ShortName:		PAL_GC_MAX_A_*	
Valid Projects:		BDW	
Power:		Always on	
Reset:		soft	
Address:		4AC10h-4AC1Bh	
Name:		Pipe B Gamma Correction Max	
ShortName:		PAL_GC_MAX_B_*	
Valid Projects:		BDW	
Power:		off/on	
Reset:		soft	
Address:		4B410h-4B41Bh	
Name:		Pipe C Gamma Correction Max	
ShortName:		PAL_GC_MAX_C_*	
Valid Projects:		BDW	
Power:		off/on	
Reset:		soft	
DWord	Bit	Description	
0	31:17	Reserved	
		Format:	MBZ
	16:0	Red Max GC Point	
		Default Value:	1000000000000000000b
		Format:	U1.16
The 513th entry for the red color channel of the 12 bit interpolated gamma correction. This value is represented in a 1.16 format with 1 integer and 16 fractional bits.			
Restriction			
The value should always be programmed to be less than or equal to 1.0.			
1	31:17	Reserved	
		Format:	MBZ

PAL_GC_MAX				
	16:0	Green Max GC Point		
		Default Value:	10000000000000000000b	
		Format:	U1.16	
		The 513th entry for the green color channel of the 12 bit interpolated gamma correction. This value is represented in a 1.16 format with 1 integer and 16 fractional bits.		
		Restriction		
		The value should always be programmed to be less than or equal to 1.0.		
2	31:17	Reserved		
	Format:	MBZ		
	Blue Max GC Point			
		Default Value:	1000000000000000b	
		Format:	U1.16	
		The 513th entry for the blue color channel of the 12 bit interpolated gamma correction. This value is represented in a 1.16 format with 1 integer and 16 fractional bits.		
		Restriction		
		The value should always be programmed to be less than or equal to 1.0.		

PAL_LGC

PAL_LGC		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	4A000h-4A3FFh	
Name:	Pipe A Legacy Palette	
ShortName:	PAL_LGC_A_*	
Valid Projects:	BDW	
Power:	Always on	
Reset:	soft	
Address:	4A800h-4ABFFh	
Name:	Pipe B Legacy Palette	
ShortName:	PAL_LGC_B_*	
Valid Projects:	BDW	
Power:	off/on	
Reset:	soft	
Address:	4B000h-4B3FFh	
Name:	Pipe C Legacy Palette	
ShortName:	PAL_LGC_C_*	
Valid Projects:	BDW	
Power:	off/on	
Reset:	soft	
There are 256 instances of this register format per display pipe.		
Restriction		
This register must be written only as a full 32 bit dword. Byte or word writes are not supported.		
DWord	Bit	Description
0	31:24	Reserved Format: <input type="text"/> MBZ
	23:16	Red Legacy Palette Entry Default Value: <input type="text"/> UUh Red legacy palette entry value.

PAL_LGC		
	15:8	Green Legacy Palette Entry Default Value: <input type="text" value="UUh"/> Green legacy palette entry value.
	7:0	Blue Legacy Palette Entry Default Value: <input type="text" value="UUh"/> Blue legacy palette entry value.

PAL_PREC_DATA

PAL_PREC_DATA		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	4A404h-4A407h	
Name:	Pipe A Precision Palette Data	
ShortName:	PAL_PREC_DATA_A	
Valid Projects:	BDW	
Power:	Always on	
Reset:	soft	
Address:	4AC04h-4AC07h	
Name:	Pipe B Precision Palette Data	
ShortName:	PAL_PREC_DATA_B	
Valid Projects:	BDW	
Power:	off/on	
Reset:	soft	
Address:	4B404h-4B407h	
Name:	Pipe C Precision Palette Data	
ShortName:	PAL_PREC_DATA_C	
Valid Projects:	BDW	
Power:	off/on	
Reset:	soft	
These are the precision palette entries used for the 10 bpc, split, and 12 bpc gamma. The Precision Palette Index Value indicates the precision palette location to be accessed through this register.		
Programming Notes		
For 10 bpc, program with the color 10 bit palette entry fraction value. For 12 bpc gamma odd indexes, program with the upper 10 bits of the color palette entry fraction value. For 12 bpc gamma even indexes, program the MSbs with the lower 6 bits of the color palette entry fraction value, then program all 0s in the LSbs. For split gamma indexes 0 to 511, program with the first gamma (before CSC) color 10 bit palette entry fraction value. For split gamma indexes 512 to 1023, program with the second gamma (after CSC) color 10 bit palette entry fraction value.		
Restriction		
This register must be written only as a full 32 bit dword. Byte or word writes are not supported.		
DWord	Bit	Description

PAL_PREC_DATA			
0	31:30	Reserved	
	29:20	Red Precision Palette Entry <table border="1"> <tr> <td>Default Value:</td> <td>UUUUUUUUUUUb</td> </tr> </table> <p>Red precision palette entry value.</p>	Default Value:
Default Value:	UUUUUUUUUUUb		
19:10	Green Precision Palette Entry <table border="1"> <tr> <td>Default Value:</td> <td>UUUUUUUUUUUb</td> </tr> </table> <p>Green precision palette entry value.</p>	Default Value:	UUUUUUUUUUUb
Default Value:	UUUUUUUUUUUb		
9:0	Blue Precision Palette Entry <table border="1"> <tr> <td>Default Value:</td> <td>UUUUUUUUUUUb</td> </tr> </table> <p>Blue precision palette entry value.</p>	Default Value:	UUUUUUUUUUUb
Default Value:	UUUUUUUUUUUb		

PAL_PREC_INDEX

PAL_PREC_INDEX											
Register Space:	MMIO: 0/2/0										
Project:	BDW										
Default Value:	0x00000000										
Access:	R/W										
Size (in bits):	32										
Address:	4A400h-4A403h										
Name:	Pipe A Precision Palette Index										
ShortName:	PAL_PREC_INDEX_A										
Valid Projects:	BDW										
Power:	Always on										
Reset:	soft										
Address:	4AC00h-4AC03h										
Name:	Pipe B Precision Palette Index										
ShortName:	PAL_PREC_INDEX_B										
Valid Projects:	BDW										
Power:	off/on										
Reset:	soft										
Address:	4B400h-4B403h										
Name:	Pipe C Precision Palette Index										
ShortName:	PAL_PREC_INDEX_C										
Valid Projects:	BDW										
Power:	off/on										
Reset:	soft										
This index controls access to the array of precision palette data values.											
DWord	Bit	Description									
0	31	<p>Precision Palette Format This field selects the format of the precision palette data.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Non-split</td><td>10 bpc or 12 bpc gamma format</td></tr> <tr> <td>1b</td><td>Split</td><td>Split gamma format</td></tr> </tbody> </table> <p>Restriction</p> <p>It must be set when reading or writing precision palette entries for split gamma mode. It must be cleared before programming the legacy palette.</p>	Value	Name	Description	0b	Non-split	10 bpc or 12 bpc gamma format	1b	Split	Split gamma format
Value	Name	Description									
0b	Non-split	10 bpc or 12 bpc gamma format									
1b	Split	Split gamma format									

PAL_PREC_INDEX

	30:16	Reserved	Format:	MBZ
	15	Index Auto Increment This field enables the index auto increment.		
			Value	Name
			0b	No Increment
			1b	Auto Increment
	14:10	Reserved	Format:	MBZ
	9:0	Index Value This field indicates the data location to be accessed through the data register. This value can be automatically incremented by a read or a write to the data register if the index auto increment bit is set. When automatically incrementing, the current automatically calculated index value can be read here, and the index will roll over to 0 after reaching the end of the allowed range.	Value	Name
		[0,1023]		

PASID Capability

PASID_CAP_0_2_0_PCI - PASID Capability				
Register Space: PCI: 0/2/0				
Project: BDW				
Default Value: 0x00001400				
Size (in bits): 16				
Address: 00104h				
PASID capability reports support for Process Address Space ID(PASID) on Device-2, compliant to PCI-Express PASID ECN.				
DWord	Bit	Description		
0	12:8	Maximum PASID Width		
		<table border="1"> <tr> <td>Default Value:</td><td>10100b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Indicates the width of the PASID field supported by the Endpoint. Hardwired to 14h to indicate support for all PASID values (20 bits).</p>	Default Value:	10100b
Default Value:	10100b			
Access:	RO			
7:3	Reserved			
	<table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ	
Format:	MBZ			
2	Privilege Mode Supported			
	<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Hardwired to 0, the Endpoint supports operating in Non-privileged mode only, and will never request privileged mode in requests with PASID.</p>	Default Value:	0b	Access:
Default Value:	0b			
Access:	RO			
1	Execute Permission Supported			
	<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Hardwired to 0, the Endpoint will never request Execute permission for requests with PASID.</p>	Default Value:	0b	Access:
Default Value:	0b			
Access:	RO			
0	Reserved			
	<table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ	
Format:	MBZ			

PASID Control

PASID_CTRL_0_2_0_PCI - PASID Control			
Register Space: PCI: 0/2/0 Project: BDW Default Value: 0x00000000 Size (in bits): 8			
Address: 00106h			
Process Address Space ID (PASID) control for Device-2.			
DWord	Bit	Description	
0	2	Privileged Mode Enable	
	2	Default Value:	0b
	2	Access:	RO
Hardwired to 0, the Endpoint is not permitted to request privileged mode in requests with PASID.			
1	1	Execute Permission Enable	
	1	Default Value:	0b
	1	Access:	RO
Hardwired to 0, the Endpoint is not permitted to request execute permission in requests with PASID.			
0	0	PASID Enable	
	0	Default Value:	0b
	0	Access:	R/W
If Set, the Endpoint is permitted to generate requests with PASID. If Clear, the Endpoint is not permitted to do so. Behavior is undefined if this bit changes value when ATS Enable field in ATS Capability is Set.			

PASID Extended Capability Header

PASID_EXTCAP_0_2_0_PCI - PASID Extended Capability Header						
Register Space:	PCI: 0/2/0					
Project:	BDW					
Default Value:	0x2001001B					
Size (in bits):	32					
Address:	00100h					
PASID capability reports support for Process Address Space ID(PASID) on Device-2, compliant to PCI-Express PASID ECN.						
DWord	Bit	Description				
0	31:20	Next Capability Offset				
		<table border="1"> <tr> <td>Default Value:</td><td>001000000000b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>This is a hardwired pointer to the next item in the capabilities list.</p>	Default Value:	001000000000b	Access:	RO
Default Value:	001000000000b					
Access:	RO					
19:16	Version <table border="1"> <tr> <td>Default Value:</td><td>0001b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Hardwired to capability version 1.</p>	Default Value:	0001b	Access:	RO	
Default Value:	0001b					
Access:	RO					
	15:0	Capability ID <table border="1"> <tr> <td>Default Value:</td><td>0000000000011011b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Hardwired to the PASID Extended Capability ID</p>	Default Value:	0000000000011011b	Access:	RO
Default Value:	0000000000011011b					
Access:	RO					

PAT Index

PAT_INDEX - PAT Index				
DWord	Bit	Description		
0	31:10	Reserved <table border="1"> <tr> <td>Default Value:</td> <td>0000000000000000000000000000000b</td> </tr> </table>	Default Value:	0000000000000000000000000000000b
Default Value:	0000000000000000000000000000000b			
	9:8	Class of Service <table border="1"> <tr> <td>Default Value:</td> <td>00b</td> </tr> </table> <p>This field controls the Class of Service sent to the LLC to determine which sub-set of Ways the surface will be stored in. The allocation of certain LLC ways to different class of service settings is a project dependent decision and listed in the Bspec</p> <ul style="list-style-type: none"> 00: Class0 01: Class1 10: Class2 11: Class3 	Default Value:	00b
Default Value:	00b			
	7:6	Reserved <table border="1"> <tr> <td>Default Value:</td> <td>00b</td> </tr> </table>	Default Value:	00b
Default Value:	00b			
	5:4	LRU AGE <table border="1"> <tr> <td>Default Value:</td> <td>00b</td> </tr> </table> <ul style="list-style-type: none"> 00: Take the age value from Uncore CRs 01: Assign the age of "0" 10: Do not change the age on a hit 11: Assign the age of "3" 	Default Value:	00b
Default Value:	00b			
	3:2	Target Cache <table border="1"> <tr> <td>Default Value:</td> <td>00b</td> </tr> </table> <ul style="list-style-type: none"> 00: eLLC only 01: LLC only 10: LLC/eLLC allowed 11: LLC/eLLC allowed 	Default Value:	00b
Default Value:	00b			
	1:0	Mem Type <table border="1"> <tr> <td>Default Value:</td> <td>11b</td> </tr> </table> <ul style="list-style-type: none"> 00: Uncacheable(UC) 01: Write Combining(WC) 10: Write through(WT) 11: Write back(WB) 	Default Value:	11b
Default Value:	11b			

PAT Index High

PAT_INDEX_H - PAT Index High										
DWord	Bit	Description								
0	31:0	<p>PAT Index High</p> <table border="1"> <tr> <td>Default Value:</td><td>03030303h</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <table border="1"> <thead> <tr> <th>Description</th><th>Project</th></tr> </thead> <tbody> <tr> <td> Bit[31:24]: PAT Index#7: Index#7 definition for page tables. (See bit[7:0] for definition.) Bit[23:16]: PAT Index#6: Index#6 definition for page tables. (See bit[7:0] for definition.) Bit[15:8]: PAT Index#5: Index#5 definition for page tables. (See bit[7:0] for definition.) Bit[7:0]: PAT Index#4: Index#4 definition for page tables. Bit[7:6]: Reserved. Bit[5:4]: (See below.) 00b: Age is 0. 01b: Age is 1. 10b: Age is 2. 11b: Age is 3. Bit[3:2]: (See below.) 00b: eLLC only. 01b: LLC only. 10b: LLC and eLLC allowed. 11b: L3, LLC, and eLLC are allowed. Bit[1:0]: (see below): 00b: Uncacheable (UC). 01b: Write Combining (WC). 10b: Write Through (WT). 11b: Write Back (WB). </td><td>BDW</td></tr> </tbody> </table>	Default Value:	03030303h	Access:	R/W	Description	Project	Bit[31:24]: PAT Index#7: Index#7 definition for page tables. (See bit[7:0] for definition.) Bit[23:16]: PAT Index#6: Index#6 definition for page tables. (See bit[7:0] for definition.) Bit[15:8]: PAT Index#5: Index#5 definition for page tables. (See bit[7:0] for definition.) Bit[7:0]: PAT Index#4: Index#4 definition for page tables. Bit[7:6]: Reserved. Bit[5:4]: (See below.) 00b: Age is 0. 01b: Age is 1. 10b: Age is 2. 11b: Age is 3. Bit[3:2]: (See below.) 00b: eLLC only. 01b: LLC only. 10b: LLC and eLLC allowed. 11b: L3, LLC, and eLLC are allowed. Bit[1:0]: (see below): 00b: Uncacheable (UC). 01b: Write Combining (WC). 10b: Write Through (WT). 11b: Write Back (WB).	BDW
Default Value:	03030303h									
Access:	R/W									
Description	Project									
Bit[31:24]: PAT Index#7: Index#7 definition for page tables. (See bit[7:0] for definition.) Bit[23:16]: PAT Index#6: Index#6 definition for page tables. (See bit[7:0] for definition.) Bit[15:8]: PAT Index#5: Index#5 definition for page tables. (See bit[7:0] for definition.) Bit[7:0]: PAT Index#4: Index#4 definition for page tables. Bit[7:6]: Reserved. Bit[5:4]: (See below.) 00b: Age is 0. 01b: Age is 1. 10b: Age is 2. 11b: Age is 3. Bit[3:2]: (See below.) 00b: eLLC only. 01b: LLC only. 10b: LLC and eLLC allowed. 11b: L3, LLC, and eLLC are allowed. Bit[1:0]: (see below): 00b: Uncacheable (UC). 01b: Write Combining (WC). 10b: Write Through (WT). 11b: Write Back (WB).	BDW									

PAT Index Low

PAT_INDEX_L-PATIndexLow									
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x03030303 Size (in bits): 32									
Address: 040E0h									
DWord	Bit	Description							
0	31:0	PAT Index Low <table border="1"> <tr> <td>Default Value:</td><td>03030303h</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> <tr> <td colspan="2"> Bit[31:24]: PAT Index#3: Index#3 definition for page tables. (See bit[7:0] for definition.) Bit[23:16]: PAT Index#2: Index#2 definition for page tables. (See bit[7:0] for definition.) Bit[15:8]: PAT Index#1: Index#1 definition for page tables. (See bit[7:0] for definition.) Bit[7:0]: PAT Index#0: Index#0 definition for page tables. Bit[7:6]: Reserved. Bit[5:4]: (See below.) 00b: Age is 0. 01b: Age is 1. 10b: Age is 2. 11b: Age is 3. Bit[3:2]: (See below.) 00b: eLLC only. 01b: LLC only. 10b: LLC and eLLC allowed. 11b: L3, LLC, and eLLC are allowed. Bit[1:0]: (see below): 00b: Uncacheable (UC). 01b: Write Combining (WC). 10b: Write Through (WT). 11b: Write Back (WB). </td><td>Project</td></tr> </table>	Default Value:	03030303h	Access:	R/W	Bit[31:24]: PAT Index#3: Index#3 definition for page tables. (See bit[7:0] for definition.) Bit[23:16]: PAT Index#2: Index#2 definition for page tables. (See bit[7:0] for definition.) Bit[15:8]: PAT Index#1: Index#1 definition for page tables. (See bit[7:0] for definition.) Bit[7:0]: PAT Index#0: Index#0 definition for page tables. Bit[7:6]: Reserved. Bit[5:4]: (See below.) 00b: Age is 0. 01b: Age is 1. 10b: Age is 2. 11b: Age is 3. Bit[3:2]: (See below.) 00b: eLLC only. 01b: LLC only. 10b: LLC and eLLC allowed. 11b: L3, LLC, and eLLC are allowed. Bit[1:0]: (see below): 00b: Uncacheable (UC). 01b: Write Combining (WC). 10b: Write Through (WT). 11b: Write Back (WB).		Project
Default Value:	03030303h								
Access:	R/W								
Bit[31:24]: PAT Index#3: Index#3 definition for page tables. (See bit[7:0] for definition.) Bit[23:16]: PAT Index#2: Index#2 definition for page tables. (See bit[7:0] for definition.) Bit[15:8]: PAT Index#1: Index#1 definition for page tables. (See bit[7:0] for definition.) Bit[7:0]: PAT Index#0: Index#0 definition for page tables. Bit[7:6]: Reserved. Bit[5:4]: (See below.) 00b: Age is 0. 01b: Age is 1. 10b: Age is 2. 11b: Age is 3. Bit[3:2]: (See below.) 00b: eLLC only. 01b: LLC only. 10b: LLC and eLLC allowed. 11b: L3, LLC, and eLLC are allowed. Bit[1:0]: (see below): 00b: Uncacheable (UC). 01b: Write Combining (WC). 10b: Write Through (WT). 11b: Write Back (WB).		Project							

PCI Command

PCICMD_0_2_0_PCI - PCI Command					
DWord	Bit	Description			
Register Space: PCI: 0/2/0 Project: BDW Default Value: 0x00000000 Size (in bits): 16					
Address: 00004h					
This 16-bit register provides basic control over the IGD's ability to respond to PCI cycles. The PCICMD Register in the IGD disables the IGD PCI compliant master accesses to main memory.					
0	10	Interrupt Disable			
	Default Value:	0b			
	Access:	R/W			
	FLR Resettable This bit disables the device from asserting INTx#. 0: Enable the assertion of this device's INTx# signal. 1: Disable the assertion of this device's INTx# signal. DO_INTx messages will not be sent to DMI.				
	9	Fast Back-to-Back			
	Default Value:	0b			
	Access:	RO			
	Not Implemented. Hardwired to 0.				
8	8	SERR Enable			
	Default Value:	0b			
	Access:	RO			
	Not Implemented. Hardwired to 0.				
	7	Wait Cycle Control			
	Default Value:	0b			
	Access:	RO			
	Not Implemented. Hardwired to 0.				
6	6	Parity Error Enable			
	Default Value:	0b			
	Access:	RO			
	Not Implemented. Hardwired to 0. Since the IGD belongs to the category of devices that does not corrupt programs or data in system memory or hard drives, the IGD ignores any parity error that it detects and continues with normal operation.				

PCICMD_0_2_0_PCI - PCI Command

		Video Palette Snooping					
	5	<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>This bit is hardwired to 0 to disable snooping.</p>	Default Value:	0b	Access:	RO	
Default Value:	0b						
Access:	RO						
	4	Memory Write and Invalidate Enable <table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Hardwired to 0. The IGD does not support memory write and invalidate commands.</p>	Default Value:	0b	Access:	RO	
Default Value:	0b						
Access:	RO						
	3	Special Cycle Enable <table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>This bit is hardwired to 0. The IGD ignores Special cycles.</p>		Default Value:	0b	Access:	RO
Default Value:	0b						
Access:	RO						
	2	Bus Master Enable <table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>FLR Resettable 0: Disable IGD bus mastering. 1: Enable the IGD to function as a PCI compliant master.</p>	Default Value:	0b	Access:	R/W	
Default Value:	0b						
Access:	R/W						
	1	Memory Access Enable <table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>FLR Resettable This bit controls the IGD's response to memory space accesses. 0: Disable. 1: Enable.</p>	Default Value:	0b	Access:	R/W	
Default Value:	0b						
Access:	R/W						
	0	I/O Access Enable <table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>FLR Resettable This bit controls the IGD's response to I/O space accesses. 0: Disable. 1: Enable.</p>	Default Value:	0b	Access:	R/W	
Default Value:	0b						
Access:	R/W						

PCI Express Cap ID and Control

PXID_PXC - PCI Express Cap ID and Control					
DWord	Bit	Description			
0	31:30	<p>Reserved</p> <table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ	
Format:	MBZ				
29:25	<p>Interrupt Message Number</p> <table border="1"> <tr> <td>Default Value:</td><td>00h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Hardwired to 0.</p>	Default Value:	00h	Access:	RO
Default Value:	00h				
Access:	RO				
24	<p>Slot Implemented</p> <table border="1"> <tr> <td>Default Value:</td><td>0h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Hardwired to 0.</p>	Default Value:	0h	Access:	RO
Default Value:	0h				
Access:	RO				
23:20	<p>Device/Port Type</p> <table border="1"> <tr> <td>Default Value:</td><td>9h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Indicates Root Complex Integrated Endpoint.</p>	Default Value:	9h	Access:	RO
Default Value:	9h				
Access:	RO				
19:16	<p>Capability Version</p> <table border="1"> <tr> <td>Default Value:</td><td>1h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Indicates version #1 PCI Express capability.</p>	Default Value:	1h	Access:	RO
Default Value:	1h				
Access:	RO				
15:8	<p>Next Capability</p> <table border="1"> <tr> <td>Default Value:</td><td>00h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Indicates this is the last structure in the list.</p>	Default Value:	00h	Access:	RO
Default Value:	00h				
Access:	RO				

PXID_PXC - PCI Express Cap ID and Control

	7:0	Cap ID
		Default Value:
		Access:
Indicates this is a PCI Express capability structure.		

PCI Status

PCISTS2_0_2_0_PCI - PCI Status						
DWord	Bit	Description				
0	15	<p>Detected Parity Error</p> <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Since the IGD does not detect parity, this bit is always hardwired to 0.</p>	Default Value:	0b	Access:	RO
Default Value:	0b					
Access:	RO					
	14	<p>Signaled System Error</p> <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>The IGD never asserts SERR#, therefore this bit is hardwired to 0.</p>	Default Value:	0b	Access:	RO
Default Value:	0b					
Access:	RO					
	13	<p>Received Master Abort Status</p> <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>The IGD never gets a Master Abort, therefore this bit is hardwired to 0.</p>	Default Value:	0b	Access:	RO
Default Value:	0b					
Access:	RO					
	12	<p>Received Target Abort Status</p> <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>The IGD never gets a Target Abort, therefore this bit is hardwired to 0.</p>	Default Value:	0b	Access:	RO
Default Value:	0b					
Access:	RO					
	11	<p>Signaled Target Abort Status</p> <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Hardwired to 0. The IGD does not use target abort semantics.</p>	Default Value:	0b	Access:	RO
Default Value:	0b					
Access:	RO					
	10:9	<p>DEVSEL Timing</p> <table border="1"> <tr> <td>Default Value:</td> <td>00b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Hardwired to 00.</p>	Default Value:	00b	Access:	RO
Default Value:	00b					
Access:	RO					

PCISTS2_0_2_0_PCI - PCI Status

	8	Master Data Parity Error Detected		
		Default Value:	0b	
		Access:	RO	
		Since Parity Error Response is hardwired to disabled, and the IGD does not do any parity detection, this bit is hardwired to 0.		
	7	Fast Back-to-Back		
		Default Value:	1b	
		Access:	RO	
		Hardwired to 1. The IGD accepts fast back-to-back when the transactions are not to the same agent.		
	6	User Defined Format		
		Default Value:	0b	
		Access:	RO	
		Hardwired to 0.		
	5	66 MHz PCI Capable		
		Default Value:	0b	
		Access:	RO	
		Hardwired to 0.		
	4	Capability List		
		Default Value:	1b	
		Access:	RO	
		This bit is hardwired to 1 to indicate that the register at 34h provides an offset into the function's PCI Configuration Space containing a pointer to the location of the first item in the list.		
	3	Interrupt Status		
		Default Value:	0b	
		Access:	RO Variant	
		This bit reflects the state of the interrupt in the device. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the devices INTx# signal be asserted.		
	2:0	Reserved		
		Format:	MBZ	

PCU Interrupt Definition

PCU Interrupt Definition						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	444E0h-444EFh					
Name:	PCU Interrupts					
ShortName:	PCU_INTERRUPT					
Valid Projects:	BDW					
Power:	Always on					
Reset:	soft					
This table indicates which events are mapped to each bit of the PCU Interrupt registers.						
0x444E0 = ISR						
0x444E4 = IMR						
0x444E8 = IIR						
0x444EC = IER						
DWord	Bit	Description				
0	31:26	Unused_Int_31_26 <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Project:</td><td style="padding: 2px;">BDW</td></tr> <tr> <td colspan="2" style="padding: 2px;">These interrupts are currently unused.</td></tr> </table>	Project:	BDW	These interrupts are currently unused.	
Project:	BDW					
These interrupts are currently unused.						
25	PCU_Pcode2driver_Mailbox_Event					
24	PCU_THERMAL_Event					
23:0	Unused_Int_23_0 <p>These interrupts are currently unused.</p>					

PCU INTERRUPT ENABLE REGISTER

PCU_INTERRUPT_IER - PCU INTERRUPT ENABLE REGISTER				
Register Space:	MMIO: 0/2/0			
Project:	BDW			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	444ECh-444EFh			
This table indicates which events are mapped to each bit of the GT interrupt 1 register. The IER enabled PCU interrupt IIR sticky bits are ORed together to generate PCU interrupt pending bit in the master interrupt control register.				
DWord	Bit	Description		
0	31:26	UNUSED0 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table>	Access:	R/W
Access:	R/W			
25	PCU_MAILBOX_EVT <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>PCU Pcode 2 driver mailbox event</p>	Access:	R/W	
Access:	R/W			
24	PCU_THERMAL_EVT <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>PCU thermal event</p>	Access:	R/W	
Access:	R/W			
23:0	UNUSED1 <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table>	Access:	R/W	
Access:	R/W			

PCU INTERRUPT IDENTITY REGISTER

PCU_INTERRUPT_IIR - PCU INTERRUPT IDENTITY REGISTER				
Register Space:	MMIO: 0/2/0			
Project:	BDW			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	444E8h-444EBh			
<p>This table indicates which events are mapped to each bit of the GT interrupt 1 register. The IER enabled PCU interrupt IIR sticky bits are ORed together to generate PCU interrupt pending bit in the master interrupt control register.</p>				
DWord	Bit	Description		
0	31:26	UNUSED0 <table border="1"> <tr> <td>Access:</td> <td>R/W One Clear</td> </tr> </table>	Access:	R/W One Clear
Access:	R/W One Clear			
25	PCU_MAILBOX_EVT <table border="1"> <tr> <td>Access:</td> <td>R/W One Clear</td> </tr> </table> <p>PCU Pcode 2 driver mailbox event</p>	Access:	R/W One Clear	
Access:	R/W One Clear			
24	PCU_THERMAL_EVT <table border="1"> <tr> <td>Access:</td> <td>R/W One Clear</td> </tr> </table> <p>PCU thermal event</p>	Access:	R/W One Clear	
Access:	R/W One Clear			
23:0	UNUSED1 <table border="1"> <tr> <td>Access:</td> <td>R/W One Clear</td> </tr> </table>	Access:	R/W One Clear	
Access:	R/W One Clear			

PCU INTERRUPT MASK REGISTER

PCU_INTERRUPT_IMR - PCU INTERRUPT MASK REGISTER					
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x03000000 Size (in bits): 32					
Address: 444E4h-444E7h					
This table indicates which events are mapped to each bit of the GT interrupt 1 register. The IER enabled PCU interrupt IIR sticky bits are ORed together to generate PCU interrupt pending bit in the master interrupt control register.					
DWord	Bit	Description			
0	31:26	UNUSED0 <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table>	Access:	R/W	
Access:	R/W				
25	PCU_MAILBOX_EVT <table border="1"> <tr> <td>Default Value:</td><td>1b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> PCU Pcode 2 driver mailbox event	Default Value:	1b	Access:	R/W
Default Value:	1b				
Access:	R/W				
24	PCU_THERMAL_EVT <table border="1"> <tr> <td>Default Value:</td><td>1b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> PCU thermal event	Default Value:	1b	Access:	R/W
Default Value:	1b				
Access:	R/W				
23:0	UNUSED1 <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table>	Access:	R/W		
Access:	R/W				

PCU INTERRUPT STATUS REGISTER

PCU_INTERRUPT_ISR - PCU INTERRUPT STATUS REGISTER		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	444E0h-444E3h	
<p>This table indicates which events are mapped to each bit of the GT interrupt 1 register. The IER enabled PCU interrupt IIR sticky bits are ORed together to generate PCU interrupt pending bit in the master interrupt control register.</p>		
DWord	Bit	Description
0	31:26	UNUSED0 Access: RO
	25	PCU_MAILBOX_EVT Access: RO PCU Pcode 2 driver mailbox event
	24	PCU_THERMAL_EVT Access: RO PCU thermal event
	23:0	UNUSED1 Access: RO

Pending Head Pointer Register

UHPTR - Pending Head Pointer Register					
Register Space:	MMIO: 0/2/0				
Project:	BDW				
Default Value:	0x00000000				
Access:	R/W				
Size (in bits):	32				
Address:	02134h-02137h				
Name:	Pending Head Pointer Register				
ShortName:	UHPTR_RCSUNIT				
Address:	12134h-12137h				
Name:	Pending Head Pointer Register				
ShortName:	UHPTR_VCSUNIT0				
Address:	1A134h-1A137h				
Name:	Pending Head Pointer Register				
ShortName:	UHPTR_VECSUNIT				
Address:	1C134h-1C137h				
Name:	Pending Head Pointer Register				
ShortName:	UHPTR_VCSUNIT1				
Address:	22134h-22137h				
Name:	Pending Head Pointer Register				
ShortName:	UHPTR_BCSUNIT				
Programming Notes			Source		
Once SW uses UHPTR to preempt the existing workload, should explicitly program MI_SET_CONTEXT to save the preempted context status before submitting the new workload. In case SW doesn't want to save the state of the preempted context, it should at the minimum program RS_PREEMPT_STATUS to 0x0 so that the register status doesn't interfere with the new workloads.			RenderCS		
DWord	Bit	Description			
0	31:3	Head Pointer Address <table border="1"> <tr> <td>Format:</td><td>GraphicsAddress[31:3]</td></tr> </table>		Format:	GraphicsAddress[31:3]
Format:	GraphicsAddress[31:3]				
		Description This register represents the GFX address offset where execution should continue in the ring buffer following execution of a Preemptable Command. Refer to the Preemption section for the list of preemptable commands supported in ring buffer mode of scheduling.			

UHPTR - Pending Head Pointer Register

	2:1	Reserved										
		Format:										
	0	Head Pointer Valid										
		Description										
		<p>This bit is set by the software to request a pre-emption.</p> <p>It is reset by hardware when a Preemptable command is parsed by the command streamer. The hardware uses the head pointer programmed in this register at the time the reset is generated. Refer to the Preemption section for the list of preemptable commands supported in ring buffer mode of scheduling.</p> <p>This bit is treated as set by command streamer only when arbitration is not disabled using MI_ARB_ON_OFF command. Preemption will not occur on MI_ARB_CHEK command when UHPTR is valid if the arbitration is disabled using MI_ARB_ON_OFF command.</p>										
		<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: left; padding: 2px;">Value</th><th style="text-align: left; padding: 2px;">Name</th><th style="text-align: left; padding: 2px;">Description</th></tr> </thead> <tbody> <tr> <td style="text-align: center; padding: 2px;">0</td><td style="text-align: center; padding: 2px;">InValid</td><td style="padding: 2px;">No valid updated head pointer register, resume execution at the current location in the ring buffer</td></tr> <tr> <td style="text-align: center; padding: 2px;">1</td><td style="text-align: center; padding: 2px;">Valid</td><td style="padding: 2px;">Indicates that there is an updated head pointer programmed in this register</td></tr> </tbody> </table>		Value	Name	Description	0	InValid	No valid updated head pointer register, resume execution at the current location in the ring buffer	1	Valid	Indicates that there is an updated head pointer programmed in this register
Value	Name	Description										
0	InValid	No valid updated head pointer register, resume execution at the current location in the ring buffer										
1	Valid	Indicates that there is an updated head pointer programmed in this register										

Performance Counter 1 LSB

PERFCNT1_LSB - Performance Counter 1 LSB				
Register Space:	MMIO: 0/2/0			
Project:	BDW			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	091B8h			
<p>GT implements 2 general purpose counters each with 44-bits, each counter can be programmed to count one main event out of set of events (see the event list). Some events are simple duration events and some are edge detects (0=>1 transition is counted). The nature of the event is also programmed to the register that allocates the counter value.</p>				
DWord	Bit	Description		
0	31:0	<p>Counter Value (LSB - 31:0 of 43:0)</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td><td style="padding: 2px; text-align: right;">RO</td></tr> </table> <p>The Counter Value: This is the field where the counter value can be observed via a simple read to the register.</p>	Access:	RO
Access:	RO			

Performance Counter 1 MSB

PERFCNT1_MSB - Performance Counter 1 MSB				
DWord	Bit	Description		
0	31	<p>Counter 1 Enable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Counter#1 Enable. 0: Counter is disabled. The count value is not deterministic. 1: Counter is enabled. Once enabled, the counter is activated if the global enable (from NCU) is also asserted.</p>	Access:	R/W
Access:	R/W			
30	<p>Overflow Enable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Overflow Enable. 0: Overflow reporting is enabled. 1: Overflow reporting is disabled.</p>	Access:	R/W	
Access:	R/W			
29	<p>Edge Detect</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Edge Detect: 0: Edge detect is enabled. 1: Edge detect is disabled.</p>	Access:	R/W	
Access:	R/W			
28	<p>Counter Clear</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Counter Clear.</p>	Access:	R/W	
Access:	R/W			
27:20	<p>Event Selection</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Event Selection: The event list (see attached). Used as a MUX control to select the event to Counter.</p>	Access:	R/W	
Access:	R/W			

PERFCNT1_MSB - Performance Counter 1 MSB		
	19:12	RSVD Access: RO
	11:0	Counter Value (MSB - 43:32 of 43:0) Access: RO The Counter Value: This is the field where the counter value can be observed via a simple read to the register.

Performance Counter 2 LSB

PERFCNT2_LSB - Performance Counter2LSB				
DWord	Bit	Description		
0	31:0	<p>Counter Value (LSB - 31:0 of 43:0)</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px; text-align: right;">RO</td> </tr> </table> <p>The Counter Value: This is the field where the counter value can be observed via a simple read to the register.</p>	Access:	RO
Access:	RO			

Performance Counter 2 MSB

PERFCNT2_MSB - Performance Counter 2 MSB				
DWord	Bit	Description		
0	31	<p>Counter 2 Enable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Counter#2 Enable. 0: Counter is disabled. The count value is not deterministic. 1: Counter is enabled. Once enabled, the counter is activated if the global enable (from NCU) is also asserted.</p>	Access:	R/W
Access:	R/W			
	30	<p>Overflow Enable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Overflow Enable. 0: Overflow reporting is enabled. 1: Overflow reporting is disabled.</p>	Access:	R/W
Access:	R/W			
	29	<p>Edge Detect</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Edge Detect. 0: Edge detect is enabled. 1: Edge detect is disabled.</p>	Access:	R/W
Access:	R/W			
	28	<p>Counter Clear</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Counter Clear.</p>	Access:	R/W
Access:	R/W			
	27:20	<p>Event Selection</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Event Selection: The event list (see attached). Used as a MUX control to select the event to Counter.</p>	Access:	R/W
Access:	R/W			

PERFCNT2_MSB - Performance Counter 2 MSB

	19:12	RSVD
		Access: RO
	11:0	Counter Value (MSB - 43:32 of 43:0)
		Access: RO The Counter Value: This is the field where the counter value can be observed via a simple read to the register.

Performance Matrix Events LSB

PERFMATRIX LSB - Performance Matrix Events LSB			
Register Space: MMIO: 0/2/0			
Project: BDW			
Default Value: 0x00000000			
Size (in bits): 32			
Address: 091C8h			
Performance Matrix Events			
DWord	Bit	Description	
0	31	NONE - No Details as to Snoop related infor	
	31	<table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>NONE - No Details as to Snoop related infor.</p>	Access:
Access:	R/W		
30	NID7		
30	<table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>NID 7.</p>	Access:	R/W
Access:	R/W		
29	NID 6		
29	<table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>NID 6.</p>	Access:	R/W
Access:	R/W		
28	NID 5		
28	<table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>NID 5.</p>	Access:	R/W
Access:	R/W		
27	27	NID 4	
	27	<table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>NID 4.</p>	Access:
Access:	R/W		
26	26	NID 3	
	26	<table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>NID 3.</p>	Access:
Access:	R/W		
25	25	NID 2	
	25	<table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>NID 2.</p>	Access:
Access:	R/W		

PERFMATRIX LSB - Performance Matrix Events LSB

	24	NID1
		Access: R/W NID 1.
	23	NID0
		Access: R/W NID 0.
	22	Local Node
		Access: R/W Local Node.
	21	F-STATE
		Access: R/W F-STATE.
	20	S-State
		Access: R/W S-STATE.
	19	E-STATE
		Access: R/W E-STATE.
	18	M-STATE
		Access: R/W M-STATE.
	17	No Supplier Details
		Access: R/W No Supplier Details.
	16	Snoop Response from Uncore
		Access: R/W Account for any snoop response from Uncore.
	15	IDI requests
		Access: R/W Any - any requests that crosses IDI.

PERFMATRIX LSB - Performance Matrix Events LSB

	14:12	ECORSVD
		Access: R/W ECORSVD - For future changes.
	11	WCIL AND WCILF
		Access: R/W Write Combining.
	10	LOCK
		Access: R/W Locks - count locks & split lock requests.
	9	MLC Prefetch to LLC - Code
		Access: R/W MLC prefetch to LLC - Code.
	8	LLCRFO
		Access: R/W MLC prefetch to LLC - RFO.
	7	MLC Prefetch to LLC - Data
		Access: R/W MLC prefetch to LLC - Load (exclude LRUhints).
	6	MPL RFOs
		Access: R/W PF Ifetch = MPL Fetches.
	5	PF Ifetch
		Access: R/W PF Ifetch = MPL Fetches.
	4	MPL Reads
		Access: R/W PF Data Rd = MPL Reads.
	3	Write Back
		Access: R/W Writeback = MLC_EVICT/DCUWB.

PERFMATRIX LSB - Performance Matrix Events LSB

	2	Demand Ifetch
		Access: R/W Demand Ifetch = IFU Fetches.
	1	Demand RFO
		Access: R/W Demand RFO = DCU RFOs.
	0	Demand Data Rd
		Access: R/W Demand Data Rd = DCU reads (exclude partials).

Performance Matrix Events MSB

PERFMATRIX_MSB - Performance Matrix Events MSB				
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x00000000 Size (in bits): 32				
Address: 091CCh				
Performance Matrix Events				
DWord	Bit	Description		
0	31:6	RSVD <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
Access:	RO			
5	NON Dram <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Non Dram - Target was non-DRAM system address.</p>	Access:	R/W	
Access:	R/W			
4	Hit Modified <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>A snoop was needed and it HitMed in local or remote cache. HitM denotes a cache-line was modified before snoop effect. This includes:</p> <ul style="list-style-type: none"> • Snoop HitM w/ Invalidation and WB (LLC miss, CRD/DRD) • Snoop Forward Modified w/ Invalidation (LLC Hit/Miss, RFO) • Snoop MtoS (LLC Hit, CRD/DRD) 	Access:	R/W	
Access:	R/W			
3	Hit with Forward <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>A snoop was needed and data was Forwarded from a remote socket:</p> <ul style="list-style-type: none"> • Snoop Forward Clean, Left Shared (LLC Miss, CRD/DRD) 	Access:	R/W	
Access:	R/W			
2	Hit No Forward <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>A snoop was needed and it Hits in at least one snooped cache. Hit denotes a cache-line was valid before snoop effect. This includes:</p> <ul style="list-style-type: none"> • Snoop Hit w/ Invalidation (LLC Hit, RFO) • Snoop Hit, Left Shared (LLC Hit/Miss, CRD/DRD) • Snoop Forward Clean w/ Invalidation (LLC Miss, RFO) 	Access:	R/W	
Access:	R/W			

PERFMATRIX_MSB - Performance Matrix Events MSB

	1	SNOOP Miss	
		Access:	R/W
		A snoop was need and it missed all snooped caches: <ul style="list-style-type: none"> • For LLC Hit, ResHitl was returned by all cores • For LLC Miss, Rspl was returned by all sockets 	
	0	NO Snoop Was needed	
		Access:	R/W
		No snoop was neeeded to satisfy the request.	

PF_CTRL

PF_CTRL		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Access:	Double Buffered	
Size (in bits):	32	
Double Buffer	Start of vertical blank after armed	
Update Point:		
Double Buffer Armed Write to PF_WIN_SZ		
By:		
Address:	68080h-68083h	
Name:	PF A Control	
ShortName:	PF_CTRL_A	
Power:	Always on	
Reset:	soft	
Address:	68880h-68883h	
Name:	PF B Control	
ShortName:	PF_CTRL_B	
Power:	off/on	
Reset:	soft	
Address:	69080h-69083h	
Name:	PF C Control	
ShortName:	PF_CTRL_C	
Power:	off/on	
Reset:	soft	
The panel fitter is used to scale the pipe output from the pipe source size to the pipe active size. Each panel fitter is tied to a pipe. All panel fitters are capable of using 7x5 tap filtering. When the horizontal source size is less than or equal to 2048 pixels, the panel fitter uses 7x5 tap filtering. When the horizontal source size is greater than 2048 pixels, the panel fitter uses 3x3 tap filtering. When the horizontal source size is greater than 4096 pixels, the panel fitter cannot be enabled.		
Restriction		
The panel fitter must not be enabled when the horizontal source size is greater than 4096 pixels. When using panel fitter pipe down scaling (pipe source size is larger than panel fitter window size) the maximum supported pixel rate will be reduced by the down scale amount and the watermark for planes on the same pipe has to increase by the down scale amount. Pipe down scaling is only supported up to 1.125 (pipe source size / panel fitter window size) in each direction.		
DWord	Bit	Description

PF_CTRL													
0	31	Enable Pipe Scaler This field enables the panel fitter pipe scaler.											
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Disable</td></tr> <tr> <td>1b</td><td>Enable</td></tr> </tbody> </table>	Value	Name	0b	Disable	1b	Enable					
Value	Name												
0b	Disable												
1b	Enable												
	30:29	Reserved	Format: MBZ										
	28	Reserved											
	27	Reserved											
	26:25	Reserved											
	24:23	FILTER SELECT Selects filter coefficients. The medium coefficients will provide an unfiltered image when the scale factor is 1:1.	<table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>00b</td><td>Medium</td></tr> <tr> <td>01b</td><td>Medium</td></tr> <tr> <td>10b</td><td>Edge Enhance</td></tr> <tr> <td>11b</td><td>Edge Soften</td></tr> </tbody> </table>	Value	Name	00b	Medium	01b	Medium	10b	Edge Enhance	11b	Edge Soften
Value	Name												
00b	Medium												
01b	Medium												
10b	Edge Enhance												
11b	Edge Soften												
	22	Reserved	Format: MBZ										
	21	Reserved											
	20	Reserved											
	19:18	Reserved	Format: MBZ										
	17	Reserved											
	16:0	Reserved	Format: MBZ										

PF_PWR_GATE

PF_PWR_GATE											
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x00000000 Access: Double Buffered Size (in bits): 32 Double Buffer Update Point: Start of vertical blank after armed Double Buffer Armed Write to PF_WIN_SZ By:											
Address:	68060h-68063h										
Name:	PF A Power Gate Control										
ShortName:	PF_PWR_GATE_A										
Power:	Always on										
Reset:	soft										
Address:	68860h-68863h										
Name:	PF B Power Gate Control										
ShortName:	PF_PWR_GATE_B										
Power:	off/on										
Reset:	soft										
Address:	69060h-69063h										
Name:	PF C Power Gate Control										
ShortName:	PF_PWR_GATE_C										
Power:	off/on										
Reset:	soft										
DWord	Bit	Description									
0	31	Reserved									
	30:5	Reserved									
	4:3	Settling Time Time for RAMs in a given filter group to settle after they are powered up. <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>00b</td><td>32 cdclks</td></tr> <tr> <td>01b</td><td>64 cdclks</td></tr> <tr> <td>10b</td><td>96 cdclks</td></tr> <tr> <td>11b</td><td>128 cdclks</td></tr> </tbody> </table>	Value	Name	00b	32 cdclks	01b	64 cdclks	10b	96 cdclks	11b
Value	Name										
00b	32 cdclks										
01b	64 cdclks										
10b	96 cdclks										
11b	128 cdclks										

PF_PWR_GATE												
	2	Reserved Format: MBZ										
	1:0	SLPEN Delay Delay between sleep enables of individual banks of RAMs. <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>00b</td><td>8 cdclks</td></tr> <tr> <td>01b</td><td>16 cdclks</td></tr> <tr> <td>10b</td><td>24 cdclks</td></tr> <tr> <td>11b</td><td>32 cdclks</td></tr> </tbody> </table>	Value	Name	00b	8 cdclks	01b	16 cdclks	10b	24 cdclks	11b	32 cdclks
Value	Name											
00b	8 cdclks											
01b	16 cdclks											
10b	24 cdclks											
11b	32 cdclks											

PF_WIN_POS

PF_WIN_POS		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Access:	Double Buffered	
Size (in bits):	32	
Double Buffer	Start of vertical blank or framestart after armed	
Update Point:		
Double Buffer Armed Write to PF_WIN_SZ		
By:		
Address:	68070h-68073h	
Name:	PF A Window Position	
ShortName:	PF_WIN_POS_A	
Power:	Always on	
Reset:	soft	
Address:	68870h-68873h	
Name:	PF B Window Position	
ShortName:	PF_WIN_POS_B	
Power:	off/on	
Reset:	soft	
Address:	69070h-69073h	
Name:	PF C Window Position	
ShortName:	PF_WIN_POS_C	
Power:	off/on	
Reset:	soft	
Coordinates are determined with a value of (0,0) being the upper left corner of the display device (rotation does not affect this).		
Workaround		
Double-buffering updates at the start of vertical blank and at the framestart. If programming needs to be delayed to the next frame then the register writes have to be delayed to after the framestart of the current frame.		
Restriction		
When pipe scaling is enabled, the scaled output must equal the pipe active area, so Pipe active size = (2 * PF window position) + PF window size.		
DWord	Bit	Description

PF_WIN_POS		
0	31:29	Reserved Format: MBZ
	28:16	XPOS This field specifies the horizontal coordinate in pixels of the upper left most pixel of the panel fitted display window. Restriction The X position must not be programmed to be 1 (28:16=0 0000 0000 0001b).
	15:12	Reserved Format: MBZ
	11:0	YPOS This field specifies the vertical coordinate in lines of the upper left most pixel of the panel fitter display window. Restriction Bit 0 must be zero for interlaced modes.

PF_WIN_SZ

PF_WIN_SZ				
Register Space:	MMIO: 0/2/0			
Project:	BDW			
Default Value:	0x00000000			
Access:	Double Buffered			
Size (in bits):	32			
Double Buffer Update Point:	Start of vertical blank or framestart			
Address:	68074h-68077h			
Name:	PF A Window Size			
ShortName:	PF_WIN_SZ_A			
Power:	Always on			
Reset:	soft			
Address:	68874h-68877h			
Name:	PF B Window Size			
ShortName:	PF_WIN_SZ_B			
Power:	off/on			
Reset:	soft			
Address:	69074h-69077h			
Name:	PF C Window Size			
ShortName:	PF_WIN_SZ_C			
Power:	off/on			
Reset:	soft			
Writes to this register arm PF registers on this pipe.				
Workaround				
Double-buffering updates at the start of vertical blank and at the framestart. If programming needs to be delayed to the next frame then the register writes have to be delayed to after the framestart of the current frame.				
Restriction				
When pipe scaling is enabled, the scaled output must equal the pipe active area, so Pipe active size = (2 * PF window position) + PF window size.				
DWord	Bit	Description		
0	31:29	Reserved		
		Format: MBZ		
	28:16	XSIZE This field specifies the horizontal size in pixels of the panel fitted window.		

PF_WIN_SZ				
	15:12	<p>Reserved</p> <table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ
Format:	MBZ			
	11:0	<p>YSIZE This field specifies the vertical size in pixels of the panel fitted window.</p> <table border="1"> <tr> <td>Restriction</td></tr> <tr> <td>Bit 0 must be zero for interlaced modes.</td></tr> </table>	Restriction	Bit 0 must be zero for interlaced modes.
Restriction				
Bit 0 must be zero for interlaced modes.				

PIPE_FLIPCNT

PIPE_FLIPCNT								
Register Space:	MMIO: 0/2/0							
Project:	BDW							
Default Value:	0x00000000							
Access:	RO							
Size (in bits):	32							
Address:	70044h-70047h							
Name:	Pipe A Flip Count							
ShortName:	PIPE_FLIPCNT_A							
Valid Projects:	BDW							
Power:	Always on							
Reset:	soft							
Address:	71044h-71047h							
Name:	Pipe B Flip Count							
ShortName:	PIPE_FLIPCNT_B							
Valid Projects:	BDW							
Power:	off/on							
Reset:	soft							
Address:	72044h-72047h							
Name:	Pipe C Flip Count							
ShortName:	PIPE_FLIPCNT_C							
Valid Projects:	BDW							
Power:	off/on							
Reset:	soft							
There is one instance of this register format per each pipe A/B/C.								
DWord	Bit	Description						
0	31:0	Pipe Flip Counter <table border="1"> <thead> <tr> <th colspan="2">Description</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td colspan="2">This field provides read back of the display pipe flip counter. The counter increments on the start of each flip to the primary plane of this pipe. The start of flip is when the plane surface address is updated, not when the flip completes. The flip can be through command streamer asynchronous and synchronous flips or MMIO writes to the primary plane surface address. It rolls over back to 0 after (2^32)-1 flips.</td> <td>BDW</td> </tr> </tbody> </table>	Description		Project	This field provides read back of the display pipe flip counter. The counter increments on the start of each flip to the primary plane of this pipe. The start of flip is when the plane surface address is updated, not when the flip completes. The flip can be through command streamer asynchronous and synchronous flips or MMIO writes to the primary plane surface address. It rolls over back to 0 after (2^32)-1 flips.		BDW
Description		Project						
This field provides read back of the display pipe flip counter. The counter increments on the start of each flip to the primary plane of this pipe. The start of flip is when the plane surface address is updated, not when the flip completes. The flip can be through command streamer asynchronous and synchronous flips or MMIO writes to the primary plane surface address. It rolls over back to 0 after (2^32)-1 flips.		BDW						

PIPE_FLIPTMSTMP

PIPE_FLIPTMSTMP								
Register Space:	MMIO: 0/2/0							
Project:	BDW							
Default Value:	0x00000000							
Access:	R/W							
Size (in bits):	32							
Address:	7004Ch-7004Fh							
Name:	Pipe A Flip Time Stamp							
ShortName:	PIPE_FLIPTMSTMP_A							
Valid Projects:	BDW							
Power:	Always on							
Reset:	soft							
Address:	7104Ch-7104Fh							
Name:	Pipe B Flip Time Stamp							
ShortName:	PIPE_FLIPTMSTMP_B							
Valid Projects:	BDW							
Power:	off/on							
Reset:	soft							
Address:	7204Ch-7204Fh							
Name:	Pipe C Flip Time Stamp							
ShortName:	PIPE_FLIPTMSTMP_C							
Valid Projects:	BDW							
Power:	off/on							
Reset:	soft							
There is one instance of this register format per each pipe A/B/C.								
DWord	Bit	Description						
0	31:0	<p>Pipe Flip Time Stamp</p> <table border="1"> <thead> <tr> <th colspan="2">Description</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td colspan="2">This field provides read back of the display pipe flip time stamp. The time stamp value is sampled on the start of each flip to the primary plane of this pipe. The start of flip is when the plane surface address is updated, not when the flip completes. The flip can be through command streamer asynchronous and synchronous flips or MMIO writes to the primary plane surface address. The TIMESTAMP_CTR register has the current time stamp value.</td> <td>BDW</td> </tr> </tbody> </table>	Description		Project	This field provides read back of the display pipe flip time stamp. The time stamp value is sampled on the start of each flip to the primary plane of this pipe. The start of flip is when the plane surface address is updated, not when the flip completes. The flip can be through command streamer asynchronous and synchronous flips or MMIO writes to the primary plane surface address. The TIMESTAMP_CTR register has the current time stamp value.		BDW
Description		Project						
This field provides read back of the display pipe flip time stamp. The time stamp value is sampled on the start of each flip to the primary plane of this pipe. The start of flip is when the plane surface address is updated, not when the flip completes. The flip can be through command streamer asynchronous and synchronous flips or MMIO writes to the primary plane surface address. The TIMESTAMP_CTR register has the current time stamp value.		BDW						

PIPE_FRMCNT

PIPE_FRMCNT		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Address:	70040h-70043h	
Name:	Pipe A Frame Count	
ShortName:	PIPE_FRMCNT_A	
Valid Projects:	BDW	
Power:	Always on	
Reset:	soft	
Address:	71040h-71043h	
Name:	Pipe B Frame Count	
ShortName:	PIPE_FRMCNT_B	
Valid Projects:	BDW	
Power:	off/on	
Reset:	soft	
Address:	72040h-72043h	
Name:	Pipe C Frame Count	
ShortName:	PIPE_FRMCNT_C	
Valid Projects:	BDW	
Power:	off/on	
Reset:	soft	
There is one instance of this register format per each pipe A/B/C.		
DWord	Bit	Description
0	31:0	Pipe Frame Counter Provides read back of the display pipe frame counter. This counter increments on every start of vertical blank and rolls over back to 0 after $(2^{32}) - 1$ frames.

PIPE_FRMTMSTMP

PIPE_FRMTMSTMP		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	70048h-7004Bh	
Name:	Pipe A Frame Time Stamp	
ShortName:	PIPE_FRMTMSTMP_A	
Valid Projects:	BDW	
Power:	Always on	
Reset:	soft	
Address:	71048h-7104Bh	
Name:	Pipe B Frame Time Stamp	
ShortName:	PIPE_FRMTMSTMP_B	
Valid Projects:	BDW	
Power:	off/on	
Reset:	soft	
Address:	72048h-7204Bh	
Name:	Pipe C Frame Time Stamp	
ShortName:	PIPE_FRMTMSTMP_C	
Valid Projects:	BDW	
Power:	off/on	
Reset:	soft	
There is one instance of this register format per each pipe A/B/C.		
DWord	Bit	Description
0	31:0	<p>Pipe Frame Time Stamp</p> <p>This field provides read back of the display pipe frame time stamp. The time stamp value is sampled at every start of vertical blank. The TIMESTAMP_CTR register has the current time stamp value.</p>

PIPE_MISC

PIPE_MISC			
Register Space:	MMIO: 0/2/0		
Project:	BDW		
Default Value:	0x00000000		
Access:	Double Buffered		
Size (in bits):	32		
Double Buffer Update Point:	Start of vertical blank OR pipe disabled		
Address:	70030h-70033h		
Name:	Pipe A Miscellaneous		
ShortName:	PIPE_MISC_A		
Valid Projects:	BDW		
Power:	Always on		
Reset:	soft		
Address:	71030h-71033h		
Name:	Pipe B Miscellaneous		
ShortName:	PIPE_MISC_B		
Valid Projects:	BDW		
Power:	off/on		
Reset:	soft		
Address:	72030h-72033h		
Name:	Pipe C Miscellaneous		
ShortName:	PIPE_MISC_C		
Valid Projects:	BDW		
Power:	off/on		
Reset:	soft		
There is one instance of this register format per each pipe A/B/C.			
DWord	Bit	Description	
0	31:28	Reserved	
		Project:	BDW
	27:26	Reserved	
	Project:	BDW	
25:24	Reserved		

PIPE MISC

		Change Mask for Primary Flip		
		Project: BDW		
This field controls change tracking for the primary plane flip. Change tracking can be used by PSR/SRD and WD.				
		Value Name		
	0b	Not Masked		
	1b	Masked		
22	Change Mask for Sprite Enable			
Project: BDW				
This field controls change tracking for the sprite plane enable. Change tracking can be used by PSR/SRD and WD.				
		Value Name		
	0b	Not Masked		
	1b	Masked		
21	Change Mask for Cursor Move			
Project: BDW				
This field controls change tracking for the cursor plane movement. Change tracking can be used by PSR/SRD and WD.				
		Value Name		
	0b	Not Masked		
	1b	Masked		
20	Change Mask for Vblank Vsync Int			
This field controls change tracking for the vblank or vsync interrupt enable. Change tracking can be used by PSR/SRD and WD.				
		Value Name		
	0b	Not Masked		
	1b	Masked		
19	Reserved			
18	Reserved			
17	Reserved			
16	Reserved			

PIPE_MISC

	15:14	Rotation Info This field indicates to internal KVMR screen capture that the display has been rotated through software or hardware rotation. Select the closest value if the rotation is not an exact multiple of 90 degrees. Hardware rotation of the display output is controlled through the plane control registers, not through this field. <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center; background-color: #e0e0ff;">Value</th><th style="text-align: center; background-color: #e0e0ff;">Name</th><th style="text-align: center; background-color: #e0e0ff;">Description</th></tr> </thead> <tbody> <tr> <td style="text-align: center;">00b</td><td style="text-align: center;">None</td><td>No rotation on this pipe</td></tr> <tr> <td style="text-align: center;">01b</td><td style="text-align: center;">90</td><td>90 degree rotation on this pipe</td></tr> <tr> <td style="text-align: center;">10b</td><td style="text-align: center;">180</td><td>180 degree rotation on this pipe</td></tr> <tr> <td style="text-align: center;">11b</td><td style="text-align: center;">270</td><td>270 degree rotation on this pipe</td></tr> </tbody> </table> <p style="text-align: center;">Restriction</p> This field must be programmed in order for internal KVMR screen capture to work correctly when display is rotated by software or hardware.		Value	Name	Description	00b	None	No rotation on this pipe	01b	90	90 degree rotation on this pipe	10b	180	180 degree rotation on this pipe	11b	270	270 degree rotation on this pipe
Value	Name	Description																
00b	None	No rotation on this pipe																
01b	90	90 degree rotation on this pipe																
10b	180	180 degree rotation on this pipe																
11b	270	270 degree rotation on this pipe																
	13:12	Reserved <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Project:</td><td style="width: 50%;">BDW</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>		Project:	BDW	Format:	MBZ											
Project:	BDW																	
Format:	MBZ																	
	11	Pipe output color space select This field indicates the output color space. This field affects the values of the pipe border and some capture functions. This field does not affect the planes, pipe CSC, or ports. <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center; background-color: #e0e0ff;">Value</th><th style="text-align: center; background-color: #e0e0ff;">Name</th></tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td><td>RGB</td></tr> <tr> <td style="text-align: center;">1b</td><td>YUV</td></tr> </tbody> </table> <p style="text-align: center;">Restriction</p> This field must be set to match the color space that will be output from the pipe CSC or output from the planes if the pipe CSC is bypassed.		Value	Name	0b	RGB	1b	YUV									
Value	Name																	
0b	RGB																	
1b	YUV																	
	10	xvYCC Color Range Limit This field limits the color range of the pipe output to 1 to 254 for 8-bit components, 4 to 1019 for 10bit components, and 16 to 4079 for 12-bit components. Values outside of the range will be clamped to fit within the range. <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center; background-color: #e0e0ff;">Value</th><th style="text-align: center; background-color: #e0e0ff;">Name</th><th style="text-align: center; background-color: #e0e0ff;">Description</th></tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td><td>Full</td><td>Do not limit the range</td></tr> <tr> <td style="text-align: center;">1b</td><td>Limit</td><td>Limit range</td></tr> </tbody> </table>		Value	Name	Description	0b	Full	Do not limit the range	1b	Limit	Limit range						
Value	Name	Description																
0b	Full	Do not limit the range																
1b	Limit	Limit range																
	9:8	Reserved <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Format:</td><td style="width: 50%;">MBZ</td></tr> </table>		Format:	MBZ													
Format:	MBZ																	

PIPE_MISC

		Dithering BPC This field selects the number of bits per color to be used in dithering.															
	7:5	<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>000b</td><td>8 bpc</td><td>8 bits per color</td></tr> <tr> <td>001b</td><td>10 bpc</td><td>10 bits per color</td></tr> <tr> <td>010b</td><td>6 bpc</td><td>6 bits per color</td></tr> <tr> <td>Others</td><td>Reserved</td><td>Reserved</td></tr> </tbody> </table>	Value	Name	Description	000b	8 bpc	8 bits per color	001b	10 bpc	10 bits per color	010b	6 bpc	6 bits per color	Others	Reserved	Reserved
Value	Name	Description															
000b	8 bpc	8 bits per color															
001b	10 bpc	10 bits per color															
010b	6 bpc	6 bits per color															
Others	Reserved	Reserved															
Programming Notes																	
When dithering is enabled, the value selected here should match the bits per color selected in the Transcoder DDI Function Control register attached to this pipe.																	
	4	Dithering enable This field enables dithering.															
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Disable</td></tr> <tr> <td>1b</td><td>Enable</td></tr> </tbody> </table>	Value	Name	0b	Disable	1b	Enable									
Value	Name																
0b	Disable																
1b	Enable																
	3:2	Dithering type This field selects the dithering type.															
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>00b</td><td>Spatial</td><td>Spatial</td></tr> <tr> <td>01b</td><td>ST1</td><td>Spatio-Temporal 1</td></tr> <tr> <td>10b</td><td>ST2</td><td>Spatio-Temporal 2</td></tr> <tr> <td>11b</td><td>Temporal</td><td>Temporal</td></tr> </tbody> </table>	Value	Name	Description	00b	Spatial	Spatial	01b	ST1	Spatio-Temporal 1	10b	ST2	Spatio-Temporal 2	11b	Temporal	Temporal
Value	Name	Description															
00b	Spatial	Spatial															
01b	ST1	Spatio-Temporal 1															
10b	ST2	Spatio-Temporal 2															
11b	Temporal	Temporal															
	1	Reserved															
		<table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ													
Format:	MBZ																
	0	BFI enable This field enables black frame insertion.															
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Disable</td></tr> <tr> <td>1b</td><td>Enable</td></tr> </tbody> </table>	Value	Name	0b	Disable	1b	Enable									
Value	Name																
0b	Disable																
1b	Enable																
Restriction		Project															
Do not enable BFI when the pipe is attached to transcoder EDP.		BDW															

PIPE_SCANLINE

PIPE_SCANLINE											
Register Space:	MMIO: 0/2/0										
Project:	BDW										
Default Value:	0x00000000										
Access:	RO										
Size (in bits):	32										
Address:	70000h-70003h										
Name:	Pipe A Scan Line										
ShortName:	PIPE_SCANLINE_A										
Valid Projects:	BDW										
Power:	Always on										
Reset:	soft										
Address:	71000h-71003h										
Name:	Pipe B Scan Line										
ShortName:	PIPE_SCANLINE_B										
Valid Projects:	BDW										
Power:	off/on										
Reset:	soft										
Address:	72000h-72003h										
Name:	Pipe C Scan Line										
ShortName:	PIPE_SCANLINE_C										
Valid Projects:	BDW										
Power:	off/on										
Reset:	soft										
This register enables the read back of the pipe vertical line counter. The value increments at the leading edge of HSYNC. The value resets to line zero at the first active line of the display. In interlaced display timings, the scan line counter provides the current line in the field. One field can have a total number of lines that is one greater than the other field.											
DWord	Bit	Description									
0	31	Current Field This is an indication of the current display field. <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Odd</td><td>First field (odd field)</td></tr> <tr> <td>1b</td><td>Even</td><td>Second field (even field)</td></tr> </tbody> </table> Reserved	Value	Name	Description	0b	Odd	First field (odd field)	1b	Even	Second field (even field)
Value	Name	Description									
0b	Odd	First field (odd field)									
1b	Even	Second field (even field)									

PIPE_SCANLINE		
	12:0	<p>Line Counter for Display This is an indication of the current display scan line.</p> <p>Programming Notes</p> <p>The line count value is from the display output timing generator, representing the scan line currently being output to a receiver. Due to buffering within the display engine, the line being fetched (read) from the frame buffer is not directly linked to the line being output. It is possible for the fetched line to be hundreds of lines ahead of the timing generator output line.</p>

PIPE_SCANLINECOMP

PIPE_SCANLINECOMP	
Register Space:	MMIO: 0/2/0
Project:	BDW
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	70004h-70007h
Name:	Pipe A Scan Line Compare
ShortName:	PIPE_SCANLINECOMP_A
Valid Projects:	BDW
Power:	Always on
Reset:	soft
Address:	71004h-71007h
Name:	Pipe B Scan Line Compare
ShortName:	PIPE_SCANLINECOMP_B
Valid Projects:	BDW
Power:	off/on
Reset:	soft
Address:	72004h-72007h
Name:	Pipe C Scan Line Compare
ShortName:	PIPE_SCANLINECOMP_C
Valid Projects:	BDW
Power:	off/on
Reset:	soft

PIPE_SCANLINECOMP

This register is used to initiate a display scan line compare. This MMIO driven scan line compare can not be used at the same time as the command streamer driven scan line compare on the same pipe. When this register is written with the Initiate Compare bit set to 1b, the Display Engine (DE) will start comparing the display pipe or plane (selectable) current scan line value (current scan line) with the start scan line value (current scan line \geq start scan line) and the end scan line value (current scan line \leq end scan line) to decide if the pipe scan line is inside or outside the scan line window of interest. DE will wait until the current scan line is either outside (Inclusive mode) or inside (Exclusive mode) the scan line window, then trigger a scan line event and stop any further comparing. The scan line event can cause display to send a scan line compare response to the command streamer, (used for releasing a MI_WAIT_FOR_EVENT on scan line window), if unmasked in the DERRMR mask register 0x44050. The scan line event can also cause display to generate a scan line compare interrupt, if the interrupt registers are configured for that. The value programmed should be the desired value - 1, so for scan line 0, the value programmed is vertical total, and for scan line 1, the value programmed is 0. The programmable range can include the vertical blank. In interlaced display timings, the current scan line is the current line of the current interlaced field. Either MMIO or a MI_LOAD_REGISTER_IMM command can be used to unmask the scan line render response 0x44050. That can be done anytime before programming this register. There is one instance of this register per pipe.

Restriction

A new scan line compare must not be started until after the previous compare has finished. The end scan line value must be greater than or equal to the start scan line value. When using LRI care must be taken to follow all the programming rules for LRI targetting the display engine.

DWord	Bit	Description									
0	31	<p>Initiate Compare</p> <p>This field initiates the scan line compare. When this register is written with this bit set to 1b, the display engine will do one complete comparison cycle, trigger a scan line event, then stop comparing.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Do nothing</td></tr> <tr> <td>1b</td><td>Initiate compare</td></tr> </tbody> </table> <p>Restriction</p> <p>Do not write this register again until after any previous scan line compare has completed.</p>	Value	Name	0b	Do nothing	1b	Initiate compare			
Value	Name										
0b	Do nothing										
1b	Initiate compare										
30		<p>Inclusive Exclusive Select</p> <p>This field selects whether the scan line compare is done in inclusive mode, where display triggers the scan line event when outside the scan line window, or inclusive mode, where display triggers when inside the window.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Exclusive</td><td>Exclusive mode: trigger scan line event when inside the scan line window</td></tr> <tr> <td>1b</td><td>Inclusive</td><td>Inclusive mode: trigger scan line event when outside the scan line window</td></tr> </tbody> </table>	Value	Name	Description	0b	Exclusive	Exclusive mode: trigger scan line event when inside the scan line window	1b	Inclusive	Inclusive mode: trigger scan line event when outside the scan line window
Value	Name	Description									
0b	Exclusive	Exclusive mode: trigger scan line event when inside the scan line window									
1b	Inclusive	Inclusive mode: trigger scan line event when outside the scan line window									
29		<p>Counter Select</p> <p>This field selects whether the scan line compare is done using the pipe timing generator scanline counter or a plane scanline counter. The pipe timing generator counts the scanlines being output from display. The plane counts the scan lines being fetched from the frame buffer.</p>									

PIPE_SCANLINECOMP

		Value	Name	Description	Project									
		0b	Timing generator	Use the scanline count from the pipe timing generator										
		1b	Primary plane	Use the scanline count from the primary plane	BDW									
Programming Notes														
<p>Due to buffering within the display engine, the line being fetched from the frame buffer is not directly linked to the line being output. It is possible for the fetched line to be hundreds of lines ahead of the timing generator output line. The plane scan line count more closely represents what data is currently being fetched by the plane.</p>														
28:16 Start Scan Line This field specifies the starting scan line number of the scan line window.														
15 Render Response Destination This bit indicates what destination to send the scan line event render response to. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>CS</td> <td>Send scan line event response to CS</td> </tr> <tr> <td>1b</td> <td>BCS</td> <td>Send scan line event response to BCS</td> </tr> </tbody> </table>						Value	Name	Description	0b	CS	Send scan line event response to CS	1b	BCS	Send scan line event response to BCS
Value	Name	Description												
0b	CS	Send scan line event response to CS												
1b	BCS	Send scan line event response to BCS												
14:13 Reserved														
12:0 End Scan Line This field specifies the ending scan line number of the scan line window.														

PIPE_SRCSZ

PIPE_SRCSZ

Register Space:	MMIO: 0/2/0
Project:	BDW
Default Value:	0x00000000
Access:	Double Buffered
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank

Address:	6001Ch-6001Fh
Name:	Pipe A Source Image Size
ShortName:	PIPE_SRCSZ_A
Valid Projects:	BDW
Power:	Always on
Reset:	soft

Address:	6101Ch-6101Fh
Name:	Pipe B Source Image Size
ShortName:	PIPE_SRCSZ_B
Valid Projects:	BDW
Power:	off/on
Reset:	soft

Address:	6201Ch-6201Fh
Name:	Pipe C Source Image Size
ShortName:	PIPE_SRCSZ_C
Valid Projects:	BDW
Power:	off/on
Reset:	soft

There is one instance of this register for each pipe.

Programming Notes

In VGA display mode, this register is ignored and the VGA size from the VGA registers is used instead.

DWord	Bit	Description	
0	31:29	Reserved	Format: MBZ

PIPE_SRCSZ

	28:16	Horizontal Source Size This field specifies Horizontal Source Size. This determines the horizontal size of the image created by the display planes. This field is programmed to the number of pixels desired minus one.				
Restriction						
This register must always be programmed to the same value as the Horizontal Active, except when panel fitting is enabled. Horizontal source sizes larger than 4096 pixels can not be used when Frame Buffer Compression or Panel Fitting are enabled. Horizontal source size should be atleast 8 pixels when panel fitting is enabled.						
	15:12	Reserved				
		<table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Project:</td><td style="width: 50%;">BDW</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	BDW	Format:	MBZ
Project:	BDW					
Format:	MBZ					
	11:0	Vertical Source Size This field specifies Vertical Source Size. This determines the vertical size of the image created by the display planes. This field is programmed to the number of lines desired minus one.				
Restriction						
Vertical source sizes larger than 4096 lines are not supported. This register must always be programmed to the same value as the Vertical Active, except when panel fitting is enabled. Vertical source size should be atleast 8 lines when panel fitting is enabled.						

PIXCLK_GATE

PIXCLK_GATE											
Register Space: MMIO: 0/2/0 Project: DevLPT:H Default Value: 0x00000000 Access: R/W Size (in bits): 32											
Address: C6020h-C6023h Name: Pixel Clock Gate ShortName: PIXCLK_GATE Power: Always on Reset: soft											
DWord	Bit	Description									
0	31:1	Reserved Format:									
	0	Pixel Clock UnGate This field controls the pixel clock gate. The display pixel clock must be gated prior to disabling the clock, and kept gated until after the clock is enabled and the warmup period has passed. <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Gate</td><td>Gate the pixel clock</td></tr> <tr> <td>1b</td><td>Ungate</td><td>Ungate the pixel clock</td></tr> </tbody> </table>		Value	Name	Description	0b	Gate	Gate the pixel clock	1b	Ungate
Value	Name	Description									
0b	Gate	Gate the pixel clock									
1b	Ungate	Ungate the pixel clock									

PLANE_SURFLIVE

PLANE_SURFLIVE	
Register Space:	MMIO: 0/2/0
Project:	BDW
Default Value:	0x00000000 [BDW]
Size (in bits):	32
Address:	700ACh-700AFh
Name:	Cursor A Live Base Address
ShortName:	CUR_SURFLIVE_A
Valid Projects:	BDW
Power:	Always on
Reset:	soft
Address:	701ACh-701AFh
Name:	Primary A Live Base Address
ShortName:	PRI_SURFLIVE_A
Valid Projects:	BDW
Power:	Always on
Reset:	soft
Address:	701BCh-701BFh
Name:	Primary A Left Eye Live Base Address
ShortName:	PRI_LEFT_SURFLIVE_A
Valid Projects:	BDW
Power:	Always on
Reset:	soft
Address:	702ACh-702AFh
Name:	Sprite A Live Base Address
ShortName:	SPR_SURFLIVE_A
Valid Projects:	BDW
Power:	Always on
Reset:	soft
Address:	702BCh-702BFh
Name:	Sprite A Left Eye Live Base Address
ShortName:	SPR_LEFT_SURFLIVE_A
Valid Projects:	BDW
Power:	Always on
Reset:	soft
Address:	710ACh-710AFh

PLANE_SURFLIVE

Name:	Cursor B Live Base Address
ShortName:	CUR_SURFLIVE_B
Valid Projects:	BDW
Power:	off/on
Reset:	soft
Address:	711ACh-711AFh
Name:	Primary B Live Base Address
ShortName:	PRI_SURFLIVE_B
Valid Projects:	BDW
Power:	off/on
Reset:	soft
Address:	711BCh-711BFh
Name:	Primary B Left Eye Live Base Address
ShortName:	PRI_LEFT_SURFLIVE_B
Valid Projects:	BDW
Power:	off/on
Reset:	soft
Address:	712ACh-712AFh
Name:	Sprite B Live Base Address
ShortName:	SPR_SURFLIVE_B
Valid Projects:	BDW
Power:	off/on
Reset:	soft
Address:	712BCh-712BFh
Name:	Sprite B Left Eye Live Base Address
ShortName:	SPR_LEFT_SURFLIVE_B
Valid Projects:	BDW
Power:	off/on
Reset:	soft
Address:	720ACh-720AFh
Name:	Cursor C Live Base Address
ShortName:	CUR_SURFLIVE_C
Valid Projects:	BDW
Power:	off/on
Reset:	soft
Address:	721ACh-721AFh
Name:	Primary C Live Base Address

PLANE_SURFLIVE

ShortName:	PRI_SURFLIVE_C		
Valid Projects:	BDW		
Power:	off/on		
Reset:	soft		
Address:	721BCh-721BFh		
Name:	Primary C Left Eye Live Base Address		
ShortName:	PRI_LEFT_SURFLIVE_C		
Valid Projects:	BDW		
Power:	off/on		
Reset:	soft		
Address:	722ACh-722AFh		
Name:	Sprite C Live Base Address		
ShortName:	SPR_SURFLIVE_C		
Valid Projects:	BDW		
Power:	off/on		
Reset:	soft		
Address:	722BCh-722BFh		
Name:	Sprite C Left Eye Live Base Address		
ShortName:	SPR_LEFT_SURFLIVE_C		
Valid Projects:	BDW		
Power:	off/on		
Reset:	soft		
There is one instance of this register for each plane.			
DWord	Bit	Description	
0	31:0	Live Surface Base Address	
		Project:	BDW
		Access:	RO
This gives the live value of the surface base address as being currently used for the plane.			

PORT_CLK_SEL

PORT_CLK_SEL	
Register Space:	MMIO: 0/2/0
Project:	BDW
Default Value:	0xE0000000
Access:	R/W
Size (in bits):	32
Address:	46100h-46103h
Name:	DDIA Port Clock Select
ShortName:	PORT_CLK_SEL_DDIA
Valid Projects:	BDW
Power:	Always on
Reset:	soft
Address:	46104h-46107h
Name:	DDIB Port Clock Select
ShortName:	PORT_CLK_SEL_DDIB
Valid Projects:	BDW
Power:	Always on
Reset:	soft
Address:	46108h-4610Bh
Name:	DDIC Port Clock Select
ShortName:	PORT_CLK_SEL_DDIC
Valid Projects:	BDW
Power:	Always on
Reset:	soft
Address:	4610Ch-4610Fh
Name:	DDID Port Clock Select
ShortName:	PORT_CLK_SEL_DDID
Valid Projects:	BDW
Power:	Always on
Reset:	soft
Address:	46110h-46113h
Name:	DDIE Port Clock Select
ShortName:	PORT_CLK_SEL_DDIE
Valid Projects:	BDW
Power:	Always on
Reset:	soft

PORT_CLK_SEL																																	
DWord	Bit	Description																															
0		This register maps the PLL outputs to the port. There is one instance of this register format per DDI.																															
	31:29	<p>Port Clock Select</p> <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td colspan="2">Select which PLL output to use for this port. The PLL output frequency is 1/2 the bit clock rate and doubled to become the DDI I/O bit rate.</td></tr> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> <tr> <td>000b</td><td>LCPLL 2700</td><td>LCPLL 2700 MHz (DP 5.4 GHz)</td></tr> <tr> <td>001b</td><td>LCPLL 1350</td><td>LCPLL 1350 MHz (DP 2.7 GHz)</td></tr> <tr> <td>010b</td><td>LCPLL 810</td><td>LCPLL 810 MHz (DP 1.62 GHz)</td></tr> <tr> <td>011b</td><td>SPLL</td><td>SPLL (DP or FDI) - Frequency programmed through SPLL_CTL</td></tr> <tr> <td>100b</td><td>WRPLL1</td><td>WRPLL1 (HDMI, DVI, DP, or FDI) - Frequency programmed through WRPLL_CTL1</td></tr> <tr> <td>101b</td><td>WRPLL2</td><td>WRPLL2 (HDMI, DVI, DP, or FDI) - Frequency programmed through WRPLL_CTL2</td></tr> <tr> <td>110b</td><td>Reserved</td><td>Reserved</td></tr> <tr> <td>111b</td><td>None [Default]</td><td>No PLL selected. Clock is disabled for this port.</td></tr> </table> <p>Restriction</p> <p>This must not be changed while the port is enabled or any transcoder directed to the port is enabled.</p>	Project:	BDW	Select which PLL output to use for this port. The PLL output frequency is 1/2 the bit clock rate and doubled to become the DDI I/O bit rate.		Value	Name	Description	000b	LCPLL 2700	LCPLL 2700 MHz (DP 5.4 GHz)	001b	LCPLL 1350	LCPLL 1350 MHz (DP 2.7 GHz)	010b	LCPLL 810	LCPLL 810 MHz (DP 1.62 GHz)	011b	SPLL	SPLL (DP or FDI) - Frequency programmed through SPLL_CTL	100b	WRPLL1	WRPLL1 (HDMI, DVI, DP, or FDI) - Frequency programmed through WRPLL_CTL1	101b	WRPLL2	WRPLL2 (HDMI, DVI, DP, or FDI) - Frequency programmed through WRPLL_CTL2	110b	Reserved	Reserved	111b	None [Default]	No PLL selected. Clock is disabled for this port.
Project:	BDW																																
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111b	None [Default]	No PLL selected. Clock is disabled for this port.																															
	28	<p>Reserved</p> <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	BDW	Format:	MBZ																											
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	27:0	<p>Reserved</p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ																													
Format:	MBZ																																

Power Context Save

PWRCTXSAVE - Power Context Save		
DWord	Bit	Description
0	31:16	Mask Bits Default Value: 0000h Access: RO
	15	Extra Bits15 Default Value: 0b Access: R/W Extra Bits for future use.
	14	Extra Bits14 Default Value: 0b Access: R/W Extra Bits for future use.
	13	Extra Bits13 Default Value: 0b Access: R/W Extra Bits for future use.
	12	Extra Bits12 Default Value: 0b Access: R/W Extra Bits for future use.
	11	Extra Bits11 Default Value: 0b Access: R/W Extra Bits for future use.

PWRCTXSAVE - Power Context Save

	10	Extra Bits10				
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Extra Bits for future use.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
	9	Power Context Save Request				
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Power Context Save. Bit[9].</p> <p>Power Context Save Request.</p> <p>1'b0: Power context save is not being requested (default).</p> <p>1'b1: Power context save is being requested.</p> <p>Unit needs to self-clear this bit upon sampling.</p> <p>This bit is self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
	8:0	Power Context Save Quad Word Credits				
		<table border="1"> <tr> <td>Default Value:</td><td>000000000b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Power Context Save. Bits[8:0].</p> <p>QWord Credits for Power Context Save Request.</p> <p>An initial length packet is required per power context save session, but that packet does not consume a credit. See protocol description for more details.</p> <p>Minimum Credits = 1: Unit may send 1 QWord pair.</p> <p>Maximum Credits = 511: Unit may send 511 QWord pairs.</p> <p>A QWord pair is defined as a 32-bit register address and the corresponding 32-bits of register data.</p> <p>Only valid with PWRCTX_SAVE_REQ (Bit9).</p>	Default Value:	000000000b	Access:	R/W
Default Value:	000000000b					
Access:	R/W					

Power context Save Register for LPFC

LPCSR - Power context Save Register for LPFC						
DWord	Bit	Description				
0	31:10	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Reserved.</td> <td></td> </tr> </table>	Access:	RO	Reserved.	
Access:	RO					
Reserved.						
9:0	<p>Power context save register command</p> <table border="1"> <tr> <td>Access:</td> <td>R/W Hardware Clear</td> </tr> </table> <p>Bit[9]. Power Context Save Request. 1'b0: Power context save is not being requested (default). 1'b1: Power context save is being requested. Unit needs to self-clear this bit upon sampling. Bits[8:0]. QWord Credits for Power Context Save Request. Minimum Credits = 1: Unit may send 1 QWord pair (enough for first LRI at least). Maximum Credits = 511: Unit may send 511 QWord pairs. A QWord pair is defined as a 32-bit register address and the corresponding 32-bits of register data. Note that the LRI header and END commands are 64-bits each (32-bit command followed by 32-bit NOOP) and consume one QWord credit. Only valid with PWRCTX_SAVE_REQ (Bit9).</p>	Access:	R/W Hardware Clear			
Access:	R/W Hardware Clear					

Power Context Save request

PCTXSAVEREQ - Power Context Save request						
DWord	Bit	Description				
0	31:16	Message Mask <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td colspan="2">Message Mask bots for lower 16 bits</td></tr> </table>	Access:	RO	Message Mask bots for lower 16 bits	
Access:	RO					
Message Mask bots for lower 16 bits						
15:10	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td colspan="2">Reserved</td></tr> </table>	Access:	RO	Reserved		
Access:	RO					
Reserved						
9	Power context save <table border="1"> <tr> <td>Access:</td> <td>R/W Set</td> </tr> <tr> <td colspan="2">Power Context Save Request 1'b0 : Power context save is not being requested 1'b1 : Power context save is being requested CPUUnit self-clears this bit upon sampling.</td></tr> </table>	Access:	R/W Set	Power Context Save Request 1'b0 : Power context save is not being requested 1'b1 : Power context save is being requested CPUUnit self-clears this bit upon sampling.		
Access:	R/W Set					
Power Context Save Request 1'b0 : Power context save is not being requested 1'b1 : Power context save is being requested CPUUnit self-clears this bit upon sampling.						
8:0	Power Context Save request credit count <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td colspan="2">QWord Credits for Power Context Save Request Minimum Credits = 1 : Unit may send 1 QWord pair (enough for first LRI at least) Maximum Credits = 511 : Unit may send 511 QWord pairs A QWord pair is defined as a 32-bit register address and the corresponding 32-bits of register data. Note that the LRI header and END commands are 64-bits each (32-bit command followed by 32-bit NOOP) and will consume one QWord credit. Only valid with PWRCTX_SAVE_REQ (Bit9).</td></tr> </table>	Access:	R/W	QWord Credits for Power Context Save Request Minimum Credits = 1 : Unit may send 1 QWord pair (enough for first LRI at least) Maximum Credits = 511 : Unit may send 511 QWord pairs A QWord pair is defined as a 32-bit register address and the corresponding 32-bits of register data. Note that the LRI header and END commands are 64-bits each (32-bit command followed by 32-bit NOOP) and will consume one QWord credit. Only valid with PWRCTX_SAVE_REQ (Bit9).		
Access:	R/W					
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PP_CONTROL

PP_CONTROL											
Register Space: MMIO: 0/2/0 Project: DevLPT Default Value: 0x00000000 Access: R/W Size (in bits): 32											
Address: C7204h-C7207h Name: Panel Power Control ShortName: PP_CONTROL Power: Always on Reset: soft											
DWord	Bit	Description									
0	31:16	Reserved									
	15:4	Reserved Format: MBZ									
	3	VDD Override This bit is used to force on VDD for the embedded DisplayPort panel so AUX transactions can occur without enabling the panel power sequence. This is intended for panels that require VDD to be asserted before accessing AUX port on the receiver. When software clears this bit from '1' to '0' (disable VDD override) it must ensure that T4 power cycle delay is met before setting this bit to '1' again. <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Not Force</td><td>Panel VDD controlled by Panel Power Sequence state machine</td></tr> <tr> <td>1b</td><td>Force</td><td>Force panel VDD on</td></tr> </tbody> </table>	Value	Name	Description	0b	Not Force	Panel VDD controlled by Panel Power Sequence state machine	1b	Force	Force panel VDD on
Value	Name	Description									
0b	Not Force	Panel VDD controlled by Panel Power Sequence state machine									
1b	Force	Force panel VDD on									
2	2	Backlight Enable Enabling this bit enables the panel backlight when hardware is in the correct panel power sequence state. The backlight should be enabled and disabled only at the correct points as defined in the mode set sequence. <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Disable</td><td>Backlight disabled</td></tr> <tr> <td>1b</td><td>Enable</td><td>Backlight enabled</td></tr> </tbody> </table>	Value	Name	Description	0b	Disable	Backlight disabled	1b	Enable	Backlight enabled
Value	Name	Description									
0b	Disable	Backlight disabled									
1b	Enable	Backlight enabled									
1	Power Down on Reset Enabling this bit causes the panel to power down on reset warning or FLR. If the panel is not on during a reset event, this bit is ignored. <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Do not Run</td><td>Do not run panel power down sequence when reset is detected</td></tr> <tr> <td>1b</td><td>Run</td><td>Run panel power down sequence when reset is detected</td></tr> </tbody> </table>	Value	Name	Description	0b	Do not Run	Do not run panel power down sequence when reset is detected	1b	Run	Run panel power down sequence when reset is detected	
Value	Name	Description									
0b	Do not Run	Do not run panel power down sequence when reset is detected									
1b	Run	Run panel power down sequence when reset is detected									

PP_CONTROL											
	0	Power State Target									
<p>This bit sets the panel power state target. It can be written at any time and takes effect at the completion of any current power cycle.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Off</td><td>The panel power state target is off. If the panel is either on or in a power on sequence, a power off sequence is started as soon as the panel reaches the power on state. This may include a power cycle delay. If the panel is currently off, there is no change of the power state or sequencing done.</td></tr> <tr> <td>1b</td><td>On</td><td>The panel power state target is on. If the panel is in either the off state or a power off sequence, and all pre-conditions are met, a power on sequence is started as soon as the panel reaches the power off state. This may include a power cycle delay. If the panel is currently on, there is no change of the power state or sequencing done.</td></tr> </tbody> </table>			Value	Name	Description	0b	Off	The panel power state target is off. If the panel is either on or in a power on sequence, a power off sequence is started as soon as the panel reaches the power on state. This may include a power cycle delay. If the panel is currently off, there is no change of the power state or sequencing done.	1b	On	The panel power state target is on. If the panel is in either the off state or a power off sequence, and all pre-conditions are met, a power on sequence is started as soon as the panel reaches the power off state. This may include a power cycle delay. If the panel is currently on, there is no change of the power state or sequencing done.
Value	Name	Description									
0b	Off	The panel power state target is off. If the panel is either on or in a power on sequence, a power off sequence is started as soon as the panel reaches the power on state. This may include a power cycle delay. If the panel is currently off, there is no change of the power state or sequencing done.									
1b	On	The panel power state target is on. If the panel is in either the off state or a power off sequence, and all pre-conditions are met, a power on sequence is started as soon as the panel reaches the power off state. This may include a power cycle delay. If the panel is currently on, there is no change of the power state or sequencing done.									
Workaround											
<p>On LP systems with ISCLK PLL shutdown enabled, display register C2020h bit 12 must be set to 1b before setting panel power state target to "On". If no other feature requires register C2020h bit 12, it can be cleared to 0b after the panel power state target has been set to "Off" and the panel power status indicates the panel is off and the power cycle delay is not active. To save power, register C2020h bit 12 must be cleared to 0b when internal graphics is put in the D3 device power state.</p>											

PP_DIVISOR

PP_DIVISOR															
DWord	Bit	Description													
0	31:8	Reference divider This field provides the value of the divider used for the creation of the panel timer reference clock. The output of the divider is used as the time base (100 us) for all other timers. The value of zero must not be used. The value should be $(100 * \text{Ref clock frequency in MHz} / 2) - 1$.	<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>001869h</td> <td>125 MHz [Default]</td> <td></td> <td>DevLPT:H</td> </tr> <tr> <td>0004AFh</td> <td>24 MHz [Default]</td> <td></td> <td>DevLPT:LP</td> </tr> </tbody> </table>	Value	Name	Description	Project	001869h	125 MHz [Default]		DevLPT:H	0004AFh	24 MHz [Default]		DevLPT:LP
Value	Name	Description	Project												
001869h	125 MHz [Default]		DevLPT:H												
0004AFh	24 MHz [Default]		DevLPT:LP												
	7:5	Reserved Format:	MBZ												
	4:0	Power Cycle Delay Default Value: 6h 500 mS Programmable value of time panel must remain in a powered down state after powering down. This provides the time delay for the eDP T12 time value; the shortest time from panel power disable to power enable. If a panel power on sequence is attempted during this delay, the power on sequence will not commence until the delay is complete. The time unit used is the 100 ms timer. This register needs to be programmed to a "+1" value. For instance to achieve 400 ms, program a value of 5. Writing a value of 0 selects no delay or is used to abort the delay if it is active. For devices coming out of reset, the timer will be set to the default value and the count down will begin after the de-assertion of reset. Even if the panel is not enabled, the count happens after reset.													

PP_OFF_DELAYS

PP_OFF_DELAYS			
Register Space: MMIO: 0/2/0 Project: DevLPT Default Value: 0x00000000 Access: R/W Size (in bits): 32			
Address: C720Ch-C720Fh Name: Panel Power Off Sequencing Delays ShortName: PP_OFF_DELAYS Power: Always on Reset: soft			
DWord	Bit	Description	
0	31:29	Reserved	Format: MBZ
	28:16	Power Down delay Programmable value of panel power sequencing delay during power down. Software programs this field with the time delay for the eDP T10 time value; the time from source ending valid video data to source disabling panel power. Software controls the source valid video data output, so this together with T9 is only used as a step towards the final power down delay. The time unit used is the 100us timer.	
	15:13	Reserved	Format: MBZ
	12:0	Backlight off to power down Power backlight off to power down delay. Programmable value of panel power sequencing delay during power down. Software programs this field with the time delay for the eDP T9 time value; the time from backlight disable to source ending valid video data. Software controls the backlight disable and source valid video data output, so this together with T10 is only used as a step towards the final power down delay. The time unit used is the 100us timer.	

PP_ON_DELAYS

PP_ON_DELAYS			
Register Space: MMIO: 0/2/0 Project: DevLPT Default Value: 0x00000000 Access: R/W Size (in bits): 32			
Address: C7208h-C720Bh Name: Panel Power On Sequencing Delays ShortName: PP_ON_DELAYS Power: Always on Reset: soft			
DWord	Bit	Description	
0	31:29	Reserved	Format: MBZ
	28:16	Power up delay Programmable value of panel power sequencing delay during panel power up. Software programs this field with the time delay for the eDP T3 time value; the time from the source enabling panel power to when the sink HPD and AUX channel are ready. Software controls when AUX channel transactions start, so this is just used as a timer. The time unit used is the 100us timer.	
	15:13	Reserved	Format: MBZ
	12:0	Power on to backlight on Power on to backlight enable delay. Programmable value of panel power sequencing delay during panel power up. Software programs this field with a value of 1b to get the minimum delay from hardware. Software controls the source valid video data output and backlight enable after this delay has been met. Hardware will not allow the backlight to enable until after this delay and the power up delay (eDP T3) have passed. The time unit used is the 100us timer.	

PP_STATUS

PP_STATUS																	
DWord	Bit	Description															
0	31	<p>Panel Power On Status Software is responsible for enabling the embedded panel display only at the correct point as defined in the mode set sequence. This bit will become "0" only after the panel power down sequencing is completed.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Off</td> <td>Indicates that the panel power down sequencing has completed. A power cycle delay may be currently active.</td> </tr> <tr> <td>1b</td> <td>On</td> <td>Indicates that the panel is currently powered up or is currently in the power down sequence.</td> </tr> </tbody> </table>	Value	Name	Description	0b	Off	Indicates that the panel power down sequencing has completed. A power cycle delay may be currently active.	1b	On	Indicates that the panel is currently powered up or is currently in the power down sequence.						
Value	Name	Description															
0b	Off	Indicates that the panel power down sequencing has completed. A power cycle delay may be currently active.															
1b	On	Indicates that the panel is currently powered up or is currently in the power down sequence.															
	30	<p>Reserved</p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ													
Format:	MBZ																
	29:28	<p>Power Sequence Progress</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>None</td> <td>Indicates that the panel is not in a power sequence</td> </tr> <tr> <td>01b</td> <td>Power Up</td> <td>Indicates that the panel is in a power up sequence (may include power cycle delay)</td> </tr> <tr> <td>10b</td> <td>Power Down</td> <td>Indicates that the panel is in a power down sequence</td> </tr> <tr> <td>11b</td> <td>Reserved</td> <td>Reserved</td> </tr> </tbody> </table>	Value	Name	Description	00b	None	Indicates that the panel is not in a power sequence	01b	Power Up	Indicates that the panel is in a power up sequence (may include power cycle delay)	10b	Power Down	Indicates that the panel is in a power down sequence	11b	Reserved	Reserved
Value	Name	Description															
00b	None	Indicates that the panel is not in a power sequence															
01b	Power Up	Indicates that the panel is in a power up sequence (may include power cycle delay)															
10b	Power Down	Indicates that the panel is in a power down sequence															
11b	Reserved	Reserved															
	27	<p>Power Cycle Delay Active Power cycle delays occur after a panel power down sequence or after a hardware reset. On reset, a power cycle delay will occur using the default value for the timing.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Not Active</td> <td>A power cycle delay is not currently active</td> </tr> <tr> <td>1b</td> <td>Active [Default]</td> <td>A power cycle delay is currently active</td> </tr> </tbody> </table>	Value	Name	Description	0b	Not Active	A power cycle delay is not currently active	1b	Active [Default]	A power cycle delay is currently active						
Value	Name	Description															
0b	Not Active	A power cycle delay is not currently active															
1b	Active [Default]	A power cycle delay is currently active															

PP_STATUS			
	26:4	Reserved Format:	MBZ
	3:0	Reserved	

PPGTT Page Fault Data Registers

PP_PFD[0:31] - PPGTT Page Fault Data Registers				
DWord	Bit	Description		
0	31:12	<p>Fault Entry Page Address</p> <table border="1"> <tr> <td>Format:</td> <td>GraphicsAddress[31:12]</td> </tr> </table> <p>This RO field contains the faulting page address for this Fault Log entry. This field will contain a valid fault address only if the bit in the GTT Page Fault Indication Register corresponding with the address offset of this entry is set.</p>	Format:	GraphicsAddress[31:12]
Format:	GraphicsAddress[31:12]			
11:0	<p>Reserved</p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ	
Format:	MBZ			

Predicate Rendering Data Result

MI_PREDICATE_RESULT - Predicate Rendering Data Result				
DWord	Bit	Description		
0	31:1	Reserved <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ
Format:	MBZ			
0	MI_PREDICATE_RESULT This bit is the result of the last MI_PREDICATE.			

Predicate Rendering Data Result 1

MI_PREDICATE_RESULT_1 - Predicate Rendering Data Result 1		
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x00000000 Access: R/W Size (in bits): 32		
Address:		0241Ch-0241Fh
Name:		Predicate Rendering Data Result 1
ShortName:		MI_PREDICATE_RESULT_1_RCSUNIT
Address:		1241Ch-1241Fh
Name:		Predicate Rendering Data Result 1
ShortName:		MI_PREDICATE_RESULT_1_VCSUNIT0
Address:		1A41Ch-1A41Fh
Name:		Predicate Rendering Data Result 1
ShortName:		MI_PREDICATE_RESULT_1_VECSUNIT
Address:		1C41Ch-1C41Fh
Name:		Predicate Rendering Data Result 1
ShortName:		MI_PREDICATE_RESULT_1_VCSUNIT1
Address:		2241Ch-2241Fh
Name:		Predicate Rendering Data Result 1
ShortName:		MI_PREDICATE_RESULT_1_BCSUNIT
DWord	Bit	Description
0	31:1	Reserved
		Format: MBZ
	0	MI_PREDICATE_RESULT_1
		This bit is used to predicate MI_BATCH_BUFFER_START commands in the RCS command stream. Usage Model: MI_MATH command will be used to do some ALU operations over GPR followed by a MI_LOAD_REGISTER_REGISTER to move the result from GPR to MI_PREDICATE_RESULT_1.

Predicate Rendering Data Result 2

MI_PREDICATE_RESULT_2 - Predicate Rendering Data Result 2										
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x00000000 Access: R/W Size (in bits): 32										
Address: 023BCh-023BFh Name: Predicate Rendering Data Result 2 ShortName: MI_PREDICATE_RESULT_2_RCSUNIT Valid Projects: [BDW]										
Address: 123BCh-123BFh Name: Predicate Rendering Data Result 2 ShortName: MI_PREDICATE_RESULT_2_VCSUNIT0 Valid Projects: [BDW]										
Address: 1A3BCh-1A3BFh Name: Predicate Rendering Data Result 2 ShortName: MI_PREDICATE_RESULT_2_VECSUNIT Valid Projects: [BDW]										
Address: 1C3BCh-1C3BFh Name: Predicate Rendering Data Result 2 ShortName: MI_PREDICATE_RESULT_2_VCSUNIT1 Valid Projects: [BDW]										
Address: 223BCh-223BFh Name: Predicate Rendering Data Result 2 ShortName: MI_PREDICATE_RESULT_2_BCSUNIT Valid Projects: [BDW]										
DWord	Bit	Description								
0	31:1	Reserved Format: MBZ								
	0	MI_PREDICATE_RESULT_2 This bit must be loaded with by SW based on GT mode of operation. This register must be loaded appropriately before using MI_SET_PREDICATE command. <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th><th style="text-align: center;">Name</th><th style="text-align: center;">Description</th></tr> </thead> <tbody> <tr> <td style="text-align: center;">0h</td><td style="text-align: center;">[Default]</td><td>Indicates GT2 mode and lower slice is disabled.</td></tr> <tr> <td style="text-align: center;">1h</td><td></td><td>Indicates GT3 mode and lower slice is enabled.</td></tr> </tbody> </table>	Value	Name	Description	0h	[Default]	Indicates GT2 mode and lower slice is disabled.	1h	
Value	Name	Description								
0h	[Default]	Indicates GT2 mode and lower slice is disabled.								
1h		Indicates GT3 mode and lower slice is enabled.								

Predicate Rendering Data Storage

MI_PREDICATE_DATA - Predicate Rendering Data Storage		
Register Space: MMIO: 0/2/0 Project: BDW Source: RenderCS Default Value: 0x00000000, 0x00000000 Access: R/W Size (in bits): 64		
Address: 02410h-02417h Valid Projects: BDW		
DWord	Bit	Description
0	63:32	MI_PREDICATE_DATA_UDW This register is used either as computed value based off the MI_PREDICATE_SRC0 and MI_PREDICATE_SRC1 or a temporary register. See Predicate Rendering section for more details.
	31:0	MI_PREDICATE_DATA_LDW This register is used either as computed value based off the MI_PREDICATE_SRC0 and MI_PREDICATE_SRC1 or a temporary register. See Predicate Rendering section for more details.

Predicate Rendering Temporary Register0

MI_PREDICATE_SRC0 - Predicate Rendering Temporary Register0		
Description		
DWord	Bit	Description
0	63:0	MI_PREDICATE_SRC0 This register is a temporary register for Predicate Rendering. See Predicate Rendering section for more details.

Predicate Rendering Temporary Register1

MI_PREDICATE_SRC1 - Predicate Rendering Temporary Register1		
Register Space: MMIO: 0/2/0 Project: BDW Source: RenderCS Default Value: 0x00000000, 0x00000000 Access: R/W Size (in bits): 64		
Address: 02408h-0240Fh Valid Projects: BDW		
DWord	Bit	Description
0	63:0	MI_PREDICATE_SRC1 This register is a temporary register for Predicate Rendering. See Predicate Rendering section for more details.

Previous Frequency Request (PREQ)

RP_STATUS7 - Previous Frequency Request(PREQ)				
Register Space: MMIO: 0/2/0				
Project: BDW				
Default Value: 0x00000000				
Size (in bits): 32				
Address: 0A528h				
DWord	Bit	Description		
0	31:0	<p>Previous Preq Request</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Store previous request written to the PCU's IO_PREQ register. RC6 clears last sent, otherwise.</p>	Access:	R/W
Access:	R/W			

Previous Idle/Busy/Avg Count for Freq Down Recommendation

RP_STATUS2 - Previous Idle/Busy/Avg Count for Freq Down Recommendation				
DWord	Bit	Description		
0	31:24	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Reserved.</p>	Access:	RO
Access:	RO			
23:0	<p>Previous Busy in Down EI</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Previous Busy in Down EI (PRVBSYTAVG): Reports the busyness at the end of the previous down evaluation interval.</p> <p>0 = 0 usec. 1 = 1.28 usec. 2 = 2.56 usec. 3 = 3.84 usec. FF FFFF = 21.474 sec.</p> <p>pmcr_previous_ei_down_busy[23:0].</p>	Access:	RO	
Access:	RO			

Previous Idle/Busy/Avg Count for Freq Up Recommendation

RP_STATUS1 - Previous Idle/Busy/Avg Count for Freq Up Recommendation				
DWord	Bit	Description		
0	31:24	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Reserved.</p>	Access:	RO
Access:	RO			
23:0	<p>Previous Busy in UP EI</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Reports the busyness at the end of the previous Up evaluation interval. 0 = 0 usec. 1 = 1.28 usec. 2 = 2.56 usec. 3 = 3.84 usec. FF FFFF = 21.474 sec. pmcr_previous_ei_up_busy[23:0].</p>	Access:	RO	
Access:	RO			

PRI_CTL

PRI_CTL												
Register Space:	MMIO: 0/2/0											
Project:	BDW											
Default Value:	0x00000000											
Access:	Double Buffered											
Size (in bits):	32											
Double Buffer Update Point:	Start of vertical blank or pipe not enabled; after armed											
Double Buffer Armed By:	Write to PRI_SURF or primary plane not enabled											
Address:	70180h-70183h											
Name:	Primary A Control											
ShortName:	PRI_CTL_A											
Power:	Always on											
Reset:	soft											
Address:	71180h-71183h											
Name:	Primary B Control											
ShortName:	PRI_CTL_B											
Power:	off/on											
Reset:	soft											
Address:	72180h-72183h											
Name:	Primary C Control											
ShortName:	PRI_CTL_C											
Power:	off/on											
Reset:	soft											
DWord	Bit	Description										
0	31	<p>Primary Plane Enable</p> <table border="1"> <tr> <td>Format:</td><td>Enable</td></tr> <tr> <td colspan="2">When this bit is set, the primary plane will generate pixels for display. When cleared to zero, primary plane memory fetches cease and plane output is transparent.</td></tr> <tr> <th>Value</th><th>Name</th></tr> <tr> <td>0b</td><td>Disable</td></tr> <tr> <td>1b</td><td>Enable</td></tr> </table>	Format:	Enable	When this bit is set, the primary plane will generate pixels for display. When cleared to zero, primary plane memory fetches cease and plane output is transparent.		Value	Name	0b	Disable	1b	Enable
Format:	Enable											
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Value	Name											
0b	Disable											
1b	Enable											

PRI_CTL																																
	30	<p>Gamma Enable This bit enables pipe gamma correction for the plane pixel data.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Disable</td></tr> <tr> <td>1b</td><td>Enable</td></tr> </tbody> </table>	Value	Name	0b	Disable	1b	Enable																								
Value	Name																															
0b	Disable																															
1b	Enable																															
	29:26	<p>Source Pixel Format This field selects the source pixel format for the primary plane. The 8-bpp indexed format will always use the pipe palette. Before entering the blender, each source format is converted to the pipe pixel format. Alpha values are ignored.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0010b</td><td>8-bit Indexed</td><td>8-bit Indexed</td></tr> <tr> <td>0101b</td><td>16-bit BGRX 5:6:5</td><td>16-bit BGRX (5:6:5 MSB-R:G:B)</td></tr> <tr> <td>0110b</td><td>32-bit BGRX 8:8:8</td><td>32-bit BGRX (8:8:8:8 MSB-X:R:G:B)</td></tr> <tr> <td>1000b</td><td>32-bit RGBX 10:10:10</td><td>32-bit RGBX (2:10:10:10 MSB-X:B:G:R)</td></tr> <tr> <td>1001b</td><td>32-bit XR_BIAS RGBX 10:10:10</td><td>32-bit Extended Range Bias RGBX (2:10:10:10 MSB-X:B:G:R)</td></tr> <tr> <td>1010b</td><td>32-bit BGRX 10:10:10</td><td>32-bit BGRX (2:10:10:10 MSB-X:R:G:B)</td></tr> <tr> <td>1100b</td><td>64-bit RGBX FP</td><td>64-bit RGBX Floating Point(16:16:16:16 MSB-X:B:G:R)</td></tr> <tr> <td>1110b</td><td>32-bit RGBX 8:8:8</td><td>32-bit RGBX (8:8:8:8 MSB-X:B:G:R)</td></tr> <tr> <td>Others</td><td>Reserved</td><td>Reserved</td></tr> </tbody> </table>	Value	Name	Description	0010b	8-bit Indexed	8-bit Indexed	0101b	16-bit BGRX 5:6:5	16-bit BGRX (5:6:5 MSB-R:G:B)	0110b	32-bit BGRX 8:8:8	32-bit BGRX (8:8:8:8 MSB-X:R:G:B)	1000b	32-bit RGBX 10:10:10	32-bit RGBX (2:10:10:10 MSB-X:B:G:R)	1001b	32-bit XR_BIAS RGBX 10:10:10	32-bit Extended Range Bias RGBX (2:10:10:10 MSB-X:B:G:R)	1010b	32-bit BGRX 10:10:10	32-bit BGRX (2:10:10:10 MSB-X:R:G:B)	1100b	64-bit RGBX FP	64-bit RGBX Floating Point(16:16:16:16 MSB-X:B:G:R)	1110b	32-bit RGBX 8:8:8	32-bit RGBX (8:8:8:8 MSB-X:B:G:R)	Others	Reserved	Reserved
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Others	Reserved	Reserved																														
	25	Reserved																														
	24	<p>Pipe CSC Enable This bit enables pipe color space conversion for the plane pixel data.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Disable</td></tr> <tr> <td>1b</td><td>Enable</td></tr> </tbody> </table>	Value	Name	0b	Disable	1b	Enable																								
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0b	Disable																															
1b	Enable																															
	23:16	Reserved																														
	15	<p>180 Display Rotation This mode causes the plane image to be rotated 180 degrees.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0b</td><td>No rotation</td></tr> <tr> <td>1b</td><td>180 degree rotation</td></tr> </tbody> </table>	Value	Name	0b	No rotation	1b	180 degree rotation																								
Value	Name																															
0b	No rotation																															
1b	180 degree rotation																															

PRI_CTL												
	14	Trickle Feed Enable										
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Enable</td></tr> <tr> <td>1b</td><td>Disable</td></tr> </tbody> </table>		Value	Name	0b	Enable	1b	Disable			
Value	Name											
0b	Enable											
1b	Disable											
		Restriction										
		Do not program this field to 1b.										
	13:11	Reserved										
	10	Tiled Surface This bit indicates that the surface data is in tiled memory. The tile pitch is specified in bytes in the plane stride register. This bit may be updated through MMIO writes or through a command streamer initiated synchronous flip.										
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Linear memory</td></tr> <tr> <td>1b</td><td>X-Tiled memory</td></tr> </tbody> </table>		Value	Name	0b	Linear memory	1b	X-Tiled memory			
Value	Name											
0b	Linear memory											
1b	X-Tiled memory											
		Restriction										
		Y tiling is not supported.										
	9	Async Address Update Enable This bit will enable asynchronous updates of the plane surface address when written by MMIO (MMIO asynchronous flips). The surface address will change with the next plane TLB request or when start of vertical blank is reached. Updates during vertical blank may not complete until after the first few active lines are displayed.										
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Sync</td><td>Surface Address MMIO writes will update synchronous to start of vertical blank</td></tr> <tr> <td>1b</td><td>Async</td><td>Surface Address MMIO writes will update asynchronously</td></tr> </tbody> </table>		Value	Name	Description	0b	Sync	Surface Address MMIO writes will update synchronous to start of vertical blank	1b	Async	Surface Address MMIO writes will update asynchronously
Value	Name	Description										
0b	Sync	Surface Address MMIO writes will update synchronous to start of vertical blank										
1b	Async	Surface Address MMIO writes will update asynchronously										
		Restriction										
		No command streamer initiated flips to this plane are allowed when this bit is enabled. Each surface address write must be followed by a wait for flip done indication before writing the surface address register again. Linear memory does not support async updates.										
	8	Reserved										
		Format:	MBZ									

PRI_CTL																	
	7:6	<p>Stereo Surface Vblank Mask This field controls which vertical blank (left eye, right eye, or both) will be used for the plane surface address double-buffering during stereo 3D mode. This field is ignored when not in stereo 3D mode.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>00b</td><td>Mask None</td><td>No masking. Both the left and right eye vertical blanks will be used.</td></tr> <tr> <td>01b</td><td>Mask Left</td><td>Mask the left eye vertical blank. Only the right eye vertical blank will be used.</td></tr> <tr> <td>10b</td><td>Mask Right</td><td>Mask the right eye vertical blank. Only the left eye vertical blank will be used.</td></tr> <tr> <td>Others</td><td>Reserved</td><td>Reserved.</td></tr> </tbody> </table>	Value	Name	Description	00b	Mask None	No masking. Both the left and right eye vertical blanks will be used.	01b	Mask Left	Mask the left eye vertical blank. Only the right eye vertical blank will be used.	10b	Mask Right	Mask the right eye vertical blank. Only the left eye vertical blank will be used.	Others	Reserved	Reserved.
Value	Name	Description															
00b	Mask None	No masking. Both the left and right eye vertical blanks will be used.															
01b	Mask Left	Mask the left eye vertical blank. Only the right eye vertical blank will be used.															
10b	Mask Right	Mask the right eye vertical blank. Only the left eye vertical blank will be used.															
Others	Reserved	Reserved.															
	5:0	<p>Reserved</p> <table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ													
Format:	MBZ																

PRI_LEFT_SURF

PRI_LEFT_SURF				
Register Space:	MMIO: 0/2/0			
Project:	BDW			
Default Value:	0x00000000			
Access:	Double Buffered			
Size (in bits):	32			
Double Buffer Update Point:	Start of left or right eye vertical blank (selectable) or pipe not enabled; after armed			
Double Buffer Armed By:	Write to PRI_SURF or primary plane not enabled			
Address:	701B0h-701B3h			
Name:	Primary A Left Eye Base Address			
ShortName:	PRI_LEFT_SURF_A			
Power:	Always on			
Reset:	soft			
Address:	711B0h-711B3h			
Name:	Primary B Left Eye Base Address			
ShortName:	PRI_LEFT_SURF_B			
Power:	off/on			
Reset:	soft			
Address:	721B0h-721B3h			
Name:	Primary C Left Eye Base Address			
ShortName:	PRI_LEFT_SURF_C			
Power:	off/on			
Reset:	soft			
Restriction				
This register must be programmed with a valid address prior to enabling stereo 3D on this pipe. This register must not be updated asynchronously.				
DWord	Bit	Description		
0	31:12	Left Surface Base Address		
		<table border="1"> <tr> <td>Format:</td><td>GraphicsAddress[31:12]</td></tr> <tr> <td colspan="2">This address specifies the stereo 3D left eye surface base address bits 31:12.</td></tr> </table>	Format:	GraphicsAddress[31:12]
Format:	GraphicsAddress[31:12]			
This address specifies the stereo 3D left eye surface base address bits 31:12.				
	11:0	Restriction		
		This surface must have the same stride, tiling, and panning offset parameters as the right eye surface and meet all the same restrictions.		
	11:0	Reserved		

PRI_OFFSET

PRI_OFFSET			
Register Space:	MMIO: 0/2/0		
Project:	BDW		
Default Value:	0x00000000		
Access:	Double Buffered		
Size (in bits):	32		
Double Buffer Update Point:	Start of vertical blank or pipe not enabled		
Address:	701A4h-701A7h		
Name:	Primary A Offset		
ShortName:	PRI_OFFSET_A		
Power:	Always on		
Reset:	soft		
Address:	711A4h-711A7h		
Name:	Primary B Offset		
ShortName:	PRI_OFFSET_B		
Power:	off/on		
Reset:	soft		
Address:	721A4h-721A7h		
Name:	Primary C Offset		
ShortName:	PRI_OFFSET_C		
Power:	off/on		
Reset:	soft		
This register specifies the panning for the plane surface. The start position is specified in this register as a (x, y) offset from the beginning of the surface. When performing 180 rotation, hardware will internally add the plane size to the offsets so the plane will start displaying from the bottom right corner of the image.			
Restriction			
The plane size + offset must not exceed the maximum supported plane size.			
DWord	Bit	Description	
0	31:28	Reserved	
		Format:	MBZ
	27:16	Start Y Position The vertical offset in lines of the beginning of the active display plane relative to the display surface.	
	15:13	Reserved	
		Format:	MBZ

PRI_OFFSET		
	12:0	Start X Position The horizontal offset in pixels of the beginning of the active display plane relative to the display surface.

PRI_STRIDE

PRI_STRIDE		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Access:	Double Buffered	
Size (in bits):	32	
Double Buffer Update Point:	Start of vertical blank or pipe not enabled; after armed	
Double Buffer Armed Write to PRI_SURF or primary plane not enabled By:		
Address:	70188h-7018Bh	
Name:	Primary A Stride	
ShortName:	PRI_STRIDE_A	
Power:	Always on	
Reset:	soft	
Address:	71188h-7118Bh	
Name:	Primary B Stride	
ShortName:	PRI_STRIDE_B	
Power:	off/on	
Reset:	soft	
Address:	72188h-7218Bh	
Name:	Primary C Stride	
ShortName:	PRI_STRIDE_C	
Power:	off/on	
Reset:	soft	
DWord	Bit	Description
0	31:16	Reserved
	15:6	Stride This field specifies the stride bits 15:6 for the plane. This value is used to determine the line to line increment for the plane data fetches. This field is programmed in units of 64 bytes. This register may be updated through MMIO writes or through command streamer initiated flips.
		Restriction When using linear memory, this must be at least 64 byte aligned. When using tiled memory, this must be at least 512 byte aligned. The stride is limited to a maximum of 32K bytes.
	5:0	Reserved

PRI_SURF

PRI_SURF				
Register Space:	MMIO: 0/2/0			
Project:	BDW			
Default Value:	0x00000000			
Access:	Double Buffered			
Size (in bits):	32			
Double Buffer Update Point:	Start of left or right eye vertical blank (selectable), pipe not enabled, or next plane line request if asynchronous flip			
Address:	7019Ch-7019Fh			
Name:	Primary A Base Address			
ShortName:	PRI_SURF_A			
Power:	Always on			
Reset:	soft			
Address:	7119Ch-7119Fh			
Name:	Primary B Base Address			
ShortName:	PRI_SURF_B			
Power:	off/on			
Reset:	soft			
Address:	7219Ch-7219Fh			
Name:	Primary C Base Address			
ShortName:	PRI_SURF_C			
Power:	off/on			
Reset:	soft			
Writes to this register arm primary registers for this pipe. A write to this register is considered a flip and can cause a flip done interrupt if the interrupt registers are configured for that. The values in this register may be updated through MMIO writes or through command streamer initiated flips. Synchronous updates (synchronous command streamer flips or synchronous MMIO writes) will update the plane surface values at the start of the next vertical blank. Asynchronous updates (asynchronous command streamer flips or asynchronous MMIO writes) will update the plane surface values at the next TLB request or at the start of the next vertical blank. Stereo 3D synchronous updates (stereo 3D command streamer flips or synchronous MMIO writes while stereo 3D is enabled) will update at the start of either the left or right eye vertical blank, selectable by the plane control register stereo surface vblank mask.				
DWord	Bit	Description		
0	31:12	<p>Surface Base Address</p> <table border="1"> <tr> <td>Format:</td><td>GraphicsAddress[31:12]</td></tr> </table> <p>This address specifies the surface base address bits 31:12. In stereo 3D mode this is the right eye base address. In non-stereo 3D mode this is the only base address. It represents an offset from the graphics memory aperture base and is mapped to physical pages through the global GTT.</p>	Format:	GraphicsAddress[31:12]
Format:	GraphicsAddress[31:12]			

PRI_SURF							
	<p>Workaround</p> <p>To prevent false VT-d type 6 errors, use 256KB address alignment and allocate an extra 128 Page Table Entries (PTEs) beyond the end of the displayed surface. Only the PTEs will be used, not the pages themselves.</p>						
<p>Restriction</p> <p>It must be at least 4KB aligned. When performing asynchronous flips and the display surface is in tiled memory, this address must be 256KB aligned.</p>							
11:4	Reserved						
3	<p>Ring Flip Source</p> <p>This bit indicates if the source of the last ring flip was CS or BCS.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0b</td><td>CS</td></tr> <tr> <td>1b</td><td>BCS</td></tr> </tbody> </table>	Value	Name	0b	CS	1b	BCS
Value	Name						
0b	CS						
1b	BCS						
2	Reserved						
1:0	Reserved						

Primitives Generated By VF

IA_PRIMITIVES_COUNT - Primitives Generated By VF		
Register Space: MMIO: 0/2/0 Project: BDW Source: RenderCS Default Value: 0x00000000, 0x00000000 Access: R/W Size (in bits): 64 Trusted Type: 1		
Address: 02318h Valid Projects: BDW		
This register stores the count of primitives generated by VF. This register is part of the context save and restore.		
DWord	Bit	Description
0	63:32	IA Primitives Count Report UDW Total number of primitives output by the Vertex Fetch (IA) stage. This count is updated for every primitive output by the VF stage, as long as Statistics Enable is set in VF_STATE (see the Vertex Fetch Chapter in the 3D Volume.)
	31:0	IA Primitives Count Report LDW Total number of primitives output by the Vertex Fetch (IA) stage. This count is updated for every primitive output by the VF stage, as long as Statistics Enable is set in VF_STATE (see the Vertex Fetch Chapter in the 3D Volume.)

Private PAT

PRIV_PAT - Private PAT																																										
DWord	Bit	Description																																								
0	31:0	<p>Private PAT</p> <table border="1"> <tr> <td>Default Value:</td><td>00000003h</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <table border="1"> <thead> <tr> <th>Description</th><th>Project</th></tr> </thead> <tbody> <tr> <td>Bit[31:8]: Reserved.</td><td></td></tr> <tr> <td>Bit[7:6]: Reserved.</td><td></td></tr> <tr> <td>Bit[5:4]: (See below.)</td><td></td></tr> <tr> <td>00b: Age is 0.</td><td></td></tr> <tr> <td>01b: Age is 1.</td><td></td></tr> <tr> <td>10b: Age is 2.</td><td></td></tr> <tr> <td>11b: Age is 3.</td><td></td></tr> <tr> <td>Bit[3:2]: (See below.)</td><td></td></tr> <tr> <td>00b: eLLC only.</td><td></td></tr> <tr> <td>01b: LLC only.</td><td></td></tr> <tr> <td>10b: LLC and eLLC allowed.</td><td></td></tr> <tr> <td>11b: L3, LLC, and eLLC are allowed.</td><td></td></tr> <tr> <td>Bit[1:0]: (see below):</td><td></td></tr> <tr> <td>00b: Uncacheable (UC).</td><td></td></tr> <tr> <td>01b: Write Combining (WC).</td><td></td></tr> <tr> <td>10b: Write Through (WT).</td><td></td></tr> <tr> <td>11b: Write Back (WB).</td><td></td></tr> </tbody> </table>	Default Value:	00000003h	Access:	R/W	Description	Project	Bit[31:8]: Reserved.		Bit[7:6]: Reserved.		Bit[5:4]: (See below.)		00b: Age is 0.		01b: Age is 1.		10b: Age is 2.		11b: Age is 3.		Bit[3:2]: (See below.)		00b: eLLC only.		01b: LLC only.		10b: LLC and eLLC allowed.		11b: L3, LLC, and eLLC are allowed.		Bit[1:0]: (see below):		00b: Uncacheable (UC).		01b: Write Combining (WC).		10b: Write Through (WT).		11b: Write Back (WB).	
Default Value:	00000003h																																									
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Private PAT

PRIV_PAT-PrivatePAT						
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x00000000 Size (in bits): 32						
DWord	Bit	Description				
0	31:0	Private PAT <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Bit[31:16]: Reserved. Bit[15:8]: PPGTT Private PAT. (See bit[7:0] for definition.)</p> <p>Bit[7:6]: Reserved. Bit[5:4]: (See below.) 00b: Age is 0. 01b: Age is 1. 10b: Age is 2. 11b: Age is 3. Bit[3:2]: (See below.) 00b: Override to eLLC Only. (This setting overrides the memory_object_control_state via surface state to be eLLC target only.) 01b: eLLC only. 10b: LLC only. 11b: eLLC/LLC. Bit[1:0]: (see below): 00b: Uncached with fence. 01b: Write Combining (traditional UC). 10b: Write Through. 11b: Write Back.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

PS Depth Count

PS_DEPTH_COUNT - PS Depth Count		
Register Space: MMIO: 0/2/0 Project: BDW Source: RenderCS Default Value: 0x00000000, 0x00000000 Access: R/W Size (in bits): 64 Trusted Type: 1		
Address: 02350h		
<p>This register stores the value of the count of samples that have passed the depth test. This register is part of the context save and restore. Note that the value of this register can be obtained in a pipeline-synchronous fashion without a pipeline flush by using the 3DCONTROL command. See 3D Overview in the 3D volume.</p>		
DWord	Bit	Description
0..1	63:32	<p>Depth Count UDW</p> <p>This register reflects the total number of samples that have passed the depth test (i.e., will be visible). All samples are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Samples that pass the depth test but fail the stencil test will not be counted.</p>
	31:0	<p>Depth Count LDW</p> <p>This register reflects the total number of samples that have passed the depth test (i.e., will be visible). All samples are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Samples that pass the depth test but fail the stencil test will not be counted.</p>

PS Depth Count for Slice0

PS_DEPTH_COUNT_SLICE0 - PS Depth Count for Slice0		
DWord	Bit	Description
0..1	63:32	<p>Depth Count UDW</p> <p>This register reflects the total number of pixels that have passed the depth test in Slice0(i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.</p>
	31:0	<p>Depth Count LDW</p> <p>This register reflects the total number of pixels that have passed the depth test in Slice0(i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.</p>

PS Depth Count for Slice1

PS_DEPTH_COUNT_SLICE1 - PS Depth Count for Slice1

Register Space:	MMIO: 0/2/0	
Project:	BDW	
Source:	RenderCS	
Default Value:	0x00000000, 0x00000000	
Access:	R/W	
Size (in bits):	64	
Trusted Type:	1	
Address:	022F8h	
<p>This register stores the value of the count of pixels that have passed the depth test in Slice1. This register is part of the context save and restore. This register should not be programmed by SW. Note: In GT3 mode there are two slices Slice0 (Upper Slice) and Slice1 (Lower slice).</p>		
DWord	Bit	Description
0..1	63:32	<p>Depth Count UDW</p> <p>This register reflects the total number of pixels that have passed the depth test in Slice1(i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.</p>
	31:0	<p>Depth Count LDW</p> <p>This register reflects the total number of pixels that have passed the depth test in Slice1(i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.</p>

PS Depth Count for Slice2

PS_DEPTH_COUNT_SLICE2 - PS Depth Count for Slice2		
Register Space: MMIO: 0/2/0 Project: BDW Source: RenderCS Default Value: 0x00000000, 0x00000000 Access: R/W Size (in bits): 64 Trusted Type: 1		
Address: 02450h		
This register stores the value of the count of pixels that have passed the depth test in Slice2. This register is part of the render context save and restore. This register should not be programmed by SW.		
DWord	Bit	Description
0..1	63:32	Depth Count UDW This register reflects the depth test in slice2 (i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.
	31:0	Depth Count LDW This register reflects the depth test in slice2 (i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.

PS Depth Count for Slice3

PS_DEPTH_COUNT_SLICE3 - PS Depth Count for Slice3		
Register Space: MMIO: 0/2/0 Project: BDW Source: RenderCS Default Value: 0x00000000, 0x00000000 Access: R/W Size (in bits): 64 Trusted Type: 1		
Address: 02460h		
This register stores the value of the count of pixels that have passed the depth test in Slice3. This register is part of the render context save and restore. This register should not be programmed by SW.		
DWord	Bit	Description
0..1	63:32	Depth Count UDW This register reflects the depth test in slice3 (i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.
	31:0	Depth Count LDW This register reflects the depth test in slice3 (i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.

PS Invocation Count

PS_INVOCATION_COUNT - PS Invocation Count		
DWord	Bit	Description
0..1	63:32	<p>PS Invocation Count UDW</p> <p>Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.</p>
	31:0	<p>PS Invocation Count LDW</p> <p>Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.</p>

PS Invocation Count for Slice0

PS_INVOCATION_COUNT_SLICE0 - PS Invocation Count for Slice0		
Register Space: MMIO: 0/2/0 Project: BDW Source: RenderCS Default Value: 0x00000000, 0x00000000 Access: R/W Size (in bits): 64 Trusted Type: 1		
Address: 022C8h		
This register stores the value of the count of pixels that get shaded in Slice0. This register is part of the context save and restore. This register should not be programmed by SW. Note: In GT3 mode there are two slices Slice0 (Upper Slice) and Slice1 (Lower slice).		
Workaround		Project
Workaround (BDW bug# 1897768) : HW reports this count 4X the actual value and therefore SW must divide the count by 4 for correct reporting.		BDW
DWord	Bit	Description
0..1	63:32	<p>PS Invocation Count UDW</p> <p>Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice0. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.</p>
	31:0	<p>PS Invocation Count LDW</p> <p>Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice0. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.</p>

PS Invocation Count for Slice1

PS_INVOCATION_COUNT_SLICE1 - PS Invocation Count for Slice1		
Register Space: MMIO: 0/2/0 Project: BDW Source: RenderCS Default Value: 0x00000000, 0x00000000 Access: R/W Size (in bits): 64 Trusted Type: 1		
Address: 022F0h		
This register stores the value of the count of pixels that get shaded in Slice0. This register is part of the context save and restore. This register should not be programmed by SW. Note: In GT3 mode there are two slices Slice0 (Upper Slice) and Slice1 (Lower slice).		
Workaround		Project
Workaround (BDW bug# 1897768) : HW reports this count 4X the actual value and therefore SW must divide the count by 4 for correct reporting.		BDW
DWord	Bit	Description
0..1	63:32	PS Invocation Count UDW Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice1. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.
	31:0	PS Invocation Count LDW Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice1. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.

PS Invocation Count for Slice2

PS_INVOCATION_COUNT_SLICE2 - PS Invocation Count for Slice2		
Register Space: MMIO: 0/2/0 Project: BDW Source: RenderCS Default Value: 0x00000000, 0x00000000 Access: R/W Size (in bits): 64 Trusted Type: 1		
Address: 02448h		
This register stores the value of the count of pixels that get shaded in Slice2. This register is part of the render context save and restore. This register should not be programmed by SW.		
DWord	Bit	Description
0..1	63:32	<p>PS Invocation Count UDW</p> <p>Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice2. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.</p>
	31:0	<p>PS Invocation Count LDW</p> <p>Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice2. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.</p>

PS Invocation Count for Slice3

PS_INVOCATION_COUNT_SLICE3 - PS Invocation Count for Slice3		
Register Space: MMIO: 0/2/0 Project: BDW Source: RenderCS Default Value: 0x00000000, 0x00000000 Access: R/W Size (in bits): 64 Trusted Type: 1		
Address: 02458h		
This register stores the value of the count of pixels that get shaded in Slice3. This register is part of the render context save and restore. This register should not be programmed by SW.		
DWord	Bit	Description
0..1	63:32	PS Invocation Count UDW Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice3. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.
	31:0	PS Invocation Count LDW Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice3. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.

PTE SW Fault Repair High

PTESWC_H - PTE SW Fault Repair High								
Register Space:	MMIO: 0/2/0							
Project:	BDW							
Default Value:	0x00000000							
Size (in bits):	32							
Address:	04104h							
DWord	Bit	Description						
0	31:0	<p>PTE SW Fault Repair High</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> <tr> <td colspan="2">Fixed PTE entry is written by SW here.</td></tr> </table>	Default Value:	00000000h	Access:	R/W	Fixed PTE entry is written by SW here.	
Default Value:	00000000h							
Access:	R/W							
Fixed PTE entry is written by SW here.								

PTE SW Fault Repair Low

<u>PTESWC_L-PTESWFaultRepairLow</u>						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04100h					
DWord	Bit	Description				
0	31:0	<p>PTE SW Fault Repair Low</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Fixed PTE entry is written by SW here.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

Push Bus Metric Control

PUSHBUS_CONTROL - Push Bus Metric Control

Register Space: MMIO: 0/2/0

Project: BDW

Default Value: 0x00000000

Size (in bits): 32

Address: 0A248h

Control bits for Metric Generation on Push Bus.

Register is locked by PUSHBUS_CONTROL.LOCK

Register is not reset by FLR.

DWord	Bit	Description	
0	31	Push Bus Metric Lock	
		Access:	R/W Lock
		Controls whether Push Bus Registers are writeable. 0: Registers are writeable (unlocked). 1: Writes to registers have no effect (locked). Lock bit cannot be cleared without cold reset (i.e., writing a 0 after having written a 1 does not clear the lock).	
	30:7	Reserved	Access: RO
	6	Mask VECS in C0 Residency Calculation	Access: R/W Lock
		Mask VECS in C0 Residency Calculation. 0: Include agent in calculation (default). 1: Mask agent off in calculation.	
	5	Mask VCS1 in C0 Residency Calculation	Access: R/W Lock
		Mask VCS1 in C0 Residency Calculation. 0: Include agent in calculation (default). 1: Mask agent off in calculation.	
	4	Mask VCS0 in C0 Residency Calculation	Access: R/W Lock
		Mask VCS0 in C0 Residency Calculation. 0: Include agent in calculation (default). 1: Mask agent off in calculation.	

PUSHBUS_CONTROL - Push Bus Metric Control				
	3	Mask WIN in C0 Residency Calculation <table border="1"> <tr> <td>Access:</td><td>R/W Lock</td></tr> </table> <p>Mask WIN in C0 Residency Calculation. 0: Include agent in calculation (default). 1: Mask agent off in calculation.</p>	Access:	R/W Lock
Access:	R/W Lock			
	2	C0 Residency Time Enable <table border="1"> <tr> <td>Access:</td><td>R/W Lock</td></tr> </table> <p>C0 Residency Time Enable. 0: Counter reflects number of GT core clocks (default). 1: Counter reflects number of 1280 ns periods.</p>	Access:	R/W Lock
Access:	R/W Lock			
	1	Video Busyness/C1 Residency Time Enable <table border="1"> <tr> <td>Access:</td><td>R/W Lock</td></tr> </table> <p>Video Busyness/C1 Residency Time Enable. 0: Counter reflects number of GT core clocks (default). 1: Counter reflects number of 1280 ns periods</p>	Access:	R/W Lock
Access:	R/W Lock			
	0	C1 Residency Select <table border="1"> <tr> <td>Access:</td><td>R/W Lock</td></tr> </table> <p>C1 Residency Select. 0: Video Busyness metric selected (default). 1: C1 Residency metric selected.</p>	Access:	R/W Lock
Access:	R/W Lock			

Push Bus Metric Counter Enable

PUSHBUS_ENABLE - Push Bus Metric Counter Enable

Register Space: MMIO: 0/2/0

Project: BDW

Default Value: 0x00000000

Size (in bits): 32

Address: 0A250h

Enables the counter for each metric; note that it does not control the metric generation logic.

Field Encoding per Metric:

0: Accumulator in PM disabled and held at zero (default).

1: Accumulator in PM is enabled.

Register is locked by PUSHBUS_CONTROL.LOCK.

Register is not reset by FLR.

DWord	Bit	Description	
0	31:9	Reserved	
	Access:		RO
	8	Reserved	
	Project:	BDW	
	Access:		RO
	7	Push Bus Counter Enable for GFX Read LLC Metric	
	Access:	R/W Lock	
	6	Push Bus Counter Enable for GFX Write LLC Metric	
	Access:	R/W Lock	
	5	Push Bus Counter Enable for GFX Read eDRAM Metric	
	Access:	R/W Lock	
	4	Push Bus Counter Enable for GFX Write eDRAM Metric	
	Access:	R/W Lock	
	3	Push Bus Counter Enable for GFX RW DRAM Metric	
	Access:	R/W Lock	
	2	Push Bus Counter Enable for C0 Residency Metric	
	Access:	R/W Lock	
	1	Push Bus Counter Enable for Memory Bound Count Metric	
	Access:	R/W Lock	
	0	Push Bus Counter Enable for Video Busyness/C1 Residency Metric	
	Access:	R/W Lock	

Push Bus Metric Counter Overflow

PUSHBUS_OVERFLOW - Push Bus Metric Counter Overflow		
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x00000000 Size (in bits): 32		
Address: 0A258h		
Sticky bit to indicate that the activity counter has overflowed. Clear overflow bit by writing a 1 to it.		
Field Encoding per Metric:		
0: Activity register has not overflowed (default).		
1: Activity register has overflowed (sticky).		
Register is not reset by FLR.		
DWord	Bit	Description
0	31:9	Reserved
		Access: RO
	8	Reserved
		Project: BDW
		Access: RO
	7	Push Bus Overflow Indication for GFX Read LLC Metric
		Access: R/WC
	6	Push Bus Overflow Indication for GFX Write LLC Metric
		Access: R/WC
	5	Push Bus Overflow Indication for GFX Read eDRAM Metric
		Access: R/WC
	4	Push Bus Overflow Indication for GFX Write eDRAM Metric
		Access: R/WC
	3	Push Bus Overflow Indication for GFX RW DRAM Metric
		Access: R/WC
	2	Push Bus Overflow Indication for C0 Residency Metric
		Access: R/WC
	1	Push Bus Overflow Indication for Memory Bound Count Metric
		Access: R/WC
	0	Push Bus Overflow Indication for Video Busyness/C1 Residency Metric
		Access: R/WC

Push Bus Metric Counter Shift Value

PUSHBUS_SHIFT - Push Bus Metric Counter Shift Value		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A25Ch	
This field determines how the input to the activity counter is shifted. It is used to amplify the importance of each metric event.		
Field Encoding per Metric:		
00b:	No shift (default).	
01b:	Shift by 1 bit left.	
10b:	Shift by 2 bits left.	
11b:	Shift by 3 bits left.	
Register is locked by PUSHBUS_CONTROL.LOCK.		
Register is not reset by FLR.		
DWord	Bit	Description
0	31:18	Reserved
		Access: RO
	17:16	Reserved
		Project: BDW
		Access: RO
	15:14	Push Bus Shift Value for GFX Read LLC Metric
		Access: R/W Lock
	13:12	Push Bus Shift Value for GFX Write LLC Metric
		Access: R/W Lock
	11:10	Push Bus Shift Value for GFX Read eDRAM Metric
		Access: R/W Lock
	9:8	Push Bus Shift Value for GFX Write eDRAM Metric
		Access: R/W Lock
	7:6	Push Bus Shift Value for GFX RW DRAM Metric
		Access: R/W Lock
	5:4	Push Bus Shift Value for C0 Residency Metric
		Access: R/W Lock
	3:2	Push Bus Shift Value for Memory Bound Count Metric
		Access: R/W Lock
	1:0	Push Bus Shift Value for Video Busyness/C1 Residency Metric
		Access: R/W Lock

Push Bus Metric Event Override

PUSHBUS_OVERRIDE - Push Bus Metric Event Override		
DWord	Bit	Description
0	31:9	Reserved
		Access: RO
	8	Reserved
		Project: BDW
		Access: RO
	7	Push Bus Override for GFX Read LLC Metric
		Access: R/W Lock
	6	Push Bus Override for GFX Write LLC Metric
		Access: R/W Lock
	5	Push Bus Override for GFX Read eDRAM Metric
		Access: R/W Lock
	4	Push Bus Override for GFX Write eDRAM Metric
		Access: R/W Lock
	3	Push Bus Override for GFX RW DRAM Metric
		Access: R/W Lock
	2	Push Bus Override for C0 Residency Metric
		Access: R/W Lock
	1	Push Bus Override for Memory Bound Count Metric
		Access: R/W Lock
	0	Push Bus Override for Video Busyness/C1 Residency Metric
		Access: R/W Lock

PWRCTXSAVE Message Register for Boot Controller Unit

MSG_PWRCTXSAVE - PWRCTXSAVE Message Register for Boot Controller Unit

Register Space: MMIO: 0/2/0

Project: BDW

Default Value: 0x00000000

Size (in bits): 32

Address: 0850Ch

Message registers have bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16].

To set bit0, for example, the data would be 0x0001_0001.

To clear bit0, for example, the data would be 0x0001_0000.

Note that mask bit is the data bit offset + 16.

Message registers are protected from non-GT writes via the Message Channel.

DWord	Bit	Description	
0	31:10	RSVD	
		Access:	RO
	9	Power Context Save Request	
		Access:	R/W
		Power Context Save Request 1'b0: Power context save is not being requested (default). 1'b1: Power context save is being requested. Unit needs to self-clear this bit upon sampling.	
	8:0	QWord Credits for Power Context Save Request	
		Access:	R/W
		QWord Credits for Power Context Save Request. Minimum Credits = 1: Unit may send 1 QWord pair (enough for first LRI at least). Maximum Credits = 511: Unit may send 511 QWord pairs. A QWord pair is defined as a 32-bit register address and the corresponding 32-bits of register data. Note that the LRI header and END commands are 64-bits each (32-bit command followed by 32-bit NOOP) and consume one QWord credit. Only valid with PWRCTXSAVE_REQ (Bit9).	

PWRCTXSAVE Message Register for Power Management Unit

MSG_PWRCTXSAVE_GPM - PWRCTXSAVE Message Register for Power Management Unit

Register Space: MMIO: 0/2/0

Project: BDW

Default Value: 0x00000000

Size (in bits): 16

Address: 08044h

Message registers have bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16].

To set bit0, for example, the data would be 0x0001_0001.

To clear bit0, for example, the data would be 0x0001_0000.

Note that mask bit is the data bit offset + 16.

Message registers are protected from non-GT writes via the Message Channel.

DWord	Bit	Description	
0	15:10	Reserved	Access: RO
	9	Power Context Save Request	Access: R/W Power Context Save Request. 1'b0: Power context save is not being requested (default). 1'b1: Power context save is being requested. Unit needs to self-clear this bit upon sampling.
	8:0	QWord Credits for Power Context Save Request	Access: R/W QWord Credits for Power Context Save Request. Minimum Credits = 1: Unit may send 1 QWord pair (enough for first LRI at least). Maximum Credits = 511: Unit may send 511 QWord pairs A QWord pair is defined as a 32-bit register address and the corresponding 32-bits of register data. Note that the LRI header and END commands are 64-bits each (32-bit command followed by 32-bit NOOP) and consume one QWord credit. Only valid with PWRCTXSAVE_REQ (Bit9).

RAM Clock Gating Control 1

RCGCTL1 - RAM Clock Gating Control 1				
DWord	Bit	Description		
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x00000100 Size (in bits): 32				
Address: 09410h				
RAM Clock Gating Control Registers.(Not Ctx save on BDW A0 for slice shutdown)				
0	31	<p>USBunit RAM Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>USBunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W			
0	30	<p>VLFunit RAM Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>VLFunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W			
0	29	<p>VISunit RAM Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>VISunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W			
0	28	<p>STCunit RAM Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>STCunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W			

RCGCTL1 - RAM Clock Gating Control 1

	TDSunit RAM Clock Gating Disable		
27	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px; text-align: right;">R/W</td> </tr> </table> <p>TDSunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
26	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px; text-align: right;">R/W</td> </tr> </table> <p>VMCunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
25	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px; text-align: right;">R/W</td> </tr> </table> <p>QRCunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
24	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px; text-align: right;">R/W</td> </tr> </table> <p>SCunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
23	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px; text-align: right;">R/W</td> </tr> </table> <p>SVLunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
22	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px; text-align: right;">R/W</td> </tr> </table> <p>VFunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

RCGCTL1 - RAM Clock Gating Control 1

	URBunit RAM Clock Gating Disable		
21	<table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>URBunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
20	GAMWunit RAM Clock Gating Disable <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>GAMWunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
19	SVGunit RAM Clock Gating Disable <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>SVGunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
18	RCZunit RAM Clock Gating Disable <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>RCZunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
17	RCPBEunit RAM Clock Gating Disable <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>RCPBEunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
16	RCCunit RAM Clock Gating Disable <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>RCCunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

RCGCTL1 - RAM Clock Gating Control 1

	PSDunit RAM Clock Gating Disable		
15	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px; text-align: right;">R/W</td> </tr> </table> <p>PSDunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
14	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px; text-align: right;">R/W</td> </tr> </table> <p>MTunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
13	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px; text-align: right;">R/W</td> </tr> </table> <p>SBEunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
12	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px; text-align: right;">R/W</td> </tr> </table> <p>IZunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
11	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px; text-align: right;">R/W</td> </tr> </table> <p>IECPunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
10	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px; text-align: right;">R/W</td> </tr> </table> <p>ICunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

RCGCTL1 - RAM Clock Gating Control 1

	HIZunit RAM Clock Gating Disable	
9	Access: HIZunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	R/W
GAMunit RAM Clock Gating Disable		
8	Default Value: Access: GAMunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	1b R/W
7	BCunit RAM Clock Gating Disable	
	Access: BCunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	R/W
6	HDCunit RAM Clock Gating Disable	
	Access: GAFSunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	R/W
5	DMunit RAM Clock Gating Disable	
	Access: DMunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	R/W
4	WMFEunit RAM Clock Gating Disable	
	Access: WMFEunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	R/W

RCGCTL1 - RAM Clock Gating Control 1

	3	CSunit RAM Clock Gating Disable	Access:	R/W
CSunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)				
2				
	2	BLBunit RAM Clock Gating Disable	Access:	R/W
BLBunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)				
1				
	1	MPCunit RAM Clock Gating Disable	Access:	R/W
MPCunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)				
0				
	0	BFunit RAM Clock Gating Disable	Access:	R/W
BFunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)				

RAM Clock Gating Control 2

RCGCTL2 - RAM Clock Gating Control 2		
Register Space:	MMIO: 0/2/0	
Project:	BDW 0xFFC00000 [BDW:GT1, BDW:GT2, BDW:GT3:H, BDW:GT3E]	
Size (in bits):	32	
Address:	09414h	
RAM Clock Gating Control Registers.(Not Ctx save on BDW A0 for slice shutdown)		
DWord	Bit	Description
0	31	1x2X Assign fub XOR clock gate disable
		Default Value: 1b
		Project: BDW
		Access: R/W
		XOR based unit level clock gating disable in 1x2x_asgn fub: '0' : XOR Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : XOR Clock Gating Disabled. (i.e., clocks are toggling, always) This bit should be programmed to a 1 for BDW:B0
	30:28	VMCRunit clock gate disable
		Default Value: 111b
		Access: R/W
		VMCR unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	27:25	SMCRunit clock gate disable
		Default Value: 111b
		Access: R/W
		SMCR unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

RCGCTL2 - RAM Clock Gating Control 2

	MCRunit clock gate disable				
24:22	<table border="1" style="width: 100%;"> <tr> <td>Default Value:</td><td>111b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>MCR unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Default Value:	111b	Access:	R/W
Default Value:	111b				
Access:	R/W				
21	MUCunit RAM clock gate disable <table border="1" style="width: 100%;"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>MUC unit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W		
Access:	R/W				
20	WVISunit clock gate disable <table border="1" style="width: 100%;"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>WVIS unit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W		
Access:	R/W				
19	WAVM unit RAM clock gate disable <table border="1" style="width: 100%;"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>WAVM unit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W		
Access:	R/W				
18	WHME unit RAM clock gate disable bit <table border="1" style="width: 100%;"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>WHME unit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W		
Access:	R/W				
17	WIME unit RAM clock gate disable <table border="1" style="width: 100%;"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>WIME unit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W		
Access:	R/W				

RCGCTL2 - RAM Clock Gating Control 2

	16	WMPC unit RAM clock gating disable	Access:	R/W
WMPC unit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)				
15 SDEunit RAM clock gate disable				
	15	Access:	R/W	
SDE unit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)				
14 VSHM unit clock gate disable				
	14	Access:	R/W	
VSHM unit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)				
13 DAPRTS unit RAM clock gate disable				
	13	Access:	R/W	
DAPRTS unit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled.				
12 GS unit RAM clock gate disable				
	12	Access:	R/W	
GS unit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)				
11 Reserved				
10 GAMTunit RAM clock gate disable bit				
	10	Access:	R/W	
GAMT unit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)				

RCGCTL2 - RAM Clock Gating Control 2

	9 VCW unit RAM clock gate disable		
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px; text-align: right;">R/W</td> </tr> </table> <p>VCW unit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
	8 VEO unit RAM clock gate disable		
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px; text-align: right;">R/W</td> </tr> </table> <p>VEO unit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
	7 IMEunit RAM clock gate disable		
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px; text-align: right;">R/W</td> </tr> </table> <p>IMEunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
	6 CREunit RAM clock gate disable		
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px; text-align: right;">R/W</td> </tr> </table> <p>CREunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
	5 RSunit RAM clock gate disable		
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px; text-align: right;">R/W</td> </tr> </table> <p>RSunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
	4 MSCunit RAM Clock Gating Disable		
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px; text-align: right;">R/W</td> </tr> </table> <p>MSCunit RAM Clock Gating Disable Control '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

RCGCTL2 - RAM Clock Gating Control 2

	3	VMXunit RAM Clock Gating Disable	
		Access:	R/W
		VMXunit RAM Clock Gating Disable Control '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	2	GAunit RAM Clock Gating Disable for all EUs	
		Access:	R/W
		GAunit RAM Clock Gating Disable Control For all EUs in each Row: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	1	VSunit RAM Clock Gating Disable	
		Access:	R/W
		VSunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	0	HSunit RAM Clock Gating Disable	
		Access:	R/W
		HSunit RAM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	

RAWCLK_FREQ

RAWCLK_FREQ													
Register Space: MMIO: 0/2/0 Project: DevLPT Default Value: 0x00000800 Access: R/W Size (in bits): 32													
Address: C6204h-C6207h Name: Rawclk Frequency ShortName: RAWCLK_FREQ Power: Always on Reset: soft													
DWord	Bit	Description											
0	31:15	Reserved Format: MBZ											
	14:10	Reserved <table border="1"> <tr> <td>Project:</td><td>DevLPT:H</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	DevLPT:H	Format:	MBZ							
Project:	DevLPT:H												
Format:	MBZ												
14:10	Deglitch Amount <table border="1"> <tr> <td>Default Value:</td><td>00010b 2 clks</td></tr> <tr> <td>Project:</td><td>DevLPT:LP</td></tr> </table> <p>This field specifies the deglitch amount for GTC.</p>	Default Value:	00010b 2 clks	Project:	DevLPT:LP								
Default Value:	00010b 2 clks												
Project:	DevLPT:LP												
9:0	Rawclk frequency <table border="1"> <thead> <tr> <th>Description</th><th>Project</th></tr> </thead> <tbody> <tr> <td>Program this field to match the rawclk frequency. This is used to generate a divided down clock for miscellaneous timers in display.</td><td></td></tr> <tr> <td>Raw Clock = 125 MHz</td><td>DevLPT:H</td></tr> <tr> <td>Raw Clock = 24 MHz</td><td>DevLPT:LP</td></tr> </tbody> </table> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>00000000000b</td><td>0</td></tr> </tbody> </table>	Description	Project	Program this field to match the rawclk frequency. This is used to generate a divided down clock for miscellaneous timers in display.		Raw Clock = 125 MHz	DevLPT:H	Raw Clock = 24 MHz	DevLPT:LP	Value	Name	00000000000b	0
Description	Project												
Program this field to match the rawclk frequency. This is used to generate a divided down clock for miscellaneous timers in display.													
Raw Clock = 125 MHz	DevLPT:H												
Raw Clock = 24 MHz	DevLPT:LP												
Value	Name												
00000000000b	0												

RCC LRA 0

RCC_LRA_0 - RCC LRA 0						
DWord	Bit	Description				
0	31:24	<p>RCC LRA1 Max</p> <table border="1"> <tr> <td>Default Value:</td><td>11011111b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Maximum value of programmable LRA1.</p>	Default Value:	11011111b	Access:	R/W
Default Value:	11011111b					
Access:	R/W					
23:16	<p>RCC LRA1 Min</p> <table border="1"> <tr> <td>Default Value:</td><td>01100000b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Minimum value of programmable LRA1.</p>	Default Value:	01100000b	Access:	R/W	
Default Value:	01100000b					
Access:	R/W					
15:8	<p>RCC LRA0 Max</p> <table border="1"> <tr> <td>Default Value:</td><td>01011111b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Maximum value of programmable LRA0.</p>	Default Value:	01011111b	Access:	R/W	
Default Value:	01011111b					
Access:	R/W					
7:0	<p>RCC LRA0 Min</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Minimum value of programmable LRA0.</p>	Default Value:	00000000b	Access:	R/W	
Default Value:	00000000b					
Access:	R/W					

RCC LRA 1

RCC_LRA_1 - RCC LRA 1					
DWord	Bit	Description			
0	31:2	Reserved			
		<table border="1"> <tr> <td>Default Value:</td><td>00000000000000000000000000000000b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	00000000000000000000000000000000b	Access:
Default Value:	00000000000000000000000000000000b				
Access:	RO				
1	MSC LRA <table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Which LRA should MSC use.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b				
Access:	R/W				
0	RCC LRA <table border="1"> <tr> <td>Default Value:</td><td>1b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Which LRA should RCC use.</p>	Default Value:	1b	Access:	R/W
Default Value:	1b				
Access:	R/W				

RCC Virtual page Address Registers

RCCTLB_VA - RCC Virtual page Address Registers				
Register Space:	MMIO: 0/2/0			
Project:	BDW			
Source:	RenderCS			
Default Value:	0x00000000			
Access:	RO			
Size (in bits):	32			
Trusted Type:	1			
Address:	04A00h-04A03h			
These registers are directly mapped to the current Virtual Addresses in the RCCTLB (Render Cache for Color TLB).				
DWord	Bit	Description		
0	31:12	Address		
		<table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>GraphicsAddress[31:12]</td></tr> </table> <p>Page virtual address.</p>	Project:	All
Project:	All			
Format:	GraphicsAddress[31:12]			
	11:0	Reserved		
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	BDW
Project:	BDW			
Format:	MBZ			

RC EI Counter

RC_STATUS1 - RC EI Counter		
DWord	Bit	Description
0	31:24	Reserved
	23:0	RC EI Counter Access: R/W pmcr_rc_ei_store[23:0].

RC Evaluation Interval

RC_EI - RC Evaluation Interval				
DWord	Bit	Description		
0	31:24	Reserved <table border="1"> <tr> <td>Access:</td><td>RO</td></tr> </table>	Access:	RO
Access:	RO			
23:0	Render Standby Evaluation Interval <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>0 = 0 usec. 1 = 1.28 usec. 2 = 2.56 usec. 3 = 3.84 usec. FF FFFF = 21.474 sec. pmcr_rc_ei[23:0].</p>	Access:	R/W	
Access:	R/W			

RC Idle Counter

RC_STATUS2 - RC Idle Counter		
DWord	Bit	Description
0	31:24	Reserved Access: RO
	23:0	RC Idle Counter Access: R/W pmcr_rc_idle_counter_store[23:0].

RC Idle Hysteresis

RC_IDLE_HYSTERESIS - RC Idle Hysteresis				
DWord	Bit	Description		
0	31:24	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
Access:	RO			
23:0	<p>RC Idle Hysteresis Detection</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Idle intervals must be longer than this value to be considered idle. 0 = 0 usec means disabled. 1 = 1.28 usec. 2 = 2.56 usec. 3 = 3.84 usec. FF FFFF = 21.474 sec.</p> <p>This must not be set to more than 5ms to prevent the PCU from timing out on an S state entry.</p>	Access:	R/W	
Access:	R/W			

RC Promotion Timer for RC1e

RC_PROMO_TIME0 - RC Promotion Timer for RC1e				
DWord	Bit	Description		
0	31:24	Reserved <table border="1"> <tr> <td>Access:</td><td>RO</td></tr> </table>	Access:	RO
Access:	RO			
23:0	Promotion Timer for RC1e <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Absolute time starting from post-hyst idle. 0 = 0 usec. 1 = 1.28 usec. 2 = 2.56 usec. 3 = 3.84 usec. FF FFFF = 21.474 sec.</p>	Access:	R/W	
Access:	R/W			

RC Promotion Timer for RC6

RC_PROMO_TIME1 - RC Promotion Timer for RC6				
DWord	Bit	Description		
0	31:24	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
Access:	RO			
23:0	<p>Promotion Timer for RC6</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Absolute time starting from post-hyst idle. 0 = 0 usec. 1 = 1.28 usec. 2 = 2.56 usec. 3 = 3.84 usec. FF FFFF = 21.474 sec.</p>	Access:	R/W	
Access:	R/W			

RC Promotion Timer for RC6p (Deeper RC6)

RC_PROMO_TIME2 - RC Promotion Timer for RC6p (Deeper RC6)				
DWord	Bit	Description		
0	31:24	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
Access:	RO			
23:0	Promotion Timer for RC6p (Deeper RC6) <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Bits 23_0 Reserved field for Broadwell. Pre-Broadwell field description as below. Absolute time starting from post-hyst idle. 0 = 0 usec. 1 = 1.28 usec. 2 = 2.56 usec. 3 = 3.84 usec. FF FFFF = 21.474 sec. Bits 23_0 Reserved field for Broadwell.</p>	Access:	R/W	
Access:	R/W			

RC Promotion Timer for RC6pp (Deepest RC6)

RC_PROMO_TIME3 - RC Promotion Timer for RC6pp (Deepest RC6)				
DWord	Bit	Description		
0	31:24	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
Access:	RO			
23:0	<p>Promotion Timer for RC6pp (Deepest RC6)</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Bits 23_0 Reserved field for Broadwell. Pre-Broadwell field description as below. Absolute time starting from post-hyst idle. 0 = 0 usec. 1 = 1.28 usec. 2 = 2.56 usec. 3 = 3.84 usec. FF FFFF = 21.474 sec. Bits 23_0 Reserved field for Broadwell.</p>	Access:	R/W	
Access:	R/W			

RCS_PREEMPTION_HINT

RCS_PREEMPTION_HINT - RCS_PREEMPTION_HINT	
Register Space:	MMIO: 0/2/0
Project:	BDW
Source:	RenderCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	024BCh
Description	Project
This register contains the Head pointer offset in to the Ring Buffer or the Dword aligned Graphics address in to the Batch Buffer corresponding to either MI_ARB_CHECK called Preemption Hint Address. When Preemption Hint Address is enabled, RCS will honor UHPTTR only on parsing MI_ARB_CHK at Preemption Hint Address.	
This register contains the Head pointer offset into the Ring Buffer or the Dword aligned Graphics address into the Batch Buffer corresponding to the below listed commands in execlist mode of operation <ul style="list-style-type: none"> • MI_ARB_CHECK • MI_WAIT_FOR_EVENT • MI_SEMAPHORE_WAIT • 3D_PRIMITIVE • GPGPU_WALKER • MEDIA_STATE_FLUSH • PIPE_CONTROL (Only in GPGPU mode of pipeline selection) • MI_ATOMIC (Post Sync Operation set in GPGPU mode of pipeline selection) • MI_SEMAPHORE_SIGNAL (Post Sync Operation set in GPGPU mode of pipeline selection) 	BDW
Programming Notes	Project
Programming Restriction: This register should NEVER be programmed in functional mode, this should be used only in validation mode to achieve deterministic behavior of UHPTTR being sampled by a given MI_ARB_CHECK in command stream. Programmer has to ensure that RCS Preemption Hint register gets programmed before UHPTTR is programmed and well before RCS crosses the corresponding execution point. Preemption hint for both RingBuffer and Batch Buffer can't be enabled simultaneously.	
User must ensure the Preempted Hint Address programmed matches either Ring Head Offset or Batch Buffer Graphics Virtual Address and not both of them. User must also ensure the Preempted Hint Address[19:0] programmed matches either Ring Head Offset[19:0] or Batch Buffer Graphics Virtual Address[19:0] and not both of them.	BDW

RCS_PREEMPTION_HINT - RCS_PREEMPTION_HINT																		
DWord	Bit	Description																
0	31:2	<p>Preempted Hint Address</p> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>U30</td></tr> </table> <p>This field contains the Head offset in to the Ring Buffer when Preemption Hint is set to Ring Buffer and Dword aligned Graphics Address in to the batch buffer when Preemption Hint is set to Batch Buffer.</p>	Project:	BDW	Format:	U30												
Project:	BDW																	
Format:	U30																	
	1	<p>Batch Buffer Preemption Hint</p> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>Enabled</td></tr> </table> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th><th>Project</th></tr> </thead> <tbody> <tr> <td>0h</td><td>Disabled</td><td>Preemption hint is disabled in batch buffer.</td><td>BDW</td></tr> <tr> <td>1h</td><td>Enabled</td><td>Preemption hint is enabled in ring buffer and preemption hint address corresponds to the instruction in Batch Buffer.</td><td>BDW</td></tr> </tbody> </table>	Project:	BDW	Format:	Enabled	Value	Name	Description	Project	0h	Disabled	Preemption hint is disabled in batch buffer.	BDW	1h	Enabled	Preemption hint is enabled in ring buffer and preemption hint address corresponds to the instruction in Batch Buffer.	BDW
Project:	BDW																	
Format:	Enabled																	
Value	Name	Description	Project															
0h	Disabled	Preemption hint is disabled in batch buffer.	BDW															
1h	Enabled	Preemption hint is enabled in ring buffer and preemption hint address corresponds to the instruction in Batch Buffer.	BDW															
	0	<p>Ring Preemption Hint</p> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>Enable</td></tr> </table> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th><th>Project</th></tr> </thead> <tbody> <tr> <td>0h</td><td>Disable</td><td>Preemption hint is disabled in ring buffer.</td><td>BDW</td></tr> <tr> <td>1h</td><td>Enabled</td><td>Preemption hint is enabled in ring buffer and preemption hint address corresponds to the instruction in Ring Buffer.</td><td>BDW</td></tr> </tbody> </table>	Project:	BDW	Format:	Enable	Value	Name	Description	Project	0h	Disable	Preemption hint is disabled in ring buffer.	BDW	1h	Enabled	Preemption hint is enabled in ring buffer and preemption hint address corresponds to the instruction in Ring Buffer.	BDW
Project:	BDW																	
Format:	Enable																	
Value	Name	Description	Project															
0h	Disable	Preemption hint is disabled in ring buffer.	BDW															
1h	Enabled	Preemption hint is enabled in ring buffer and preemption hint address corresponds to the instruction in Ring Buffer.	BDW															

RCS_PREEMPTION_HINT_UDW

RCS_PREEMPTION_HINT_UDW - RCS_PREEMPTION_HINT_UDW				
Register Space:	MMIO: 0/2/0			
Project:	BDW			
Source:	RenderCS			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Address:	024C8h			
<p>This register contains the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space of the Batch Buffer corresponding to MI_ARB_CHECK command called Preemption Hint Address.</p>				
Programming Notes				
Programming Restriction: This register should NEVER be programmed in functional mode, this should be used only in validation mode to achieve deterministic behavior of UHPTR being sampled by a given MI_ARB_CHK in command stream.				
DWord	Bit	Description		
0	31:16	Reserved <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Format:</td> <td style="padding: 2px;">MBZ</td> </tr> </table>	Format:	MBZ
Format:	MBZ			
15:0	Preempted Hint Address Upper DWORD <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Format:</td> <td style="padding: 2px;">GraphicsAddress[47:32]</td> </tr> </table> <p>This field contains the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space of the batch buffer when Preemption Hint is set to Batch Buffer. This field is not valid when Preemption Hint is set to Ring Buffer.</p>	Format:	GraphicsAddress[47:32]	
Format:	GraphicsAddress[47:32]			

RCS Batch Buffer State Register

RCS_BB_STATE - RCS Batch Buffer State Register												
Register Space: MMIO: 0/2/0 Project: BDW Source: RenderCS Default Value: 0x00000000 [BDW] Access: RO Size (in bits): 32												
Address: 02110h												
<p>This register contains the attributes of the current batch buffer initiated from the Ring Buffer.</p> <p>This register should not be written by software. These fields should only get written by a context restore. Software should always set these fields via the MI_BATCH_BUFFER_START command when initiating a batch buffer. This register is saved and restored with context.</p>												
DWord	Bit	Description										
0	31:9	<p>Reserved</p> <table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ								
Format:	MBZ											
8	<p>Reserved</p> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	BDW	Format:	MBZ							
Project:	BDW											
Format:	MBZ											
7	<p>Resource Streamer Enable</p> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>U1</td></tr> </table> <p>When this bit is set, the Resource Streamer will execute the batch buffer. When this bit is clear the Resource Streamer will not execute the batch buffer.</p>	Project:	BDW	Format:	U1							
Project:	BDW											
Format:	U1											
6	Reserved											
5	<p>Address Space Indicator</p> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> </table> <p>Note: This field reflects the effective address space indicator security level and may not be the same as the Address Space Indicator written using MI_BATCH_BUFFER_START.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0h</td><td>GGTT [Default]</td><td>This Batch buffer is located in GGTT memory and is privileged</td></tr> <tr> <td>1h</td><td>PPGTT</td><td>This Batch buffer is located in PPGTT memory and is non-privileged.</td></tr> </tbody> </table>	Project:	BDW	Value	Name	Description	0h	GGTT [Default]	This Batch buffer is located in GGTT memory and is privileged	1h	PPGTT	This Batch buffer is located in PPGTT memory and is non-privileged.
Project:	BDW											
Value	Name	Description										
0h	GGTT [Default]	This Batch buffer is located in GGTT memory and is privileged										
1h	PPGTT	This Batch buffer is located in PPGTT memory and is non-privileged.										
4	<p>Reserved</p> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	BDW	Format:	MBZ							
Project:	BDW											
Format:	MBZ											
3:0	<p>Reserved</p> <table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ									
Format:	MBZ											

RCS Context Preemption Hint

RCS_CTXID_PREEMPTION_HINT - RCS Context PreemptionHint

Register Space: MMIO: 0/2/0

Project: BDW

Source: RenderCS

Default Value: 0x00000000

Access: R/W

Size (in bits): 32

Address: 024CCh

This register contains the Context ID of a context in execlist mode of operation. In execlist mode of operation RCS_PREEMPTION_HINT and RS_PREEMPTION_HINT registers are looked at by Render Command Streamer and Resource Streamer only on executing a context having Context ID that matches with the contents of this register. This register contents are valid and looked at only in execlist mode of operation

Programming Restriction:

This register should NEVER be programmed in functional mode, this must be used only in validation mode to achieve deterministic preemption behavior in execlist mode of operation.

DWord	Bit	Description	
0	31:0	Context ID Preemption Hint Format:	U32 If 0 this field has no effect. If nonzero it indicates the only context ID that can be preempted when execlists are enabled. A preemption attempt when the context ID of the currently executing ring context does not match this field will be ignored.

RC Wake Counter

RC_STATUS0 - RC Wake Counter		
DWord	Bit	Description
0	31:16	Reserved Access: RO
	15:0	RC Wake Counter Access: RO Incremented for each wake event, wraps around.

RC Wake Rate Limit for RC1e

RC_WAKERATE_LIMIT0 - RC Wake Rate Limit for RC1e						
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x00000000 Size (in bits): 32						
Address: 0A098h						
DWord	Bit	Description				
0	31:16	RC1/E Wakre Rate Limit <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td colspan="2">RC Promotion Time Modulated by wake rate limits when using EI method: Even though the RC1 promotion time is met, if the wake limit is exceeded, no promotion.</td></tr> </table>	Access:	R/W	RC Promotion Time Modulated by wake rate limits when using EI method: Even though the RC1 promotion time is met, if the wake limit is exceeded, no promotion.	
	Access:	R/W				
RC Promotion Time Modulated by wake rate limits when using EI method: Even though the RC1 promotion time is met, if the wake limit is exceeded, no promotion.						
15:0	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO			
Access:	RO					

RC Wake Rate Limit for RC6pp

RC_WAKERATE_LIMIT2 - RC Wake Rate Limit for RC6pp		
DWord	Bit	Description
0	31:16	Reserved Access: RO
	15:0	RC6pp (Deepest RC6) Wake Rate Limit Access: R/W Bits 15_0 Reserved field for Broadwell. Pre-Broadwell Description as below. RC Promotion Time Modulated by wake rate limits when using EI method: Even though the Deepest RC6 promotion time is met, if the wake limit is exceeded, no promotion. Bits 15_0 Reserved field for Broadwell.

RC Wake Rate Limit for RC6/RC6p

RC_WAKERATE_LIMIT1 - RC Wake Rate Limit for RC6/RC6p						
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x00000000 Size (in bits): 32						
Address: 0A09Ch						
DWord	Bit	Description				
0	31:16	RC6 Wake Rate Limit <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td colspan="2">RC Promotion Time Modulated by wake rate limits when using EI method: Even though the RC6 promotion time is met, if the wake limit is exceeded, no promotion.</td></tr> </table>	Access:	R/W	RC Promotion Time Modulated by wake rate limits when using EI method: Even though the RC6 promotion time is met, if the wake limit is exceeded, no promotion.	
Access:	R/W					
RC Promotion Time Modulated by wake rate limits when using EI method: Even though the RC6 promotion time is met, if the wake limit is exceeded, no promotion.						
	15:0	RC6p (Deeper RC6) Wake Rate Limit <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td colspan="2">Bits 15_0 Reserved field for Broadwell. Pre-Broadwell Description as below RC Promotion Time Modulated by wake rate limits when using EI method: Even though the Deep RC6 promotion time is met, if the wake limit is exceeded, no promotion. Bits 15_0 Reserved field for Broadwell.</td></tr> </table>	Access:	R/W	Bits 15_0 Reserved field for Broadwell. Pre-Broadwell Description as below RC Promotion Time Modulated by wake rate limits when using EI method: Even though the Deep RC6 promotion time is met, if the wake limit is exceeded, no promotion. Bits 15_0 Reserved field for Broadwell.	
Access:	R/W					
Bits 15_0 Reserved field for Broadwell. Pre-Broadwell Description as below RC Promotion Time Modulated by wake rate limits when using EI method: Even though the Deep RC6 promotion time is met, if the wake limit is exceeded, no promotion. Bits 15_0 Reserved field for Broadwell.						

RCZ Virtual Page Address Registers

RCZTLB_VA - RCZ Virtual Page Address Registers				
Register Space:	MMIO: 0/2/0			
Project:	BDW			
Source:	RenderCS			
Default Value:	0x00000000			
Access:	RO			
Size (in bits):	32			
Trusted Type:	1			
Address:	04B00h-04B03h			
These registers are directly mapped to the current Virtual Addresses in the RCZTLB (Render Cache for Z (Depth), Hi Z, and Stencil TLB).				
DWord	Bit	Description		
0	31:12	<p>Address</p> <table border="1"> <tr> <td>Format:</td><td>GraphicsAddress[31:12]</td></tr> </table> <p>Page virtual address.</p>	Format:	GraphicsAddress[31:12]
Format:	GraphicsAddress[31:12]			
11:0	<p>Reserved</p> <table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ	
Format:	MBZ			

Ready Bit Vector 0 for TLBPEND registers

TLBPEND_RDY0 - Ready Bit Vector 0 for TLBPEND registers		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	04708h-0470Bh	
This register contains the ready bits for entries 0-31 of TLBPEND structure (Cycles pending TLB translation).		
DWord	Bit	Description
0	31:0	Ready bits per entry

Ready Bit Vector 1 for TLBPEND registers

TLBPEND_RDY1 - Ready Bit Vector 1 for TLBPEND registers		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	0470Ch-0470Fh	
This register contains the ready bits for entries 32-63 of TLBPEND structure (Cycles pending TLB translation).		
DWord	Bit	Description
0	31:0	Ready bits per entry

Render C State Control 1

RC_CTRL0 - Render C State Control 1						
DWord	Bit	Description				
0	31	<p>HW RC Control Enable</p> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>This bit does not control RC related counters, only the control of RC state based on HW FSM. 0: HW Control FSM disable. 1: HW Control FSM enabled. RC1EN, RC6EN, DEEPRC6EN, and DEEPESTRC6EN bits in this same register need to be programmed along with this bit as follows: Enable modes first, then set HWRCCE to 1. Disable modes first, then set HWRCCE to 0.</p>	Project:	BDW	Access:	R/W
Project:	BDW					
Access:	R/W					
	30:29	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td><td>RO</td></tr> </table>	Access:	RO		
Access:	RO					
	28	<p>TO - HW RC Promotion (i.e., Depth) Selection</p> <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>0: Timeout method disabled. 1: TO method enabled. pmcr_to_enable.</p>	Access:	R/W		
Access:	R/W					
	27	<p>EI - HW RC Promotion (i.e., Depth) Selection</p> <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>0: EI disabled. 1: Evaluation Interval (EI) method enabled. pmcr_ei_enable</p>	Access:	R/W		
Access:	R/W					
	26:21	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td><td>RO</td></tr> </table>	Access:	RO		
Access:	RO					
	20	<p>RC1/e Enable</p> <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Since RC1 action is to turn off the clock trunks and this is already part of the CP registers, only need to control whether RC1e happens or not. 0: HW RC1e disabled. 1: HW RC1e enabled.</p>	Access:	R/W		
Access:	R/W					

RC_CTRL0 - Render C State Control 1

	19	Reserved	Access:	RO
		Reserved.		
	18	RC6 Enable	Access:	R/W
		0: HW RC6 not enabled. 1: HW RC6 enabled.		
	17	Deep RC6 Enable	Access:	R/W
		Bit 17 not supported in Broadwell. 0: Reserved bit for Broadwell, Pre-Broadwell: HW Deep RC6 not enabled. 1: Reserved bit for Broadwell, Pre-Broadwell: HW Deep RC6 enabled. Bit 17 not supported in Broadwell.		
	16	Deepest RC6 Enable	Access:	R/W
		Bit 18 not supported in Broadwell. 0: Reserved bit for Broadwell, Pre-Broadwell: HW Deepest RC6 not enabled. 1: Reserved bit for Broadwell, Pre-Broadwell: HW Deepest RC6 enabled. Bit 18 not supported in Broadwell.		
	15	Reserved	Access:	RO
	14	Enable Pipe State Reporting to PCU	Access:	R/W
		Enable Pipe State Reporting to PCU (PIPEREPEN): 0: Pipe state not communicated to PCU. 1: Pipe state is sent to PCU when it changes.		
	13:0	Reserved	Access:	RO

Render C State Control 2

RC_CTRL1 - Render C State Control 2				
DWord	Bit	Description		
0	31:19	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
Access:	RO			
18:16	Target SW/FSM/PCU Controlled RC state <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>000b: RC0 (this does not control clock gating). 001b: Reserved. 010b: RC1e (this does not control clock gating). 011b: Reserved. 100b: RC6. 101b: Reserved. 110b: Reserved. 111b: Reserved. pmcr_sw_rc_cmd[2:0].</p>	Access:	R/W	
Access:	R/W			
15:0	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO	
Access:	RO			

Render Geyserville Mode Control Register

RP_CTRL - Render Geyserville Mode Control Register

Register Space: MMIO: 0/2/0

Project: BDW

Default Value: 0x00000000

Size (in bits): 32

Address: 0A024h

DWord	Bit	Description
0	31:12	Reserved Access: RO
	11	RP Video Turbo Enable for Media Engine Access: R/W RPVTENMEDIA : RP Video Turbo Enable for Media Engine. This bit controls whether the Media Engine busy status is considered when requesting Video Turbo mode. 0 = Video Turbo mode is not affected by Media's Done status. 1 = Video Turbo mode is enabled when Media is busy (Done=0).
	10:9	RP Software Mode Control Access: R/W RP Software Mode Control (RPSWCTL): 00b = GT does not write to the IO_THREAD_P_REQ register. 01b = GT writes RPNSWREQ or RPVSWREQ to IO_THREAD_P_REQ on a change, depending on current video turbo mode. 10b = GT writes RPNSWREQ to IO_THREAD_P_REQ when it changes. 11b = GT writes RPVSWREQ to IO_THREAD_P_REQ when it changes. Clarification FOR: 10b => Always write the normal req, regardless of the vcs-video turbo enable bit. 11b => Always write the turbo req, regardless of the vcs-video turbo enable bit.
	8	Mask Bits for Graphics Busyness Access: R/W Mask Bits for Graphics Busyness (MBGB): 0: MFX busyness is not counted as part of gfx busyness. 1: MFX busyness is counted as part of gfx busyness. pmcr_media_mask.
	7	RP Hardware Mode Enable Access: R/W 0 - RP counters are kept at 0 (default). 1 - RP counters are enabled (program enable after counter values have been programmed).

RP_CTRL - Render Geyserville Mode Control Register

	6	Reserved
		Access: RO Reserved.
	5:3	Frequency Increase Utilization Metric Selection Access: R/W Frequency Increase Utilization Metric selection. The selection of a metric below indicates which one is used in making decision. All the metrics should be running and updating the status counters regardless of this setting. More than Busy Max Continuous (BMXC) time must be reached for a frequency increase. More than Busy Max Average (BMXA) at end of Evaluation Interval must be reached for a frequency increase. Less than Idle Min Continuous (IMNC) time must be reached for a frequency Increase (removed for DevBDW). BMXC BMXA IMNC 0 0 0: No metric enabled. 0 0 1: No metric enabled (IMNC removed for DevBDW). 0 1 0: BMXA metric enabled. 0 1 1: Reserved. 1 0 0: BMXC metric enabled 1 0 1: Reserved. 1 1 0: Reserved. 1 1 1: Reserved.
	2:0	Frequency Decrease Utilization Metric Selection Access: R/W The selection of a metric below indicates which one is used in making decision. All the metrics should be running and updating the status counters regardless of this setting. Less than Busy Min Continuous (BMNC) must be reached for a frequency decrease (removed for DevBDW). Less than Busy Min Average (BMNA) at end of Evaluation Interval must be reached for a frequency decrease More than Idle Max Continuous (IMXC) must be reached for a frequency decrease (removed for DevBDW). BMNC BMNA IMXC 0 0 0: No metric enabled. 0 0 1: No metric enabled (IMXC removed for DevBDW). 0 1 0: BMNA metric enabled. 0 1 1: Reserved. 1 0 0: No metric enabled (BMNC removed for DevBDW). 1 0 1: Reserved. 1 1 0: Reserved. 1 1 1: Reserved.

Render Mode Register for Software Interface

MI_MODE - Render Mode Register for Software Interface

Register Space: MMIO: 0/2/0

Project: BDW

Source: RenderCS

Default Value: 0x00000000

Access: R/W

Size (in bits): 32

Address: 0209Ch

The MI_MODE register contains information that controls software interface aspects of the Memory Interface function.

DWord	Bit	Description										
0	31:16	Masks										
		Format:	Mask[15:0]									
A 1 in a bit in this field allows the modification of the corresponding bit in Bits 15:0												
	15	Suspend Flush										
		Format:	U1									
<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>No Delay [Default]</td> <td>HW will not delay flush, this bit will get cleared by MI_SUSPEND_FLUSH as well</td> </tr> <tr> <td>1h</td> <td>Delay Flush</td> <td>Suspend flush is active</td> </tr> </tbody> </table>				Value	Name	Description	0h	No Delay [Default]	HW will not delay flush, this bit will get cleared by MI_SUSPEND_FLUSH as well	1h	Delay Flush	Suspend flush is active
Value	Name	Description										
0h	No Delay [Default]	HW will not delay flush, this bit will get cleared by MI_SUSPEND_FLUSH as well										
1h	Delay Flush	Suspend flush is active										
Programming Notes												
This should only be written to from the ring using MI_SUSPEND_FLUSH. It is considered undefined if written by software through MMIO												
14	14	Async Flip Performance mode										
		Project:	BDW									
		Format:	U1									
<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Performance mode enabled [Default]</td> <td>The stall of the flip event is in the windower</td> </tr> <tr> <td>1h</td> <td>Performance mode disabled</td> <td>The stall of the flip event is in the command stream</td> </tr> </tbody> </table>				Value	Name	Description	0h	Performance mode enabled [Default]	The stall of the flip event is in the windower	1h	Performance mode disabled	The stall of the flip event is in the command stream
Value	Name	Description										
0h	Performance mode enabled [Default]	The stall of the flip event is in the windower										
1h	Performance mode disabled	The stall of the flip event is in the command stream										
Programming Notes												
This bit must be set to '1' on all projects disabling Async Flip Performance mode.												

MI_MODE - Render Mode Register for Software Interface

		When Async Flip Performance mode is enabled stall is in the Windower allowing the commands following the MI_WAIT_FOR_EVENT to be parsed by command streamer, this breaks the usage model of controlling the display message generation in display engine using MI_LOAD_REGISTER_IMMEDIATE commands from ring buffer.													
13	Flush Performance mode	<table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Format:</td> <td>U1</td> </tr> </table> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>run fast restore [Default]</td> <td>No NonPipelined SV flush.</td> </tr> <tr> <td>1h</td> <td>run slow legacy restore</td> <td>With NonPipelined SV flush.</td> </tr> </tbody> </table>	Project:	BDW	Format:	U1	Value	Name	Description	0h	run fast restore [Default]	No NonPipelined SV flush.	1h	run slow legacy restore	With NonPipelined SV flush.
Project:	BDW														
Format:	U1														
Value	Name	Description													
0h	run fast restore [Default]	No NonPipelined SV flush.													
1h	run slow legacy restore	With NonPipelined SV flush.													
12	Reserved	<table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	BDW	Format:	MBZ									
Project:	BDW														
Format:	MBZ														
11	Invalidate UHPTTR enable	<table border="1"> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>If bit set H/W clears the valid bit of UHPTTR (2134h, bit 0) when current active head pointer is equal to UHPTTR.</p>	Format:	Enable											
Format:	Enable														
10	Atomic Read Return for MI_COPY_MEM_MEM	<table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Format:</td> <td>U1</td> </tr> </table> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Disable [Default]</td> <td>Hardware does a regular memory fence write to complete the write to the destination address before moving to the next instruction.</td> </tr> <tr> <td>1h</td> <td>Enable</td> <td>Hardware does Atomic Move with Read Return to complete the write to the destination address before moving to the next instruction.</td> </tr> </tbody> </table>	Project:	BDW	Format:	U1	Value	Name	Description	0h	Disable [Default]	Hardware does a regular memory fence write to complete the write to the destination address before moving to the next instruction.	1h	Enable	Hardware does Atomic Move with Read Return to complete the write to the destination address before moving to the next instruction.
Project:	BDW														
Format:	U1														
Value	Name	Description													
0h	Disable [Default]	Hardware does a regular memory fence write to complete the write to the destination address before moving to the next instruction.													
1h	Enable	Hardware does Atomic Move with Read Return to complete the write to the destination address before moving to the next instruction.													
9	Rings Idle	<table border="1"> <tr> <td>Format:</td> <td>U1</td> </tr> </table> <p>Read Only Status bit</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Not Idle [Default]</td> <td>Parser not Idle or Ring Arbiter not Idle.</td> </tr> <tr> <td>1h</td> <td>Idle</td> <td>Parser Idle and Ring Arbiter Idle.</td> </tr> </tbody> </table> <table border="1"> <tr> <td align="center">Programming Notes</td> </tr> </table> <p>Writes to this bit are not allowed.</p>	Format:	U1	Value	Name	Description	0h	Not Idle [Default]	Parser not Idle or Ring Arbiter not Idle.	1h	Idle	Parser Idle and Ring Arbiter Idle.	Programming Notes	
Format:	U1														
Value	Name	Description													
0h	Not Idle [Default]	Parser not Idle or Ring Arbiter not Idle.													
1h	Idle	Parser Idle and Ring Arbiter Idle.													
Programming Notes															

MI_MODE - Render Mode Register for Software Interface

	8	Stop Rings		
		Format:	U1	
			Description	
		0h	[Default] Normal Operation.	
		1h	Parser is turned off and Ring arbitration is turned off.	
			Programming Notes	
			Software must set this bit to force the Rings and Command Parser to Idle. Software must read a 1 in the Ring Idle bit after setting this bit to ensure that the hardware is idle.	
			Software must clear this bit for Rings to resume normal operation.	
			Due to known HW issue when Stop Rings occur during execution of a batch buffer, memory access type of the batch buffer is reset and hence on resuming the memory access type can be inconsistent with the desired memory access type. SW must not set/reset Stop Rings to achieve stall and resume function in command streamer execution, however Stop Rings can be used by SW before resetting the engine.	
	7	Reserved		
		Project:	BDW	
		Format:	MBZ	
	6	Vertex Shader Timer Dispatch Enable		
		Project:	BDW	
		Format:	Enable	
			Description	
		0h	[Default] Disable Disable the timer for dispatch of single vertices from the vertex shader. Vertex shader will try to collect 2 vertices before a dispatch	
		1h	Enable Enable the timer for dispatch of single vertices. Dispatch a single vertex shader thread after the timer expires.	
	5	Reserved		
		Format:	MBZ	

MI_MODE - Render Mode Register for Software Interface

4:1	Predicate Enable	
	Project:	BDW
	This field gets set when "MI_SET_PREDICATE" command is parsed by render command streamer. Predicate Disable is the default mode of operation.	
	Value	Name
	0h	Predicate Disable
	1h	Predicate on Result2 clear
	2h	Predicate on Result2 set
	3h	Predicate on Result clear
	4h	Predicate on Result set
	5h	Predicate when two or more slices enabled
0	Programming Notes	
	SW must use MI_SET_PREDICATE instead of MMIO access.	
	Mask IIR disable	
	Format:	Disable
	Mask IIR disable. Nominally the Interrupt controller masks interrupts in the IIR register if an interrupt acknowledge from the 3gio interface is pending. Setting this bit to a 1 allows interrupts to be visible to the interrupt controller while an interrupt acknowledge is pending.	

Render Performance Status Register

RP_STATUS0 - Render Performance Status Register

Register Space: MMIO: 0/2/0

Project: BDW

Default Value: 0x00000000

Size (in bits): 32

Address: 0A01Ch

This register reflects real-time values and thus does not have a pre-determined default value out of reset.

DWord	Bit	Description
0	31:20	Reserved
		Access: RO
	19:18	Current Actual Gear Ratio
		Access: RO
	17:16	Previous Actual Gear Ratio
		Access: RO Previous Actual Gear Ratio (PAGR).
	15	Last Requested Video Turbo Mode
		Access: RO Last Requested Video Turbo Mode (CRTM): 0 = Most recent request was a normal request (from RPNSWREQ). 1 = Most recent request was a Video Turbo request (from RPVSWREQ).
	14	Reserved
		Access: RO
13:7	Current Actual GFX Freq	
		Access: RO This is the MLC ratio that the core is actually running.
6:0	Previous Actual GFX Freq	
		Access: RO This is the MLC ratio that the core was actually running before the current actual GFX frequency.

Render Power Clock State Register

R_PWR_CLK_STATE - Render Power Clock State Register			
Register Space:	MMIO: 0/2/0		
Project:	BDW		
Source:	RenderCS		
Default Value:	0x00000000 [BDW]		
Access:	R/W		
Size (in bits):	32		
Address:	020C8h		
<p>This register contains the mode selection for configuring render engine to attain desired performance and power requirements for a given context. This register is render context save/restored. This register must be initialized correctly when the context is submitted for the first time. This register is context save/restored as part of Exec-List context image in both Exec-List and Ring-Buffer mode of scheduling. This register contents are valid only when "Enable" bit [31] of the register is set.</p>			
Programming Notes			
<p>This register must not be programmed directly through CPU MMIO cycle. Exec-List Scheduling Mode: Every context can have its own required render engine configuration by programming this register appropriately in the logical render context image in memory (LRCA) before submitting the context to the execlist submit port. This register must not be programmed using MI_LOAD_REGISTER_IMM command in ring buffer or in batch buffer, however programming "NON-SLM Indication" field through MI_LOAD_REGISTER_IMM is an exception defined below. If a need arises to change the render configuration for a context being executed in HW, Scheduler must preempt the context and update the desired render configuration in the logical render context image in memory and resubmit the context. Only "NON-SLM Indictaion" field in R_PWR_CLK_STATE register is allowed to be modified through MI_LOAD_REGISTER_IMM command in ring_buffer or privileged_batch_buffer. SW must modify only "NON-SLM Indication" field and must ensure to program other fields with the same value as in LRCA. SW must ensure to program PIPECONTROL flush command with CS Stall and HDC Flush prior to programming MI_LOAD_REGISTER_IMM command to modify "NON-SLM Indication" in R_PWR_CLK_STATE register. Example: //R_PWR_CLK_STATE register value in LRCA configured with two slices and NON-SLM indication reset: 0x80005_0000 //SW desires to set NON-SLM Indication filed in ring buffer</p> <p>MI_LOAD_REGISTER_IMM 0x20C8, 0x8005_0100 Ring Buffer Scheduling: This register must be programmed using MI_LOAD_REGISTER_IMM command in the ring buffer. When this register is being programmed to re-configure the number of slices, SW must context save the state before programming this register and restore the state after programming the register via dummy MI_SET_CONTEXT command, this will ensure the existing state is programmed to all the new slices that are powered up, in case of slice shutdown this is not required. EX: MI_SET_CONTEXT → CXTA MI_BATCH_BUFFER_START MI_BATCH_BUFFER_START MI_SET_CONTEXT → CXTB //Dummy Context to save existing render state to be restored latter. MI_LOAD_REGISTER_IMM : R_PWR_CLK_STATE (1 Slice to 3 Slices) // Slice configuration done. MI_SET_CONTEXT → CXTA // Context restore of valid state to all the slices powered up.</p>			
DWord	Bit	Description	
0	31	Power Clock State Enable	
		Project:	BDW
		Format:	U1

R_PWR_CLK_STATE - Render Power Clock State Register

		Value	Name	Description	
		0h	Power Clock State Disabled	No specific power state set, bits[30:0] are ignored.	
		1h	Power Clock State Enabled	Power Clock is set and bit[30:0] are valid and have the desired state.	
	30:0	Render Power Clock State			
		Project:	BDW		
		Format:	Power Clock State Format		

Render TLB Control Register

RTCR - Render TLB Control Register						
DWord	Bit	Description				
0	31:1	Reserved <table border="1"> <tr> <td>Default Value:</td><td>00000000000000000000000000000000b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	00000000000000000000000000000000b	Access:	RO
Default Value:	00000000000000000000000000000000b					
Access:	RO					
	0	Invalidate TLBs on the corresponding Engine <table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>SW writes 1 to invalidate the TLBs for the associated engine and HW clears the bit when invalidation is complete. To ensure proper invalidation of the TLBs, SW has to ensure the corresponding engine's HW pipeline is flushed and cleared from all its memory accesses. Otherwise HW cannot guarantee the proper invalidation for TLBs. This bit is self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					

Render Watchdog Counter

PR_CTR - Render Watchdog Counter			
Register Space:		MMIO: 0/2/0	
Project:		BDW	
Source:		RenderCS	
Default Value:		0x00000000	
Access:		RO	
Size (in bits):		32	
Address:		02190h	
DWord	Bit	Description	
0	31:0	Counter Value Format:	U32
		This register reflects the render watchdog counter value itself. It cannot be written to.	

Render Watchdog Counter Threshold

PR_CTR_THRSH - Render Watchdog Counter Threshold						
DWord	Bit	Description				
0	31:0	<p>Counter logic Threshold</p> <table border="1"> <tr> <td>Default Value:</td><td>00150000h</td></tr> <tr> <td>Format:</td><td>U32</td></tr> </table> <p>This field specifies the threshold that the hardware checks against for the value of the render clock counter before generating an interrupt. The counter in hardware generates an interrupt when the threshold is reached, rolls over and starts counting again. The interrupt generated is the "Media Hang Notify" interrupt since this watchdog timer is intended primarily to remedy VLD hangs on the main pipeline.</p>	Default Value:	00150000h	Format:	U32
Default Value:	00150000h					
Format:	U32					

Reported Bitstream Output Bit Count for Syntax Elements Only Register

MFC_BITSTREAM_SE_BITCOUNT_FRAME - Reported Bitstream Output Bit Count for Syntax Elements Only Register		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Source:	VideoCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	128A4h	
Valid Projects:	[BDW]	
Address:	1C8A4h	
Valid Projects:	[BDW:GT3]	
This register stores the count of number of bits in the bitstream due to syntax elements only. This excludes header/ byte alignment /tail/EMU/CABAC-0word/padding bits but includes the stop-one-bit. This register is part of the context save and restore.		
DWord	Bit	Description
0	31:0	<p>MFC Bitstream Syntax Element Only Bit Count</p> <p>Total number of bits in the bitstream output due to syntax elements only. It includes the data bytes only. This count is updated for every time the internal bitstream counter is incremented and its reset at image start.</p>

Reported Bitstream Output Byte Count per Frame Register

MFC_BITSTREAM_BYTECOUNT_FRAME - Reported Bitstream Output Byte Count per Frame Register		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Source:	VideoCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	128A0h	
Valid Projects:	[BDW]	
Address:	1C8A0h	
Valid Projects:	[BDW:GT3]	
This register stores the count of bytes of the bitstream output per frame		
DWord	Bit	Description
0	31:0	MFC Bitstream Byte Count per Frame Total number of bytes in the bitstream output per frame from the encoder. This includes header/tail/byte alignment/data bytes/EMU (emulation) bytes/cabac-zero word insertion/padding insertion. This count is updated for every time the internal bitstream counter is incremented and its reset at image start.

Reported Bitstream Output CABAC Bin Count Register

MFC_AVC_CABAC_BIN_COUNT_FRAME - Reported Bitstream Output CABAC Bin CountRegister		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Source:	VideoCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	128A8h	
Valid Projects:	[BDW]	
Address:	1C8A8h	
Valid Projects:	[BDW:GT3]	
This register stores the count of number of bins per frame.		
DWord	Bit	Description
0	31:0	MFC AVC Cabac Bin Count Total number of BINs in the bitstream output per frame from the encoder. This count is updated for every time the bin counter is incremented and its reset at image start.

Reported Timestamp Count

TIMESTAMP - Reported Timestamp Count						
Register Space: MMIO: 0/2/0 Project: BDW Source: RenderCS Default Value: 0x00000000h, 00000000 [BDW] Access: RO. This register is not set by the context restore. Size (in bits): 64 Address: 02358h						
DWord	Bit	Description				
0	63:36	Reserved <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	BDW	Format:	MBZ
Project:	BDW					
Format:	MBZ					
0	35:0	Timestamp Value <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>U36</td></tr> </table>	Project:	BDW	Format:	U36
Project:	BDW					
Format:	U36					
Description		Project				
This register toggles based on time stamp granularity (base unit).		BDW				

Reset Flow Control Messages

RSTFCTLMSG - Reset Flow Control Messages				
Register Space: MMIO: 0/2/0				
Project: BDW				
Default Value: 0x00000000				
Size (in bits): 32				
Address: 08108h				
Soft-Reset and FLR Flow Control Message Registers				
DWord	Bit	Description		
0	31:16	<p>Message Mask</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Message Mask In order to write to bits 15:0, the corresponding message mask bits must be written. For example, for bit 14 to be set, bit 30 needs to be 1 : 40004000</p>	Access:	RO
Access:	RO			
15:12	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Reserved</p>	Access:	RO	
Access:	RO			
11	<p>MEDIA 1 Reset flow acknowledgement message</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>PM Acknowledgement Messages for Media 1 reset: '1' : PREP_RST_MEDIA1_ACK - Acknowledgement that graphics media1 (or 2nd vbox) is prepared for reset assertion. '0' : DONE_MEDIA1_RST_ACK - Acknowledgement that graphics media1 (or 2nd vbox) reset is de-asserted</p>	Access:	R/W	
Access:	R/W			
10	<p>WIDI Reset flow acknowledgement message</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>PM Acknowledgement Messages for WIDI reset: '1' : PREP_RST_WIDI_ACK - Acknowledgement that graphics widi is prepared for reset assertion. '0' : DONE_WIDI_RST_ACK - Acknowledgement that graphics widi reset is de-asserted</p>	Access:	R/W	
Access:	R/W			
9	Reserved			

RSTFCTLMSG - Reset Flow Control Messages				
	8	Vebox Reset flow Acknowledge Message <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>PM Acknowledgement Messages for Vebox reset: '1' : PREP_RST_VEBOX_ACK - Acknowledgement that graphics VE is prepared for reset assertion. '0' : DONE_VEBOX_RST_ACK - Acknowledgement that graphics VE reset is de-asserted</p>	Access:	R/W
Access:	R/W			
	7	Blitter Reset Flow Acknowledgement Messages <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>PM Acknowledgement Messages for Blitter reset: '1' : PREP_RST_BLIT_ACK - Acknowledgement that graphics blitter is prepared for reset assertion. '0' : DONE_BLIT_RST_ACK - Acknowledgement that graphics blitter reset is de-asserted</p>	Access:	R/W
Access:	R/W			
	6	Media Reset Flow Acknowledgement Messages <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>PM Acknowledgement Messages for Media reset: '1' : PREP_RST_MEDIA_ACK - Acknowledgement that graphics media block is prepared for reset assertion. '0' : DONE_MEDIA_RST_ACK - Acknowledgement that the graphics media reset is de-asserted</p>	Access:	R/W
Access:	R/W			
	5	Render Reset Flow Acknowledgement Messages <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>PM Acknowledgement Messages for Render reset: '1' : PREP_RST_RENDER_ACK - Acknowledgement that the graphics render block is prepared for reset assertion. '0' : DONE_RENDER_RST_ACK - Acknowledgement that the graphics render reset is de-asserted</p>	Access:	R/W
Access:	R/W			
	4	GTI-Device Reset Flow Acknowledgement Messages <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>PM Acknowledgement Messages for GTI-Device reset: '1' : PREP_RST_GTIDEV_ACK - Acknowledgement that the GTI device is prepared for reset assertion. '0' : DONE_GTIDEV_RST_ACK - Acknowledgement that the GTI device reset is de-asserted</p>	Access:	R/W
Access:	R/W			
	3	Reserved <table border="1"> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Reserved</p>	Access:	RO
Access:	RO			

RSTFCTLMSG - Reset Flow Control Messages				
	2	<p>FLR Done ack from Pmunit</p> <table border="1"> <tr> <td>Access:</td><td>R/W Set</td></tr> </table> <p>FLR Done ack from Pmunit: 1: PM unit sets this bit to acknowledge the FLR done message has been forwarded to SA through GAM interface. 0: Default Value. If the bit was set by PM then Cpunit hardware clears it once FLR is completed.</p>	Access:	R/W Set
Access:	R/W Set			
	1	<p>Global Resource Arbitration Acknowledgement Messages</p> <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Global Resource Arbitration Acknowledgement Message from PM: '1' : CP_ARB_REQ_ACK - Acknowledgement for CPUnit's global resource arbitration request '0' : CP_ARB_RELEASE_ACK - Acknowledgement to CPUnit's release of global resources</p>	Access:	R/W
Access:	R/W			
	0	<p>CP Busy / Idle Status Acknowledgement Messages</p> <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>CP Busy / Idle Status Acknowledgement Message from PM: '0' : CP_NOT_BUSY_ACK - Acknowledgement that the CPunit is idle. '1' : CP_BUSY_ACK - Acknowledgement that the CPunit is busy.</p>	Access:	R/W
Access:	R/W			

RESET Messaging Register for Clocking Unit

MSG_RESET_GCP - RESET Messaging Register for Clocking Unit

Register Space: MMIO: 0/2/0

Project: BDW

Default Value: 0x00000000

Size (in bits): 16

Address: 08030h

Message registers have bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16].

To set bit0, for example, the data would be 0x0001_0001.

To clear bit0, for example, the data would be 0x0001_0000.

Note that mask bit is the data bit offset + 16.

Message registers are protected from non-GT writes via the Message Channel.

Request to Prepare for Reset.

1'b0: Reset complete (default).

1'b1: Prepare for reset.

DWord	Bit	Description
0	15:8	Reserved Access: RO
	7	Request to Prepare for FLR Access: R/W [7] Prepare for devrst_b Domain Reset (FLR) Note: All resets except busrst_b are asserted for an FLR.
	6	Request to Prepare for Media1 Reset Access: R/W [6] Prepare for cmrst_b Domain Reset (vcs1unit).
	5	Request to Prepare for Wi-Di Reset Access: R/W [5] Prepare for cwrst_b Domain Reset (winunit).
	4	Reserved
	3	Request to Prepare for Blitter Reset Access: R/W [3] Prepare for crblitrst_b Domain Reset (bcsunit).
	2	Request to Prepare for VEBox Reset Access: R/W [2] Prepare for cvrst_b Domain Reset (vecsunit).

MSG_RESET_GCP - RESET Messaging Register for Clocking Unit

	1	Request to Prepare for Media0 Reset		
		<table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>[1] Prepare for cmrst_b Domain Reset (vcs0unit).</p>	Access:	R/W
Access:	R/W			
	0	Request to Prepare for Render Reset		
		<table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>[0] Prepare for crrst_b Domain Reset (csunit).</p>	Access:	R/W
Access:	R/W			

Resource Streamer Context Offset

RS_CXT_OFFSET - Resource Streamer Context Offset												
DWord	Bit	Description										
0	31:6	<p>RS Offset</p> <table border="1"> <tr> <td>Format:</td> <td>U26</td> </tr> <tr> <td colspan="2">This field indicates the offset (64bytes granular) in to the logical rendering context to which Resource Streamer context is save/restored when enabled. This field register must not be written directly (via MMIO) unless the Command Streamer is completely idle (i.e., the Ring Buffer is empty and the pipeline is idle) and RC6 is disabled. On way to program this register is via Load Register Immediate command in the ring buffer as part of initialization sequence.</td></tr> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> <tr> <td>ECh</td><td>[Default]</td><td>DefaultValueDesc</td></tr> </table>	Format:	U26	This field indicates the offset (64bytes granular) in to the logical rendering context to which Resource Streamer context is save/restored when enabled. This field register must not be written directly (via MMIO) unless the Command Streamer is completely idle (i.e., the Ring Buffer is empty and the pipeline is idle) and RC6 is disabled. On way to program this register is via Load Register Immediate command in the ring buffer as part of initialization sequence.		Value	Name	Description	ECh	[Default]	DefaultValueDesc
Format:	U26											
This field indicates the offset (64bytes granular) in to the logical rendering context to which Resource Streamer context is save/restored when enabled. This field register must not be written directly (via MMIO) unless the Command Streamer is completely idle (i.e., the Ring Buffer is empty and the pipeline is idle) and RC6 is disabled. On way to program this register is via Load Register Immediate command in the ring buffer as part of initialization sequence.												
Value	Name	Description										
ECh	[Default]	DefaultValueDesc										
	5:0	<p>Reserved</p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ								
Format:	MBZ											

Resource Streamer Preemption Status

RS_PREEMPT_STATUS - Resource Streamer Preemption Status

Register Space: MMIO: 0/2/0

Project: BDW

Source: RenderCS

Default Value: 0x00000000

Access: R/W

Size (in bits): 32

Address: 0215Ch

Preemption from First Level Batch Buffer: This register contains the offset in to the Batch Buffer on which Resource streamer got preempted. Note that it is offset from the Batch Start Address and not the graphics address corresponding to the preempted instruction on Batch Buffer. This register's contents will be looked at by Command Streamer on the next RS Start Trigger to provide the appropriate batch start address. Following preemption, context save happens on which this register is context saved, after context save the register gets auto reset by Command Streamer. This register gets context save/restored by Render Command Streamer as part of its render context. **Preemption from Second Level Batch Buffer:** This register contains the graphics address of the instruction in Second Level Batch Buffer on which Resource streamer got preempted. This register's contents will be looked at by Command Streamer on the next RS Start Trigger to provide the appropriate batch start address. Following preemption, context save happens on which this register is context saved, after context save the register gets auto reset by Command Streamer. This register gets context save/restored by Render Command Streamer as part of its render context.

Programming Notes

- This register is accessed by Render Command Streamer as part of render context save/restore; this register should be exercised by S/W only for resetting the register contents if required.
- Following preemption if there is no context save, SW should program this register with 0x0 so that it does not interfere with proceeding workloads.

DWord	Bit	Description		
0	31:2	<p>Batch Buffer Offset</p> <table border="1"> <tr> <td>Format:</td> <td>Offset[31:2]</td> </tr> </table> <p>This field specifies the DWord-aligned offset from the batch start address on which Resource Streamer got preempted.</p>	Format:	Offset[31:2]
Format:	Offset[31:2]			
1	<p>RS_PREEMPT_STATUS</p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table> <p>This field when not set indicates RS got preempted on a natural sync point else it got preempted on a draw call.</p>	Format:	MBZ	
Format:	MBZ			

RS_PREEMPT_STATUS - Resource Streamer Preemption Status

RS_PREEMPTED	
Default Value:	0
Format:	Enable
If this bit is set indicates Resource Streamer got preempted. Other fields of this register are valid only when this bit is set.	

Revision Identification

RID2_0_2_0_PCI - Revision Identification						
DWord	Bit	Description				
0	7:4	Revision Identification Number MSB <table border="1"> <tr> <td>Default Value:</td><td>0000b</td></tr> <tr> <td>Access:</td><td>R/W Firmware Only</td></tr> </table> Four MSB of RID	Default Value:	0000b	Access:	R/W Firmware Only
Default Value:	0000b					
Access:	R/W Firmware Only					
3:0	Revision Identification Number <table border="1"> <tr> <td>Default Value:</td><td>0000b</td></tr> <tr> <td>Access:</td><td>R/W Firmware Only</td></tr> </table> Four LSB of RID	Default Value:	0000b	Access:	R/W Firmware Only	
Default Value:	0000b					
Access:	R/W Firmware Only					

RING_BUFFER_HEAD_PREEMPT_REG

RING_BUFFER_HEAD_PREEMPT_REG - RING_BUFFER_HEAD_PREEMPT_REG	
Register Space:	MMIO: 0/2/0
Project:	BDW
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	0214Ch-0214Fh
Name:	RING_BUFFER_HEAD_PREEMPT_REG
ShortName:	RING_BUFFER_HEAD_PREEMPT_REG_RCSUNIT
Address:	1214Ch-1214Fh
Name:	RING_BUFFER_HEAD_PREEMPT_REG
ShortName:	RING_BUFFER_HEAD_PREEMPT_REG_VCSUNIT0
Address:	1A14Ch-1A14Fh
Name:	RING_BUFFER_HEAD_PREEMPT_REG
ShortName:	RING_BUFFER_HEAD_PREEMPT_REG_VECSUNIT
Address:	1C14Ch-1C14Fh
Name:	RING_BUFFER_HEAD_PREEMPT_REG
ShortName:	RING_BUFFER_HEAD_PREEMPT_REG_VCSUNIT1
Address:	2214Ch-2214Fh
Name:	RING_BUFFER_HEAD_PREEMPT_REG
ShortName:	RING_BUFFER_HEAD_PREEMPT_REG_BCSUNIT
Description	
This register contains the Head pointer offset in the ring when the last PREEMPTABLE command was executed and caused the head pointer to move due to the UHPTR register being valid. If the PREEMPTABLE command is executed as part of the batch buffer then the value of the register will be the offset in the ring of the command past the batch buffer start that contained the preemptable command.	
This is a global register and context save/restored as part of power context image.	
Preemptable Commands	
<ul style="list-style-type: none"> • MI_ARB_CHECK • 3D_PRIMITIVE • GPGPU_WALKER • MEDIA_STATE_FLUSH • PIPE_CONTROL (Only in GPGPU mode of pipeline selection) • MI_ATOMIC (Post Sync Operation set in GPGPU mode of pipeline selection) 	Source
	RenderCS

RING_BUFFER_HEAD_PREEMPT_REG - RING_BUFFER_HEAD_PREEMPT_REG

- MI_SEMAPHORE_SIGNAL (Post Sync Operation set in GPGPU mode of pipeline selection)

Programming Notes

Programming Restriction:

This register should NEVER be programmed by driver. This is for HW internal use only.

DWord	Bit	Description																
0	31:21	Last Wrap Count																
	20:2	Preempted Head Offset	Format: <input type="text"/> U19 This field contains the Head pointer offset in the ring when the last MI_ARB_CHECK command was executed and caused the head pointer to move due to the UHPT register being valid.															
	1:0	Ring/Batch Indicator	Format: <input type="text"/> Enabled <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Ring</td> <td>Preemptable command was executed in ring and caused head pointer to be updated.</td> <td></td> </tr> <tr> <td>1h</td> <td>Batch</td> <td>Preemptable command was executed in batch and caused head pointer to be updated.</td> <td></td> </tr> <tr> <td>2h</td> <td>2nd level batch</td> <td>Preemptable command was executed in second level batch and caused head pointer to be updated.</td> <td>BDW</td> </tr> </tbody> </table>	Value	Name	Description	Project	0h	Ring	Preemptable command was executed in ring and caused head pointer to be updated.		1h	Batch	Preemptable command was executed in batch and caused head pointer to be updated.		2h	2nd level batch	Preemptable command was executed in second level batch and caused head pointer to be updated.
Value	Name	Description	Project															
0h	Ring	Preemptable command was executed in ring and caused head pointer to be updated.																
1h	Batch	Preemptable command was executed in batch and caused head pointer to be updated.																
2h	2nd level batch	Preemptable command was executed in second level batch and caused head pointer to be updated.	BDW															

Ring Buffer Control

RING_BUFFER_CTL - Ring Buffer Control			
Register Space:	MMIO: 0/2/0		
Project:	BDW		
Default Value:	0x00000000		
Access:	R/W		
Size (in bits):	32		
Address:	0203Ch-0203Fh		
Name:	Ring Buffer Control		
ShortName:	RING_BUFFER_CTL_RCSUNIT		
Address:	1203Ch-1203Fh		
Name:	Ring Buffer Control		
ShortName:	RING_BUFFER_CTL_VCSUNIT0		
Address:	1A03Ch-1A03Fh		
Name:	Ring Buffer Control		
ShortName:	RING_BUFFER_CTL_VECSUNIT		
Address:	1C03Ch-1C03Fh		
Name:	Ring Buffer Control		
ShortName:	RING_BUFFER_CTL_VCSUNIT1		
Address:	2203Ch-2203Fh		
Name:	Ring Buffer Control		
ShortName:	RING_BUFFER_CTL_BCSUNIT		
Description		Source	
These registers are used to define and operate the ring buffer mechanism which can be used to pass instructions to the command interface. The buffer itself is located in a physical memory region. The ring buffer is defined by a 4 Dword register set that includes starting address, length, head offset, tail offset, and control information. Refer to the Programming Interface chapter for a detailed description of the parameters specified in this ring buffer register set, restrictions on the placement of ring buffer memory, arbitration rules, and in how the ring buffer can be used to pass instructions.		RenderCS	
Ring Buffer Head and Tail Offsets must be properly programmed before it is enabled. A Ring Buffer can be enabled when empty.		BlitterCS, VideoCS, VideoEnhancementCS	
DWord	Bit	Description	
0	31:21	Reserved	
		Format:	MBZ

RING_BUFFER_CTL - Ring Buffer Control

	20:12	Buffer Length				
		Format:	U9-1 in 4 KB pages - 1			
This field is written by SW to specify the length of the ring buffer in 4 KB Pages. Range = [0 = 1 page = 4 KB, 1FFh = 512 pages = 2 MB]						
		Value	Name	Description		
		0		1 page = 4 KB		
		1FFh		512 pages = 2 MB		
	11	RBWait	Description			Project
		Indicates that this ring has executed a WAIT_FOR_EVENT instruction and is currently waiting. Software can write a "1" to clear this bit, write of "0" has no effect. When the RB is waiting for an event and this bit is cleared, the wait will be terminated and the RB will be returned to arbitration.				Source
		RenderCS: RBWait is not set on executing WAIT_FOR_EVENT instruction waiting on Async Flip Pending.			BDW	RenderCS
	10	Semaphore Wait	Description			Project
		Indicates that this ring has executed a MI_SEMAPHORE_WAIT instruction and is currently waiting for wait condition to satisfy.				BDW
	9	Reserved	Format:	MBZ		
	8	Reserved	Project:	BDW		
		Format:		MBZ		
	7:3	Reserved	Format:	MBZ		

RING_BUFFER_CTL - Ring Buffer Control

Automatic Report Head Pointer				
Project:	BDW			
Source:	BSpec			
Description				
This field is written by software to control the automatic reporting (write) of this ring buffer's Head Pointer register (register DWord 1) to the corresponding location within the Hardware Status Page. Automatic reporting can either be disabled or enabled at 4KB, 64KB or 128KB boundaries within the ring buffer.				
When ExecList Enable bit is set the head pointer will be reported to the head pointer location in the Per-Process Hardware Status Page. MI_AUTOREPORT_4KB option is not supported on DevBDW_A stepping.	BDW			
Value	Name	Description	Project	
0	MI_AUTOREPORT_OFF	Automatic reporting disabled		
1	MI_AUTOREPORT_64KB	Report every 16 pages (64KB)		
2	MI_AUTOREPORT_4KB	Report every page (4KB) This mode must not be enabled in Ring Buffer mode of scheduling to minimize the auto reports.	BDW	RenderCS
2	MI_AUTOREPORT_4KB	Report every page (4KB) This mode must not be enabled in Ring Buffer mode of scheduling to minimize the auto reports.	BDW	BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS
3	MI_AUTOREPORT_128KB	Report every 32 pages (128KB)		

RING_BUFFER_CTL - Ring Buffer Control

	0	<p>Ring Buffer Enable</p> <table border="1"> <tr> <td>Format:</td><td>Enable</td></tr> </table> <p>This field is used to enable or disable this ring buffer. It can be enabled or disabled regardless of whether there are valid instructions pending. If disabled and the ring head equals ring tail, all state currently loaded in hardware is considered invalid.</p>	Format:	Enable			
Format:	Enable						
		<table border="1"> <thead> <tr> <th>Programming Notes</th><th>Source</th></tr> </thead> <tbody> <tr> <td> <p>Ring Buffer Mode of Scheduling: SW must follow the below programming notes during SW initialization phase or while enabling render engine's ring buffer for the first time, this would be coming out of boot, standby, hibernate or reset. This flow must be also followed during ring replay when ring buffer is disabled.</p> <ul style="list-style-type: none"> • SW must set the Force Wakeup bit to prevent GT from entering C6. • SW must dispatch workload (dummy context) to initialize render engine with default state such that any context switches that occur subsequently (Power Save) will save and restore coherent device state. Indirect pointers used in 3D states must point to valid graphics surface existing in memory. PP_DCLV followed by PP_DIR_BASE register should be programmed as part of initialization workload if PPGTT is enabled in GFX_MODE register. • SW must ensure all the register (MMIO) initialization/programming through CPU happens in this block or latter, this ensures the MMIO state is save/restored on subsequent context switches (Power Sequences). • Once the render engine is programmed with valid state and the configuration, Force Wakeup bit should be reset to enable C6 entry. </td><td>RenderCS</td></tr> </tbody> </table>	Programming Notes	Source	<p>Ring Buffer Mode of Scheduling: SW must follow the below programming notes during SW initialization phase or while enabling render engine's ring buffer for the first time, this would be coming out of boot, standby, hibernate or reset. This flow must be also followed during ring replay when ring buffer is disabled.</p> <ul style="list-style-type: none"> • SW must set the Force Wakeup bit to prevent GT from entering C6. • SW must dispatch workload (dummy context) to initialize render engine with default state such that any context switches that occur subsequently (Power Save) will save and restore coherent device state. Indirect pointers used in 3D states must point to valid graphics surface existing in memory. PP_DCLV followed by PP_DIR_BASE register should be programmed as part of initialization workload if PPGTT is enabled in GFX_MODE register. • SW must ensure all the register (MMIO) initialization/programming through CPU happens in this block or latter, this ensures the MMIO state is save/restored on subsequent context switches (Power Sequences). • Once the render engine is programmed with valid state and the configuration, Force Wakeup bit should be reset to enable C6 entry. 	RenderCS	
Programming Notes	Source						
<p>Ring Buffer Mode of Scheduling: SW must follow the below programming notes during SW initialization phase or while enabling render engine's ring buffer for the first time, this would be coming out of boot, standby, hibernate or reset. This flow must be also followed during ring replay when ring buffer is disabled.</p> <ul style="list-style-type: none"> • SW must set the Force Wakeup bit to prevent GT from entering C6. • SW must dispatch workload (dummy context) to initialize render engine with default state such that any context switches that occur subsequently (Power Save) will save and restore coherent device state. Indirect pointers used in 3D states must point to valid graphics surface existing in memory. PP_DCLV followed by PP_DIR_BASE register should be programmed as part of initialization workload if PPGTT is enabled in GFX_MODE register. • SW must ensure all the register (MMIO) initialization/programming through CPU happens in this block or latter, this ensures the MMIO state is save/restored on subsequent context switches (Power Sequences). • Once the render engine is programmed with valid state and the configuration, Force Wakeup bit should be reset to enable C6 entry. 	RenderCS						
		<p>Render CS Only: Ring Buffer Mode of Scheduling: SW must follow the below programming notes before disabling ring buffer to ensure HW is not in middle of the IDLE flows.</p> <ul style="list-style-type: none"> • SW must set the Force Wakeup bit to prevent GT from entering C6. • Disable IDLE messaging in CS (Write 0x2050[31:0] = 0x00010001) • Poll/Wait for register bits of <u>0x22AC[6:0]</u> turn to 0x30 value. • Disable Ring Buffer • Enable IDLE messaging in CS (Write 0x2050[31:0] = 0x00010000) • Force Wakeup bit should be reset to enable C6 entry. 	RenderCS				

Ring Buffer Current Context ID Register

BCS_RCCID - Ring Buffer Current Context ID Register

Register Space: MMIO: 0/2/0
 Project: BDW
 Source: BlitterCS

Default Value: 0x00000000, 0x00000000
 Access: R/W
 Size (in bits): 64

Address: 22190h-22197h

This register contains the current ring context ID associated with the ring buffer.

Programming Notes

The current context registers must not be written directly (via MMIO). The RCCID register should only be updated indirectly from RNCID.

DWord	Bit	Description
0	63:0	Unnamed See Context Descriptor for BCS.

Ring Buffer Head

RING_BUFFER_HEAD - Ring Buffer Head		
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x00000000 Access: R/W Size (in bits): 32		
Address:		02034h-02037h
Name:		Ring Buffer Head
ShortName:		RING_BUFFER_HEAD_RCSUNIT
Address:		12034h-12037h
Name:		Ring Buffer Head
ShortName:		RING_BUFFER_HEAD_VCSUNIT0
Address:		1A034h-1A037h
Name:		Ring Buffer Head
ShortName:		RING_BUFFER_HEAD_VECSUNIT
Address:		1C034h-1C037h
Name:		Ring Buffer Head
ShortName:		RING_BUFFER_HEAD_VCSUNIT1
Address:		22034h-22037h
Name:		Ring Buffer Head
ShortName:		RING_BUFFER_HEAD_BCSUNIT
Description		
<p>This register is used to define and operate the ring buffer mechanism which can be used to pass instructions to the command interface. The buffer itself is located in a physical memory region. The ring buffer is defined by a 4 Dword register set that includes starting address, length, head offset, tail offset, and control information. Refer to the Programming Interface chapter for a detailed description of the parameters specified in this ring buffer register set, restrictions on the placement of ring buffer memory, arbitration rules, and in how the ring buffer can be used to pass instructions. Ring Buffer Head Offsets must be properly programmed before ring is enabled. A Ring Buffer can be enabled when empty.</p>		
DWord	Bit	Description
0	31:21	Wrap Count Format: U11 count of ring buffer wraps
		This field is incremented by 1 whenever the Head Offset wraps from the end of the buffer back to the start (i.e., whenever it wraps back to 0). Appending this field to the Head Offset field effectively creates a virtual 4GB Head "Pointer" which can be used as a tag associated with instructions placed in a ring buffer. The Wrap Count itself will wrap to 0 upon overflow.

RING_BUFFER_HEAD - Ring Buffer Head

	20:2	Head Offset
		Format: GraphicsAddress[20:2] DWord Offset
<p>This field indicates the offset of the <i>next</i> instruction DWord to be parsed. Software will initialize this field to select the first DWord to be parsed once the RB is enabled. (Writing the Head Offset while the RB is enabled is UNDEFINED). Subsequently, the device will increment this offset as it executes instructions - until it reaches the QWord specified by the Tail Offset. At this point the ring buffer is considered "empty".</p>		
Programming Notes		
<p>A RB can be enabled empty or containing some number of valid instructions.</p>		
	1	Reserved
		Format: MBZ
	0	Reserved
		Project: BDW
		Format: MBZ

Ring Buffer Start

RING_BUFFER_START - Ring Buffer Start						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Access:	R/W					
Size (in bits):	32					
Address:	02038h-0203Bh					
Name:	Ring Buffer Start					
ShortName:	RING_BUFFER_START_RCSUNIT					
Address:	12038h-1203Bh					
Name:	Ring Buffer Start					
ShortName:	RING_BUFFER_START_VCSUNIT0					
Address:	1A038h-1A03Bh					
Name:	Ring Buffer Start					
ShortName:	RING_BUFFER_START_VECSUNIT					
Address:	1C038h-1C03Bh					
Name:	Ring Buffer Start					
ShortName:	RING_BUFFER_START_VCSUNIT1					
Address:	22038h-2203Bh					
Name:	Ring Buffer Start					
ShortName:	RING_BUFFER_START_BCSUNIT					
Description						
<p>These registers are used to define and operate the "ring buffer" mechanism which can be used to pass instructions to the command interface. The buffer itself is located in a physical memory region. The ring buffer is defined by a 4 Dword register set that includes starting address, length, head offset, tail offset, and control information. Refer to the Programming Interface chapter for a detailed description of the parameters specified in this ring buffer register set, restrictions on the placement of ring buffer memory, arbitration rules, and in how the ring buffer can be used to pass instructions.</p>						
DWord	Bit	Description				
0	31:12	Starting Address				
		Format:	GraphicsAddress[31:12]RingBuffer			
		<p>This field specifies Bits 31:12 of the 4KB-aligned starting Graphics Address of the ring buffer. Address bits 31 down to 29 must be zero. All ring buffer pages must map to Main Memory (uncached) pages. Ring Buffer addresses are always translated through the global GTT.</p>				
	11:0	Reserved				
		Format:	MBZ			

Ring Buffer Tail

RING_BUFFER_TAIL - Ring Buffer Tail		
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x00000000 Access: R/W Size (in bits): 32		
Address:		02030h-02033h
Name:		Ring Buffer Tail
ShortName:		RING_BUFFER_TAIL_RCSUNIT
Address:		12030h-12033h
Name:		Ring Buffer Tail
ShortName:		RING_BUFFER_TAIL_VCSUNIT0
Address:		1A030h-1A033h
Name:		Ring Buffer Tail
ShortName:		RING_BUFFER_TAIL_VECSUNIT
Address:		1C030h-1C033h
Name:		Ring Buffer Tail
ShortName:		RING_BUFFER_TAIL_VCSUNIT1
Address:		22030h-22033h
Name:		Ring Buffer Tail
ShortName:		RING_BUFFER_TAIL_BCSUNIT
Description		
These registers are used to define and operate the "ring buffer" mechanism which can be used to pass instructions to the command interface. The buffer itself is located in a linear memory region. The ring buffer is defined by a 4 Dword register set that includes starting address, length, head offset, tail offset, and control information. Refer to the Programming Interface chapter for a detailed description of the parameters specified in this ring buffer register set, restrictions on the placement of ring buffer memory, arbitration rules, and in how the ring buffer can be used to pass instructions. Ring Buffer Tail Offsets must be properly programmed before ring is enabled. A Ring Buffer can be enabled when empty.		
DWord	Bit	Description
0	31:21	Reserved Format: MBZ

RING_BUFFER_TAIL - Ring Buffer Tail

	20:3	Tail Offset	
		Format:	GraphicsAddress[20:3]
<p>This field is written by software to specify where the valid instructions placed in the ring buffer end. The value written points to the QWord past the last valid QWord of instructions. In other words, it can be defined as the next QWord that software will write instructions into. Software must write subsequent instructions to QWords following the Tail Offset, possibly wrapping around to the top of the buffer (i.e., software can't skip around within the buffer). Note that all DWords prior to the location indicated by the Tail Offset must contain valid instruction data - which may require instruction padding by software. See Head Offset for more information.</p>			
		Programming Notes	Project
		[Ring Buffer Mode Of scheduling only][Video CS, Video Enhancement CS, Blitter CS]: HW loses Page Directory (PPGTT) information on becoming IDLE. SW must always program the PD information through MI_LOAD_REGISTER_IMM command in the ring buffer prior to programming workload begins on every ring dispatch. This will ensure Page Directory information is not lost due to IDLE flows.	BDW
	2:0	Reserved	
		Format:	MBZ

RIRB Control, Status and Size

RIRBCTL_STS_SIZE - RIRB Control, Status and Size											
Register Space: MMIO: 0/3/0 Project: BDW Default Value: 0x00420000 Access: R/W Size (in bits): 32											
Address: 0005Ch-0005Fh											
DWord	Bit	Description									
0	31:24	Reserved <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ							
Format:	MBZ										
23:20	RIRB Size Capability <table border="1"> <tr> <td>Default Value:</td> <td>4h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Default Value:	4h	Access:	RO						
Default Value:	4h										
Access:	RO										
Programming Notes											
Default of 0100b indicates that the dHDA only supports a RIRB size of 256 RIRB entries (2048B).											
19:18	Reserved <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ								
Format:	MBZ										
17:16	RIRB Size <table border="1"> <tr> <td>Default Value:</td> <td>10b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Default Value:	10b	Access:	RO						
Default Value:	10b										
Access:	RO										
Programming Notes											
This bit field is hardwired to 10b which sets the RIRB size to 256 entries (2048B).											
15:11	Reserved <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ								
Format:	MBZ										
10	Response Overrun Interrupt Status <table border="1"> <tr> <td>Access:</td> <td>R/WC</td> </tr> </table>	Access:	R/WC								
Access:	R/WC										
<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>No_Overrun [Default]</td><td>See ProgramminNotes</td></tr> <tr> <td>1b</td><td>Overrun</td><td>See ProgramminNotes</td></tr> </tbody> </table>			Value	Name	Description	0b	No_Overrun [Default]	See ProgramminNotes	1b	Overrun	See ProgramminNotes
Value	Name	Description									
0b	No_Overrun [Default]	See ProgramminNotes									
1b	Overrun	See ProgramminNotes									

RIRBCTL_STS_SIZE - RIRB Control, Status and Size

Programming Notes		
Hardware sets this bit to a 1 when the RIRB DMA engine is not able to write the incoming responses to memory before additional incoming responses overrun the internal FIFO. When the overrun occurs, the hardware will drop the responses which overrun the buffer. An interrupt may be generated if the Response Overrun Interrupt Control bit is set. Note that this status bit is set even if an interrupt is not enabled for this event. Software clears this flag by writing a 1 to this bit.		
9	Reserved	Format: MBZ
8	Response Interrupt	Access: R/WC
Value Name Description		
0b	Disable [Default]	See Programming Notes
1b	Enable	See Programming Notes
Programming Notes		
Hardware sets this bit to a 1 when an interrupt has been generated after N number of Responses are sent to the RIRB buffer OR when an empty Response slot is encountered on all SDI[x] inputs (whichever occurs first). Note: This status bit is set even if an interrupt is not enabled for this event. Software clears this flag by writing a 1 to this bit.		
7:3	Reserved	Format: MBZ
2	Response Overrun Interrupt Control	Access: R/W
Value Name Description		
0b	Disable [Default]	See Programming Notes
1b	Enable	See Programming Notes
Programming Notes		
If this bit is set (and GIE and CIE are enabled), the hardware will generate an interrupt when the Response Overrun Interrupt Status bit is set.		

RIRBCTL_STS_SIZE - RIRB Control, Status and Size

	1	RIRB DMA Enable												
		Access:	R/W Variant											
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>DMA STOP [Default]</td> <td>See Programming Notes</td> </tr> <tr> <td>1b</td> <td>DMA RUN</td> <td>See Programming Notes</td> </tr> </tbody> </table>			Value	Name	Description	0b	DMA STOP [Default]	See Programming Notes	1b	DMA RUN	See Programming Notes	
Value	Name	Description												
0b	DMA STOP [Default]	See Programming Notes												
1b	DMA RUN	See Programming Notes												
		Programming Notes												
		After SW writes a 0 to this bit, the HW may not stop immediately. The hardware will physically update the bit to a 0 when the DMA engine is truly stopped. SW must read a 0 from this bit to verify that the DMA is truly stopped.												
	0	Response Interrupt Control												
		Access:	R/W											
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disable Interrupt [Default]</td> <td>See Programming Notes</td> </tr> <tr> <td>1b</td> <td>Generate Interrupt</td> <td>See Programming Notes</td> </tr> </tbody> </table>		Value	Name	Description	0b	Disable Interrupt [Default]	See Programming Notes	1b	Generate Interrupt	See Programming Notes		
Value	Name	Description												
0b	Disable Interrupt [Default]	See Programming Notes												
1b	Generate Interrupt	See Programming Notes												
		Programming Notes												
		When generating an interrupt: 1b, (if GIE and CIE are enabled) after N number of Responses are sent to the RIRB buffer OR when an empty Response slot is encountered on all SDI_x inputs (whichever occurs first). The N counter is reset when the interrupt is generated.												

RIRB (Response Input Ring Buffer)-Lower Base Address

RIRBLBASE - RIRB (Response Input Ring Buffer)-Lower Base Address								
Register Space:	MMIO: 0/3/0							
Project:	BDW							
Default Value:	0x00000000							
Access:	R/W							
Size (in bits):	32							
Address:	00050h-00053h							
DWord	Bit	Description						
0	31:7	RIRBLBASE						
		<table border="1"> <tr> <td>Default Value:</td><td>0h</td></tr> <tr> <td colspan="2">Programming Notes</td></tr> <tr> <td colspan="2">Lower address of the Response Input Ring Buffer (RIRBLBASE) allows the RIRB Base Address to be assigned on any 128-B boundary. This register field must not be written when the DMA engine is running or the DMA transfer may be corrupted.</td></tr> </table>	Default Value:	0h	Programming Notes		Lower address of the Response Input Ring Buffer (RIRBLBASE) allows the RIRB Base Address to be assigned on any 128-B boundary. This register field must not be written when the DMA engine is running or the DMA transfer may be corrupted.	
Default Value:	0h							
Programming Notes								
Lower address of the Response Input Ring Buffer (RIRBLBASE) allows the RIRB Base Address to be assigned on any 128-B boundary. This register field must not be written when the DMA engine is running or the DMA transfer may be corrupted.								
	6:0	RIRBLBASE LOWER BITS						
		<table border="1"> <tr> <td>Default Value:</td><td>0h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> <tr> <td colspan="2">Programming Notes</td></tr> <tr> <td colspan="2">Hardwired to 0 to force 128-byte buffer alignment for cache line fetch optimizations.</td></tr> </table>	Default Value:	0h	Access:	RO	Programming Notes	
Default Value:	0h							
Access:	RO							
Programming Notes								
Hardwired to 0 to force 128-byte buffer alignment for cache line fetch optimizations.								

RIRB (Response Input Ring Buffer)-Upper Base Address

RIRBUBASE - RIRB (Response Input Ring Buffer)-Upper Base Address				
Register Space:		MMIO: 0/3/0		
Project:		BDW		
Default Value:		0x00000000		
Access:		R/W		
Size (in bits):		32		
Address:				
00054h-00057h				
DWord	Bit	Description		
0	31:0	<p>RIRBUBASE</p> <table border="1"> <tr> <td>Default Value:</td><td>0h</td></tr> </table> <p>Programming Notes</p> <p>Upper 32 bits of address of the Response Input Ring Buffer. This register field must not be written when the DMA engine is running or the DMA transfer may be corrupted.</p>	Default Value:	0h
Default Value:	0h			

RIRB Write Pointer and Interrupt Count

RIRBWP_RINTCNT - RIRB Write Pointer and Interrupt Count																
DWord	Bit	Description														
0	31:24	Reserved <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ												
Format:	MBZ															
	23:16	Response Interrupt Count <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>The DMA engine should be stopped when changing this field or else an interrupt may be lost. Note that each Response occupies 2 Dwords in the RIRB. This is compared to the total number of responses that have been returned, as opposed to the number of frames in which there were responses. If more than one codec responds in one frame, then the count is increased by the number of responses received in the frame.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00000001b</td> <td></td> <td>1 Response sent to RIRB</td> </tr> <tr> <td>00000010b-11111111b</td> <td></td> <td>2 - 255 Response sent to RIRB</td> </tr> <tr> <td>00000000b</td> <td>[Default]</td> <td>256 Responses sent to RIRB</td> </tr> </tbody> </table>	Access:	RO	Value	Name	Description	00000001b		1 Response sent to RIRB	00000010b-11111111b		2 - 255 Response sent to RIRB	00000000b	[Default]	256 Responses sent to RIRB
Access:	RO															
Value	Name	Description														
00000001b		1 Response sent to RIRB														
00000010b-11111111b		2 - 255 Response sent to RIRB														
00000000b	[Default]	256 Responses sent to RIRB														
	15	RIRB Write Pointer Reset <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>WO</td> </tr> </table> <p>Programming Notes</p> <p>Software writes a 1 to this bit to reset the RIRB Write Pointer to 0's. The RIRB DMA engine must be stopped prior to resetting the Write Pointer or else DMA transfer may be corrupted. This bit will always be read as 0.</p>	Default Value:	0b	Access:	WO										
Default Value:	0b															
Access:	WO															
	14:8	Reserved <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ												
Format:	MBZ															

RIRBWP_RINTCNT - RIRB Write Pointer and Interrupt Count

	7:0	RIRB Write Pointer
		Default Value:
		00h
		Access:
		RO Variant
): Indicates the last valid RIRB entry written by the DMA controller. Software reads this field to determine how many responses it can read from the RIRB. The value read indicates the RIRB Write Pointer offset in 2 Dword RIRB entry units (since each RIRB entry is 2 Dwords long). Supports up to 256 RIRB entries (256 x 8B=2KB). This field may be read while the DMA engine is running.		

Root Table Address Pointer Value First 31_0

RTAPV_1_310 - Root Table Address Pointer Value First 31_0						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	0F500h					
This register is used to store local copy of the Root Table address pointer value.						
DWord	Bit	Description				
0	31:0	<p>First Address 31 to 0</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Bits 31:11 = Root Table Address Pointer Value 31:11. Bits 10:1 = Reserved. Bit 0 = Enabled for Root Table Address Pointer Value 31:11.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

Root Table Address Pointer Value Second 31_0

RTAPV_2_310 - Root Table Address Pointer Value Second31_0						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	0F504h					
This register is used to store local copy of the Root Table address pointer value.						
DWord	Bit	Description				
0	31:0	<p>Second Address 31 to 0</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Bits 31:8 = Reserved. Bits 7:1 = Root Table Address Pointer Value 38:32. Bit 0 = Enabled for Root Table Address Pointer Value 38:32.</p>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

RP Decrease Limit

RP_LIMIT1 - RP Decrease Limit				
DWord	Bit	Description		
0	31:24	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
Access:	RO			
23:0	Decrease Threshold <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Decrease Threshold (DECLIMIT): This register contains the threshold used to determine whether a switch to a higher frequency is desirable. FRQDUM determines the meaning of this register: Busy Min Continuous Limit. Busy Min Average Limit. Idle Max Continuous Limit. The values are: 0 = 0 usec. 1 = 1.28 usec. 2 = 2.56 usec. 3 = 3.84 usec. FF FFFF = 21.474 sec.</p>	Access:	R/W	
Access:	R/W			

RP Downwards Evaluation Interval

RP_DECREQ_EI - RP Downwards Evaluation Interval				
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x00000000 Size (in bits): 32				
Address: 0A06Ch				
DWord	Bit	Description		
0	31:24	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
Access:	RO			
	23:0	Evaluation Interval Period for Downwards Freq Direction <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>The geyserville performance status is averaged over this interval, and the results are used to possibly recommend a switch to the slower render clock frequency (either directly by hardware or via an interrupt activating a SW decision). 0 = 0 usec. 1 = 1.28 usec. 2 = 2.56 usec. 3 = 3.84 usec. FF FFFF = 21.474 sec. pmcr_ei_down[23:0].</p>	Access:	R/W
Access:	R/W			

RP Increase Limit

RP_LIMIT0 - RP Increase Limit				
DWord	Bit	Description		
0	31:24	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
Access:	RO			
23:0	Increase Threshold <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Increase Threshold (INCLIMIT): This register contains the threshold used to determine whether a switch to a higher frequency is desirable. FRQIUM determines the meaning of this register: Busy Max Continuous Limit. Busy Max Average Limit. Idle Min Continuous Limit. The values are: 0 = 0 usec. 1 = 1.28 usec. 2 = 2.56 usec. 3 = 3.84 usec. FF FFFF = 21.474 sec.</p>	Access:	R/W	
Access:	R/W			

RP Interrupt Down Timeout Limit

INTERRUPT_LIMIT0 - RP Interrupt Down Timeout Limit				
Register Space:	MMIO: 0/2/0			
Project:	BDW			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0A010h			
DWord	Bit	Description		
0	31:24	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
Access:	RO			
23:0	RP Down Timeout Timer <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>RPDNTIMOUT: The value in this register contains the timeout value for gfx idleness without gfx wake necessary to trigger. the Render Geyerville Downward Timeout interrupt if the current frequency gear is greater than F Down Interrupt Limiter.</p> <p>00 0000h = 0 usec. 00 0001h = 1.28 usec. 00 0002h = 2.56 usec. 00 0003h = 3.84 usec. FF FFFFh = 21.474 sec.</p>	Access:	R/W	
Access:	R/W			

RP Interrupt Up/Down Frequency Limits

INTERRUPT_LIMIT1 - RP Interrupt Up/Down Frequency Limits						
DWord	Bit	Description				
0	31	Reserved <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Project:	BDW	Access:	RO
Project:	BDW					
Access:	RO					
	30:24	FUp Interrupt Limiter <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>FUp Interrupt Limiter (RPUUpLim): Upward freq based interrupts are gated if actual GT MLC ratio is equal to or higher than this value. Examples: 000_0110b = 6 (gate if MLCclk >= 600MHz). 000_0111b = 7 (gate if MLCclk >= 700MHz). 000_1010b = 10 (gate if MLCclk >= 1000MHz). All values less than or greater than the supported frequency range are reserved.</p>	Project:	BDW	Access:	R/W
Project:	BDW					
Access:	R/W					
	23	Reserved <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Project:	BDW	Access:	RO
Project:	BDW					
Access:	RO					
	22:16	F Down Interrupt Limiter <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>F Down Interrupt Limiter (RPDWNLim): FDownInterrupt Limiter (RPDWNLim): Downward based interrupts are gated if actual GT MLC ratio is equal to or lower than the values in FDownInterrupt Limiter. Examples: 000_0110b = 6 (gate if MLCclk <= 600MHz). 000_0111b = 7 (gate if MLCclk <= 700MHz). 000_1010b = 10 (gate if MLCclk <= 1000MHz). All values less than or greater than the supported frequency range are reserved.</p>	Project:	BDW	Access:	R/W
Project:	BDW					
Access:	R/W					
	15:14	Reserved <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Project:	BDW	Access:	RO
Project:	BDW					
Access:	RO					

INTERRUPT_LIMIT1 - RP Interrupt Up/Down Frequency Limits

	13:0	Reserved	Access:	RO
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RP Normal Software Frequency Request

RP_FREQ_NORMAL - RP Normal Software Frequency Request				
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x00000000 Size (in bits): 32				
Address: 0A008h				
This 32 bit value is written to the PCU IO_THREAD_P_REQ register when NOT in Video Turbo mode.				
DWord	Bit	Description		
0	31	<p>Turbo Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>The Turbo Disable bit is determined by SW. NOTE: If Turbo is disable for ANY thread, it will prevent turbo for ALL threads.</p>	Access:	R/W
Access:	R/W			
	30:24	<p>P State Request</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>This field indicates the maximum P-State request in units of 100MHz.</p>	Access:	R/W
Access:	R/W			
	23:18	<p>P State Offset</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>This field defined the number of steps that Energy Efficient P-State is allowed to fall in units of 100 MHz.</p>	Access:	R/W
Access:	R/W			
	17:14	<p>Energy Efficient policy</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>The energy efficiency policy is determined by SW.</p>	Access:	R/W
Access:	R/W			
	13:0	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
Access:	RO			

RP Software Frequency Request Hysteresis

RP_FREQ_HYST - RP Software Frequency RequestHysteresis				
Register Space: MMIO: 0/2/0				
Project: BDW				
Default Value: 0x00000000				
Size (in bits): 8				
Address: 0A004h				
DWord	Bit	Description		
0	5:0	<p>RP Software Frequency Request Hysteresis</p> <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Hysteresis Timer for ignoring Idle/Busy indications from *CS agents for the purpose of selecting video/turbo frequencies.</p> <p>0h = Disabled (default).</p> <p>1h = 1.28 usec.</p> <p>2h = 2.56 usec.</p> <p>...</p> <p>3Fh = 80.64 usec.</p>	Access:	R/W
Access:	R/W			

RP Upwards Evaluation Interval

RP_INCFREQ_EI - RP Upwards Evaluation Interval				
DWord	Bit	Description		
0	31:24	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
Access:	RO			
23:0	Evaluation Interval Period for Upwards Freq Direction <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>The geyserville performance status is averaged over this interval, and the results are used to possibly recommend a switch to the faster render clock frequency (either directly by hardware or via an interrupt activating a SW decision). 0 = 0 usec. 1 = 1.28 usec. 2 = 2.56 usec. 3 = 3.84 usec. FF FFFF = 21.474 sec. pmcr_ei_up[23:0].</p>	Access:	R/W	
Access:	R/W			

RP Video Turbo Software Frequency Request

RP_FREQ_VIDEOTURBO - RP Video Turbo Software Frequency Request

Register Space: MMIO: 0/2/0

Project: BDW

Default Value: 0x00000000

Size (in bits): 32

Address: 0A00Ch

This 32 bit value is written to the PCU IO_THREAD_P_REQ register when in Video Turbo mode.

DWord	Bit	Description
0	31	Turbo Disable Access: R/W The Turbo Disable bit is determined by SW. NOTE: If Turbo is disable for ANY thread, it will prevent turbo for ALL threads.
	30:24	P State Request Access: R/W This field indicates the maximum P-State request in units of 100MHz.
	23:18	P State Offset Access: R/W This field defined the number of steps that Energy Efficient P-State is allowed to fall in units of 100 MHz.
	17:14	Energy Efficient policy Access: R/W The energy efficiency policy is determined by SW.
	13:0	Reserved Access: RO

RS_PREEMPT_STATUS_UDW

RS_PREEMPT_STATUS_UDW - RS_PREEMPT_STATUS_UDW				
Register Space:	MMIO: 0/2/0			
Project:	BDW			
Source:	RenderCS			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Address:	02174h			
<p>Preemption from First Level Batch Buffer: This register contains the offset in to the Batch Buffer on which Resource streamer got preempted. Note that it is offset from the Batch Start Address and not the graphics address corresponding to the preempted instruction on Batch Buffer. This register's contents will be looked at by Command Streamer on the next RS Start Trigger to provide the appropriate batch start address. Following preemption, context save happens on which this register is context saved, after context save the register gets auto reset by Command Streamer. This register gets context save/restored by Render Command Streamer as part of its render context.</p> <p>Preemption from Second Level Batch Buffer: This register contains the graphics address of the instruction in Second Level Batch Buffer on which Resource streamer got preempted. This register's contents will be looked at by Command Streamer on the next RS Start Trigger to provide the appropriate batch start address. Following preemption, context save happens on which this register is context saved, after context save the register gets auto reset by Command Streamer. This register gets context save/restored by Render Command Streamer as part of its render context.</p>				
<p style="text-align: center;">Programming Notes</p> <ul style="list-style-type: none"> This register is accessed by Render Command Streamer as part of render context save/restore; this register should be exercised by S/W only for resetting the register contents if required. Following preemption if there is no context save, SW should program this register with 0x0 so that it does not interfere with proceeding workloads. 				
DWord	Bit	Description		
0	31:16	<p>Reserved</p> <table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ
Format:	MBZ			
15:0	<p>Batch Buffer Offset Upper DWORD</p> <table border="1"> <tr> <td>Format:</td><td>GraphicsAddress[47:32]</td></tr> </table> <p>This field specifies the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space of the last preempted second level batch buffer in resource streamer.</p>	Format:	GraphicsAddress[47:32]	
Format:	GraphicsAddress[47:32]			

RS Preemption Hint

RS_PRE_HINT - RS Preemption Hint					
Register Space:	MMIO: 0/2/0				
Project:	BDW				
Source:	RenderCS				
Default Value:	0x00000000				
Access:	R/W				
Size (in bits):	32				
Address:	024C0h				
<p>This register contains the Dword aligned Graphics address in to the Batch Buffer corresponding to either 3D_PRIMITIVE or RCS-RS sync command called Preemption Hint Address. When Preemption Hint Address is enabled, RS will honor preemption request from RCS only on parsing 3D_PRIMITIVE/RCS-RS sync command at Preemption Hint Address.</p>					
Programming Notes					
Programming Restriction:					
<p>This register should NEVER be programmed in functional mode, this should be used only in validation mode to achieve deterministic behavior of preempting Resource Streamer in command stream. Programmer has to ensure that RS Preemption Hint register gets programmed well before RS gets preempted by RCS. Note that this register should be programmed with caution as it can lead to indefinite stalls in RS.</p> <ul style="list-style-type: none"> a. RS will preempt on receiving preemption request from RCS only on reaching the instruction in the batch buffer corresponding to the address mentioned in RS_PREEMPT_HINT. RS could hit an RCS-RS sync command before reaching the address mentioned in the RS_PREEMPT_HINT, in this case RS should preempt on the sync command. b. RS could hit the address mentioned in 3D_PREEMPT_HINT before receiving preempt request from RCS. In this case RS will stall at this command until it receives preemption request from RCS and then preempts. 					
DWord	Bit	Description			
0	31:2	Preemption Hint Address			
		<table border="1"> <tr> <td>Format:</td><td>U30</td></tr> <tr> <td colspan="2">This field contains the Dword aligned Graphics Address in to the batch buffer as Preemption Hint.</td></tr> </table>	Format:	U30	This field contains the Dword aligned Graphics Address in to the batch buffer as Preemption Hint.
Format:	U30				
This field contains the Dword aligned Graphics Address in to the batch buffer as Preemption Hint.					
	1	Reserved			
		<table border="1"> <tr> <td>Format:</td><td>Enabled</td></tr> </table>	Format:	Enabled	
Format:	Enabled				

RS_PRE_HINT - RS Preemption Hint

	0	Preemption Hint		
		Format:		
		Enabled		
		Value	Name	Description
		0h	Disabled	Preemption hint is disabled for Resource Streamer.
		1h	Enabled	Preemption hint is enabled for Resource streamer.

RS Preemption Hint UDW

RS_PREEMPTION_HINT_UDW - RS Preemption Hint UDW				
Register Space: MMIO: 0/2/0 Project: BDW Source: RenderCS Default Value: 0x00000000 Access: R/W Size (in bits): 32				
Address: 024C4h This register contains the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space of the Batch Buffer corresponding to either 3D_PRIMITIVE or RCS-RS sync command called Preemption Hint Address. When Preemption Hint Address is enabled, RS will honor preemption request from RCS only on parsing 3D_PRIMITIVE/RCS-RS sync command at Preemption Hint Address.				
Restriction				
This register should NEVER be programmed in functional mode, this should be used only in validation mode to achieve deterministic behavior of preempting Resource Streamer in command stream. See RS_PRE_HINT definition for further restrictions.				
DWord	Bit	Description		
0	31:16	Reserved <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Format:</td><td style="width: 50%;">MBZ</td></tr> </table>	Format:	MBZ
Format:	MBZ			
15:0	Preemption Hint Address Upper DWORD <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Format:</td><td style="width: 50%;">GraphicsAddress[47:32]</td></tr> </table> <p>This field contains the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space of the batch buffer as Preemption Hint.</p>	Format:	GraphicsAddress[47:32]	
Format:	GraphicsAddress[47:32]			

Sampler control register

SAMPLER_CTL - Sampler control register		
Register Space: MMIO: 0/2/0 Project: BDW Source: RenderCS Default Value: 0x00000000 Access: R/W Size (in bits): 32		
Address: 0E140h Valid Projects: [BDW]		
DWord	Bit	Description
0	31:16	ECO Reserved 1 Reserved: MBZ
	15:8	Reserved
	7:3	Sampler unit select 00000 ? SIUnit 00001 ? PLUnit 00010 ? DGUnit 00011 ? QCUnit 00100 ? FTUnit 00101 ? DMUnit 00110 ? SCUnit 00111 ? FLUnit 01000 ? SOUnit 01001 - AVSunit
	2	ECO Reserved 2 Reserved MBZ (These bits are moved to CS unit MMIO register section at 0x208c, bit 2)
	1:0	ECO Reserved 3 Reserved MBZ

SAMPLER Mode Register

SAMPLER_MODE - SAMPLER Mode Register					
Register Space:	MMIO: 0/2/0				
Project:	BDW				
Source:	RenderCS				
Default Value:	0x00000000				
Size (in bits):	32				
Trusted Type:	1				
Address:	07028h				
Valid Projects:	[BDW]				
<p>This register has bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16]. To set bit0, for example, the data would be 0x0001_0001. To clear bit0, for example, the data would be 0x0001_0000. Note that mask bit is the data bit offset + 16.</p>					
DWord	Bit	Description			
0	31:16	Reserved <table border="1"> <tr> <td>Access:</td><td>RO</td></tr> </table>	Access:	RO	
Access:	RO				
15:14	ECO Reserved 1 <table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ		
Format:	MBZ				
11:10	Reserved <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	All	Format:	MBZ
Project:	All				
Format:	MBZ				
13:8	ECO Reserved 2 <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	BDW	Format:	MBZ
Project:	BDW				
Format:	MBZ				
7	ECO Reserved 3 <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	All	Format:	MBZ
Project:	All				
Format:	MBZ				
6	ECO_SCRATCH3C <table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ		
Format:	MBZ				
5	ECO_SCRATCH3B <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	BDW	Format:	MBZ
Project:	BDW				
Format:	MBZ				

SAMPLER_MODE - SAMPLER Mode Register

	4:0	Sample_d Quality Mode		
		Project: BDW		
		Format: U5		
This field configures the image quality mode for the sample_d message in the sampling engine. In general, performance will increase with each step of reduced quality.				
Value	Name	Description		Project
00h	Disabled	Full quality is enabled, matching prior products		All
01h-1Fh		Quality degrades with each larger value, performance improves with each larger value		All

Save Timer

SVTIMER - Save Timer																
DWord	Bit	Description														
0	31	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Reserved.</p>	Access:	RO												
Access:	RO															
	30:29	<p>Counter Enabling Selection</p> <table border="1"> <tr> <td>Default Value:</td> <td>11b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>LPFC provides rudimentary compression by allowing software to select from several predefined levels of event reporting. Based on the value of this bitfield, only a certain number of the programmed events in the "Event Selection and Base Counters" registers (CNT0CL, CNT1CL, ..., CNT7CL) will be tracked and reported:</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Selected Counters</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>Counter 0</td> </tr> <tr> <td>01</td> <td>Counters 0 & 1</td> </tr> <tr> <td>10</td> <td>Counters 0, 1, 2, & 3</td> </tr> <tr> <td>11</td> <td>Counters 0 - 7</td> </tr> </tbody> </table> <p>Signal - lpfc_cnt_enabled [1:0].</p>	Default Value:	11b	Access:	R/W	Value	Selected Counters	00	Counter 0	01	Counters 0 & 1	10	Counters 0, 1, 2, & 3	11	Counters 0 - 7
Default Value:	11b															
Access:	R/W															
Value	Selected Counters															
00	Counter 0															
01	Counters 0 & 1															
10	Counters 0, 1, 2, & 3															
11	Counters 0 - 7															
	28:24	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Reserved.</p>	Access:	RO												
Access:	RO															

SVTIMER - Save Timer

23:0	<p>Save Timer Interval</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Default Value:</td><td style="padding: 2px;">00000000000010000000000000b</td></tr> <tr> <td style="padding: 2px;">Access:</td><td style="padding: 2px;">R/W</td></tr> </table> <p>Save Timer Interval (SVTMRINT). Save Timer Interval: This is the interval for sampling the performance counters and writing to memory. Each time it expires, the counters are sampled and packetized to be sent to DMA controller. The minimum granularity of sampling period is 256 clocks. The value in this register is used as 256 x value to find the sampling window. For a 1Ghz core clock it provides up to 4ns of sampling period while matching the maximum capability of the event counters. 1h - 256clks. 2h - 512clks. ... 8h - 2048clks. Signal - lpconf_lpfcc_savetimer_int [23:0].</p>	Default Value:	00000000000010000000000000b	Access:	R/W
Default Value:	00000000000010000000000000b				
Access:	R/W				

SBI_ADDR

SBI_ADDR			
Register Space: MMIO: 0/2/0 Project: DevLPT Default Value: 0x00000000 Access: R/W Size (in bits): 32			
Address: C6000h-C6003h Name: SBI Address ShortName: SBI_ADDR Power: Always on Reset: PLTRST#			
DWord	Bit	Description	
0	31:16	Address Offset Register address offset. Program the upper 8 bits with the Target ID and the lower 8 bits with the Register Start.	
	15:11	Reserved <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:
Format:	MBZ		
10:8	Base Address Register Base Address Register (BAR). Always program to 000b.		
7:0	Routing ID Routing ID (RID). Always program to 00h.		

SBI_CTL_STAT

SBI_CTL_STAT					
Register Space: MMIO: 0/2/0 Project: DevLPT Default Value: 0x00000000 Access: R/W Size (in bits): 32					
Address: C6008h-C600Bh Name: SBI Control and Status ShortName: SBI_CTL_STAT Power: Always on Reset: PLTRST#					
DWord	Bit	Description			
0	31:17	Reserved			
		Format:	MBZ		
	16	Reserved			
		Project:	DevLPT:LP		
		Format:	MBZ		
	16	Destination ID Select			
		Project:	DevLPT:H		
This field selects between the two endpoints accessible by display.					
Value Name Description					
0b	iCLK	Addressed endpoint is iCLK, ID = 0xED			
1b	mPHY	Addressed endpoint is mPHY, ID = 0xD6			
15:8	Opcode				
	This is the opcode sent in the sideband message.				
	Value Name Description				
	02h	IORD	IO Read - use for mPHYIP access.		
	03h	IOWR	IO Write - use for mPHYIP access.		
	06h	CRRD	Read Private Control Register - use for iCLKIP access		
7:3	CRWr				
	07h	CRWR	Write Private Control Register - use for iCLKIP access		
	Others	Reserved	Reserved		
7:3	Reserved				
		Format:	MBZ		

SBI_CTL_STAT																
	2:1	<p>Response Status</p> <table border="1"> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>This field gives the response status from hardware for the previously completed transaction. The value is only meaningful when the status bit Busy is 0b.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>00b</td><td>Successful</td><td>Previous transaction was successful</td></tr> <tr> <td>01b</td><td>Unsuccessful</td><td>Previous transaction was unsuccessful or not supported</td></tr> <tr> <td>Others</td><td>Reserved</td><td>Reserved</td></tr> </tbody> </table>	Access:	RO	Value	Name	Description	00b	Successful	Previous transaction was successful	01b	Unsuccessful	Previous transaction was unsuccessful or not supported	Others	Reserved	Reserved
Access:	RO															
Value	Name	Description														
00b	Successful	Previous transaction was successful														
01b	Unsuccessful	Previous transaction was unsuccessful or not supported														
Others	Reserved	Reserved														
	0	<p>Busy</p> <table border="1"> <tr> <td>Access:</td><td>Write/Read Status</td></tr> </table> <p>Software sets this bit to trigger an sideband access using the current contents of registers SBI_ADDR, SBI_DATA, and SBI_CTL_STAT. Software must not change the contents of these registers while this BUSY bit is set. Access on the sideband is always handled by the hardware as a non-posted transaction. Hardware updates this bit to reflect the status of the previous transaction, keeping it at the Busy state while the transaction is in progress and clearing it when the transaction completes. Software must wait for this bit to clear to Ready prior to starting a new transaction.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Ready</td><td>The Display sideband interface is read for a new transaction</td></tr> <tr> <td>1b</td><td>Busy</td><td>The Display sideband interface is busy with the previous transaction.</td></tr> </tbody> </table>	Access:	Write/Read Status	Value	Name	Description	0b	Ready	The Display sideband interface is read for a new transaction	1b	Busy	The Display sideband interface is busy with the previous transaction.			
Access:	Write/Read Status															
Value	Name	Description														
0b	Ready	The Display sideband interface is read for a new transaction														
1b	Busy	The Display sideband interface is busy with the previous transaction.														

SBI_DATA

SBI_DATA		
Register Space: MMIO: 0/2/0 Project: DevLPT Default Value: 0x00000000 Access: Write/Read Status Size (in bits): 32		
Address: C6004h-C6007h Name: SBI Data ShortName: SBI_DATA Power: Always on Reset: PLTRST#		
DWord	Bit	Description
0	31:0	Data Register data associated with the addressed register. With a write on the Sideband interface, the content of this register is delivered to the addressed register when the Sideband access is triggered. With a read on the Sideband interface, the hardware updates the content of this register with the return value of the addressed register upon read completion of the triggered Sideband access. The read value is only meaningful when the status bit SBI_CTL_STAT Busy is 0b (Ready).

SBLC_PWM_CTL1

SBLC_PWM_CTL1											
Register Space: MMIO: 0/2/0 Project: DevLPT Default Value: 0x00000000 Access: R/W Size (in bits): 32											
Address: C8250h-C8253h Name: South BLM Control 1 ShortName: SBLC_PWM_CTL1 Power: Always on Reset: soft											
DWord	Bit	Description									
0	31	PWM PCH Enable This bit enables the PWM counter logic in the PCH. Disabled PWM will drive 0, which can be inverted to 1 with the polarity bit. <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Disable</td><td>PCH PWM disabled</td></tr> <tr> <td>1b</td><td>Enable</td><td>PCH PWM enabled</td></tr> </tbody> </table> Restriction Program the frequency and duty cycle before enabling PWM. The PWM PCH Override Enable must be set when using a CPU that does not control the PCH display PWM duty cycle, such as Broadwell.	Value	Name	Description	0b	Disable	PCH PWM disabled	1b	Enable	PCH PWM enabled
Value	Name	Description									
0b	Disable	PCH PWM disabled									
1b	Enable	PCH PWM enabled									
PWM PCH Override Enable This bit enables the duty cycle to be controlled through the SBLC_PWM_CTL2 Backlight Duty Cycle Override value, instead of being controlled by the CPU display. <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Disable</td><td>Override disabled (CPU display controls PWM duty cycle)</td></tr> <tr> <td>1b</td><td>Enable</td><td>Override enabled (Override register value controls PWM duty cycle)</td></tr> </tbody> </table> Restriction The PWM PCH Override Enable must be set when using a CPU that does not control the PCH display PWM duty cycle, such as Broadwell.	Value	Name	Description	0b	Disable	Override disabled (CPU display controls PWM duty cycle)	1b	Enable	Override enabled (Override register value controls PWM duty cycle)		
Value	Name	Description									
0b	Disable	Override disabled (CPU display controls PWM duty cycle)									
1b	Enable	Override enabled (Override register value controls PWM duty cycle)									
Backlight Polarity This field controls the polarity of the PWM signal. <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>High</td><td>Active High</td></tr> <tr> <td>1b</td><td>Low</td><td>Active Low</td></tr> </tbody> </table>	Value	Name	Description	0b	High	Active High	1b	Low	Active Low		
Value	Name	Description									
0b	High	Active High									
1b	Low	Active Low									

SBLC_PWM_CTL1

	28:0	Reserved	
		Format:	MBZ

SBLC_PWM_CTL2

SBLC_PWM_CTL2			
Register Space: MMIO: 0/2/0 Project: DevLPT Default Value: 0x00000000 Access: R/W Size (in bits): 32			
Address: C8254h-C8257h Name: South BLM Control 2 ShortName: SBLC_PWM_CTL2 Power: Always on Reset: soft			
DWord	Bit	Description	
0	31:16	Backlight Modulation Frequency	
		Description	Project
		This field determines the number of time base events in total for a complete cycle of modulated backlight control. This field is normally set once during initialization based on the frequency of the clock that is being used and the desired PWM frequency. This value represents the period of the PWM stream in clock periods multiplied by 128 (default increment) or 16 (alternate increment selected in 0xC2004 bit 5).	
		PWM clock is 135 MHz, non-spread, 100ppm	DevLPT:H
		PWM clock is 24 MHz, non-spread, <100ppm	DevLPT:LP
	15:0	Backlight Duty Cycle Override	This value overrides the CPU control of PWM duty cycle when the PWM PCH Override Enable bit is set. This field determines the number of time base events for the active portion of the PWM backlight control. This should never be larger than the frequency field. A value of zero will turn the backlight off. A value equal to the backlight modulation frequency field will be full on. When written, the new value will take affect at the end of the current PWM cycle. This value represents the active time of the PWM stream in clock periods multiplied by 128 (default increment) or 16 (alternate increment selected in 0xC2004 bit 5).

SCRATCH1

SCRATCH1 - SCRATCH1

Register Space:	MMIO: 0/2/0
Project:	BDW 0x00000001 [BDW:GT2:G, BDW:GT2:H, BDW:GT3:H, BDW:GT3E]
Size (in bits):	64
Address:	0B11Ch

DWord	Bit	Description
0 Project: BDW	31:5	SCRATCH
		Project: BDW
		Access: R/W
	4	Non coherent pm flush
		Project: BDW
		Access: R/W
		0:(default) When PM flush is sent to L3, LSQC will generate Query to flush coherent and Non coherent Lines (DC/L3 ways) from L3. 1: When PM flush is sent to L3, LSQC will generate Query to flush only the Coherent Lines (DC/L3 ways) from L3. lbcf_csr_lsqc_flush_nc_on_pm_flush_dis
3:2	SCRATCHN	
		Project: BDW
		Access: R/W
1	LSLM Last credit fix	
		Project: BDW
		Access: R/W
		0:(default) The last read return credit is always given to SLM. 1: The last read return credit is given to SLM when SLM is enabled. The last read return credit is given to Non-SLM when SLM is disabled. lbcf_csr_lslm_lastcreditfix_disable
	0	Reserved

SCRATCH for LNCUnit

SCRATCH_LNCF1 - SCRATCH for LNCUnit								
DWord	Bit	Description						
0	31:3	SCRATCH register for LNCUnit <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table>	Project:	BDW	Access:	R/W		
Project:	BDW							
Access:	R/W							
	2	Memory fill delay <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Incf_csr_Ini_gt2_memfill_dis. 0:mem fills gt2 latency will be 1 . 1:mem fill gt2 latency will be same as gt3.</p>	Access:	R/W				
Access:	R/W							
	1	flush start delay <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Incf_csr_Ini_disable_flush_start_delay. 0:Flush processing in LNUnit starts one clock after receiving the flush command default. 1:Flush processing in LNUnit starts in the same clock in which flush command is received.</p>	Access:	R/W				
Access:	R/W							
	0	Non-IA coherent atomics enable <table border="1"> <tr> <td>Default Value:</td><td>1b</td></tr> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>0: atomics in GT1 (). 1: atomics in L3 (non-IA atomic) (Default). Output signal from LNCF unit Incf_csr_Ini_glblatmcs_I3. Value for this bit should be same as lbcf_csr_lsqc_glblatmcs_I3 b118[22]. Value of this bit should be same as LBCF register bit 0xb11c[8]. Adding Xbuf 8 MCP.</p>	Default Value:	1b	Project:	BDW	Access:	R/W
Default Value:	1b							
Project:	BDW							
Access:	R/W							

Scratch Register 0

SCRATCH0 - Scratch Register 0		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A198h	
DWord	Bit	Description
0	31:0	Scratch Register 0 Access: R/W Register bits that have no connection to design.

Scratch Register 1

SCRATCH1 - ScratchRegister1		
DWord	Bit	Description
0	31:0	Scratch Register 1 Access: R/W Register bits that have no connection to design.

Second Buffer Size

SBS - Second Buffer Size				
DWord	Bit	Description		
0	31:16	<p>Second Virtual Buffer Base</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Second Virtual Buffer Base (SVBB0). Second Virtual Buffer Base: Programmed by driver to allocate a memory space for performance data storage. The buffer size should be aligned to the size of the memory allocated so it naturally aligns to the base (i.e. for 128KB bit[16]=0, 256KB bit[17:16]=0, 512KB bit[18:16]=0). Signal - lpconf_lpfc_virtual_base1 [31:16].</p>	Access:	R/W
Access:	R/W			
15:12	<p>Second Buffer Size 0</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Second Buffer Size: Determines the allowed buffer size for performance data storage. 0000b: 64KB. 0001b: 128KB. 0010b: 256KB. 0011b: 512KB. ... 1111b: 2GB. Signal - lpconf_lpfc_buffer_size1 [3:0].</p>	Access:	R/W	
Access:	R/W			
11:0	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>Reserved.</p>	Access:	RO	
Access:	RO			

Second Level Batch Buffer Head Pointer Preemption Register

SBB_PREEMPT_ADDR - Second Level Batch Buffer Head Pointer Preemption Register

Register Space:	MMIO: 0/2/0
Project:	BDW
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Trusted Type:	1
Address:	0213Ch-0213Fh
Name:	Second Level Batch Buffer Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_RCSUNIT
Address:	1213Ch-1213Fh
Name:	Second Level Batch Buffer Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_VCSUNIT0
Address:	1A13Ch-1A13Fh
Name:	Second Level Batch Buffer Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_VECSUNIT
Address:	1C13Ch-1C13Fh
Name:	Second Level Batch Buffer Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_VCSUNIT1
Address:	2213Ch-2213Fh
Name:	Second Level Batch Buffer Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_BCSUNIT

Description

This register gets updated with the DWord-aligned graphics memory address of the PREEMPTABLE command in the second level batch buffer on which preemption has occurred.

This register value should be looked at only when the preemption has occurred in the second level batch buffer. This is indicated by "Ring/Batch Indicator" in "RING_BUFFER_HEAD_PREEMPT_REG". This register value retains its previous value and doesn't change when the preemption occurs on a preemptable command in ring buffer or in batch buffer.

Preemption is triggered by valid UH PTR in ring buffer mode of scheduling and by a pending execlist in Exec-List mode of scheduling.

This is a global register and context save/restored as part of power context image.

Preemptable Commands	Source
MI_ARB_CHECK	RenderCS
3D_PRIMITIVE	

SBB_PREEMPT_ADDR - Second Level Batch Buffer Head Pointer Preemption Register

GPGPU_WALKER	
MEDIA_STATE_FLUSH	
PIPE_CONTROL (Only in GPGPU mode of pipeline selection)	
MI_ATOMIC (Post Sync Operation set in GPGPU mode of pipeline selection)	
MI_SEMAPHORE_SIGNAL (Post Sync Operation set in GPGPU mode of pipeline selection)	

Programming Notes

Programming Restriction: This register should NEVER be programmed by driver, this is for HW internal use only.

DWord	Bit	Description		
0	31:2	<p>Second Level Batch Buffer Head Pointer</p> <table border="1"> <tr> <td>Format:</td> <td>GraphicsAddress[31:2]</td> </tr> </table> <p>This field specifies the DWord-aligned Graphics Memory Address of the PREEMPTABLE command in a batch buffer where the Preemption has occurred.</p>	Format:	GraphicsAddress[31:2]
Format:	GraphicsAddress[31:2]			
1:0	<p>Reserved</p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ	
Format:	MBZ			

Second Level Batch Buffer Head Pointer Register

SBB_ADDR - Second Level Batch Buffer Head Pointer Register

Register Space:	MMIO: 0/2/0			
Project:	BDW			
Source:	CommandStreamer			
Default Value:	0x00000000			
Access:	RO			
Size (in bits):	32			
Address:	02114h-02117h			
Name:	Second Level Batch Buffer Head Pointer Register			
ShortName:	SBB_ADDR_RCSUNIT			
Address:	12114h-12117h			
Name:	Second Level Batch Buffer Head Pointer Register			
ShortName:	SBB_ADDR_VCSUNIT0			
Address:	1A114h-1A117h			
Name:	Second Level Batch Buffer Head Pointer Register			
ShortName:	SBB_ADDR_VECSUNIT			
Address:	1C114h-1C117h			
Name:	Second Level Batch Buffer Head Pointer Register			
ShortName:	SBB_ADDR_VCSUNIT1			
Address:	22114h-22117h			
Name:	Second Level Batch Buffer Head Pointer Register			
ShortName:	SBB_ADDR_BCSUNIT			
This register contains the current DWord Graphics Memory Address of the last-initiated batch buffer.				
Programming Notes				
This register should NEVER be programmed by driver, this is for HW internal use only. This register should not be written by software. These fields should only get written by a context restore. Software should always set these fields via the MI_BATCH_BUFFER_START command when initiating a batch buffer. This register is saved and restored with context.				
DWord	Bit	Description		
0	31:2	<p>Second Level Batch Buffer Head Pointer</p> <table border="1"> <tr> <td>Format:</td><td>GraphicsAddress[31:2]</td></tr> </table> <p>This field specifies the DWord-aligned Graphics Memory Address where the last initiated Second Level Batch Buffer is currently fetching commands. This field is meaningful only when Valid field is set to "1".</p>	Format:	GraphicsAddress[31:2]
Format:	GraphicsAddress[31:2]			

SBB_ADDR - Second Level Batch Buffer Head Pointer Register

	1	Reserved	Format:	MBZ
	0	Valid	Format:	U1
Value	Name	Description	Project	
0h	Invalid [Default]	Second Level Batch buffer Invalid	BDW	
1h	Valid	Second Batch buffer Valid.	BDW	

Second Level Batch Buffer State Register

SBB_STATE - Second Level Batch Buffer State Register

Register Space:	MMIO: 0/2/0
Project:	BDW
Source:	RenderCS
Default Value:	0x00000000 [BDW]
Access:	R/W
Size (in bits):	32

Address: 02118h

This register contains the attributes of the second level batch buffer initiated from the batch Buffer.

This register should not be written by software. These fields should only get written by a context restore. Software should always set these fields via the MI_BATCH_BUFFER_START command when initiating a batch buffer. This register is saved and restored with context.

DWord	Bit	Description	
0	31:9	Reserved	
		Format:	MBZ
	8	Reserved	
		Project:	BDW
		Format:	MBZ
	7	Resource Streamer Enable	
		Format:	U1
		When this bit is set, the Resource Streamer will execute the batch buffer. When this bit is clear the Resource Streamer will not execute the batch buffer.	
	6	Reserved	
		Project:	BDW
		Format:	MBZ
	5	Address Space Indicator	
		Project:	BDW
		Note: This field reflects the effective address space indicator security level and may not be the same as the Address Space Indicator written using MI_BATCH_BUFFER_START.	
Value	Name	Description	
0h	GGTT [Default]	This second level batch buffer is located in GGTT memory and is privileged	
1h	PPGTT	This second level batch buffer is located in PPGTT memory and is non-privileged.	

SBB_STATE - Second Level Batch Buffer State Register

	4	Reserved	
		Project:	BDW
		Format:	MBZ
	3:0	Reserved	
		Format:	MBZ

Second Level Batch Buffer Upper Head Pointer Preemption Register

SBB_PREEMPT_ADDR_UDW - Second Level Batch Buffer Upper Head Pointer Preemption Register

Register Space:	MMIO: 0/2/0			
Project:	BDW			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Address:	02138h-0213Bh			
Name:	Second Level Batch Buffer Upper Head Pointer Preemption Register			
ShortName:	SBB_PREEMPT_ADDR_UDW_RCSUNIT			
Address:	12138h-1213Bh			
Name:	Second Level Batch Buffer Upper Head Pointer Preemption Register			
ShortName:	SBB_PREEMPT_ADDR_UDW_VCSUNIT0			
Address:	1A138h-1A13Bh			
Name:	Second Level Batch Buffer Upper Head Pointer Preemption Register			
ShortName:	SBB_PREEMPT_ADDR_UDW_VECSUNIT			
Address:	1C138h-1C13Bh			
Name:	Second Level Batch Buffer Upper Head Pointer Preemption Register			
ShortName:	SBB_PREEMPT_ADDR_UDW_VCSUNIT1			
Address:	22138h-2213Bh			
Name:	Second Level Batch Buffer Upper Head Pointer Preemption Register			
ShortName:	SBB_PREEMPT_ADDR_UDW_BCSUNIT			
This register contains the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space of the last preempted second level batch buffer. This register follows the same rules as the SBB_PREEMPT_ADDR register.				
Programming Notes				
Programming Restriction: This register should NEVER be programmed by driver, this is for HW internal use only.				
DWord	Bit	Description		
0	31:16	Reserved <table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ
	Format:	MBZ		
15:0	Second Level Batch Buffer Head Pointer Upper DWORD <table border="1"> <tr> <td>Format:</td><td>GraphicsAddress[47:32]</td></tr> </table> <p>This field specifies the 4GB aligned base address of gfx 4GB virtual address space of the last preempted second level batch buffer.</p>	Format:	GraphicsAddress[47:32]	
Format:	GraphicsAddress[47:32]			

Second Level Batch Buffer Upper Head Pointer Register

SBB_ADDR_UDW - Second Level Batch Buffer Upper Head Pointer Register

Register Space:	MMIO: 0/2/0			
Project:	BDW			
Default Value:	0x00000000			
Access:	RO			
Size (in bits):	32			
Address:	0211Ch-0211Fh			
Name:	Second Level Batch Buffer Upper Head Pointer Register			
ShortName:	SBB_ADDR_UDW_RCSUNIT			
Address:	1211Ch-1211Fh			
Name:	Second Level Batch Buffer Upper Head Pointer Register			
ShortName:	SBB_ADDR_UDW_VCSUNIT0			
Address:	1A11Ch-1A11Fh			
Name:	Second Level Batch Buffer Upper Head Pointer Register			
ShortName:	SBB_ADDR_UDW_VECSUNIT			
Address:	1C11Ch-1C11Fh			
Name:	Second Level Batch Buffer Upper Head Pointer Register			
ShortName:	SBB_ADDR_UDW_VCSUNIT1			
Address:	2211Ch-2211Fh			
Name:	Second Level Batch Buffer Upper Head Pointer Register			
ShortName:	SBB_ADDR_UDW_BCSUNIT			
This register contains the current Upper DWord of Graphics Memory Address of the last-initiated batch buffer.				
Programming Restriction: This register should NEVER be programmed by driver. This is for HW internal use only.				
DWord	Bit	Description		
0	31:16	Reserved <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ
	Format:	MBZ		
15:0	Batch Buffer Head Pointer Upper DWORD <table border="1"> <tr> <td>Format:</td> <td>GraphicsAddress[47:32]</td> </tr> </table> <p>This field specifies the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space where the last initiated Batch Buffer is currently fetching commands. If no batch buffer is currently active, the Valid bit in BB_ADDR will be 0 and this field is meaningless.</p>	Format:	GraphicsAddress[47:32]	
Format:	GraphicsAddress[47:32]			

Semaphore Polling Interval on Wait

SEMA_WAIT_POLL - Semaphore Polling Interval on Wait				
Register Space:	MMIO: 0/2/0			
Project:	BDW			
Source:	RenderCS			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Address:	0224Ch			
<p>The SEMA_WAIT_POLL register contains Poll Interval field which specifies the minimum number of microseconds allowed for command streamer to wait before re-fetching the data from the address mentioned in the MI_SEMAPHORE_WAIT command on WAIT Mode set to POLL until the condition is satisfied while the context is not switched out.</p> <p>When a value of 0 is written the poll interval will be equal to the memory latency of the read completion.</p>				
DWord	Bit	Description		
0	31:21	Reserved <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Format:</td><td style="padding: 2px;">MBZ</td></tr> </table>	Format:	MBZ
Format:	MBZ			
20:0	Poll Interval Minimum number of micro-seconds allowed			

SERR_INT

SERR_INT											
Register Space:	MMIO: 0/2/0										
Project:	DevLPT										
Default Value:	0x00000000										
Access:	R/WC										
Size (in bits):	32										
Address:	C4040h-C4043h										
Name:	South Error Interrupts										
ShortName:	SERR_INT										
Power:	Always on										
Reset:	soft										
These are sticky bits, cleared by writing 1 to them. All the South Error Interrupt bits are ORed together to go to the South Display Engine ISR Error Interrupts Combined bit.											
DWord	Bit	Description									
0	31	<p>South Poison Status This bit is set upon receiving the poison message.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Not Detected</td><td>Event not detected</td></tr> <tr> <td>1b</td><td>Detected</td><td>Event detected</td></tr> </tbody> </table>	Value	Name	Description	0b	Not Detected	Event not detected	1b	Detected	Event detected
Value	Name	Description									
0b	Not Detected	Event not detected									
1b	Detected	Event detected									
	30:1	Reserved									
	0	<p>Reserved</p> <table border="1"> <tr> <td>Project:</td><td>DevLPT:H</td></tr> </table>	Project:	DevLPT:H							
Project:	DevLPT:H										
	0	<p>Reserved</p> <table border="1"> <tr> <td>Project:</td><td>DevLPT:LP</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	DevLPT:LP	Format:	MBZ					
Project:	DevLPT:LP										
Format:	MBZ										

SFUSE_STRAP

SFUSE_STRAP										
Register Space: MMIO: 0/2/0 Project: DevLPT Default Value: 0x00000000 Access: RO Size (in bits): 32										
Address: C2014h-C2017h Name: South Fuses and Straps ShortName: SFUSE_STRAP Power: Always on Reset: soft										
DWord	Bit	Description								
0	31:8	Reserved								
	7	Internal Display Capability Disable This bit indicates whether the internal display capability is disabled. When disabled, PCH display hardware will prevent all PCH display functionality and put clocks inside the display partition into their lowest power state. The CPU display will not work due to GMBUS, DP AUX, panel power sequencing, and hot plugs being disabled. Must use external graphics for display. <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Enable</td></tr> <tr> <td>1b</td><td>Disable</td></tr> </tbody> </table>	Value	Name	0b	Enable	1b	Disable		
Value	Name									
0b	Enable									
1b	Disable									
	6	CRT DAC Capability Disable <table border="1"> <tr> <td>Project:</td><td>DevLPT:H</td></tr> </table> This bit indicates whether the CRT DAC (VGA port) display capability is disabled. When disabled, PCH display hardware will prevent the CRT DAC (VGA port) DAC_CTL enable register bit from being set to 1b, force pcdclk to come from raw clock, and force the pixel clock to be gated off. Other ports on the CPU display will continue to work. <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Enable</td></tr> <tr> <td>1b</td><td>Disable</td></tr> </tbody> </table>	Project:	DevLPT:H	Value	Name	0b	Enable	1b	Disable
Project:	DevLPT:H									
Value	Name									
0b	Enable									
1b	Disable									
	6	Reserved								
	5	Reserved								
		Format: MBZ								

SFUSE_STRAP

SFUSE_STRAP		
4	Lane Reversal Strap	
	Project:	DevLPT:H
	This bit indicates the state of the DMI/FDI lane reversal strap.	
4	Reserved	
	Project:	DevLPT:LP
3	Reserved	
	Format:	MBZ
2	Digital Port B Present Strap	
	This bit indicates the state of the digital port B present strap. The strap is set if DDPB_CTRLDATA pin is 1b at rising edge of PCH_PWROK.	
1	Digital Port C Present Strap	
	This bit indicates the state of the digital port C present strap. The strap is set if DDPC_CTRLDATA pin is 1b at rising edge of PCH_PWROK.	
0	Reserved	
	Project:	DevLPT:LP
0	Digital Port D Present Strap	
	Project:	DevLPT:H
	This bit indicates the state of the digital port D present strap. The strap is set if DDPD_CTRLDATA pin is 1b at rising edge of PCH_PWROK.	
	There is no port D present strap on LPT:LP or WPT.	

SHOTPLUG_CTL

SHOTPLUG_CTL							
Register Space: MMIO: 0/2/0 Project: DevLPT Default Value: 0x00000000 Access: R/W Size (in bits): 32							
Address: C4030h-C4033h Name: South Hot Plug Control ShortName: SHOTPLUG_CTL Power: Always on Reset: soft							
Description		Project					
The DDI-A HPD Input Enable is found in the North Display Engine registers.		DevLPT:H					
DWord	Bit	Description					
0	31:29	Reserved <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Format:</td><td style="width: 50%;">MBZ</td></tr> </table>	Format:	MBZ			
Format:	MBZ						
28	DDI A HPD Input Enable <p>This field enables the hot plug detection input on the PCH for port A. This only applies to systems that have the CPU and PCH in the same package, where the DDI A HPD input is connected to the PCH and the HPD must be enabled in both the North Display Engine Registers HOTPLUG_CTL and the South Display Engine Registers SHOTPLUG_CTL. The HPD status is found in North Display Engine Registers HOTPLUG_CTL.</p> <p>On systems that have the CPU and PCH in separate packages, the DDI A HPD input is connected to the CPU, and the DDI A HPD input must be enabled in only the North Display Engine Registers HOTPLUG_CTL.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%;">Value</th><th style="width: 50%;">Name</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Disable</td></tr> <tr> <td>1b</td><td>Enable</td></tr> </tbody> </table>	Value	Name	0b	Disable	1b	Enable
Value	Name						
0b	Disable						
1b	Enable						
27:21	Reserved <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Format:</td><td style="width: 50%;">MBZ</td></tr> </table>	Format:	MBZ				
Format:	MBZ						

SHOTPLUG_CTL														
20	DDI D HPD Input Enable Controls the state of the HPD buffer for the digital port D.													
	<table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Disable</td></tr> <tr> <td>1b</td><td>Enable</td></tr> </tbody> </table>	Value	Name	0b	Disable	1b	Enable							
Value	Name													
0b	Disable													
1b	Enable													
	Restriction													
	The DDI D HPD is not connected on some SKUs.													
19:18	Reserved	Format: MBZ												
17:16	DDI D HPD Status Access: R/WC This field reflects the hot plug detect status on port D. This bit is used for either monitor hotplug/unplug or for notification of a sink event. When HPD input is enabled and either a long or short pulse is detected, one of these bits will set and the hotplug IIR will be set (if unmasked in the IMR). The hotplug ISR gives the live state of the HPD pin. Due to the possibility of back to back HPD events it is recommended that software filters the value read from the ISR. These are sticky bits, cleared by writing 1s to both of them. The short pulse duration is programmed in SHPD_PULSE_CNT.													
	<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>00b</td><td>No Detect</td><td>Digital port hot plug event not detected</td></tr> <tr> <td>X1b</td><td>Short Detect</td><td>Digital port short pulse hot plug event detected</td></tr> <tr> <td>1Xb</td><td>Long Detect</td><td>Digital port long pulse hot plug event detected</td></tr> </tbody> </table>	Value	Name	Description	00b	No Detect	Digital port hot plug event not detected	X1b	Short Detect	Digital port short pulse hot plug event detected	1Xb	Long Detect	Digital port long pulse hot plug event detected	
Value	Name	Description												
00b	No Detect	Digital port hot plug event not detected												
X1b	Short Detect	Digital port short pulse hot plug event detected												
1Xb	Long Detect	Digital port long pulse hot plug event detected												
	Restriction													
	The DDI D HPD is not connected on some SKUs..													
15:13	Reserved	Format: MBZ												
12	DDI C HPD Input Enable Controls the state of the HPD buffer for the digital port C.													
	<table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Disable</td></tr> <tr> <td>1b</td><td>Enable</td></tr> </tbody> </table>	Value	Name	0b	Disable	1b	Enable							
Value	Name													
0b	Disable													
1b	Enable													
11:10	Reserved	Format: MBZ												

SHOTPLUG_CTL														
9:8	DDI C HPD Status													
	Access:	R/WC												
<p>This field reflects the hot plug detect status on port C. This bit is used for either monitor hotplug/unplug or for notification of a sink event. When HPD input is enabled and either a long or short pulse is detected, one of these bits will set and the hotplug IIR will be set (if unmasked in the IMR). The hotplug ISR gives the live state of the HPD pin. Due to the possibility of back to back HPD events it is recommended that software filters the value read from the ISR. These are sticky bits, cleared by writing 1s to both of them. The short pulse duration is programmed in SHPD_PULSE_CNT.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>00b</td><td>No Detect</td><td>Digital port hot plug event not detected</td></tr> <tr> <td>X1b</td><td>Short Detect</td><td>Digital port short pulse hot plug event detected</td></tr> <tr> <td>1Xb</td><td>Long Detect</td><td>Digital port long pulse hot plug event detected</td></tr> </tbody> </table>			Value	Name	Description	00b	No Detect	Digital port hot plug event not detected	X1b	Short Detect	Digital port short pulse hot plug event detected	1Xb	Long Detect	Digital port long pulse hot plug event detected
Value	Name	Description												
00b	No Detect	Digital port hot plug event not detected												
X1b	Short Detect	Digital port short pulse hot plug event detected												
1Xb	Long Detect	Digital port long pulse hot plug event detected												
7:5	Reserved													
	Format:	MBZ												
4	DDI B HPD Input Enable													
<p>Controls the state of the HPD buffer for the digital port B.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Disable</td></tr> <tr> <td>1b</td><td>Enable</td></tr> </tbody> </table>			Value	Name	0b	Disable	1b	Enable						
Value	Name													
0b	Disable													
1b	Enable													
3:2	Reserved													
	Format:	MBZ												
1:0	DDI B HPD Status													
	Access:	R/WC												
<p>This field reflects the hot plug detect status on port B. This bit is used for either monitor hotplug/unplug or for notification of a sink event. When HPD input is enabled and either a long or short pulse is detected, one of these bits will set and the hotplug IIR will be set (if unmasked in the IMR). The hotplug ISR gives the live state of the HPD pin. Due to the possibility of back to back HPD events it is recommended that software filters the value read from the ISR. These are sticky bits, cleared by writing 1s to both of them. The short pulse duration is programmed in SHPD_PULSE_CNT.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>00b</td><td>No Detect</td><td>Digital port hot plug event not detected</td></tr> <tr> <td>X1b</td><td>Short Detect</td><td>Digital port short pulse hot plug event detected</td></tr> <tr> <td>1Xb</td><td>Long Detect</td><td>Digital port long pulse hot plug event detected</td></tr> </tbody> </table>			Value	Name	Description	00b	No Detect	Digital port hot plug event not detected	X1b	Short Detect	Digital port short pulse hot plug event detected	1Xb	Long Detect	Digital port long pulse hot plug event detected
Value	Name	Description												
00b	No Detect	Digital port hot plug event not detected												
X1b	Short Detect	Digital port short pulse hot plug event detected												
1Xb	Long Detect	Digital port long pulse hot plug event detected												

SHPD_FILTER_CNT

SHPD_FILTER_CNT

Register Space: MMIO: 0/2/0

Project: DevLPT

Default Value: 0x000001F2

Access: R/W

Size (in bits): 32

Address: C4038h-C403Bh

Name: South HPD Filter count

ShortName: SHPD_FILTER_CNT

Power: Always on

Reset: global

This register must be programmed properly before enabling DDI HPD detection. This register is on the chip reset, not the FLR reset.

DWord	Bit	Description				
0	31:17	Reserved	<table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ	
Format:	MBZ					
16:0	HPD Filter Count	<table border="1"> <tr> <td>Default Value:</td> <td>001F2h 500 microseconds</td> </tr> <tr> <td colspan="2">These bits define the duration of the filter for DDI HPD. The value is the number of microseconds minus 2. The default value of 0x001F2 = 500 microseconds</td></tr> </table>	Default Value:	001F2h 500 microseconds	These bits define the duration of the filter for DDI HPD. The value is the number of microseconds minus 2. The default value of 0x001F2 = 500 microseconds	
Default Value:	001F2h 500 microseconds					
These bits define the duration of the filter for DDI HPD. The value is the number of microseconds minus 2. The default value of 0x001F2 = 500 microseconds						

SHPD_PULSE_CNT

SHPD_PULSE_CNT		
Register Space:	MMIO: 0/2/0	
Project:	DevLPT	
Default Value:	0x000007CE	
Access:	R/W	
Size (in bits):	32	
Address:	C4034h-C4037h	
Name:	South HPD Pulse count DDI B	
ShortName:	SHPD_PULSE_CNT	
Power:	Always on	
Reset:	global	
Address:	C4044h-C4047h	
Name:	South HPD Pulse count DDI C	
ShortName:	SHPD_PULSE_CNT_C	
Valid Projects:	[DevLPT:LP]	
Power:	Always on	
Reset:	global	
Address:	C4048h-C404Bh	
Name:	South HPD Pulse count DDI D	
ShortName:	SHPD_PULSE_CNT_D	
Valid Projects:	[DevLPT:LP]	
Power:	Always on	
Reset:	global	
Description		Project
This register must be programmed properly before enabling DDI HPD detection. This register is on the chip reset, not the FLR reset.		
There is one instance of this register per DDI B, C, D.		DevLPT:LP
There is one instance of this register that applies to all DDI B, C, D.		DevLPT:H
DWord	Bit	Description
0	31:17	Reserved
		Format:
		MBZ

SHPD_PULSE_CNT		
	16:0	ShortPulse Count
Default Value:		007CEh 2000 microseconds
		Description
These bits define the duration of the pulse defined as a short pulse for DDI HPD. The value is the number of microseconds minus 2. The default value of 0x007CE = 2,000 microseconds (2 milliseconds) is for Displayport. For HDMI or DVI it should be programmed to 0x1869E = 100,000 microseconds (100 milliseconds).		
0xC2004 bits 10:8 allow pulse length to be overridden to 100ms for individual DDIs B/C/D		DevLPT:H

SINTERRUPT

SINTERRUPT															
Register Space: MMIO: 0/2/0 Project: DevLPT Default Value: 0x00000000, 0x00000000, 0x00000000, 0x00000000 Access: RO, R/W, R/WC, R/W Size (in bits): 128															
See the South Display Engine Interrupt Bit Definition Table to find the source event for each interrupt bit.															
DWord	Bit	Description													
0	31:0	ISR <table border="1"> <tr> <td>Access:</td><td>RO</td></tr> <tr> <td colspan="2">These are the Interrupt Status Register Bits. This field contains the non-persistent values of all interrupt status bits. The IMR selects which of these interrupt conditions are reported in the persistent IIR</td></tr> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> <tr> <td>0b</td><td>Condition Doesn't Exist</td><td>Interrupt condition currently does not exist</td></tr> <tr> <td>1b</td><td>Condition Exists</td><td>Interrupt condition currently exists</td></tr> </table> <p>Programming Notes</p> <p>Some inputs to this register are short pulses; therefore software should not expect to use this register to sample these conditions.</p>	Access:	RO	These are the Interrupt Status Register Bits. This field contains the non-persistent values of all interrupt status bits. The IMR selects which of these interrupt conditions are reported in the persistent IIR		Value	Name	Description	0b	Condition Doesn't Exist	Interrupt condition currently does not exist	1b	Condition Exists	Interrupt condition currently exists
Access:	RO														
These are the Interrupt Status Register Bits. This field contains the non-persistent values of all interrupt status bits. The IMR selects which of these interrupt conditions are reported in the persistent IIR															
Value	Name	Description													
0b	Condition Doesn't Exist	Interrupt condition currently does not exist													
1b	Condition Exists	Interrupt condition currently exists													
1	31:0	IMR <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> <tr> <td colspan="2">These are the Interrupt Mask Register Bits. This field contains a bit mask which selects which interrupt bits from the ISR are reported in the IIR.</td></tr> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> <tr> <td>0b</td><td>Not Masked</td><td>Interrupt not masked</td></tr> <tr> <td>1b</td><td>Masked</td><td>Interrupt masked</td></tr> </table>	Access:	R/W	These are the Interrupt Mask Register Bits. This field contains a bit mask which selects which interrupt bits from the ISR are reported in the IIR.		Value	Name	Description	0b	Not Masked	Interrupt not masked	1b	Masked	Interrupt masked
Access:	R/W														
These are the Interrupt Mask Register Bits. This field contains a bit mask which selects which interrupt bits from the ISR are reported in the IIR.															
Value	Name	Description													
0b	Not Masked	Interrupt not masked													
1b	Masked	Interrupt masked													

SINTERRUPT												
2	31:0	IIR										
Access:			R/WC									
<p>These are the Interrupt Identity Register Bits. This field holds the persistent values of the interrupt bits from the ISR which are unmasked by the IMR. If enabled by the IER, bits set in this register will generate a PCH display interrupt. Bits set in this register will remain set (persist) until the interrupt condition is cleared by writing a '1' to the appropriate bits. For each bit, the IIR can store a second pending interrupt if two or more of the same interrupt conditions occur before the first condition is cleared. Upon clearing the interrupt, the IIR bit and PCH display interrupt will momentarily go low, then return high to indicate there is another interrupt pending. Only the rising edge of the PCH Display interrupt will cause the North Display IIR (DEIIR) PCH Display Interrupt event bit to be set, so all PCH Display Interrupts, including back to back interrupts, must be cleared here before a new PCH Display Interrupt can cause the DEIIR to be set.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Condition Not Detected</td><td>Interrupt condition not detected</td></tr> <tr> <td>1b</td><td>Condition Detected</td><td>Interrupt condition detected</td></tr> </tbody> </table>				Value	Name	Description	0b	Condition Not Detected	Interrupt condition not detected	1b	Condition Detected	Interrupt condition detected
Value	Name	Description										
0b	Condition Not Detected	Interrupt condition not detected										
1b	Condition Detected	Interrupt condition detected										
3	31:0	IER										
Access:			R/W									
<p>These are the Interrupt Enable Register Bits. The field enables a PCH display interrupt to be generated whenever the corresponding bit in the IIR becomes set. A disabled interrupt will still appear in the IIR.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Disabled</td><td>Interrupt disabled</td></tr> <tr> <td>1b</td><td>Enabled</td><td>Interrupt enabled</td></tr> </tbody> </table>				Value	Name	Description	0b	Disabled	Interrupt disabled	1b	Enabled	Interrupt enabled
Value	Name	Description										
0b	Disabled	Interrupt disabled										
1b	Enabled	Interrupt enabled										

Slice Shutdown (aka Bypass Idle Hysteresis)

SLICESHUTDOWN - Slice Shutdown (aka Bypass Idle Hysteresis)				
Register Space:	MMIO: 0/2/0			
Project:	BDW			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0A190h			
DWord	Bit	Description		
0	31:3	Reserved <table border="1"> <tr> <td>Access:</td><td>RO</td></tr> </table>	Access:	RO
Access:	RO			
0	Bypass Idle Hysteresis Enable (aka Slice Shutdown) <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>1 - Bypass idle hysteresis requirements for making an RC wish. 0 - Honor idle hysteresis (default).</p>	Access:	R/W	
Access:	R/W			

Snoop control register

SNPCR - Snoop control register		
DWord	Bit	Description
0	31:23	Reserved Access: RO
	22:21	IDICOS Access: R/W 00b: default value. Resources for each setting is determined by uncore registers.
	20	Non Temporal Access: R/W Indication to uncore that - Request is of the type that should get minimal cache resources in the uncore.
	19:17	RSVD Access: RO
	16	Restrict Snoops to MSQC, no forwarding to L3 Access: R/W 1'b0 - Snoops are not restricted. 1'b1 - Restrict snoops to MSQC and do not forward to Node snoop unit (L3). For BDW steppings including E0/G1, L3 coherency is not functional, for all the BDW steppings till G1, this bit needs to be programmed 1'b1 by Gfx Driver.
	15	Thread ID Access: R/W 1 bit Thread ID for GT.
	14	Force Invalidate Access: R/W Force Invalidate - Forces the invalidate flag to be set with snoop lookups all the time. 0: Normal invalidation (based on req) - Default. 1: Forced invalidation.

SNPCR - Snoop control register

		IDI Pend Timer					
	13:11	<table border="1"> <tr> <td>Default Value:</td><td>011b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>IDIpPEND timer - Time to wait before monitoring the sq_snpc_idipend signal. 000b => 0 clocks. 001b => 1 clock. 010b => 2 clocks. 011b => 4 clocks (default.) 100b => 8. 101b => 16. 110b => 32. 111b => 64.</p>	Default Value:	011b	Access:	R/W	
Default Value:	011b						
Access:	R/W						
	10:8	<table border="1"> <tr> <td>Default Value:</td><td>011b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Retry Limit - Number of times to retry before switching to the freeze mechanism. 000b => Always freeze (first shot). 001b => 1 retry. 010b => 2 retry. 011b => 4 retry (default). 100b => 8 retry. 101b => 16 retry. 110b => 32 retry. 111b => infinite (no freeze).</p>	Default Value:	011b	Access:	R/W	
Default Value:	011b						
Access:	R/W						
	7:3	<table border="1"> <tr> <td>Default Value:</td><td>01000b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Retry Timer - Time between receiving a reject from SQ and repeating the monitor sequence. 00000b => 0 clocks. 00001b => 1 clock. 00010b => 2 clocks. 00011b => 3 clocks. 00111b => 7 clocks. 01000b => 8 clocks (Default). ... 11111b => 32 clocks.</p>		Default Value:	01000b	Access:	R/W
Default Value:	01000b						
Access:	R/W						

SNPCR - Snoop control register

	2:0	MLCSQ Timer	
		Access:	R/W
<p>MLC-SQ Timer - Time between doing an MLC lookup and SQ lookup.</p> <p>000b => 0 clocks (default).</p> <p>001b => 1 clock.</p> <p>010b => 2 clocks.</p> <p>011b => 4 clocks.</p> <p>100b => 8.</p> <p>101b => 16.</p> <p>110b => 32.</p> <p>111b => 64.</p>			

Software SCI

SWSCI_0_2_0_PCI - Software SCI						
DWord	Bit	Description				
0	15	<p>SMI or SCI event select</p> <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W Once</td> </tr> </table> <p>0 = SMI (default) 1 = SCI If selected event source is SMI, SMI trigger and associated scratch bits accesses are performed via SWSMI register. If SCI event source is selected, the rest of the bits in this register provide SCI trigger capability and associated SW scratch pad area.</p>	Default Value:	0b	Access:	R/W Once
Default Value:	0b					
Access:	R/W Once					
	14:1	<p>Software scratch bits</p> <table border="1"> <tr> <td>Default Value:</td> <td>000000000000000b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Read/write bits not used by hardware.</p>	Default Value:	000000000000000b	Access:	R/W
Default Value:	000000000000000b					
Access:	R/W					
	0	<p>Software SCI Event</p> <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>If SCI event is selected (SMISCISEL = 1), on a 0 to 1 transition of GSSCIE bit, a SCI message will be sent to cause the TCOSCI_STS bit in GPE0 register to be set to 1. Software must write a 0 to clear this bit.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					

Software SMI

SWSMI_0_2_0_PCI - Software SMI						
DWord	Bit	Description				
0	15:8	<p>Software Scratch Bits</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table>	Default Value:	00000000b	Access:	R/W
Default Value:	00000000b					
Access:	R/W					
7:1	<p>Software Flag</p> <table border="1"> <tr> <td>Default Value:</td> <td>0000000b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Used to indicate caller and SMI function desired, as well as return result.</p>	Default Value:	0000000b	Access:	R/W	
Default Value:	0000000b					
Access:	R/W					
0	<p>GMCH Software SMI Event</p> <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>When Set this bit will trigger an SMI. Software must write a "0" to clear this bit. SMI will be triggered only if SWSCI[SMISCISEL] is set to select SMI.</p>	Default Value:	0b	Access:	R/W	
Default Value:	0b					
Access:	R/W					

South Display Engine Interrupt Bit Definition

South Display Engine Interrupt Bit Definition						
DWord	Bit	Description				
0	31:28	<p>Reserved</p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ		
Format:	MBZ					
	27	<p>AUX Channel D This is an active high pulse on the AUX D done event</p>				
	26	<p>AUX Channel C This is an active high pulse on the AUX C done event</p>				
	25	<p>AUX Channel B This is an active high pulse on the AUX B done event</p>				
	24	<p>Reserved</p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ		
Format:	MBZ					
	23	<p>DisplayPort/HDMI/DVI D Hotplug The ISR is an active high level representing the Digital Port D hotplug line when the Digital Port D hotplug detect input is enabled. The unmasked IIR is set on either a short or long pulse detection status in the Digital Port Hot Plug Control Register.</p> <table border="1"> <thead> <tr> <th>Restriction</th> <th>Project</th> </tr> </thead> <tbody> <tr> <td>Restriction : The DDI D HPD pin is not connected in the package for LP parts and should not be used.</td> <td>DevLPT:LP</td> </tr> </tbody> </table>	Restriction	Project	Restriction : The DDI D HPD pin is not connected in the package for LP parts and should not be used.	DevLPT:LP
Restriction	Project					
Restriction : The DDI D HPD pin is not connected in the package for LP parts and should not be used.	DevLPT:LP					
	22	<p>DisplayPort/HDMI/DVI C Hotplug The ISR is an active high level representing the Digital Port C hotplug line when the Digital Port C hotplug detect input is enabled. The unmasked IIR is set on either a short or long pulse detection status in the Digital Port Hot Plug Control Register.</p>				

South Display Engine Interrupt Bit Definition		
	21	DisplayPort/HDMI/DVI B Hotplug The ISR is an active high level representing the Digital Port B hotplug line when the Digital Port B hotplug detect input is enabled. The unmasked IIR is set on either a short or long pulse detection status in the Digital Port Hot Plug Control Register.
	20	Reserved Format: MBZ
	19	CRT Hotplug Project: DevLPT:H The ISR is an active high level representing the ORed together blue and green channel detection status as of the last detection cycle. The unmasked IIR is set on the rising or falling edges of the blue or green channel detection status in the Analog Port CRT DAC Control Register.
	19	Reserved Project: DevLPT:LP Format: MBZ
	18	Reserved Format: MBZ
	17	Gmbus This is an active high pulse when any of the events unmasked events in GMBUS4 Interrupt Mask register occur.
	16	South Error Interrupts Combined This is an active high level while any of the South Error Interrupt bits are set.
	15	GTC PCH Interrupts Combined The ISR is an active high level while any of the GTC_PCH_IIR bits are set.
	14:1	Reserved Format: MBZ
	0	FDI RX Interrupts Combined A Project: DevLPT:H This is an active high level while any of the FDI_RX_ISR bits are set for transcoder A.
	0	Reserved Project: DevLPT:LP Format: MBZ

SPLL_CTL

SPLL_CTL								
DWord	Bit	Description						
0	31	<p>PLL Enable This bit will enable or disable the PLL.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disable</td> </tr> <tr> <td>1b</td> <td>Enable</td> </tr> </tbody> </table> <p>Restriction This field must not be changed while any port clock select is direct to this PLL.</p>	Value	Name	0b	Disable	1b	Enable
Value	Name							
0b	Disable							
1b	Enable							
	30	<p>Reserved Format: <input type="text"/> MBZ</p>						
	29:28	<p>Reference Select Select between PLL references.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>01b</td> <td>Muxed SSC</td> <td>CPU internal SSC when CPU Internal SSC is fused enabled, else the PCH SSC reference.</td> </tr> </tbody> </table> <p>Restriction This field must not be changed while this PLL is enabled.</p>	Value	Name	Description	01b	Muxed SSC	CPU internal SSC when CPU Internal SSC is fused enabled, else the PCH SSC reference.
Value	Name	Description						
01b	Muxed SSC	CPU internal SSC when CPU Internal SSC is fused enabled, else the PCH SSC reference.						

SPLL_CTL															
	27:26	Frequency Select Select between PLL frequencies.													
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>00b</td><td>810 MHz</td><td>810 MHz (DisplayPort 1.62 GHz bit clock)</td></tr> <tr> <td>01b</td><td>1350 MHz</td><td>1350 MHz (FDI and DisplayPort 2.7 GHz bit clock)</td></tr> <tr> <td>11b</td><td>Reserved</td><td>Reserved</td></tr> </tbody> </table>	Value	Name	Description	00b	810 MHz	810 MHz (DisplayPort 1.62 GHz bit clock)	01b	1350 MHz	1350 MHz (FDI and DisplayPort 2.7 GHz bit clock)	11b	Reserved	Reserved	
Value	Name	Description													
00b	810 MHz	810 MHz (DisplayPort 1.62 GHz bit clock)													
01b	1350 MHz	1350 MHz (FDI and DisplayPort 2.7 GHz bit clock)													
11b	Reserved	Reserved													
	25:0	Reserved													
		Format:	MBZ												

SPR_CTL

SPR_CTL												
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x00000000 Access: Double Buffered Size (in bits): 32 Double Buffer Update Point: Start of vertical blank or pipe not enabled; after armed Double Buffer Armed Write to SPR_SURF or sprite not enabled By:												
Address:	70280h-70283h											
Name:	Sprite A Control											
ShortName:	SPR_CTL_A											
Power:	Always on											
Reset:	soft											
Address:	71280h-71283h											
Name:	Sprite B Control											
ShortName:	SPR_CTL_B											
Power:	off/on											
Reset:	soft											
Address:	72280h-72283h											
Name:	Sprite C Control											
ShortName:	SPR_CTL_C											
Power:	off/on											
Reset:	soft											
DWord	Bit	Description										
0	31	Sprite Enable <table border="1"> <tr> <td>Format:</td><td>Enable</td></tr> <tr> <td colspan="2">When this bit is set, the sprite plane will generate pixels for display. When cleared to zero, sprite plane memory fetches cease and sprite output is transparent.</td></tr> <tr> <th>Value</th><th>Name</th></tr> <tr> <td>0b</td><td>Disable</td></tr> <tr> <td>1b</td><td>Enable</td></tr> </table>	Format:	Enable	When this bit is set, the sprite plane will generate pixels for display. When cleared to zero, sprite plane memory fetches cease and sprite output is transparent.		Value	Name	0b	Disable	1b	Enable
Format:	Enable											
When this bit is set, the sprite plane will generate pixels for display. When cleared to zero, sprite plane memory fetches cease and sprite output is transparent.												
Value	Name											
0b	Disable											
1b	Enable											

SPR_CTL

		Pipe Gamma Enable This bit enables pipe gamma correction for the sprite pixel data.																								
	30	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th><th style="text-align: center;">Name</th></tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td><td>Disable</td></tr> <tr> <td style="text-align: center;">1b</td><td>Enable</td></tr> </tbody> </table>	Value	Name	0b	Disable	1b	Enable																		
Value	Name																									
0b	Disable																									
1b	Enable																									
	29	Reserved																								
		Format: MBZ																								
	28	YUV Range Correction Disable Setting this bit disables the YUV range correction logic inside the sprite. The range correction logic is used to expand the compressed range YUV to full range YUV. The Y channel is expanded from the 8 bit +16 to +235 range to full range. The U and V channels are expanded from the 8 bit -112 to +112 range to full range. Extended range values will be preserved after the expansion. This bit has no effect on RGB source pixel formats since they automatically bypass range correction.																								
		<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th><th style="text-align: center;">Name</th></tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td><td>Enable</td></tr> <tr> <td style="text-align: center;">1b</td><td>Disable</td></tr> </tbody> </table>	Value	Name	0b	Enable	1b	Disable																		
Value	Name																									
0b	Enable																									
1b	Disable																									
	27:25	Source Pixel Format This field selects the source pixel format for the sprite plane. Before entering the blender, each source format is converted to the pipe pixel format. Alpha values are ignored. YUV 4:2:2 byte order is programmed separately. YUV 4:4:4 byte order is not programmable. RGB color order is programmed separately, except RGB XR_BIAS byte order is not programmable.																								
		<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th><th style="text-align: center;">Name</th><th style="text-align: center;">Description</th></tr> </thead> <tbody> <tr> <td style="text-align: center;">000b</td><td>YUV 16-bit 4:2:2</td><td>YUV 16-bit 4:2:2 packed</td></tr> <tr> <td style="text-align: center;">001b</td><td>RGB 32-bit 2:10:10:10</td><td>RGB 32-bit 2:10:10:10</td></tr> <tr> <td style="text-align: center;">010b</td><td>RGB 32-bit 8:8:8:8</td><td>RGB 32-bit 8:8:8:8</td></tr> <tr> <td style="text-align: center;">011b</td><td>RGB 64-bit 16:16:16:16</td><td>RGB 64-bit 16:16:16:16 Floating Point</td></tr> <tr> <td style="text-align: center;">100b</td><td>YUV 32-bit 4:4:4</td><td>YUV 32-bit 4:4:4 packed (8:8:8:8 MSB-X:Y:U:V)</td></tr> <tr> <td style="text-align: center;">101b</td><td>RGB 32-bit XR_BIAS 10:10:10</td><td>RGB 32-bit Extended Range Bias RGBX (2:10:10:10 MSB-X:B:G:R)</td></tr> <tr> <td style="text-align: center;">Others</td><td>Reserved</td><td>Reserved</td></tr> </tbody> </table>	Value	Name	Description	000b	YUV 16-bit 4:2:2	YUV 16-bit 4:2:2 packed	001b	RGB 32-bit 2:10:10:10	RGB 32-bit 2:10:10:10	010b	RGB 32-bit 8:8:8:8	RGB 32-bit 8:8:8:8	011b	RGB 64-bit 16:16:16:16	RGB 64-bit 16:16:16:16 Floating Point	100b	YUV 32-bit 4:4:4	YUV 32-bit 4:4:4 packed (8:8:8:8 MSB-X:Y:U:V)	101b	RGB 32-bit XR_BIAS 10:10:10	RGB 32-bit Extended Range Bias RGBX (2:10:10:10 MSB-X:B:G:R)	Others	Reserved	Reserved
Value	Name	Description																								
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011b	RGB 64-bit 16:16:16:16	RGB 64-bit 16:16:16:16 Floating Point																								
100b	YUV 32-bit 4:4:4	YUV 32-bit 4:4:4 packed (8:8:8:8 MSB-X:Y:U:V)																								
101b	RGB 32-bit XR_BIAS 10:10:10	RGB 32-bit Extended Range Bias RGBX (2:10:10:10 MSB-X:B:G:R)																								
Others	Reserved	Reserved																								
		Programming Notes																								
		When using YUV formats and the sprite internal CSC is disabled, the sprite output will default to not having a 1/2 offset on the U and V channels. The 1/2 offset can be preserved by setting register 420B0h (pipe A), 420B4h (pipe B), 420B8h (pipe C) bit 30 to 1b.																								

SPR_CTL

		Pipe CSC Enable This bit enables pipe color space conversion for the plane pixel data. This is separate from the color conversion logic within the sprite plane.									
	24	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center; background-color: #e0e0ff;">Value</th> <th style="text-align: center; background-color: #e0e0ff;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td><td>Disable</td></tr> <tr> <td style="text-align: center;">1b</td><td>Enable</td></tr> </tbody> </table>	Value	Name	0b	Disable	1b	Enable			
Value	Name										
0b	Disable										
1b	Enable										
	23	Reserved Format: MBZ									
	22	Sprite Source Key Enable This bit enables source color keying. Sprite pixel values that match (within range) the key will become transparent. Source key can not be enabled if destination key is enabled.									
		<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center; background-color: #e0e0ff;">Value</th> <th style="text-align: center; background-color: #e0e0ff;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td><td>Disable</td></tr> <tr> <td style="text-align: center;">1b</td><td>Enable</td></tr> </tbody> </table>	Value	Name	0b	Disable	1b	Enable			
Value	Name										
0b	Disable										
1b	Enable										
	21	Reserved Format: MBZ									
	20	RGB Color Order This field is used to select the color order when using RGB data formats, except RGB 32-bit XR_BIAS 10:10:10. For other formats, this field is ignored.									
		<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center; background-color: #e0e0ff;">Value</th> <th style="text-align: center; background-color: #e0e0ff;">Name</th> <th style="text-align: center; background-color: #e0e0ff;">Description</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td><td>BGRX</td><td>BGRX (MSB-X:R:G:B)</td></tr> <tr> <td style="text-align: center;">1b</td><td>RGBX</td><td>RGBX (MSB-X:B:G:R)</td></tr> </tbody> </table>	Value	Name	Description	0b	BGRX	BGRX (MSB-X:R:G:B)	1b	RGBX	RGBX (MSB-X:B:G:R)
Value	Name	Description									
0b	BGRX	BGRX (MSB-X:R:G:B)									
1b	RGBX	RGBX (MSB-X:B:G:R)									
	19	Sprite YUV to RGB CSC Dis This bit controls the sprite internal YUV to RGB color space conversion. RGB source pixel formats automatically bypass the sprite internal color space conversion.									
		<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center; background-color: #e0e0ff;">Value</th> <th style="text-align: center; background-color: #e0e0ff;">Name</th> <th style="text-align: center; background-color: #e0e0ff;">Description</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td><td>Enable</td><td>YUV pixel data goes through the sprite color conversion</td></tr> <tr> <td style="text-align: center;">1b</td><td>Disable</td><td>YUV pixel data bypasses the sprite color conversion</td></tr> </tbody> </table>	Value	Name	Description	0b	Enable	YUV pixel data goes through the sprite color conversion	1b	Disable	YUV pixel data bypasses the sprite color conversion
Value	Name	Description									
0b	Enable	YUV pixel data goes through the sprite color conversion									
1b	Disable	YUV pixel data bypasses the sprite color conversion									
	18	Sprite YUV to RGB CSC Format This bit specifies the source YUV format for the sprite internal YUV to RGB color space conversion operation. This field is ignored when source data is RGB.									
		<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center; background-color: #e0e0ff;">Value</th> <th style="text-align: center; background-color: #e0e0ff;">Name</th> <th style="text-align: center; background-color: #e0e0ff;">Description</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td><td>BT.601</td><td>ITU-R Recommendation BT.601</td></tr> <tr> <td style="text-align: center;">1b</td><td>BT.709</td><td>ITU-R Recommendation BT.709</td></tr> </tbody> </table>	Value	Name	Description	0b	BT.601	ITU-R Recommendation BT.601	1b	BT.709	ITU-R Recommendation BT.709
Value	Name	Description									
0b	BT.601	ITU-R Recommendation BT.601									
1b	BT.709	ITU-R Recommendation BT.709									

SPR_CTL

		YUV 422 Byte Order This field is used to select the byte order when using YUV 4:2:2 data formats. For other formats, this field is ignored.															
	17:16	<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>YUYV</td> <td>YUYV (8:8:8:8 MSB-V:Y2:U:Y1)</td> </tr> <tr> <td>01b</td> <td>UYVY</td> <td>UYVY (8:8:8:8 MSB-Y2:V:Y1:U)</td> </tr> <tr> <td>10b</td> <td>YVYU</td> <td>YVYU (8:8:8:8 MSB-U:Y2:V:Y1)</td> </tr> <tr> <td>11b</td> <td>VYUY</td> <td>VYUY (8:8:8:8 MSB-Y2:U:Y1:V)</td> </tr> </tbody> </table>	Value	Name	Description	00b	YUYV	YUYV (8:8:8:8 MSB-V:Y2:U:Y1)	01b	UYVY	UYVY (8:8:8:8 MSB-Y2:V:Y1:U)	10b	YVYU	YVYU (8:8:8:8 MSB-U:Y2:V:Y1)	11b	VYUY	VYUY (8:8:8:8 MSB-Y2:U:Y1:V)
Value	Name	Description															
00b	YUYV	YUYV (8:8:8:8 MSB-V:Y2:U:Y1)															
01b	UYVY	UYVY (8:8:8:8 MSB-Y2:V:Y1:U)															
10b	YVYU	YVYU (8:8:8:8 MSB-U:Y2:V:Y1)															
11b	VYUY	VYUY (8:8:8:8 MSB-Y2:U:Y1:V)															
	15	180 Display Rotation This mode causes the plane image to be rotated 180 degrees. In addition to setting this bit, adjust the plane position to match the physical orientation of the display. <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>No rotation</td> </tr> <tr> <td>1b</td> <td>180 degree rotation</td> </tr> </tbody> </table>	Value	Name	0b	No rotation	1b	180 degree rotation									
Value	Name																
0b	No rotation																
1b	180 degree rotation																
	14	Trickle Feed Enable <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Enable</td> </tr> <tr> <td>1b</td> <td>Disable</td> </tr> </tbody> </table> Restriction Do not program this field to 1b.	Value	Name	0b	Enable	1b	Disable									
Value	Name																
0b	Enable																
1b	Disable																
	13	Sprite Gamma Disable This bit controls sprite internal gamma correction. <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>1b</td> <td>Disable</td> </tr> <tr> <td>0b</td> <td>Enable</td> </tr> </tbody> </table>	Value	Name	1b	Disable	0b	Enable									
Value	Name																
1b	Disable																
0b	Enable																
	12:11	Reserved															
	10	Tiled Surface This bit indicates that the surface data is in tiled memory. The tile pitch is specified in bytes in the stride register. This bit may be updated through MMIO writes or through a command streamer initiated synchronous flip. <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Linear memory</td> </tr> <tr> <td>1b</td> <td>X-Tiled memory</td> </tr> </tbody> </table> Restriction Y tiling is not supported.	Value	Name	0b	Linear memory	1b	X-Tiled memory									
Value	Name																
0b	Linear memory																
1b	X-Tiled memory																

SPR_CTL																			
	9:8	Reserved																	
		Format:	MBZ																
	7:6	Stereo Surface Vblank Mask																	
		This field controls which vertical blank (left eye, right eye, or both) will be used for the plane surface address double-buffering during stereo 3D mode. This field is ignored when not in stereo 3D mode.																	
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>00b</td><td>Mask None</td><td>No masking. Both the left and right eye vertical blanks will be used.</td></tr> <tr> <td>01b</td><td>Mask Left</td><td>Mask the left eye vertical blank. Only the right eye vertical blank will be used.</td></tr> <tr> <td>10b</td><td>Mask Right</td><td>Mask the right eye vertical blank. Only the left eye vertical blank will be used.</td></tr> <tr> <td>Others</td><td>Reserved</td><td>Reserved.</td></tr> </tbody> </table>			Value	Name	Description	00b	Mask None	No masking. Both the left and right eye vertical blanks will be used.	01b	Mask Left	Mask the left eye vertical blank. Only the right eye vertical blank will be used.	10b	Mask Right	Mask the right eye vertical blank. Only the left eye vertical blank will be used.	Others	Reserved	Reserved.
Value	Name	Description																	
00b	Mask None	No masking. Both the left and right eye vertical blanks will be used.																	
01b	Mask Left	Mask the left eye vertical blank. Only the right eye vertical blank will be used.																	
10b	Mask Right	Mask the right eye vertical blank. Only the left eye vertical blank will be used.																	
Others	Reserved	Reserved.																	
	5:3	Reserved																	
		Format:	MBZ																
	2	Sprite Destination Key																	
		This bit enables the destination key function. When blending together sprite and primary planes, if the primary plane pixel matches the key value, then the sprite pixel is output, otherwise the primary pixel is output.																	
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Disable</td></tr> <tr> <td>1b</td><td>Enable</td></tr> </tbody> </table>			Value	Name	0b	Disable	1b	Enable									
Value	Name																		
0b	Disable																		
1b	Enable																		
		Restriction																	
		Destination Key can not be enabled if source key is enabled.																	
	1:0	Reserved																	
		Format:	MBZ																

SPR_GAMC

SPR_GAMC	
Register Space:	MMIO: 0/2/0
Project:	BDW
Default Value:	0x00000000, 0x04010040, 0x08020080, 0x0C0300C0, 0x10040100, 0x14050140, 0x18060180, 0x1C0701C0, 0x20080200, 0x24090240, 0x280A0280, 0x2C0B02C0, 0x300C0300, 0x340D0340, 0x380E0380, 0x3C0F03C0
Access:	R/W
Size (in bits):	512
Address:	70400h-7043Fh
Name:	Sprite A Gamma Correction
ShortName:	SPR_GAMC_A_*
Power:	Always on
Reset:	soft
Address:	71400h-7143Fh
Name:	Sprite B Gamma Correction
ShortName:	SPR_GAMC_B_*
Power:	off/on
Reset:	soft
Address:	72400h-7243Fh
Name:	Sprite C Gamma Correction
ShortName:	SPR_GAMC_C_*
Power:	off/on
Reset:	soft
<p>These registers are used to determine the characteristics of the gamma correction for the sprite pixel data pre-blending. Additional gamma correction can be done in the display pipe gamma if desired. The gamma correction curve is represented by specifying a set of gamma entry reference points spaced equally along the curve for values between -1 and 1. For extended values there is an extended gamma entry reference point at the maximum allowed input value. All input values are clamped to the greater than -3.0 and less than 3.0 range before the gamma calculation. * For input values greater than or equal to 0 and less than 1.0, the input value is used to linearly interpolate between two adjacent points of the first 17 gamma entries to create the result value. The first 16 entries are stored in SPR_GAMC with 10 bits per color in an unsigned 0.10 format with 0 integer and 10 fractional. The 17th entry is stored in the SPR_GAMC16 register with 11 bits per color in an unsigned 1.10 format with 1 integer and 10 fractional bits. * For input values greater than or equal to 1.0 and less than 3.0, the input value is used to linearly interpolate between the 17th and 18th gamma entries to create the result value. The 18th entry is stored in the SPR_GAMC17 register with 12 bits per color in an unsigned 2.10 format with 2 integer and 10 fractional bits. * For negative input values, gamma is mirrored along the X-axis, giving the same result as positive input values, except for a negative sign. When gamma input may be negative, the first gamma point should be programmed to a value of 0.0 in order to have a symmetric mirroring. Gamma correction can be enabled or disabled through the sprite control register. See Pipe Gamma for an example gamma curve diagram.</p>	

SPR_GAMC

Programming Notes

To program the gamma correction entries, calculate the desired gamma curve for inputs from 0 to 3.0. For inputs of 0 to 1.0, multiply the input value by 16 to find the gamma entry number, then store the desired gamma result in that entry. For inputs greater than 1.0 and less than or equal to 3.0, store the result for an input of 3.0 in the 18th gamma entry (SRP_GAMC17).

Restriction

The gamma curve must be flat or increasing, never decreasing. The gamma correction registers should only be updated when the sprite is off, otherwise screen artifacts may show temporarily.

DWord	Bit	Description	
0	31:30	Reserved	Format: MBZ
	29:20	Red	Default Value: 00 0000 0000b Format: U0.10
	19:10	Green	Default Value: 00 0000 0000b Format: U0.10
	9:0	Blue	Default Value: 00 0000 0000b Format: U0.10
1	31:30	Reserved	Format: MBZ
	29:20	Red	Default Value: 00 0100 0000b Format: U0.10
	19:10	Green	Default Value: 00 0100 0000b Format: U0.10
	9:0	Blue	Default Value: 00 0100 0000b Format: U0.10
2	31:30	Reserved	Format: MBZ
	29:20	Red	Default Value: 00 1000 0000b Format: U0.10

SPR_GAMC				
	19:10	Green		
		Default Value:	00 1000 0000b	
	9:0	Blue		
		Default Value:	00 1000 0000b	
	31:30	Reserved		
		Format:	MBZ	
	29:20	Red		
		Default Value:	00 1100 0000b	
	19:10	Green		
		Default Value:	00 1100 0000b	
	9:0	Blue		
		Default Value:	00 1100 0000b	
	31:30	Reserved		
		Format:	MBZ	
	29:20	Red		
		Default Value:	01 0000 0000b	
	19:10	Green		
		Default Value:	01 0000 0000b	
	9:0	Blue		
		Default Value:	01 0000 0000b	
	31:30	Reserved		
		Format:	MBZ	
	29:20	Red		
		Default Value:	01 0100 0000b	
	19:10	Green		
		Default Value:	01 0100 0000b	

SPR_GAMC			
	9:0	Blue	
		Default Value:	01 0100 0000b
		Format:	U0.10
6	31:30	Reserved	
		Format:	MBZ
	29:20	Red	
		Default Value:	01 1000 0000b
		Format:	U0.10
6	19:10	Green	
		Default Value:	01 1000 0000b
		Format:	U0.10
	9:0	Blue	
		Default Value:	01 1000 0000b
		Format:	U0.10
7	31:30	Reserved	
		Format:	MBZ
	29:20	Red	
		Default Value:	01 1100 0000b
		Format:	U0.10
7	19:10	Green	
		Default Value:	01 1100 0000b
		Format:	U0.10
	9:0	Blue	
		Default Value:	01 1100 0000b
		Format:	U0.10
8	31:30	Reserved	
		Format:	MBZ
	29:20	Red	
		Default Value:	10 0000 0000b
		Format:	U0.10
8	19:10	Green	
		Default Value:	10 0000 0000b
		Format:	U0.10
	9:0	Blue	
		Default Value:	10 0000 0000b
		Format:	U0.10

SPR_GAMC			
9	31:30	Reserved	Format: MBZ
		Red	Default Value: 10 0100 0000b
		Green	Format: U0.10
			Default Value: 10 0100 0000b
10	9:0	Blue	Format: U0.10
		Red	Default Value: 10 0100 0000b
			Format: U0.10
		Green	Default Value: 10 1000 0000b
11	19:10	Blue	Format: U0.10
			Default Value: 10 1000 0000b
		Red	Format: U0.10
		Green	Default Value: 10 1100 0000b
12	31:30	Blue	Format: U0.10
		Red	Default Value: 10 1100 0000b
			Format: U0.10
		Green	Default Value: 10 1100 0000b
12	9:0	Blue	Format: U0.10
		Red	Default Value: 10 1100 0000b
12	31:30	Green	Format: U0.10
		Blue	Default Value: 10 1100 0000b
12	9:0	Red	Format: U0.10
		Green	Default Value: 10 1100 0000b
12	19:10	Blue	Format: U0.10
		Red	Default Value: 10 1100 0000b
12	29:20	Green	Format: U0.10
		Blue	Default Value: 10 1100 0000b
12	31:30	Red	Format: U0.10
		Green	Default Value: 10 1100 0000b

SPR_GAMC			
	29:20	Red	
		Default Value:	11 0000 0000b
		Format:	U0.10
	19:10	Green	
		Default Value:	11 0000 0000b
		Format:	U0.10
	9:0	Blue	
		Default Value:	11 0000 0000b
		Format:	U0.10
13	31:30	Reserved	
		Format:	MBZ
	29:20	Red	
		Default Value:	11 0100 0000b
		Format:	U0.10
	19:10	Green	
		Default Value:	11 0100 0000b
		Format:	U0.10
	9:0	Blue	
		Default Value:	11 0100 0000b
		Format:	U0.10
14	31:30	Reserved	
		Format:	MBZ
	29:20	Red	
		Default Value:	11 1000 0000b
		Format:	U0.10
	19:10	Green	
		Default Value:	11 1000 0000b
		Format:	U0.10
	9:0	Blue	
		Default Value:	11 1000 0000b
		Format:	U0.10
15	31:30	Reserved	
		Format:	MBZ
	29:20	Red	
		Default Value:	11 1100 0000b
		Format:	U0.10

SPR_GAMC		
19:10	Green	Default Value: 11 1100 0000b
		Format: U0.10
9:0	Blue	Default Value: 11 1100 0000b
		Format: U0.10

SPR_GAMC16

SPR_GAMC16			
Register Space:	MMIO: 0/2/0		
Project:	BDW		
Default Value:	0x00000400, 0x00000400, 0x00000400		
Access:	R/W		
Size (in bits):	96		
Address:	70440h-7044Bh		
Name:	Sprite A Gamma Correction Point 16		
ShortName:	SPR_GAMC16_A_*		
Power:	Always on		
Reset:	soft		
Address:	71440h-7144Bh		
Name:	Sprite B Gamma Correction Point 16		
ShortName:	SPR_GAMC16_B_*		
Power:	off/on		
Reset:	soft		
Address:	72440h-7244Bh		
Name:	Sprite C Gamma Correction Point 16		
ShortName:	SPR_GAMC16_C_*		
Power:	off/on		
Reset:	soft		
These registers are used to determine the 17th reference point (point 16 when counting from 0) for sprite gamma correction. The values are represented in an unsigned 1.10 format with 1 integer and 10 fractional bits. See SPR_GAMC for sprite gamma programming information.			
Restriction			
The value should always be programmed to be less than or equal to 1.0.			
DWord	Bit	Description	
0	31:11	Reserved	
		Format:	MBZ
	10:0	GAMC16R	
		Default Value:	00000400h
		Format:	U1.10
This value specifies the 17th reference point that is used for the red color channel sprite gamma correction.			

SPR_GAMC16			
1	31:11	Reserved	
	10:0	GAMC16G	
		Default Value:	00000400h
		Format:	U1.10
		This value specifies the 17th reference point that is used for the green color channel sprite gamma correction.	
2	31:11	Reserved	
	10:0	GAMC16B	
	Default Value:	00000400h	
	Format:	U1.10	
	This value specifies the 17th reference point that is used for the blue color channel sprite gamma correction.		

SPR_GAMC17

SPR_GAMC17				
Register Space:	MMIO: 0/2/0			
Project:	BDW			
Default Value:	0x00000C00, 0x00000C00, 0x00000C00			
Access:	R/W			
Size (in bits):	96			
Address:	7044Ch-70457h			
Name:	Sprite A Gamma Correction Point 17			
ShortName:	SPR_GAMC17_A_*			
Power:	Always on			
Reset:	soft			
Address:	7144Ch-71457h			
Name:	Sprite B Gamma Correction Point 17			
ShortName:	SPR_GAMC17_B_*			
Power:	off/on			
Reset:	soft			
Address:	7244Ch-72457h			
Name:	Sprite C Gamma Correction Point 17			
ShortName:	SPR_GAMC17_C_*			
Power:	off/on			
Reset:	soft			
These registers are used to determine the 18th reference point (point 17 when counting from 0) for sprite gamma correction. The values are represented in an unsigned 2.10 format with 2 integer and 10 fractional bits. See SPR_GAMC for sprite gamma programming information.				
Restriction				
The value should always be programmed to be less than or equal to 3.0.				
DWord	Bit	Description		
0	31:12	Reserved		
		Format: MBZ		
	11:0	GAMC17R		
		Default Value: 00000C00h		
		Format: U2.10		
		This value specifies the 18th reference point that is used for the red color channel sprite gamma correction.		

SPR_GAMC17			
1	31:12	Reserved	
		Format:	MBZ
11:0	GAMC17G	Default Value:	00000C00h
		Format:	U2.10
This value specifies the 18th reference point that is used for the green color channel sprite gamma correction.			
2	31:12	Reserved	
		Format:	MBZ
11:0	GAMC17B	Default Value:	00000C00h
		Format:	U2.10
This value specifies the 18th reference point that is used for the blue color channel sprite gamma correction.			

SPR_KEYMAX

SPR_KEYMAX		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Access:	Double Buffered	
Size (in bits):	32	
Double Buffer Update Point:	Start of vertical blank or pipe not enabled	
Address:	702A0h-702A3h	
Name:	Sprite A Key Color Max	
ShortName:	SPR_KEYMAX_A	
Power:	Always on	
Reset:	soft	
Address:	712A0h-712A3h	
Name:	Sprite B Key Color Max	
ShortName:	SPR_KEYMAX_B	
Power:	off/on	
Reset:	soft	
Address:	722A0h-722A3h	
Name:	Sprite C Key Color Max	
ShortName:	SPR_KEYMAX_C	
Power:	off/on	
Reset:	soft	
For source key when sprite source is YUV, this register specifies the source key YUV maximum color value to be used together with the YUV minimum color value and the color channel enable bits to determine if the sprite matches the source key color range.		
DWord	Bit	Description
0	31:24	Reserved
		Format: MBZ
	23:16	V Source Key Max Value Specifies the color key maximum value for the sprite V channel source key
	15:8	Y Source Key Max Value Specifies the color key maximum value for the sprite Y channel source key
	7:0	U Source Key Max Value Specifies the color key maximum value for the sprite U channel source key

SPR_KEYMSK

SPR_KEYMSK				
Register Space:	MMIO: 0/2/0			
Project:	BDW			
Default Value:	0x00000000			
Access:	Double Buffered			
Size (in bits):	32			
Double Buffer Update Point:	Start of vertical blank or pipe not enabled			
Address:	70298h-7029Bh			
Name:	Sprite A Key Mask			
ShortName:	SPR_KEYMSK_A			
Power:	Always on			
Reset:	soft			
Address:	71298h-7129Bh			
Name:	Sprite B Key Mask			
ShortName:	SPR_KEYMSK_B			
Power:	off/on			
Reset:	soft			
Address:	72298h-7229Bh			
Name:	Sprite C Key Mask			
ShortName:	SPR_KEYMSK_C			
Power:	off/on			
Reset:	soft			
For source key, this register specifies which channels to perform key color checking on. A disabled channel will match on the full range. For destination key, this register specifies the key mask to be used with the color value bits to determine if the primary plane pixels match the key. A zero bit in the mask indicates that the corresponding bit match failure should be ignored when determining if the pixel matches.				
Restriction				
Source key and destination key are mutually exclusive modes of operation, they can not be used simultaneously. For the function that is not enabled, the associated bits in this register should be programmed to zeroes.				
DWord	Bit	Description		
0	31:27	<p>Reserved</p> <table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ
Format:	MBZ			

SPR_KEYMSK								
	26	V R Source Key Channel Enable Enables the V/Red channel for source key color comparison. <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Disable</td></tr> <tr> <td>1b</td><td>Enable</td></tr> </tbody> </table>	Value	Name	0b	Disable	1b	Enable
Value	Name							
0b	Disable							
1b	Enable							
	25	Y G Source Key Channel Enable Enables the Y/Green channel for source key color comparison. <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Disable</td></tr> <tr> <td>1b</td><td>Enable</td></tr> </tbody> </table>	Value	Name	0b	Disable	1b	Enable
Value	Name							
0b	Disable							
1b	Enable							
	24	U B Source Key Channel Enable Enables the U/Blue channel for source key color comparison. <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Disable</td></tr> <tr> <td>1b</td><td>Enable</td></tr> </tbody> </table>	Value	Name	0b	Disable	1b	Enable
Value	Name							
0b	Disable							
1b	Enable							
	23:16	R Dest Key Mask Value Specifies the destination color key mask for the Red channel						
	15:8	G Dest Key Mask Value Specifies the destination color key mask for the Green channel						
	7:0	B Dest Key Mask Value Specifies the destination color key mask for the Blue channel						

SPR_KEYVAL

SPR_KEYVAL		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Access:	Double Buffered	
Size (in bits):	32	
Double Buffer Update Point:	Start of vertical blank or pipe not enabled	
Address:	70294h-70297h	
Name:	Sprite A Key Color Value	
ShortName:	SPR_KEYVAL_A	
Power:	Always on	
Reset:	soft	
Address:	71294h-71297h	
Name:	Sprite B Key Color Value	
ShortName:	SPR_KEYVAL_B	
Power:	off/on	
Reset:	soft	
Address:	72294h-72297h	
Name:	Sprite C Key Color Value	
ShortName:	SPR_KEYVAL_C	
Power:	off/on	
Reset:	soft	
For source key when sprite source is YUV, this register specifies the source key YUV minimum color value to be used together with the YUV maximum color value and the color channel enable bits to determine if the sprite matches the source key color range. For source key when sprite source is RGB, this register specifies the source key RGB color value to be used together with the color channel enable bits to determine if the sprite matches the source key color. For destination key, this register specifies the destination key RGB color value to be used together with the RGB mask bits to determine if the primary matches the destination key color. A key match can only occur for positive pixel values in the 0 to 1 range. Extended range pixel values will not match.		
DWord	Bit	Description
0	31:24	Reserved
		Format: MBZ
23:16	V R Min Dest Key Value	
	Specifies the color key minimum value for the sprite V channel source key, the compare value for sprite Red channel source key, or the compare value for the primary Red channel destination key.	

SPR_KEYVAL		
	15:8	Y G Min Dest Key Value Specifies the color key minimum value for the sprite Y channel source key, the compare value for sprite Green channel source key, or the compare value for the primary Green channel destination key.
	7:0	U B Min Dest Key Value Specifies the color key minimum value for the sprite U channel source key, the compare value for sprite Blue channel source key, or the compare value for the primary Blue channel destination key.

SPR_LEFT_SURF

SPR_LEFT_SURF			
Register Space:	MMIO: 0/2/0		
Project:	BDW		
Default Value:	0x00000000		
Access:	Double Buffered		
Size (in bits):	32		
Double Buffer Update Point:		Start of left or right eye vertical blank (selectable) or pipe not enabled; after armed	
Double Buffer Armed Write to SPR_SURF or sprite not enabled By:			
Address:	702B0h-702B3h		
Name:	Sprite A Left Eye Base Address		
ShortName:	SPR_LEFT_SURF_A		
Power:	Always on		
Reset:	soft		
Address:	712B0h-712B3h		
Name:	Sprite B Left Eye Base Address		
ShortName:	SPR_LEFT_SURF_B		
Power:	off/on		
Reset:	soft		
Address:	722B0h-722B3h		
Name:	Sprite C Left Eye Base Address		
ShortName:	SPR_LEFT_SURF_C		
Power:	off/on		
Reset:	soft		
Restriction			
This register must be programmed with a valid address prior to enabling stereo 3D on this pipe.			
DWord	Bit	Description	
0	31:12	Left Surface Base Address	
		Format:	GraphicsAddress[31:12]
		This address specifies the stereo 3D left eye surface base address bits 31:12.	
Restriction			
This surface must have the same stride, tiling, and panning offset parameters as the right eye surface and meet all the same restrictions.			
11:0	Reserved		

SPR_OFFSET

SPR_OFFSET		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Access:	Double Buffered	
Size (in bits):	32	
Double Buffer Update Point:	Start of vertical blank or pipe not enabled	
Address:	702A4h-702A7h	
Name:	Sprite A Offset	
ShortName:	SPR_OFFSET_A	
Power:	Always on	
Reset:	soft	
Address:	712A4h-712A7h	
Name:	Sprite B Offset	
ShortName:	SPR_OFFSET_B	
Power:	off/on	
Reset:	soft	
Address:	722A4h-722A7h	
Name:	Sprite C Offset	
ShortName:	SPR_OFFSET_C	
Power:	off/on	
Reset:	soft	
This register specifies the panning for the sprite surface. The start position is specified in this register as a (x, y) offset from the beginning of the surface. When performing 180 rotation, hardware will internally add the sprite size to the offsets so the sprite will start displaying from the bottom right corner of the image.		
Restriction		
The sprite size + offset must not exceed the maximum supported sprite size.		
DWord	Bit	Description
0	31:28	Reserved
		Format: MBZ
	27:16	Start Y Position The vertical offset in lines of the beginning of the active display plane relative to the display surface.
	15:13	Reserved
		Format: MBZ

SPR_OFFSET				
	12:0	<p>Start X Position The horizontal offset in pixels of the beginning of the active display plane relative to the display surface.</p> <table border="1"><tr><th>Restriction</th></tr><tr><td>This offset must be even pixel aligned for YUV 4:2:2 formats.</td></tr></table>	Restriction	This offset must be even pixel aligned for YUV 4:2:2 formats.
Restriction				
This offset must be even pixel aligned for YUV 4:2:2 formats.				

SPR_POS

SPR_POS		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Access:	Double Buffered	
Size (in bits):	32	
Double Buffer Update Point:	Start of vertical blank or pipe not enabled; after armed	
Double Buffer Armed By:	Write to SPR_SURF or sprite not enabled	
Address:	7028Ch-7028Fh	
Name:	Sprite A Position	
ShortName:	SPR_POS_A	
Power:	Always on	
Reset:	soft	
Address:	7128Ch-7128Fh	
Name:	Sprite B Position	
ShortName:	SPR_POS_B	
Power:	off/on	
Reset:	soft	
Address:	7228Ch-7228Fh	
Name:	Sprite C Position	
ShortName:	SPR_POS_C	
Power:	off/on	
Reset:	soft	
This register specifies the screen position of the sprite. The origin of the sprite position is always the upper left corner of the display pipe source image area. When performing 180 degree rotation, the sprite image is rotated by hardware, but the position is not, so it must be adjusted if it is desired to maintain the same apparent position on a physically rotated display.		
Restriction		
The sprite must be completely contained within the pipe source area. Pipe source size >= sprite position + sprite size.		
DWord	Bit	Description
0	31:28	Reserved Format: MBZ
	27:16	Y Position This specifies the vertical position of the sprite upper left corner in lines.

SPR_POS			
	15:13	Reserved	
	12:0	X Position This specifies the horizontal position of the sprite upper left corner in pixels.	Format: MBZ

SPR_SIZE

SPR_SIZE			
Register Space:	MMIO: 0/2/0		
Project:	BDW		
Default Value:	0x00000000		
Access:	Double Buffered		
Size (in bits):	32		
Double Buffer Update Point:	Start of vertical blank or pipe not enabled; after armed		
Double Buffer Armed By:	Write to SPR_SURF or sprite not enabled		
Address:	70290h-70293h		
Name:	Sprite A Size		
ShortName:	SPR_SIZE_A		
Power:	Always on		
Reset:	soft		
Address:	71290h-71293h		
Name:	Sprite B Size		
ShortName:	SPR_SIZE_B		
Power:	off/on		
Reset:	soft		
Address:	72290h-72293h		
Name:	Sprite C Size		
ShortName:	SPR_SIZE_C		
Power:	off/on		
Reset:	soft		
This register specifies the size of the sprite.			
Restriction			
The sprite must be completely contained within the pipe source area. Pipe source size \geq sprite position + sprite size.			
DWord	Bit	Description	
0	31:28	Reserved	
		Format:	MBZ
	27:16	Height	This specifies the height of the sprite in lines. The value in the register is the height minus one.
		Restriction	
		The height must be at least one line.	

SPR_SIZE			
	15:13	Reserved	
		Format:	MBZ
	12:0	Width	This specifies the width of the sprite in pixels. The value in the register is the width minus one.
			Restriction
The width (prior to minus one) must be even when a YUV 4:2:2 source pixel format is used. The width must be at least one pixel. This should be less than or equal to the stride in pixels.			

SPR_STRIDE

SPR_STRIDE		
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x00000000 Access: Double Buffered Size (in bits): 32 Double Buffer Update Point: Start of vertical blank or pipe not enabled; after armed Double Buffer Armed Write to SPR_SURF or sprite not enabled By: Address: 70288h-7028Bh Name: Sprite A Stride ShortName: SPR_STRIDE_A Power: Always on Reset: soft		
Address: 71288h-7128Bh Name: Sprite B Stride ShortName: SPR_STRIDE_B Power: off/on Reset: soft		
Address: 72288h-7228Bh Name: Sprite C Stride ShortName: SPR_STRIDE_C Power: off/on Reset: soft		
DWord	Bit	Description
0	31:15	Reserved
	14:6	Stride This field specifies the stride bits 14:6 for the sprite. This value is used to determine the line to line increment for the sprite data fetches. This field is programmed in units of 64 bytes. This register may be updated through MMIO writes or through a command streamer initiated synchronous flip.
		Restriction
		When using linear memory, this must be at least 64 byte aligned. When using tiled memory, this must be at least 512 byte aligned. The stride is limited to a maximum of 16K bytes.
5:0 Reserved		

SPR_SURF

SPR_SURF				
Register Space:	MMIO: 0/2/0			
Project:	BDW			
Default Value:	0x00000000			
Access:	Double Buffered			
Size (in bits):	32			
Double Buffer Update Point:	Start of left or right eye vertical blank (selectable) or pipe not enabled			
Address:	7029Ch-7029Fh			
Name:	Sprite A Base Address			
ShortName:	SPR_SURF_A			
Power:	Always on			
Reset:	soft			
Address:	7129Ch-7129Fh			
Name:	Sprite B Base Address			
ShortName:	SPR_SURF_B			
Power:	off/on			
Reset:	soft			
Address:	7229Ch-7229Fh			
Name:	Sprite C Base Address			
ShortName:	SPR_SURF_C			
Power:	off/on			
Reset:	soft			
Writes to this register arm sprite registers for this pipe.				
A write to this register is considered a flip and can cause a flip done interrupt if the interrupt registers are configured for that. The values in this register may be updated through MMIO writes or through command streamer initiated flips, including synchronous flips.				
Synchronous updates (synchronous command streamer flips or synchronous MMIO writes) will update the plane surface values at the start of the next vertical blank.				
Restriction				
Asynchronous updates are not supported by sprite.				
DWord	Bit	Description		
0	31:12	<p>Surface Base Address</p> <table border="1"> <tr> <td>Format:</td><td>GraphicsAddress[31:12]</td></tr> </table> <p>This address specifies the surface base address bits 31:12. It represents an offset from the graphics memory aperture base and is mapped to physical pages through the global GTT.</p>	Format:	GraphicsAddress[31:12]
Format:	GraphicsAddress[31:12]			

SPR_SURF							
	<p>Workaround</p> <p>To prevent false VT-d type 6 errors, use 128KB address alignment and allocate an extra 64 Page Table Entries (PTEs) beyond the end of the displayed surface. Only the PTEs will be used, not the pages themselves.</p>						
<p>Restriction</p> <p>It must be at least 4KB aligned.</p>							
11:4	Reserved						
3	<p>Ring Flip Source</p> <p>This bit indicates if the source of the last ring flip was CS or BCS.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0b</td><td>CS</td></tr> <tr> <td>1b</td><td>BCS</td></tr> </tbody> </table>	Value	Name	0b	CS	1b	BCS
Value	Name						
0b	CS						
1b	BCS						
2	Reserved						
1:0	Reserved						

SQ Error Status

SQERR - SQ Error Status			
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x00000000 Size (in bits): 32			
Address: 09034h			
SQ Error Status register			
DWord	Bit	Description	
0	31:9	RSVD	Access: RO
	8	SQ RW Port Address Decode Error	Access: RO SQ RW Address Decode Error. This bit is cleared when SW writes to this bit.
	7:1	RSVD	Access: RO
	0	SQ RO Port Address Decode Error	Access: RO SQ RO Address Decode Error. This bit is cleared when SW writes to this bit.

SQ RO Port Decode Error Address LSB

SQROERRADDR_LSB - SQ RO Port Decode Error Address LSB		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	09210h	
SQ RO Port Decode Error Address		
DWord	Bit	Description
0	31:0	SQ RO Port Error Address LSB Access: RO SQ RO Port Decode Error Address.

SQ RO Port Decode Error Address MSB

SQROERRADDR_MSB - SQ RO Port Decode Error Address MSB				
Register Space:	MMIO: 0/2/0			
Project:	BDW			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	09214h			
SQ RO Port Decode Error Address				
DWord	Bit	Description		
0	31:8	RSVD <table border="1"> <tr> <td>Access:</td><td>RO</td></tr> </table>	Access:	RO
Access:	RO			
7:0	SQ RO Port Error Address MSB <table border="1"> <tr> <td>Access:</td><td>RO</td></tr> </table> SQ RO Port Decode Error Address.	Access:	RO	
Access:	RO			

SQ RW Port Decode Error Address LSB

SQRWERRADDR_LSB - SQ RW Port Decode Error Address LSB		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	09218h	
SQ RW Port Deocde Error Address		
DWord	Bit	Description
0	31:0	SQ RW Port Error Address LSB Access: RO SQ RW Port Error Address.

SQ RW Port Decode Error Address MSB

SQRWERRADDR_MSB - SQ RW Port Decode Error Address MSB				
Register Space:	MMIO: 0/2/0			
Project:	BDW			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	0921Ch			
SQ RW Port Deocde Error Address				
DWord	Bit	Description		
0	31:8	RSVD <table border="1"> <tr> <td>Access:</td><td>RO</td></tr> </table>	Access:	RO
Access:	RO			
7:0	SQ RW Port Error Address MSB <table border="1"> <tr> <td>Access:</td><td>RO</td></tr> </table> SQ RW Port Error Address.	Access:	RO	
Access:	RO			

SRD_AUX_CTL

SRD_AUX_CTL											
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x000300E1 Access: R/W Size (in bits): 32											
Address: 6F810h-6F813h Name: Transcoder EDP SRD AUX Channel Control ShortName: SRD_AUX_CTL Power: Always on Reset: soft											
Restriction											
This register must be programmed prior to enabling SRD and must not be changed while SRD is enabled. SRD AUX channel transactions must not be sent while DDI A AUX is being used. SRD must be completely disabled before a DDI A AUX channel transaction can be sent.											
DWord	Bit	Description									
0	31:28	Reserved									
	27:26	Time out timer value This field is used to determine how long to wait for receiver response before timing out. <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>00b</td><td>400us</td></tr> <tr> <td>01b</td><td>600us</td></tr> <tr> <td>10b</td><td>800us</td></tr> <tr> <td>11b</td><td>1600us</td></tr> </tbody> </table>	Value	Name	00b	400us	01b	600us	10b	800us	11b
Value	Name										
00b	400us										
01b	600us										
10b	800us										
11b	1600us										
25	Reserved										
24:20	Message Size The value written to this field indicates the total number bytes to transmit (including the header). The value read from this field indicates the number of bytes received, including the header, in the last transaction transaction. Sync/Stop are not part of the message or the message size. Reads of this field will give the response message size. The read value will not be valid while Send/Busy bit 31 is asserted. <table border="1"> <thead> <tr> <th>Restriction</th></tr> </thead> <tbody> <tr> <td>Message sizes of 0 or >20 are not allowed. Reads and writes are valid only when the done bit is set and timeout or receive error has not occurred.</td></tr> </tbody> </table>	Restriction	Message sizes of 0 or >20 are not allowed. Reads and writes are valid only when the done bit is set and timeout or receive error has not occurred.								
Restriction											
Message sizes of 0 or >20 are not allowed. Reads and writes are valid only when the done bit is set and timeout or receive error has not occurred.											

SRD_AUX_CTL								
	19:16	<p>Precharge Time</p> <table border="1"> <tr> <td>Default Value:</td><td>0011b 6us</td></tr> </table> <p>Used to determine the precharge time for the Aux Channel. During this time the Aux Channel will drive the SYNC pattern. Every microsecond gives one additional SYNC pulse beyond the hard coded 26 SYNC pulses. The value is the number of microseconds times 2. Default is 3 decimal which gives 6us of precharge which is 6 extra SYNC pulses for a total of 32.</p>	Default Value:	0011b 6us				
Default Value:	0011b 6us							
	15:12	Reserved						
	11	<p>Interrupt on Error</p> <p>Enable an interrupt when the transaction completes with a receive error or times out.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Disable</td></tr> <tr> <td>1b</td><td>Enable</td></tr> </tbody> </table>	Value	Name	0b	Disable	1b	Enable
Value	Name							
0b	Disable							
1b	Enable							
	10:0	<p>2X Bit Clock divider</p> <table border="1"> <tr> <td>Default Value:</td><td>00 1110 0001b 225</td></tr> </table> <p>This field is used to determine the 2X bit clock the Aux Channel logic runs on. This value divides the input clock frequency down to 2X bit clock rate. It should be programmed to get as close as possible to the ideal rate of 2MHz. The input clock is the cdclk. Default is 225 decimal which divides the default 450 MHz cdclk input clock to become 2MHz bit clock.</p> <table border="1"> <tr> <td>Restriction</td></tr> </table> <p>The default value only works with cdclk 450 MHz. It must be programmed if the CD clock frequency is changed.</p>	Default Value:	00 1110 0001b 225	Restriction			
Default Value:	00 1110 0001b 225							
Restriction								

SRD_AUX_DATA

SRD_AUX_DATA		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Access:	Write/Read Status	
Size (in bits):	32	
Address:	6F814h-6F827h	
Name:	Transcoder EDP SRD AUX Channel Data	
ShortName:	SRD_AUX_DATA_*	
Power:	Always on	
Reset:	soft	
There are 5 instances of this register format.		
Restriction		
This register must be programmed prior to enabling SRD and must not be changed while SRD is enabled.		
DWord	Bit	Description
0	31:0	SRD AUX CH DATA This field contains a dword of the SRD AUX data to be transmitted in the SRD AUX message. The most significant byte is transmitted first.

SRD_CTL

SRD_CTL	
Register Space:	MMIO: 0/2/0
Project:	BDW 0x00100001 [BDW]
Access:	R/W
Size (in bits):	32
Address:	60800h-60803h
Name:	Transcoder A SRD Control
ShortName:	SRD_CTL_A
Valid Projects:	BDW
Power:	off/on
Reset:	soft
Address:	61800h-61803h
Name:	Transcoder B SRD Control
ShortName:	SRD_CTL_B
Valid Projects:	BDW
Power:	off/on
Reset:	soft
Address:	62800h-62803h
Name:	Transcoder C SRD Control
ShortName:	SRD_CTL_C
Valid Projects:	BDW
Power:	off/on
Reset:	soft
Address:	6F800h-6F803h
Name:	Transcoder EDP SRD Control
ShortName:	SRD_CTL_EDP
Valid Projects:	BDW
Power:	Always on
Reset:	soft
There is one instance of this register format per each transcoder A/B/C/EDP.	
Programming Notes	
To use FBC modification tracking for idleness calculations when FBC is disabled, program FBC_CTL CPU Fence Enable, FBC_CONTROL_SA_REGISTER, FBC_CPU_FENCE_OFFSET_REGISTER, FBC_RT_BASE_ADDR_REGISTER, and BLITTER_TRACKING_REGISTER as they are programmed when FBC is enabled.	

SRD_CTL

Cursor front buffer modifications are not tracked in hardware. If the cursor front buffer is modified, touch (write without changing) any cursor register to trigger the PSR idleness tracking.

Restriction

Only the SRD Enable and Single Frame Update Enable fields can be changed while SRD is enabled. The other fields must not be changed while SRD is enabled.

DWord	Bit	Description							
0	31	SRD Enable This bit enables the Self Refreshing Display function. Updates will take place at the start of the next vertical blank. The port will send SRD VDMs while enabled. When idleness conditions have been met for the programmed number of idle frames, hardware will enter SRD (sleep) and can disable the link and stop fetching data from memory. When activity occurs, hardware will exit SRD (wake) and re-enable the link and resume fetching data from memory. <table border="1" style="width: 100%; margin-top: 5px;"> <thead> <tr> <th style="text-align: center;">Value</th><th style="text-align: center;">Name</th></tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td><td>Disable</td></tr> <tr> <td style="text-align: center;">1b</td><td>Enable</td></tr> </tbody> </table>	Value	Name	0b	Disable	1b	Enable	
Value	Name								
0b	Disable								
1b	Enable								
Workaround									
Registers 0x42080 bit 15, 0x420B0 bit 0, 0x420B4 bit 0, and 0x420B8 bit 0 must be programmed to 1b before enabling SRD and kept at 1b while SRD is enabled. It is safe to have them as 1b even when SRD is disabled.									
Restriction									
SRD must not be enabled when the PSR Setup time from DPCD 00071h is greater than the time for vertical blank minus one line. SRD must not be enabled together with Interlacing, Black Frame Insertion (BFI), or audio on the same transcoder.									
30	Single Frame Update Enable Access: Double Buffered	This field enables the single frame update mode where a plane flip will cause a single frame to be sent to the receiver. Updates to this field will take effect at the next vertical blank. <table border="1" style="width: 100%; margin-top: 5px;"> <thead> <tr> <th style="text-align: center;">Value</th><th style="text-align: center;">Name</th></tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td><td>Disable</td></tr> <tr> <td style="text-align: center;">1b</td><td>Enable</td></tr> </tbody> </table>		Value	Name	0b	Disable	1b	Enable
Value	Name								
0b	Disable								
1b	Enable								
Programming Notes									
Set register PIPE_MISC field Change Mask for Vblank Vsync Int to 1b (Masked) if vblank or vsync interrupts will be used together with single frame update.									

SRD_CTL

Workaround

When Single Frame Update is enabled, register write events must be masked to prevent flips from exiting out of the single frame mode. Mask register write events by setting register x6F860 bit 16 to 1. Unmask register write events by clearing register 0x6F860 bit 16 to 0. Masking register write events means that some events will not trigger PSR to exit and update the screen. If flips are happening frequently, the next flip will soon cause a screen update. If flips are not happening often enough, it may be necessary to disable Single Frame Update or to unmask the register write events temporarily in order to get the screen to update for non-flip events.

When Single Frame Update will be used with sprite, the sprite enable must be masked. Mask the sprite enable by setting register PIPE_MISC field Change Mask for Sprite Enable to 1. Unmask the sprite enable by clearing register PIPE_MISC field Change Mask for Sprite Enable to 0.

Restriction

This mode should only be enabled with link standby.

29 Reserved

Project:	BDW
Format:	MBZ

28 Reserved

Format:	MBZ
---------	-----

27 Link Ctrl

This field controls the behavior of the link when in SRD (sleeping). The timing generator and pixel data fetches are disabled when the link is disabled. Only pixel data fetches are disabled when the link is in standby.

This field is ignored by transcoder A/B/C since they only operate in standby.

Value	Name	Description
0b	Disable	Link is disabled when in SRD (sleeping)
1b	Standby	Link is in standby when in SRD (sleeping)

26:25 Reserved

Format:	MBZ
---------	-----

24:20 Max Sleep Time

Default Value:	00001b 1/8 second
----------------	-------------------

This field is the maximum time to spend in SRD (sleeping). It is programmed in increments of approximately 1/8 a second. Programming all 1s gives ~3.875 seconds.

Restriction

Programming all 0s is invalid.

19:14 Reserved

Project:	BDW
Format:	MBZ

SRD_CTL												
	13	Reserved										
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> </table>	Project:	BDW								
Project:	BDW											
	12	Reserved										
	11	TP2 TP3 Select This field controls whether TP1 is followed by TP2 or TP3 for training the link on exiting SRD (waking). <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>TP2</td><td>Use TP1 followed by TP2</td></tr> <tr> <td>1b</td><td>TP3</td><td>Use TP1 followed by TP3</td></tr> </tbody> </table>	Value	Name	Description	0b	TP2	Use TP1 followed by TP2	1b	TP3	Use TP1 followed by TP3	
Value	Name	Description										
0b	TP2	Use TP1 followed by TP2										
1b	TP3	Use TP1 followed by TP3										
	10	Reserved										
	9:8	TP2 TP3 Time This field selects the TP2 or TP3 time when training the link on exiting SRD (waking). <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>00b</td><td>500us</td></tr> <tr> <td>01b</td><td>100us</td></tr> <tr> <td>10b</td><td>2.5ms</td></tr> <tr> <td>11b</td><td>0us Skip TP2/TP3</td></tr> </tbody> </table>	Value	Name	00b	500us	01b	100us	10b	2.5ms	11b	0us Skip TP2/TP3
Value	Name											
00b	500us											
01b	100us											
10b	2.5ms											
11b	0us Skip TP2/TP3											
	7:6	Reserved <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	BDW	Format:	MBZ						
Project:	BDW											
Format:	MBZ											
	5:4	TP1 Time This field selects the TP1 time when training the link on exiting SRD (waking). <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>00b</td><td>500us</td></tr> <tr> <td>01b</td><td>100us</td></tr> <tr> <td>10b</td><td>2.5ms</td></tr> <tr> <td>11b</td><td>0us Slip TP1</td></tr> </tbody> </table>	Value	Name	00b	500us	01b	100us	10b	2.5ms	11b	0us Slip TP1
Value	Name											
00b	500us											
01b	100us											
10b	2.5ms											
11b	0us Slip TP1											
	3:0	Idle Frames <table border="1"> <tr> <td>Default Value:</td><td>0001b 1 idle frame</td></tr> </table> This field is the number of idle frames required before entering SRD (sleeping).	Default Value:	0001b 1 idle frame								
Default Value:	0001b 1 idle frame											

SRD_IIR

SRD_IIR								
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x00000000 Access: R/WC Size (in bits): 32								
Address: 64838h-6483Bh Name: SRD Interrupt Identity ShortName: SRD_IIR Valid Projects: BDW Power: Always on Reset: soft								
See the SRD interrupt bit definition to find the source event for each interrupt bit.								
DWord	Bit	Description						
0	31:0	<p>Interrupt Identity Bits</p> <p>This field holds the persistent values of the SRD interrupt bits which are unmasked by the SRD_IMR. Bits set in this register will propagate to the SRD interrupt in the Display Engine Miscellaneous Interrupts. Bits set in this register will remain set (persist) until the interrupt condition is cleared by writing a '1' to the appropriate bits</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Condition Not Detected</td></tr> <tr> <td>1b</td><td>Condition Detected</td></tr> </tbody> </table>	Value	Name	0b	Condition Not Detected	1b	Condition Detected
Value	Name							
0b	Condition Not Detected							
1b	Condition Detected							

SRD_IMR

SRD_IMR														
Register Space:	MMIO: 0/2/0													
Project:	BDW													
Default Value:	0x03030307													
Access:	R/W													
Size (in bits):	32													
Address:	64834h-64837h													
Name:	SRD Interrupt Mask													
ShortName:	SRD_IMR													
Valid Projects:	BDW													
Power:	Always on													
Reset:	soft													
See the SRD interrupt bit definition to find the source event for each interrupt bit.														
DWord	Bit	Description												
0	31:0	Interrupt_Mask_Bits This field contains a bit mask which selects which SRD events are reported int the SRD_IIR. <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Project</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Not Masked</td><td></td></tr> <tr> <td>1b</td><td>Masked</td><td></td></tr> <tr> <td>03030307h</td><td>All interrupts masked [Default]</td><td>BDW</td></tr> </tbody> </table>	Value	Name	Project	0b	Not Masked		1b	Masked		03030307h	All interrupts masked [Default]	BDW
Value	Name	Project												
0b	Not Masked													
1b	Masked													
03030307h	All interrupts masked [Default]	BDW												

SRD_PERF_CNT

SRD_PERF_CNT			
Register Space:	MMIO: 0/2/0		
Project:	BDW		
Default Value:	0x00000000		
Access:	Write/Read Status		
Size (in bits):	32		
Address:	60844h-60847h		
Name:	Transcoder A SRD Performance Counter		
ShortName:	SRD_PERF_CNT_A		
Valid Projects:	BDW		
Power:	off/on		
Reset:	soft		
Address:	61844h-61847h		
Name:	Transcoder B SRD Performance Counter		
ShortName:	SRD_PERF_CNT_B		
Valid Projects:	BDW		
Power:	off/on		
Reset:	soft		
Address:	62844h-62847h		
Name:	Transcoder C SRD Performance Counter		
ShortName:	SRD_PERF_CNT_C		
Valid Projects:	BDW		
Power:	off/on		
Reset:	soft		
Address:	6F844h-6F847h		
Name:	Transcoder EDP SRD Performance Counter		
ShortName:	SRD_PERF_CNT_EDP		
Valid Projects:	BDW		
Power:	Always on		
Reset:	soft		
Description			Project
There is one instance of this register format per each transcoder A/B/C/EDP.			BDW
DWord	Bit	Description	
0	31:24	Reserved	Format: MBZ

SRD_PERF_CNT		
	23:0	SRD Perf Cnt This field increments every millisecond while in SRD (sleeping) and the display CD clock is running. It will stop incrementing when out of SRD (awake), then resume when back in SRD (sleeping). The value is maintained while SRD is disabled, and counting will resume from the previous value when SRD is re-enabled. Writes to this register will set the count to the written value, then it will increment from that value onwards.

SRD_STATUS

SRD_STATUS			
Register Space:	MMIO: 0/2/0		
Project:	BDW		
Default Value:	0x00000000		
Access:	RO		
Size (in bits):	32		
Address:	60840h-60843h		
Name:	Transcoder A SRD Status		
ShortName:	SRD_STATUS_A		
Valid Projects:	BDW		
Power:	off/on		
Reset:	soft		
Address:	61840h-61843h		
Name:	Transcoder B SRD Status		
ShortName:	SRD_STATUS_B		
Valid Projects:	BDW		
Power:	off/on		
Reset:	soft		
Address:	62840h-62843h		
Name:	Transcoder C SRD Status		
ShortName:	SRD_STATUS_C		
Valid Projects:	BDW		
Power:	off/on		
Reset:	soft		
Address:	6F840h-6F843h		
Name:	Transcoder EDP SRD Status		
ShortName:	SRD_STATUS_EDP		
Valid Projects:	BDW		
Power:	Always on		
Reset:	soft		
Description			Project
There is one instance of this register format per each transcoder A/B/C/EDP.			BDW
DWord	Bit	Description	
0	31:29	SRD State	
		Access:	RO
		This field indicates the live state of SRD	

SRD_STATUS				
		Value	Name	Description
		000b	IDLE	Reset state
		001b	SRDONACK	Wait for TG/Stream to send on frame of data after SRD conditions are met
		010b	SRDENT	SRD entry
		011b	BUFOFF	Wait for buffer turn off
		100b	BUFON	Wait for buffer turn on
		101b	AUXACK	Wait for AUX to acknowledge on SRD exit
		110b	SRDOFFACK	Wait for TG/Stream to acknowledge the SRD VDM exit
		Others	Reserved	Reserved
	28	Reserved		Format: MBZ
	27:26	Link Status		
		Access:		RO
		This field indicates the live status of the link.		
		Value	Name	Description
		00b	Full Off	Link is fully off
		01b	Full On	Link is fully on
		10b	Standby	Link is in standby
		11b	Reserved	Reserved
	25	Reserved		Format: MBZ
	24:20	Max Sleep Time Counter		
		Access:		RO
		This field provides the live status of the sleep time counter.		
	19:16	SRD Entry Count		
		Access:		RO
		The value in this register represents the number of times SRD has been entered (gone to sleep). The count will increment with each entry. After reaching the maximum count value the counter will rollover and continue from 0.		

SRD_STATUS																	
15	Aux Error	<p>Access: RO</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th colspan="2" style="text-align: center; background-color: #e0e0ff;">Description</th></tr> </thead> <tbody> <tr> <td colspan="2">This field indicates an error on the last SRD AUX handshake.</td></tr> <tr> <td colspan="2">The Aux Error status non-EDP transcoders follows the mapping from Aux channel to transcoder: Aux B to SRD_STATUS_A. Aux C to SRD_STATUS_B. Aux D to SRD_STATUS_C.</td></tr> </tbody> </table> <table border="1" style="margin-top: 10px; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th><th style="text-align: center;">Name</th><th style="text-align: center;">Description</th></tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td><td>No Error</td><td>AUX had no error</td></tr> <tr> <td style="text-align: center;">1b</td><td>Error</td><td>AUX error (receive error or timeout) occurred</td></tr> </tbody> </table>	Description		This field indicates an error on the last SRD AUX handshake.		The Aux Error status non-EDP transcoders follows the mapping from Aux channel to transcoder: Aux B to SRD_STATUS_A. Aux C to SRD_STATUS_B. Aux D to SRD_STATUS_C.		Value	Name	Description	0b	No Error	AUX had no error	1b	Error	AUX error (receive error or timeout) occurred
Description																	
This field indicates an error on the last SRD AUX handshake.																	
The Aux Error status non-EDP transcoders follows the mapping from Aux channel to transcoder: Aux B to SRD_STATUS_A. Aux C to SRD_STATUS_B. Aux D to SRD_STATUS_C.																	
Value	Name	Description															
0b	No Error	AUX had no error															
1b	Error	AUX error (receive error or timeout) occurred															
14:13	Reserved	<p>Format: MBZ</p>															
12	Sending Aux	<p>Access: RO</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th colspan="2" style="text-align: center; background-color: #e0e0ff;">Description</th></tr> </thead> <tbody> <tr> <td colspan="2">This field indicates if the SRD AUX handshake is currently being sent.</td></tr> <tr> <td colspan="2">The Sending Aux status non-EDP transcoders follows the mapping from Aux channel to transcoder: Aux B to SRD_STATUS_A. Aux C to SRD_STATUS_B. Aux D to SRD_STATUS_C.</td></tr> </tbody> </table> <table border="1" style="margin-top: 10px; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th><th style="text-align: center;">Name</th><th style="text-align: center;">Description</th></tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td><td>Not Sending</td><td>Not sending AUX handshake</td></tr> <tr> <td style="text-align: center;">1b</td><td>Sending</td><td>Sending AUX handshake</td></tr> </tbody> </table>	Description		This field indicates if the SRD AUX handshake is currently being sent.		The Sending Aux status non-EDP transcoders follows the mapping from Aux channel to transcoder: Aux B to SRD_STATUS_A. Aux C to SRD_STATUS_B. Aux D to SRD_STATUS_C.		Value	Name	Description	0b	Not Sending	Not sending AUX handshake	1b	Sending	Sending AUX handshake
Description																	
This field indicates if the SRD AUX handshake is currently being sent.																	
The Sending Aux status non-EDP transcoders follows the mapping from Aux channel to transcoder: Aux B to SRD_STATUS_A. Aux C to SRD_STATUS_B. Aux D to SRD_STATUS_C.																	
Value	Name	Description															
0b	Not Sending	Not sending AUX handshake															
1b	Sending	Sending AUX handshake															
11:10	Reserved	<p>Format: MBZ</p>															
9	Sending Idle	<p>Access: RO</p> <p>This field indicates if idles are currently being sent.</p> <table border="1" style="margin-top: 10px; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th><th style="text-align: center;">Name</th><th style="text-align: center;">Description</th></tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td><td>Not Sending</td><td>Not sending idle</td></tr> <tr> <td style="text-align: center;">1b</td><td>Sending</td><td>Sending idle</td></tr> </tbody> </table>	Value	Name	Description	0b	Not Sending	Not sending idle	1b	Sending	Sending idle						
Value	Name	Description															
0b	Not Sending	Not sending idle															
1b	Sending	Sending idle															
8	Sending TP2 TP3	<p>Access: RO</p> <p>This field indicates if TP2 or TP3 is currently being sent.</p> <table border="1" style="margin-top: 10px; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th><th style="text-align: center;">Name</th><th style="text-align: center;">Description</th></tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td><td>Not Sending</td><td>Not sending TP2 or TP3</td></tr> <tr> <td style="text-align: center;">1b</td><td>Sending</td><td>Sending TP2 or TP3</td></tr> </tbody> </table>	Value	Name	Description	0b	Not Sending	Not sending TP2 or TP3	1b	Sending	Sending TP2 or TP3						
Value	Name	Description															
0b	Not Sending	Not sending TP2 or TP3															
1b	Sending	Sending TP2 or TP3															

SRD_STATUS			
	7:5	Reserved	
		Format:	MBZ
	4	Sending TP1	
		Access:	RO
		This field indicates if TP1 is currently being sent.	
		Value	Name
		0b	Not Sending
		1b	Sending
	3:0	Idle Frame Counter	
		Access:	RO
		This field provides the live status of the idle frame counter.	

Staggered EU/SAMPLER PAUSE with Lock bit

GFX_PAUSE - Staggered EU/SAMPLER PAUSE with Lock bit

Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	0A000h					
Lock bit LOCK applies to all RW/L fields this register. These bits are not reset on FLR (device reset).						
DWord	Bit	Description				
0	31:19	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td colspan="2">Reserved.</td></tr> </table>	Access:	RO	Reserved.	
Access:	RO					
Reserved.						
18	<p>Graphics Pause Lock</p> <table border="1"> <tr> <td>Access:</td> <td>R/W Lock</td> </tr> <tr> <td colspan="2">0 = Bits of GFXPAUSE register are R/W. 1 = All bits of GFXPAUSE register are RO (including this lock bit). Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 does not clear the lock). These bits are not reset on FLR.</td></tr> </table>	Access:	R/W Lock	0 = Bits of GFXPAUSE register are R/W. 1 = All bits of GFXPAUSE register are RO (including this lock bit). Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 does not clear the lock). These bits are not reset on FLR.		
Access:	R/W Lock					
0 = Bits of GFXPAUSE register are R/W. 1 = All bits of GFXPAUSE register are RO (including this lock bit). Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 does not clear the lock). These bits are not reset on FLR.						
17	<p>Pause Enable for EUs</p> <table border="1"> <tr> <td>Access:</td> <td>R/W Lock</td> </tr> <tr> <td colspan="2">0 = Disabled. EUs are not paused during frequency changes. 1 = Enabled. EUs are paused before graphics clocks are gated, and unpaused (staggered per EU) when the clocks are ungated. This field is locked by LOCK. These bits are not reset on FLR.</td></tr> </table>	Access:	R/W Lock	0 = Disabled. EUs are not paused during frequency changes. 1 = Enabled. EUs are paused before graphics clocks are gated, and unpaused (staggered per EU) when the clocks are ungated. This field is locked by LOCK. These bits are not reset on FLR.		
Access:	R/W Lock					
0 = Disabled. EUs are not paused during frequency changes. 1 = Enabled. EUs are paused before graphics clocks are gated, and unpaused (staggered per EU) when the clocks are ungated. This field is locked by LOCK. These bits are not reset on FLR.						
16	<p>Pause Enable for Sampler</p> <table border="1"> <tr> <td>Access:</td> <td>R/W Lock</td> </tr> <tr> <td colspan="2">0 = Disabled. Sampler is not paused during frequency changes. 1 = Enabled. Sampler is paused before graphics clocks are gated, and unpaused when the clocks are ungated. This field is locked by LOCK. These bits are not reset on FLR.</td></tr> </table>	Access:	R/W Lock	0 = Disabled. Sampler is not paused during frequency changes. 1 = Enabled. Sampler is paused before graphics clocks are gated, and unpaused when the clocks are ungated. This field is locked by LOCK. These bits are not reset on FLR.		
Access:	R/W Lock					
0 = Disabled. Sampler is not paused during frequency changes. 1 = Enabled. Sampler is paused before graphics clocks are gated, and unpaused when the clocks are ungated. This field is locked by LOCK. These bits are not reset on FLR.						

GFX_PAUSE - Staggered EU/SAMPLER PAUSE with Lock bit

15:0	Pause Count Timer	
	Access:	R/W Lock
<p>This is the minimum time the PMunit waits after asserting the EU or Sampler pause (if those are enabled) before allowing the core clocks to be gated.</p> <p>0000h = Disabled.</p> <p>0001h - Count 1 CSclk.</p> <p>...</p> <p>FFFFh = Count 65535 CSclks.</p> <p>This field is locked by LOCK.</p> <p>These bits are not reset on FLR.</p>		

Storage 0 (timestamp - lsb)

MISC_STATUS0 - Storage 0 (timestamp - lsb)				
DWord	Bit	Description		
0	31:0	<p>Time Stamp Storage</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>pmcr_time_stamp_lsb[31:0].</p>	Access:	R/W
Access:	R/W			
Time Stamp Storage pmcr_time_stamp_store[31:0]				

Storage 1 (timestamp - msb)

MISC_STATUS1 - Storage 1 (timestamp-msb)		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0A504h	
DWord	Bit	Description
0	31:0	Time Stamp Storage2 Access: R/W pmcr_time_stamp_msb[31:0].

Storage 2 (Same as RC_STATUS0 - wakerate_cntr)

RC_STATUS0_DUP - Storage 2 (Same as RC_STATUS0 - wakerate_cntr)				
DWord	Bit	Description		
0	31:16	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
Access:	RO			
15:0	Wake Rate Counter <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> pmcr_wake_rate_store[15:0].	Access:	R/W	
Access:	R/W			

Storage 5 (same as RP_STATUS3 - incfreq_ei_cntr)

RP_STATUS3_DUP - Storage 5 (same as RP_STATUS3 - incfreq_ei_cntr)				
DWord	Bit	Description		
0	31:24	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
Access:	RO			
23:0	RP EI Up Counter <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>pmcr_ei_up_counter_store[23:0].</p>	Access:	R/W	
Access:	R/W			

Storage 6 (Same as RP_STATUS5 - incfreq_cntr)

RP_STATUS5_DUP - Storage 6 (Same as RP_STATUS5 - incfreq_cntr)				
DWord	Bit	Description		
0	31:24	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
Access:	RO			
23:0	RP EI Up Busy Counter <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> pmcr_ei_up_busy_counter_store[23:0].	Access:	R/W	
Access:	R/W			

Storage 7 (same as RP_STATUS4 - decfreq_ei_cntr)

RP_STATUS4_DUP - Storage 7 (same as RP_STATUS4 - decfreq_ei_cntr)				
DWord	Bit	Description		
0	31:24	RESERVED <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
Access:	RO			
23:0	RP EI Down Counter <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>pmcr_ei_down_counter_store[23:0].</p>	Access:	R/W	
Access:	R/W			

Storage 8 (same as RP_STATUS6 - decfreq_cntr)

RP_STATUS6_DUP - Storage 8 (same as RP_STATUS6 - decfreq_cntr)				
DWord	Bit	Description		
0	31:24	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
Access:	RO			
23:0	RP EI Down Busy Counter <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> pmcr_ei_down_busy_counter_store[23:0].	Access:	R/W	
Access:	R/W			

Stream Output Num Primitives Written Counter

SO_NUM_PRIMS_WRITTEN[0:3] - Stream Output Num Primitives Written Counter				
Register Space:	MMIO: 0/2/0			
Project:	BDW			
Source:	RenderCS			
Default Value:	0x00000000, 0x00000000			
Access:	R/W			
Size (in bits):	64			
Address:	05200h-0521Fh			
<p>There is one 64-bit register for each of the 4 supported streams: 5200h-5207h SO_NUM_PRIMS_WRITTEN0 (for Stream Out Stream #0) 5208h-520Fh SO_NUM_PRIMS_WRITTEN1 (for Stream Out Stream #1) 5210h-5217h SO_NUM_PRIMS_WRITTEN2 (for Stream Out Stream #2) 5218h-521Fh SO_NUM_PRIMS_WRITTEN3 (for Stream Out Stream #3). These registers are used to count the number of primitives (aka objects: points, lines, triangles) which the SO stage has successfully written to a particular "stream's" Streamed Vertex Output buffers, subject to buffer overflow detection. (See the Stream Output section of the 3D pipeline volume). These registers are part of the context save and restore.</p>				
DWord	Bit	Description		
0	63:0	<p>Num Prims Written Count</p> <table border="1"> <tr> <td>Format:</td><td>U64</td></tr> </table> <p>This count is incremented (by one) every time a GS thread outputs a DataPort Streamed Vertex Buffer Write message with the Increment Num Prims Written bit set in the message header (see the Geometry Shader and Data Port chapters in the 3D Volume.)</p>	Format:	U64
Format:	U64			

Stream Output Primitive Storage Needed Counters

SO_PRIM_STORAGE_NEEDED[0:3] - Stream Output Primitive Storage Needed Counters

Register Space:	MMIO: 0/2/0
Project:	BDW
Source:	RenderCS
Default Value:	0x00000000, 0x00000000
Access:	RW. This register is set by the context restore.
Size (in bits):	64
Address:	05240h-0525Fh

There is one 64-bit register for each of the 4 supported streams:

5240h-5247h SO_PRIM_STORAGE_NEEDED0 (for Stream Out Stream #0)
5248h-524Fh SO_PRIM_STORAGE_NEEDED1 (for Stream Out Stream #1)
5250h-5257h SO_PRIM_STORAGE_NEEDED2 (for Stream Out Stream #2)
5258h-525Fh SO_PRIM_STORAGE_NEEDED3 (for Stream Out Stream #3)

These registers are used to count the number of primitives (aka objects: points, lines, triangles) which the SO stage has or would have written to a particular "stream's" Streamed Vertex Output buffers if all buffers had been large enough to accommodate the writes. (See the Stream Output section of the 3D pipeline volume).

These registers are part of the context save and restore.

DWord	Bit	Description				
0	63:0	<p>Prim Storage Needed Count</p> <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Format:</td> <td>U64</td> </tr> </table> <p>This count is incremented (by one) by the SOL stage for each object (point, line, triangle) it writes or attempts to write to the corresponding stream's output buffers. The count is not affected by the actual number of buffers bound to the stream.</p>	Project:	BDW	Format:	U64
Project:	BDW					
Format:	U64					

Stream Output Write Offsets

SO_WRITE_OFFSET[0:3] - Stream Output Write Offsets

Register Space:	MMIO: 0/2/0
Project:	BDW
Source:	RenderCS
Default Value:	0x00000000
Access:	RW. This register is set by the context restore.
Size (in bits):	32
Address:	05280h-0528Fh

There is one R/W 32-bit register for each of the 4 supported stream output buffer slots:

5280h-5283h SO_WRITE_OFFSET0 (for Stream Out Buffer #0)

5284h-5287h SO_WRITE_OFFSET1 (for Stream Out Buffer #1)

5288h-528Bh SO_WRITE_OFFSET2 (for Stream Out Buffer #2)

528Ch-528Fh SO_WRITE_OFFSET3 (for Stream Out Buffer #3)

These registers are used to set and track a DWord-granular Write Offset for each of the 4 Stream Output Buffer slots. Software can directly write them via MI_LOAD_REGxxx commands. The SOL stage will increment them as part of stream output processing. Software can cause them to be written to memory via MI_STORE_REGxxx commands. (See the Stream Output section of the 3D pipeline volume).

These registers are part of the context save and restore.

Programming Notes

- Software must ensure that no HW stream output operations can be in process or otherwise pending at the point that the MI_LOAD/STORE commands are processed. This will likely require a pipeline flush.
- The SOL stage will effectively advance the write offset by the buffer's Surface Pitch after each vertex is written (assuming no overflow is detected in any targetted SO buffer). Under "normal" conditions one would expect software to initialize the WriteOffset to some (possibly zero) multiple of Surface Pitch in order to align vertex writes to the buffer's Base Address, though it is not required to do so.

DWord	Bit	Description		
0	31:2	Write Offset		
		<table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Format:</td> <td>U30</td> </tr> </table> <p>This field contains a DWord offset from the corresponding SO buffer's Base Address value. The SOL stage uses this value as a write offset when performing writes to the buffer. The SOL stage will increment this value as a part of performing stream output to the buffer. Note that the SOL stage uses the buffer's Surface Pitch to advance the Write Offset, without regard to the buffer's Base Address (see Programming Notes above).</p>	Project:	BDW
Project:	BDW			
Format:	U30			
	1:0	Reserved		
		<table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ
Format:	MBZ			

Stream Synchronization

SSYNC - Stream Synchronization													
DWord	Bit	Description											
0	31:3	<p>Reserved</p> <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	BDW	Format:	MBZ							
Project:	BDW												
Format:	MBZ												
	2	<p>Stream Synchronization Bit 3</p> <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> </table> <p>when set to 1, block data from being sent on or received from the link. Each bit controls the associated Stream Descriptor; bit 0 corresponds to the first Stream Descriptor, etc. To synchronously start a set of DMA engines, the bits in the SSYNC register are first set to a 1. The RUN bits for the associated Stream Descriptors are then set to a 1 to start the DMA engines.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disable [Default]</td> <td>Sync Disabled for the stream 3</td> </tr> <tr> <td>1b</td> <td>Enable</td> <td>Sync Enabled for the stream 3</td> </tr> </tbody> </table> <p>Programming Notes</p> <p>When all streams are ready (FIFORDY=1), the associated SSYNC bits can all be set to 0 at the same time, and transmission or reception of bits to or from the link will begin together at the start of the next full link frame. To synchronously stop streams, first the bits are set in the SSYNC register, and then the individual RUN bits in the Stream Descriptors are cleared by software. The streams are numbered and the SSYNC bits assigned sequentially, based on their order in the register set. Bit 2: Output Stream 3</p>	Project:	BDW	Value	Name	Description	0b	Disable [Default]	Sync Disabled for the stream 3	1b	Enable	Sync Enabled for the stream 3
Project:	BDW												
Value	Name	Description											
0b	Disable [Default]	Sync Disabled for the stream 3											
1b	Enable	Sync Enabled for the stream 3											

SSYNC - Stream Synchronization

	1	<p>Stream Synchronization Bit 2</p> <p>when set to 1, block data from being sent on or received from the link. Each bit controls the associated Stream Descriptor; bit 0 corresponds to the first Stream Descriptor, etc. To synchronously start a set of DMA engines, the bits in the SSYNC register are first set to a 1. The RUN bits for the associated Stream Descriptors are then set to a 1 to start the DMA engines.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center; background-color: #e0e0ff;">Value</th><th style="text-align: center; background-color: #e0e0ff;">Name</th><th style="text-align: center; background-color: #e0e0ff;">Description</th></tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td><td style="text-align: center;">Disable [Default]</td><td>Sync Disabled for the stream 2</td></tr> <tr> <td style="text-align: center;">1b</td><td style="text-align: center;">Enable</td><td>Sync Enabled for the stream 2</td></tr> </tbody> </table> <p style="text-align: center;">Programming Notes</p> <p>When all streams are ready (FIFORDY=1), the associated SSYNC bits can all be set to 0 at the same time, and transmission or reception of bits to or from the link will begin together at the start of the next full link frame. To synchronously stop streams, first the bits are set in the SSYNC register, and then the individual RUN bits in the Stream Descriptors are cleared by software. The streams are numbered and the SSYNC bits assigned sequentially, based on their order in the register set. Bit 1: Output Stream 2</p>	Value	Name	Description	0b	Disable [Default]	Sync Disabled for the stream 2	1b	Enable	Sync Enabled for the stream 2
Value	Name	Description									
0b	Disable [Default]	Sync Disabled for the stream 2									
1b	Enable	Sync Enabled for the stream 2									
	0	<p>Stream Synchronization Bit 1</p> <p>when set to 1, block data from being sent on or received from the link. Each bit controls the associated Stream Descriptor; bit 0 corresponds to the first Stream Descriptor, etc. To synchronously start a set of DMA engines, the bits in the SSYNC register are first set to a 1. The RUN bits for the associated Stream Descriptors are then set to a 1 to start the DMA engines.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center; background-color: #e0e0ff;">Value</th><th style="text-align: center; background-color: #e0e0ff;">Name</th><th style="text-align: center; background-color: #e0e0ff;">Description</th></tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td><td style="text-align: center;">Disable [Default]</td><td>Sync Disabled for the stream 1</td></tr> <tr> <td style="text-align: center;">1b</td><td style="text-align: center;">Enable</td><td>Sync Enabled for the stream 1</td></tr> </tbody> </table> <p style="text-align: center;">Programming Notes</p> <p>When all streams are ready (FIFORDY=1), the associated SSYNC bits can all be set to 0 at the same time, and transmission or reception of bits to or from the link will begin together at the start of the next full link frame. To synchronously stop streams, first the bits are set in the SSYNC register, and then the individual RUN bits in the Stream Descriptors are cleared by software. The streams are numbered and the SSYNC bits assigned sequentially, based on their order in the register set. Bit 0: Output Stream 1</p>	Value	Name	Description	0b	Disable [Default]	Sync Disabled for the stream 1	1b	Enable	Sync Enabled for the stream 1
Value	Name	Description									
0b	Disable [Default]	Sync Disabled for the stream 1									
1b	Enable	Sync Enabled for the stream 1									

Subsystem Identification

SID2_0_2_0_PCI - Subsystem Identification						
Register Space:	PCI: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	16					
Address:	0002Eh					
This register is used to uniquely identify the subsystem where the PCI device resides.						
DWord	Bit	Description				
0	15:0	<p>Subsystem Identification</p> <table border="1"> <tr> <td>Default Value:</td><td>0000000000000000b</td></tr> <tr> <td>Access:</td><td>R/W Once</td></tr> </table> <p>This value is used to identify a particular subsystem. This field should be programmed by BIOS during boot-up. Once written, this register becomes Read_Only. This register can only be cleared by a Reset.</p>	Default Value:	0000000000000000b	Access:	R/W Once
Default Value:	0000000000000000b					
Access:	R/W Once					

Subsystem Vendor ID and SubSystem ID

SVID_SID - Subsystem Vendor ID and SubSystem ID						
Register Space: PCI: 0/3/0 Project: BDW Default Value: 0x00000000 Access: R/W Once Size (in bits): 32						
Address: 0002Ch-0002Fh Power: Always on Reset: global						
DWord	Bit	Description				
0	31:16	Subsystem ID <table border="1"> <tr> <td>Default Value:</td><td>0000h</td></tr> <tr> <td>Access:</td><td>R/W Once</td></tr> </table> No functionality.	Default Value:	0000h	Access:	R/W Once
Default Value:	0000h					
Access:	R/W Once					
15:0	Subsystem Vendor ID <table border="1"> <tr> <td>Default Value:</td><td>0000h</td></tr> <tr> <td>Access:</td><td>R/W Once</td></tr> </table> No functionality	Default Value:	0000h	Access:	R/W Once	
Default Value:	0000h					
Access:	R/W Once					

Subsystem Vendor Identification

SVID2_0_2_0_PCI - Subsystem Vendor Identification						
DWord	Bit	Description				
0	15:0	<p>Subsystem Vendor ID</p> <table border="1"> <tr> <td>Default Value:</td><td>0000000000000000b</td></tr> <tr> <td>Access:</td><td>R/W Once</td></tr> </table> <p>This value is used to identify the vendor of the subsystem. This register should be programmed by BIOS during boot-up. Once written, this register becomes Read_Only. This register can only be cleared by a Reset.</p>	Default Value:	0000000000000000b	Access:	R/W Once
Default Value:	0000000000000000b					
Access:	R/W Once					

Super Queue GFX cycle Options register

SQCFG - Super Queue GFX cycle Options register						
DWord	Bit	Description				
0	31:10	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO		
Access:	RO					
	9:3	<p>SQ Full Limit for Performance Monitor</p> <table border="1"> <tr> <td>Default Value:</td> <td>0110000b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Watermark for SQ Full Metrics This field sets a watermark where any SQ level above is considered as SQ FULL condition. This is added to compensate for the credit loop between the page walker and GTI which would make the number of active entries oscillate even the pipeline is backed up towards page walker. Range of allowed programming is 0-64. Default is 48.</p>	Default Value:	0110000b	Access:	R/W
Default Value:	0110000b					
Access:	R/W					
	2	<p>SQ Read-Only Port Reject Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>This indicates whether rejections can be issued from the Super Queue to GFX for read cycles on the Read Only port. Rejected cycles are retried at a later time by GFX. By default, read cycles that have a matching address elsewhere in the Super Queue are rejected, and GFX is notified of the rejection. If this bit is set, no rejections ever occur on the SQ-GFX interface. SQ accepts all requests, but in the case of a matching address, the SQ stalls the Read-Only port until the address match disappears (matching entry is retired by SQ). 1 = Rejections are disabled, SQ stalls if needed. 0 = Rejections are enabled.</p>	Access:	R/W		
Access:	R/W					

SQCFG - Super Queue GFX cycle Options register

	1	SQ Read Port GFX Read Ownership		
		<table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table>	Access:	R/W
Access:	R/W			
SQ Read Port GFX Read Ownership (SQRWO): SQ Read-Only Port GFX Read Ownership Indication. This indicates the type of request that is issued to uncore for each read cycle from the GFX Read-Only port which produces a miss in the MLC. By default, read cycles that have no matching MLC entry produce a regular read request from uncore through the IDI. If this bit is set, the request is changed from a regular read to a request for ownership (RFO) of the cacheline. This applies for all read requests from the GFX Read-Only port ONLY.				
		1 = All GFX reads from RO port require ownership of the cacheline. 0 = GFX reads from RO port do.		
	0	MSQD Poisoned Writes Propagation Enable		
		<table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table>	Access:	R/W
Access:	R/W			
		0: POISON propagation disabled i.e. MSQD always drives 0 to BGF (default mode). 1: POISON propagation enabled. Poison bit from writes are passed out to BGF.		

Super Queue Internal Cnt Register I

SQCNT1 - Super Queue Internal Cnt Register I				
SQ Internal Counter Register				
DWord	Bit	Description		
0	31:24	<p>RSVD</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
Access:	RO			
	23:20	<p>SQRWCQD</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Read-Write Request Queue Command Get Delay: This indicates the number of clocks that are inserted between each GFX cycle being accepted on the GFX Read or GFX Write ports. By default, this is disabled, which means that the RWRQ is able to accept one cycle per clock. By any other value, the RWRQ inserts the number of idle clocks listed in this register before accepting another cycle from GFX, essentially throttling the bandwidth. During each idle clock, RWRQ is guaranteed not to assert its command get to either read or write port.</p> <p>0000b = Disabled (no additional clocks added). 0001b = One idle clock inserted between command gets. 0010b = Two idle clocks inserted between command gets. ... 1111b = Fifteen idle clocks inserted between command gets.</p>	Access:	R/W
Access:	R/W			
	19:16	<p>SQCQD</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Read-Only Request Queue Command Get Delay: This indicates the number of clocks that are inserted between each GFX cycle being accepted on the GFX Read-Only port. By default, this is disabled, which means that the RORQ will be able to accept one cycle per clock. By any other value, the RORQ inserts the number of idle clocks listed in this register before accepting another cycle from GFX, essentially throttling the bandwidth. During each idle clock, RORQ is guaranteed not to assert its command get.</p> <p>0000b = Disabled (no additional clocks added). 0001b = One idle clock inserted between command gets. 0010b = Two idle clocks inserted between command gets. ... 1111b = Fifteen idle clocks inserted between command gets.</p>	Access:	R/W
Access:	R/W			

SQCNT1 - Super Queue Internal Cnt Register I

	15:10	SQDPTH				
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table>	Project:	BDW	Access:	R/W
Project:	BDW					
Access:	R/W					
		<p>Super Queue Depth:</p> <p>This indicates the maximum number of cycles supported at any given time by Super Queue. By default, this is 64, which is the maximum size of the Super Queue, but can be throttled back to support fewer GFX cycles.</p> <p>Note: By limiting the depth of the super queue, effectively the recycle queue limits the SQIDs that are allowed to be used.</p> <p>3Fh = SQ Depth of 63. 3Eh = SQ Depth of 62. ... 07h = SQ Depth of 7. 06h = SQ Depth of 6. 05h = SQ Depth of 5. 04h = SQ Depth of 4. 03h = SQ Depth of 3. 02h = SQ Depth of 2. 01h = Reserved. 00h = Disabled (SQ Depth of 64) (default).</p>				
<hr/>						
	9	RSVD				
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Project:	BDW	Access:	RO
Project:	BDW					
Access:	RO					
<hr/>						
	8:6	Reserved				
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> </table>	Project:	BDW		
Project:	BDW					
<hr/>						
	5:0	SQIDICNT				
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table>	Project:	BDW	Access:	R/W
Project:	BDW					
Access:	R/W					
<p>Outstanding SQ IDI Cycle Counter:</p> <p>This indicates the maximum number of outstanding cycles that are presented to IDI/uncore at any given time by Super Queue. By default, this is 64, but can be throttled back to support fewer IDI cycles.</p> <p>0 = Disabled (64). 1-63 = Max number of outstanding IDI cycles.</p>						
<table border="1"> <thead> <tr> <th>Programming Notes</th><th>Project</th></tr> </thead> <tbody> <tr> <td>For devices with 2 CPU Cores and Big graphics (GT3), such as BDW 2+3, the Driver should program this field to 36 decimal, to avoid overloading the IDI Ring and provide optimal performance.</td><td>BDW</td></tr> </tbody> </table>			Programming Notes	Project	For devices with 2 CPU Cores and Big graphics (GT3), such as BDW 2+3, the Driver should program this field to 36 decimal, to avoid overloading the IDI Ring and provide optimal performance.	BDW
Programming Notes	Project					
For devices with 2 CPU Cores and Big graphics (GT3), such as BDW 2+3, the Driver should program this field to 36 decimal, to avoid overloading the IDI Ring and provide optimal performance.	BDW					

Super Queue Internal Counters Register II

SQCNT2 - Super Queue Internal Counters Register II				
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x00000000 Size (in bits): 32				
Address: 09028h Super Queue Internal Counter register				
DWord	Bit	Description		
0	31:30	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO
	Access:	RO		
	29	Enable Promotion on Read <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Enable Promotion on Read Match: Enable the promotion of write request if matched with a Read request.</p>	Access:	R/W
	Access:	R/W		
	28	Priority 3 Pool Count Disable <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Priority3 Pool Count Disable: When set, priority3 pool becomes unlimited. And priority3 pool count value should not be used in reset of the remaining counters.</p>	Access:	R/W
	Access:	R/W		
27:25	Priority3 Pool Count: <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Priority3 Pool Count: The count of cycles is selected from priority3 pool before switching to lower priority pools. Count is used as the power of 2. 000b: 1 request 001b: 2 requests 010b: 4 requests 011b: 8 requests ... 111b: 128 requests </p>	Access:	R/W	
Access:	R/W			
24	Priority2 Pool Count Disable <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Priority2 Pool Count Disable: When set, priority2 pool becomes unlimited. And priority2 pool count value should not be used in reset of the remaining counters.</p>	Access:	R/W	
Access:	R/W			

SQCNT2 - Super Queue Internal Counters Register II

	23:21	Priority2 Pool count	
		Access:	R/W
<p>Priority2 Pool Count:</p> <p>The count of cycles is selected from priority2 pool before switching to lower priority pools. Count is used as the power of 2.</p> <p>000: 1 request 001: 2 requests 010: 4 requests 011: 8 requests ... 111: 128 requests</p>			
	20	Priority1 Pool Count Disable	
<p>Priority1 Pool Count Disable: When set, priority1 pool becomes unlimited. And priority1 pool count value should not be used in reset of the remaining counters.</p>			
	19:17	Priority1 Pool Count	
		Access:	R/W
<p>Priority1 Pool Count:</p> <p>The count of cycles is selected from priority1 pool before switching to lower priority pools. Count is used as the power of 2.</p> <p>000: 1 request 001: 2 requests 010: 4 requests 011: 8 requests ... 111: 128 requests</p>			
	16	Priority0 Pool Count Disable	
<p>Priority0 Pool Count Disable: When set, priority0 pool becomes unlimited. And priority0 pool count value should not be used in reset of the remaining counters.</p>			

SQCNT2 - Super Queue Internal Counters Register II

	15:13	Priority0 Pool Count	
		Access:	R/W
<p>Priority0 Pool Count:</p> <p>The count of cycles is selected from priority0 pool before switching to lower priority pools. Count is used as the power of 2.</p> <p>000: 1 request 001: 2 requests 010: 4 requests 011: 8 requests ... 111: 128 requests</p>			
	12	Enable Priority Selection	
		Access:	R/W
<p>Enable Priority Selection:</p> <p>Enables the use of priority bits coming from GFX core. If disabled, all slots in SQ are treated as same priority</p> <p>0b: Disabled (default). 1b: Enabled.</p>			
	11:8	Reserved	
		Project:	BDW
	7:0	LRU Hint counter	
		Access:	RO
<p>Reserved</p>			

SWF

SWF		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	4F000h-4F08Fh	
Name:	Software Flags	
ShortName:	SWF_*	
Valid Projects:	BDW	
Power:	Always on	
Reset:	soft	
These registers are used as scratch pad data storage space and have no direct effect on hardware operation. There are 36 instances of this register format.		
DWord	Bit	Description
0	31:0	Software Flags Software flags

System Validation (SV) Determinism Control Registers with Lock bit

SV_CTRL0 - System Validation (SV) Determinism Control Registers with Lock bit												
Register Space:	MMIO: 0/2/0											
Project:	BDW											
Default Value:	0x00000000											
Size (in bits):	32											
Address:	0A240h											
Lock bit SVCTRL_LOCK applies to all RW/L fields this register. These bits are not reset on FLR (device reset).												
DWord	Bit	Description										
0	31	Lock fo SV Control Registers <table border="1"> <tr> <td>Access:</td> <td>R/W Lock</td> </tr> <tr> <td colspan="2">Controls whether SV control registers are writeable.</td></tr> <tr> <td colspan="2">0: Registers are writeable.</td></tr> <tr> <td colspan="2">1: Registers cannot be written anymore.</td></tr> <tr> <td colspan="2">Lock bit cannot be cleared without cold reset (i.e., writing a 0 after a 1 was written does NOT clear the lock).</td></tr> </table>	Access:	R/W Lock	Controls whether SV control registers are writeable.		0: Registers are writeable.		1: Registers cannot be written anymore.		Lock bit cannot be cleared without cold reset (i.e., writing a 0 after a 1 was written does NOT clear the lock).	
Access:	R/W Lock											
Controls whether SV control registers are writeable.												
0: Registers are writeable.												
1: Registers cannot be written anymore.												
Lock bit cannot be cleared without cold reset (i.e., writing a 0 after a 1 was written does NOT clear the lock).												
30	Reserved											
29:6	Reserved											
5	Reserved											
4	Reserved											
3	Reserved											
2	Reserved											
1	Reserved											
0	Reserved											

Thread Dispatched Count Register

TDL_THR_DISP_COUNT - Thread Dispatched Count Register					
Register Space: MMIO: 0/2/0					
Project:	BDW				
Default Value:	0x00000000				
Access:	RO				
Size (in bits):	32				
Address:	0E4BCh				
Valid Projects:	[BDW]				
This register provides the count of threads dispatched/valid in the subslice.					
DWord	Bit	Description			
0	31:6	Reserved <table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ	
Format:	MBZ				
5:0	Thread Count <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0-56</td><td>Valid Range</td></tr> </tbody> </table>	Value	Name	0-56	Valid Range
Value	Name				
0-56	Valid Range				

Thread Faulted Count Register

TDL_THR_PF_COUNT - Thread Faulted Count Register					
DWord	Bit	Description			
0	31	Canonical fault indication bit to CS The bit is set when a canonical fault on data fetch is reported by EU.			
	30:6	Reserved Format: <input type="text"/> MBZ			
	5:0	Thread Count <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0-56</td> <td>Valid Range</td> </tr> </tbody> </table>	Value	Name	0-56
Value	Name				
0-56	Valid Range				

Thread Fault Status Register 0

TDL_THR_PF_STATUS0 - Thread Fault Status Register 0		
Register Space:	MMIO	0/2/0
Project:	BDW	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Address:	0E6B8h	
This register provides the status of each thread in the SubSlice. A bit set indicates the thread in the specific thread slot is faulted.		
DWord	Bit	Description
0	31:24	Row0, EU3, [Reserved, T6-T0]
	23:16	Row0, EU2, [Reserved, T6-T0]
	15:8	Row0, EU1, [Reserved, T6-T0]
	7:0	Row0, EU0, [Reserved, T6-T0]

Thread Fault Status Register 1

TDL_THR_PF_STATUS1 - Thread Fault Status Register 1		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Address:	0E7B8h	
This register provides the status of each thread in the SubSlice. A bit set indicates the thread in the specific thread slot is faulted.		
DWord	Bit	Description
0	31:24	Row1, EU3, [Reserved, T6-T0]
	23:16	Row1, EU2, [Reserved, T6-T0]
	15:8	Row1, EU1, [Reserved, T6-T0]
	7:0	Row1, EU0, [Reserved, T6-T0]

Thread Load Status Register 0

TDL_THR_STATUS0 - Thread Load Status Register 0		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Address:	0E4B8h	
This register provides the status of each thread in the SubSlice.		
DWord	Bit	Description
0	31:24	Row0, EU3, [Reserved, T6-T0]
	23:16	Row0, EU2, [Reserved, T6-T0]
	15:8	Row0, EU1, [Reserved, T6-T0]
	7:0	Row0, EU0, [Reserved, T6-T0]

Thread Load Status Register 1

TDL_THR_STATUS1 - Thread Load Status Register 1		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Address:	0E5B8h	
This register provides the status of each thread in the SubSlice. A bit set indicates a valid thread is loaded in the thread slot.		
DWord	Bit	Description
0	31:24	Row1, EU3, [Reserved, T6-T0]
	23:16	Row1, EU2, [Reserved, T6-T0]
	15:8	Row1, EU1, [Reserved, T6-T0]
	7:0	Row1, EU0, [Reserved, T6-T0]

Thread Mode Register

FF_MODE - Thread Mode Register

Register Space:	MMIO: 0/2/0
Project:	BDW
Source:	RenderCS 0x00A00000 [BDW]
Access:	R/W
Size (in bits):	32
Address:	020A0h
Valid Projects:	BDW

This register is used to program the FF shader Mode.

DWord	Bit	Description			
0	31	Reserved			
		Project:	BDW		
		Format:	MBZ		
	30	TDS external Cache Disable			
		Project:	BDW		
		Value	Name	Description	Project
		0b	Enable [Default]	The external TDS Cache is enabled if there is enough handles to enable the cache.	
		1b	Disable	The external TDS Cache is disabled even if there is enough handles to enable the cache. Only the internal TDS Cache will be used.	
	29:26	DS Hit Max Value			
		Format:	U4		
		Value	Name	Description	Project
		9	[Default]	If the number of hits reaches the DS Hit Max Value and there is a pending miss to be dispatched, the DS will dispatch the pending miss vertex as a single dispatch.	
		[1,9]		Programming the value beyond the range will have undefined behavior if DS Reference Count Full Force miss enable is 0. When DS Reference Count Full Force miss enable is 1 then the value can be [1, Fh].	BDW
		Value	Name	Description	Project
		9	[Default]		BDW
		[1,9]			BDW

FF_MODE - Thread Mode Register

	25:20	VS Hit Max Value									
		<table border="1"> <tr> <td>Format:</td><td>U6</td></tr> </table>	Format:	U6							
Format:	U6										
Description											
<p>If the number of hits reaches the VS Hit Max Value and there is a pending miss to be dispatched, the VS will dispatch the pending miss vertex as a single dispatch.</p> <p>Programming the value beyond the range will have undefined behavior if VS Reference Count Full Force miss enable is 0. When VS Reference Count Full Force miss enable is 1 then the value can be [1,3Fh].</p>											
		<table border="1"> <thead> <tr> <th style="text-align: center;">Value</th><th style="text-align: center;">Name</th></tr> </thead> <tbody> <tr> <td>10</td><td>[Default]</td></tr> <tr> <td>[1,26]</td><td></td></tr> </tbody> </table>	Value	Name	10	[Default]	[1,26]				
Value	Name										
10	[Default]										
[1,26]											
	19	DS Reference Count Full Force Miss Enable									
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>Enable</td></tr> </table>	Project:	BDW	Format:	Enable					
Project:	BDW										
Format:	Enable										
<table border="1"> <thead> <tr> <th style="text-align: center;">Value</th><th style="text-align: center;">Name</th><th style="text-align: center;">Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>[Default]</td><td>On a hit to the DS cache and the associated handle's reference count is full then stall until a dereference.</td></tr> <tr> <td>1b</td><td></td><td>On a hit to the DS cache and the associated handle's reference count is full then force the cycle as a miss and allocate a new handle.</td></tr> </tbody> </table>			Value	Name	Description	0b	[Default]	On a hit to the DS cache and the associated handle's reference count is full then stall until a dereference.	1b		On a hit to the DS cache and the associated handle's reference count is full then force the cycle as a miss and allocate a new handle.
Value	Name	Description									
0b	[Default]	On a hit to the DS cache and the associated handle's reference count is full then stall until a dereference.									
1b		On a hit to the DS cache and the associated handle's reference count is full then force the cycle as a miss and allocate a new handle.									
Programming Notes											
<p>To work around bugs, this must be set to 0.</p>											
	18	Reserved									
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	BDW	Format:	MBZ					
Project:	BDW										
Format:	MBZ										
	17:16	Reserved									
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	BDW	Format:	MBZ					
Project:	BDW										
Format:	MBZ										

FF_MODE - Thread Mode Register

	15	VS Reference Count Full Force Miss Enable		
		Project:	BDW	
		Format:	U1	
		Value	Name	Description
		[0,1]		
		0b	[Default]	On a hit to the VS cache and the associated handle's reference count is full then stall until a dereference.
		1b		On a hit to the VS cache and the associated handle's reference count is full then force the cycle as a miss and allocate a new handle.
		Programming Notes		Project
		To work around bugs, this must be set to 0.		BDW
	14:13	Reserved		
		Project:	BDW	
		Format:	MBZ	
	12	Reserved		
		Default Value:	0h	
		Project:	BDW	
		Format:	MBZ	
	11:7	Reserved		
		Format:	MBZ	
	6:5	Reserved		
		Project:	BDW	
		Format:	MBZ	
	4	Reserved		
		Default Value:	0h	
		Project:	BDW	
		Format:	MBZ	
	3:1	Reserved		
		Format:	MBZ	
	0	Reserved		
		Project:	BDW	
		Format:	MBZ	

TiledResources Invalid Tile Detection Register

TRINVTILEDETCT - TiledResources Invalid Tile Detection Register											
Register Space: MMIO: 0/2/0 Default Value: 0x00000000 Size (in bits): 32											
Address: 04DECh Name: TiledResources Invalid Tile Detection Register ShortName: TRINVTILEDETCT											
DWord	Bit	Description									
0	31:0	Invalid Tile Detection Value <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td><td style="padding: 2px; text-align: right;">R/W</td></tr> <tr> <th style="background-color: #e0e0e0; text-align: left; padding: 2px;">Value</th><th style="background-color: #e0e0e0; text-align: left; padding: 2px;">Name</th><th style="background-color: #e0e0e0; text-align: left; padding: 2px;">Description</th></tr> <tr> <td style="padding: 2px;">00000000h</td><td style="padding: 2px; text-align: center;">[Default]</td><td style="padding: 2px;">A 32bit value programmed to enable h/w to perform a match of TR-VA TT entries to detect Invalid Tiles. Hardware will flag each entry and space behind it as Invalid Tile for matched entries.</td></tr> </table>		Access:	R/W	Value	Name	Description	00000000h	[Default]	A 32bit value programmed to enable h/w to perform a match of TR-VA TT entries to detect Invalid Tiles. Hardware will flag each entry and space behind it as Invalid Tile for matched entries.
Access:	R/W										
Value	Name	Description									
00000000h	[Default]	A 32bit value programmed to enable h/w to perform a match of TR-VA TT entries to detect Invalid Tiles. Hardware will flag each entry and space behind it as Invalid Tile for matched entries.									

Tiled Resources Translation Table Control Registers

TRTTE - Tiled Resources Translation Table Control Registers								
DWord	Bit	Description						
0	31:2	Reserved						
		Access:	RO					
	1	<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00000000000000000000000000000000b</td> <td>[Default]</td> <td>Reserved</td> </tr> </tbody> </table>		Value	Name	Description	00000000000000000000000000000000b	[Default]
Value	Name	Description						
00000000000000000000000000000000b	[Default]	Reserved						
0	TR-VA Translation Table Memory Location Default Value: 0b Access: R/W This field specifies whether the translation tables for TR to VA are in virtual address space v/s physical (GPA) address space. 0: Tables are in Physical (GPA) space 1: Tables are in Virtual address space							
0	TR - TT Enable Default Value: 0b Access: R/W TR translation tables are disabled as default. This field needs to be enabled via s/w to get TR translation active.							

TiledResources VA Detection Registers

TRVADR - TiledResources VA Detection Registers										
DWord	Bit	Description								
0	31:8	<p>Reserved</p> <table border="1"> <tr> <td>Default Value:</td> <td>000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Default Value:	000000h	Access:	RO				
Default Value:	000000h									
Access:	RO									
	7:4	<p>TR - VA Mask Value</p> <table border="1"> <tr> <td>Default Value:</td> <td>0000b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>4bit MASK value that is mapped to incoming address bits[47:44] MASK bits are used to identify which address bits need to be considered for compare. If particular mask bit is "1", mapping address bit needs to be compared to DATA value provided. If "0", corresponding address bit is masked which makes it don't care for compare. (This field defaults to "0000" to disable detection.). Note: The only usage model for GFX driver to set this field to "1111". Behaviour of h/w for any other setting is not defined. Note: GFX driver shall use same TRVA MASK value for all contexts.</p>	Default Value:	0000b	Access:	R/W				
Default Value:	0000b									
Access:	R/W									
	3:0	<p>TR- VA Data Value</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0000b</td> <td>[Default]</td> <td> 4bit Data value that is mapped to incoming address bits[47:44]. Data bits are used to compare address values that are not filtered by the TRVAMV for match Note: GFX driver shall use same TRVA Data value for all contexts </td> </tr> </tbody> </table>	Access:	R/W	Value	Name	Description	0000b	[Default]	4bit Data value that is mapped to incoming address bits[47:44]. Data bits are used to compare address values that are not filtered by the TRVAMV for match Note: GFX driver shall use same TRVA Data value for all contexts
Access:	R/W									
Value	Name	Description								
0000b	[Default]	4bit Data value that is mapped to incoming address bits[47:44]. Data bits are used to compare address values that are not filtered by the TRVAMV for match Note: GFX driver shall use same TRVA Data value for all contexts								

Tiled Resources VA Translation Table L3 ptr - DW0

TRVATTL3PTRDW0 - Tiled Resources VA Translation Table L3 ptr - DW0							
Register Space:		MMIO: 0/2/0					
Default Value:		0x00000000					
Size (in bits):		32					
Address:		04DE0h					
Name:		Tiled Resources VA Translation Table L3 ptr - DW0					
ShortName:		TRVATTL3PTRDW0					
DWord	Bit	Description					
0	31:12	TR - VA transIn Table L3 Pointer (Lower Address)					
		<table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table>	Access:	R/W			
Access:	R/W						
11:0	<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>00000h</td><td>[Default]</td><td>Lower address bits for tiled resource VA to virtual address translation L3 table</td></tr> </tbody> </table>	Value	Name	Description	00000h	[Default]	Lower address bits for tiled resource VA to virtual address translation L3 table
Value	Name	Description					
00000h	[Default]	Lower address bits for tiled resource VA to virtual address translation L3 table					
	11:0	Reserved					
		<table border="1"> <tr> <td>Default Value:</td><td>000h</td></tr> </table>	Default Value:	000h			
Default Value:	000h						
<table border="1"> <tr> <td>Access:</td><td>RO</td></tr> </table>	Access:	RO					
Access:	RO						
Reserved							

Tiled Resources VA Translation Table L3 ptr - DW1

TRVATTL3PTRDW1 - Tiled Resources VA Translation Table L3 ptr - DW1										
DWord	Bit	Description								
0	31:16	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> <tr> <td>0000h</td><td>[Default]</td><td>Reserved</td></tr> </table>	Access:	RO	Value	Name	Description	0000h	[Default]	Reserved
Access:	RO									
Value	Name	Description								
0000h	[Default]	Reserved								
	15:0	<p>TR - VA transln Table L3 Pointer (Upper Address)</p> <table border="1"> <tr> <td>Default Value:</td> <td>0000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td colspan="2">Upper address bits for tiled resource VA to virtual address translation L3 table</td></tr> </table>	Default Value:	0000h	Access:	R/W	Upper address bits for tiled resource VA to virtual address translation L3 table			
Default Value:	0000h									
Access:	R/W									
Upper address bits for tiled resource VA to virtual address translation L3 table										

TIMESTAMP_CTR

TIMESTAMP_CTR		
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x00000000 Access: R/WC Size (in bits): 32		
Address: 44070h-44073h Name: Time Stamp Counter ShortName: TIMESTAMP_CTR Valid Projects: BDW Power: Always on Reset: global		
The register is not reset by an FLR.		
DWord	Bit	Description
0	31:0	TIMESTAMP Counter This field increments every microsecond. The value in this field is latched in the Pipe Flip TIMESTAMP registers when flips occur, and in the Pipe Frame TIMESTAMP registers at start of vertical blank. The register value will reset if any value is written to it. The register is not reset by an FLR.

TLB_RD_ADDRESS Register

TLB_RD_ADDR - TLB_RD_ADDRESS Register					
DWord	Bit	Description			
0	31:12	Reserved			
		<table border="1"> <tr> <td>Default Value:</td><td>000000000000000000000000b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	000000000000000000000000b	Access:
Default Value:	000000000000000000000000b				
Access:	RO				
	11:0	Reserved			

TLB_RD_DATA0 Register

TLB_RD_DATA0 - TLB_RD_DATA0 Register								
DWord	Bit	Description						
0	31:0	<p>TLB_READ_DATA0 Register</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> <tr> <td colspan="2">address [43:12]</td></tr> </table>	Default Value:	00000000h	Access:	RO	address [43:12]	
Default Value:	00000000h							
Access:	RO							
address [43:12]								

TLB_RD_DATA1 Register

TLB_RD_DATA1 - TLB_RD_DATA1 Register								
DWord	Bit	Description						
0	31:0	TLB_READ_DATA1 Register <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> <tr> <td colspan="2"> Bit[31:5] Reserved Bit[4] Cycle GTT SEL (1-GGTT Cycle, 0-PPGTT Cycle) Bit[3:0] address [47:44] </td></tr> </table>	Default Value:	00000000h	Access:	RO	Bit[31:5] Reserved Bit[4] Cycle GTT SEL (1-GGTT Cycle, 0-PPGTT Cycle) Bit[3:0] address [47:44]	
Default Value:	00000000h							
Access:	RO							
Bit[31:5] Reserved Bit[4] Cycle GTT SEL (1-GGTT Cycle, 0-PPGTT Cycle) Bit[3:0] address [47:44]								

TRANS_CLK_SEL

TRANS_CLK_SEL		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	46140h-46143h	
Name:	Transcoder A Clock Select	
ShortName:	TRANS_CLK_SEL_A	
Valid Projects:	BDW	
Power:	Always on	
Reset:	soft	
Address:	46144h-46147h	
Name:	Transcoder B Clock Select	
ShortName:	TRANS_CLK_SEL_B	
Valid Projects:	BDW	
Power:	Always on	
Reset:	soft	
Address:	46148h-4614Bh	
Name:	Transcoder C Clock Select	
ShortName:	TRANS_CLK_SEL_C	
Valid Projects:	BDW	
Power:	Always on	
Reset:	soft	
Description		
This register maps the port clock to the transcoder. There is one instance of this register format per transcoder A/B/C.		
DWord	Bit	Description

TRANS_CLK_SEL																							
0	31:29	<p>Trans Clock Select Select which PLL to use for this transcoder. Transcoder EDP always uses DDIA clock.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>000b</td><td>None</td><td>No PLL selected. Clock is disabled for this transcoder.</td></tr> <tr> <td>010b</td><td>DDIB</td><td>Select DDIB clock</td></tr> <tr> <td>011b</td><td>DDIC</td><td>Select DDIC clock</td></tr> <tr> <td>100b</td><td>DDID</td><td>Select DDID clock. [BDW] Not supported on BDW ULT systems.</td></tr> <tr> <td>101b</td><td>DDIE</td><td>Select DDIE clock</td></tr> <tr> <td>Others</td><td>Reserved</td><td>Reserved</td></tr> </tbody> </table> <p>Restriction This must not be changed while the transcoder is enabled.</p>	Value	Name	Description	000b	None	No PLL selected. Clock is disabled for this transcoder.	010b	DDIB	Select DDIB clock	011b	DDIC	Select DDIC clock	100b	DDID	Select DDID clock. [BDW] Not supported on BDW ULT systems.	101b	DDIE	Select DDIE clock	Others	Reserved	Reserved
Value	Name	Description																					
000b	None	No PLL selected. Clock is disabled for this transcoder.																					
010b	DDIB	Select DDIB clock																					
011b	DDIC	Select DDIC clock																					
100b	DDID	Select DDID clock. [BDW] Not supported on BDW ULT systems.																					
101b	DDIE	Select DDIE clock																					
Others	Reserved	Reserved																					
	28:0	Reserved																					

TRANS_CONF

TRANS_CONF		
DWord	Bit	Description
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Access:	Double Buffered	
Size (in bits):	32	
Double Buffer Update Point:	Start of vertical blank (WD cap sync) OR transcoder disabled	
Address:	70008h-7000Bh	
Name:	Transcoder A Configuration	
ShortName:	TRANS_CONF_A	
Valid Projects:	BDW	
Power:	off/on	
Reset:	soft	
Address:	71008h-7100Bh	
Name:	Transcoder B Configuration	
ShortName:	TRANS_CONF_B	
Valid Projects:	BDW	
Power:	off/on	
Reset:	soft	
Address:	72008h-7200Bh	
Name:	Transcoder C Configuration	
ShortName:	TRANS_CONF_C	
Valid Projects:	BDW	
Power:	off/on	
Reset:	soft	
Address:	7F008h-7F00Bh	
Name:	Transcoder EDP Configuration	
ShortName:	TRANS_CONF_EDP	
Valid Projects:	BDW	
Power:	Always on	
Reset:	soft	

TRANS_CONF

TRANS_CONF																	
0	31	<p>Transcoder Enable Setting this bit to the value of one, turns on this transcoder. Turning the transcoder off disables the timing generator and synchronization pulses to the display will not be maintained. Enabling the transcoder may be internally delayed for one frame while the display data buffers are re-configured.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center; background-color: #e0e0ff;">Value</th><th style="text-align: center; background-color: #e0e0ff;">Name</th></tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td><td>Disable</td></tr> <tr> <td style="text-align: center;">1b</td><td>Enable</td></tr> </tbody> </table> <p>Restriction Timing registers must contain valid values before this bit is enabled.</p>	Value	Name	0b	Disable	1b	Enable									
Value	Name																
0b	Disable																
1b	Enable																
30		<p>Transcoder State Access: RO This read only bit indicates the actual state of the transcoder.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center; background-color: #e0e0ff;">Value</th><th style="text-align: center; background-color: #e0e0ff;">Name</th></tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td><td>Disabled</td></tr> <tr> <td style="text-align: center;">1b</td><td>Enabled</td></tr> </tbody> </table> <p>Workaround Project Workaround : The transcoder state may incorrectly show it is enabled before the transcoder has been enabled for the first time after a reset. That should not impact the normal usage of this field during the mode set disable sequence. BDW</p>	Value	Name	0b	Disabled	1b	Enabled									
Value	Name																
0b	Disabled																
1b	Enabled																
29:23		Reserved															
22:21		<p>Interlaced Mode These bits control the transcoder interlaced mode. This field is ignored by WD.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center; background-color: #e0e0ff;">Value</th><th style="text-align: center; background-color: #e0e0ff;">Name</th><th style="text-align: center; background-color: #e0e0ff;">Description</th></tr> </thead> <tbody> <tr> <td style="text-align: center;">00b</td><td>PF-PD</td><td>Progressive Fetch with Progressive Display</td></tr> <tr> <td style="text-align: center;">01b</td><td>PF-ID</td><td>Progressive Fetch with Interlaced Display</td></tr> <tr> <td style="text-align: center;">11b</td><td>IF-ID</td><td>Interlaced Fetch with Interlaced Display</td></tr> <tr> <td style="text-align: center;">Others</td><td>Reserved</td><td>Reserved</td></tr> </tbody> </table> <p>Restriction VGA display modes do not work while in interlaced fetch mode. Progressive Fetch with Interlaced Display requires the pipe scaler to be functioning with the 7x5 filter. Progressive Fetch with Interlaced Display effectively down scales the vertical by 2X, which reduces the maximum supported pixel rate by half.</p>	Value	Name	Description	00b	PF-PD	Progressive Fetch with Progressive Display	01b	PF-ID	Progressive Fetch with Interlaced Display	11b	IF-ID	Interlaced Fetch with Interlaced Display	Others	Reserved	Reserved
Value	Name	Description															
00b	PF-PD	Progressive Fetch with Progressive Display															
01b	PF-ID	Progressive Fetch with Interlaced Display															
11b	IF-ID	Interlaced Fetch with Interlaced Display															
Others	Reserved	Reserved															
20:7		Reserved															
6:0		Format: MBZ															

TRANS_CONF

		Project:	BDW
		Format:	MBZ

TRANS_CONF

TRANS_CONF														
Register Space: MMIO: 0/2/0 Project: DevLPT:H Default Value: 0x00000000 Access: R/W Size (in bits): 32 Double Buffer Update Point: Start of vertical blank OR transcoder disabled														
Address: F0008h-F000Bh Name: Transcoder A Config ShortName: TRANS_CONF_A Power: Always on Reset: soft														
DWord	Bit	Description												
0	31	Transcoder Enable Setting this bit to the value of one, turns on the transcoder. Turning the transcoder off disables the timing generator and synchronization pulses to the display will not be maintained. Transcoder timing registers must contain valid values before this bit is enabled. <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Disable</td><td>Disabled</td></tr> <tr> <td>1b</td><td>Enable</td><td>Enabled</td></tr> </tbody> </table>	Value	Name	Description	0b	Disable	Disabled	1b	Enable	Enabled			
Value	Name	Description												
0b	Disable	Disabled												
1b	Enable	Enabled												
	30	Transcoder State <table border="1"> <tr> <td>Access:</td><td>RO</td></tr> </table> This read only bit indicates the actual state of the transcoder. Since there can be some delay between disabling the transcoder and the transcoder actually shutting off, this bit indicates the true current state of the transcoder. <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Disabled</td><td>Transcoder is disabled</td></tr> <tr> <td>1b</td><td>Enabled</td><td>Transcoder is enabled</td></tr> </tbody> </table>	Access:	RO	Value	Name	Description	0b	Disabled	Transcoder is disabled	1b	Enabled	Transcoder is enabled	
Access:	RO													
Value	Name	Description												
0b	Disabled	Transcoder is disabled												
1b	Enabled	Transcoder is enabled												
	29:24	Reserved <table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ										
Format:	MBZ													
	23:21	Interlaced Mode These bits are used for control of the transcoder interlaced mode. <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>000b</td><td>Progressive</td><td>Progressive</td></tr> <tr> <td>011b</td><td>Interlaced</td><td>Interlaced (north display must also be set to interlaced)</td></tr> <tr> <td>Others</td><td>Reserved</td><td>Reserved</td></tr> </tbody> </table>	Value	Name	Description	000b	Progressive	Progressive	011b	Interlaced	Interlaced (north display must also be set to interlaced)	Others	Reserved	Reserved
Value	Name	Description												
000b	Progressive	Progressive												
011b	Interlaced	Interlaced (north display must also be set to interlaced)												
Others	Reserved	Reserved												

TRANS_CONF

	20:0	Reserved	Format:	MBZ
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TRANS_DDI_FUNC_CTL

TRANS_DDI_FUNC_CTL		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00030000	
Access:	R/W	
Size (in bits):	32	
Address:	60400h-60403h	
Name:	Transcoder A DDI Function Control	
ShortName:	TRANS_DDI_FUNC_CTL_A	
Valid Projects:	BDW	
Power:	off/on	
Reset:	soft	
Address:	61400h-61403h	
Name:	Transcoder B DDI Function Control	
ShortName:	TRANS_DDI_FUNC_CTL_B	
Valid Projects:	BDW	
Power:	off/on	
Reset:	soft	
Address:	62400h-62403h	
Name:	Transcoder C DDI Function Control	
ShortName:	TRANS_DDI_FUNC_CTL_C	
Valid Projects:	BDW	
Power:	off/on	
Reset:	soft	
Address:	6F400h-6F403h	
Name:	Transcoder EDP DDI Function Control	
ShortName:	TRANS_DDI_FUNC_CTL_EDP	
Valid Projects:	BDW	
Power:	Always on	
Reset:	soft	
Description		
There is one instance of this register per each transcoder A/B/C/EDP.		
DWord	Bit	Description

TRANS_DDI_FUNC_CTL																														
0	31	<p>TRANS DDI Function Enable This bit enables the transcoder DDI function.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Disable</td></tr> <tr> <td>1b</td><td>Enable</td></tr> </tbody> </table>	Value	Name	0b	Disable	1b	Enable																						
Value	Name																													
0b	Disable																													
1b	Enable																													
	30:28	<p>DDI Select These bits determine which DDI port this transcoder will connect to. It is not valid to enable and direct more than one transcoder to one DDI, except when using DisplayPort multistreaming. These bits are ignored by transcoder EDP since it can only connect to DDI A (EDP DDI).</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th><th>Programming Notes</th></tr> </thead> <tbody> <tr> <td>000b</td><td>None</td><td>No port connected</td><td></td></tr> <tr> <td>001b</td><td>DDI B</td><td>DDI B</td><td></td></tr> <tr> <td>010b</td><td>DDI C</td><td>DDI C</td><td></td></tr> <tr> <td>011b</td><td>DDI D</td><td>DDI D</td><td>[BDW] Do not select on ULT or ULX. DDI D is not supported for ULT or ULX and must not be selected.</td></tr> <tr> <td>100b</td><td>DDI E</td><td>DDI E</td><td></td></tr> <tr> <td>Others</td><td>Reserved</td><td>Reserved</td><td></td></tr> </tbody> </table> <p>Restriction This field must not be changed while the function is enabled.</p>	Value	Name	Description	Programming Notes	000b	None	No port connected		001b	DDI B	DDI B		010b	DDI C	DDI C		011b	DDI D	DDI D	[BDW] Do not select on ULT or ULX. DDI D is not supported for ULT or ULX and must not be selected.	100b	DDI E	DDI E		Others	Reserved	Reserved	
Value	Name	Description	Programming Notes																											
000b	None	No port connected																												
001b	DDI B	DDI B																												
010b	DDI C	DDI C																												
011b	DDI D	DDI D	[BDW] Do not select on ULT or ULX. DDI D is not supported for ULT or ULX and must not be selected.																											
100b	DDI E	DDI E																												
Others	Reserved	Reserved																												
	27	<p>Reserved</p> <table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ																										
Format:	MBZ																													

TRANS_DDI_FUNC_CTL

	26:24	TRANS DDI Mode Select																						
<p>This field determines the mode of operation. HDMI mode enables a null packet (32 bytes of a value of 0) to be sent when Vsync=1, and also enables preambles and guardbands prior to the null packets, in accordance with the HDMI specification. DVI mode will function as HDMI if DIP packets or audio are enabled.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center; background-color: #e0e0ff;">Value</th> <th style="text-align: center; background-color: #e0e0ff;">Name</th> <th style="text-align: center; background-color: #e0e0ff;">Description</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">000b</td><td>HDMI</td><td>Function in HDMI mode</td></tr> <tr> <td style="text-align: center;">001b</td><td>DVI</td><td>Function in DVI mode</td></tr> <tr> <td style="text-align: center;">010b</td><td>DP SST</td><td>Function in DisplayPort SST mode</td></tr> <tr> <td style="text-align: center;">011b</td><td>DP MST</td><td>Function in DisplayPort MST mode</td></tr> <tr> <td style="text-align: center;">100b</td><td>FDI</td><td>Function in FDI mode</td></tr> <tr> <td style="text-align: center;">Others</td><td>Reserved</td><td>Reserved</td></tr> </tbody> </table> <p>Restriction</p> <p>This field must not be changed while the function is enabled. The DisplayPort mode (SST or MST) selected here must match the mode selected in the DisplayPort Transport Control register for the transport attached to this transcoder. Transcoder EDP and DDI A can only function in DP SST mode.</p> <p>Only DDI E is allowed to operate in FDI mode. DDI E can only function in DP SST mode or FDI mode.</p>	Value	Name	Description	000b	HDMI	Function in HDMI mode	001b	DVI	Function in DVI mode	010b	DP SST	Function in DisplayPort SST mode	011b	DP MST	Function in DisplayPort MST mode	100b	FDI	Function in FDI mode	Others	Reserved	Reserved			
Value	Name	Description																						
000b	HDMI	Function in HDMI mode																						
001b	DVI	Function in DVI mode																						
010b	DP SST	Function in DisplayPort SST mode																						
011b	DP MST	Function in DisplayPort MST mode																						
100b	FDI	Function in FDI mode																						
Others	Reserved	Reserved																						
	23	Reserved																						
<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Project:</td> <td style="width: 50%;">BDW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	BDW	Format:	MBZ																				
Project:	BDW																							
Format:	MBZ																							
	22:20	Bits Per Color																						
<p>This field selects the number of bits per color output on the DDI connected to this transcoder. Dithering should be enabled when selecting a pixel color depth higher or lower than the pixel color depth of the frame buffer.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center; background-color: #e0e0ff;">Value</th> <th style="text-align: center; background-color: #e0e0ff;">Name</th> <th style="text-align: center; background-color: #e0e0ff;">Description</th> <th style="text-align: center; background-color: #e0e0ff;">Programming Notes</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">000b</td><td>8 bpc</td><td></td><td></td></tr> <tr> <td style="text-align: center;">001b</td><td>10 bpc</td><td></td><td>Not supported by HDMI or DVI</td></tr> <tr> <td style="text-align: center;">010b</td><td>6 bpc</td><td></td><td>Not supported by HDMI or DVI</td></tr> <tr> <td style="text-align: center;">011b</td><td>12 bpc</td><td></td><td></td></tr> <tr> <td style="text-align: center;">Others</td><td>Reserved</td><td>Reserved</td><td></td></tr> </tbody> </table> <p>Restriction</p> <p>This field must not be changed while the function is enabled.</p>	Value	Name	Description	Programming Notes	000b	8 bpc			001b	10 bpc		Not supported by HDMI or DVI	010b	6 bpc		Not supported by HDMI or DVI	011b	12 bpc			Others	Reserved	Reserved	
Value	Name	Description	Programming Notes																					
000b	8 bpc																							
001b	10 bpc		Not supported by HDMI or DVI																					
010b	6 bpc		Not supported by HDMI or DVI																					
011b	12 bpc																							
Others	Reserved	Reserved																						

TRANS_DDI_FUNC_CTL

	19:18	Port Sync Mode Master Select															
		<table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> </table> <p>This field indicates which transcoder will be the master to this transcoder when in port sync mode. This bit is ignored by transcoder EDP since it cannot be slaved to another port.</p>	Project:	BDW													
Project:	BDW																
		<table border="1"> <thead> <tr> <th style="background-color: #d9e1f2;">Value</th> <th style="background-color: #d9e1f2;">Name</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>Transcoder EDP</td> </tr> <tr> <td>01b</td> <td>Transcoder A</td> </tr> <tr> <td>10b</td> <td>Transcoder B</td> </tr> <tr> <td>11b</td> <td>Transcoder C</td> </tr> </tbody> </table>			Value	Name	00b	Transcoder EDP	01b	Transcoder A	10b	Transcoder B	11b	Transcoder C			
Value	Name																
00b	Transcoder EDP																
01b	Transcoder A																
10b	Transcoder B																
11b	Transcoder C																
		Restriction															
		A port cannot be slaved to itself.															
	17:16	Sync Polarity															
		This field indicates the polarity of Hsync and Vsync.															
		<table border="1"> <thead> <tr> <th style="background-color: #d9e1f2;">Value</th> <th style="background-color: #d9e1f2;">Name</th> <th style="background-color: #d9e1f2;">Description</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>Low</td> <td>VS and HS are active low (inverted)</td> </tr> <tr> <td>01b</td> <td>VS Low, HS High</td> <td>VS is active low (inverted), HS is active high</td> </tr> <tr> <td>10b</td> <td>VS High, HS Low</td> <td>VS is active high, HS is active low (inverted)</td> </tr> <tr> <td>11b</td> <td>High [Default]</td> <td>VS and HS are active high</td> </tr> </tbody> </table>	Value	Name	Description	00b	Low	VS and HS are active low (inverted)	01b	VS Low, HS High	VS is active low (inverted), HS is active high	10b	VS High, HS Low	VS is active high, HS is active low (inverted)	11b	High [Default]	VS and HS are active high
Value	Name	Description															
00b	Low	VS and HS are active low (inverted)															
01b	VS Low, HS High	VS is active low (inverted), HS is active high															
10b	VS High, HS Low	VS is active high, HS is active low (inverted)															
11b	High [Default]	VS and HS are active high															

TRANS_DDI_FUNC_CTL

	15	Port Sync Mode Enable						
		<table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> </table>	Project:	BDW				
Project:	BDW							
<p>This field enables the DisplayPort SST port sync mode on this transcoder. This mode forces two or more transcoders to be in sync with one transcoder master and one or more transcoder slaves. The master is unaware that it is operating in this mode. Only the slave is aware that it is operating in this mode. Port sync mode is only enabled in the slave transcoder. This bit is ignored by transcoder EDP since it cannot be slaved to another port.</p> <table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td> <td>Disable</td> </tr> <tr> <td style="text-align: center;">1b</td> <td>Enable</td> </tr> </tbody> </table>			Value	Name	0b	Disable	1b	Enable
Value	Name							
0b	Disable							
1b	Enable							
<p>Workaround</p> <p>Program register 45280h bits 2:1 = 11b before enabling Port Sync Mode and keep them at those values while Port Sync Mode is enabled. The bits should be restored after Port Sync Mode is disabled.</p>								
		<p>Restriction</p> <p>Follow the instructions for enabling and disabling Sync Mode in the Display Mode Set Sequence - Sequence for DisplayPort. Port Sync Mode must only be enabled with DisplayPort SST. Port Sync Mode Master Select must be programmed with a valid value when Port sync Mode is enabled. The slave and master transcoders and associated ports must have identical parameters and properties. They must be connected to the same PLL, have the same color format, link width (number of lanes enabled), resolution, refresh rate, dot clock, TU size, M and N programming, etc.</p>						
	14:12	Reserved						
		<p>Restriction</p> <p>This field must not be changed while the function is enabled. It is not valid to have the same pipes driving multiple enabled transcoders.</p>						
	11:10	Reserved						
		<table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ				
Format:	MBZ							
	9	Reserved						
	8	DP VC Payload Allocate						
		<p>This bit enables DisplayPort Virtual Channel payload allocation. This bit is ignored by transcoder EDP since it does not support multistreaming.</p> <table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td> <td>Disable</td> </tr> <tr> <td style="text-align: center;">1b</td> <td>Enable</td> </tr> </tbody> </table>	Value	Name	0b	Disable	1b	Enable
Value	Name							
0b	Disable							
1b	Enable							
	7:6	Reserved						
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Project:	BDW							
Format:	MBZ							

TRANS_DDI_FUNC_CTL																	
	5	Reserved															
	4	Reserved															
		Project: BDW															
		Format: MBZ															
	3:1	DP Port Width Selection															
		Project: BDW															
		<table border="1"> <thead> <tr> <th>Description</th><th>Project</th></tr> </thead> <tbody> <tr> <td>This bit selects the number of lanes to be enabled on the DDI link for DisplayPort or FDI.</td><td>BDW</td></tr> <tr> <td>This field is ignored for HDMI and DVI which always use all 4 lanes.</td><td></td></tr> </tbody> </table>	Description	Project	This bit selects the number of lanes to be enabled on the DDI link for DisplayPort or FDI.	BDW	This field is ignored for HDMI and DVI which always use all 4 lanes.										
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Value	Name	Description															
000b	x1	x1 Mode															
001b	x2	x2 Mode															
011b	x4	x4 Mode (not allowed with DDI-E, some restrictions with DDI-A)															
Others	Reserved	Reserved															
		<table border="1"> <thead> <tr> <th>Restriction</th><th>Project</th></tr> </thead> <tbody> <tr> <td>When in DisplayPort or FDI modes the value selected here must match the value selected in the DDI Buffer Control register for the DDI attached to this pipe.</td><td>BDW</td></tr> <tr> <td>This field must not be changed while the DDI is enabled. DDI E only supports x1 and x2 when DDI_BUF_CTL_A DDIA Lane Capability Control is set to DDIA x2, otherwise DDI E is not supported. DDI A (EDP) supports x1, x2, and x4 when DDI_BUF_CTL_A DDIA Lane Capability Control is set to DDIA x4, otherwise DDI A only supports x1 and x2.</td><td></td></tr> </tbody> </table>	Restriction	Project	When in DisplayPort or FDI modes the value selected here must match the value selected in the DDI Buffer Control register for the DDI attached to this pipe.	BDW	This field must not be changed while the DDI is enabled. DDI E only supports x1 and x2 when DDI_BUF_CTL_A DDIA Lane Capability Control is set to DDIA x2, otherwise DDI E is not supported. DDI A (EDP) supports x1, x2, and x4 when DDI_BUF_CTL_A DDIA Lane Capability Control is set to DDIA x4, otherwise DDI A only supports x1 and x2.										
Restriction	Project																
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	0	Reserved															
		Project: BDW															
		Format: MBZ															

TRANS_FRM_TIME

TRANS_FRM_TIME										
Register Space:	MMIO: 0/2/0									
Project:	BDW									
Default Value:	0x00000000									
Access:	R/W									
Size (in bits):	32									
Address:	6E020h-6E023h									
Name:	Transcoder WD0 Frame Time									
ShortName:	TRANS_FRM_TIME_WD0									
Valid Projects:	BDW									
Power:	off/on									
Reset:	soft									
This register is only for WD transcoders.										
Programming Notes										
Examples: For 60Hz the frame time is 16,666.66us, program integer 16,665 and fraction 2/3. For 24Hz the frame time is 41,666.66us, program integer 41,665 and fraction 2/3. For 59.94Hz the frame time is 16,683.33us, program integer 16,682 and fraction 1/3.										
Restriction		Project								
This register should not be changed while the transcoder or port are enabled.		BDW								
DWord	Bit	Description								
0	31:16	Frame Time Integer This field specifies the integer portion of the time in microseconds for a display frame. This is used to determine the rate at which to generate frames when capturing display. This field is programmed to the integer number of microseconds desired minus one.								
		<table border="1"> <thead> <tr> <th>Restriction</th> </tr> </thead> <tbody> <tr> <td>A value of 0 is invalid when the transcoder is enabled.</td></tr> </tbody> </table>	Restriction	A value of 0 is invalid when the transcoder is enabled.						
Restriction										
A value of 0 is invalid when the transcoder is enabled.										
	15:14	Frame Time Fraction This field specifies the fractional portion of the time in microseconds for a display frame. This is used to determine the rate at which to generate frames when capturing display.								
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>00b</td><td>0</td></tr> <tr> <td>01b</td><td>1/3</td></tr> <tr> <td>10b</td><td>2/3</td></tr> <tr> <td>Others</td><td>Reserved</td></tr> </tbody> </table>	Value	Name	00b	0	01b	1/3	10b	2/3
Value	Name									
00b	0									
01b	1/3									
10b	2/3									
Others	Reserved									
	13:0	Reserved								

TRANS_HBLANK

TRANS_HBLANK		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	60004h-60007h	
Name:	Transcoder A Horizontal Blank	
ShortName:	TRANS_HBLANK_A	
Valid Projects:	BDW	
Power:	off/on	
Reset:	soft	
Address:	61004h-61007h	
Name:	Transcoder B Horizontal Blank	
ShortName:	TRANS_HBLANK_B	
Valid Projects:	BDW	
Power:	off/on	
Reset:	soft	
Address:	62004h-62007h	
Name:	Transcoder C Horizontal Blank	
ShortName:	TRANS_HBLANK_C	
Valid Projects:	BDW	
Power:	off/on	
Reset:	soft	
Address:	6F004h-6F007h	
Name:	Transcoder EDP Horizontal Blank	
ShortName:	TRANS_HBLANK_EDP	
Valid Projects:	BDW	
Power:	Always on	
Reset:	soft	
There is one instance of this register for each transcoder A/B/C/EDP.		
Restriction		
This register should not be changed while the transcoder or port are enabled.		
DWord	Bit	Description
0	31:29	Reserved

TRANS_HBLANK		
	28:16	Horizontal Blank End This field specifies Horizontal Blank End position relative to the horizontal active display start.
		Restriction
		The minimum horizontal blank size is 32 pixels. For HDMI Audio transmission the minimum is 138 pixels. This register must always be programmed to the same value as the Horizontal Total.
	15:13	Reserved
	12:0	Horizontal Blank Start This field specifies the Horizontal Blank Start position relative to the horizontal active display start.
		Restriction
		This register must always be programmed to the same value as the Horizontal Active.
		In FDI mode bit 12 must not be set.

TRANS_HSYNC

TRANS_HSYNC		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	60008h-6000Bh	
Name:	Transcoder A Horizontal Sync	
ShortName:	TRANS_HSYNC_A	
Valid Projects:	BDW	
Power:	off/on	
Reset:	soft	
Address:	61008h-6100Bh	
Name:	Transcoder B Horizontal Sync	
ShortName:	TRANS_HSYNC_B	
Valid Projects:	BDW	
Power:	off/on	
Reset:	soft	
Address:	62008h-6200Bh	
Name:	Transcoder C Horizontal Sync	
ShortName:	TRANS_HSYNC_C	
Valid Projects:	BDW	
Power:	off/on	
Reset:	soft	
Address:	6F008h-6F00Bh	
Name:	Transcoder EDP Horizontal Sync	
ShortName:	TRANS_HSYNC_EDP	
Valid Projects:	BDW	
Power:	Always on	
Reset:	soft	
Description		
There is one instance of this register for each transcoder A/B/C/EDP.		
Restriction		
This register should not be changed while the transcoder or port are enabled.		
DWord	Bit	Description

TRANS_HSYNC					
0	31:29	Reserved			
		Format:	MBZ		
	28:16	Horizontal Sync End	This field specifies the Horizontal Sync End position relative to the horizontal active display start. It is programmed with HorizontalActive+FrontPorch+Sync-1		
			Restriction		
			This value must be greater than the horizontal sync start and less than Horizontal Total.		
	15:13	Reserved			
		Format:	MBZ		
	12:0	Horizontal Sync Start	This field specifies the Horizontal Sync Start position relative to the horizontal active display start. It is programmed with HorizontalActive + FrontPorch - 1		
			Restriction		
			This value must be greater than Horizontal Active. In HDMI modes the minimum gap between horizontal blank start and horizontal sync start is 16 pixels.		

TRANS_HTOTAL

TRANS_HTOTAL	
Register Space:	MMIO: 0/2/0
Project:	BDW
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	60000h-60003h
Name:	Transcoder A Horizontal Total
ShortName:	TRANS_HTOTAL_A
Valid Projects:	BDW
Power:	off/on
Reset:	soft
Address:	61000h-61003h
Name:	Transcoder B Horizontal Total
ShortName:	TRANS_HTOTAL_B
Valid Projects:	BDW
Power:	off/on
Reset:	soft
Address:	62000h-62003h
Name:	Transcoder C Horizontal Total
ShortName:	TRANS_HTOTAL_C
Valid Projects:	BDW
Power:	off/on
Reset:	soft
Address:	6E000h-6E003h
Name:	Transcoder WD0 Horizontal Total
ShortName:	TRANS_HTOTAL_WD0
Valid Projects:	BDW
Power:	off/on
Reset:	soft
Address:	6F000h-6F003h
Name:	Transcoder EDP Horizontal Total
ShortName:	TRANS_HTOTAL_EDP
Valid Projects:	BDW
Power:	Always on
Reset:	soft

TRANS_HTOTAL

Restriction

This register should not be changed while the transcoder or port are enabled.

DWord	Bit	Description
0	31:29	Reserved Format: MBZ
	28:16	Horizontal Total This field specifies Horizontal Total size. This should be equal to the sum of the horizontal active and the horizontal blank sizes. This field is programmed to the number of pixels desired minus one. This field is ignored by WD transcoders. <h3 style="background-color: #e0e0ff; padding: 2px;">Restriction</h3> This register must always be programmed to the same value as the Horizontal Blank End.
	15:13	Reserved Format: MBZ
	12:0	Horizontal Active This field specifies Horizontal Active Display size. The first horizontal active display pixel is considered pixel number 0. This field is programmed to the number of pixels desired minus one. <h3 style="background-color: #e0e0ff; padding: 2px;">Restriction</h3> The minimum horizontal active display size is 64 pixels. In HDMI modes the minimum is 256 pixels. This register must always be programmed to the same value as the Horizontal Blank Start. In FDI mode bit 12 must not be set.

TRANS_MSA_MISC

TRANS_MSA_MISC	
Register Space:	MMIO: 0/2/0
Project:	BDW
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	60410h-60413h
Name:	Transcoder A MSA Misc
ShortName:	TRANS_MSA_MISC_A
Valid Projects:	BDW
Power:	off/on
Reset:	soft
Address:	61410h-61413h
Name:	Transcoder B MSA Misc
ShortName:	TRANS_MSA_MISC_B
Valid Projects:	BDW
Power:	off/on
Reset:	soft
Address:	62410h-62413h
Name:	Transcoder C MSA Misc
ShortName:	TRANS_MSA_MISC_C
Valid Projects:	BDW
Power:	off/on
Reset:	soft
Address:	6F410h-6F413h
Name:	Transcoder EDP MSA Misc
ShortName:	TRANS_MSA_MISC_EDP
Valid Projects:	BDW
Power:	Always on
Reset:	soft
Description	
There is one instance of this register per each transcoder A/B/C/EDP. This register selects what value will be sent in the DisplayPort Main Stream Attribute (MSA) Miscellaneous (MISC) fields. The MSA MISC fields are mostly used to indicate the color encoding format and need to be programmed to indicate color space, bits per color, etc.	

TRANS_MSA_MISC

Programming Notes

See the DisplayPort specification for the details on what to program in these fields.

DWord	Bit	Description		
0	31:16	<p>MSA Unused This field selects the value that will be sent in the DisplayPort MSA unused fields.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="text-align: center; padding: 2px;">Programming Notes</td></tr> <tr> <td style="padding: 2px;">This should be usually programmed with all 0s.</td></tr> </table>	Programming Notes	This should be usually programmed with all 0s.
Programming Notes				
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15:8	<p>MSA MISC1 This field selects the value that will be sent in the DisplayPort MSA MISC1 field. When TRANS_STEREO3D_CTL bit FS_MSA_MISC1_Drive_En is enabled, hardware will drive MISC1 bits 2:1 (bits 10:9 of this register) with the field sequential stereo 3D left or right eye indication, and any value written to those bits here will be ignored.</p>			
7:0	<p>MSA MISC0 This field selects the value that will be sent in the DisplayPort MSA MISC0 field.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="text-align: center; padding: 2px;">Restriction</td></tr> <tr> <td style="padding: 2px;">Before enabling DisplayPort, bit 0 should always be set to 1 to indicate link clock and stream clock are synchronous.</td></tr> </table>	Restriction	Before enabling DisplayPort, bit 0 should always be set to 1 to indicate link clock and stream clock are synchronous.	
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TRANS_MULT

TRANS_MULT		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	6002Ch-6002Fh	
Name:	Transcoder A Multiply	
ShortName:	TRANS_MULT_A	
Valid Projects:	BDW	
Power:	off/on	
Reset:	soft	
Address:	6102Ch-6102Fh	
Name:	Transcoder B Multiply	
ShortName:	TRANS_MULT_B	
Valid Projects:	BDW	
Power:	off/on	
Reset:	soft	
Address:	6202Ch-6202Fh	
Name:	Transcoder C Multiply	
ShortName:	TRANS_MULT_C	
Valid Projects:	BDW	
Power:	off/on	
Reset:	soft	
Description		
There is one instance of this register for each transcoder A/B/C.		
Restriction		
This register should not be changed while the transcoder or port are enabled.		
DWord	Bit	Description
0	31:3	Reserved

TRANS_MULT

	2:0	Multiplier This field specifies the data multiplier value used by HDMI and DVI.
Value	Name	Description
000b	X1	Multiply by 1
001b	X2	Multiply by 2
011b	X4	Multiply by 4
Others	Reserved	Reserved

TRANS_SPACE

TRANS_SPACE		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	60024h-60027h	
Name:	Transcoder A Space	
ShortName:	TRANS_SPACE_A	
Valid Projects:	BDW	
Power:	off/on	
Reset:	soft	
Address:	61024h-61027h	
Name:	Transcoder B Space	
ShortName:	TRANS_SPACE_B	
Valid Projects:	BDW	
Power:	off/on	
Reset:	soft	
Address:	62024h-62027h	
Name:	Transcoder C Space	
ShortName:	TRANS_SPACE_C	
Valid Projects:	BDW	
Power:	off/on	
Reset:	soft	
Address:	6F024h-6F027h	
Name:	Transcoder EDP Space	
ShortName:	TRANS_SPACE_EDP	
Valid Projects:	BDW	
Power:	Always on	
Reset:	soft	
Description		
There is one instance of this register for each transcoder A/B/C/EDP.		
Restriction		
This register should not be changed while the transcoder or port are enabled.		
DWord	Bit	Description

TRANS_SPACE		
0	31:12	Reserved
	11:0	Vertical Active Space This field specifies Stereo 3D Vertical Active space. This determines the number of constant pixel value lines inserted between the left and right eye active video regions in the stereo 3D stacked frame mode. This field will only be used when the transcoder is in the stereo 3D stacked frame mode. This field should usually be programmed to be the same as the width of the vertical blank.

TRANS_VBLANK

TRANS_VBLANK		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	60010h-60013h	
Name:	Transcoder A Vertical Blank	
ShortName:	TRANS_VBLANK_A	
Valid Projects:	BDW	
Power:	off/on	
Reset:	soft	
Address:	61010h-61013h	
Name:	Transcoder B Vertical Blank	
ShortName:	TRANS_VBLANK_B	
Valid Projects:	BDW	
Power:	off/on	
Reset:	soft	
Address:	62010h-62013h	
Name:	Transcoder C Vertical Blank	
ShortName:	TRANS_VBLANK_C	
Valid Projects:	BDW	
Power:	off/on	
Reset:	soft	
Address:	6F010h-6F013h	
Name:	Transcoder EDP Vertical Blank	
ShortName:	TRANS_VBLANK_EDP	
Valid Projects:	BDW	
Power:	Always on	
Reset:	soft	
There is one instance of this register for each transcoder A/B/C/EDP.		
Restriction		
This register should not be changed while the transcoder or port are enabled.		
DWord	Bit	Description
0	31:29	Reserved

TRANS_VBLANK		
	28:16	Vertical Blank End This field specifies Vertical Blank End position relative to the vertical active display start. Restriction
		This register must always be programmed to the same value as the Vertical Total. The minimum vertical blank size is 5 lines. With SRD/PSR and/or DisplayPort VDIP GMP the minimum is 8 lines.
	15:13	Reserved
	12:0	Vertical Blank Start This field specifies the Vertical Blank Start position relative to the vertical active display start. Restriction
		This register must always be programmed to the same value as the Vertical Active.

TRANS_VSYNC

TRANS_VSYNC		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	60014h-60017h	
Name:	Transcoder A Vertical Sync	
ShortName:	TRANS_VSYNC_A	
Valid Projects:	BDW	
Power:	off/on	
Reset:	soft	
Address:	61014h-61017h	
Name:	Transcoder B Vertical Sync	
ShortName:	TRANS_VSYNC_B	
Valid Projects:	BDW	
Power:	off/on	
Reset:	soft	
Address:	62014h-62017h	
Name:	Transcoder C Vertical Sync	
ShortName:	TRANS_VSYNC_C	
Valid Projects:	BDW	
Power:	off/on	
Reset:	soft	
Address:	6F014h-6F017h	
Name:	Transcoder EDP Vertical Sync	
ShortName:	TRANS_VSYNC_EDP	
Valid Projects:	BDW	
Power:	Always on	
Reset:	soft	
Description		
There is one instance of this register for each transcoder A/B/C/EDP.		
Restriction		
This register should not be changed while the transcoder or port are enabled.		
DWord	Bit	Description

TRANS_VSYNC		
0	31:29	Reserved
	28:16	Vertical Sync End This field specifies the Vertical Sync End position relative to the vertical active display start. It is programmed with VerticalActive+FrontPorch+Sync-1
		Restriction
		This value must be greater than the vertical sync start and less than Vertical Total.
	15:13	Reserved
	12:0	Vertical Sync Start This field specifies the Vertical Sync Start position relative to the vertical active display start. It is programmed with VerticalActive+FrontPorch-1
		Restriction
		This value must be greater than Vertical Active.

TRANS_VSYNCSHIFT

TRANS_VSYNCSHIFT		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	60028h-6002Bh	
Name:	Transcoder A Vertical Sync Shift	
ShortName:	TRANS_VSYNCSHIFT_A	
Valid Projects:	BDW	
Power:	off/on	
Reset:	soft	
Address:	61028h-6102Bh	
Name:	Transcoder B Vertical Sync Shift	
ShortName:	TRANS_VSYNCSHIFT_B	
Valid Projects:	BDW	
Power:	off/on	
Reset:	soft	
Address:	62028h-6202Bh	
Name:	Transcoder C Vertical Sync Shift	
ShortName:	TRANS_VSYNCSHIFT_C	
Valid Projects:	BDW	
Power:	off/on	
Reset:	soft	
Address:	6F028h-6F02Bh	
Name:	Transcoder EDP Vertical Sync Shift	
ShortName:	TRANS_VSYNCSHIFT_EDP	
Valid Projects:	BDW	
Power:	Always on	
Reset:	soft	
Description		
There is one instance of this register for each transcoder A/B/C/EDP.		
Restriction		
This register should not be changed while the transcoder or port are enabled.		
DWord	Bit	Description

TRANS_VSYNCSHIFT

0	31:13	Reserved
	12:0	<p>Second Field VSync Shift</p> <p>This value specifies the vertical sync alignment for the start of the interlaced second field, expressed in terms of the absolute pixel number relative to the horizontal active display start. This value will only be used if the transcoder is programmed to an interlaced mode. Typically, the interlaced second field vertical sync should start one pixel after the point halfway between successive horizontal syncs, so the value of this register should be programmed = horizontal sync start - floor[horizontal total / 2] Calculate using the actual horizontal sync start and horizontal total values and not the minus one values programmed into the registers. This vertical sync shift only occurs during the interlaced second field. In all other cases the vertical sync start position is aligned with horizontal sync start.</p>

TRANS_VTOTAL

TRANS_VTOTAL	
Register Space:	MMIO: 0/2/0
Project:	BDW
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	6000Ch-6000Fh
Name:	Transcoder A Vertical Total
ShortName:	TRANS_VTOTAL_A
Valid Projects:	BDW
Power:	off/on
Reset:	soft
Address:	6100Ch-6100Fh
Name:	Transcoder B Vertical Total
ShortName:	TRANS_VTOTAL_B
Valid Projects:	BDW
Power:	off/on
Reset:	soft
Address:	6200Ch-6200Fh
Name:	Transcoder C Vertical Total
ShortName:	TRANS_VTOTAL_C
Valid Projects:	BDW
Power:	off/on
Reset:	soft
Address:	6E00Ch-6E00Fh
Name:	Transcoder WD0 Vertical Total
ShortName:	TRANS_VTOTAL_WD0
Valid Projects:	BDW
Power:	off/on
Reset:	soft
Address:	6F00Ch-6F00Fh
Name:	Transcoder EDP Vertical Total
ShortName:	TRANS_VTOTAL_EDP
Valid Projects:	BDW
Power:	Always on
Reset:	soft

TRANS_VTOTAL								
Restriction								
This register should not be changed while the transcoder or port are enabled.								
DWord	Bit	Description						
0	31:29	Reserved						
	28:16	<p>Vertical Total</p> <p>This field specifies Vertical Total size. This should be equal to the sum of the vertical active and the vertical blank sizes. For progressive display modes, this field is programmed to the number of lines desired minus one. For interlaced display modes, this field is programmed with the number of lines desired minus two. The vertical counter is incremented on the leading edge of the horizontal sync. Both even and odd vertical totals are supported. This field is ignored by WD transcoders.</p> <table border="1"> <thead> <tr> <th colspan="2">Restriction</th> </tr> </thead> <tbody> <tr> <td colspan="2">This register must always be programmed to the same value as the Vertical Blank End.</td></tr> </tbody> </table>	Restriction		This register must always be programmed to the same value as the Vertical Blank End.			
Restriction								
This register must always be programmed to the same value as the Vertical Blank End.								
	15:13	Reserved						
	12	Reserved						
	11:0	<p>Vertical Active</p> <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> </table> <p>This field specifies Vertical Active Display size. The first vertical active display line is considered line number 0. This field is programmed to the number of lines desired minus one.</p> <table border="1"> <thead> <tr> <th colspan="2">Restriction</th> </tr> </thead> <tbody> <tr> <td colspan="2">When using the internal panel fitting logic, the minimum vertical active area must be seven lines. This register must always be programmed to the same value as the Vertical Blank Start.</td></tr> </tbody> </table>	Project:	BDW	Restriction		When using the internal panel fitting logic, the minimum vertical active area must be seven lines. This register must always be programmed to the same value as the Vertical Blank Start.	
Project:	BDW							
Restriction								
When using the internal panel fitting logic, the minimum vertical active area must be seven lines. This register must always be programmed to the same value as the Vertical Blank Start.								

TRANS_WD_FUNC_CTL

TRANS_WD_FUNC_CTL

Register Space: MMIO: 0/2/0

Project: BDW

Default Value: 0x00000000

Access: R/W

Size (in bits): 32

DWord	Bit	Description												
0	31	WD Function Enable This bit enables the WD function.												
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disable</td> </tr> <tr> <td>1b</td> <td>Enable</td> </tr> </tbody> </table>	Value	Name	0b	Disable	1b	Enable						
Value	Name													
0b	Disable													
1b	Enable													
30:28	Reserved	Format: MBZ												
27	Reserved	Project: BDW Format: MBZ												
26	Reserved	Project: BDW Format: MBZ												
25:23	Reserved	Format: MBZ												
22:20	WD Color Mode This field selects the capture color format.	<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>YUV 4:4:4</td> <td>YUV 32-bit 4:4:4 packed (8:8:8:8 MSB-Y:U:X:V)</td> </tr> <tr> <td>001b</td> <td>YUV 4:2:2</td> <td>YUV 16-bit 4:2:2 packed (8:8:8:8 MSB- Y1:U1:Y2:V1) Drop U2 and V2</td> </tr> <tr> <td>Others</td> <td>Reserved</td> <td>Reserved</td> </tr> </tbody> </table>	Value	Name	Description	000b	YUV 4:4:4	YUV 32-bit 4:4:4 packed (8:8:8:8 MSB-Y:U:X:V)	001b	YUV 4:2:2	YUV 16-bit 4:2:2 packed (8:8:8:8 MSB- Y1:U1:Y2:V1) Drop U2 and V2	Others	Reserved	Reserved
Value	Name	Description												
000b	YUV 4:4:4	YUV 32-bit 4:4:4 packed (8:8:8:8 MSB-Y:U:X:V)												
001b	YUV 4:2:2	YUV 16-bit 4:2:2 packed (8:8:8:8 MSB- Y1:U1:Y2:V1) Drop U2 and V2												
Others	Reserved	Reserved												
	Restriction													
	This field must not be changed while the function is enabled.													
19:16	Reserved	Project: BDW Format: MBZ												

TRANS_WD_FUNC_CTL

	15	Reserved	Format:	MBZ									
	14:12	WD Input Select	These bits determine the input to WD.										
		<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center; background-color: #e0e0ff;">Value</th><th style="text-align: center; background-color: #e0e0ff;">Name</th></tr> </thead> <tbody> <tr><td style="text-align: center;">000b</td><td style="text-align: center;">Pipe A</td></tr> <tr><td style="text-align: center;">101b</td><td style="text-align: center;">Pipe B</td></tr> <tr><td style="text-align: center;">110b</td><td style="text-align: center;">Pipe C</td></tr> <tr><td style="text-align: center;">Others</td><td style="text-align: center;">Reserved</td></tr> </tbody> </table>		Value	Name	000b	Pipe A	101b	Pipe B	110b	Pipe C	Others	Reserved
Value	Name												
000b	Pipe A												
101b	Pipe B												
110b	Pipe C												
Others	Reserved												
		Restriction											
		This field must not be changed while the function is enabled. It is not valid to have the same pipes driving multiple enabled transcoders.											
	11:0	Reserved	Format:	MBZ									

TRNULLDETCT

REG_TEMPLATE - TRNULLDETCT									
DWord	Bit	Description							
0	31:0	Null Tile Detection Value							
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00000000h</td> <td>[Default]</td> <td> A 32bit value programmed to enable h/w to perform a match of TR-VA TT entries to detect Null Tiles. Hardware will flag each entry and space behind it as Null Tile for matched entries. </td> </tr> </tbody> </table>	Value	Name	Description	00000000h	[Default]	A 32bit value programmed to enable h/w to perform a match of TR-VA TT entries to detect Null Tiles. Hardware will flag each entry and space behind it as Null Tile for matched entries.	R/W
Value	Name	Description							
00000000h	[Default]	A 32bit value programmed to enable h/w to perform a match of TR-VA TT entries to detect Null Tiles. Hardware will flag each entry and space behind it as Null Tile for matched entries.							

Unblock Message Ack to Busy Detection Timer (sleep timer)

RC_WAKE_HYSTERESIS - Unblock Message Ack to Busy Detection Timer (sleep timer)				
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x00000000 Size (in bits): 32 Address: 0A0B0h				
After the time programmed in this register is met and graphics is still idle, then RC6x is allowed to be entered. 0 = 0 usec. 1 = 1.28 usec. 2 = 2.56 usec. 3 = 3.84 usec. FF FFFF = 21.474 sec. pmcr_rc_sleep[23:0].				
DWord	Bit	Description		
0	31:24	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> Reserved.	Access:	RO
Access:	RO			
23:0	Unblock Message Ack to Busy Detection Timer <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> This register prevents GT RC6 entry for the programmed time after a previous GT RC6 exit, meaning the minimum amount of time GT has to be in RC0. 0 = 0 usec. 1 = 1.28 usec. 2 = 2.56 usec. 3 = 3.84 usec. FF FFFF = 21.474 sec. pmcr_rc_sleep[23:0].	Access:	R/W	
Access:	R/W			

Unit Level Clock Gating Control 1

UCGCTL1 - Unit Level Clock Gating Control 1

Register Space:	MMIO: 0/2/0			
Project:	BDW 0x02C00000 [NOVALIDPROJECTS] 0x02F00000 [BDW]			
Size (in bits):	32			
Address:	09400h			
Unit Level Clock Gating Control Registers.(Not Ctx save on BDW A0 for slice shutdown)				
DWord	Bit	Description		
0	31	Sarbunit Clock Gating Disable <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>SARB unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W			
30	IEFunit Clock Gating Disable <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>IEFunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	
Access:	R/W			
29	IECPunit Clock Gating Disable <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>IECPunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	
Access:	R/W			
28	ICunit Clock Gating Disable <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>ICunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	
Access:	R/W			

UCGCTL1 - Unit Level Clock Gating Control 1

	HIZunit Clock Gating Disable	
27	Access: 	R/W
	HIZunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
26	GWunit Clock Gating Disable	
	Access: 	R/W
	GWunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
25	GTIunit Clock Gating Disable	
	Default Value: 1b	
	Access: 	R/W
	GTI Units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
24	GSunit Clock Gating Disable	
	Access: 	R/W
	GSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
23	GPMunit Clock Gating Disable	
	Default Value: 1b	
	Access: 	R/W
	GPMunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	

UCGCTL1 - Unit Level Clock Gating Control 1

	GAMunit/GAMWunit Clock Gating Disable						
22	<table border="1"> <tr> <td>Default Value:</td><td>1b</td></tr> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>GAMunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) (Clock gating needs to be disabled for GAMunit on BDW A-step)</p>	Default Value:	1b	Project:	BDW	Access:	R/W
Default Value:	1b						
Project:	BDW						
Access:	R/W						
21	GACunit Clock Gating Disable <table border="1"> <tr> <td>Default Value:</td><td>1b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>GACunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Default Value:	1b	Access:	R/W		
Default Value:	1b						
Access:	R/W						
20	GABunit Clock Gating Disable <table border="1"> <tr> <td>Default Value:</td><td>1b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>GABunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Default Value:	1b	Access:	R/W		
Default Value:	1b						
Access:	R/W						
19	FTunit Clock Gating Disable <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>FTunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W				
Access:	R/W						
18	FLunit Clock Gating Disable <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>FLunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W				
Access:	R/W						

UCGCTL1 - Unit Level Clock Gating Control 1

	EU_FPUunit Clock Gating Disable	
17	Access: 	R/W
	EU_FPUunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
16	EU_TCunit Clock Gating Disable	
	Access: 	R/W
	EU_TCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
15	EU_EMunit Clock Gating Disable	
	Access: 	R/W
	EU_EMunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
14	EU_GAunit Clock Gating Disable	
	Access: 	R/W
	EU_GAunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
13	EUunit Clock Gating Disable	
	Access: 	R/W
	EUunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
12	SVLunit Clock Gating Disable	
	Access: 	R/W
	SVLunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	

UCGCTL1 - Unit Level Clock Gating Control 1

	DTunit Clock Gating Disable				
11	<table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>DTunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W		
Access:	R/W				
DMunit Clock Gating Disable					
10	<table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>DMunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W		
Access:	R/W				
DGunit Clock Gating Disable					
9	<table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>DGunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W		
Access:	R/W				
DAPunit Clock Gating Disable					
8	<table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>DAPunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W		
Access:	R/W				
CSunit Clock Gating Disable					
7	<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>CSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) Due to known HW issue, irrespective of this bit setting CSunit level clock gating is always disabled.</p>	Project:	BDW	Access:	R/W
Project:	BDW				
Access:	R/W				
CLunit Clock Gating Disable					
6	<table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>CLunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W		
Access:	R/W				

UCGCTL1 - Unit Level Clock Gating Control 1

	BLBunit Clock Gating Disable		
5	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td><td style="padding: 2px; text-align: right;">R/W</td></tr> </table> <p>BLBunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
4	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td><td style="padding: 2px; text-align: right;">R/W</td></tr> </table> <p>BFunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
3	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td><td style="padding: 2px; text-align: right;">R/W</td></tr> </table> <p>BDunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
2	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td><td style="padding: 2px; text-align: right;">R/W</td></tr> </table> <p>BCSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
1	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td><td style="padding: 2px; text-align: right;">R/W</td></tr> </table> <p>AVSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
0	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td><td style="padding: 2px; text-align: right;">R/W</td></tr> </table> <p>SPARE RAM Clock Gating Disable Control: '0' : RAM Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : RAM Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

Unit Level Clock Gating Control 2

UCGCTL2 - Unit Level Clock Gating Control 2				
DWord	Bit	Description		
Register Space: MMIO: 0/2/0				
Project: BDW				
Default Value: 0x00000000 [BDW]				
Size (in bits): 32				
Address: 09404h				
Unit Level Clock Gating Control Registers.(Not Ctx save on BDW A0 for slice shutdown)				
0	31	VUnit Clock Gating Disable <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>VUnit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W			
30	VDSunit Clock Gating Disable <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>VDSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	
Access:	R/W			
29	VDlunit Clock Gating Disable <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>VDlunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	
Access:	R/W			
28	VCSunit Clock Gating Disable <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>VCSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	
Access:	R/W			

UCGCTL2 - Unit Level Clock Gating Control 2

	27 DTOunit Clock Gating Disable		
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td><td style="padding: 2px; text-align: center;">R/W</td></tr> </table> <p style="margin-top: 2px;">DTOunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
<hr/>			
	26 VCPunit Clock Gating Disable		
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td><td style="padding: 2px; text-align: center;">R/W</td></tr> </table> <p style="margin-top: 2px;">VCPunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
<hr/>			
	25 VCDunit Clock Gating Disable		
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td><td style="padding: 2px; text-align: center;">R/W</td></tr> </table> <p style="margin-top: 2px;">VCDunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
<hr/>			
	24 URBMunit Clock Gating Disable		
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td><td style="padding: 2px; text-align: center;">R/W</td></tr> </table> <p style="margin-top: 2px;">URBMunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
<hr/>			
	23 TSGunit Clock Gating Disable		
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td><td style="padding: 2px; text-align: center;">R/W</td></tr> </table> <p style="margin-top: 2px;">TSGunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
<hr/>			
	22 TDUnit Clock Gating Disable		
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td><td style="padding: 2px; text-align: center;">R/W</td></tr> </table> <p style="margin-top: 2px;">TDUnit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

UCGCTL2 - Unit Level Clock Gating Control 2

	21	TDSunit Clock Gating Disable		
		<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px; text-align: right;">R/W</td> </tr> </table>	Access:	R/W
Access:	R/W			
		<p>TDSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p> <p>Programming note: To work around a clock gating issue for A0-D0, the clock gating disable must be set to a 1 unless the offset h229c bit 11, Replay Mode, is set to 0, mid-cmdbuf preemption Project BDW : To work around a clock gating issue for A0-D0, the clock gating disable must be set to a 1 unless the offset h229c bit 11, Replay Mode, is set to 0, mid-cmdbuf preemption</p>		
	20	SVSMunit Clock Gating Disable		
		<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px; text-align: right;">R/W</td> </tr> </table>	Access:	R/W
Access:	R/W			
		<p>SVSMunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>		
	19	SVGunit Clock Gating Disable		
		<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px; text-align: right;">R/W</td> </tr> </table>	Access:	R/W
Access:	R/W			
		<p>SVGunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>		
	18	SQunit Clock Gating Disable		
		<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px; text-align: right;">R/W</td> </tr> </table>	Access:	R/W
Access:	R/W			
		<p>SQunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>		
	17	Slunit Clock Gating Disable		
		<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px; text-align: right;">R/W</td> </tr> </table>	Access:	R/W
Access:	R/W			
		<p>Slunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>		

UCGCTL2 - Unit Level Clock Gating Control 2

	SFunit Clock Gating Disable	
16	Access: 	R/W
	SFunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
15	SECunit Clock Gating Disable	
	Access: 	R/W
	SECunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
14	SCunit Clock Gating Disable	
	Access: 	R/W
	SCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
13	RCZunit Clock Gating Disable	
	Access: 	R/W
	RCZunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
12	RCPBunit Clock Gating Disable	
	Project: 	BDW
	Access: 	R/W
	RCPBunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
11	RCCunit Clock Gating Disable	
	Access: 	R/W
	RCCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	

UCGCTL2 - Unit Level Clock Gating Control 2

	QCunit Clock Gating Disable		
10	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px; text-align: center;">R/W</td> </tr> </table> <p>QCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
9	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px; text-align: center;">R/W</td> </tr> </table> <p>PSDunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
8	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px; text-align: center;">R/W</td> </tr> </table> <p>PLunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
7	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px; text-align: center;">R/W</td> </tr> </table> <p>MTunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
6	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px; text-align: center;">R/W</td> </tr> </table> <p>MPCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
5	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px; text-align: center;">R/W</td> </tr> </table> <p>TDGunitClock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

UCGCTL2 - Unit Level Clock Gating Control 2

	4	MSCunit Clock Gating Disable	
		Access:	R/W
MSCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)			
	3	TEunit Clock Gating Disable	
TEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)			
	2	TETGunit Clock Gating Disable	
		Access:	R/W
TETGunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)			
	1	MAunit Clock Gating Disable	
		Access:	R/W
MAunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)			
	0	IZunit Clock Gating Disable	
		Access:	R/W
IZunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)			

Unit Level Clock Gating Control 3

UCGCTL3 - Unit Level Clock Gating Control 3				
Register Space:	MMIO: 0/2/0			
Project:	BDW 0x04000000 [BDW:GT1, BDW:GT2, BDW:GT3:H, BDW:GT3E]			
Size (in bits):	32			
Address:	09408h			
Unit Level Clock Gating Control Registers. (Not Ctx save on BDW A0 for slice shutdown)				
DWord	Bit	Description		
0	31	Flunits 2nd Clock Gating Disable <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Flunits 2nd Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W			
30	SVRRunit Clock Gating Disable <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>SVRRunits' Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	
Access:	R/W			
29	VCRunit Clock Gating Disable <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>VCRunits' Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	
Access:	R/W			
28	EDTunit Clock Gating Disable <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>EDTunits' Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	
Access:	R/W			

UCGCTL3 - Unit Level Clock Gating Control 3

	VClunit Clock Gating Disable						
27	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td><td style="padding: 2px; text-align: center;">R/W</td></tr> </table> <p>VClunits' Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W				
Access:	R/W						
2x Assign fub XOR Clock Gating Disable							
26	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Default Value:</td><td style="padding: 2px; text-align: center;">1b</td></tr> <tr> <td style="padding: 2px;">Project:</td><td style="padding: 2px; text-align: center;">BDW</td></tr> <tr> <td style="padding: 2px;">Access:</td><td style="padding: 2px; text-align: center;">R/W</td></tr> </table> <p>2x Assign fub XOR Clock Gating Disable Control: '0' : 2x Assign fub XOR Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : 2x Assign fub XOR Clock Gating Disabled. (i.e., clocks are toggling, always) This bit should be programmed to a 1 for BDW:B0</p>	Default Value:	1b	Project:	BDW	Access:	R/W
Default Value:	1b						
Project:	BDW						
Access:	R/W						
25	HSunit Clock Gating Disable <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td><td style="padding: 2px; text-align: center;">R/W</td></tr> </table> <p>HSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W				
Access:	R/W						
24	SOLunit Clock Gating Disable <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td><td style="padding: 2px; text-align: center;">R/W</td></tr> </table> <p>SOLunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W				
Access:	R/W						
23	QRCunit Clock Gating Disable <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td><td style="padding: 2px; text-align: center;">R/W</td></tr> </table> <p>QRCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W				
Access:	R/W						

UCGCTL3 - Unit Level Clock Gating Control 3					
	22	MSPBISTunit Clock Gating Disable			
		<table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table>	Access:	R/W	
Access:	R/W				
		<p>MSPBISTunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>			
	21	BSPunit Clock Gating Disable			
		<table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table>	Access:	R/W	
Access:	R/W				
		<p>BSPunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>			
	20	OACSunit Clock Gating Disable			
		<table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table>	Access:	R/W	
Access:	R/W				
		<p>OACSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>			
	19	SBEunit Clock Gating Disable			
		<table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table>	Access:	R/W	
Access:	R/W				
		<p>SBEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>			
	18	BCunit Clock Gating Disable			
		<table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table>	Access:	R/W	
Access:	R/W				
		<p>BCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>			
	17	WMBE Clock Gating Disable			
		<table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table>	Access:	R/W	
Access:	R/W				
		<p>WMBEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>			

UCGCTL3 - Unit Level Clock Gating Control 3

	16 WMFUnit Clock Gating Disable		
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px; text-align: right;">R/W</td> </tr> </table> <p>WMFUnit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
	15 VSCunit Clock Gating Disable		
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px; text-align: right;">R/W</td> </tr> </table> <p>VSCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
	14 Reserved		
	13 USBunit Clock Gating Disable		
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px; text-align: right;">R/W</td> </tr> </table> <p>USBunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
	12 STCunit Clock Gating Disable		
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px; text-align: right;">R/W</td> </tr> </table> <p>STCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
	11 VSunit Clock Gating Disable		
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px; text-align: right;">R/W</td> </tr> </table> <p>VSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
	10 VOPunit Clock Gating Disable		
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px; text-align: right;">R/W</td> </tr> </table> <p>VOPunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

UCGCTL3 - Unit Level Clock Gating Control 3

	9 VMXunit Clock Gating Disable		
	<table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>VMXunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
	8 VMEunit Clock Gating Disable		
	<table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>VMEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
	7 VMDunit Clock Gating Disable		
	<table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>VMDunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
	6 VMCunit Clock Gating Disable		
	<table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>VMCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
	5 VLFunit Clock Gating Disable		
	<table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>VLFunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
	4 VITunit Clock Gating Disable		
	<table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>VITunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
	3 VIPunit Clock Gating Disable		

UCGCTL3 - Unit Level Clock Gating Control 3

		Access:	R/W
		VIPunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	2	VINunit Clock Gating Disable	
		Access:	R/W
		VINunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	1	VFTunit Clock Gating Disable	
		Access:	R/W
		VFTunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	0	VFEunit Clock Gating Disable	
		Access:	R/W
		VFEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	

Unit Level Clock Gating Control 4

UCGCTL4 - Unit Level Clock Gating Control 4						
DWord	Bit	Description				
0	31:30	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>rsvd</td> <td></td> </tr> </table>	Access:	RO	rsvd	
Access:	RO					
rsvd						
	29	GAFSRRB unit Clock Gate Disable <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>GAFSRRB units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W		
Access:	R/W					
	28	RAMDFT units Clock Gate Disable <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>RAMDFT units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W		
Access:	R/W					
	27	L3 CBR 2x Clock Gate Disable <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>L3 CBR units 2x Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W		
Access:	R/W					
	26	L3 CBR 1x Clock Gate Disable <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>L3 CBR units 1x Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W		
Access:	R/W					

UCGCTL4 - Unit Level Clock Gating Control 4

	25	L3 BANK 2x Clock Gate Disable	Access:	R/W
L3 BANK units 2x Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)				
	24	L3 BANK 1x Clock Gate Diable	Access:	R/W
L3 BANK units 1x Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)				
	23	MBGFunit Clock Gate Disable	Default Value:	1b
Default Value: Access:				
MBGFunits Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)				
	22	MSQDunit 2x Clock Gate Disable	Default Value:	1b
Default Value: Access:				
MSQD units cu2x Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)				
	21	MSQDunit Clock Gate Disable	Default Value:	1b
Default Value: Access:				
MSQD units 1x Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)				

UCGCTL4 - Unit Level Clock Gating Control 4

	20	MISDunits 2x Clock Gate Disable					
		<table border="1" style="width: 100%;"> <tr> <td>Default Value:</td><td>1b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table>	Default Value:	1b	Access:	R/W	
Default Value:	1b						
Access:	R/W						
		<p>MISDunits cu2x Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>					
	19	MISDunit Clock Gate Disable					
		<table border="1" style="width: 100%;"> <tr> <td>Default Value:</td><td>1b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table>	Default Value:	1b	Access:	R/W	
Default Value:	1b						
Access:	R/W						
		<p>MISDunits 1x Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>					
	18	GAFMunit Clock Gate Disable					
		<table border="1" style="width: 100%;"> <tr> <td>Access:</td><td>R/W</td></tr> </table>	Access:	R/W			
Access:	R/W						
		<p>GAFMunit' Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>					
	17	GAPCunit Clock Gate Disable					
		<table border="1" style="width: 100%;"> <tr> <td>Access:</td><td>R/W</td></tr> </table>	Access:	R/W			
Access:	R/W						
		<p>GAPCunits Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>					
	16	GAPZunit Clock Gate Disable					
		<table border="1" style="width: 100%;"> <tr> <td>Access:</td><td>R/W</td></tr> </table>	Access:	R/W			
Access:	R/W						
		<p>GAPZunits' Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>					
	15	GAPL3unit Clock Gate Disable					
		<table border="1" style="width: 100%;"> <tr> <td>Access:</td><td>R/W</td></tr> </table>	Access:	R/W			
Access:	R/W						
		<p>GAPL3 units' Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>					

UCGCTL4 - Unit Level Clock Gating Control 4

	14	GAFSunit Clock Gate Disable	Access:	R/W
		GAFSunits' Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
	13	GAHSunit Clock Gate Disable	Access:	R/W
		GAHSunits' Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
	12	VISunit Clock Gate Disable	Access:	R/W
		VISunits' Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
	11	VACunit Clock Gate Disable	Access:	R/W
		VACunits' Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
	10	VAMunit Clock Gate Disable	Access:	R/W
		VAMunits Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
	9	VADuit Clock Gating Disable	Access:	R/W
		VADunits Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		

UCGCTL4 - Unit Level Clock Gating Control 4

	8	JPGunit Clock Gating Disable	
		Access:	R/W
		JPGunits Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	7	VBPunits Clock Gating Disable	
		Access:	R/W
		VBPunits Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	6	VHRunit Clock Gating Disable	
		Access:	R/W
		VHRunits Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	5	VID4 VINunit Clock Gating Disable	
		Access:	R/W
		VID4 VINunits' Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	4	VID3 VINunit Clock Gating Disable	
		Access:	R/W
		VID3 VINunits' Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	3	VID2 VINunit Clock Gating Disable	
		Access:	R/W
		VID2 VINunits' Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	

UCGCTL4 - Unit Level Clock Gating Control 4

	2	VID1 VINunit Clock Gating Disable		
		Access:	R/W	
VID1 VINunits' Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)				
	1:0	MSQCunit Clock Gating Disable		
		Default Value:	11b	
		Access:	R/W	
MSQCunits' Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) Errata: DEVBDW:A0 - Unit level Clock gating for MSQC cannot be enabled SW WA: DEVBDW:A0 - Disable MSQC clock gating by setting bit 1:0 in UCGCTL4 register				

Unit Level Clock Gating Control 5

UCGCTL5 - Unit Level Clock Gating Control 5				
DWord	Bit	Description		
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x00000000 Size (in bits): 32				
Address: 09418h				
Unit Clock Gating Control Register 5.(Not Ctx save on BDW A0 for slice shutdown)				
0	31	<p>VCOunit clock gating disable bit</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>WVCOP units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always).</p>	Access:	R/W
Access:	R/W			
0	30	<p>VMBunit clock gate disable bit</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>VMB units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W			
0	29	<p>VDMunit clock gate disable bit</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>VDM units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W			
0	28	<p>L3BANK unit cclk gating disable bit</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>L3bank units cclk Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W			

UCGCTL5 - Unit Level Clock Gating Control 5

	L3BANK cu2x clock gate disable bit	
27	Access: R/W	L3BANK units cu2x Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks
26	LNIunit clock gate disable bit	Access: R/W
	LNI units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
25	LNEUNIT clock gate disable bit	Access: R/W
	LNE units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
24	VVPunit clock gate disable bit	Access: R/W
	VVP units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
23	WVFT unit clock gate disable bits	Access: R/W
	WVFT units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
22	WBPS unit clock gate disable bit	Access: R/W
	WBPS units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	

UCGCTL5 - Unit Level Clock Gating Control 5

	WVMX unit clock gate disable bit		
21	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px; text-align: center;">R/W</td> </tr> </table> <p>WVMX units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
20	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px; text-align: center;">R/W</td> </tr> </table> <p>WVIP units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
19	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px; text-align: center;">R/W</td> </tr> </table> <p>WVIT units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
18	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px; text-align: center;">R/W</td> </tr> </table> <p>WVIS units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
17	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px; text-align: center;">R/W</td> </tr> </table> <p>RPM units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
16	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px; text-align: center;">R/W</td> </tr> </table> <p>OASC units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

UCGCTL5 - Unit Level Clock Gating Control 5

	VECS unit clock gate disable		
15	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px; text-align: center;">R/W</td> </tr> </table> <p>VECS units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
14	GAHSV unit clock gate disable <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px; text-align: center;">R/W</td> </tr> </table> <p>GAHSV units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
13	GAHSD unit clock gate disable <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px; text-align: center;">R/W</td> </tr> </table> <p>GAHSD units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
12	GAV unit's clock gate disable <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px; text-align: center;">R/W</td> </tr> </table> <p>GAV units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
11	RSunit's clock gate disable <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px; text-align: center;">R/W</td> </tr> </table> <p>RW units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
10	VFW units clock gate disable <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px; text-align: center;">R/W</td> </tr> </table> <p>VFW units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

UCGCTL5 - Unit Level Clock Gating Control 5

	9 VCW unit's clock gate disable		
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td><td style="padding: 2px; text-align: center;">R/W</td></tr> </table> <p>VCW units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
	8 VEO unit's clock gate disable		
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td><td style="padding: 2px; text-align: center;">R/W</td></tr> </table> <p>VEO units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
	7 VDN unit's clock gate disable		
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td><td style="padding: 2px; text-align: center;">R/W</td></tr> </table> <p>VDN units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
	6 VTQunit's clock gate disable		
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td><td style="padding: 2px; text-align: center;">R/W</td></tr> </table> <p>VTQunits Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
	5 VPRunit's clock gate disable		
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td><td style="padding: 2px; text-align: center;">R/W</td></tr> </table> <p>VPR units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
	4 IMEunit's clock gate disable		
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td><td style="padding: 2px; text-align: center;">R/W</td></tr> </table> <p>IME units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

UCGCTL5 - Unit Level Clock Gating Control 5

	3 CREunit clock gate disable	Access:	R/W
CRE units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)			
2 GAPSL unit clock gate disable			
	Access:	R/W	
GAPSL units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)			
1 GAPSU Clock gate disable			
	Access:	R/W	
GAPSU units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)			
0 SPMunit Clock gate disable			
	Access:	R/W	
SPM units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)			

Unit Level Clock Gating Control 6

UCGCTL6 - Unit Level Clock Gating Control 6				
DWord	Bit	Description		
0	30:28	<p>HDCunit clock gate disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>HDC units Clock Gating Disable Control: HDCREQ bit 28, HDCRET bit 29, HDCTLB bit 30. '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W			
27	<p>MUCunit clock gate disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>MUC units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	
Access:	R/W			
26	<p>GACVunit cclk gate disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>GACV units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	
Access:	R/W			
25	<p>GACBunit clock gate disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>GACB units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	
Access:	R/W			

UCGCTL6 - Unit Level Clock Gating Control 6

	GAPSunit clock gate disable	
24	Access: R/W	<p>GAPS units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>
23	GAMTunit clock gate disable	Access: R/W
	GAMT units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
22	Reserved	
22	Reserved	
21	OASCREP	OASCREP units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
20	OAADDRunit clock gate disable bit	OAADDR units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
19	GACVunit clock gate disable	GACV units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
18	BDMunit clock gate disable	BDM units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

UCGCTL6 - Unit Level Clock Gating Control 6

	GATSunit clock gate disable	
17	Access:	R/W
	GATS units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
16	OATREPunit clock gate disable	
	Access:	R/W
	OATREP units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
15	STunit clock gate disable	
	Access:	R/W
	ST units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
14	SDEunit clock gate disable	
	Access:	R/W
	SDE units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) Programming Note :For BDW, steppings this must be set to 1	
13	VIN(VID6) unit clock gate disable	
	Access:	R/W
	VIN(VID6) units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
12	VIN(VID5) unit clock gate disable	
	Access:	R/W
	VIN(VID5) units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	

UCGCTL6 - Unit Level Clock Gating Control 6

	11 WVOPunit clock gate disable		
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px; text-align: right;">R/W</td> </tr> </table> <p>WVOP units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
	10 WUSB unit clock gate disable		
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px; text-align: right;">R/W</td> </tr> </table> <p>WUSB units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
	9 WSECunit clock gate disable		
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px; text-align: right;">R/W</td> </tr> </table> <p>WSEC units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
	8 WRSunit clkok gate disable		
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px; text-align: right;">R/W</td> </tr> </table> <p>WRS units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
	7 WQRCunit clock gate disable		
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px; text-align: right;">R/W</td> </tr> </table> <p>WQRC units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
	6 WMPC unit level clock gate disable		
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px; text-align: right;">R/W</td> </tr> </table> <p>WMPC units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

UCGCTL6 - Unit Level Clock Gating Control 6

	5 WINunit Clock gate disable		
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px; text-align: center;">R/W</td> </tr> </table> <p>WIN units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
	4 WIME unit clock gate disable		
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px; text-align: center;">R/W</td> </tr> </table> <p>WIME units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
	3 WHME unit clock gate disable		
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px; text-align: center;">R/W</td> </tr> </table> <p>WHME units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
	2 WAVMunit Clock Gate Disable		
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px; text-align: center;">R/W</td> </tr> </table> <p>WAVM units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
	1 VSHMunit clock gate disable		
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px; text-align: center;">R/W</td> </tr> </table> <p>VSHM units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		
	0 VSLunit Clock gating disable		
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px; text-align: center;">R/W</td> </tr> </table> <p>VSL units Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W
Access:	R/W		

URB Context Offset

URB_CXT_OFFSET - URB Context Offset						
DWord	Bit	Description				
0	31:6	<p>URB Offset</p> <table border="1"> <tr> <td>Default Value:</td> <td>26Bh</td> </tr> <tr> <td colspan="2">This field indicates the offset (64bytes granular) in to the logical rendering context to which URB contents are save/restored when enabled. This field register must not be written directly (via MMIO) unless the Command Streamer is completely idle (i.e., the Ring Buffer is empty and the pipeline is idle) and RC6 is disabled. One way to program this register is via Load Register Immediate command in the ring buffer as part of initialization sequence.</td></tr> </table>	Default Value:	26Bh	This field indicates the offset (64bytes granular) in to the logical rendering context to which URB contents are save/restored when enabled. This field register must not be written directly (via MMIO) unless the Command Streamer is completely idle (i.e., the Ring Buffer is empty and the pipeline is idle) and RC6 is disabled. One way to program this register is via Load Register Immediate command in the ring buffer as part of initialization sequence.	
Default Value:	26Bh					
This field indicates the offset (64bytes granular) in to the logical rendering context to which URB contents are save/restored when enabled. This field register must not be written directly (via MMIO) unless the Command Streamer is completely idle (i.e., the Ring Buffer is empty and the pipeline is idle) and RC6 is disabled. One way to program this register is via Load Register Immediate command in the ring buffer as part of initialization sequence.						
5:0	<p>Reserved</p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ			
Format:	MBZ					

UTIL_PIN_CTL

UTIL_PIN_CTL											
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x00000000 Access: R/W Size (in bits): 32											
Address: 48400h-48403h Name: Utility Pin Control ShortName: UTIL_PIN_CTL Valid Projects: BDW Power: Always on Reset: soft											
<p>This register controls the display utility pin. The nominal supply is 1 Volt and can be level shifted depending on usage. The maximum switching frequency is 100 KHz.</p>											
DWord	Bit	Description									
0	31	<p>Util Pin Enable This bit enables the utility pin.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Disable</td></tr> <tr> <td>1b</td><td>Enable</td></tr> </tbody> </table>	Value	Name	0b	Disable	1b	Enable			
Value	Name										
0b	Disable										
1b	Enable										
30:29	<p>Pipe Select This bit selects which pipe will be used when the utility pin is outputting timing related signals.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>00b</td><td>Pipe A</td></tr> <tr> <td>01b</td><td>Pipe B</td></tr> <tr> <td>10b</td><td>Pipe C</td></tr> <tr> <td>11b</td><td>Reserved</td></tr> </tbody> </table>	Value	Name	00b	Pipe A	01b	Pipe B	10b	Pipe C	11b	Reserved
Value	Name										
00b	Pipe A										
01b	Pipe B										
10b	Pipe C										
11b	Reserved										
	<p>Restriction The field should only be changed when the utility pin is disabled or not configured to use any timing signals.</p>										
28	Reserved										

UTIL_PIN_CTL																							
	27:24	<p>Util Pin Mode This bit configures the utility pin mode of operation for output.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0000b</td><td>Data</td><td>Output the Util_Pin_Output_Data value.</td></tr> <tr> <td>0001b</td><td>PWM</td><td>Output from the backlight PWM circuit.</td></tr> <tr> <td>0100b</td><td>Vblank</td><td>Output the vertical blank.</td></tr> <tr> <td>0101b</td><td>Vsync</td><td>Output the vertical sync.</td></tr> <tr> <td>1000b</td><td>Right/Left Eye Level</td><td>Output the stereo 3D right/left eye level signal. Asserted for the left eye and de-asserted for the right eye.</td></tr> <tr> <td>Others</td><td>Reserved</td><td>Reserved</td></tr> </tbody> </table> <p>Restriction The field should only be changed when the utility pin is disabled.</p>	Value	Name	Description	0000b	Data	Output the Util_Pin_Output_Data value.	0001b	PWM	Output from the backlight PWM circuit.	0100b	Vblank	Output the vertical blank.	0101b	Vsync	Output the vertical sync.	1000b	Right/Left Eye Level	Output the stereo 3D right/left eye level signal. Asserted for the left eye and de-asserted for the right eye.	Others	Reserved	Reserved
Value	Name	Description																					
0000b	Data	Output the Util_Pin_Output_Data value.																					
0001b	PWM	Output from the backlight PWM circuit.																					
0100b	Vblank	Output the vertical blank.																					
0101b	Vsync	Output the vertical sync.																					
1000b	Right/Left Eye Level	Output the stereo 3D right/left eye level signal. Asserted for the left eye and de-asserted for the right eye.																					
Others	Reserved	Reserved																					
	23	<p>Util Pin Output Data This bit selects what the value to drive as an output when in the data mode.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0b</td><td>0</td></tr> <tr> <td>1b</td><td>1</td></tr> </tbody> </table>	Value	Name	0b	0	1b	1															
Value	Name																						
0b	0																						
1b	1																						
	22	<p>Util Pin Output Polarity This bit inverts the polarity of the pin output.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Not inverted</td></tr> <tr> <td>1b</td><td>Inverted</td></tr> </tbody> </table>	Value	Name	0b	Not inverted	1b	Inverted															
Value	Name																						
0b	Not inverted																						
1b	Inverted																						
	21:20	Reserved																					
	19:16	Reserved																					
		Project: BDW																					
	15:0	Reserved																					

Valid Bit Vector 0 for CVS

CVSTLB_VLD_0 - Valid Bit Vector 0 for CVS						
DWord	Bit	Description				
0	31:0	<p>Valid Bit Vector 0 for CVS</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Valid Bits per Entry.</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 0 for L3

L3TLB_VLD_0 - Valid Bit Vector 0 for L3						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04D00h					
This register contains the valid bits for entries 0-31 of L3TLB.						
DWord	Bit	Description				
0	31:0	<p>Valid Bit Vector 0 for L3</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Valid Bits per Entry.</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 0 for MFX

MFXTLB_VLD_0 - Valid Bit Vector 0 for MFX						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04BA0h					
This register contains the valid bits for entries 0-31 of MFXTLB.						
DWord	Bit	Description				
0	31:0	<p>Valid Bit Vector 0 for MFX</p> <table border="1"> <tr> <td>Default Value:</td><td>0000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Valid Bits per Entry.</p>	Default Value:	0000000h	Access:	RO
Default Value:	0000000h					
Access:	RO					

Valid Bit Vector 0 for MFX SL1

MFXTLB_VLD_SL1_0 - Valid Bit Vector 0 for MFX SL1								
Register Space:	MMIO: 0/2/0							
Project:	BDW							
Default Value:	0x00000000							
Size (in bits):	32							
Address:	04BC0h							
This register contains the valid bits for entries 0-31 of MFX SL1 TLB.								
DWord	Bit	Description						
0	31:0	<p>Valid Bit Vector 0 for MFX SL1</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> <tr> <td colspan="2">Valid Bits per Entry.</td></tr> </table>	Default Value:	00000000h	Access:	RO	Valid Bits per Entry.	
Default Value:	00000000h							
Access:	RO							
Valid Bits per Entry.								

Valid Bit Vector 0 for MTTLB

MTTLB_VLD0 - Valid Bit Vector 0 for MTTLB		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	04780h-04783h	
This register contains the valid bits for entries 0-31 of MTTLB (Texture and constant cache TLB).		
DWord	Bit	Description
0	31:0	Valid bits per entry

Valid Bit Vector 0 for MTVICTLB

VICTLB_VLD0 - Valid Bit Vector 0 for MTVICTLB		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	04788h-0478Bh	
This register contains the valid bits for entries 0-31 of VICTLB (Vertex Fetch, Instruction Cache, and Command Streamer TLB).		
DWord	Bit	Description
0	31:0	Valid bits per entry

Valid Bit Vector 0 for RCC

RCCTLB_VLD_0 - Valid Bit Vector 0 for RCC						
DWord	Bit	Description				
0	31:0	<p>Valid Bit Vector 0 for RCC</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Valid Bits per Entry.</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 0 for RCCTLB

RCCTLB_VLD0 - Valid Bit Vector 0 for RCCTLB		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	04790h-04793h	
This register contains the valid bits for entries 0-31 of RCCTLB (Render Cache for Color TLB).		
DWord	Bit	Description
0	31:0	Valid bits per entry

Valid Bit Vector 0 for RCZTLB

RCZTLB_VLD0 - Valid Bit Vector 0 for RCZTLB		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	04798h-0479Bh	
This register contains the valid bits for entries 0-31 of RCZTLB (Render Cache for Z (Depth), Hi Z, and Stencil TLB).		
DWord	Bit	Description
0	31:0	Valid bits per entry

Valid Bit Vector 0 for TLBPEND registers

TLBPEND_VLD0 - Valid Bit Vector 0 for TLBPEND registers		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	04700h-04703h	
This register contains the valid bits for entries 0-31 of TLBPEND structure (Cycles pending TLB translation).		
DWord	Bit	Description
0	31:0	Valid bits per entry

Valid Bit Vector 0 for VEBX

VEBXTLB_VLD_0 - Valid Bit Vector 0 for VEBX						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04B20h					
This register contains the valid bits for entries 0-31 of VEBXTLB.						
DWord	Bit	Description				
0	31:0	<p>Valid Bit Vector 0 for VEBX</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Valid Bits per Entry.</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 0 for WIDI

BWDTLB_VLD_0 - Valid Bit Vector 0 for WIDI						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04DC0h					
This register contains the valid bits for entries 0-31 of BWDTLB.						
DWord	Bit	Description				
0	31:0	Valid Bit Vector 0 for WIDI <table border="1"><tr><td>Default Value:</td><td>00000000h</td></tr><tr><td>Access:</td><td>RO</td></tr></table> <p>Valid Bits per Entry.</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 0 for Z

ZTLB_VLD_0 - Valid Bit Vector 0 for Z						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04B34h					
This register contains the valid bits for entries 0-31 of ZTLB.						
DWord	Bit	Description				
0	31:0	<p>Valid Bit Vector 0 for Z</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Valid Bits per Entry.</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 1 for CVS

CVSTLB_VLD_1 - Valid Bit Vector 1 for CVS						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04C04h					
This register contains the valid bits for entries 0-31 of CVSTLB.						
DWord	Bit	Description				
0	31:0	<p>Valid Bit Vector 1 for CVS</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Valid Bits per Entry.</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 1 for L3

L3TLB_VLD_1 - Valid Bit Vector 1 for L3						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04D04h					
This register contains the valid bits for entries 0-31 of L3TLB.						
DWord	Bit	Description				
0	31:0	<p>Valid Bit Vector 1 for L3</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Valid Bits per Entry.</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 1 for MFX

MFXTLB_VLD_1 - Valid Bit Vector 1 for MFX						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04BA4h					
This register contains the valid bits for entries 0-31 of MFXTLB.						
DWord	Bit	Description				
0	31:0	<p>Valid Bit Vector 1 for MFX</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Valid Bits per Entry.</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 1 for MFX SL1

MFXTLB_VLD_SL1_1 - Valid Bit Vector 1 for MFX SL1								
Register Space:	MMIO: 0/2/0							
Project:	BDW							
Default Value:	0x00000000							
Size (in bits):	32							
Address:	04BC4h							
This register contains the valid bits for entries 0-31 of MFX SL1 TLB.								
DWord	Bit	Description						
0	31:0	<p>Valid Bit Vector 1 for MFX SL1</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> <tr> <td colspan="2">Valid Bits per Entry.</td></tr> </table>	Default Value:	00000000h	Access:	RO	Valid Bits per Entry.	
Default Value:	00000000h							
Access:	RO							
Valid Bits per Entry.								

Valid Bit Vector 1 for MTTLB

MTTLB_VLD1 - Valid Bit Vector 1 for MTTLB		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	04784h-04787h	
This register contains the valid bits for entries 0-31 of MTTLB (Texture and constant cache TLBVertex Fetch, Instruction Cache, and Command Streamer TLB).		
DWord	Bit	Description
0	31:0	Valid bits per entry

Valid Bit Vector 1 for MTVICTLB

MTVICTLB_VLD1 - Valid Bit Vector 1 for MTVICTLB

Register Space: MMIO: 0/2/0

Project: BDW

Source: RenderCS

Default Value: 0x00000000

Access: RO

Size (in bits): 32

Trusted Type: 1

Address: 0478Ch-0478Fh

This register contains the valid bits for entries 0-31 of VICTLB (Vertex Fetch, Instruction Cache, and Command Streamer TLB).

DWord	Bit	Description
0	31:0	Valid bits per entry

Valid Bit Vector 1 for RCC

RCCTLB_VLD_1 - Valid Bit Vector 1 for RCC						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04DA44h					
This register contains the valid bits for entries 0-31 of RCCTLB.						
DWord	Bit	Description				
0	31:0	<p>Valid Bit Vector 1 for RCC</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Valid Bits per Entry.</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 1 for RCCTLB

RCCTLB_VLD1 - Valid Bit Vector 1 for RCCTLB		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	04794h-04797h	
This register is reserved for future RCC TLB extension.		
DWord	Bit	Description
0	31:0	Reserved Format: MBZ

Valid Bit Vector 1 for RCZTLB

RCZTLB_VLD1 - Valid Bit Vector 1 for RCZTLB		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	0479Ch-0479Fh	
This register contains the valid bits for entries 0-31 of RCZTLB (Render Cache for Z (Depth), Hi Z, and Stencil TLB).		
DWord	Bit	Description
0	31:0	Valid bits per entry

Valid Bit Vector 1 for TLBPEND registers

TLBPEND_VLD1 - Valid Bit Vector 1 for TLBPEND registers		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Source:	RenderCS	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Trusted Type:	1	
Address:	04704h-04707h	
This register contains the valid bits for entries 32-63 of TLBPEND structure (Cycles pending TLB translation).		
DWord	Bit	Description
0	31:0	Valid bits per entry

Valid Bit Vector 1 for VEBX

VEBXTLB_VLD_1 - Valid Bit Vector 1 for VEBX						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04B24h					
This register contains the valid bits for entries 0-31 of VEBXTLB.						
DWord	Bit	Description				
0	31:0	<p>Valid Bit Vector 1 for VEBX</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Valid Bits per Entry.</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 1 for WIDI

BWDTLB_VLD_1 - Valid Bit Vector 1 for WIDI						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04DC4h					
This register contains the valid bits for entries 0-31 of BWDTLB.						
DWord	Bit	Description				
0	31:0	<p>Valid Bit Vector 1 for WIDI</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Valid Bits per Entry.</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 1 for Z

ZTLB_VLD_1 - Valid Bit Vector 1 for Z						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04B38h					
This register contains the valid bits for entries 0-31 of ZTLB.						
DWord	Bit	Description				
0	31:0	<p>Valid Bit Vector 1 for Z</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Valid Bits per Entry.</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 2 for CVS

CVSTLB_VLD_2 - Valid Bit Vector 2 for CVS						
DWord	Bit	Description				
0	31:0	<p>Valid Bit Vector 2 for CVS</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Valid Bits per Entry.</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 2 for GAB

BWDTLB_VLD_3 - Valid Bit Vector 2 for GAB						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04DCCh					
This register contains the valid bits for entries 0-31 of BWDTLB.						
DWord	Bit	Description				
0	31:0	<p>Valid Bit Vector 3 for GAB</p> <table border="1"> <tr> <td>Default Value:</td><td>0000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Valid Bits per Entry.</p>	Default Value:	0000000h	Access:	RO
Default Value:	0000000h					
Access:	RO					

Valid Bit Vector 2 for L3

L3TLB_VLD_2 - Valid Bit Vector 2 for L3						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04D08h					
This register contains the valid bits for entries 0-31 of L3TLB.						
DWord	Bit	Description				
0	31:0	<p>Valid Bit Vector 2 for L3</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Valid Bits per Entry.</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 2 for MFX

MFXTLB_VLD_2 - Valid Bit Vector 2 for MFX						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04BA8h					
This register contains the valid bits for entries 0-31 of MFXTLB.						
DWord	Bit	Description				
0	31:0	<p>Valid Bit Vector 2 for MFX</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Valid Bits per Entry.</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 2 for MFX SL1

MFXTLB_VLD_SL1_2 - Valid Bit Vector 2 for MFX SL1								
Register Space:	MMIO: 0/2/0							
Project:	BDW							
Default Value:	0x00000000							
Size (in bits):	32							
Address:	04BC8h							
This register contains the valid bits for entries 0-31 of MFX SL1 TLB.								
DWord	Bit	Description						
0	31:0	<p>Valid Bit Vector 2 for MFX SL1</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> <tr> <td colspan="2">Valid Bits per Entry.</td></tr> </table>	Default Value:	00000000h	Access:	RO	Valid Bits per Entry.	
Default Value:	00000000h							
Access:	RO							
Valid Bits per Entry.								

Valid Bit Vector 2 for RCC

RCCTLB_VLD_2 - Valid Bit Vector 2 for RCC						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04DA8h					
This register contains the valid bits for entries 0-31 of RCCTLB.						
DWord	Bit	Description				
0	31:0	<p>Valid Bit Vector 2 for RCC</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Valid Bits per Entry.</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 2 for Z

ZTLB_VLD_2 - Valid Bit Vector 2 for Z						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04B3Ch					
This register contains the valid bits for entries 0-31 of ZTLB.						
DWord	Bit	Description				
0	31:0	<p>Valid Bit Vector 2 for Z</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Valid Bits per Entry.</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 3 for CVS

CVSTLB_VLD_3 - Valid Bit Vector 3 for CVS						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04C0Ch					
This register contains the valid bits for entries 0-31 of CVSTLB.						
DWord	Bit	Description				
0	31:0	<p>Valid Bit Vector 3 for CVS</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Valid Bits per Entry.</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 3 for L3

L3TLB_VLD_3 - Valid Bit Vector 3 for L3						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04D0Ch					
This register contains the valid bits for entries 0-31 of L3TLB.						
DWord	Bit	Description				
0	31:0	<p>Valid Bit Vector 3 for L3</p> <table border="1"> <tr> <td>Default Value:</td><td>0000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Valid Bits per Entry.</p>	Default Value:	0000000h	Access:	RO
Default Value:	0000000h					
Access:	RO					

Valid Bit Vector 3 for MFX

MFXTLB_VLD_3 - Valid Bit Vector 3 for MFX						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04BACCh					
This register contains the valid bits for entries 0-31 of MFXTLB.						
DWord	Bit	Description				
0	31:0	Valid Bit Vector 3 for MFX <table border="1"><tr><td>Default Value:</td><td>00000000h</td></tr><tr><td>Access:</td><td>RO</td></tr></table> <p>Valid Bits per Entry.</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 3 for MFX SL1

MFXTLB_VLD_SL1_3 - Valid Bit Vector 3 for MFX SL1								
Register Space:	MMIO: 0/2/0							
Project:	BDW							
Default Value:	0x00000000							
Size (in bits):	32							
Address:	04BCCh							
This register contains the valid bits for entries 0-31 of MFX SL1 TLB.								
DWord	Bit	Description						
0	31:0	<p>Valid Bit Vector 3 for MFX SL1</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> <tr> <td colspan="2">Valid Bits per Entry.</td></tr> </table>	Default Value:	00000000h	Access:	RO	Valid Bits per Entry.	
Default Value:	00000000h							
Access:	RO							
Valid Bits per Entry.								

Valid Bit Vector 3 for RCC

RCCTLB_VLD_3 - Valid Bit Vector 3 for RCC						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04DACH					
This register contains the valid bits for entries 0-31 of RCCTLB.						
DWord	Bit	Description				
0	31:0	<p>Valid Bit Vector 3 for RCC</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Valid Bits per Entry.</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 3 for Z

ZTLB_VLD_3 - Valid Bit Vector 3 for Z						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04B40h					
This register contains the valid bits for entries 0-31 of ZTLB.						
DWord	Bit	Description				
0	31:0	<p>Valid Bit Vector 3 for Z</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Valid Bits per Entry.</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 4 for L3

L3TLB_VLD_4 - Valid Bit Vector 4 for L3						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04D10h					
This register contains the valid bits for entries 0-31 of L3TLB.						
DWord	Bit	Description				
0	31:0	<p>Valid Bit Vector 4 for L3</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Valid Bits per Entry.</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 4 for MFX

MFXTLB_VLD_4 - Valid Bit Vector 4 for MFX						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04BB0h					
This register contains the valid bits for entries 0-31 of MFXTLB.						
DWord	Bit	Description				
0	31:0	<p>Valid Bit Vector 4 for MFX</p> <table border="1"> <tr> <td>Default Value:</td><td>0000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Valid Bits per Entry.</p>	Default Value:	0000000h	Access:	RO
Default Value:	0000000h					
Access:	RO					

Valid Bit Vector 4 for MFX SL1

MFXTLB_VLD_SL1_4 - Valid Bit Vector 4 for MFX SL1								
Register Space:	MMIO: 0/2/0							
Project:	BDW							
Default Value:	0x00000000							
Size (in bits):	32							
Address:	04BD0h							
This register contains the valid bits for entries 0-31 of MFX SL1 TLB.								
DWord	Bit	Description						
0	31:0	Valid Bit Vector 4 for MFX SL1 <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> <tr> <td colspan="2">Valid Bits per Entry.</td></tr> </table>	Default Value:	00000000h	Access:	RO	Valid Bits per Entry.	
Default Value:	00000000h							
Access:	RO							
Valid Bits per Entry.								

Valid Bit Vector 4 for RCC

RCCTLB_VLD_4 - Valid Bit Vector 4 for RCC						
DWord	Bit	Description				
0	31:0	<p>Valid Bit Vector 4 for RCC</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Valid Bits per Entry.</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 4 for Z

ZTLB_VLD_4 - Valid Bit Vector 4 for Z						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04B44h					
This register contains the valid bits for entries 0-31 of ZTLB.						
DWord	Bit	Description				
0	31:0	<p>Valid Bit Vector 4 for Z</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Valid Bits per Entry.</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 5 for L3

L3TLB_VLD_5 - Valid Bit Vector 5 for L3						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04D14h					
This register contains the valid bits for entries 0-31 of L3TLB.						
DWord	Bit	Description				
0	31:0	<p>Valid Bit Vector 5 for L3</p> <table border="1"> <tr> <td>Default Value:</td><td>0000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Valid Bits per Entry.</p>	Default Value:	0000000h	Access:	RO
Default Value:	0000000h					
Access:	RO					

Valid Bit Vector 5 for MFX

MFXTLB_VLD_5 - Valid Bit Vector 5 for MFX						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04BB4h					
This register contains the valid bits for entries 0-31 of MFXTLB.						
DWord	Bit	Description				
0	31:0	Valid Bit Vector 5 for MFX <table border="1"><tr><td>Default Value:</td><td>0000000h</td></tr><tr><td>Access:</td><td>RO</td></tr></table> <p>Valid Bits per Entry.</p>	Default Value:	0000000h	Access:	RO
Default Value:	0000000h					
Access:	RO					

Valid Bit Vector 5 for MFX SL1

MFXTLB_VLD_SL1_5 - Valid Bit Vector 5 for MFX SL1								
Register Space:	MMIO: 0/2/0							
Project:	BDW							
Default Value:	0x00000000							
Size (in bits):	32							
Address:	04BD4h							
This register contains the valid bits for entries 0-31 of MFX SL1 TLB.								
DWord	Bit	Description						
0	31:0	<p>Valid Bit Vector 5 for MFX SL1</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> <tr> <td colspan="2">Valid Bits per Entry.</td></tr> </table>	Default Value:	00000000h	Access:	RO	Valid Bits per Entry.	
Default Value:	00000000h							
Access:	RO							
Valid Bits per Entry.								

Valid Bit Vector 5 for RCC

RCCTLB_VLD_5 - Valid Bit Vector 5 for RCC						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04DB4h					
This register contains the valid bits for entries 0-31 of RCCTLB.						
DWord	Bit	Description				
0	31:0	<p>Valid Bit Vector 5 for RCC</p> <table border="1"> <tr> <td>Default Value:</td><td>0000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Valid Bits per Entry.</p>	Default Value:	0000000h	Access:	RO
Default Value:	0000000h					
Access:	RO					

Valid Bit Vector 5 for Z

ZTLB_VLD_5 - Valid Bit Vector 5 for Z						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04B48h					
This register contains the valid bits for entries 0-31 of ZTLB.						
DWord	Bit	Description				
0	31:0	<p>Valid Bit Vector 5 for Z</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Valid Bits per Entry.</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 6 for L3

L3TLB_VLD_6 - Valid Bit Vector 6 for L3						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04D18h					
This register contains the valid bits for entries 0-31 of L3TLB.						
DWord	Bit	Description				
0	31:0	<p>Valid Bit Vector 6 for L3</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Valid Bits per Entry.</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 6 for MFX

MFXTLB_VLD_6 - Valid Bit Vector 6 for MFX						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04BB8h					
This register contains the valid bits for entries 0-31 of MFXTLB.						
DWord	Bit	Description				
0	31:0	<p>Valid Bit Vector 6 for MFX</p> <table border="1"> <tr> <td>Default Value:</td><td>0000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Valid Bits per Entry.</p>	Default Value:	0000000h	Access:	RO
Default Value:	0000000h					
Access:	RO					

Valid Bit Vector 6 for MFX SL1

MFXTLB_VLD_SL1_6 - Valid Bit Vector 6 for MFX SL1								
Register Space:	MMIO: 0/2/0							
Project:	BDW							
Default Value:	0x00000000							
Size (in bits):	32							
Address:	04BD8h							
This register contains the valid bits for entries 0-31 of MFX SL1 TLB.								
DWord	Bit	Description						
0	31:0	<p>Valid Bit Vector 6 for MFX SL1</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> <tr> <td colspan="2">Valid Bits per Entry.</td></tr> </table>	Default Value:	00000000h	Access:	RO	Valid Bits per Entry.	
Default Value:	00000000h							
Access:	RO							
Valid Bits per Entry.								

Valid Bit Vector 6 for RCC

RCCTLB_VLD_6 - Valid Bit Vector 6 for RCC						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04DB8h					
This register contains the valid bits for entries 0-31 of RCCTLB.						
DWord	Bit	Description				
0	31:0	<p>Valid Bit Vector 6 for RCC</p> <table border="1"> <tr> <td>Default Value:</td><td>0000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Valid Bits per Entry.</p>	Default Value:	0000000h	Access:	RO
Default Value:	0000000h					
Access:	RO					

Valid Bit Vector 6 for Z

ZTLB_VLD_6 - Valid Bit Vector 6 for Z						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04B4Ch					
This register contains the valid bits for entries 0-31 of ZTLB.						
DWord	Bit	Description				
0	31:0	<p>Valid Bit Vector 6 for Z</p> <table border="1"> <tr> <td>Default Value:</td><td>0000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Valid Bits per Entry.</p>	Default Value:	0000000h	Access:	RO
Default Value:	0000000h					
Access:	RO					

Valid Bit Vector 7 for L3

L3TLB_VLD_7 - Valid Bit Vector 7 for L3						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04D1Ch					
This register contains the valid bits for entries 0-31 of L3TLB.						
DWord	Bit	Description				
0	31:0	<p>Valid Bit Vector 7 for L3</p> <table border="1"> <tr> <td>Default Value:</td><td>0000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Valid Bits per Entry.</p>	Default Value:	0000000h	Access:	RO
Default Value:	0000000h					
Access:	RO					

Valid Bit Vector 7 for MFX

MFXTLB_VLD_7 - Valid Bit Vector 7 for MFX						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04BBCh					
This register contains the valid bits for entries 0-31 of MFXTLB.						
DWord	Bit	Description				
0	31:0	<p>Valid Bit Vector 7 for MFX</p> <table border="1"> <tr> <td>Default Value:</td><td>0000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Valid Bits per Entry.</p>	Default Value:	0000000h	Access:	RO
Default Value:	0000000h					
Access:	RO					

Valid Bit Vector 7 for MFX SL1

MFXTLB_VLD_SL1_7 - Valid Bit Vector 7 for MFX SL1								
Register Space:	MMIO: 0/2/0							
Project:	BDW							
Default Value:	0x00000000							
Size (in bits):	32							
Address:	04BDCh							
This register contains the valid bits for entries 0-31 of MFX SL1 TLB.								
DWord	Bit	Description						
0	31:0	<p>Valid Bit Vector 7 for MFX SL1</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> <tr> <td colspan="2">Valid Bits per Entry.</td></tr> </table>	Default Value:	00000000h	Access:	RO	Valid Bits per Entry.	
Default Value:	00000000h							
Access:	RO							
Valid Bits per Entry.								

Valid Bit Vector 7 for RCC

RCCTLB_VLD_7 - Valid Bit Vector 7 for RCC						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04DBCh					
This register contains the valid bits for entries 0-31 of RCCTLB.						
DWord	Bit	Description				
0	31:0	<p>Valid Bit Vector 7 for RCC</p> <table border="1"> <tr> <td>Default Value:</td><td>0000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Valid Bits per Entry.</p>	Default Value:	0000000h	Access:	RO
Default Value:	0000000h					
Access:	RO					

Valid Bit Vector 7 for Z

ZTLB_VLD_7 - Valid Bit Vector 7 for Z						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04B50h					
This register contains the valid bits for entries 0-31 of ZTLB.						
DWord	Bit	Description				
0	31:0	<p>Valid Bit Vector 7 for Z</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Valid Bits per Entry.</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 8 for L3

L3TLB_VLD_8 - Valid Bit Vector 8 for L3						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04D20h					
This register contains the valid bits for entries 0-31 of L3TLB.						
DWord	Bit	Description				
0	31:0	<p>Valid Bit Vector 8 for L3</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Valid Bits per Entry.</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 8 for Z

ZTLB_VLD_8 - Valid Bit Vector 8 for Z						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04B54h					
This register contains the valid bits for entries 0-31 of ZTLB.						
DWord	Bit	Description				
0	31:0	<p>Valid Bit Vector 8 for Z</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Valid Bits per Entry.</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 9 for L3

L3TLB_VLD_9 - Valid Bit Vector 9 for L3						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04D24h					
This register contains the valid bits for entries 0-31 of L3TLB.						
DWord	Bit	Description				
0	31:0	<p>Valid Bit Vector 9 for L3</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Valid Bits per Entry.</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 9 for Z

ZTLB_VLD_9 - Valid Bit Vector 9 for Z						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04B58h					
This register contains the valid bits for entries 0-31 of ZTLB.						
DWord	Bit	Description				
0	31:0	<p>Valid Bit Vector 9 for Z</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Valid Bits per Entry.</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 10 for L3

L3TLB_VLD_10 - Valid Bit Vector 10 for L3						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04D28h					
This register contains the valid bits for entries 0-31 of L3TLB.						
DWord	Bit	Description				
0	31:0	<p>Valid Bit Vector 10 for L3</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Valid Bits per Entry.</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 10 for Z

ZTLB_VLD_10 - Valid Bit Vector 10 for Z						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04B5Ch					
This register contains the valid bits for entries 0-31 of ZTLB.						
DWord	Bit	Description				
0	31:0	<p>Valid Bit Vector 10 for Z</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Valid Bits per Entry.</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 11 for L3

L3TLB_VLD_11 - Valid Bit Vector 11 for L3						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04D2Ch					
This register contains the valid bits for entries 0-31 of L3TLB.						
DWord	Bit	Description				
0	31:0	Valid Bit Vector 11 for L3 <table border="1"><tr><td>Default Value:</td><td>00000000h</td></tr><tr><td>Access:</td><td>RO</td></tr></table> <p>Valid Bits per Entry.</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 11 for Z

ZTLB_VLD_11 - Valid Bit Vector 11 for Z						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04B60h					
This register contains the valid bits for entries 0-31 of ZTLB.						
DWord	Bit	Description				
0	31:0	<p>Valid Bit Vector 11 for Z</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Valid Bits per Entry.</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 12 for L3

L3TLB_VLD_12 - Valid Bit Vector 12 for L3						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04D30h					
This register contains the valid bits for entries 0-31 of L3TLB.						
DWord	Bit	Description				
0	31:0	<p>Valid Bit Vector 12 for L3</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Valid Bits per Entry.</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 12 for Z

ZTLB_VLD_12 - Valid Bit Vector 12 for Z						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04B64h					
This register contains the valid bits for entries 0-31 of ZTLB.						
DWord	Bit	Description				
0	31:0	<p>Valid Bit Vector 12 for Z</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Valid Bits per Entry.</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 13 for L3

L3TLB_VLD_13 - Valid Bit Vector 13 for L3						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04D34h					
This register contains the valid bits for entries 0-31 of L3TLB.						
DWord	Bit	Description				
0	31:0	Valid Bit Vector 13 for L3 <table border="1"><tr><td>Default Value:</td><td>00000000h</td></tr><tr><td>Access:</td><td>RO</td></tr></table> <p>Valid Bits per Entry.</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 13 for Z

ZTLB_VLD_13 - Valid Bit Vector 13 for Z						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04B68h					
This register contains the valid bits for entries 0-31 of ZTLB.						
DWord	Bit	Description				
0	31:0	<p>Valid Bit Vector 13 for Z</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Valid Bits per Entry.</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 14 for L3

L3TLB_VLD_14 - Valid Bit Vector 14 for L3						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04D38h					
This register contains the valid bits for entries 0-31 of L3TLB.						
DWord	Bit	Description				
0	31:0	<p>Valid Bit Vector 14 for L3</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Valid Bits per Entry.</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 14 for Z

ZTLB_VLD_14 - Valid Bit Vector 14 for Z						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04B6Ch					
This register contains the valid bits for entries 0-31 of ZTLB.						
DWord	Bit	Description				
0	31:0	<p>Valid Bit Vector 14 for Z</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Valid Bits per Entry.</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 15 for L3

L3TLB_VLD_15 - Valid Bit Vector 15 for L3						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04D3Ch					
This register contains the valid bits for entries 0-31 of L3TLB.						
DWord	Bit	Description				
0	31:0	<p>Valid Bit Vector 15 for L3</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Valid Bits per Entry.</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 15 for Z

ZTLB_VLD_15 - Valid Bit Vector 15 for Z						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04B70h					
This register contains the valid bits for entries 0-31 of ZTLB.						
DWord	Bit	Description				
0	31:0	<p>Valid Bit Vector 15 for Z</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Valid Bits per Entry.</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 16 for L3

L3TLB_VLD_16 - Valid Bit Vector 16 for L3						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04D40h					
This register contains the valid bits for entries 0-31 of L3TLB.						
DWord	Bit	Description				
0	31:0	<p>Valid Bit Vector 16 for L3</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Valid Bits per Entry.</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 17 for L3

L3TLB_VLD_17 - Valid Bit Vector 17 for L3						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04D44h					
This register contains the valid bits for entries 0-31 of L3TLB.						
DWord	Bit	Description				
0	31:0	<p>Valid Bit Vector 17 for L3</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Valid Bits per Entry.</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 18 for L3

L3TLB_VLD_18 - Valid Bit Vector 18 for L3						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04D48h					
This register contains the valid bits for entries 0-31 of L3TLB.						
DWord	Bit	Description				
0	31:0	<p>Valid Bit Vector 18 for L3</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Valid Bits per Entry.</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 19 for L3

L3TLB_VLD_19 - Valid Bit Vector 19 for L3						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04D4Ch					
This register contains the valid bits for entries 0-31 of L3TLB.						
DWord	Bit	Description				
0	31:0	<p>Valid Bit Vector 19 for L3</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Valid Bits per Entry.</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 20 for L3

L3TLB_VLD_20 - Valid Bit Vector 20 for L3						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04D50h					
This register contains the valid bits for entries 0-31 of L3TLB.						
DWord	Bit	Description				
0	31:0	<p>Valid Bit Vector 20 for L3</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Valid Bits per Entry.</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 21 for L3

L3TLB_VLD_21 - Valid Bit Vector 21 for L3						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04D54h					
This register contains the valid bits for entries 0-31 of L3TLB.						
DWord	Bit	Description				
0	31:0	<p>Valid Bit Vector 21 for L3</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Valid Bits per Entry.</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 22 for L3

L3TLB_VLD_22 - Valid Bit Vector 22 for L3						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04D58h					
This register contains the valid bits for entries 0-31 of L3TLB.						
DWord	Bit	Description				
0	31:0	<p>Valid Bit Vector 22 for L3</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Valid Bits per Entry.</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector 23 for L3

L3TLB_VLD_23 - Valid Bit Vector 23 for L3						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04D5Ch					
This register contains the valid bits for entries 0-31 of L3TLB.						
DWord	Bit	Description				
0	31:0	<p>Valid Bit Vector 23 for L3</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Valid Bits per Entry.</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector for VLF

VLFTLB_VLD - Valid Bit Vector for VLF						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04B30h					
This register contains the valid bits for entries 0-31 of VLFTLB.						
DWord	Bit	Description				
0	31:0	<p>Valid Bit Vector for VLF</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Valid Bits per Entry.</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Valid Bit Vector for VLFSL1

VLFSL1TLB_VLD - Valid Bit Vector for VLFSL1						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	04B2Ch					
This register contains the valid bits for entries 0-31 of VLFSL1TLB.						
DWord	Bit	Description				
0	31:0	<p>Valid Bit Vector for VLFSL1</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Valid Bits per Entry.</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

VBLANK

VBLANK			
Register Space: MMIO: 0/2/0 Project: DevLPT:H Default Value: 0x00000000 Access: R/W Size (in bits): 32			
Address: E0010h-E0013h Name: Transcoder A Vertical Blank ShortName: TRANS_VBLANK_A Power: Always on Reset: soft			
DWord	Bit	Description	
0	31:29	Reserved	Format: MBZ
	28:16	Vertical Blank End This field specifies Vertical Blank End position relative to the vertical active display start. The minimum vertical blank size is 5 lines. This register must always be programmed to the same value as the Vertical Total.	
	15:13	Reserved	Format: MBZ
	12:0	Vertical Blank Start This field specifies the Vertical Blank Start position relative to the vertical active display start. This register must always be programmed to the same value as the Vertical Active	

VCES Idle Switch Delay

VECS_IDLEDLY - VCES Idle Switch Delay							
Register Space: MMIO: 0/2/0 Project: BDW Source: VideoEnhancementCS Default Value: 0x00000000 Access: R/W Size (in bits): 32							
Address: 1A23Ch							
<p>The IDLEDLY register contains an Idle Delay field which specifies the minimum number of microseconds allowed for command streamer to wait before a context is switched out leading to IDLE state in execlists mode, i.e following this context switch there is no active element available in HW to execute.</p> <p>A default value of 0, means that by default, there is no restriction to wait on a context switch leading to IDLE. This register has no significance when execlists are not enabled.</p>							
DWord	Bit	Description					
0	31:21	Reserved <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	All	Format:	MBZ	
Project:	All						
Format:	MBZ						
20:0	IDLE Delay <table border="1"> <tr> <td>Default Value:</td><td>0h</td></tr> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U21</td></tr> </table> <p>Minimum number of micro-seconds allowed.</p>	Default Value:	0h	Project:	All	Format:	U21
Default Value:	0h						
Project:	All						
Format:	U21						

VCS_PREEMPTION_HINT

VCS_PREEMPTION_HINT - VCS_PREEMPTION_HINT

Register Space: MMIO: 0/2/0

Project: BDW

Source: VideoCS

Default Value: 0x00000000

Access: R/W

Size (in bits): 32

Address: 124BCh

Valid Projects: [BDW]

Address: 1C4BCh

Valid Projects: [BDW:GT3]

This register contains the Head pointer offset in to the Ring Buffer or the Dword aligned Graphics address in to the Batch Buffer corresponding to either MI_ARB_CHECK called Preemption Hint Address. When Preemption Hint Address is enabled, VCS will honor UHPTTR only on parsing MI_ARB_CHK at Preemption Hint Address.

This register contains the Head pointer offset into the Ring Buffer or the Dword aligned Graphics address into the Batch Buffer corresponding to the below listed commands in execlist mode of operation

- MI_ARB_CHECK
- MI_WAIT_FOR_EVENT
- MI_SEMAPHORE_WAIT

Programming Notes

Programming Restriction: This register should NEVER be programmed in functional mode, this should be used only in validation mode to achieve deterministic behavior of UHPTTR being sampled by a given MI_ARB_CHECK in command stream. Programmer has to ensure that VCS Preemption Hint register gets programmed before UHPTTR is programmed and well before VCS crosses the corresponding execution point. Preemption hint for both RingBuffer and Batch Buffer can't be enabled simultaneously.

DWord	Bit	Description				
0	31:2	Preempted Hint Address <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Format:</td><td style="width: 50%;">U30</td></tr> <tr> <td>Format:</td><td>GraphicsAddress[31:2]</td></tr> </table> <p>This field contains the Head offset in to the Ring Buffer when Preemption Hint is set to Ring Buffer and Dword aligned Graphics Address in to the batch buffer when Preemption Hint is set to Batch Buffer.</p>	Format:	U30	Format:	GraphicsAddress[31:2]
Format:	U30					
Format:	GraphicsAddress[31:2]					

VCS_PREEMPTION_HINT - VCS_PREEMPTION_HINT

	1	Batch Buffer Preemption Hint									
		Format: <input type="text"/> Enable									
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Disabled</td> <td>Preemption hint is disabled in batch buffer.</td> </tr> <tr> <td>1h</td> <td>Enabled</td> <td>Preemption hint is enabled in ring buffer and preemption hint address corresponds to the instruction in Batch Buffer.</td> </tr> </tbody> </table>	Value	Name	Description	0h	Disabled	Preemption hint is disabled in batch buffer.	1h	Enabled	Preemption hint is enabled in ring buffer and preemption hint address corresponds to the instruction in Batch Buffer.
Value	Name	Description									
0h	Disabled	Preemption hint is disabled in batch buffer.									
1h	Enabled	Preemption hint is enabled in ring buffer and preemption hint address corresponds to the instruction in Batch Buffer.									
	0	Ring Preemption Hint									
		Format: <input type="text"/> Enable									
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Disable</td> <td>Preemption hint is disabled in ring buffer.</td> </tr> <tr> <td>1h</td> <td>Enabled</td> <td>Preemption hint is enabled in ring buffer and preemption hint address corresponds to the instruction in Ring Buffer.</td> </tr> </tbody> </table>	Value	Name	Description	0h	Disable	Preemption hint is disabled in ring buffer.	1h	Enabled	Preemption hint is enabled in ring buffer and preemption hint address corresponds to the instruction in Ring Buffer.
Value	Name	Description									
0h	Disable	Preemption hint is disabled in ring buffer.									
1h	Enabled	Preemption hint is enabled in ring buffer and preemption hint address corresponds to the instruction in Ring Buffer.									

VCS_PREEMPTION_HINT_UDW

VCS_PREEMPTION_HINT_UDW - VCS_PREEMPTION_HINT_UDW				
Register Space:	MMIO: 0/2/0			
Project:	BDW			
Source:	VideoCS			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Address:	124C8h			
Valid Projects:	[BDW]			
Address:	1C4C8h			
Valid Projects:	[BDW:GT3]			
This register contains the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space of the Batch Buffer corresponding to MI_ARB_CHECK command called Preemption Hint Address.				
Programming Notes				
Programming Restriction: This register should NEVER be programmed in functional mode, this should be used only in validation mode to achieve deterministic behavior of UHPTTR being sampled by a given MI_ARB_CHK in command stream.				
DWord	Bit	Description		
0	31:16	Reserved <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Format:</td><td style="width: 50%;">MBZ</td></tr> </table>	Format:	MBZ
	Format:	MBZ		
15:0	Preempted Hint Address Upper DWORD <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Format:</td><td style="width: 50%;">GraphicsAddress[47:32]</td></tr> </table> <p>This field contains the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space of the batch buffer when Preemption Hint is set to Batch Buffer. This field is not valid when Preemption Hint is set to Ring Buffer.</p>	Format:	GraphicsAddress[47:32]	
Format:	GraphicsAddress[47:32]			

VCS2 CSB Fifo Status Register

VCS2_CSB_FSR - VCS2 CSB Fifo Status Register		
DWord	Bit	Description
0	31	Not Empty Access: RO
	30:13	Reserved
	12:8	FIFO Maximum Occupancy Count
	7:5	Reserved
	4:0	FIFO Occupancy Count Project: BDW Access: RO

VCS Context ID Preemption Hint

VCS_CTXID_PREEMPTION_HINT - VCS Context ID Preemption Hint				
Register Space:	MMIO: 0/2/0			
Project:	BDW			
Source:	VideoCS			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Address:	124CCh			
Valid Projects:	[BDW]			
Address:	1C4CCh			
Valid Projects:	[BDW:GT3]			
<p>This register contains the Context ID of a context in execlist mode of operation. In execlist mode of operation VCS_PREEMPTION_HINT registers are looked at by Video Command Streamer on executing a context having Context ID that matches with the contents of this register. This register contents are valid and looked at only in execlist mode of operation.</p>				
Programming Notes				
<p>This register should NEVER be programmed in functional mode, this must be used only in validation mode to achieve deterministic preemption behavior in execlist mode of operation.</p>				
DWord	Bit	Description		
0	31:0	Context ID Preemption Hint <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Format:</td><td style="padding: 2px; text-align: right;">U32</td></tr> </table> <p>If 0 this field has no effect. If nonzero it indicates the only context ID that can be preempted when execlists are enabled. A preemption attempt when the context ID of the currently executing ring context does not match this field will be ignored.</p>	Format:	U32
Format:	U32			

VCS Context Sizes

VCS_CXT_SIZE - VCS Context Sizes									
DWord	Bit	Description							
0	31:21	Reserved <table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ					
Format:	MBZ								
20:16	VCS Context Size <table border="1"> <tr> <td>Format:</td><td>U5</td></tr> </table> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Project</th></tr> </thead> <tbody> <tr> <td>Ah</td><td>[Default]</td><td>BDW</td></tr> </tbody> </table>	Format:	U5	Value	Name	Project	Ah	[Default]	BDW
Format:	U5								
Value	Name	Project							
Ah	[Default]	BDW							
15:13	Reserved <table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ						
Format:	MBZ								
12:8	VCR Context Size <table border="1"> <tr> <td>Format:</td><td>U5</td></tr> </table> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Project</th></tr> </thead> <tbody> <tr> <td>11h</td><td>[Default]</td><td>BDW</td></tr> </tbody> </table>	Format:	U5	Value	Name	Project	11h	[Default]	BDW
Format:	U5								
Value	Name	Project							
11h	[Default]	BDW							
7:5	Reserved <table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ						
Format:	MBZ								
4:0	Exclist Context Size <table border="1"> <tr> <td>Format:</td><td>U5</td></tr> </table> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Project</th></tr> </thead> <tbody> <tr> <td>5h</td><td>[Default]</td><td>BDW</td></tr> </tbody> </table>	Format:	U5	Value	Name	Project	5h	[Default]	BDW
Format:	U5								
Value	Name	Project							
5h	[Default]	BDW							

VCS Context Timestamp Count

VCS_CTX_TIMESTAMP - VCS Context Timestamp Count						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Source:	VideoCS					
Default Value:	0x00000000					
Access:	R/W					
Size (in bits):	32					
Address:	123A8h					
Valid Projects:	[BDW]					
Address:	1C3A8h					
Valid Projects:	[BDW:GT3]					
<p>This register provides a mechanism to obtain cumulative run time of a GPU context on HW. This register gets context save/restored on a context switch. SW must reset this register on very first submission of a context to HW, then afterwards gets context save/restored maintaining the cumulative run time of the corresponding context. This register (effectively) counts at a constant frequency by adjusting the increment amount according to the actual reference clock frequency. SW therefore does not need to know the reference clock frequency. This register gets reset on an engine reset.</p> <p>This register is context save restore on a context switch.</p>						
DWord	Bit	Description				
0	31:0	<p>Timestamp Value</p> <table border="1"> <tr> <td>Format:</td><td>U32</td></tr> <tr> <td colspan="2">This register increments for every 80 ns of time.</td></tr> </table>	Format:	U32	This register increments for every 80 ns of time.	
Format:	U32					
This register increments for every 80 ns of time.						

VCS Counter for the bit stream decode engine

VCS_CNTR - VCS Counter for the bit stream decode engine				
Register Space:	MMIO: 0/2/0			
Project:	BDW			
Source:	VideoCS			
Default Value:	0xFFFFFFFF			
Access:	R/W			
Size (in bits):	32			
Address:	12178h-1217Bh			
Valid Projects:	[BDW]			
Address:	1C178h-1C17Bh			
Valid Projects:	[BDW:GT3]			
DWord	Bit	Description		
0	31:0	<p>Count Value</p> <table border="1"> <tr> <td>Default Value:</td><td>ffffffffffh</td></tr> </table> <p>Writing a Zero value to this register starts the counting.</p> <p>Writing a Value of FFFF FFFF to this counter stops the counter.</p>	Default Value:	ffffffffffh
Default Value:	ffffffffffh			

VCS Error Identity Register

VCS_EIR - VCS Error Identity Register												
Register Space: MMIO: 0/2/0 Project: BDW Source: VideoCS Default Value: 0x00000000 Access: R/WC Size (in bits): 32												
Address: 120B0h Valid Projects: [BDW]												
Address: 1C0B0h Valid Projects: [DevBDW:GT3, DevBDW:GT4]												
The EIR register contains the persistent values of Hardware-Detected Error Condition bits. Any bit set in this register will cause the Master Error bit in the ISR to be set. The EIR register is also used by software to clear detected errors (by writing a 1 to the appropriate bit(s) except for the unrecoverable bits described).												
DWord	Bit	Description										
0	31:16	Reserved <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ								
Format:	MBZ											
15:0	Error Identity Bits <table border="1"> <tr> <td>Format:</td> <td>Array of Error condition bits ee the table titled Hardware-Detected Error Bits</td> </tr> </table> <p>This register contains the persistent values of ESR error status bits that are unmasks via the EMR register. The logical OR of all (defined) bits in this register is reported in the Master Error bit of the Interrupt Status Register. In order to clear an error condition, software must first clear the error by writing a 1 to the appropriate bit(s) in this field. If required, software should then proceed to clear the Master Error bit of the IIR.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0h</td><td>[Default]</td><td></td></tr> <tr> <td>1h</td><td>Error occurred</td><td>Error occurred</td></tr> </tbody> </table>	Format:	Array of Error condition bits ee the table titled Hardware-Detected Error Bits	Value	Name	Description	0h	[Default]		1h	Error occurred	Error occurred
Format:	Array of Error condition bits ee the table titled Hardware-Detected Error Bits											
Value	Name	Description										
0h	[Default]											
1h	Error occurred	Error occurred										
Programming Notes Writing a 1 to a set bit will cause that error condition to be cleared. However, the Page Table Error bit (Bit 4) cannot be cleared except by reset (i.e., it is a fatal error).												

VCS Error Mask Register

VCS_EMR - VCS Error Mask Register		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Source:	VideoCS 0xFFFFFFFF [BDW]	
Access:	R/W	
Size (in bits):	32	
Address:	120B4h	
Valid Projects:	[BDW]	
Address:	1C0B4h	
Valid Projects:	[DevBDW:GT3, DevBDW:GT4]	
<p>The EMR register is used by software to control which Error Status Register bits are "masked" or "unmasked". "Unmasked" bits will be reported in the EIR, thus setting the Master Error ISR bit and possibly triggering a CPU interrupt, and will persist in the EIR until cleared by software. "Masked" bits will not be reported in the EIR and therefore cannot generate Master Error conditions or CPU interrupts.</p> <p>Undefined or reserved bits in the Hardware Detected Error Bit Table will always return a read value of '1'</p>		
DWord	Bit	Description
0	31:16	Reserved
		Default Value: FFFFh Project: BDW Format: Must Be One
	15:0	Error Mask Bits
		Format: Array of error condition mask bits See the table titled Hardware-Detected Error Bits. This register contains a bit mask that selects which error condition bits (from the ESR) are reported in the EIR.
Value	Name	Description
0000h	Not Masked	Will be reported in the EIR
FFFFh	Masked [Default]	Will not be reported in the EIR

VCS Error Status Register

VCS_ESR - VCS Error Status Register												
Register Space: MMIO: 0/2/0 Project: BDW Source: VideoCS Default Value: 0x00000000 Access: RO Size (in bits): 32												
Address: 120B8h Valid Projects: [BDW]												
Address: 1C0B8h Valid Projects: [BDW:GT3]												
The ESR register contains the current values of all Hardware-Detected Error condition bits (these are all by definition persistent). The EMR register selects which of these error conditions are reported in the persistent EIR (i.e., set bits must be cleared by software) and thereby causing a Master Error interrupt condition to be reported in the ISR.												
DWord	Bit	Description										
0	31:16	Reserved <table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ								
Format:	MBZ											
15:0	Error Status Bits <table border="1"> <tr> <td>Format:</td><td>Array of error condition bits See the table titled Hardware-Detected Error Bits.</td></tr> </table> <p>This register contains the non-persistent values of all hardware-detected error condition bits.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0h</td><td>[Default]</td><td></td></tr> <tr> <td>1h</td><td>Error Condition Detected</td><td>Error Condition detected</td></tr> </tbody> </table>	Format:	Array of error condition bits See the table titled Hardware-Detected Error Bits.	Value	Name	Description	0h	[Default]		1h	Error Condition Detected	Error Condition detected
Format:	Array of error condition bits See the table titled Hardware-Detected Error Bits.											
Value	Name	Description										
0h	[Default]											
1h	Error Condition Detected	Error Condition detected										

VCS Execute Condition Code Register

VCS_EXCC - VCS Execute Condition Code Register

Register Space:	MMIO: 0/2/0
Project:	BDW
Source:	VideoCS
Default Value:	0x00000000
Access:	R/W, RO
Size (in bits):	32
Trusted Type:	1

Address:	12028h
Valid Projects:	[BDW]

Address:	1C028h
Valid Projects:	[DevBDW:GT3, DevBDW:GT4]

This register contains user defined and hardware generated conditions that are used by MI_WAIT_FOR_EVENT commands. An MI_WAIT_FOR_EVENT instruction excludes the executing ring from arbitration if the selected event evaluates to a 1, while instruction is discarded if the condition evaluates to a 0. Once excluded, a ring is enabled into arbitration when the selected condition evaluates to a 0.

This register also contains control for the invalidation of indirect state pointers on context restore.

DWord	Bit	Description			
0	31:16	Mask Bits <table border="1"> <tr> <td>Format:</td> <td>Mask[15:0]</td> </tr> </table> <p>These bits serve as a write enable for bits 15:0. If this register is written with any of these bits clear the corresponding bit in the field 15:0 will not be modified. Reading these bits always returns 0s.</p>	Format:	Mask[15:0]	
Format:	Mask[15:0]				
15:5	Reserved <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ		
Format:	MBZ				
4:0	Reserved <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	BDW	Format:	MBZ
Project:	BDW				
Format:	MBZ				

VCS General Purpose Register

VCS_GPR - VCS General Purpose Register			
Register Space:	MMIO: 0/2/0		
Project:	BDW		
Source:	VideoCS		
Default Value:	0x00000000, 0x00000000		
Access:	R/W		
Size (in bits):	64		
Address:	12600h-1267Fh		
Valid Projects:	[BDW]		
Address:	1C600h-1C67Fh		
Valid Projects:	[BDW:GT3]		
This is a general purpose register bank of sixteen 64-bit registers, used as temporary storage by the MI_MATH command to do ALU operations.			
Programming Notes			
Any operation that initiates a read to register 0x1266C will return the value of 0x1260c register. This does not include context save or MI_MATH command operation.	Project BDW		
DWord	Bit	Description	
0	63:0	Reserved	Format: MBZ

VCS Hardware Status Mask Register

VCS_HWSTAM - VCS Hardware Status Mask Register

Register Space: MMIO: 0/2/0

Project: BDW

Source: VideoCS

Default Value: 0xFFFFFFFF

Access: R/W

Size (in bits): 32

Trusted Type: 1

Address: 12098h

Valid Projects: [BDW]

Address: 1C098h

Valid Projects: [BDW:GT3]

Access: RO for Reserved Control bits

The HWSTAM register has the same format as the Interrupt Control Registers. The bits in this register are "mask" bits that prevent the corresponding bits in the Interrupt Status Register from generating a "Hardware Status Write" (PCI write cycle). Any unmasked interrupt bit (HWSTAM bit set to 0) will allow the Interrupt Status Register to be written to the ISR location (within the memory page specified by the Hardware Status Page Address Register) when that Interrupt Status Register bit changes state.

Programming Notes

- To write the interrupt to the HWSP, the corresponding IMR bit must also be clear (enabled).
- At most 1 bit can be unmasked at any given time.

DWord	Bit	Description				
0	31:0	<p>Hardware Status Mask Register</p> <table border="1"> <tr> <td>Default Value:</td><td>FFFFFFFFh</td></tr> <tr> <td>Format:</td><td>Array of Masks</td></tr> </table> <p>Refer to the table in the Interrupt Control Register section for bit definitions.</p>	Default Value:	FFFFFFFFh	Format:	Array of Masks
Default Value:	FFFFFFFFh					
Format:	Array of Masks					

VCS Idle Switch Delay

VCS_IDLEDLY - VCS Idle Switch Delay		
Register Space: MMIO: 0/2/0 Project: BDW Source: VideoCS Default Value: 0x00000000 Access: R/W Size (in bits): 32		
Address: 1223Ch Valid Projects: [BDW]		
Address: 1C23Ch Valid Projects: [BDW:GT3]		
The IDLEDLY register contains an Idle Delay field which specifies the minimum number of microseconds allowed for command streamer to wait before a context is switched out leading to IDLE state in Execlist mode, i.e following this context switch there is no active element available in HW to execute. A default value of 0, means that by default, there is no restriction to wait on a context switch leading to IDLE. This register has no significance when Execlists are not enabled.		
DWord	Bit	Description
0	31:21	Reserved
		Project: All Format: MBZ
	20:0	IDLE Delay
		Project: All Format: U21 Minimum number of micro-seconds allowed.

VCS Instruction Parser Mode Register

VCS_INSTPM - VCS Instruction Parser Mode Register						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Source:	VideoCS					
Default Value:	0x00000000					
Access:	R/W					
Size (in bits):	32					
Address:	120C0h-120C3h					
Valid Projects:	[BDW]					
Address:	1C0C0h-1C0C3h					
Valid Projects:	[BDW:GT3]					
The VCS_INSTPM register is used to control the operation of the VCS Instruction Parser. Certain classes of instructions can be disabled (ignored) - often useful for detecting performance bottlenecks. Also, "Synchronizing Flush" operations can be initiated - useful for ensuring the completion (vs. only parsing) of rendering instructions. DefaultValue=0000 0000h						
Programming Notes						
All reserved bits are implemented.						
DWord	Bit	Description				
0	31:16	<p>Masks</p> <table border="1"> <tr> <td>Format:</td><td>Mask[15:0]</td></tr> <tr> <td colspan="2">These bits serve as write enables for bits 15:0. If this register is written with any of these bits clear the corresponding bit in the field 15:0 will not be modified. Reading these bits always returns 0s.</td></tr> </table>	Format:	Mask[15:0]	These bits serve as write enables for bits 15:0. If this register is written with any of these bits clear the corresponding bit in the field 15:0 will not be modified. Reading these bits always returns 0s.	
Format:	Mask[15:0]					
These bits serve as write enables for bits 15:0. If this register is written with any of these bits clear the corresponding bit in the field 15:0 will not be modified. Reading these bits always returns 0s.						
15:11	<p>Reserved</p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	All	Format:	MBZ	
Project:	All					
Format:	MBZ					
10	Reserved					
9	Reserved					
8:7	Reserved					
6:5	Reserved					

VCS_INSTPM - VCS Instruction Parser Mode Register

	4:0	Reserved
		Access:
		Format:

VCS Interrupt Mask Register

VCS_IMR - VCS Interrupt Mask Register																
Register Space:	MMIO: 0/2/0															
Project:	BDW															
Source:	VideoCS															
Default Value:	0xFFFFFFFF															
Access:	R/W															
Size (in bits):	32															
Address:	120A8h															
Valid Projects:	[BDW]															
Address:	1C0A8h															
Valid Projects:	[BDW:GT3]															
<p>The IMR register is used by software to control which Interrupt Status Register bits are masked or unmasked. Unmasked bits will be reported in the IIR, possibly triggering a CPU interrupt, and will persist in the IIR until cleared by software. Masked bits will not be reported in the IIR and therefore cannot generate CPU interrupts.</p>																
DWord	Bit	Description														
0	31:0	<p>Interrupt Mask Bits</p> <table border="1"> <tr> <td>Format:</td> <td>Array of interrupt mask bits Refer to the Interrupt Control Register section for bit definitions.</td> </tr> </table> <p>This field contains a bit mask which selects which interrupt bits (from the ISR) are reported in the IIR.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>FFFF FFFFh</td><td>[Default]</td><td></td></tr> <tr> <td>0h</td><td>Not Masked</td><td>Will be reported in the IIR</td></tr> <tr> <td>1h</td><td>Masked</td><td>Will not be reported in the IIR</td></tr> </tbody> </table>	Format:	Array of interrupt mask bits Refer to the Interrupt Control Register section for bit definitions.	Value	Name	Description	FFFF FFFFh	[Default]		0h	Not Masked	Will be reported in the IIR	1h	Masked	Will not be reported in the IIR
Format:	Array of interrupt mask bits Refer to the Interrupt Control Register section for bit definitions.															
Value	Name	Description														
FFFF FFFFh	[Default]															
0h	Not Masked	Will be reported in the IIR														
1h	Masked	Will not be reported in the IIR														

VCS Mode Register for Software Interface

VCS_MI_MODE - VCS Mode Register for Software Interface														
Register Space: MMIO: 0/2/0 Project: BDW Source: VideoCS 0x00000200 [BDW] Access: R/W Size (in bits): 32														
Address: 1209Ch-1209Fh Valid Projects: [BDW]														
Address: 1C09Ch-1C09Fh Valid Projects: [BDW:GT3]														
The MI_MODE register contains information that controls software interface aspects of the command parser.														
DWord	Bit	Description												
0	31:16	Masks A 1 in a bit in this field allows the modification of the corresponding bit in Bits 15:0.												
	15	Suspend Flush <table border="1"> <tr> <td>Mask:</td><td>MMIO(0x209c)#31</td></tr> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> <tr> <td>0h</td><td>No Delay</td><td>HW will not delay flush, this bit will get cleared by MI_SUSPEND_FLUSH as well</td></tr> <tr> <td>1h</td><td>DelayFlush</td><td>Suspend flush is active</td></tr> </table>	Mask:	MMIO(0x209c)#31	Value	Name	Description	0h	No Delay	HW will not delay flush, this bit will get cleared by MI_SUSPEND_FLUSH as well	1h	DelayFlush	Suspend flush is active	
Mask:	MMIO(0x209c)#31													
Value	Name	Description												
0h	No Delay	HW will not delay flush, this bit will get cleared by MI_SUSPEND_FLUSH as well												
1h	DelayFlush	Suspend flush is active												
14:12	Reserved <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table>	Access:	R/W											
Access:	R/W													
11	Invalidate UHPT enable If bit set H/W clears the valid bit of BCS_UHPT (4134h, bit 0) when current active head pointer is equal to UHPT.													
10	Atomic Read Return for MI_COPY_MEM_MEM <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>U1</td></tr> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> <tr> <td>0h</td><td>Disable [Default]</td><td>Hardware does a regular memory fence write to complete the write to the destination address before moving to the next instruction.</td></tr> <tr> <td>1h</td><td>Enable</td><td>Hardware does Atomic Move with Read Return to complete the write to the destination address before moving to the next instruction.</td></tr> </table>	Project:	BDW	Format:	U1	Value	Name	Description	0h	Disable [Default]	Hardware does a regular memory fence write to complete the write to the destination address before moving to the next instruction.	1h	Enable	Hardware does Atomic Move with Read Return to complete the write to the destination address before moving to the next instruction.
Project:	BDW													
Format:	U1													
Value	Name	Description												
0h	Disable [Default]	Hardware does a regular memory fence write to complete the write to the destination address before moving to the next instruction.												
1h	Enable	Hardware does Atomic Move with Read Return to complete the write to the destination address before moving to the next instruction.												

VCS_MI_MODE - VCS Mode Register for Software Interface

	9	Ring Idle (Read Only Status bit)	
		Access:	RO
<i>Writes to this bit are not allowed.</i>			
Value	Name		
0	Parser not idle		
1	Parser idle [Default]		
	8	Stop Ring	
		Software must set this bit to force the Ring and Command Parser to Idle. Software must read a "1" in Ring Idle bit after setting this bit to ensure that the hardware is idle.	
<i>Software must clear this bit for Ring to resume normal operation.</i>			
Value	Name		
0	Normal Operation		
1	Parser is turned off		
	7:0	Reserved	
		Access:	R/W

VCS Reported Timestamp Count

VCS_TIMESTAMP - VCS Reported Timestamp Count				
Register Space:	MMIO: 0/2/0			
Project:	BDW			
Source:	VideoCS			
Default Value:	0x00000000, 0x00000000			
Access:	RO. This register is not set by the context restore.			
Size (in bits):	64			
Address:	12358h			
Valid Projects:	[BDW]			
Address:	1C358h			
Valid Projects:	[BDW:GT3]			
This register provides an elapsed real-time value that can be used as a timestamp. This register is not reset by a graphics reset. It will maintain its value unless a full chipset reset is performed. Note: This timestamp register reflects the value of the PCU TSC. The PCU TSC counts 10ns increments; this timestamp reflects bits 38:3 of the TSC (i.e. 80ns granularity, rolling over every 1.5 hours).				
DWord	Bit	Description		
0	63:36	Reserved <table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ
Format:	MBZ			
35:0	Timestamp Value <table border="1"> <tr> <td>Format:</td><td>U36</td></tr> </table> <p>This register toggles every 80 ns. The upper 28 bits are zero.</p>	Format:	U36	
Format:	U36			

VCS Reset Control Register

VCS_RESET_CTRL - VCS Reset Control Register				
DWord	Bit	Description		
0	31:16	<p>Mask Bits</p> <table border="1"> <tr> <td>Format:</td> <td>Mask[15:0]</td> </tr> </table> <p>Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)</p>	Format:	Mask[15:0]
Format:	Mask[15:0]			
	15:2	<p>Reserved</p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ
Format:	MBZ			
	1	<p>Ready for Reset</p> <table border="1"> <tr> <td>Format:</td> <td>U1</td> </tr> </table> <p>When set indicates video codec engine is ready for reset. This bit gets cleared on engine reset or when Soft Reset In progress is cleared.</p>	Format:	U1
Format:	U1			
	0	<p>Request Reset</p> <table border="1"> <tr> <td>Format:</td> <td>U1</td> </tr> </table> <p>When set indicates SW wishes to reset the video codec engine. On seeing this bit set Command Streamer will take appropriate action and set Ready For Reset status bit. This bit gets cleared on engine reset.</p>	Format:	U1
Format:	U1			

VCS Ring Buffer Next Context ID Register

VCS_RNCID - VCS Ring Buffer Next Context ID Register		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Source:	VideoCS	
Default Value:	0x00000000, 0x00000000	
Access:	R/W	
Size (in bits):	64	
Address:	12198h-1219Fh	
Valid Projects:	[BDW]	
Address:	1C198h-1C19Fh	
Valid Projects:	[BDW:GT3]	
This register contains the next ring context ID associated with the ring buffer.		
Programming Notes		
The current context (RCCID) register can be updated indirectly from this register on a context switch event. Note that this can only be triggered when arbitration is enabled or if the current context runs dry (head pointer becomes equal to tail pointer).		
DWord	Bit	Description
0	63:0	Context ID See Context Descriptor for VCS.

VCS Semaphore Polling Interval on Wait

VCS_SEMA_WAIT_POLL - VCS Semaphore Polling Interval on Wait				
Register Space:	MMIO: 0/2/0			
Project:	BDW			
Source:	VideoCS			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Address:	1224Ch			
Valid Projects:	[BDW]			
Address:	1C24Ch			
Valid Projects:	[BDW:GT3]			
<p>The SEMA_WAIT_POLL register contains Poll Interval field which specifies the minimum number of microseconds allowed for command streamer to wait before re-fetching the data from the address mentioned in the MI_SEMAPHORE_WAIT command on WAIT Mode set to POLL until the condition is satisfied while the context is not switched out. When value of 0 is written the poll interval will be equal to the memory latency of the read completion.</p>				
DWord	Bit	Description		
0	31:21	Reserved <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Format:</td><td style="width: 50%;">MBZ</td></tr> </table>	Format:	MBZ
Format:	MBZ			
20:0	Poll Interval Minimum number of micro-seconds allowed			

VCS Threshold for the counter of bit stream decode engine

VCS_THRSH - VCS Threshold for the counter of bit stream decode engine		
Register Space: MMIO: 0/2/0 Project: BDW Source: VideoCS Default Value: 0x00150000 Access: R/W Size (in bits): 32		
Address: 1217Ch-1217Fh		
Address: 1C17Ch-1C17Fh		
Valid Projects: [BDW:GT3]		
DWord	Bit	Description
0	31:0	Threshold Value Default Value: 00150000h The value in this register reflects the number of clocks the bit stream decode engine is expected to run. If the value is exceeded the counter is reset and an interrupt may be enabled in the device.

VCW Clock Count

VCW_CLOCK_CNT - VCW Clock Count					
Register Space: MMIO: 0/2/0 Project: BDW Source: VideoEnhancementCS Default Value: 0x00000000 Access: RO Size (in bits): 32 Trusted Type: 1					
Address: 08820h ShortName: VCW0_CLOCK_CNT					
Address: 08920h ShortName: VCW1_CLOCK_CNT					
DWord	Bit	Description			
0	31:24	Reserved <table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ	
Format:	MBZ				
23:0	Max clock count <table border="1"> <tr> <td>Default Value:</td><td>0h</td></tr> <tr> <td colspan="2">Maximum number of clocks taken by VCW to process a column</td></tr> </table>	Default Value:	0h	Maximum number of clocks taken by VCW to process a column	
Default Value:	0h				
Maximum number of clocks taken by VCW to process a column					

VCW Internal Latency

VCW_INTERNAL_LAT - VCW Internal Latency				
Register Space: MMIO: 0/2/0 Project: BDW Source: VideoEnhancementCS Default Value: 0x00000000 Access: RO Size (in bits): 32 Trusted Type: 1				
Address: 08824h ShortName: VCW0_INTERNAL_LAT				
Address: 08924h ShortName: VCW1_INTERNAL_LAT				
DWord	Bit	Description		
0	31:24	Reserved <table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ
Format:	MBZ			
23:0	VCW internal data latency count <table border="1"> <tr> <td>Default Value:</td><td>0h</td></tr> </table>	Default Value:	0h	
Default Value:	0h			

VCW Min Max Latency

VCW_MINMAX_LAT - VCW Min Max Latency				
DWord	Bit	Description		
0	31:16	<p>Current request count</p> <table border="1"> <tr> <td>Default Value:</td> <td>0h</td> </tr> </table>	Default Value:	0h
Default Value:	0h			
15:8	<p>Max latency</p> <table border="1"> <tr> <td>Default Value:</td> <td>0h</td> </tr> </table> <p>Maximum number of clocks taken for tag 200h</p>	Default Value:	0h	
Default Value:	0h			
7:0	<p>Min latency</p> <table border="1"> <tr> <td>Default Value:</td> <td>0h</td> </tr> </table> <p>Minimum number of clocks taken for tag 200h</p>	Default Value:	0h	
Default Value:	0h			

VCW Total Latency

VCW_TOTAL_LAT - VCW Total Latency						
DWord	Bit	Description				
0	31:0	<p>Total latency</p> <table border="1"> <tr> <td>Default Value:</td> <td>0h</td> </tr> <tr> <td>Accumulation of latency per frame for tag 200h</td> <td></td> </tr> </table>	Default Value:	0h	Accumulation of latency per frame for tag 200h	
Default Value:	0h					
Accumulation of latency per frame for tag 200h						

VCW XY position

VCW_XY_POS - VCW XY position				
DWord	Bit	Description		
0	31:16	<p>Current Y value</p> <table border="1"> <tr> <td>Default Value:</td> <td>0h</td> </tr> </table> <p>Current Y position of VCW walker</p>	Default Value:	0h
Default Value:	0h			
15:0	<p>Current X value</p> <table border="1"> <tr> <td>Default Value:</td> <td>0h</td> </tr> </table> <p>Current X position of VCW walker</p>	Default Value:	0h	
Default Value:	0h			

VEBOX TLB Control Register

VTCR - VEBOX TLB Control Register						
DWord	Bit	Description				
0	31:1	Reserved <table border="1"> <tr> <td>Default Value:</td><td>00000000000000000000000000000000b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	00000000000000000000000000000000b	Access:	RO
Default Value:	00000000000000000000000000000000b					
Access:	RO					
	0	Invalidate TLBs on the corresponding Engine <table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>SW writes 1 to invalidate the TLBs for the associated engine and HW clears the bit when invalidation is complete. To ensure proper invalidation of the TLBs, SW has to ensure the corresponding engine's HW pipeline is flushed and cleared from all its memory accesses. Otherwise HW cannot guarantee the proper invalidation for TLBs. This bit is self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					

VEBX Context Element Descriptor (High Part)

VEBX_CTX_EDR_H - VEBX Context Element Descriptor (High Part)		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	044C4h	
DWord	Bit	Description
0	31:0	VEBX Context Element Descriptor (High Part)
		Default Value: 00000000h
		Access: R/W

VEBX Context Element Descriptor (Low Part)

VEBX_CTX_EDR_L - VEBX Context Element Descriptor (Low Part)		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000009	
Size (in bits):	32	
Address:	044C0h	
DWord	Bit	Description
0	31:0	VEBX Context Element Descriptor (Low Part)
		Default Value: 00000009h
		Access: R/W

VEBX Context Element Descriptor (Low Part)

VEBX_CTX_EDR_L - VEBX Context Element Descriptor (Low Part)		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000009	
Size (in bits):	32	
Address:	044C0h	
DWord	Bit	Description
0	31:0	VEBX Context Element Descriptor
		Default Value: 00000009h
		Access: R/W

VEBX Fault Counter

VEBX_FAULT_CNTR - VEBX Fault Counter		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	045C0h	
DWord	Bit	Description
0	31:0	VEBX Fault Counter Default Value: 00000000h Access: RO

VEBX Fixed Counter

VEBX_FIXED_CNTR - VEBX Fixed Counter		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	045C4h	
DWord	Bit	Description
0	31:0	VEBX Fixed Counter
		Default Value: 00000000h
		Access: RO

VEBX LRA 0

VEBX_LRA_0 - VEBX LRA 0						
DWord	Bit	Description				
0	31:30	Reserved <table border="1"> <tr> <td>Default Value:</td><td>00b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	00b	Access:	RO
Default Value:	00b					
Access:	RO					
29:24	VEBX LRA1 Max <table border="1"> <tr> <td>Default Value:</td><td>101111b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Maximum value of programmable LRA1.</p>	Default Value:	101111b	Access:	R/W	
Default Value:	101111b					
Access:	R/W					
23:22	Reserved <table border="1"> <tr> <td>Default Value:</td><td>00b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	00b	Access:	RO	
Default Value:	00b					
Access:	RO					
21:16	VEBX LRA1 Min <table border="1"> <tr> <td>Default Value:</td><td>100000b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Minimum value of programmable LRA1.</p>	Default Value:	100000b	Access:	R/W	
Default Value:	100000b					
Access:	R/W					
15:14	Reserved <table border="1"> <tr> <td>Default Value:</td><td>00b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	00b	Access:	RO	
Default Value:	00b					
Access:	RO					
13:8	VEBX LRA0 Max <table border="1"> <tr> <td>Default Value:</td><td>011111b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Maximum value of programmable LRA0.</p>	Default Value:	011111b	Access:	R/W	
Default Value:	011111b					
Access:	R/W					
7:6	Reserved <table border="1"> <tr> <td>Default Value:</td><td>00b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	00b	Access:	RO	
Default Value:	00b					
Access:	RO					

VEBX_LRA_0 - VEBX LRA 0		
	5:0	VEBXLRA0 Min Default Value: 000000b Access: R/W Minimum value of programmable LRA0.

VEBX LRA 1

VEBX_LRA_1 - VEBX LRA 1						
DWord	Bit	Description				
0	31:30	Reserved <table border="1"> <tr> <td>Default Value:</td><td>00b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	00b	Access:	RO
Default Value:	00b					
Access:	RO					
29:28	VECS <table border="1"> <tr> <td>Default Value:</td><td>00b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Which LRA should VECS use.</p>	Default Value:	00b	Access:	R/W	
Default Value:	00b					
Access:	R/W					
27:26	VFW <table border="1"> <tr> <td>Default Value:</td><td>01b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Which LRA should VFW use.</p>	Default Value:	01b	Access:	R/W	
Default Value:	01b					
Access:	R/W					
25:24	VEO <table border="1"> <tr> <td>Default Value:</td><td>10b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Which LRA should VEO use.</p>	Default Value:	10b	Access:	R/W	
Default Value:	10b					
Access:	R/W					
23:14	Reserved <table border="1"> <tr> <td>Default Value:</td><td>0000000000b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	0000000000b	Access:	RO	
Default Value:	0000000000b					
Access:	RO					
13:8	VEBXLRA2 Max <table border="1"> <tr> <td>Default Value:</td><td>111111b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Minimum value of programmable LRA2.</p>	Default Value:	111111b	Access:	R/W	
Default Value:	111111b					
Access:	R/W					
7:6	Reserved <table border="1"> <tr> <td>Default Value:</td><td>00b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	00b	Access:	RO	
Default Value:	00b					
Access:	RO					

VEBX_LRA_1 - VEBX LRA 1

	5:0	VEBXLRA2 Min
		Default Value:
		Access:
Minimum value of programmable LRA2.		

VEBX_PDP0/PML4/PASID Descriptor (High Part)

VEBX_CTX_PDP0_H - VEBX_PDP0/PML4/PASID Descriptor (High Part)						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	044CCh					
DWord	Bit	Description				
0	31:0	VEBX_PDP0/PML4/PASID Descriptor (High Part)				
		<table border="1"><tr><td>Default Value:</td><td>00000000h</td></tr><tr><td>Access:</td><td>R/W</td></tr></table>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

VEBX_PDP0/PML4/PASID Descriptor (Low Part)

VEBX_CTX_PDP0_L - VEBX PDP0/PML4/PASID Descriptor (Low Part)						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	044C8h					
DWord	Bit	Description				
0	31:0	VEBX PDP0/PML4/PASID Descriptor (Low Part) <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

VEBX PDP1 Descriptor Register (High Part)

VEBX_CTX_PDP1_H - VEBX PDP1 Descriptor Register (High Part)		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	044D4h	
DWord	Bit	Description
0	31:0	VEBX PDP1 Descriptor Register (High Part)
		Default Value: 00000000h
		Access: R/W

VEBX PDP1 Descriptor Register (Low Part)

VEBX_CTX_PDP1_L - VEBX PDP1 Descriptor Register (Low Part)						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	044D0h					
DWord	Bit	Description				
0	31:0	VEBX PDP1 Descriptor Register (Low Part)				
		<table border="1"><tr><td>Default Value:</td><td>00000000h</td></tr><tr><td>Access:</td><td>R/W</td></tr></table>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

VEBX PDP2 Descriptor Register (High Part)

VEBX_CTX_PDP2_H - VEBX PDP2 Descriptor Register (High Part)		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	044DCh	
DWord	Bit	Description
0	31:0	VEBX PDP2 Descriptor Register (High Part)
		Default Value: 00000000h
		Access: R/W

VEBX PDP2 Descriptor Register (Low Part)

VEBX_CTX_PDP2_L - VEBX PDP2 Descriptor Register (Low Part)		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	044D8h	
DWord	Bit	Description
0	31:0	VEBX PDP2 Descriptor Register (Low Part)
		Default Value: 00000000h
		Access: R/W

VEBX PDP3 Descriptor Register (High Part)

VEBX_CTX_PDP3_H - VEBX PDP3 Descriptor Register (High Part)		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	044E4h	
DWord	Bit	Description
0	31:0	VEBX PDP3 Descriptor Register (High Part)
		Default Value: 00000000h
		Access: R/W

VEBX PDP3 Descriptor Register (Low Part)

VEBX_CTX_PDP3_L - VEBX PDP3 Descriptor Register (Low Part)						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Size (in bits):	32					
Address:	044E0h					
DWord	Bit	Description				
0	31:0	VEBX PDP3 Descriptor Register (Low Part)				
		<table border="1"><tr><td>Default Value:</td><td>00000000h</td></tr><tr><td>Access:</td><td>R/W</td></tr></table>	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					

VECS_PREEMPTION_HINT

VECS_PREEMPTION_HINT - VECS_PREEMPTION_HINT				
Register Space:	MMIO: 0/2/0			
Project:	BDW			
Source:	VideoEnhancementCS			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Address:	1A4BCh			
<p>This register contains the Head pointer offset in to the Ring Buffer or the Dword aligned Graphics address in to the Batch Buffer corresponding to either MI_ARB_CHECK called Preemption Hint Address. When Preemption Hint Address is enabled, VECS will honor UHPTR only on parsing MI_ARB_CHK at Preemption Hint Address.</p> <p>This register contains the Head pointer offset into the Ring Buffer or the Dword aligned Graphics address into the Batch Buffer corresponding to the below listed commands in execlist mode of operation</p> <ul style="list-style-type: none"> • MI_ARB_CHECK • MI_WAIT_FOR_EVENT • MI_SEMAPHORE_WAIT 				
<p>Programming Notes</p> <p>Programming Restriction: This register should NEVER be programmed in functional mode, this should be used only in validation mode to achieve deterministic behavior of UHPTR being sampled by a given MI_ARB_CHECK in command stream. Programmer has to ensure that VECS Preemption Hint register gets programmed before UHPTR is programmed and well before VECS crosses the corresponding execution point. Preemption hint for both RingBuffer and Batch Buffer can't be enabled simultaneously.</p>				
DWord	Bit	Description		
0	31:2	Preempted Hint Address		
		<table border="1"> <tr> <td>Format:</td><td>U30</td></tr> <tr> <td>Format:</td><td>GraphicsAddress[31:2]</td></tr> </table> <p>This field contains the Head offset in to the Ring Buffer when Preemption Hint is set to Ring Buffer and Dword aligned Graphics Address in to the batch buffer when Preemption Hint is set to Batch Buffer.</p>	Format:	U30
Format:	U30			
Format:	GraphicsAddress[31:2]			
	1	Batch Buffer Preemption Hint		
		<table border="1"> <tr> <td>Format:</td><td>Enable</td></tr> </table>	Format:	Enable
Format:	Enable			
Value	Name	Description		
0h	Disabled	Preemption hint is disabled in batch buffer.		
1h	Enabled	Preemption hint is enabled in ring buffer and preemption hint address corresponds to the instruction in Batch Buffer.		

VECS_PREEMPTION_HINT - VECS_PREEMPTION_HINT

	0	<p>Ring Preemption Hint</p> <table border="1"> <tr> <td>Format:</td><td>Enable</td></tr> </table> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0h</td><td>Disable</td><td>Preemption hint is disabled in ring buffer.</td></tr> <tr> <td>1h</td><td>Enabled</td><td>Preemption hint is enabled in ring buffer and preemption hint address corresponds to the instruction in Ring Buffer.</td></tr> </tbody> </table>	Format:	Enable	Value	Name	Description	0h	Disable	Preemption hint is disabled in ring buffer.	1h	Enabled	Preemption hint is enabled in ring buffer and preemption hint address corresponds to the instruction in Ring Buffer.
Format:	Enable												
Value	Name	Description											
0h	Disable	Preemption hint is disabled in ring buffer.											
1h	Enabled	Preemption hint is enabled in ring buffer and preemption hint address corresponds to the instruction in Ring Buffer.											

VECS Context ID Preemption Hint

VECS_CTXID_PREEMPTION_HINT - VECS Context ID Preemption Hint						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Source:	VideoEnhancementCS					
Default Value:	0x00000000					
Access:	R/W					
Size (in bits):	32					
Address:	1A4CCh					
<p>This register contains the Context ID of a context in Execlist mode of operation. In execlist mode of operation VECS_PREEMPTION_HINT registers are looked at by Video Enhancement Command Streamer on executing a context having Context ID that matches with the contents of this register. This register contents are valid and looked at only in Execlist mode of operation.</p>						
Programming Notes						
<p>This register should NEVER be programmed in functional mode, this must be used only in validation mode to achieve deterministic preemption behavior in execlist mode of operation.</p>						
DWord	Bit	Description				
0	31:0	Context ID Preemption Hint <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Format:</td><td style="padding: 2px; text-align: right;">U32</td></tr> <tr> <td colspan="2" style="padding: 2px;">If 0 this field has no effect. If nonzero it indicates the only context ID that can be preempted when execlists are enabled. A preemption attempt when the context ID of the currently executing ring context does not match this field will be ignored.</td></tr> </table>	Format:	U32	If 0 this field has no effect. If nonzero it indicates the only context ID that can be preempted when execlists are enabled. A preemption attempt when the context ID of the currently executing ring context does not match this field will be ignored.	
Format:	U32					
If 0 this field has no effect. If nonzero it indicates the only context ID that can be preempted when execlists are enabled. A preemption attempt when the context ID of the currently executing ring context does not match this field will be ignored.						

VECS Context Timestamp Count

VECS_CTX_TIMESTAMP - VECS Context Timestamp Count				
Register Space:	MMIO: 0/2/0			
Project:	BDW			
Source:	VideoEnhancementCS			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Address:	1A3A8h			
<p>This register provides a mechanism to obtain cumulative run time of a GPU context on HW. This register gets context save/restored on a context switch. SW must reset this register on very first submission of a context to HW, then afterwards gets context save/restored maintaining the cumulative run time of the corresponding context. Note that the value of this register can be obtained in a 3D pipeline-synchronous fashion without a pipeline flush by using the PIPE_CONTROL command. See 3D Geometry Pipeline in the "3D and Media" volume. This register (effectively) counts at a constant frequency by adjusting the increment amount according to the actual reference clock frequency. SW therefore does not need to know the reference clock frequency. This register gets reset on an engine reset.</p>				
This register is context save restore on a context switch.				
DWord	Bit	Description		
0	31:0	<p>Timestamp Value</p> <table border="1"> <tr> <td>Format:</td><td>U32</td></tr> </table> <p>This register increments for every 80 ns of time.</p>	Format:	U32
Format:	U32			

VECS Counter for the Video Enhancement Engine

VECS_CNTR - VECS Counter for the Video Enhancement Engine				
Register Space: MMIO: 0/2/0				
Project: BDW				
Source: VideoEnhancementCS				
Default Value: 0xFFFFFFFF				
Access: R/W				
Size (in bits): 32				
Address: 1A178h				
DWord	Bit	Description		
0	31:0	<p>Count Value</p> <table border="1"> <tr> <td>Default Value:</td> <td>ffffffffffh</td> </tr> </table> <p>Writing a Zero value to this register starts the counting. Writing a Value of FFFF FFFF to this counter stops the counter.</p>	Default Value:	ffffffffffh
Default Value:	ffffffffffh			

VECS CSB Fifo Status Register

VECS_CSB_FSR - VECS CSB Fifo Status Register		
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x00000000 Size (in bits): 32		
Address: 0C5D4h Name: VECS CSB Fifo Status Register ShortName: VECS_CSB_FSR		
This RO register holds status of the CSB fifo.		
DWord	Bit	Description
0	31	Not Empty Access: RO
	30:13	Reserved
	12:8	FIFO Maximum Occupancy Count
	7:5	Reserved
	4:0	FIFO Occupancy Count Access: RO

VECS Error Identity Register

VECS_EIR - VECS Error Identity Register			
Register Space: MMIO: 0/2/0 Project: BDW Source: VideoEnhancementCS Default Value: 0x00000000 Access: R/WC Size (in bits): 32			
Address: 1A0B0h			
The EIR register contains the persistent values of Hardware-Detected Error Condition bits. Any bit set in this register will cause the Master Error bit in the ISR to be set. The EIR register is also used by software to clear detected errors (by writing a '1' to the appropriate bit(s) except for the unrecoverable bits described).			
DWord	Bit	Description	
0	31:16	Reserved	
		Project:	All
		Format:	MBZ
	15:0	Error Identity Bits	
		Project:	All
		Format:	Array of Error condition bits See Table 1 5. Hardware-Detected Error Bits
This register contains the persistent values of ESR error status bits that are unmasks via the EMR register. (See Error! Reference source not found.). The logical OR of all (defined) bits in this register is reported in the Master Error bit of the Interrupt Status Register. In order to clear an error condition, software must first clear the error by writing a '1' to the appropriate bit(s) in this field. If required, software should then proceed to clear the Master Error bit of the IIR.			
Value	Name	Description	Project
0h	[Default]		
1h	Error occurred	Error occurred	All
Programming Notes			
Writing a '1' to a set bit will cause that error condition to be cleared. However, the Page Table Error bit (Bit 4) can not be cleared except by reset (i.e., it is a fatal error).			

VECS Error Mask Register

VECS_EMR - VECS Error Mask Register

Register Space: MMIO: 0/2/0

Project: BDW

Source: VideoEnhancementCS

0xFFFFFFFF [BDW]

Access: R/W

Size (in bits): 32

Address: 1A0B4h

The EMR register is used by software to control which Error Status Register bits are "masked" or "unmasked". "Unmasked" bits will be reported in the EIR, thus setting the Master Error ISR bit and possibly triggering a CPU interrupt, and will persist in the EIR until cleared by software. "Masked" bits will not be reported in the EIR and therefore cannot generate Master Error conditions or CPU interrupts.

Undefined or reserved bits in the Hardware Detected Error Bit Table will always return a read value of '1'

DWord	Bit	Description													
0	31:16	<p>Reserved</p> <table border="1"> <tr> <td>Default Value:</td><td>FFFFh</td></tr> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>Must Be One</td></tr> </table>	Default Value:	FFFFh	Project:	BDW	Format:	Must Be One							
Default Value:	FFFFh														
Project:	BDW														
Format:	Must Be One														
	15:0	<p>Error Mask Bits</p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>Array of error condition mask bits See Table 1 5. Hardware-Detected Error Bits</td></tr> </table> <p>This register contains a bit mask that selects which error condition bits (from the ESR) are reported in the EIR.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0000h</td><td>Not Masked</td><td>Will be reported in the EIR</td></tr> <tr> <td>FFFFh</td><td>Masked [Default]</td><td>Will not be reported in the EIR</td></tr> </tbody> </table>	Project:	All	Format:	Array of error condition mask bits See Table 1 5. Hardware-Detected Error Bits	Value	Name	Description	0000h	Not Masked	Will be reported in the EIR	FFFFh	Masked [Default]	Will not be reported in the EIR
Project:	All														
Format:	Array of error condition mask bits See Table 1 5. Hardware-Detected Error Bits														
Value	Name	Description													
0000h	Not Masked	Will be reported in the EIR													
FFFFh	Masked [Default]	Will not be reported in the EIR													

VECS Error Status Register

VECS_ESR - VECS Error Status Register			
Register Space: MMIO: 0/2/0 Project: BDW Source: VideoEnhancementCS Default Value: 0x00000000 Access: RO Size (in bits): 32			
Address: 1A0B8h			
The ESR register contains the current values of all Hardware-Detected Error condition bits (these are all by definition "persistent"). The EMR register selects which of these error conditions are reported in the persistent EIR (i.e., set bits must be cleared by software) and thereby causing a Master Error interrupt condition to be reported in the ISR.			
DWord	Bit	Description	
0	31:16	Reserved	
		Project:	All
	15:0	Error Status Bits	
		Project:	All
		Format:	Array of error condition bits See Table 1 5. Hardware-Detected Error Bits
		This register contains the non-persistent values of all hardware-detected error condition bits.	
Value	Name	Description	Project
0h	[Default]		
1h	Error Condition Detected	Error Condition detected	All

VECS General Purpose Register

VECS_GPR - VECS General Purpose Register			
Register Space:	MMIO: 0/2/0		
Project:	BDW		
Source:	VideoEnhancementCS		
Default Value:	0x00000000, 0x00000000		
Access:	R/W		
Size (in bits):	64		
Address:	1A600h-1A67Fh		
This is a general purpose register bank of sixteen 64-bit registers, used as temporary storage by the MI_MATH command to do ALU operations.			
Programming Notes			
Any operation that initiates a read to register 0x1A66C will return the value of 0x1A60c register. This does not include context save or MI_MATH command operation.	BDW		
DWord	Bit	Description	
0	63:0	Reserved	Format: MBZ

VECS Hardware Status Mask Register

VECS_HWSTAM - VECS Hardware Status Mask Register								
Register Space:	MMIO: 0/2/0							
Project:	BDW							
Source:	VideoEnhancementCS							
Default Value:	0xFFFFFFFF							
Access:	R/W							
Size (in bits):	32							
Trusted Type:	1							
Address:	1A098h							
Access: RO for Reserved Control bits								
<p>The HWSTAM register has the same format as the Interrupt Control Registers. The bits in this register are "mask" bits that prevent the corresponding bits in the Interrupt Status Register from generating a "Hardware Status Write" (PCI write cycle). Any unmasked interrupt bit (HWSTAM bit set to 0) will allow the Interrupt Status Register to be written to the ISR location (within the memory page specified by the Hardware Status Page Address Register) when that Interrupt Status Register bit changes state.</p>								
Programming Notes								
<ul style="list-style-type: none"> • To write the interrupt to the HWSP, the corresponding IMR bit must also be clear (enabled). • At most 1 bit can be unmasked at any given time. 								
DWord	Bit	Description						
0	31:0	Hardware Status Mask Register <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Default Value:</td><td style="padding: 2px;">FFFFFFFFh</td></tr> <tr> <td style="padding: 2px;">Project:</td><td style="padding: 2px;">All</td></tr> <tr> <td style="padding: 2px;">Format:</td><td style="padding: 2px;">Array of Masks</td></tr> </table> <p style="margin-top: 2px;">refer to Table 4-4 in Interrupt Control Register section for bit definitions</p>	Default Value:	FFFFFFFFh	Project:	All	Format:	Array of Masks
Default Value:	FFFFFFFFh							
Project:	All							
Format:	Array of Masks							

VECS Instruction Parser Mode Register

VECS_INSTPM - VECS Instruction Parser Mode Register					
Register Space:	MMIO: 0/2/0				
Project:	BDW				
Source:	VideoEnhancementCS				
Default Value:	0x00000000				
Access:	R/W				
Size (in bits):	32				
Address:	1A0C0h-1A0C3h				
<p>The VECS_INSTPM register is used to control the operation of the VECS Instruction Parser. Certain classes of instructions can be disabled (ignored) - often useful for detecting performance bottlenecks. Also, "Synchronizing Flush" operations can be initiated - useful for ensuring the completion (vs. only parsing) of rendering instructions.</p>					
Programming Notes					
All reserved bits are implemented					
DWord	Bit	Description			
0	31:16	<p>Masks</p> <table border="1"> <tr> <td>Format:</td><td>Mask[15:0]</td></tr> </table> <p>These bits serve as write enables for bits 15:0. If this register is written with any of these bits clear the corresponding bit in the field 15:0 will not be modified. Reading these bits always returns 0s.</p>	Format:	Mask[15:0]	
Format:	Mask[15:0]				
15:11	<p>Reserved</p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	All	Format:	MBZ
Project:	All				
Format:	MBZ				
10	<p>Reserved</p> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	BDW	Format:	MBZ
Project:	BDW				
Format:	MBZ				
9	<table border="1"> <tr> <td colspan="2" style="text-align: center;">Programming Notes</td></tr> <tr> <td colspan="2">This bit is not context save and restored. SW must set this bit through the Work Around Batch buffer in to retain through standby and set this bit on each context submission.</td></tr> </table>	Programming Notes		This bit is not context save and restored. SW must set this bit through the Work Around Batch buffer in to retain through standby and set this bit on each context submission.	
Programming Notes					
This bit is not context save and restored. SW must set this bit through the Work Around Batch buffer in to retain through standby and set this bit on each context submission.					
8:7	<table border="1"> <tr> <td colspan="2" style="text-align: center;">Reserved</td></tr> <tr> <td colspan="2">Format:</td></tr> </table>	Reserved		Format:	
Reserved					
Format:					

VECS_INSTPM - VECS Instruction Parser Mode Register

	6:5	Reserved
	Project:	BDW
	Format:	MBZ
	4:0	Reserved

VECS Interrupt Mask Register

VECS_IMR - VECS Interrupt Mask Register																							
DWord	Bit	Description																					
0	31:0	Interrupt Mask Bits																					
<table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>Array of interrupt mask bits Refer to Table 4-4 in Interrupt Control Register section for bit definitions</td></tr> </table> <p>This field contains a bit mask which selects which interrupt bits (from the ISR) are reported in the IIR.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th><th>Project</th></tr> </thead> <tbody> <tr> <td>FFFF FFFFh</td><td>[Default]</td><td></td><td></td></tr> <tr> <td>0h</td><td>Not Masked</td><td>Will be reported in the IIR</td><td>All</td></tr> <tr> <td>1h</td><td>Masked</td><td>Will not be reported in the IIR</td><td>All</td></tr> </tbody> </table>				Project:	All	Format:	Array of interrupt mask bits Refer to Table 4-4 in Interrupt Control Register section for bit definitions	Value	Name	Description	Project	FFFF FFFFh	[Default]			0h	Not Masked	Will be reported in the IIR	All	1h	Masked	Will not be reported in the IIR	All
Project:	All																						
Format:	Array of interrupt mask bits Refer to Table 4-4 in Interrupt Control Register section for bit definitions																						
Value	Name	Description	Project																				
FFFF FFFFh	[Default]																						
0h	Not Masked	Will be reported in the IIR	All																				
1h	Masked	Will not be reported in the IIR	All																				

VECS Mode Register for Software Interface

VECS_MI_MODE - VECS Mode Register for Software Interface					
Register Space:	MMIO: 0/2/0				
Project:	BDW				
Source:	VideoEnhancementCS 0x00000200 [BDW]				
Access:	R/W				
Size (in bits):	32				
Address:	1A09Ch-1A09Fh				
The MI_MODE register contains information that controls software interface aspects of the command parser					
DWord	Bit	Description			
0	31:16	Masks A "1" in a bit in this field allows the modification of the corresponding bit in Bits 15:0			
	15	Suspend Flush			
		Project:	All		
		Mask:	MMIO(0x209c)#31		
		Value	Name	Description	Project
		0h	No Delay	HW will not delay flush, this bit will get cleared by MI_SUSPEND_FLUSH as well	All
		1h	Delay Flush	Suspend flush is active	All
	14:12	Reserved		Format:	MBZ
	11	Invalidate UHPT Enable If bit set H/W clears the valid bit of BCS_UHPT (4134h, bit 0) when current active head pointer is equal to UHPT.			
	10	Atomic Read Return for MI_COPY_MEM_MEM		Project:	BDW
		Format:		U1	
Value	Name	Description			
0h	Disable [Default]	Hardware does a regular memory fence write to complete the write to the destination address before moving to the next instruction.			
1h	Enable	Hardware does Atomic Move with Read Return to complete the write to the destination address before moving to the next instruction.			

VECS_MI_MODE - VECS Mode Register for Software Interface

	9	Ring Idle (Read Only Status bit) Writes to this bit are not allowed.	
		Value	Name
		0	Parser not idle
		1	Parser idle [Default]
	8	Stop Ring 0 = Normal Operation. 1 = Parser is turned off. Software must set this bit to force the Ring and Command Parser to Idle. Software must read a "1" in Ring Idle bit after setting this bit to ensure that the hardware is idle. <i>Software must clear this bit for Ring to resume normal operation.</i>	
	7:0	Reserved Format:	
			MBZ

VECS PREEMPTION HINT UDW

VECS_PREEMPTION_HINT_UDW - VECS PREEMPTION HINT UDW				
Register Space:	MMIO: 0/2/0			
Project:	BDW			
Source:	VideoEnhancementCS			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Address:	1A4C8h			
<p>This register contains the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space of the Batch Buffer corresponding to MI_ARB_CHECK command called Preemption Hint Address.</p>				
Programming Notes				
Programming Restriction: This register should NEVER be programmed in functional mode, this should be used only in validation mode to achieve deterministic behavior of UHPTR being sampled by a given MI_ARB_CHK in command stream.				
DWord	Bit	Description		
0	31:16	Reserved <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Format:</td><td style="width: 50%;">MBZ</td></tr> </table>	Format:	MBZ
	Format:	MBZ		
15:0	Preempted Hint Address Upper DWORD <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Format:</td><td style="width: 50%;">GraphicsAddress[47:32]</td></tr> </table> <p>This field contains the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space of the batch buffer when Preemption Hint is set to Batch Buffer. This field is not valid when Preemption Hint is set to Ring Buffer.</p>	Format:	GraphicsAddress[47:32]	
Format:	GraphicsAddress[47:32]			

VECS Reported Timestamp Count

VECS_TIMESTAMP - VECS Reported Timestamp Count						
DWord	Bit	Description				
0	63:36	<p>Reserved</p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	All	Format:	MBZ
Project:	All					
Format:	MBZ					
35:0	<p>TimeStampValue</p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>U36</td></tr> </table> <p>This register toggles every 80 ns. The upper 28 bits are zero.</p>	Project:	All	Format:	U36	
Project:	All					
Format:	U36					

VECS Reset Control Register

VECS_RESET_CTRL - VECS Reset Control Register				
DWord	Bit	Description		
0	31:16	<p>Mask Bits</p> <table border="1"> <tr> <td>Format:</td> <td>Mask[15:0]</td> </tr> </table> <p>Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)</p>	Format:	Mask[15:0]
Format:	Mask[15:0]			
15:2	<p>Reserved</p> <table border="1"> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ	
Format:	MBZ			
1	<p>Ready for Reset</p> <table border="1"> <tr> <td>Format:</td> <td>U1</td> </tr> </table> <p>When set indicates video enhancement engine is ready for reset. This bit gets cleared on engine reset or when Soft Reset In progress is cleared.</p>	Format:	U1	
Format:	U1			
0	<p>Request Reset</p> <table border="1"> <tr> <td>Format:</td> <td>U1</td> </tr> </table> <p>When set indicates SW wishes to reset the video enhancement engine. On seeing this bit set Command Streamer will take appropriate action and set Ready For Reset status bit. This bit gets cleared on engine reset.</p>	Format:	U1	
Format:	U1			

VECS Semaphore Polling Interval on Wait

VECS_SEMA_WAIT_POLL - VECS Semaphore Polling Interval on Wait				
Register Space:	MMIO: 0/2/0			
Project:	BDW			
Source:	VideoEnhancementCS			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Address:	1A24Ch			
<p>The SEMA_WAIT_POLL register contains Poll Interval field which specifies the minimum number of microseconds allowed for command streamer to wait before re-fetching the data from the address mentioned in the MI_SEMAPHORE_WAIT command on WAIT Mode set to POLL until the condition is satisfied while the context is not switched out. When value of 0 is written the poll interval will be equal to the memory latency of the read completion.</p>				
DWord	Bit	Description		
0	31:21	Reserved <table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ
Format:	MBZ			
20:0	Poll Interval Minimum number of micro-seconds allowed			

VECS Threshold for the Counter of Video Enhancement Engine

VECS_CTR_THRSH - VECS Threshold for the Counter of Video Enhancement Engine				
Register Space:	MMIO: 0/2/0			
Project:	BDW			
Source:	VideoEnhancementCS			
Default Value:	0x00150000			
Access:	R/W			
Size (in bits):	32			
Address:	1A17Ch			
DWord	Bit	Description		
0	31:0	<p>Threshold Value</p> <table border="1"> <tr> <td>Default Value:</td> <td>00150000h</td> </tr> </table> <p>The value in this register reflects the number of clocks the bit stream decode engine is expected to run. If the value is exceeded the counter is reset and an interrupt may be enabled in the device.</p>	Default Value:	00150000h
Default Value:	00150000h			

Vendor Defined ID and Device ID

VID_DID - Vendor Defined ID and Device ID												
DWord	Bit	Description										
0	31:16	<p>Device ID</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td colspan="2">Audio device ID</td> </tr> <tr> <th>Value</th><th>Name</th><th>Project</th></tr> <tr> <td>160Ch</td><td>[Default]</td><td>BDW</td></tr> </table>	Access:	RO	Audio device ID		Value	Name	Project	160Ch	[Default]	BDW
Access:	RO											
Audio device ID												
Value	Name	Project										
160Ch	[Default]	BDW										
<p>Vendor ID</p> <table border="1"> <tr> <td>Default Value:</td> <td>8086h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td colspan="2">Intel is the Vendor</td></tr> </table>	Default Value:	8086h	Access:	RO	Intel is the Vendor							
Default Value:	8086h											
Access:	RO											
Intel is the Vendor												

Vendor Identification

VID2_0_2_0_PCI - Vendor Identification						
Register Space: PCI: 0/2/0						
Project: BDW						
Default Value: 0x00008086						
Size (in bits): 16						
Address: 00000h						
This register combined with the Device Identification register uniquely identifies any PCI device.						
DWord	Bit	Description				
0	15:0	<p>Vendor Identification Number</p> <table border="1"> <tr> <td>Default Value:</td><td>1000000010000110b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>PCI standard identification for Intel.</p>	Default Value:	1000000010000110b	Access:	RO
Default Value:	1000000010000110b					
Access:	RO					

VEO Current Pipe 0 XY Register

VEO_CURRENT0_XY - VEO Current Pipe 0 XY Register		
Register Space: MMIO: 0/2/0 Project: BDW Source: VideoEnhancementCS Default Value: 0x00000000 Access: RO Size (in bits): 32 Trusted Type: 1		
Address: 08854h ShortName: VEO0_CURRENT0_XY		
Address: 08954h ShortName: VEO1_CURRENT0_XY		
DWord	Bit	Description
0	31:30	Reserved
	29:16	Current Input Pipe 0 X
		Default Value: <input type="text" value="0h"/>
	15	Reserved
	14:0	Current Input Pipe 0 Y
		Default Value: <input type="text" value="0h"/>

VEO DN Pipe 0 XY Register

VEO_DN0_XY - VEO DN Pipe 0 XY Register					
Register Space: MMIO: 0/2/0 Project: BDW Source: VideoEnhancementCS Default Value: 0x00000000 Access: RO Size (in bits): 32 Trusted Type: 1					
Address: 0884Ch ShortName: VEO0_DN0_XY					
Address: 0894Ch ShortName: VEO1_DN0_XY					
DWord	Bit	Description			
0	31:30	Reserved			
	29:16	DN Pipe 0 X <table border="1"> <tr> <td>Default Value:</td><td>0h</td></tr> <tr> <td>dn_input_x[13:0]</td><td></td></tr> </table>	Default Value:	0h	dn_input_x[13:0]
Default Value:	0h				
dn_input_x[13:0]					
15	Reserved				
14:0	DN Pipe 0 Y <table border="1"> <tr> <td>Default Value:</td><td>0h</td></tr> <tr> <td>dn_input_y[14:0]</td><td></td></tr> </table>	Default Value:	0h	dn_input_y[14:0]	
Default Value:	0h				
dn_input_y[14:0]					

VEO DN Pipe 1 XY Register

VEO_DN1_XY - VEO DN Pipe 1 XY Register		
Register Space: MMIO: 0/2/0 Project: BDW Source: VideoEnhancementCS Default Value: 0x00000000 Access: RO Size (in bits): 32 Trusted Type: 1		
Address: 08850h ShortName: VEO0_DN1_XY		
Address: 08950h ShortName: VEO1_DN1_XY		
DWord	Bit	Description
0	31:30	Reserved
	29:16	DN Pipe 1 X
		Default Value: 0h
	15	Reserved
	14:0	DN Pipe 1 Y
		Default Value: 0h

VEO DV Count Register

VEO_DV_COUNT - VEO DV Count Register		
DWord	Bit	Description
0	31:24	Pipe1 Motion History DV/Hold Maxcount
		Default Value: 0h
	23:16	Pipe1 Pixel History DV/Hold Maxcount
		Default Value: 0h
1	15:8	Pipe0 Motion History DV/Hold Maxcount
		Default Value: 0h
2	7:0	Pipe0 Pixel History DV/Hold Maxcount
		Default Value: 0h

VEO DV Hold Register

VEO_DVHOLD - VEO DV Hold Register		
Register Space: MMIO: 0/2/0 Project: BDW Source: VideoEnhancementCS Default Value: 0x00000000 Access: RO Size (in bits): 32 Trusted Type: 1		
Address: 0885Ch ShortName: VEO0_DVHOLD		
Address: 0895Ch ShortName: VEO1_DVHOLD		
Datavalid/Hold signals for VEO interface		
DWord	Bit	Description
0	31	vdn_p0_veo_pixel_dv Default Value: 0h
	30	veo_vdn_p0_pixel_hold Default Value: 0h
	29	vdn_p0_veo_mh_dv Default Value: 0h
	28	veo_vdn_p0_mh_hold Default Value: 0h
	27	vdn_p0_veo_bne_luma_dv Default Value: 0h
	26	veo_vdn_p0_bne_luma_hold Default Value: 0h
	25	vdn_p0_veo_bne_chroma_dv Default Value: 0h
	24	veo_vdn_p0_bne_chroma_hold Default Value: 0h
	23	vdi_p0_veo_pixel_dv Default Value: 0h
	22	veo_vdi_p0_pixel_hold Default Value: 0h

VEO_DVHOLD - VEO DV Hold Register

	21	vdi_p0_veo_stmm_dv	Default Value:	0h
	20	veo_vdi_p0_stmm_hold	Default Value:	0h
	19	vdi_p0_veo_fmd_dv	Default Value:	0h
	18	veo_vdi_p0_fmd_hold	Default Value:	0h
	17	iecp_p0_veo_dv	Default Value:	0h
	16	veo_iecp_p0_hold	Default Value:	0h
	15	vdn_p1_veo_pixel_dv	Default Value:	0h
	14	veo_vdn_p1_pixel_hold	Default Value:	0h
	13	vdn_p1_veo_mh_dv	Default Value:	0h
	12	veo_vdn_p1_mh_hold	Default Value:	0h
	11	vdn_p1_veo_bne_luma_dv	Default Value:	0h
	10	veo_vdn_p1_bne_luma_hold	Default Value:	0h
	9	vdn_p1_veo_bne_chroma_dv	Default Value:	0h
	8	veo_vdn_p1_bne_chroma_hold	Default Value:	0h
	7	vdi_p1_veo_pixel_dv	Default Value:	0h
	6	veo_vdi_p1_pixel_hold	Default Value:	0h
	5	vdi_p1_veo_stmm_dv	Default Value:	0h
	4	veo_vdi_p1_stmm_hold	Default Value:	0h

VEO_DVHOLD - VEO DV Hold Register

	3	vdi_p1_veo_fmd_dv
		Default Value: 0h
	2	veo_vdi_p1_fmd_hold
		Default Value: 0h
	1	iecp_p1_veo_dv
		Default Value: 0h
	0	veo_iecp_p1_hold
		Default Value: 0h

VEO Previous Pipe 0 XY Register

VEO_PREVIOUS0_XY - VEO Previous Pipe 0 XY Register		
Register Space: MMIO: 0/2/0 Project: BDW Source: VideoEnhancementCS Default Value: 0x00000000 Access: RO Size (in bits): 32 Trusted Type: 1		
Address: 08858h ShortName: VEO0_PREVIOUS0_XY		
Address: 08958h ShortName: VEO1_PREVIOUS0_XY		
DWord	Bit	Description
0	31:30	Reserved
	29:16	Previous Input Pipe 0 X
	15	Reserved
	14:0	Previous Input Pipe 0 Y

VEO State Register

VEO_STATE - VEO State Register		
Register Space: MMIO: 0/2/0 Project: BDW Source: VideoEnhancementCS 0x00024000 [BDW] Access: RO Size (in bits): 32 Trusted Type: 1		
Address: 08840h ShortName: VEO0_STATE		
Address: 08940h ShortName: VEO1_STATE		
Data valids and holds for the statistics interface		
DWord	Bit	Description
0	31	iecp_p0_veo_his_dv Default Value: 0h
	30	iecp_p0_veo_skin_dv Default Value: 0h
	29	iecp_p0_veo_rgb_his_dv Default Value: 0h
	28	iecp_p0_veo_out_dist_dv Default Value: 0h
	27	iecp_p1_veo_his_dv Default Value: 0h
	26	iecp_p1_veo_skin_dv Default Value: 0h
	25	iecp_p1_veo_out_dist_dv Default Value: 0h
	24	veo_iecp_p0_rgb_his_hold Default Value: 0h
	23	Reserved
	22:19	VSC_FSM_State Default Value: 0h State of the VEO_VSC_CNTRL state machine

VEO_STATE - VEO State Register									
	18:16	GAV Command Credit Count							
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Project</th></tr> </thead> <tbody> <tr> <td>2h</td><td>[Default]</td><td>BDW</td></tr> </tbody> </table>	Value	Name	Project	2h	[Default]	BDW	
Value	Name	Project							
2h	[Default]	BDW							
	15:12	GAV Data Credit Count							
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Project</th></tr> </thead> <tbody> <tr> <td>4h</td><td>[Default]</td><td>BDW</td></tr> </tbody> </table>	Value	Name	Project	4h	[Default]	BDW	
Value	Name	Project							
4h	[Default]	BDW							
	11:8	Reserved							
		<table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ					
Format:	MBZ								
	7:0	GAV Stall Clk Cnt Max							
		<table border="1"> <tr> <td>Default Value:</td><td>0h</td></tr> </table> <p>The longest stall from GAV since the beginning of the frame.</p>	Default Value:	0h					
Default Value:	0h								

VF Scratch Pad

VFSKPD - VF Scratch Pad						
Register Space: MMIO: 0/2/0 Project: BDW Source: RenderCS Default Value: 0x00000000 Access: R/W Size (in bits): 32						
Address: 02470h Address: 083A8h-083ABh Valid Projects: [BDW]						
DWord	Bit	Description				
0	31:16	<p>Mask Bits</p> <table border="1"> <tr> <td>Format:</td><td>Mask[15:0]</td></tr> </table> <p>Must be set to modify corresponding bit in Bits 15:0. (All bits implemented)</p>	Format:	Mask[15:0]		
Format:	Mask[15:0]					
	15	<p>Reserved</p> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>PBC</td></tr> </table>	Project:	BDW	Format:	PBC
Project:	BDW					
Format:	PBC					
	14:12	<p>Reserved</p> <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>PBC</td></tr> </table>	Project:	All	Format:	PBC
Project:	All					
Format:	PBC					
	11	<p>Reserved</p> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>PBC</td></tr> </table>	Project:	BDW	Format:	PBC
Project:	BDW					
Format:	PBC					
	10	<p>Reserved</p> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>PBC</td></tr> </table>	Project:	BDW	Format:	PBC
Project:	BDW					
Format:	PBC					
	9	<p>Reserved</p> <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>PBC</td></tr> </table>	Project:	BDW	Format:	PBC
Project:	BDW					
Format:	PBC					

VFSKPD - VF Scratch Pad

	8	End Offset Guardband Disable									
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>U1</td></tr> </table>	Project:	BDW	Format:	U1					
Project:	BDW										
Format:	U1										
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0h</td><td>Enable [Default]</td><td>When 3DPRIMITIVE.End Offset Enable is set to 1, VF will use the guardband to determine when a draw call can be pre-empted. VF will not allow pre-emption in the guardband region.</td></tr> <tr> <td>1h</td><td>Disable</td><td>When set to Disable, there will not be any preemption or GB consideration for autodraw (3DPRIMITIVE.End Offset Enable set to 1).</td></tr> </tbody> </table>	Value	Name	Description	0h	Enable [Default]	When 3DPRIMITIVE.End Offset Enable is set to 1, VF will use the guardband to determine when a draw call can be pre-empted. VF will not allow pre-emption in the guardband region.	1h	Disable	When set to Disable, there will not be any preemption or GB consideration for autodraw (3DPRIMITIVE.End Offset Enable set to 1).
Value	Name	Description									
0h	Enable [Default]	When 3DPRIMITIVE.End Offset Enable is set to 1, VF will use the guardband to determine when a draw call can be pre-empted. VF will not allow pre-emption in the guardband region.									
1h	Disable	When set to Disable, there will not be any preemption or GB consideration for autodraw (3DPRIMITIVE.End Offset Enable set to 1).									
	7	Guardband Disable									
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>U1</td></tr> </table>	Project:	BDW	Format:	U1					
Project:	BDW										
Format:	U1										
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Value	Name	Description									
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1h	Disable	VF will not use the guardband to determine when a draw call can be pre-empted. VF will allow pre-emption on any vertex in the draw call.									
	6	Reserved									
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>PBC</td></tr> </table>	Project:	BDW	Format:	PBC					
Project:	BDW										
Format:	PBC										
	5	TLB Prefetch Enable									
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>U1</td></tr> </table>	Project:	BDW	Format:	U1					
Project:	BDW										
Format:	U1										
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0h</td><td>Disable [Default]</td><td>The VF will generate prefetch of TLB when it is fetching sequential vertex data and four or fewer vertex buffers are valid.</td></tr> <tr> <td>1h</td><td>Enable</td><td>VF will disable prefetch of TLB entries.</td></tr> </tbody> </table>	Value	Name	Description	0h	Disable [Default]	The VF will generate prefetch of TLB when it is fetching sequential vertex data and four or fewer vertex buffers are valid.	1h	Enable	VF will disable prefetch of TLB entries.
Value	Name	Description									
0h	Disable [Default]	The VF will generate prefetch of TLB when it is fetching sequential vertex data and four or fewer vertex buffers are valid.									
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	4	Reserved									
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>PBC</td></tr> </table>	Project:	BDW	Format:	PBC					
Project:	BDW										
Format:	PBC										
	3	Reserved									
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>PBC</td></tr> </table>	Project:	BDW	Format:	PBC					
Project:	BDW										
Format:	PBC										

VFSKPD - VF Scratch Pad											
	2	Vertex Cache Implicit Disable Inhibit									
		<table border="1"> <tr> <td>Format:</td><td>U1</td></tr> </table>	Format:	U1							
Format:	U1										
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0h</td><td>[Default]</td><td>Allow VF to disable VS0 when Sequential index or Prim ID is a valid Element.</td></tr> <tr> <td>1h</td><td></td><td>VF never implicitly disables the vertex cache. Software must disable the VS0 Cache when required.</td></tr> </tbody> </table>	Value	Name	Description	0h	[Default]	Allow VF to disable VS0 when Sequential index or Prim ID is a valid Element.	1h		VF never implicitly disables the vertex cache. Software must disable the VS0 Cache when required.
Value	Name	Description									
0h	[Default]	Allow VF to disable VS0 when Sequential index or Prim ID is a valid Element.									
1h		VF never implicitly disables the vertex cache. Software must disable the VS0 Cache when required.									
	1	Disable Over Fetch Cache									
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> </table>	Project:	BDW							
Project:	BDW										
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0h</td><td>[Default]</td><td>Cache will check for data in cache before making a request to memory</td></tr> <tr> <td>1h</td><td></td><td>Always re-fetch new data from memory.</td></tr> </tbody> </table>	Value	Name	Description	0h	[Default]	Cache will check for data in cache before making a request to memory	1h		Always re-fetch new data from memory.
Value	Name	Description									
0h	[Default]	Cache will check for data in cache before making a request to memory									
1h		Always re-fetch new data from memory.									
		<p style="text-align: center;">Programming Notes</p> <p>Note that the Disable Multiple Miss Read squash bit must be cleared for Disable Over Fetch Cache to be set.</p>									
	0	Disable Multiple Miss Read squash									
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>Disable</td></tr> </table>	Project:	BDW	Format:	Disable					
Project:	BDW										
Format:	Disable										
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0h</td><td>[Default]</td><td>Allow VF to squash reads that are to the same cacheline for vertex buffer requests.</td></tr> <tr> <td>1h</td><td></td><td>Disallow VF from squashing reads that are to the same cacheline for vertex buffer requests.</td></tr> </tbody> </table>	Value	Name	Description	0h	[Default]	Allow VF to squash reads that are to the same cacheline for vertex buffer requests.	1h		Disallow VF from squashing reads that are to the same cacheline for vertex buffer requests.
Value	Name	Description									
0h	[Default]	Allow VF to squash reads that are to the same cacheline for vertex buffer requests.									
1h		Disallow VF from squashing reads that are to the same cacheline for vertex buffer requests.									

VFW Credit Count Register

VFW_CREDIT_CNT - VFW Credit Count Register								
Register Space: MMIO: 0/2/0 Project: BDW Source: VideoEnhancementCS 0x00000002 [BDW] Access: RO Size (in bits): 32 Trusted Type: 1								
Address: 08810h ShortName: VFW0_CREDIT_CNT								
Address: 08910h ShortName: VFW1_CREDIT_CNT								
DWord	Bit	Description						
0	31:8	Reserved						
	7:0	Credit Count The number of outstanding credits between VFW and GAV. If zero VEBOX cannot proceed due to GAV not releasing credits. <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Project</th></tr> </thead> <tbody> <tr> <td>2h</td><td>[Default]</td><td>BDW</td></tr> </tbody> </table>		Value	Name	Project	2h	[Default]
Value	Name	Project						
2h	[Default]	BDW						

VGA_CONTROL

VGA_CONTROL								
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x80000000 Access: R/W Size (in bits): 32								
Address: 41000h-41003h Name: VGA Control ShortName: VGA_CONTROL Valid Projects: BDW Power: Always on Reset: global								
Restriction								
VGA requires panel fitting to be enabled. VGA is always connected to pipe A. VGA display should only be enabled if all display planes other than VGA are disabled.								
DWord	Bit	Description						
0	31	<p>VGA Display Disable</p> <p>This bit will disable the VGA compatible display mode. It has no effect on VGA register or A0000-BFFF memory aperture accesses which are controlled by the PCI configuration and VGA I/O register settings.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th><th style="text-align: center;">Name</th></tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td><td>Enable</td></tr> <tr> <td style="text-align: center;">1b</td><td>Disable [Default]</td></tr> </tbody> </table>	Value	Name	0b	Enable	1b	Disable [Default]
Value	Name							
0b	Enable							
1b	Disable [Default]							
Restriction								
The VGA SR01 screen off bit must be programmed when enabling and disabling VGA. See the VGA Registers document.								
<p>Reserved</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Format:</td><td style="width: 50%;">PBC</td></tr> </table>	Format:	PBC						
Format:	PBC							
	26	<p>VGA Border Enable</p> <p>This bit determines if the VGA border areas are included in the active display area. The border will be scaled along with the pixel data.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th><th style="text-align: center;">Name</th></tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td><td>Disable</td></tr> <tr> <td style="text-align: center;">1b</td><td>Enable</td></tr> </tbody> </table>	Value	Name	0b	Disable	1b	Enable
Value	Name							
0b	Disable							
1b	Enable							
<p>Reserved</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Format:</td><td style="width: 50%;">PBC</td></tr> </table>	Format:	PBC						
Format:	PBC							

VGA_CONTROL																	
24	Pipe CSC Enable	<table border="1"> <thead> <tr> <th colspan="2">Description</th> </tr> </thead> <tbody> <tr> <td colspan="2">This bit enables pipe color space conversion for the VGA pixel data.</td> </tr> </tbody> </table> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Disable</td></tr> <tr> <td>1b</td><td>Enable</td></tr> </tbody> </table>	Description		This bit enables pipe color space conversion for the VGA pixel data.		Value	Name	0b	Disable	1b	Enable					
Description																	
This bit enables pipe color space conversion for the VGA pixel data.																	
Value	Name																
0b	Disable																
1b	Enable																
23:21	Reserved	<table border="1"> <tr> <td>Format:</td><td>PBC</td></tr> </table>	Format:	PBC													
Format:	PBC																
20	Legacy 8Bit Palette En	<p>This bit affects reads and writes to the palette through VGA I/O addresses. In the 6-bit mode, the 8-bits of data are shifted up two bits on the write (upper two bits are lost) and shifted two bits down on the read. This provides backward compatibility for original VGA programs as well as VESA VBE support for 8-bit palette. It does not affect palette accesses through the palette register MMIO path.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0b</td><td>6 bit DAC</td></tr> <tr> <td>1b</td><td>8 bit DAC</td></tr> </tbody> </table>	Value	Name	0b	6 bit DAC	1b	8 bit DAC									
Value	Name																
0b	6 bit DAC																
1b	8 bit DAC																
19	Reserved																
18	Reserved																
17:16	Reserved	<table border="1"> <tr> <td>Format:</td><td>PBC</td></tr> </table>	Format:	PBC													
Format:	PBC																
15:12	Reserved																
11:8	Reserved																
7:6	Blink Duty Cycle	<p>Controls the VGA text mode blink duty cycle relative to the VGA cursor blink duty cycle.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>00b</td><td>100%</td><td>100% Duty Cycle, Full Cursor Rate</td></tr> <tr> <td>01b</td><td>25%</td><td>25% Duty Cycle, 1/2 Cursor Rate</td></tr> <tr> <td>10b</td><td>50%</td><td>50% Duty Cycle, 1/2 Cursor Rate</td></tr> <tr> <td>11b</td><td>75%</td><td>75% Duty Cycle, 1/2 Cursor Rate</td></tr> </tbody> </table>	Value	Name	Description	00b	100%	100% Duty Cycle, Full Cursor Rate	01b	25%	25% Duty Cycle, 1/2 Cursor Rate	10b	50%	50% Duty Cycle, 1/2 Cursor Rate	11b	75%	75% Duty Cycle, 1/2 Cursor Rate
Value	Name	Description															
00b	100%	100% Duty Cycle, Full Cursor Rate															
01b	25%	25% Duty Cycle, 1/2 Cursor Rate															
10b	50%	50% Duty Cycle, 1/2 Cursor Rate															
11b	75%	75% Duty Cycle, 1/2 Cursor Rate															
5:0	VSYNC Blink Rate	<p>Controls the VGA blink rate in terms of the number of VSYNCs per on/off cycle.</p> <table border="1"> <tr> <th>Programming Notes</th></tr> <tr> <td>Program with (VSYNCs/cycle)/2-1</td></tr> </table>	Programming Notes	Program with (VSYNCs/cycle)/2-1													
Programming Notes																	
Program with (VSYNCs/cycle)/2-1																	

VIC Virtual page Address Registers

VICTLB_VA - VIC Virtual page Address Registers				
Register Space:	MMIO: 0/2/0			
Project:	BDW			
Source:	RenderCS			
Default Value:	0x00000000			
Access:	RO			
Size (in bits):	32			
Trusted Type:	1			
Address:	04900h-04903h			
These registers are directly mapped to the current Virtual Addresses in the VICTLB (Vertex Fetch, Instruction Cache, and Command Streamer TLB.)				
DWord	Bit	Description		
0	31:12	<p>Address</p> <table border="1"> <tr> <td>Format:</td><td>GraphicsAddress[31:12]</td></tr> </table> <p>Page virtual address.</p>	Format:	GraphicsAddress[31:12]
Format:	GraphicsAddress[31:12]			
11:0	<p>Reserved</p> <table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ	
Format:	MBZ			

VIDEO_DIP_CTL

VIDEO_DIP_CTL		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	60200h-60203h	
Name:	Transcoder A Video Data Island Packet Control	
ShortName:	VIDEO_DIP_CTL_A	
Valid Projects:	BDW	
Power:	off/on	
Reset:	soft	
Address:	61200h-61203h	
Name:	Transcoder B Video Data Island Packet Control	
ShortName:	VIDEO_DIP_CTL_B	
Valid Projects:	BDW	
Power:	off/on	
Reset:	soft	
Address:	62200h-62203h	
Name:	Transcoder C Video Data Island Packet Control	
ShortName:	VIDEO_DIP_CTL_C	
Valid Projects:	BDW	
Power:	off/on	
Reset:	soft	
Address:	6F200h-6F203h	
Name:	Transcoder EDP Video Data Island Packet Control	
ShortName:	VIDEO_DIP_CTL_EDP	
Valid Projects:	BDW	
Power:	Always on	
Reset:	soft	
Each type of Video DIP will be sent once each frame while it is enabled.		
Restriction		
Transcoder EDP going to DDI A supports only VSC DIP.		
DWord	Bit	Description
0	31:29	Reserved

VIDEO_DIP_CTL										
28	Reserved	Project: BDW								
27	Reserved	Project: BDW								
26:25	Reserved	Project: BDW								
24	Reserved	Project: BDW								
23:21	Reserved									
20	VDIP Enable VSC This bit enables the output of the Video Stream Configuration DIP.	<table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Disable VSC DIP</td></tr> <tr> <td>1b</td><td>Enable VSC DIP</td></tr> </tbody> </table> <table border="1"> <thead> <tr> <th>Restriction</th></tr> </thead> <tbody> <tr> <td>VSC can only be enabled with DisplayPort. VSC should be enabled prior to enabling PSR or stereo 3D if VSC will be used to transmit stereo 3D related information.</td></tr> </tbody> </table>	Value	Name	0b	Disable VSC DIP	1b	Enable VSC DIP	Restriction	VSC can only be enabled with DisplayPort. VSC should be enabled prior to enabling PSR or stereo 3D if VSC will be used to transmit stereo 3D related information.
Value	Name									
0b	Disable VSC DIP									
1b	Enable VSC DIP									
Restriction										
VSC can only be enabled with DisplayPort. VSC should be enabled prior to enabling PSR or stereo 3D if VSC will be used to transmit stereo 3D related information.										
19:17	Reserved									
16	VDIP Enable GCP This bit enables the output of the General Control Packet (GCP) DIP. GCP is different from other DIPs in that much of the payload is automatically reflected in the packet, and therefore there is a VIDEO_DIP_GCP register instead of DIP data buffers for GCP.	<table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Disable GCP DIP</td></tr> <tr> <td>1b</td><td>Enable GCP DIP</td></tr> </tbody> </table> <table border="1"> <thead> <tr> <th>Restriction</th></tr> </thead> <tbody> <tr> <td>GCP is only supported with HDMI when the bits per color is not equal to 8. GCP must be enabled prior to enabling TRANS_DDI_FUNC_CTL for HDMI with bits per color not equal to 8 and disabled after disabling TRANS_DDI_FUNC_CTL</td></tr> </tbody> </table>	Value	Name	0b	Disable GCP DIP	1b	Enable GCP DIP	Restriction	GCP is only supported with HDMI when the bits per color is not equal to 8. GCP must be enabled prior to enabling TRANS_DDI_FUNC_CTL for HDMI with bits per color not equal to 8 and disabled after disabling TRANS_DDI_FUNC_CTL
Value	Name									
0b	Disable GCP DIP									
1b	Enable GCP DIP									
Restriction										
GCP is only supported with HDMI when the bits per color is not equal to 8. GCP must be enabled prior to enabling TRANS_DDI_FUNC_CTL for HDMI with bits per color not equal to 8 and disabled after disabling TRANS_DDI_FUNC_CTL										
15:13	Reserved									

VIDEO_DIP_CTL								
12	VDIP Enable AVI This bit enables the output of the Auxiliary Video Information DIP.							
	<table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Disable AVI DIP</td></tr> <tr> <td>1b</td><td>Enable AVI DIP</td></tr> </tbody> </table>	Value	Name	0b	Disable AVI DIP	1b	Enable AVI DIP	
Value	Name							
0b	Disable AVI DIP							
1b	Enable AVI DIP							
		Restriction						
		Only enable with HDMI.						
11:9	Reserved							
8	VDIP Enable VS This bit enables the output of the Vendor Specific (VS) DIP.							
	<table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Disable VS DIP</td></tr> <tr> <td>1b</td><td>Enable VS DIP</td></tr> </tbody> </table>	Value	Name	0b	Disable VS DIP	1b	Enable VS DIP	
Value	Name							
0b	Disable VS DIP							
1b	Enable VS DIP							
		Restriction						
		Only enable with HDMI.						
7:5	Reserved							
4	VDIP Enable GMP This bit enables the output of the Gamut Metadata Packet (GMP) DIP. GMP can be enabled with either DisplayPort or HDMI.							
	<table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Disable GMP DIP</td></tr> <tr> <td>1b</td><td>Enable GMP DIP</td></tr> </tbody> </table>	Value	Name	0b	Disable GMP DIP	1b	Enable GMP DIP	
Value	Name							
0b	Disable GMP DIP							
1b	Enable GMP DIP							
		Restriction						
		GMP is not supported on transcoder EDP going to DDI A.						
3:1	Reserved							
0	VDIP Enable SPD This bit enables the output of the Source Product Description (SPD) DIP.							
	<table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Disable SPD DIP</td></tr> <tr> <td>1b</td><td>Enable SPD DIP</td></tr> </tbody> </table>	Value	Name	0b	Disable SPD DIP	1b	Enable SPD DIP	
Value	Name							
0b	Disable SPD DIP							
1b	Enable SPD DIP							
		Restriction						
		Only enable with HDMI.						

VIDEO_DIP_DATA

VIDEO_DIP_DATA	
Register Space:	MMIO: 0/2/0
Project:	BDW
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	60220h-6023Fh
Name:	Transcoder A Video Data Island Packet AVI Data
ShortName:	VIDEO_DIP_AVI_DATA_A_*
Valid Projects:	BDW
Power:	off/on
Reset:	soft
Address:	60260h-6027Fh
Name:	Transcoder A Video Data Island Packet VS Data
ShortName:	VIDEO_DIP_VS_DATA_A_*
Valid Projects:	BDW
Power:	off/on
Reset:	soft
Address:	602A0h-602BFh
Name:	Transcoder A Video Data Island Packet SPD Data
ShortName:	VIDEO_DIP_SPD_DATA_A_*
Valid Projects:	BDW
Power:	off/on
Reset:	soft
Address:	602E0h-602FFh
Name:	Transcoder A Video Data Island Packet GMP Data
ShortName:	VIDEO_DIP_GMP_DATA_A_*
Valid Projects:	BDW
Power:	off/on
Reset:	soft
Address:	60320h-60343h
Name:	Transcoder A Video Data Island Packet VSC Data
ShortName:	VIDEO_DIP_VSC_DATA_A_*
Valid Projects:	BDW
Power:	off/on
Reset:	soft

VIDEO_DIP_DATA

Address:	61220h-6123Fh
Name:	Transcoder B Video Data Island Packet AVI Data
ShortName:	VIDEO_DIP_AVI_DATA_B_*
Valid Projects:	BDW
Power:	off/on
Reset:	soft
Address:	61260h-6127Fh
Name:	Transcoder B Video Data Island Packet VS Data
ShortName:	VIDEO_DIP_VS_DATA_B_*
Valid Projects:	BDW
Power:	off/on
Reset:	soft
Address:	612A0h-612BFh
Name:	Transcoder B Video Data Island Packet SPD Data
ShortName:	VIDEO_DIP_SPD_DATA_B_*
Valid Projects:	BDW
Power:	off/on
Reset:	soft
Address:	612E0h-612FFh
Name:	Transcoder B Video Data Island Packet GMP Data
ShortName:	VIDEO_DIP_GMP_DATA_B_*
Valid Projects:	BDW
Power:	off/on
Reset:	soft
Address:	61320h-61343h
Name:	Transcoder B Video Data Island Packet VSC Data
ShortName:	VIDEO_DIP_VSC_DATA_B_*
Valid Projects:	BDW
Power:	off/on
Reset:	soft
Address:	62220h-6223Fh
Name:	Transcoder C Video Data Island Packet AVI Data
ShortName:	VIDEO_DIP_AVI_DATA_C_*
Valid Projects:	BDW
Power:	off/on
Reset:	soft
Address:	62260h-6227Fh

VIDEO_DIP_DATA

Name:	Transcoder C Video Data Island Packet VS Data			
ShortName:	VIDEO_DIP_VS_DATA_C_*			
Valid Projects:	BDW			
Power:	off/on			
Reset:	soft			
Address:	622A0h-622BFh			
Name:	Transcoder C Video Data Island Packet SPD Data			
ShortName:	VIDEO_DIP_SPD_DATA_C_*			
Valid Projects:	BDW			
Power:	off/on			
Reset:	soft			
Address:	622E0h-622FFh			
Name:	Transcoder C Video Data Island Packet GMP Data			
ShortName:	VIDEO_DIP_GMP_DATA_C_*			
Valid Projects:	BDW			
Power:	off/on			
Reset:	soft			
Address:	62320h-62343h			
Name:	Transcoder C Video Data Island Packet VSC Data			
ShortName:	VIDEO_DIP_VSC_DATA_C_*			
Valid Projects:	BDW			
Power:	off/on			
Reset:	soft			
Address:	6F320h-6F343h			
Name:	Transcoder EDP Video Data Island Packet VSC Data			
ShortName:	VIDEO_DIP_VSC_DATA_EDP_*			
Valid Projects:	BDW			
Power:	Always on			
Reset:	soft			
There are multiple instances of this register format per DIP type and per transcoder.				
DWord	Bit	Description		
0	31:0	<p>Video DIP DATA</p> <p>This field contains the video DIP data to be transmitted.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center; background-color: #e0f2ff;">Restriction</th> </tr> </thead> <tbody> <tr> <td>Data should be loaded before enabling the transmission through the DIP type enable bit.</td> </tr> </tbody> </table>	Restriction	Data should be loaded before enabling the transmission through the DIP type enable bit.
Restriction				
Data should be loaded before enabling the transmission through the DIP type enable bit.				

VIDEO_DIP_ECC

VIDEO_DIP_ECC	
Register Space:	MMIO: 0/2/0
Project:	BDW
Default Value:	0x00000000
Access:	RO
Size (in bits):	32
Address:	60240h-60247h
Name:	Transcoder A Video Data Island Packet AVI ECC
ShortName:	VIDEO_DIP_AVI_ECC_A_*
Valid Projects:	BDW
Power:	off/on
Reset:	soft
Address:	60280h-60287h
Name:	Transcoder A Video Data Island Packet VS ECC
ShortName:	VIDEO_DIP_VS_ECC_A_*
Valid Projects:	BDW
Power:	off/on
Reset:	soft
Address:	602C0h-602C7h
Name:	Transcoder A Video Data Island Packet SPD ECC
ShortName:	VIDEO_DIP_SPD_ECC_A_*
Valid Projects:	BDW
Power:	off/on
Reset:	soft
Address:	60300h-60313h
Name:	Transcoder A Video Data Island Packet GMP ECC
ShortName:	VIDEO_DIP_GMP_ECC_A_*
Valid Projects:	BDW
Power:	off/on
Reset:	soft
Address:	60344h-6034Fh
Name:	Transcoder A Video Data Island Packet VSC ECC
ShortName:	VIDEO_DIP_VSC_ECC_A_*
Valid Projects:	BDW
Power:	off/on
Reset:	soft

VIDEO_DIP_ECC	
Address:	61240h-61247h
Name:	Transcoder B Video Data Island Packet AVI ECC
ShortName:	VIDEO_DIP_AVI_ECC_B_*
Valid Projects:	BDW
Power:	off/on
Reset:	soft
Address:	61280h-61287h
Name:	Transcoder B Video Data Island Packet VS ECC
ShortName:	VIDEO_DIP_VS_ECC_B_*
Valid Projects:	BDW
Power:	off/on
Reset:	soft
Address:	612C0h-612C7h
Name:	Transcoder B Video Data Island Packet SPD ECC
ShortName:	VIDEO_DIP_SPD_ECC_B_*
Valid Projects:	BDW
Power:	off/on
Reset:	soft
Address:	61300h-61313h
Name:	Transcoder B Video Data Island Packet GMP ECC
ShortName:	VIDEO_DIP_GMP_ECC_B_*
Valid Projects:	BDW
Power:	off/on
Reset:	soft
Address:	61344h-6134Fh
Name:	Transcoder B Video Data Island Packet VSC ECC
ShortName:	VIDEO_DIP_VSC_ECC_B_*
Valid Projects:	BDW
Power:	off/on
Reset:	soft
Address:	62240h-62247h
Name:	Transcoder C Video Data Island Packet AVI ECC
ShortName:	VIDEO_DIP_AVI_ECC_C_*
Valid Projects:	BDW
Power:	off/on
Reset:	soft
Address:	62280h-62287h

VIDEO_DIP_ECC		
Name:	Transcoder C Video Data Island Packet VS ECC	
ShortName:	VIDEO_DIP_VS_ECC_C_*	
Valid Projects:	BDW	
Power:	off/on	
Reset:	soft	
Address:	622C0h-622C7h	
Name:	Transcoder C Video Data Island Packet SPD ECC	
ShortName:	VIDEO_DIP_SPD_ECC_C_*	
Valid Projects:	BDW	
Power:	off/on	
Reset:	soft	
Address:	62300h-62313h	
Name:	Transcoder C Video Data Island Packet GMP ECC	
ShortName:	VIDEO_DIP_GMP_ECC_C_*	
Valid Projects:	BDW	
Power:	off/on	
Reset:	soft	
Address:	62344h-6234Fh	
Name:	Transcoder C Video Data Island Packet VSC ECC	
ShortName:	VIDEO_DIP_VSC_ECC_C_*	
Valid Projects:	BDW	
Power:	off/on	
Reset:	soft	
Address:	6F344h-6F34Fh	
Name:	Transcoder EDP Video Data Island Packet VSC ECC	
ShortName:	VIDEO_DIP_VSC_ECC_EDP_*	
Valid Projects:	BDW	
Power:	Always on	
Reset:	soft	
There are multiple instances of this register format per DIP type and per transcoder.		
DWord	Bit	Description
0	31:0	Video DIP ECC This field contains the video DIP ECC value for read back.

VIDEO_DIP_GCP

VIDEO_DIP_GCP				
Register Space:		MMIO: 0/2/0		
Project:		BDW		
Default Value:		0x00000000		
Access:		R/W		
Size (in bits):		32		
Address:		60210h-60213h		
Name:		Transcoder A Video Data Island Packet GCP		
ShortName:		VIDEO_DIP_GCP_A		
Valid Projects:		BDW		
Power:		off/on		
Reset:		soft		
Address:		61210h-61213h		
Name:		Transcoder B Video Data Island Packet GCP		
ShortName:		VIDEO_DIP_GCP_B		
Valid Projects:		BDW		
Power:		off/on		
Reset:		soft		
Address:		62210h-62213h		
Name:		Transcoder C Video Data Island Packet GCP		
ShortName:		VIDEO_DIP_GCP_C		
Valid Projects:		BDW		
Power:		off/on		
Reset:		soft		
DWord	Bit	Description		
0	31:3	Reserved		
		Format:	MBZ	
	2	GCP color indication		
		Value	Name	Description
		0b	Don't Indicate	Don't indicate color depth. CD and PP bits in GCP set to zero.
		1b	Indicate	Indicate color depth using CD bits in GCP. The color depth value comes from the TRANS_DDI_FUNC_CTL register.
		Restriction		
This bit must be set when in HDMI deep color (12 BPC) mode.				

VIDEO_DIP_GCP

	1	GCP default phase enable GCP default phase indicates that video timings meet alignment requirements such that the following conditions are met: <ol style="list-style-type: none"> 1. Htotal is an even number 2. Hactive is an even number 3. Front and back porches for Hsync are even numbers 4. Vsync always starts on an even-numbered pixel within a line in interlaced modes (starting counting with 0) <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #d9e1f2;"> <th style="text-align: center; padding: 2px;">Value</th><th style="text-align: center; padding: 2px;">Name</th><th style="text-align: center; padding: 2px;">Description</th></tr> </thead> <tbody> <tr> <td style="text-align: center; padding: 2px;">0b</td><td style="text-align: center; padding: 2px;">Clear</td><td style="text-align: center; padding: 2px;">Default phase bit in GCP is cleared.</td></tr> <tr> <td style="text-align: center; padding: 2px;">1b</td><td style="text-align: center; padding: 2px;">Set</td><td style="text-align: center; padding: 2px;">Default phase bit in GCP is set.</td></tr> </tbody> </table> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #d9e1f2;"> <th style="text-align: center; padding: 2px;">Restriction</th></tr> </thead> <tbody> <tr> <td style="text-align: center; padding: 2px;">Do not set this bit if these requirements are not met.</td></tr> </tbody> </table>	Value	Name	Description	0b	Clear	Default phase bit in GCP is cleared.	1b	Set	Default phase bit in GCP is set.	Restriction	Do not set this bit if these requirements are not met.
Value	Name	Description											
0b	Clear	Default phase bit in GCP is cleared.											
1b	Set	Default phase bit in GCP is set.											
Restriction													
Do not set this bit if these requirements are not met.													
	0	Reserved											

Video BIOS ROM Base Address

ROMADR_0_2_0_PCI - Video BIOS ROM Base Address

Register Space:	PCI: 0/2/0			
Project:	BDW			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	00030h			
The IGD does not use a separate BIOS ROM, therefore this register is hardwired to 0s.				
DWord	Bit	Description		
0	31:18	ROM Base Address		
		<table border="1"> <tr> <td>Default Value:</td><td>0000000000000000b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Hardwired to 0's.</p>	Default Value:	0000000000000000b
Default Value:	0000000000000000b			
Access:	RO			
17:11	Address Mask			
	<table border="1"> <tr> <td>Default Value:</td><td>0000000b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>Hardwired to 0s to indicate 256 KB address range.</p>	Default Value:	0000000b	Access:
Default Value:	0000000b			
Access:	RO			
10:1	Reserved			
0	0	ROM BIOS Enable		
		<table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	0b
Default Value:	0b			
Access:	RO			
Hardwired to 0 to indicate ROM not accessible.				

Video Enhancement Mode Register

VEBOX_MODE - Video Enhancement Mode Register

Register Space:	MMIO: 0/2/0
Project:	BDW
Source:	VideoEnhancementCS
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1

Address: 1A29Ch

DWord	Bit	Description						
0	31:16	Mask Bits <table border="1"> <tr> <td>Format:</td> <td>Mask[15:0]</td> </tr> </table> <p>Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)</p>	Format:	Mask[15:0]				
Format:	Mask[15:0]							
	15	Exelist Enable <table border="1"> <tr> <td>Default Value:</td> <td>0h</td> </tr> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Mask:</td> <td>MMIO#31</td> </tr> </table> <p>When set, software can utilize the exelist registers to load a context into hardware. When this bit is clear the exelist mechanism cannot be used. The ring must be loaded via MMIO access.</p> <p style="text-align: center;">Programming Notes</p> <p>This bit is not intended to be changed dynamically. Changing the value of this bit while rendering is in progress will have UNDEFINED results. This bit should be changed only after a full reset and before submitting any commands to the device</p>	Default Value:	0h	Project:	BDW	Mask:	MMIO#31
Default Value:	0h							
Project:	BDW							
Mask:	MMIO#31							
	14	Interrupt Steering Bit <table border="1"> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Format:</td> <td>U1</td> </tr> </table> <p>When set, Command Streamer sends interrupt messages to the SHIM of the ON CHIP Micro Controller through message channel.</p> <p>When reset, Command Streamer sends the interrupt messages to Display Engine as config writes on GAM interface.</p>	Project:	BDW	Format:	U1		
Project:	BDW							
Format:	U1							
	13:10	Reserved <table border="1"> <tr> <td>Project:</td> <td>All</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Project:	All	Format:	MBZ		
Project:	All							
Format:	MBZ							

VEBOX_MODE - Video Enhancement Mode Register

	9	Per-Process GTT Enable									
		<table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>Enable Per-Process GTT BS Mode Enable</td></tr> </table>	Project:	All	Format:	Enable Per-Process GTT BS Mode Enable					
Project:	All										
Format:	Enable Per-Process GTT BS Mode Enable										
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0h</td><td>PPGTT Disable [Default]</td><td>When clear, the Global GTT will be used to translate memory access from designated commands and for commands that select the PPGTT as their translation space in Basic Scheduler Mode.</td></tr> <tr> <td>1h</td><td>PPGTT Enable</td><td>When set, the PPGTT will be used to translate memory access from designated commands and for commands that select the PPGTT as their translation space.</td></tr> </tbody> </table>	Value	Name	Description	0h	PPGTT Disable [Default]	When clear, the Global GTT will be used to translate memory access from designated commands and for commands that select the PPGTT as their translation space in Basic Scheduler Mode.	1h	PPGTT Enable	When set, the PPGTT will be used to translate memory access from designated commands and for commands that select the PPGTT as their translation space.
Value	Name	Description									
0h	PPGTT Disable [Default]	When clear, the Global GTT will be used to translate memory access from designated commands and for commands that select the PPGTT as their translation space in Basic Scheduler Mode.									
1h	PPGTT Enable	When set, the PPGTT will be used to translate memory access from designated commands and for commands that select the PPGTT as their translation space.									
		Programming Notes									
		This bit is used for enabling PPGTT access in Ring Buffer mode of scheduling. Privilege field in context descriptor states the same in Execlist mode of scheduling. This field should be set before programming PDP0/1/2/3 registers in order to set the PPGTT translation of memory access.									
	8	Reserved									
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> </table>	Project:	BDW							
Project:	BDW										
	7	64Bit Virtual Addressing Enable									
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>Enable</td></tr> </table>	Project:	BDW	Format:	Enable					
Project:	BDW										
Format:	Enable										
		Per-Process GTT Enable									
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0h</td><td>64Bit Virtual Addressing Disable [Default]</td><td>When clear indicates GFX operating in 32bit Virtual Addressing for PPGTT based memory access.</td></tr> <tr> <td>1h</td><td>64Bit Virtual Addressing Enable</td><td>When Set indicates GFX operating in 64bit (48bit Canonical) Virtual Addressing for PPGTT based memory access.</td></tr> </tbody> </table>	Value	Name	Description	0h	64Bit Virtual Addressing Disable [Default]	When clear indicates GFX operating in 32bit Virtual Addressing for PPGTT based memory access.	1h	64Bit Virtual Addressing Enable	When Set indicates GFX operating in 64bit (48bit Canonical) Virtual Addressing for PPGTT based memory access.
Value	Name	Description									
0h	64Bit Virtual Addressing Disable [Default]	When clear indicates GFX operating in 32bit Virtual Addressing for PPGTT based memory access.									
1h	64Bit Virtual Addressing Enable	When Set indicates GFX operating in 64bit (48bit Canonical) Virtual Addressing for PPGTT based memory access.									
		Programming Notes									
		This bit is only valid when PPGTT is enabled in ring buffer mode of scheduling. Context Descriptor has a similar bit to control 64bit virtual addressing in execlist mode of scheduling. Irrespective of this field set or clear virtual addresses translated through GGTT are always 32Bit. This field should be programmed before enabling PPGTT access. When this field is not set or for GGTT virtual addresses, Graphics Address [47:32] field of any commands or register exercised by SW should be programmed to 0x0.									
	6:5	Reserved									
		<table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	All	Format:	MBZ					
Project:	All										
Format:	MBZ										

VEBOX_MODE - Video Enhancement Mode Register

	4	Reserved	Project:	BDW
	3:1	Reserved	Project:	BDW
			Format:	MBZ
	0	Privilege Check Disable	Project:	BDW
			Format:	Enable
This field when set, disables Privilege Violation checks on non-privileged batch buffers. When set Privileged commands are allowed to be executed from non-privileged batch buffers.				

Video Mode Register

MFX_MODE - Video Mode Register													
Register Space: MMIO: 0/2/0 Project: BDW Source: VideoCS, VideoCS2 Default Value: 0x00000000 Access: R/W Size (in bits): 32 Trusted Type: 1													
Address: 1229Ch													
Valid Projects: [BDW]													
Address: 1C29Ch													
Valid Projects: [DevBDW:GT3, DevBDW:GT4]													
DWord	Bit	Description											
0	31:16	Mask Bits <table border="1"> <tr> <td>Format:</td><td>Mask[15:0]</td></tr> <tr> <td colspan="2" rowspan="2">Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)</td></tr> </table>	Format:	Mask[15:0]	Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)								
Format:	Mask[15:0]												
Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)													
15	Exelist Enable <table border="1"> <tr> <td>Default Value:</td><td>0h</td></tr> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Mask:</td><td>MMIO#31</td></tr> <tr> <td colspan="2">When set, software can utilize the exelist registers to load a context into hardware. When this bit is clear the Execution List mechanism cannot be used. The ring must be loaded via MMIO access.</td></tr> <tr> <td colspan="2" style="text-align: center;">Programming Notes</td></tr> <tr> <td colspan="2" rowspan="3">This bit is not intended to be changed dynamically. Changing the value of this bit while rendering is in progress will have UNDEFINED results. This bit should be changed only after a full reset and before submitting any commands to the device</td></tr> </table>	Default Value:	0h	Project:	BDW	Mask:	MMIO#31	When set, software can utilize the exelist registers to load a context into hardware. When this bit is clear the Execution List mechanism cannot be used. The ring must be loaded via MMIO access.		Programming Notes		This bit is not intended to be changed dynamically. Changing the value of this bit while rendering is in progress will have UNDEFINED results. This bit should be changed only after a full reset and before submitting any commands to the device	
Default Value:	0h												
Project:	BDW												
Mask:	MMIO#31												
When set, software can utilize the exelist registers to load a context into hardware. When this bit is clear the Execution List mechanism cannot be used. The ring must be loaded via MMIO access.													
Programming Notes													
This bit is not intended to be changed dynamically. Changing the value of this bit while rendering is in progress will have UNDEFINED results. This bit should be changed only after a full reset and before submitting any commands to the device													
		Interrupt Steering Bit <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>U1</td></tr> <tr> <td colspan="2">When set, Command Streamer sends interrupt messages to the SHIM of the ON CHIP Micro Controller through message channel. When reset, Command Streamer sends the interrupt messages to Display Engine as config writes on GAM interface.</td></tr> </table>	Project:	BDW	Format:	U1	When set, Command Streamer sends interrupt messages to the SHIM of the ON CHIP Micro Controller through message channel. When reset, Command Streamer sends the interrupt messages to Display Engine as config writes on GAM interface.						
Project:	BDW												
Format:	U1												
When set, Command Streamer sends interrupt messages to the SHIM of the ON CHIP Micro Controller through message channel. When reset, Command Streamer sends the interrupt messages to Display Engine as config writes on GAM interface.													
13:10	Reserved <table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	All	Format:	MBZ								
Project:	All												
Format:	MBZ												

MFX_MODE - Video Mode Register

	9	Per-Process GTT Enable									
		<table border="1"> <tr> <td>Format:</td><td colspan="2">Enable Per-Process GTT BS Mode Enable</td></tr> </table>	Format:	Enable Per-Process GTT BS Mode Enable							
Format:	Enable Per-Process GTT BS Mode Enable										
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0h</td><td>PPGTT Disable [Default]</td><td>When clear, the Global GTT will be used to translate memory access from designated commands and for commands that select the PPGTT as their translation space.</td></tr> <tr> <td>1h</td><td>PPGTT Enable</td><td>When set, the PPGTT will be used to translate memory access from designated commands and for commands that select the PPGTT as their translation space.</td></tr> </tbody> </table>	Value	Name	Description	0h	PPGTT Disable [Default]	When clear, the Global GTT will be used to translate memory access from designated commands and for commands that select the PPGTT as their translation space.	1h	PPGTT Enable	When set, the PPGTT will be used to translate memory access from designated commands and for commands that select the PPGTT as their translation space.
Value	Name	Description									
0h	PPGTT Disable [Default]	When clear, the Global GTT will be used to translate memory access from designated commands and for commands that select the PPGTT as their translation space.									
1h	PPGTT Enable	When set, the PPGTT will be used to translate memory access from designated commands and for commands that select the PPGTT as their translation space.									
		Programming Notes									
		This bit is used for enabling PPGTT access in Ring Buffer mode of scheduling. Privilege field in context descriptor states the same in Execlist Mode of scheduling. This field should be set before programming PDP0/1/2/3 registers in order to set the PPGTT translation of memory access.									
	8	Reserved									
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> </table>	Project:	BDW							
Project:	BDW										
	7	64Bit Virtual Addressing Enable									
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>Enable</td></tr> </table>	Project:	BDW	Format:	Enable					
Project:	BDW										
Format:	Enable										
		Per-Process GTT Enable									
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0h</td><td>64Bit Virtual Addressing Disable [Default]</td><td>When clear indicates GFX operating in 32bit Virtual Addressing for PPGTT based memory access.</td></tr> <tr> <td>1h</td><td>64Bit Virtual Addressing Enable</td><td>When Set indicates GFX operating in 64bit (48bit Canonical) Virtual Addressing for PPGTT based memory access.</td></tr> </tbody> </table>	Value	Name	Description	0h	64Bit Virtual Addressing Disable [Default]	When clear indicates GFX operating in 32bit Virtual Addressing for PPGTT based memory access.	1h	64Bit Virtual Addressing Enable	When Set indicates GFX operating in 64bit (48bit Canonical) Virtual Addressing for PPGTT based memory access.
Value	Name	Description									
0h	64Bit Virtual Addressing Disable [Default]	When clear indicates GFX operating in 32bit Virtual Addressing for PPGTT based memory access.									
1h	64Bit Virtual Addressing Enable	When Set indicates GFX operating in 64bit (48bit Canonical) Virtual Addressing for PPGTT based memory access.									
		Programming Notes									
		This bit is only valid when PPGTT is enabled in ring buffer mode of scheduling. Context Descriptor has a similar bit to control 64bit virtual addressing in execlist mode of scheduling. Irrespective of this field set or clear virtual addresses translated through GTT are always 32Bit. This field should be programmed before enabling PPGTT access. When this field is not set or for GTT virtual addresses, Graphics Address [47:32] field of any commands or register exercised by SW should be programmed to 0x0.									
	6:5	Reserved									
		<table border="1"> <tr> <td>Project:</td><td>All</td></tr> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Project:	All	Format:	MBZ					
Project:	All										
Format:	MBZ										
	4	Reserved									
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> </table>	Project:	BDW							
Project:	BDW										

MFX_MODE - Video Mode Register

	3:1	Reserved	
		Project:	BDW
		Format:	MBZ
	0	Privilege Check Disable	
		Project:	BDW
		Format:	Enable
		This field when set, disables Privilege Violation checks on non-privileged batch buffers. When set Privileged commands are allowed to be executed from non-privileged batch buffers.	

VS Invocation Counter

VS_INVOCATION_COUNT - VS Invocation Counter		
Register Space: MMIO: 0/2/0 Project: BDW Source: RenderCS Default Value: 0x00000000, 0x00000000 Access: R/W Size (in bits): 64 Trusted Type: 1		
Address: 02320h Valid Projects: BDW		
This register stores the value of the vertex count shaded by VS. This register is part of the context save and restore.		
DWord	Bit	Description
0	63:32	VS Invocation Count Report UDW Number of vertices that are dispatched as threads by the VS stage. Updated only when Statistics Enable is set in VS_STATE (see the Vertex Shader Chapter in the 3D Volume.)
	31:0	VS Invocation Count Report LDW Number of vertices that are dispatched as threads by the VS stage. Updated only when Statistics Enable is set in VS_STATE (see the Vertex Shader Chapter in the 3D Volume.)

VSYNC

VSYNC		
Register Space: MMIO: 0/2/0 Project: DevLPT:H Default Value: 0x00000000 Access: R/W Size (in bits): 32		
Address: E0014h-E0017h Name: Transcoder A Vertical Sync ShortName: TRANS_VSYNC_A Power: Always on Reset: soft		
DWord	Bit	Description
0	31:29	Reserved Format: MBZ
	28:16	Vertical Sync End This field specifies the Vertical Sync End position relative to the vertical active display start. It is programmed with VerticalActive+FrontPorch+Sync-1. This value must be greater than the vertical sync start and less than Vertical Total.
	15:13	Reserved Format: MBZ
	12:0	Vertical Sync Start This field specifies the Vertical Sync Start position relative to the vertical active display start. It is programmed with VerticalActive+FrontPorch-1. This value must be greater than Vertical Active.

VSYNC SHIFT

VSYNC SHIFT			
Register Space: MMIO: 0/2/0 Project: DevLPT:H Default Value: 0x00000000 Access: R/W Size (in bits): 32			
Address: E0028h-E002Bh Name: Transcoder A Vertical Sync Shift ShortName: TRANS_VSYNCSHIFT_A Power: Always on Reset: soft			
DWord	Bit	Description	
0	31:13	Reserved	Format: MBZ
	12:0	Second Field VSync Shift	<p>This value specifies the vertical sync alignment for the start of the interlaced second field, expressed in terms of the absolute pixel number relative to the horizontal active display start. This value will only be used if the transcoder is in an interlaced mode. Typically, the interlaced second field vertical sync should start one pixel after the point halfway between successive horizontal syncs, so the value of this register should be programmed to: (horizontal sync start - floor[horizontal total / 2]) (Calculations uses the actual horizontal sync start and horizontal total values and not the minus one values programmed into the registers) This vertical sync shift only occurs during the interlaced second field. In all other cases the vertical sync start position is aligned with horizontal sync start.</p>

VTOTAL

VTOTAL			
Register Space: MMIO: 0/2/0 Project: DevLPT:H Default Value: 0x00000000 Access: R/W Size (in bits): 32			
Address: E000Ch-E000Fh Name: Transcoder A Vertical Total ShortName: TRANS_VTOTAL_A Power: Always on Reset: soft			
DWord	Bit	Description	
0	31:29	Reserved	Format: MBZ
	28:16	Vertical Total This field specifies Vertical Total size. This should be equal to the sum of the vertical active and the vertical blank sizes. For progressive display modes, this field is programmed to the number of lines desired minus one. For interlaced display modes, this field is programmed with the number of lines desired minus two. The vertical counter is incremented on the leading edge of the horizontal sync. Both even and odd vertical totals are supported. This register must always be programmed to the same value as the Vertical Blank End.	
	15:12	Reserved	Format: MBZ
	11:0	Vertical Active This field specifies Vertical Active Display size. Note that the first vertical active display line is considered line number 0. This field is programmed to the number of lines desired minus one. This register must always be programmed to the same value as the Vertical Blank Start.	

Wait For Event and Display Flip Flags Register

SYNC_FLIP_STATUS - Wait For Event and Display Flip Flags Register

Register Space:	MMIO: 0/2/0
Project:	BDW
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	022D0h
Name:	RCS Wait For Event and Display Flip Flags Register
ShortName:	RCS_SYNC_FLIP_STATUS
Valid Projects:	[BDW]
Address:	122D0h-122D3h
Name:	Wait For Event and Display Flip Flags Register
ShortName:	SYNC_FLIP_STATUS_VCSUNIT0
Address:	1A2D0h-1A2D3h
Name:	Wait For Event and Display Flip Flags Register
ShortName:	SYNC_FLIP_STATUS_VECSUNIT
Address:	1C2D0h-1C2D3h
Name:	Wait For Event and Display Flip Flags Register
ShortName:	SYNC_FLIP_STATUS_VCSUNIT1
Address:	222D0h
Name:	BCS Wait For Event and Display Flip Flags Register
ShortName:	BCS_SYNC_FLIP_STATUS
Valid Projects:	[BDW]
This register is the saved value of what wait for events are still valid. This register is part of context save and restore for RC6 feature.	

Programming Notes

Programming Restriction: This register should NEVER be programmed by SW, this is for HW internal use only.

DWord	Bit	Description	
0	31	Reserved	Format: MBZ

SYNC_FLIP_STATUS - Wait For Event and Display Flip Flags Register

	30 Display Plane A Asynchronous Display Flip Pending		
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Format:</td><td style="padding: 2px; text-align: center;">Enable</td></tr> </table>	Format:	Enable
Format:	Enable		
<p>This field enables a wait for the duration of a Display Plane A "Flip Pending" condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>			
	29 Display Plane A Synchronous Flip Display Pending		
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Format:</td><td style="padding: 2px; text-align: center;">Enable</td></tr> </table>	Format:	Enable
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	28 Display Sprite A Synchronous Flip Display Pending		
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Format:</td><td style="padding: 2px; text-align: center;">Enable</td></tr> </table>	Format:	Enable
Format:	Enable		
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	27 Reserved		
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Format:</td><td style="padding: 2px; text-align: center;">MBZ</td></tr> </table>	Format:	MBZ
Format:	MBZ		
	26 Display Plane B Asynchronous Display Flip Pending		
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Format:</td><td style="padding: 2px; text-align: center;">Enable</td></tr> </table>	Format:	Enable
Format:	Enable		
<p>This field enables a wait for the duration of a Display Plane B "Flip Pending" condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>			
	25 Display Plane B Synchronous Flip Display Pending		
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Format:</td><td style="padding: 2px; text-align: center;">Enable</td></tr> </table>	Format:	Enable
Format:	Enable		
<p>This field enables a wait for the duration of a Display Plane B Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>			

SYNC_FLIP_STATUS - Wait For Event and Display Flip Flags Register

	Display Sprite B Syncronous Flip Display Pending		
	<table border="1"> <tr> <td>Format:</td><td>Enable</td></tr> </table>	Format:	Enable
Format:	Enable		
<p>This field enables a wait for the duration of a Display Sprite B Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>			
23	Reserved		
	<table border="1"> <tr> <td>Source:</td><td>BlitterCS</td></tr> </table>	Source:	BlitterCS
Source:	BlitterCS		
	<table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ
Format:	MBZ		
23	Display Plane A Asynchronous Performance Flip Pending Wait Enable		
	<table border="1"> <tr> <td>Source:</td><td>RenderCS</td></tr> </table>	Source:	RenderCS
Source:	RenderCS		
	<table border="1"> <tr> <td>Format:</td><td>Enable</td></tr> </table>	Format:	Enable
Format:	Enable		
<p>This field enables a wait for the duration of a Display Plane A Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>			
22	Display Plane A Asynchronous Flip Pending Wait Enable		
	<table border="1"> <tr> <td>Format:</td><td>Enable</td></tr> </table>	Format:	Enable
Format:	Enable		
<p>This field enables a wait for the duration of a Display Plane A Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>			
21	Display Plane A Syncronous Flip Pending Wait Enable		
	<table border="1"> <tr> <td>Format:</td><td>Enable</td></tr> </table>	Format:	Enable
Format:	Enable		
<p>This field enables a wait for the duration of a Display Plane A Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>			
20	Display Sprite A Syncronous Flip Pending Wait Enable		
	<table border="1"> <tr> <td>Format:</td><td>Enable</td></tr> </table>	Format:	Enable
Format:	Enable		
<p>This field enables a wait for the duration of a Display Sprite A Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>			
19	Reserved		
	<table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ
Format:	MBZ		

SYNC_FLIP_STATUS - Wait For Event and Display Flip Flags Register

18	Display Pipe A Scan Line Wait Enable				
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Format:</td><td style="padding: 2px;">Enable</td></tr> </table>	Format:	Enable		
Format:	Enable				
<p>This field enables a wait while a Display Pipe A Scan Line condition exists. This condition is defined as the the start of the scan line specified in the Pipe A Display Scan Line Count Range Compare Register. See Scan Line Event in the Device Programming Interface chapter of MI Functions.</p>					
17	Display Pipe A Vertical Blank Wait Enable				
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Format:</td><td style="padding: 2px;">Enable</td></tr> </table>	Format:	Enable		
Format:	Enable				
<p>This field enables a wait until the next Display Pipe A Vertical Blank event occurs. This event is defined as the start of the next Display Pipe A vertical blank period. Note that this can cause a wait for up to an entire refresh period. See Vertical Blank Event (See Programming Interface).</p>					
16	Reserved				
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Project:</td><td style="padding: 2px;">BDW</td></tr> <tr> <td style="padding: 2px;">Format:</td><td style="padding: 2px;">MBZ</td></tr> </table>	Project:	BDW	Format:	MBZ
Project:	BDW				
Format:	MBZ				
15	Reserved				
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Source:</td><td style="padding: 2px;">BlitterCS</td></tr> <tr> <td style="padding: 2px;">Format:</td><td style="padding: 2px;">MBZ</td></tr> </table>	Source:	BlitterCS	Format:	MBZ
Source:	BlitterCS				
Format:	MBZ				
15	Display Plane B Asynchronous Performance Flip Pending Wait Enable				
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Source:</td><td style="padding: 2px;">RenderCS</td></tr> <tr> <td style="padding: 2px;">Format:</td><td style="padding: 2px;">Enable</td></tr> </table>	Source:	RenderCS	Format:	Enable
Source:	RenderCS				
Format:	Enable				
<p>This field enables a wait for the duration of a Display Plane B Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>					
14	Display Plane B Asynchronous Flip Pending Wait Enable				
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Format:</td><td style="padding: 2px;">Enable</td></tr> </table>	Format:	Enable		
Format:	Enable				
<p>This field enables a wait for the duration of a Display Plane B Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>					
13	Display Plane B Synchronous Flip Pending Wait Enable				
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Format:</td><td style="padding: 2px;">Enable</td></tr> </table>	Format:	Enable		
Format:	Enable				
<p>This field enables a wait for the duration of a Display Plane B Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>					

SYNC_FLIP_STATUS - Wait For Event and Display Flip Flags Register

12	Display Sprite B Syncronous Flip Pending Wait Enable				
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Format:</td><td style="padding: 2px;">Enable</td></tr> </table>	Format:	Enable		
Format:	Enable				
<p>This field enables a wait for the duration of a Display Sprite B Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>					
11	Reserved				
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Format:</td><td style="padding: 2px;">MBZ</td></tr> </table>	Format:	MBZ		
Format:	MBZ				
10	Display Pipe B Scan Line Wait Enable				
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Format:</td><td style="padding: 2px;">Enable</td></tr> </table>	Format:	Enable		
Format:	Enable				
<p>This field enables a wait while a Display Pipe B Scan Line condition exists. This condition is defined as the the start of the scan line specified in the Pipe B Display Scan Line Count Range Compare Register. See Scan Line Event in the Device Programming Interface chapter of MI Functions.</p>					
9	Display Pipe B Vertical Blank Wait Enable				
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Format:</td><td style="padding: 2px;">Enable</td></tr> </table>	Format:	Enable		
Format:	Enable				
<p>This field enables a wait until the next Display Pipe B Vertical Blank event occurs. This event is defined as the start of the next Display Pipe B vertical blank period. Note that this can cause a wait for up to an entire refresh period. See Vertical Blank Event (See Programming Interface).</p>					
8	Reserved				
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Project:</td><td style="padding: 2px;">BDW</td></tr> <tr> <td style="padding: 2px;">Format:</td><td style="padding: 2px;">MBZ</td></tr> </table>	Project:	BDW	Format:	MBZ
Project:	BDW				
Format:	MBZ				
7:5	Reserved				
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Format:</td><td style="padding: 2px;">MBZ</td></tr> </table>	Format:	MBZ		
Format:	MBZ				
4:0	Reserved				
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Project:</td><td style="padding: 2px;">BDW</td></tr> <tr> <td style="padding: 2px;">Format:</td><td style="padding: 2px;">MBZ</td></tr> </table>	Project:	BDW	Format:	MBZ
Project:	BDW				
Format:	MBZ				

Wait For Event and Display Flip Flags Register 1

SYNC_FLIP_STATUS_1 - Wait For Event and Display Flip Flags Register 1					
Register Space:	MMIO: 0/2/0				
Project:	BDW				
Default Value:	0x00000000 [BDW]				
Access:	R/W				
Size (in bits):	32				
Address:	022D4h				
Name:	RCS Wait For Event and Display Flip Flags Register 1				
ShortName:	RCS_SYNC_FLIP_STATUS_1				
Address:	122D4h-122D7h				
Name:	Wait For Event and Display Flip Flags Register 1				
ShortName:	SYNC_FLIP_STATUS_1_VCSUNIT0				
Address:	1A2D4h-1A2D7h				
Name:	Wait For Event and Display Flip Flags Register 1				
ShortName:	SYNC_FLIP_STATUS_1_VECSUNIT				
Address:	1C2D4h-1C2D7h				
Name:	Wait For Event and Display Flip Flags Register 1				
ShortName:	SYNC_FLIP_STATUS_1_VCSUNIT1				
Address:	222D4h				
Name:	BCS Wait For Event and Display Flip Flags Register 1				
ShortName:	BCS_SYNC_FLIP_STATUS_1				
Valid Projects:	[DevBDW]				
This register is the saved value of what wait for events are still valid. This register is part of context save and restore for RC6 feature.					
DWord	Bit	Description			
0	31:27	Reserved <table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ	
	Format:	MBZ			
26	Display Sprite C3 Synchronous Flip Pending Wait Enable <table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>Enable</td></tr> </table> <p>This field enables a wait for the duration of a Display Sprite C3 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>	Project:	BDW	Format:	Enable
Project:	BDW				
Format:	Enable				

SYNC_FLIP_STATUS_1 - Wait For Event and Display Flip Flags Register 1

25	Display Sprite C3 Synchronous Flip Display Pending				
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Project:</td><td style="padding: 2px;">BDW</td></tr> <tr> <td style="padding: 2px;">Format:</td><td style="padding: 2px;">Enable</td></tr> </table>	Project:	BDW	Format:	Enable
Project:	BDW				
Format:	Enable				
	<p>This field enables a wait for the duration of a Display Sprite C3 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>				
<hr/>					
24	Display Sprite B3 Synchronous Flip Pending Wait Enable				
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Project:</td><td style="padding: 2px;">BDW</td></tr> <tr> <td style="padding: 2px;">Format:</td><td style="padding: 2px;">Enable</td></tr> </table>	Project:	BDW	Format:	Enable
Project:	BDW				
Format:	Enable				
	<p>This field enables a wait for the duration of a Display Sprite B3 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>				
<hr/>					
23	Display Sprite B3 Synchronous Flip Display Pending				
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Project:</td><td style="padding: 2px;">BDW</td></tr> <tr> <td style="padding: 2px;">Format:</td><td style="padding: 2px;">Enable</td></tr> </table>	Project:	BDW	Format:	Enable
Project:	BDW				
Format:	Enable				
	<p>This field enables a wait for the duration of a Display Sprite B3 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>				
<hr/>					
22	Display Sprite A3 Synchronous Flip Pending Wait Enable				
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Project:</td><td style="padding: 2px;">BDW</td></tr> <tr> <td style="padding: 2px;">Format:</td><td style="padding: 2px;">Enable</td></tr> </table>	Project:	BDW	Format:	Enable
Project:	BDW				
Format:	Enable				
	<p>This field enables a wait for the duration of a Display Sprite A3 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>				
<hr/>					
21	Display Sprite A3 Synchronous Flip Display Pending				
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Project:</td><td style="padding: 2px;">BDW</td></tr> <tr> <td style="padding: 2px;">Format:</td><td style="padding: 2px;">Enable</td></tr> </table>	Project:	BDW	Format:	Enable
Project:	BDW				
Format:	Enable				
	<p>This field enables a wait for the duration of a Display Sprite A3 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>				

SYNC_FLIP_STATUS_1 - Wait For Event and Display Flip Flags Register 1

20 19 18 17 16	<p>Display Sprite C2 Synchronous Flip Pending Wait Enable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>Enable</td></tr> </table> <p>This field enables a wait for the duration of a Display Sprite C2 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p> <p>Display Sprite C2 Synchronous Flip Display Pending</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>Enable</td></tr> </table> <p>This field enables a wait for the duration of a Display Sprite C2 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p> <p>Display Sprite B2 Synchronous Flip Pending Wait Enable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>Enable</td></tr> </table> <p>This field enables a wait for the duration of a Display Sprite B2 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p> <p>Display Sprite B2 Synchronous Flip Display Pending</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>Enable</td></tr> </table> <p>This field enables a wait for the duration of a Display Sprite B2 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p> <p>Display Sprite A2 Synchronous Flip Pending Wait Enable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Project:</td><td>BDW</td></tr> <tr> <td>Format:</td><td>Enable</td></tr> </table> <p>This field enables a wait for the duration of a Display Sprite A2 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>	Project:	BDW	Format:	Enable																
Project:	BDW																				
Format:	Enable																				
Project:	BDW																				
Format:	Enable																				
Project:	BDW																				
Format:	Enable																				
Project:	BDW																				
Format:	Enable																				
Project:	BDW																				
Format:	Enable																				

SYNC_FLIP_STATUS_1 - Wait For Event and Display Flip Flags Register 1

	Display Sprite A2 Synchronous Flip Display Pending					
15	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Project:</td><td style="padding: 2px;">BDW</td></tr> <tr> <td style="padding: 2px;">Format:</td><td style="padding: 2px;">Enable</td></tr> </table> <p>This field enables a wait for the duration of a Display Sprite A2 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>	Project:	BDW	Format:	Enable	
Project:	BDW					
Format:	Enable					
14	Display Plane C Scan Line Event Pending <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Project:</td><td style="padding: 2px;">BDW</td></tr> <tr> <td style="padding: 2px;">Format:</td><td style="padding: 2px;">Enable</td></tr> </table> <p>This field indicates scan line event operation is pending from Display Plane-C. This field gets set when MI_SCANLINE_INCL/EXCL command is parsed for Display Plane-C and gets reset on scan line event completion for Display Plane-C.</p>	Project:	BDW	Format:	Enable	
Project:	BDW					
Format:	Enable					
13	Display Plane B Scan Line Event Pending <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Project:</td><td style="padding: 2px;">BDW</td></tr> <tr> <td style="padding: 2px;">Format:</td><td style="padding: 2px;">Enable</td></tr> </table> <p>This field indicates scan line event operation is pending from Display Plane-B. This field gets set when MI_SCANLINE_INCL/EXCL command is parsed for Display Plane-B and gets reset on scan line event completion for Display Plane-B.</p>		Project:	BDW	Format:	Enable
Project:	BDW					
Format:	Enable					
12	Display Plane A Scan Line Event Pending <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Project:</td><td style="padding: 2px;">BDW</td></tr> <tr> <td style="padding: 2px;">Format:</td><td style="padding: 2px;">Enable</td></tr> </table> <p>This field indicates scan line event operation is pending from Display Plane-A. This field gets set when MI_SCANLINE_INCL/EXCL command is parsed for Display Plane-A and gets reset on scan line event completion for Display Plane-A.</p>	Project:	BDW	Format:	Enable	
Project:	BDW					
Format:	Enable					
11	Reserved <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Project:</td><td style="padding: 2px;">BDW</td></tr> <tr> <td style="padding: 2px;">Format:</td><td style="padding: 2px;">MBZ</td></tr> </table>	Project:	BDW	Format:	MBZ	
Project:	BDW					
Format:	MBZ					
10	Display Plane C Asynchronous Display Flip Pending <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Format:</td><td style="padding: 2px;">Enable</td></tr> </table> <p>This field enables a wait for the duration of a Display Plane C Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable			
Format:	Enable					

SYNC_FLIP_STATUS_1 - Wait For Event and Display Flip Flags Register 1

9	Display Plane C Syncronous Flip Display Pending				
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Format:</td><td style="padding: 2px;">Enable</td></tr> </table>	Format:	Enable		
Format:	Enable				
This field enables a wait for the duration of a Display Plane C Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).					
8	Display Sprite C Syncronous Flip Display Pending				
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Format:</td><td style="padding: 2px;">Enable</td></tr> </table>	Format:	Enable		
Format:	Enable				
This field enables a wait for the duration of a Display Sprite C Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.					
7	Reserved				
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Source:</td><td style="padding: 2px;">BlitterCS</td></tr> <tr> <td style="padding: 2px;">Format:</td><td style="padding: 2px;">MBZ</td></tr> </table>	Source:	BlitterCS	Format:	MBZ
Source:	BlitterCS				
Format:	MBZ				
7	Display Plane C Asynchronous Performance Flip Pending Wait Enable				
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Source:</td><td style="padding: 2px;">RenderCS</td></tr> <tr> <td style="padding: 2px;">Format:</td><td style="padding: 2px;">Enable</td></tr> </table>	Source:	RenderCS	Format:	Enable
Source:	RenderCS				
Format:	Enable				
This field enables a wait for the duration of a Display Plane C Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).					
6	Display Plane C Asynchronous Flip Pending Wait Enable				
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Format:</td><td style="padding: 2px;">Enable</td></tr> </table>	Format:	Enable		
Format:	Enable				
This field enables a wait for the duration of a Display Plane C "Flip Pending" condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).					
5	Display Plane C Syncronous Flip Pending Wait Enable				
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Format:</td><td style="padding: 2px;">Enable</td></tr> </table>	Format:	Enable		
Format:	Enable				
This field enables a wait for the duration of a Display Plane C Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).					

SYNC_FLIP_STATUS_1 - Wait For Event and Display Flip Flags Register 1

	4	Display Sprite C Syncronous Flip Pending Wait Enable		
		<table border="1" style="width: 100%;"> <tr> <td style="padding: 2px;">Format:</td> <td style="padding: 2px;">Enable</td> </tr> </table>	Format:	Enable
Format:	Enable			
<p>This field enables a wait for the duration of a Display Sprite C Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>				
	3	Reserved		
		<table border="1" style="width: 100%;"> <tr> <td style="padding: 2px;">Format:</td> <td style="padding: 2px;">MBZ</td> </tr> </table>	Format:	MBZ
Format:	MBZ			
<p></p>				
	2	Display Pipe C Scan Line Wait Enable		
		<table border="1" style="width: 100%;"> <tr> <td style="padding: 2px;">Format:</td> <td style="padding: 2px;">Enable</td> </tr> </table>	Format:	Enable
Format:	Enable			
<p>This field enables a wait while a Display Pipe C Scan Line condition exists. This condition is defined as the start of the scan line specified in the Pipe C Display Scan Line Count Range Compare Register. See Scan Line Event in the Device Programming Interface chapter of MI Functions.</p>				
	1	Display Pipe C Vertical Blank Wait Enable		
		<table border="1" style="width: 100%;"> <tr> <td style="padding: 2px;">Format:</td> <td style="padding: 2px;">Enable</td> </tr> </table>	Format:	Enable
Format:	Enable			
<p>This field enables a wait until the next Display Pipe C Vertical Blank event occurs. This event is defined as the start of the next Display Pipe C vertical blank period. Note that this can cause a wait for up to an entire refresh period. See Vertical Blank Event (See Programming Interface).</p>				
	0	Reserved		
		<table border="1" style="width: 100%;"> <tr> <td style="padding: 2px;">Project:</td> <td style="padding: 2px;">BDW</td> </tr> </table>	Project:	BDW
Project:	BDW			
		<table border="1" style="width: 100%;"> <tr> <td style="padding: 2px;">Format:</td> <td style="padding: 2px;">MBZ</td> </tr> </table>	Format:	MBZ
Format:	MBZ			

Wake Enable and Wake Status

WAKEEN_WAKESTS - Wake Enable and Wake Status										
Register Space: MMIO: 0/3/0 Project: BDW Default Value: 0x00000000 Access: R/W Size (in bits): 32										
Address: 0000Ch-0000Fh										
DWord	Bit	Description								
0	31:17	Reserved								
		Format:	MBZ							
	16	SDIWAKE								
		Default Value:	0b							
		Access:	R/WC							
Programming Notes										
Flag bits that indicate which SDI signal(s) received a "State Change" event. The bits are cleared by writing 1's to them. These bits are in the Suspend well and only cleared on a power-on reset. Software must not make assumptions about the reset state of these bits and must set them appropriately.										
15:1	Reserved									
	Format:	MBZ								
0	0	SDIWEN								
		<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th><th style="text-align: center;">Name</th><th style="text-align: center;">Description</th></tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td><td>Disable [Default]</td><td>SDI is disabled</td></tr> <tr> <td style="text-align: center;">1b</td><td>Enable</td><td>SDI is enabled to generate wake event.</td></tr> </tbody> </table>		Value	Name	Description	0b	Disable [Default]	SDI is disabled	1b
Value	Name	Description								
0b	Disable [Default]	SDI is disabled								
1b	Enable	SDI is enabled to generate wake event.								
Programming Notes										
Bits which control which SDI signal(s) may generate a wake event. A '1' bit in the bit mask indicates that the associated SDIN signal is enabled to generate a wake. These bits are in the Suspend well and only cleared on a power-on reset. Software must not make assumptions about the reset state of these bits and must set them appropriately.										

Walkers Fault Register

WF_REG - Walkers Fault Register								
DWord	Bit	Description						
0	31:1	Walkers Fault Register <table border="1"> <tr> <td>Default Value:</td><td>00000000000000000000000000000000b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> <tr> <td colspan="2">All bits are only valid with bit[0]=1.</td></tr> </table>	Default Value:	00000000000000000000000000000000b	Access:	R/W	All bits are only valid with bit[0]=1.	
Default Value:	00000000000000000000000000000000b							
Access:	R/W							
All bits are only valid with bit[0]=1.								
	0	Valid Bit <table border="1"> <tr> <td>Default Value:</td><td>0b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> <tr> <td colspan="2">This bit indicates that the first fault for this engine has been recorded. It can only be cleared by SW, which also clears the other fields.</td></tr> </table>	Default Value:	0b	Access:	R/W	This bit indicates that the first fault for this engine has been recorded. It can only be cleared by SW, which also clears the other fields.	
Default Value:	0b							
Access:	R/W							
This bit indicates that the first fault for this engine has been recorded. It can only be cleared by SW, which also clears the other fields.								

Wall Clock Counter

WALCLK - Wall Clock Counter				
DWord	Bit	Description		
0	31:0	<p>Wall Clock Counter</p> <table border="1"> <tr> <td>Default Value:</td> <td>0h</td> </tr> </table> <p>Wall Clock Counter (Counter): 32 bit counter that is incremented on each link BCLK (24MHz) period and rolls over from FFFF_FFFFh to 0000_0000h. This counter will roll over to zero with a period of approximately 179 seconds. This counter is enabled when the controller is out of reset (CRST is 1). Software uses this counter to synchronize between multiple controllers. Will be reset on controller reset.</p>	Default Value:	0h
Default Value:	0h			

Wall Clock Counter Alias

WALCLKA - Wall Clock CounterAlias						
DWord	Bit	Description				
0	31:0	<p>COUNTERA This is an alias of the WALCK register. 32 bit counter that is incremented on each link BCLK period and rolls over from FFFF_FFFFh to 0000_0000h. This counter will roll over to zero with a period of approximately 179 seconds.</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <th colspan="2">Programming Notes</th> </tr> <tr> <td colspan="2">This counter is enabled while the BCLK bit is set to 1. Software uses this counter to synchronize between multiple controllers. Will be reset on controller reset.</td> </tr> </table>	Programming Notes		This counter is enabled while the BCLK bit is set to 1. Software uses this counter to synchronize between multiple controllers. Will be reset on controller reset.	
Programming Notes						
This counter is enabled while the BCLK bit is set to 1. Software uses this counter to synchronize between multiple controllers. Will be reset on controller reset.						

WD_IIR

WD_IIR							
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x00000000 Access: R/WC Size (in bits): 32							
Address: 6E564h-6E567h Name: WDO Interrupt Identity ShortName: WD_IIR_0 Valid Projects: BDW Power: off/on Reset: soft							
See the WD interrupt bit definition to find the source event for each interrupt bit.							
DWord	Bit	Description					
0	31:8	Reserved Format: MBZ					
	7:0	Interrupt Identity Bits This field holds the persistent values of the WD interrupt bits which are unmasked by the WD_IMR. Bits set in this register will propagate to the WD interrupt in the Display Engine Miscellaneous Interrupts. Bits set in this register will remain set (persist) until the interrupt condition is cleared by writing a '1' to the appropriate bits. <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Condition Not Detected</td></tr> <tr> <td>1b</td><td>Condition Detected</td></tr> </tbody> </table>	Value	Name	0b	Condition Not Detected	1b
Value	Name						
0b	Condition Not Detected						
1b	Condition Detected						

WD_IMR

WD_IMR									
Register Space:	MMIO: 0/2/0								
Project:	BDW								
Default Value:	0x000000FF								
Access:	R/W								
Size (in bits):	32								
Address:	6E560h-6E563h								
Name:	WD0 Interrupt Mask								
ShortName:	WD_IMR_0								
Valid Projects:	BDW								
Power:	off/on								
Reset:	soft								
See the WD interrupt bit definition to find the source event for each interrupt bit.									
DWord	Bit	Description							
0	31:8	Reserved Format: MBZ							
	7:0	Interrupt Mask Bits This field contains a bit mask which selects which WD events are reported in the WD_IIR. <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="background-color: #e0e0ff; width: 50%;">Value</th><th style="background-color: #e0e0ff; width: 50%;">Name</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Not Masked</td></tr> <tr> <td>1b</td><td>Masked</td></tr> <tr> <td>000000FFh</td><td>All interrupts masked [Default]</td></tr> </tbody> </table>	Value	Name	0b	Not Masked	1b	Masked	000000FFh
Value	Name								
0b	Not Masked								
1b	Masked								
000000FFh	All interrupts masked [Default]								

WD_PERF_CNT

WD_PERF_CNT		
DWord	Bit	Description
0	31:24	Reserved
		Format: MBZ
	23:0	WD Perf Cnt This field increments every millisecond while capturing. It does not count the time after capture is completed and waiting for the next capsync. Writes to this register will set the count to the written value, then it will increment from that value onwards.

WD_QUICKCAP_CTRL

WD_QUICKCAP_CTRL														
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0xC0000000 Access: R/W Size (in bits): 32														
Address: 6E540h-6E543h Name: WD0 Quick Capture Control ShortName: WD_QUICKCAP_CTRL_0 Valid Projects: BDW Power: off/on Reset: soft														
Some of the WD Quickcap masking is controlled here and some in the PIPE_MISC register.														
Programming Notes														
To use FBC modification tracking for idleness calculations when FBC is disabled, program FBC_CTL CPU Fence Enable bit 28, FBC_CONTROL_SA_REGISTER, FBC_CPU_FENCE_OFFSET_REGISTER, FBC_RT_BASE_ADDR_REGISTER, and BLITTER_TRACKING_REGISTER as they are programmed when FBC is enabled.														
DWord	Bit	Description												
0	31:30	WD Quickcap Override This field overrides the WD quick capture entry and exit. <table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>00b,01b</td><td>No Override</td><td>Do not override. Use regular entry and exit conditions.</td></tr> <tr> <td>10b</td><td>Override Entry</td><td>Override to force entry</td></tr> <tr> <td>11b</td><td>Override Standby [Default]</td><td>Override to force exit</td></tr> </tbody> </table> <p>Restriction</p> <p>Quickcap is only supported on pipe A. Keep this field set to the default value when using WD on other pipes.</p>	Value	Name	Description	00b,01b	No Override	Do not override. Use regular entry and exit conditions.	10b	Override Entry	Override to force entry	11b	Override Standby [Default]	Override to force exit
Value	Name	Description												
00b,01b	No Override	Do not override. Use regular entry and exit conditions.												
10b	Override Entry	Override to force entry												
11b	Override Standby [Default]	Override to force exit												
Reserved <table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ												
Format:	MBZ													

WD_QUICKCAP_CTRL

	28	WD Mask Max Sleep This field controls the mask for the max quick capture frames event.									
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Not Masked</td><td>Not Masked - will be considered in idleness tracking</td></tr> <tr> <td>1b</td><td>Masked</td><td>Masked - will not be considered in idleness tracking</td></tr> </tbody> </table>	Value	Name	Description	0b	Not Masked	Not Masked - will be considered in idleness tracking	1b	Masked	Masked - will not be considered in idleness tracking
Value	Name	Description									
0b	Not Masked	Not Masked - will be considered in idleness tracking									
1b	Masked	Masked - will not be considered in idleness tracking									
	27:25	Reserved									
		Format: MBZ									
	24	WD Mask FBC Modify This field controls the mask for the FBC front buffer modify event.									
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Not Masked</td><td>Not Masked - will be considered in idleness tracking</td></tr> <tr> <td>1b</td><td>Masked</td><td>Masked - will not be considered in idleness tracking</td></tr> </tbody> </table>	Value	Name	Description	0b	Not Masked	Not Masked - will be considered in idleness tracking	1b	Masked	Masked - will not be considered in idleness tracking
Value	Name	Description									
0b	Not Masked	Not Masked - will be considered in idleness tracking									
1b	Masked	Masked - will not be considered in idleness tracking									
	23:18	Reserved									
		Format: MBZ									
	17	WD Mask KVMR Session En This field controls the mask for the KVMR session enabled event.									
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Not Masked</td><td>Not Masked - will be considered in idleness tracking</td></tr> <tr> <td>1b</td><td>Masked</td><td>Masked - will not be considered in idleness tracking</td></tr> </tbody> </table>	Value	Name	Description	0b	Not Masked	Not Masked - will be considered in idleness tracking	1b	Masked	Masked - will not be considered in idleness tracking
Value	Name	Description									
0b	Not Masked	Not Masked - will be considered in idleness tracking									
1b	Masked	Masked - will not be considered in idleness tracking									
	16	WD Mask Reg Write This field controls the mask for the register write event.									
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Not Masked</td><td>Not Masked - will be considered in idleness tracking</td></tr> <tr> <td>1b</td><td>Masked</td><td>Masked - will not be considered in idleness tracking</td></tr> </tbody> </table>	Value	Name	Description	0b	Not Masked	Not Masked - will be considered in idleness tracking	1b	Masked	Masked - will not be considered in idleness tracking
Value	Name	Description									
0b	Not Masked	Not Masked - will be considered in idleness tracking									
1b	Masked	Masked - will not be considered in idleness tracking									
	15:2	Reserved									
		Format: MBZ									
	1	WD Quickcap Entry Completion Access: R/WC This is a sticky bit which is set on WD quickcap entry completion. Clear this bit by writing a 1b to it.									
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Not complete</td><td>Entry not complete</td></tr> <tr> <td>1b</td><td>Complete</td><td>Entry complete</td></tr> </tbody> </table>	Value	Name	Description	0b	Not complete	Entry not complete	1b	Complete	Entry complete
Value	Name	Description									
0b	Not complete	Entry not complete									
1b	Complete	Entry complete									
	0	Reserved									
		Format: MBZ									

WD_STATUS

WD_STATUS				
DWord	Bit	Description		
0	31:16	<p>WD_Capsync Count</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>The value in this register represents the live status of the capsync counter.</p>	Access:	RO
Access:	RO			
	15:8	<p>WD_Laterun Frame Count</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>The value in this register represents the number of frames WD has dropped due to late run. The count will increment at each capture sync when late run is detected. After reaching the maximum count value the counter will rollover and continue from 0. A register write will reset the counter.</p>	Access:	RO
Access:	RO			
	7:0	<p>Quickcap Frame Counter</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>This field provides the live status of the quick capture frame counter.</p>	Access:	RO
Access:	RO			

WD_STRIDE

WD_STRIDE				
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x00000000 Access: Double Buffered Size (in bits): 32 Double Buffer Update Point: Start of capture sync or transcoder not enabled				
Address: 6E510h-6E513h Name: WDO Stride ShortName: WD_STRIDE_0 Valid Projects: BDW Power: off/on Reset: soft				
DWord	Bit	Description		
0	31:16	Reserved <table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ
Format:	MBZ			
15:6	WD Stride This field specifies the stride bits 15:6. This value is used to determine the line to line increment for the capture data writes. This field is programmed in units of 64 bytes. <table border="1"> <tr> <th>Restriction</th></tr> <tr> <td>The stride is limited to a maximum of 32K bytes.</td></tr> </table>	Restriction	The stride is limited to a maximum of 32K bytes.	
Restriction				
The stride is limited to a maximum of 32K bytes.				
5:0	Reserved <table border="1"> <tr> <td>Format:</td><td>MBZ</td></tr> </table>	Format:	MBZ	
Format:	MBZ			

WD_SURF

WD_SURF							
Register Space:	MMIO: 0/2/0						
Project:	BDW						
Default Value:	0x00000000						
Access:	Double Buffered						
Size (in bits):	32						
Double Buffer Update Point:		Start of capture sync or transcoder not enabled					
Address:	6E514h-6E517h						
Name:	WD0 Surface Base Address						
ShortName:	WD_SURF_0						
Valid Projects:	BDW						
Power:	off/on						
Reset:	soft						
Writes to this register arm WD registers.							
DWord	Bit	Description					
0	31:12	WD Surface Base Address					
		Format:	GraphicsAddress[31:12]				
		This address specifies the surface base address bits 31:12. It is mapped to physical pages through the global GTT.					
		<table border="1"> <thead> <tr> <th>Restriction</th><th>Project</th></tr> </thead> <tbody> <tr> <td>It must be at least 4KB aligned. It must use linear memory.</td><td></td></tr> <tr> <td>The mapped pages must be located in graphics data stolen memory.</td><td>BDW</td></tr> </tbody> </table>		Restriction	Project	It must be at least 4KB aligned. It must use linear memory.	
Restriction	Project						
It must be at least 4KB aligned. It must use linear memory.							
The mapped pages must be located in graphics data stolen memory.	BDW						
11:0	Reserved						
	Format:	MBZ					

WD_TAIL_CFG

WD_TAIL_CFG			
Register Space:	MMIO: 0/2/0		
Project:	BDW		
Default Value:	0x00000010		
Access:	Double Buffered		
Size (in bits):	32		
Double Buffer Update Point:	Start of capture sync or transcoder not enabled; after armed		
Double Buffer Armed Write to WD_SURF or WD not enabled By:			
Address:	6E520h-6E523h		
Name:	WD0 Tail Pointer Config		
ShortName:	WD_TAIL_CFG_0		
Valid Projects:	BDW		
Power:	off/on		
Reset:	soft		
DWord	Bit	Description	
0	31:28	Reserved	Format: MBZ
	27:16	Tail Initial Update Delay This field specifies the minimum number of scan lines that WD capture must wait for at the beginning of each frame before any tail pointer updates will be sent.	
	15:12	Reserved	Format: MBZ
	11:4	Tail Update Period Default Value: 01h 16 lines This field specifies the number of scan lines that the WD capture will write back to memory before sending each tail pointer message. This field is programmed in multiples of 16 scan lines.	
		Restriction	
		A value of 0 is not valid.	
	3:0	Reserved	Format: MBZ

WD_WNIC_MSG_ADDR

WD_WNIC_MSG_ADDR						
Register Space: MMIO: 0/2/0 Project: BDW Access: R/W Size (in bits): 64						
Address: 6E530h-6E537h Name: WDO WNIC Message Address ShortName: WD_WNIC_MSG_ADDR_0_* Valid Projects: BDW Power: off/on Reset: soft						
DWord	Bit	Description				
0 0x6E530	31:0	WD WNIC MSG Address This register specifies address bits 31:0 for the Display to WNIC messages. <div style="background-color: #e0e0ff; padding: 2px;"> Restriction </div> The address must be DWord aligned.				
1 0x6E534	31:0	Reserved <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Project:</td><td style="padding: 2px;">BDW</td></tr> <tr> <td style="padding: 2px;">Format:</td><td style="padding: 2px;">MBZ</td></tr> </table>	Project:	BDW	Format:	MBZ
Project:	BDW					
Format:	MBZ					

WGBOX State Arbitration Priority Control

APC - WGBOX State Arbitration Priority Control			
DWord	Bit	Description	
0	31:9	Reserved Format:	MBZ

WGBOX Video CSR 8

WG_CNTX_FRAME_BYTEOFFSET - WGBOX Video CSR 8			
Register Space:	MMIO: 0/2/0	Bit	Description
Default Value:	0x00000000		
Access:	R/W		
Size (in bits):	32		
DWord	0	31:0	FrameSize
This field indicates the current frame Start Byte offset. This field is updated at the end of a frame			

WGBOX Video CSR 99

WG_CNTX_SVRSTR_REG_99 - WGBOXVideoCSR99

Register Space: MMIO: 0/2/0

Default Value: 0x00000000

Access: R/W

Size (in bits): 32

DWord	Bit	Description
0	31:0	Scratch data

WIDI LRA 0

WIDI_LRA_0 - WIDI LRA 0						
DWord	Bit	Description				
0	31:30	Reserved <table border="1"> <tr> <td>Default Value:</td> <td>00b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Default Value:	00b	Access:	RO
Default Value:	00b					
Access:	RO					
29:24	WIDI LRA1 Max <table border="1"> <tr> <td>Default Value:</td> <td>110111b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Maximum value of programmable LRA1.</p>	Default Value:	110111b	Access:	R/W	
Default Value:	110111b					
Access:	R/W					
23:22	Reserved <table border="1"> <tr> <td>Default Value:</td> <td>00b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Default Value:	00b	Access:	RO	
Default Value:	00b					
Access:	RO					
21:16	WIDI LRA1 Min <table border="1"> <tr> <td>Default Value:</td> <td>100000b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Minimum value of programmable LRA1.</p>	Default Value:	100000b	Access:	R/W	
Default Value:	100000b					
Access:	R/W					
15:14	Reserved <table border="1"> <tr> <td>Default Value:</td> <td>00b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Default Value:	00b	Access:	RO	
Default Value:	00b					
Access:	RO					
13:8	WIDI LRA0 Max <table border="1"> <tr> <td>Default Value:</td> <td>011111b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Maximum value of programmable LRA0.</p>	Default Value:	011111b	Access:	R/W	
Default Value:	011111b					
Access:	R/W					
7:6	Reserved <table border="1"> <tr> <td>Default Value:</td> <td>00b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Default Value:	00b	Access:	RO	
Default Value:	00b					
Access:	RO					
5:0	WIDILRA0 Min <table border="1"> <tr> <td>Default Value:</td> <td>000000b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>Minimum value of programmable LRA0.</p>	Default Value:	000000b	Access:	R/W	
Default Value:	000000b					
Access:	R/W					

WIDI LRA 1

WIDI_LRA_1 - WIDI LRA 1						
DWord	Bit	Description				
0	31:30	Reserved <table border="1"> <tr> <td>Default Value:</td><td>00b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	00b	Access:	RO
Default Value:	00b					
Access:	RO					
29:28	VMX <table border="1"> <tr> <td>Default Value:</td><td>00b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Which LRA should VMX use.</p>	Default Value:	00b	Access:	R/W	
Default Value:	00b					
Access:	R/W					
27:26	BSP <table border="1"> <tr> <td>Default Value:</td><td>00b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Which LRA should BSP use.</p>	Default Value:	00b	Access:	R/W	
Default Value:	00b					
Access:	R/W					
25:24	IME <table border="1"> <tr> <td>Default Value:</td><td>01b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Which LRA should IME/WRS use.</p>	Default Value:	01b	Access:	R/W	
Default Value:	01b					
Access:	R/W					
23:14	Reserved <table border="1"> <tr> <td>Default Value:</td><td>0000000000b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	0000000000b	Access:	RO	
Default Value:	0000000000b					
Access:	RO					
13:8	Reserved					
7:6	Reserved <table border="1"> <tr> <td>Default Value:</td><td>00b</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	00b	Access:	RO	
Default Value:	00b					
Access:	RO					
5:0	Reserved					

WIDI TLB Control Register

WTCR - WIDI TLB Control Register						
DWord	Bit	Description				
0	31:1	<p>Reserved</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000000000000000000000000000b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Default Value:	00000000000000000000000000000000b	Access:	RO
Default Value:	00000000000000000000000000000000b					
Access:	RO					
	0	<p>Invalidate TLBs on the corresponding Engine</p> <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>SW writes 1 to invalidate the TLBs for the associated engine and HW clears the bit when invalidation is complete. To ensure proper invalidation of the TLBs, SW has to ensure the corresponding engine's HW pipeline is flushed and cleared from all its memory accesses. Otherwise HW cannot guarantee the proper invalidation for TLBs.</p> <p>This bit is self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					

WM_LINETIME

WM_LINETIME					
Register Space:	MMIO: 0/2/0				
Project:	BDW				
Default Value:	0x00000000				
Access:	R/W				
Size (in bits):	32				
Address:	45270h-45273h				
Name:	Pipe A Watermark Line Time				
ShortName:	WM_LINETIME_A				
Valid Projects:	BDW				
Power:	Always on				
Reset:	soft				
Address:	45274h-45277h				
Name:	Pipe B Watermark Line Time				
ShortName:	WM_LINETIME_B				
Valid Projects:	BDW				
Power:	Always on				
Reset:	soft				
Address:	45278h-4527Bh				
Name:	Pipe C Watermark Line Time				
ShortName:	WM_LINETIME_C				
Valid Projects:	BDW				
Power:	Always on				
Reset:	soft				
There is one instance of this register format per each pipe A, B, C.					
DWord	Bit	Description			
0	31:25	Reserved			
	24:16	IPS Line Time			
		<table border="1"> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td colspan="2">This field specifies the IPS line time for the current screen resolution in units of 0.125us. This value needs to be programmed before enabling IPS. IPS line time in microseconds = Pipe horizontal total number of pixels / CD clock frequency in MHz. Multiply by 8 to get units of 0.125us and round to nearest integer. This field only needs to be programmed for pipes that will have IPS enabled on them.</td></tr> </table>	Project:	BDW	This field specifies the IPS line time for the current screen resolution in units of 0.125us. This value needs to be programmed before enabling IPS. IPS line time in microseconds = Pipe horizontal total number of pixels / CD clock frequency in MHz. Multiply by 8 to get units of 0.125us and round to nearest integer. This field only needs to be programmed for pipes that will have IPS enabled on them.
Project:	BDW				
This field specifies the IPS line time for the current screen resolution in units of 0.125us. This value needs to be programmed before enabling IPS. IPS line time in microseconds = Pipe horizontal total number of pixels / CD clock frequency in MHz. Multiply by 8 to get units of 0.125us and round to nearest integer. This field only needs to be programmed for pipes that will have IPS enabled on them.					
15:9	Reserved				

WM_LINETIME	
8:0	<p>Line Time This field specifies the line time for the current screen resolution in units of 0.125us.</p> <p>Programming Notes</p> <p>Line time in microseconds = Pipe horizontal total number of pixels / pixel rate in MHz. Multiply by 8 to get units of 0.125us and round to nearest integer. Program the smallest line time when using multiple refresh rates.</p> <p>Restriction</p> <p>The line time value must be programmed before enabling any display low power watermark. Maximum supported line time is 63.875us (11111111b).</p>

WM_LP

WM_LP						
Register Space:	MMIO: 0/2/0					
Project:	BDW					
Default Value:	0x00000000					
Access:	R/W					
Size (in bits):	32					
Address:	45108h-4510Bh					
Name:	Low Power 1 Watermarks					
ShortName:	WM_LP1					
Power:	Always on					
Reset:	soft					
Address:	4510Ch-4510Fh					
Name:	Low Power 2 Watermarks					
ShortName:	WM_LP2					
Power:	Always on					
Reset:	soft					
Address:	45110h-45113h					
Name:	Low Power 3 Watermarks					
ShortName:	WM_LP3					
Power:	Always on					
Reset:	soft					
These are Low Power watermark values which will be used when display is in a LP state. There is one instance of this register format per each LP level 1,2,3.						
DWord	Bit	Description				
0	31	Enabled Enables this LP watermark. This bit allows the associated LP state to be used.				
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>1b</td><td>Enable</td></tr> <tr> <td>0b</td><td>Disable</td></tr> </tbody> </table>	Value	Name	1b	Enable
Value	Name					
1b	Enable					
0b	Disable					
	30:24	Restriction The watermark line time registers for all enabled pipes must be programmed with the correct values prior to enabling.				
		Latency This field contains two times the integer value of the name of the latency level associated with this LP watermark. Example: 0000100b = level 2.				

WM_LP		
	23:19	FBC LP Watermark Number of equivalent lines of the primary display for this watermark.
	18:8	LP Primary Watermark Number in 64Bs of data in the display data buffer below which the Primary Plane stream will wake memory.
	7:0	LP Cursor Watermark Number in 64Bs of data in the display data buffer below which the Cursor Plane stream will wake memory.

WM_LP_SPR

WM_LP_SPR		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	45120h-45123h	
Name:	Low Power 1 Sprite Watermarks	
ShortName:	WM_LP1_SPR	
Power:	Always on	
Reset:	soft	
Address:	45124h-45127h	
Name:	Low Power 2 Sprite Watermarks	
ShortName:	WM_LP2_SPR	
Power:	Always on	
Reset:	soft	
Address:	45128h-4512Bh	
Name:	Low Power 3 Sprite Watermarks	
ShortName:	WM_LP3_SPR	
Power:	Always on	
Reset:	soft	
This is the Low Power Sprite watermark value which will be used when display is in a LP state. There is one instance of this register format per each LP level 1,2,3.		
DWord	Bit	Description
0	31:11	Reserved
	10:0	LP Sprite Watermark Number in 64Bs of data in the display data buffer below which the Sprite Plane stream will wake memory.

WM_MISC

WM_MISC													
DWord	Bit	Description											
0	31:20	Reserved <table> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Format:</td> <td>PBC</td> </tr> </table>	Project:	BDW	Format:	PBC							
Project:	BDW												
Format:	PBC												
	19:4	Reserved <table> <tr> <td>Project:</td> <td>BDW</td> </tr> </table>	Project:	BDW									
Project:	BDW												
	3	Reserved <table> <tr> <td>Project:</td> <td>BDW</td> </tr> </table>	Project:	BDW									
Project:	BDW												
	2	Reserved <table> <tr> <td>Project:</td> <td>BDW</td> </tr> <tr> <td>Format:</td> <td>PBC</td> </tr> </table>	Project:	BDW	Format:	PBC							
Project:	BDW												
Format:	PBC												
	1	Reserved <table> <tr> <td>Project:</td> <td>BDW</td> </tr> </table>	Project:	BDW									
Project:	BDW												
	0	Data Buffer Partitioning <table> <tr> <td>Project:</td> <td>BDW</td> </tr> </table> <p>This bit controls the data buffer partitioning when between sprite and primary during low power states.</p> <table> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>1/2</td> <td>Sprite has 1/2 and primary has 1/2 of the buffer</td> </tr> <tr> <td>1b</td> <td>5/6</td> <td>Sprite has 5/6 and primary has 1/6 of the buffer</td> </tr> </tbody> </table> <p>Restriction</p> <p>The 5/6 setting is for use only when Frame Buffer Compression is enabled on the primary plane, or when the primary plane is disabled.</p>	Project:	BDW	Value	Name	Description	0b	1/2	Sprite has 1/2 and primary has 1/2 of the buffer	1b	5/6	Sprite has 5/6 and primary has 1/6 of the buffer
Project:	BDW												
Value	Name	Description											
0b	1/2	Sprite has 1/2 and primary has 1/2 of the buffer											
1b	5/6	Sprite has 5/6 and primary has 1/6 of the buffer											

WM_PIPE

WM_PIPE		
Register Space:	MMIO: 0/2/0	
Project:	BDW	
Default Value:	0x00787838	
Access:	R/W	
Size (in bits):	32	
Address:	45100h-45103h	
Name:	Pipe A Watermarks	
ShortName:	WM_PIPE_A	
Power:	Always on	
Reset:	soft	
Address:	45104h-45107h	
Name:	Pipe B Watermarks	
ShortName:	WM_PIPE_B	
Power:	Always on	
Reset:	soft	
Address:	45200h-45203h	
Name:	Pipe C Watermarks	
ShortName:	WM_PIPE_C	
Power:	Always on	
Reset:	soft	
These are the watermark values which are used for requesting data. There is one instance of this register format per each pipe A/B/C.		
DWord	Bit	Description
0	31:24	Reserved
	23:16	Pipe Primary Watermark
		Default Value: 01111000b
		Number in 64Bs of data in FIFO below which the Pipe Primary Plane stream will generate requests to memory
	15:8	Pipe Sprite Watermark
	Default Value: 01111000b	
	Number in 64Bs of data in FIFO below which the Pipe Sprite Plane stream will generate requests to memory	
7:6	Reserved	

WM_PIPE					
	5:0				
	Pipe Cursor Watermark				
<table border="1"><tr><td>Default Value:</td><td>111000b</td></tr><tr><td colspan="2">Number in 64Bs of data in FIFO below which the Pipe Cursor Plane stream will generate requests to memory</td></tr></table>		Default Value:	111000b	Number in 64Bs of data in FIFO below which the Pipe Cursor Plane stream will generate requests to memory	
Default Value:	111000b				
Number in 64Bs of data in FIFO below which the Pipe Cursor Plane stream will generate requests to memory					

WRID_VALID_REG0

WRID_VALID_REG0 - WRID_VALID_REG0						
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x00000000 Size (in bits): 32						
Address: 04070h						
DWord	Bit	Description				
0	31:0	<p>WRID_VALID_REG0</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>This register is for WRID Comparison usage. RO register with IA Access Type on DEV reset. wrdp_wrid_valid_vector[31:0] There are 96 write buffer. Each bit indicate the buffer is valid if set. Divide into 3 registers to accommodate all 96 deep</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

WRID_VALID_REG1

WRID_VALID_REG1 - WRID_VALID_REG1						
DWord	Bit	Description				
0	31:0	<p>WRID_VALID_REG1</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>This register is for WRID Comparison usage. RO register with IA Access Type on DEV reset. wrdp_wrid_valid_vector[63:32] There are 96 write buffer. Each bit indicate the buffer is valid if set. Divide into 3 registers to accommodate all 96 deep.</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

WRID_VALID_REG2

WRID_VALID_REG2 - WRID_VALID_REG2						
Register Space: MMIO: 0/2/0 Project: BDW Default Value: 0x00000000 Size (in bits): 32						
Address: 04078h						
DWord	Bit	Description				
0	31:0	<p>WRID_VALID_REG2</p> <table border="1"> <tr> <td>Default Value:</td><td>00000000h</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table> <p>This register is for WRID Comparison usage. RO register with IA Access Type on DEV reset. wrdp_wrid_valid_vector[95:64] There are 96 write buffer. Each bit indicate the buffer is valid if set. Divide into 3 registers to accommodate all 96 deep.</p>	Default Value:	00000000h	Access:	RO
Default Value:	00000000h					
Access:	RO					

Write Watermark

WR_WATERMARK - Write Watermark			
DWord	Bit	Description	
0	31:20	Extra Bits	
		Default Value:	000000000000b
		Access:	R/W
	19	Watermark Timeout Enable	
		Default Value:	1b
		Access:	R/W
	18:8	Watermark Timeout	
		Default Value:	1111111110b
		Access:	R/W
		Number of clocks that the write pipe queue is allowed to keep a ready write cycle, without reads or writes to the queue. Once this value is met, and if the feature is enabled, the watermark is considered reached, and all pending write requests are issued.	
	7	Watermark Enable	
		Default Value:	1b
		Access:	R/W
		Enable Write Request Grouping	
	6:0	High Watermark	
		Default Value:	0100100b
		Access:	R/W
		This is the number of write requests to be collected before initiating a write burst. Once a burst is initiated, it continues until all the available writes are requested.	

WRPLL_CTL

WRPLL_CTL								
Register Space:	MMIO: 0/2/0							
Project:	BDW	0x00202418 [BDW]						
Access:	R/W							
Size (in bits):	32							
Address:	46040h-46043h							
Name:	WRPLL 1 Control							
ShortName:	WRPLL_CTL1							
Valid Projects:	BDW							
Power:	Always on							
Reset:	soft							
Address:	46060h-46063h							
Name:	WRPLL 2 Control							
ShortName:	WRPLL_CTL2							
Valid Projects:	BDW							
Power:	Always on							
Reset:	soft							
Programming Notes								
<p>The WR PLL can drive the DDI ports at programmable frequencies for HDMI, DVI, DisplayPort, and FDI. There are two instances of this register format to support the two WR PLLs. The dividers must be programmed depending on the frequency of the selected reference. The divider programming algorithm is supplied separately.</p> <p>The following formula is for reference only. Always follow the divider programming algorithm to achieve the best quality.</p> <p>PLL Frequency = (Reference Frequency / Reference Divider) * (Feedback Divider / Post Divider)</p> <p>TMDS rate or symbol clock frequency = PLL frequency / 5</p> <p>Link rate or bit clock frequency = PLL frequency * 2</p>								
DWord	Bit	Description						
0	31	<p>PLL Enable This bit will enable or disable the PLL.</p> <table border="1"> <thead> <tr> <th>Value</th><th>Name</th></tr> </thead> <tbody> <tr> <td>0b</td><td>Disable</td></tr> <tr> <td>1b</td><td>Enable</td></tr> </tbody> </table> <p>Restriction This field must not be changed while any port is using this PLL.</p>	Value	Name	0b	Disable	1b	Enable
Value	Name							
0b	Disable							
1b	Enable							

WRPLL_CTL															
	30	Reserved													
		Format:	MBZ												
	29:28	Reference Select													
		Project:	BDW												
		Select between PLL references.													
		<table border="1"> <thead> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>01b</td><td>PCH SSC</td><td>PCH Spread reference</td></tr> <tr> <td>10b</td><td>Muxed SSC</td><td>CPU internal SSC when CPU Internal SSC is fused enabled, else the PCH SSC reference.</td></tr> <tr> <td>11b</td><td>LCPLL 2700</td><td>LCPLL 2700MHz output</td></tr> </tbody> </table>		Value	Name	Description	01b	PCH SSC	PCH Spread reference	10b	Muxed SSC	CPU internal SSC when CPU Internal SSC is fused enabled, else the PCH SSC reference.	11b	LCPLL 2700	LCPLL 2700MHz output
Value	Name	Description													
01b	PCH SSC	PCH Spread reference													
10b	Muxed SSC	CPU internal SSC when CPU Internal SSC is fused enabled, else the PCH SSC reference.													
11b	LCPLL 2700	LCPLL 2700MHz output													
		Programming Notes													
		Muxed SSC is recommended for DisplayPort. PCH SSC is required for FDI or HDMI and DVI clock bending. LCPLL 2700 MHz output is recommended for HDMI and DVI without clock bending.													
		Restriction													
		This field must not be changed while this PLL is enabled.													
	27:24	Reserved													
		Format:	MBZ												
	23:16	Feedback Divider													
		Default Value:	20h 32												
		Project:	BDW												
		This field selects the feedback divider (VCO divider) value for the desired output frequency. Also called the N value. This is in a 7.1 format where the upper 7 bits represent the integer value and the lowest bit represents the fractional value.													
		Restriction													
		This must not be changed while this PLL is enabled.													
	15:14	Reserved													
		Format:	MBZ												
	13:8	Post Divider													
		Default Value:	24h 36												
		Project:	BDW												
		This field selects the post divider value for the desired output frequency. Also called the P value.													
		Restriction													
		This must not be changed while this PLL is enabled.													

WRPLL_CTL	
	7:0
	Reference Divider
	Default Value:
	18h 24
	Project:
	BDW
<p>This field selects the reference divider value for the desired output frequency. Also called the R value. This is in a 7.1 format where the upper 7 bits represent the integer value and the lowest bit represents the fractional value.</p>	
Restriction	
<p>This must not be changed while this PLL is enabled.</p>	

ZTLB LRA 0

ZTLB_LRA_0 - ZTLB LRA 0								
DWord	Bit	Description						
0	31:29	Reserved <table border="1"> <tr> <td>Default Value:</td><td>000b</td></tr> <tr> <td>Project:</td><td>BDW</td></tr> <tr> <td>Access:</td><td>RO</td></tr> </table>	Default Value:	000b	Project:	BDW	Access:	RO
Default Value:	000b							
Project:	BDW							
Access:	RO							
28:27	STC LRA <table border="1"> <tr> <td>Default Value:</td><td>00b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Which LRA should STC use.</p>	Default Value:	00b	Access:	R/W			
Default Value:	00b							
Access:	R/W							
26:18	ZTLB LRA1 Min <table border="1"> <tr> <td>Default Value:</td><td>010000000b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Minimum value of programmable LRA1.</p>	Default Value:	010000000b	Access:	R/W			
Default Value:	010000000b							
Access:	R/W							
17:9	ZTLB LRA0 Max <table border="1"> <tr> <td>Default Value:</td><td>00111111b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Maximum value of programmable LRA0.</p>	Default Value:	00111111b	Access:	R/W			
Default Value:	00111111b							
Access:	R/W							
8:0	ZTLB LRA0 Min <table border="1"> <tr> <td>Default Value:</td><td>000000000b</td></tr> <tr> <td>Access:</td><td>R/W</td></tr> </table> <p>Minimum value of programmable LRA0.</p>	Default Value:	000000000b	Access:	R/W			
Default Value:	000000000b							
Access:	R/W							

ZTLB LRA 1

ZTLB_LRA_1 - ZTLB LRA 1		
Register Space: MMIO: 0/2/0 Project: BDW 0x36FC0000 [NOVALIDPROJECTS] 0x36FE813F [BDW]		
Size (in bits): 32 Address: 04A34h		
DWord	Bit	Description
0	31	Reserved Default Value: 0b Access: RO
	30:29	HIZ LRA Default Value: 01b Access: R/W Which LRA should HIZ use.
	28:27	RCZ LRA Default Value: 10b Access: R/W Which LRA should RCZ use.
	26:18	ZTLB LRA2 Max Default Value: 110111111b Project: BDW, :GT2:B Access: R/W Maximum value of programmable LRA2.
	17:9	ZTLB LRA2 Min Default Value: 101000000b Access: R/W Minimum value of programmable LRA2.
	8:0	ZTLB LRA1 Max Default Value: 100111111b Access: R/W Maximum value of programmable LRA1.