AMD RS690 ASIC Family Register Reference Guide

Technical Reference Manual
Rev. 3.00o

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Chapter 1
Introduction

1.1   About this Manual

This document is intended for BIOS engineers designing BIOSes for systems based on AMD's RS690 family of chipsets. It describes the register reference information needed to ensure the proper functioning of the RS690 ASIC. Use this document in conjunction with the related *AMD RS690 ASIC Family Register Programming Requirements Guide*, and *AMD RS690 ASIC Family BIOS Developer's Guide*.

This document covers register reference information for the following RS690 ASIC variants. Unless specified otherwise, reference to the RS690 ASIC in this document applies to all of these variants, even when these variants are not specifically mentioned.

- Desktop:
    - RS690
    - RS690C

- Mobile:
    - RS690M
    - RS690MC
    - RS690T

- *Chapter 1* outlines the notations and conventions used throughout this manual.
- *Chapter 2* provides detailed descriptions of the registers.
- *Appendix A* provides several cross-referenced lists of the registers (sorted by register name and address).

Changes and additions from the previous release of this document are highlighted in red. Refer to *Appendix B: Revision History* at the end of this manual for a detailed revision history. The names of all of the index registers and data registers in this document (used for indirect access) are highlighted in purple. Refer to section *A.2: Index Registers Sorted By Name* for a complete list of all of the index and data registers.

1.2   Nomenclature and Conventions

1.2.1   Numeric Representations

- Hexadecimal numbers are appended with "h" whenever there is a risk of ambiguity. Other numbers are assumed to be in decimal.

- Registers (or fields) of identical function are sometimes indicated by a single expression in which the part of the signal name that differs is enclosed in [ ] brackets. For example, the eight Host Data registers — HOST_DATA0 through to HOST_DATA7 — are represented by the single expression HOST_DATA[7:0].

- Series of numbers appearing in similar addresses are sometimes enclosed in [ ] brackets. For example, PCIE_HDR_LOGO exists for PCI-E device 2 to 8, and the registers' addresses are expressed collectively as pcieConfig [2:8]\:0x11C.

1.2.2 Register Description

All registers in this document are described with the format of the sample table below. All offsets are in hexadecimal notation, while programmed bits are in either binomial or hexadecimal notation.

Table 1-1 Register Description Table Notation—Example

DST_HEIGHT_WIDTH_8 - W - 32 bits - [MMReg:0x158C]			
Field Name	**Bits**	**Default**	**Description**
DST_WIDTH *(mirror bits 7:0 of DST_WIDTH:DST_WIDTH)*	23:16	0x0	Destination Width Note: This is an initiator register. Y is incremented at end of blit. Write 15: 0 to E2_DST_X, Write 31: 16 to E2_DST_WIDTH, then signal blit_start. E2_DST_Y = E2_DEST_Y (+/-) E2_DST_HEIGHT as function of direction after blit is complete
DST_HEIGHT *(mirror bits 7:0 of DST_HEIGHT:DST_HEIGHT)*	31:24	0x0	Destination Height Write 15: 0 to E2_DST_Y, Write 31: 16 to E2_DST_HEIGHT
[W] (Reserved) 15: 0 DST_WIDTH 23: 16 Destination width: range 0 to 256 (ZERO extent)			

Register Information	Example
Register name	DST_HEIGHT_WIDTH_8

Read / Write capability
  R = Readable
  W = Writable
  RW = Readable and Writable
	W

Register size	32 bits
Register address(es)*	MMReg:0x158C
Field name	DST_WIDTH
Field position/size	23:16
Field default value	0x0
Field description	Destination....complete
Field mirror information	*(mirror bits 7:0 of DST_WIDTH:DST_WIDTH)*
Brief register description	[W] (Reserved) 15: 0 DST_WIDTH 23: 16 Destination width: range 0 to 256 (ZERO extent)
* Note: There maybe more than one address; the convention used is as follows: **[aperName:offset]** - single mapping, to one aperture/decode and one offset **[aperName1, aperName2, …, aperNameN:offset]** - multiple mappings to different apertures/decodes but same offset **[aperName:startOffset-endOffset]** - mapped to an offset range in the same aperture/decode	

Warning: Do not attempt to modify the values of registers or bit fields that are marked as "Reserved." Doing so may cause the system to behave in unexpected ways.

2.1 Northbridge Configuration Space Registers

NB_VENDOR_ID - R - 16 bits - nbconfig:0x0			
Field Name	**Bits**	**Default**	**Description**
VENDOR_ID	15:0	0x1002	Vendor ID. This 16-bit field identifies the manufacturer of the device: Advnced Micro Devices, Inc.

NB_DEVICE_ID - R - 16 bits - nbconfig:0x2			
Field Name	**Bits**	**Default**	**Description**
DEVICE_ID	15:0	0x7910	Device Identifier This 16-bit field is assigned by the device manufacturer and identifies the type of device. The current northbridge device ID assignment is 0x7910. The host bridge alternate device ID is 0x7911 which is selected by the e-fuse configuration bit.

NB_COMMAND - RW - 16 bits - nbconfig:0x4			
Field Name	**Bits**	**Default**	**Description**

IO_ACCESS_EN (R)	0	0x0	I/O Access Enable
			This bit is always 0 because the RS690 does not respond to I/O cycles on the PCI Bus.
			  0=Disable
			  1=Enable

MEM_ACCESS_EN	1	0x0	Memory Access Enable
			Controls whether PCI memory accesses to system memory are accepted.
			  0=Disable
			  1=Enable

BUS_MASTER_EN (R)	2	0x1	Bus Master Enable
			This bit is always set, indicating that the RS690 is allowed to act as a bus master on the PCI Bus.
			  0=Disable
			  1=Enable

SPECIAL_CYCLE_EN (R)	3	0x0	Special Cycle
			This bit is always 0 because the RS690 ignores PCI special cycles.
			  0=Disable
			  1=Enable

MEM_WRITE_INVALIDATE_EN (R)	4	0x0	Memory Write and Invalidate Enable
			This bit is always 0 because the RS690 does not generate memory write and invalidate commands.
			  0=Disable
			  1=Enable

PAL_SNOOP_EN (R)	5	0x0	VGA Palette Snoop Enable
			This bit is always 0 indicating that the RS690 does not snoop the VGA palette address range.
			  0=Disable
			  1=Enable

PARITY_ERROR_EN (R)	6	0x0	Parity Error Response
			This bit is always 0 because the RS690 does not report data parity errors.
			  0=Disable
			  1=Enable

Reserved0 (R)	7	0x0	This bit is reserved in PCI 2.3. It is hardwired to 0.
			  0=Disable
			  1=Enable

SERR_EN	8	0x0	System Error Enable
			Controls the assertion of SERR#.
			  0=Disable
			  1=Enable

FAST_B2B_EN	9	0x0	Fast Back-to-Back to Different Devices Enable
			This bit is always 0, because the RS690 does not allow the generation of fast back-to-back transactions to different agents.
			  0=Disable
			  1=Enable

Reserved (R)	15:10	0x0	

NB_STATUS - RW - 16 bits - nbconfig:0x6			
Field Name	**Bits**	**Default**	**Description**
CAP_LIST (R)	4	0x1	Capabilities List This bit is set to indicate that this device's configuration space supports a capabilities list.
PCI_66_EN (R)	5	0x1	66-MHz Capable Indicates that the RS690 supports 66 MHz PCI operation
Reserved (R)	6	0x0	
FAST_BACK_CAPABLE (R)	7	0x0	Fast Back-to-Back Capable This bit is always 0 indicating that the RS690, as a target, is not capable of accepting fast back-to-back transactions when the transactions are not to the same agent.
DEVSEL_TIMING (R)	10:9	0x1	DEVSEL# Timing This bit field defines the timing of DEVSEL# on the RS690. The device only supports medium DEVSEL# timing.

SIGNAL_TARGET_ABORT (R)	11	0x0	Signaled Target Abort
			This bit is always 0 because the RS690 does not terminate transactions with target aborts.
			  0=No Abort
			  1=Target Abort asserted

RECEIVED_TARGET_ABORT	12	0x0	Received Target Abort
			This bit is set by whenever a CPU to PCI transaction (except for a special cycle) is terminated due to a target-abort. This bit is cleared by writing a 1.
			  0=Inactive
			  1=Active

RECEIVED_MASTER_ABORT	13	0x0	Received Master Abort
			This bit is set whenever a CPU to PCI transaction (except for a special cycle) is terminated due to a master-abort. This bit is cleared by writing a 1.
			  0=Inactive
			  1=Active

SIGNALED_SYSTEM_ERROR	14	0x0	Signaled System Error This bit is set whenever the RS690 generates a System Error and asserts the SERR# line (currently only GART Error). This bit is cleared by writing a 1. 0=No Error 1=SERR asserted
PARITY_ERROR_DETECTED (R)	15	0x0	Detected Parity Error This bit is always 0 because the RS690 does not support data parity checking.
General NB status Flags			

NB_REVISION_ID - R - 8 bits - nbconfig:0x8			
Field Name	**Bits**	**Default**	**Description**
MINOR_REV_ID	3:0	0x0	Identifies the stepping number of the device.
MAJOR_REV_ID	7:4	0x0	Identifies the revision number of the device.
Revision Identification			

NB_REGPROG_INF - R - 8 bits - nbconfig:0x9			
Field Name	**Bits**	**Default**	**Description**
REG_LEVEL_PROG_INF	7:0	0x0	Indicates a Host bridge.
Program Interface.			

NB_SUB_CLASS - R - 8 bits - nbconfig:0xA			
Field Name	**Bits**	**Default**	**Description**
SUB_CLASS_INF	7	0x0	Indicates a Host bridge.
Sub-Class Code.			

NB_BASE_CODE - R - 8 bits - nbconfig:0xB			
Field Name	**Bits**	**Default**	**Description**
BASE_CLASS_CODE	7:0	0x6	Indicates a Bridge device.
Class Code.			

NB_CACHE_LINE - R - 8 bits - nbconfig:0xC			
Field Name	**Bits**	**Default**	**Description**
CACHE_LINE_SIZE	7:0	0x0	
Cache Line Size.			

NB_LATENCY - RW - 8 bits - nbconfig:0xD			
Field Name	**Bits**	**Default**	**Description**
LATENCY_TIMER	7:0	0x0	This bit field defines the minimum amount of time (in PCI clock cycles) that the bus master can retain ownership of the bus. This is mandatory for masters that are capable of performing a burst consisting of more than two data phases.
Latency Timer.			

NB_HEADER - R - 8 bits - nbconfig:0xE			
Field Name	**Bits**	**Default**	**Description**
HEADER_TYPE	6:0	0x0	Bits [6:5] are 0, indicating that Type 00 Configuration Space Header format is supported.

DEVICE_TYPE	7	0x0	Bit [7] is always 0, indicating that the RS690's northbridge block is a single function device.
			    0=Single-Function Device
			    1=Multi-Function Device

Header Type			

NB_BIST - R - 8 bits - nbconfig:0xF			
Field Name	**Bits**	**Default**	**Description**
BIST_COMP	3:0	0x0	
BIST_STRT	6	0x0	
BIST_CAP	7	0x0	
Built-in-self-test.			

NB_BAR2_PM2 - RW - 32 bits - nbconfig:0x18			
Field Name	**Bits**	**Default**	**Description**

MEM_IO (R)	0	0x1	I/O Space:
			This bit is hardwired to 1 to indicate that this base address register maps into x86 I/O space.
			    0=Memory
			    1=I/O

RESERVED (R)	1	0x0	
PM2_BASE_LOW (R)	4:2	0x0	This field specifies that there are 8 DWORD registers allocated to this space.
PM2_BASE	31:5	0x0	PM2_BLK Base: This bit field forms the upper part of BAR2. This field is loaded by BIOS software and specifies the base of PM2_BLK.
Descriptor for Power management PM2 Control Block.			

NB_BAR3_PCIEXP_MMCFG - RW - 32 bits - nbconfig:0x1C			
Field Name	Bits	Default	Description
MEM_IO (R)	0	0x0	Memory: This bit is hardwired to 0 to indicate that this base address register maps into memory space 　0=Memory 　1=I/O
TYPE (R)	2:1	0x2	Type: This bit field is hardwired to 2'b10 to indicate that this base register is 64 bits wide and mapping can be performed anywhere in the 64-bit address space
PREFETCH_EN (R)	3	0x0	Prefetchable: This bit is hardwired to 1 to indicate that this range is prefetchable.
MEM_BASE_LOW (R)	20:4	0x0	Base Address Low: This bit field is hardwired to return zeros to indicate that xx Kbytes are allocated to PCI Express Configuration Registers.
MEM_BASE_HIGH	31:21	0x0	Base Address High: This bit field forms the upper part of BAR3. This field is loaded by BIOS software.
Descriptor for memory mapped PCI Express Configuration registers.			

NB_BAR3_UPPER_PCIEXP_MMCFG - RW - 32 bits - nbconfig:0x20			
Field Name	Bits	Default	Description
MEM_BASE_UPPER	31:0	0x0	Upper 32-bit of BAR3 base address.
Descriptor for upper part of memory mapped PCI Express Configuration registers.			

NB_ADAPTER_ID - R - 32 bits - nbconfig:0x2C			
Field Name	Bits	Default	Description
SUBSYSTEM_VENDOR_ID *(mirror of NB_ADAPTER_ID_W:SUBSYSTEM_VENDOR_ID)*	15:0	0x0	
SUBSYSTEM_ID *(mirror of NB_ADAPTER_ID_W:SUBSYSTEM_ID)*	31:16	0x0	
Subsystem Vendor ID and Subsystem ID register			

NB_CAPABILITIES_PTR - R - 32 bits - nbconfig:0x34			
Field Name	Bits	Default	Description
CAP_PTR	7:0	0xc4	This field contains a byte offset into a device's configuration space containing the first item in the capabilities list. If no next item exists, then it is set to null.
Capabilities Pointer			

NB_PCI_CTRL - RW - 32 bits - nbconfig:0x4C			
Field Name	**Bits**	**Default**	**Description**

FUNCTION_1_ENABLE	0	0x0	Enables access to Bus0Dev0Fun1.
			  0=Disable
			  1=Enable

APIC_ENABLE	1	0x1	Not used.
			  0=Disable
			  1=Enable

AlwaysUnLk	2	0x1	If set, always issues UnLk request for CPU lock transaction.
			If not set, only issues UnLk when RdLk is successful.
			  0=Disable
			  1=Enable

Cf8Dis	3	0x0	Disables IO 0xCF8 cycle to the nbcfg block.
			  0=Enable
			  1=Disable

PMEDis	4	0x0	Disables PME message generation.
			  0=Enable
			  1=Disable

SErrDis	5	0x0	Disables SErr message generation.
			  0=Enable
			  1=Disable

BMMsgEn	6	0x0	Enables BM_Set message generation.
			  0=Disable
			  1=Enable

DisLockP2P	7	0x0	If set, P2P could sneak into the MemRdLk sequence. If not set, blocks PwP during CPU lock transactions
			  0=Enable
			  1=Disable

PMArbDisSel	10:8	0x0	Setting bit [0] disables BIF request when PMArbDis is set. Setting bit [1] disables rx0(graphics pcie) DMA request when PMArbDis is set. Setting bit [2] disables rx1(SB and general purpose pcie) DMA request when PMArbDis is set.

CsrStatus	11	0x0	1 means CSR is detected. Write 1 to clear this bit. Writing 0 has no effect.
			  0=Inactive
			  1=Active

CfgRdTime	14:12	0x2	3-bit setting for RBBM read data bus data latch latency

P2PDynamicClkOff	15	0x0	If set to 1, the dynamic clock has to be turned off in order to support P2P traffic.
			  0=Enable
			  1=Disable

WakeC2En	16	0x0	1 means enable Wake_from_C2 message. 0 means disable.
			  0=Enable
			  1=Disable

BAR2_PM2Enable	17	0x0	Enables read/write access to the NB_BAR2_PM2 register. Clearing this bit could hide BAR2.
			  0=Disable
			  1=Enable

P4IntEnable	18	0x0	Enables NB to accept A4 interrupt request from SB.
			  0=Disable
			  1=Enable

SLPEnable	20	0x0	Enables SLP logic in NB.
			  0=Enable
			  1=Disable

SLP_Pad_Enable	21	0x0	Enables SLP# pad output.
			  0=Enable
			  1=Disable

BAR1_Enable	22	0x0	Enables read/write access to NB_BAR1_RCRB register. Clearing this bit could hide BAR1.
			  0=Enable
			  1=Disable

MMIOEnable	23	0x0	Enables MMIO decoding.
			  0=Enable
			  1=Disable

IsocArbMode	24	0x0	If set, checks IOCIsocArbiter setting for arbitration. If not set, checks IsocHiPr for priority.
			  0=Enable
			  1=Disable

IsocHiPr	25	0x0	If set, ISOC has high priority. If not set, the regular channel has high priority.
			  0=Enable
			  1=Disable

HPDis	26	0x0	If set, disables HP message generation
			  0=Enable
			  1=Disable

PCI Control Register.			

NB_ADAPTER_ID_W - RW - 32 bits - nbconfig:0x50			
Field Name	Bits	Default	Description
SUBSYSTEM_VENDOR_ID	15:0	0x1002	
SUBSYSTEM_ID	31:16	0x7910	
Subsystem Vendor ID and Subsystem ID write register.			

NB_MISC_INDEX - RW - 32 bits - nbconfig:0x60			
Field Name	Bits	Default	Description
NB_MISC_IND_ADDR	6:0	0x0	Northbridge Misc. index register address.

NB_MISC_IND_WR_EN	7	0x0	Northbridge Misc. index register write enable.
			  00=Disable writes to NB_MISC_DATA
			  01=Enable writes to NB_MISC_DATA

Northbridge Misc. index register address and write enable.			

NB_MISC_DATA - RW - 32 bits - nbconfig:0x64			
Field Name	Bits	Default	Description
NBMISCDATA	31:0	0x0	Northbridge Misc. index register data.
Northbridge Misc. index register data.			

NB_CNTL - RW - 32 bits - NBMISCIND:0x0			
Field Name	**Bits**	**Default**	**Description**
HIDE_NB_AGP_CAP	0	0x0	Hides AGP Capabilities in the Host Bridge (NBCFG). 　0=Visible (Enable) 　1=Hide (Disable)
HIDE_P2P_AGP_CAP	1	0x1	Hides AGP Capabilities in the P2P Bridge (APCCFG). 　0=Visible (Enable) 　1=Hide (Disable)
HIDE_NB_GART_BAR	2	0x0	Hides NB GART BAR registers and enables MC Indexed GART registers. When this bit is set to 1, the NB GART BAR register will read back 00. However, writing to the register is not disabled. 　00=Visible (Enable) 　01=Hide (Disable)
HIDE_MMCFG_BAR	3	0x0	Enables PCI Express MMCFG BAR register. 　0=Visible (Enable) 　1=Hide (Disable)
AGPMODE30	4	0x0	Enables NB/APC AGP3.0 REGISTER MODE 　0=Disable 　1=Enable AGP3.0 REGISTER MODE
AGP30ENHANCED	5	0x0	Enables NB/APC CFG ENHANCED AGP3.0 MODE (full appendix). 　0=Disable 　1=Enable ENHANCED AGP3.0 MODE
NB_SB_CFG_EN	6	0x0	If set, enables CFG access to Dev8, which is the SB P2P Bridge. 　0=Disable 　1=Enable
HWINIT_WR_LOCK	7	0x0	If set, it locks HWINIT register values. 　0=Disable 　1=Enable
HIDE_AGP_CAP	8	0x0	Hides Int Graphics Controller AGP Capabilities. 　0=Disable 　1=Enable
STRAP_MSI_ENABLE	10	0x1	Enables Int Graphics Controller MSI Capabilities Pointer 　0=Disable 　1=Enable
TESTMODE_ENABLE (R)	13	0x0	From the Test Controller.
COM_PORT_MODE (R)	14	0x0	From the Test Controller.
ROM_CTRL_POST	31:16	0x0	ROM Based Diagnostic POST CODE.
Northbridge Control.			

NB_SPARE1 - RW - 32 bits - NBMISCIND:0x2			
Field Name	**Bits**	**Default**	**Description**
NB_SPARE1_RW	15:0	0x0	Spare read/write control bits.
NB_SPARE1_RO (R)	31:16	0x0	Spare read only status bits.
Spare register.			

NB_STRAPS_READBACK_MUX - RW - 32 bits - NBMISCIND:0x3			
Field Name	Bits	Default	Description
SELECT	7:0	0x0	This register selects which 32-bits of Power-on STRAPS to be readback in NB_STRAPS_READBACK_DATA.
Strap Readback Mux Select register.			

NB_STRAPS_READBACK_DATA - R - 32 bits - NBMISCIND:0x4			
Field Name	Bits	Default	Description
READ	31:0	0x0	Values of STRAPS as selected by the mux selector, NB_STRAPS_READBACK_MUX.
Strap Readback register.			

PCIE_LINK_CFG - RW - 32 bits - NBMISCIND:0x8			
Field Name	Bits	Default	Description
SW_RESET_DURATION_GFX	1:0	0x0	
ATOMIC_SW_RESET_GFX	2	0x0	
RST_cor_reset_GFX	3	0x0	
HOLD_TRAIN0_GFX	4	0x1	Hold Port A from Link Training 0=Allow Link Training 1=Hold (Prevent) Link Training
HOLD_TRAIN1_GFX	5	0x1	Hold Port B from Link Training 0=Allow Link Training 1=Hold (Prevent) Link Training
RST_reg_reset_GFX	6	0x0	
RST_phy_reset_GFX	7	0x0	
MULTIPORT_CONFIG_GFX	11:8	0x0	Multiport Configuration of External Graphics Link 0=Port A only 1=Port A and Port B
RESERVED_GFX	12	0x0	Reserved - do not use
RST_sty_reset_GFX	13	0x0	
CALIB_RESET_GFX	14	0x0	Software Reset of pcie calibration logic 0=Disable 1=Enable
GLOBAL_RESET_GFX	15	0x0	Software Reset of pcie core logic 0=Disable 1=Enable
SW_RESET_DURATION_GPPSB	17:16	0x0	
ATOMIC_SW_RESET_GPPSB	18	0x0	
RST_cor_reset_GPPSB	19	0x0	
HOLD_TRAIN0_GPPSB	20	0x0	Hold Port A from Link Training 0=Allow Link Training 1=Hold (Prevent) Link Training
HOLD_TRAIN1_GPPSB	21	0x1	Hold Port A from Link Training 0=Allow Link Training 1=Hold (Prevent) Link Training
HOLD_TRAIN2_GPPSB	22	0x1	Hold Port A from Link Training 0=Allow Link Training 1=Hold (Prevent) Link Training
HOLD_TRAIN3_GPPSB	23	0x1	Hold Port A from Link Training 0=Allow Link Training 1=Hold (Prevent) Link Training

HOLD_TRAIN4_GPPSB	24	0x1	Hold Port A from Link Training
			    0=Allow Link Training
			    1=Hold (Prevent) Link Training

HOLD_TRAIN5_GPPSB	25	0x1	0=Allow Link Training 1=Hold (Prevent) Link Training
HOLD_TRAIN6_GPPSB	26	0x1	0=Allow Link Training 1=Hold (Prevent) Link Training
RST_reg_reset_GPPSB	27	0x0	
RST_phy_reset_GPPSB	28	0x0	
RST_sty_reset_GPPSB	29	0x0	

CALIB_RESET_GPPSB	30	0x0	Software Reset of PCIE calibration logic
			    0=Disable
			    1=Enable

GLOBAL_RESET_GPPSB	31	0x0	Software Reset of PCIE core logic
			    0=Disable
			    1=Enable

PCIE Link Configuration Register			

IOC_DMA_ARBITER - RW - 32 bits - NBMISCIND:0x9			
Field Name	**Bits**	**Default**	**Description**
DMA_ARBITER	31:0	0x0	Arbitration algorithm implementation.
IOC DMA arbiter.			

IOC_PCIE_CSR_Count - RW - 32 bits - NBMISCIND:0xA			
Field Name	**Bits**	**Default**	**Description**
CsrDelayCount	23:0	0x0	CSR frequency counter.
CsrLimitCount	31:24	0x0	CSR limit counter.
IOC CSR counter.			

IOC_PCIE_CNTL - RW - 32 bits - NBMISCIND:0xB			
Field Name	**Bits**	**Default**	**Description**
DmaFixRelaxOrder	0	0x0	Dma RO value. Only valid if FixAttrEn is set.
DmaForceSnoop	1	0x0	Dma snoop value. Only valid if FixAttrEn is set.
DmaFixAttrEn	2	0x0	Fix dma request snoop attribute.
P2pDis	3	0x0	Disables peer-to-peer transaction target at SB.
C3STPCLKDectecEn	4	0x0	
BMSetDis	7	0x0	Disables bus-master trigger event from SB.
XactOrder	8	0x1	Enables mst read order rule.
BlockNonSp	9	0x0	Blocks non-snoop dma request if PMArbDis is set.
BlockSnoop	10	0x0	Blocks snoop dma request if PMArbDis is set.
MstRelaxOrder	11	0x0	Mst RO value. Only valid if next bit is set
MstRelaxOrderEn	12	0x0	Fixes Mst RO attribute.
MstNSoopEn	13	0x0	Enables non-snoop for mst request.
ExtDevPlug	16	0x0	Detects an external device plugged.
ExtDevCsrEn	17	0x0	Enables external device csr function.
CsrEnable	18	0x0	Enables CSR.
IntSelMod	19	0x0	Interrupt ABCD(0) or EFGH(1) mode.
SetPowEn	20	0x0	Enables set_slot_power message to SB.
IOC_SB_SetPowEn	21	0x0	Enables Set_Slot_Power_limit/Scale message to SB.
IOC_SetDMAInValidEn	22	0x1	Enables DMA InValid Request handling.
IOC_SB_SetPMETurnOffEn	23	0x0	Enables PME_Turn_Off/PME_To_Ack between NB and SB.
LockOrderingByPassDisable	24	0x0	Disables ordering rule by pass for lock transactions.

DMAInvalidMode	26	0x0	Controls DMA InValid request handling mode: mode0=Return UA for non_posted request mode1=Drop all requests
CfgDat_Enable_NS_Ordering	27	0x0	

CrsIDRdEn	28	0x0	Returns 0x0001 for DeviceID and VendorID crs response.
			  0=Enable
			  1=Disable

IOC PCIE control counter			

IOC_P2P_CNTL - RW - 32 bits - NBMISCIND:0xC			
Field Name	**Bits**	**Default**	**Description**
Dev2BridgeDis	2	0x0	Setting to 1 could hide Bus0Dev2Fun0 p2p bridge
Dev3BridgeDis	3	0x0	Setting to 1 could hide Bus0Dev3Fun0 p2p bridge
Dev4BridgeDis	4	0x0	Setting to 1 could hide Bus0Dev4Fun0 p2p bridge
Dev5BridgeDis	5	0x0	Settting to 1 could hide Bus0Dev5Fun0 p2p bridge
Dev6BridgeDis	6	0x0	Setting to 1 could hide Bus0Dev6Fun0 p2p bridge
Dev7BridgeDis	7	0x0	Setting to 1 could hide Bus0Dev7Fun0 p2p bridge
GfxMetaCtl	8	0x1	Enables double flop for metastability
SBMetaCtl	9	0x1	Enables double flop for metastability
MsgMetaCtl	10	0x1	Enables double flop for metastability
DLDownResetEn	11	0x0	Enables DLDown Reset all ioc shadowed pcie registers
NonDev0ToSBEn	12	0x1	Enabling this bit will put All Type0NonDev0 external cfg request to SB
GSMEnable	13	0x0	Enables AMD generalized stutter mode
BMREQPinEnable	14	0x0	Enables BMREQ Pin
IOC p2p bridge control			

PCIE_NBCFG_REG0 - RW - 32 bits - NBMISCIND:0x32			
Field Name	**Bits**	**Default**	**Description**
STRAP_BIF_SYMALIGN_DIS_ELIDLE_GFX	0	0x1	
spare_1	1	0x0	
STRAP_BIF_SYMALIGN_MODE_GFX	2	0x1	
spare_3	3	0x0	
STRAP_BIF_ELAST_WATERMARK_GFX	5:4	0x0	
STRAP_BIF_FORCE_COMPLIANCE_GFX	7:6	0x0	
STRAP_BIF_BYPASS_SCRAMBLER_GFX	8	0x0	
B_P90RX_INCAL_FEN	9	0x0	
spare_10	10	0x0	
B_PRX_EN_FEN_GPP	11	0x0	
STRAP_BIF_SKIP_INTERVAL_GFX	14:12	0x0	
STRAP_BIF_SKIP_INTERVAL_GPPSB	17:15	0x0	
STRAP_BIF_EXIT_LATENCY_GFX	21:18	0x0	
STRAP_BIF_EXIT_LATENCY_GPPSB	25:22	0x0	
STRAP_BIF_REVERSE_LC_LANES_GPPSB	31:26	0x0	
PCIE_NBCFG register 0			

PCIE_NBCFG_REG3 - RW - 32 bits - NBMISCIND:0x33			
Field Name	**Bits**	**Default**	**Description**
STRAP_BIF_REVERSE_LC_LANES_GFX	1:0	0x0	
STRAP_BIF_REVERSE_LANES_GFX	3:2	0x0	
STRAP_BIF_REVERSE_LANES_GPPSB	9:4	0x0	
STRAP_BIF_REVERSE_ALL_GFX	10	0x0	
STRAP_BIF_FTS_yTSx_COUNT_GFX	12:11	0x0	
STRAP_BIF_FTS_yTSx_COUNT_GPP	14:13	0x0	
STRAP_BIF_SHORT_yTSx_COUNT_GFX	16:15	0x0	
STRAP_BIF_SHORT_yTSx_COUNT_GPP	18:17	0x0	
STRAP_BIF_MED_yTSx_COUNT_GFX	20:19	0x0	
STRAP_BIF_MED_yTSx_COUNT_GPP	22:21	0x0	
STRAP_BIF_LONG_yTSx_COUNT_GFX	24:23	0x0	
STRAP_BIF_LONG_yTSx_COUNT_GPP	26:25	0x0	
STRAP_BIF_BYPASS_RCVR_DET_GFX	27	0x0	
STRAP_BIF_BYPASS_RCVR_DET_GPP	28	0x0	
STRAP_BIF_COMPLIANCE_DIS_GFX	29	0x0	
STRAP_BIF_COMPLIANCE_DIS_GPP	30	0x0	
STRAP_BIF_AER_EN_GFX	31	0x0	
PCIE_NBCFG register 3			

PCIE_NBCFG_REG4 - RW - 32 bits - NBMISCIND:0x34			
Field Name	**Bits**	**Default**	**Description**
STRAP_BIF_AER_EN_GPP	0	0x0	
STRAP_BIF_PHY_RCVRDET_3NF_GFX	1	0x1	
B_P90PLL_RESET_GFX	2	0x0	
B_P90PLL_CLKR_GFX	4:3	0x0	
B_P90RX_INCAL_EN_GFX	5	0x0	
B_PRX_ARESET	6	0x0	
iPCIE_DISP_FIFO_Clock_DISABLE_GFX	7	0x0	
B_P90PLL_IBIAS_RD_GFX	9:8	0x1	
B_P90RX_INCAL_FORCE_GFX	10	0x0	
B_P90RX_CRFR_GFX	16:11	0x0	
B_P90RX_CRPHSIZE_GFX	18:17	0x2	
B_P90RX_CRFR_ON_GFX	19	0x1	
spare_20	20	0x0	
spare_21	21	0x0	
B_P90RX_CLKG_EN_GFX	22	0x1	
B_PTX_PWRS_ENB_GFX	23	0x1	
B_PTX_DEEMPH_EN_GFX	24	0x1	
STRAP_BIF_ERR_REPORTING_DIS_GFX	25	0x1	
STRAP_BIF_ERR_REPORTING_DIS_GPPSB	26	0x1	
B_P90TX_CLKG_EN_GFX	27	0x1	
B_P90PLL_IBIAS_SEL_GFX	28	0x1	
B_PRX_DET_BLOCK_GFX	29	0x0	
B_PRX_DET_BLOCK_GPPSB	30	0x0	
spare_31	31	0x0	
PCIE_NBCFG register 4			

PCIE_NBCFG_REG5 - RW - 32 bits - NBMISCIND:0x35			
Field Name	**Bits**	**Default**	**Description**
STRAP_BIF_ECN1P1_EN_GFX	0	0x1	
STRAP_BIF_ECN1P1_EN_GPPSB	1	0x1	
B_P90TX_DRV_STR_GFX	3:2	0x1	
NonD0MA_GPPSB	4	0x0	
NonD0MA_GFX	5	0x0	
Reg_Turn_Off_Both_PLLs	7:6	0x2	
spare_10_8	10:8	0x0	
B_P90RX_CRFRSIZE_GFX	12:11	0x1	
spare_13	13	0x0	
B_P90PLL_CLKF_GFX	20:14	0x7	
B_P90RX_INCAL_GFX	28:21	0x0	
spare_31_29	31:29	0x0	
PCIE_NBCFG register 5			

PCIE_NBCFG_REG6 - RW - 32 bits - NBMISCIND:0x36			
Field Name	**Bits**	**Default**	**Description**
B_P90PLL_ENSAT_GFX	0	0x1	
B_P90PLL_ENSAT_GPPSB	1	0x1	
spare_3_2	3:2	0x0	
B_P90PLL_IBIAS_GFX	13:4	0xa	
B_P90RX_CRCTRL_GFX	20:14	0x0	
B_P90RX_CRCTRL_BPASS_GFX	21	0x0	
B_P90PLL_RESET_EN_GFX	22	0x0	
B_P90PLL_TEST_GFX	23	0x0	
STRAP_BIF_STAGGER_CNTL_GFX	25:24	0x0	
STRAP_BIF_STAGGER_CNTL_GPPSB	27:26	0x0	
spare_29_28	29:28	0x0	
REG_RXCLK_RESET_2	30	0x0	
REG_RXCLK_RESET_3	31	0x0	
PCIE_NBCFG register 6			

PCIE_NBCFG_REG7 - RW - 32 bits - NBMISCIND:0x37			
Field Name	**Bits**	**Default**	**Description**
PCIE_MUX_SEL0_GFX	1:0	0x0	
PCIE_MUX_SEL1_GFX	3:2	0x0	
PCIE_MUX_SEL2_GFX	5:4	0x0	
PCIE_MUX_SEL3_GFX	7:6	0x0	
PCIE_MUX_SEL_LEVEL2_GFX	9:8	0x0	
PCIE_lane_reversal_GFX	10	0x0	
STRAP_BIF_2VC_EN_GPPSB	11	0x0	
reconfig_gppsb_en_GPPSB	12	0x0	
reconfig_gppsb_reg_idle_force_en_GPPSB	13	0x0	
reconfig_gppsb_GPPSB	14	0x0	
reconfig_gppsb_link_config_xfer_mode_GPPSB	15	0x0	
reconfig_gppsb_use_link_up_en_GPPSB	16	0x0	
reconfig_gppsb_atomic_reset_dis_GPPSB	17	0x0	
spare_31_18	31:18	0x0	
PCIE_NBCFG register 7			

PCIE_NBCFG_REG8 - RW - 32 bits - NBMISCIND:0x38			
Field Name	Bits	Default	Description
PCIE_Reserved	31:0	0x0	
PCIE_NBCFG register 8			

PCIE_STRAP_REG2 - RW - 32 bits - NBMISCIND:0x39			
Field Name	Bits	Default	Description
PCIE_STRAP_REG_Reserved	31:0	0x0	

NB_FDHC - RW - 8 bits - nbconfig:0x68			
Field Name	Bits	Default	Description

MEM_HOLE_ENABLE	7:6	0x0	Hole Enable.
			00=No hole
			01=Hole at 512KB - 640KB
			10=Hole at 15MB - 16MB
			11=Reserved
			  0=No hole
			  1=Hole at 512KB - 640KB
			  2=Hole at 15MB - 16MB
			  3=Reserved

Fixed SDRAM Hole Control required for Slot-1 operation.			

NB_SMRAM - RW - 8 bits - nbconfig:0x69			
Field Name	Bits	Default	Description
SMM_LOCATION	2:0	0x2	0x2: SMM space at 640KB-768KB. Any other encoding disables this area.

GLOBAL_SMRAM_ENABLE	3	0x0	SMM Space globally enabled.
			Once the SMM_SPACE_LOCKED bit is set, this cannot be changed until after reset.
			  0=Disable
			  1=Enable

SMM_SPACE_LOCKED	4	0x0	SMM Space Locked
			If set, SMM_LOCATION cannot be changed until after reset. It can only be written to once.
			  0=Unlocked
			  1=Locked

SMM_SPACE_OPEN	6:5	0x0	SMM Space Opened/Closed
			Once the SMM_SPACE_LOCKED bit is set, bit 6 cannot be changed until after reset.
			  0=Open for CPU transactions to SMM memory.
			  1=Closed
			  2=Open
			  3=Reserved

System Management RAM configuration. This Register is only used in Slot-1 interface mode.			

NB_EXSMRAM - RW - 8 bits - nbconfig:0x6A			
Field Name	Bits	Default	Description

TSEG_ENABLE	0	0x0	Enables TSEG space.
			Two possible locations (based on HI_SMRAM_ENABLE)
			(TOM-TSEG_SIZE) - TOM or
			(256MB+TOM-TSEG_SIZE) - (256MB+TOM)
			  0=Disable
			  1=Enable

TSEG_SIZE	2:1	0x0	0=2MB
			  1=8MB
			  2=512KB
			  3=1MB

Reserved0	5	0x1	Reserved for future use.
EX_SMRAM_ERROR	6	0x0	This bit is set if an access is attempted while the extended SMM area is disabled

HI_SMRAM_ENABLE	7	0x0	Enable high SMM/TSEG space.
			For SMM: (256MB+640KB) - (256MB+1MB). Maps to
			(640KB - 1MB).
			For TSEG: (256MB+TOM-TSEG_SIZE) - (256MB+TOM).
			Maps to (TOM-TSEG_SIZE) - TOM.
			  0=Disable
			  1=Enable

Extended System Management RAM control register. This register controls access to the extended SMM range in system memory. It is only used in Slot-1 interface mode.			

NB_PMCR - RW - 8 bits - nbconfig:0x6B			
Field Name	Bits	Default	Description

ACPI_CTL_REG_EN (R)	0	0x0	Always forced to 0.
			  0=Disable
			  1=Enable

Power Management Control			

NB_STRAP_READ_BACK - R - 32 bits - nbconfig:0x6C			
Field Name	Bits	Default	Description
DEVICE_ID	0	0x0	Hardware Configuration Bit. Indicates Device ID.

INTGFX_EN	3	0x0	Hardware Configuration Bit. Indicates that Internal Graphics has been enabled.
			  0=Disable
			  1=Enable

HDCP_KEY_VALID	4	0x0	Hardware Configuration Bit. Indicates that HDMI - HDCP keys have been programmed into the e-fuses.
			  0=not programmed
			  1=programmed

AUDIO_DISABLE	5	0x0	Hardware Configuration Bit. Indicates that High Resolution Audio is not available.
			  0=Enable
			  1=Disable

MOBILE_GFX	6	0x0	Hardware Configuration Bit. Indicates that the NB is a Mobile Part. This will affect the GFX controller Device ID.

iSTRAP_SIDE_PORT_ENb	7	0x0	This is Pin Strap GPIO[0]. Indicates that the Side Port Memory has been enabled. 0=Enable 1=Disable
STRAP_SMS_BYPASS	8	0x0	This is an EEPROM Strap. Indicates that SMS bypass has been selected.
STRAP_DEBUG_BUS_EN	9	0x0	This is Pin Strap GPIO[5]. Indicates that the Debug Bus has been enabled by pin strap GPIO[5] 0=Disable 1=Enable
LOAD_EEPROM_STRAPS	10	0x0	This is Pin Strap GPIO[1]. Indicates that EEPROM based straps for NB has been selected. 0=Disable 1=Enable
STRAP_PCIE_GPP_MODE	13:11	0x0	This is Pin Strap GPIO[4:2]. Indicates PCIe GPP mode of operation. 0=Use register value 1=Use register value 2=4-1-1-1-1 3=4-2-1-1 4=4-2-2 5=4-4 6=4-0-0-0-0 7=Use register value
EFUSE_CF_DISABLE	14	0x0	Hardware Configuration Bit. Indicates that CrossFire mode of operation is not allowed. 0=Enable 1=Disable
DISABLE_EFUSE_PGM	15	0x0	Hardware Configuration Bit. Indicates that the e-fuse programming is disabled. 0=Disable 1=Enable
STRAP_FASTBOOT_L	16	0x0	Hardware Configuration Bit from JTAG. When LOW, indicates shorten reset timers for testing purposes. 0=Short Timers for Production Test 1=Normal Operation
RS690 Strap Read Back Register			

SCRATCH_NBCFG - RW - 32 bits - nbconfig:0x78			
Field Name	**Bits**	**Default**	**Description**
SCRATCH	31:0	0x0	All of the bits in this register can be both written to, and read from, but the register does not control anything.
This register is used for scratch reading and writing.			

SCRATCH_1_NBCFG - RW - 32 bits - nbconfig:0x54			
Field Name	**Bits**	**Default**	**Description**
SCRATCH_1	31:0	0x0	

SCRATCH_2_NBCFG - RW - 32 bits - nbconfig:0x98			
Field Name	Bits	Default	Description
SCRATCH_2	31:0	0x0	

NB_HT_TRANS_COMP_CNTL - RW - 32 bits - nbconfig:0x94			
Field Name	Bits	Default	Description
TXP_COMPDATA	4:0	0x5	Calculates the compensation value for the transmitter falling edge
TXP_CTL	6:5	0x0	Transmitter falling edge PHY control value 00=Apply TXP_CALCCOMP directly 01=Apply TXP_COMPDATA directly 10=Apply the sum of TXP_CALCCOMP and TXP_COMPDATA 11=Apply the diff of TXP_CALCCOMP and TXP_COMPDATA
TXP_CALCCOMP (R)	12:8	0x5	Transmitter falling edge compensation circuitry data value
RESERVED_15_13	15:13	0x0	Bit [15]=CfgHTiu_HT_EMP_EN_TST Bit [14]=CfgHTiu_HT_TX_COMPOVR Bit [13]=CfgHTiu_HT_TX_FCOMPCYC
TXN_COMPDATA	20:16	0x4	Transmitter falling edge compensation circuitry data value
TXN_CTL	22:21	0x0	Transmitter falling edge PHY control value 00=Apply TXN_CALCCOMP directly 01=Apply TXN_COMPDATA directly 10=Apply the sum of TXN_CALCCOMP and TXN_COMPDATA 11=Apply the diff of TXN_CALCCOMP and TXN_COMPDATA
TXT_CALCCOMP (R)	28:24	0x4	Calculates the compensation value for the transmitter falling edge
RESERVED_31to29	31:29	0x0	
HT transmitter comp control			

NB_HT_CLK_CNTL_RECEIVER_COMP_CNTL - RW - 32 bits - nbconfig:0x80			
Field Name	Bits	Default	Description
RX_COMPDATA	4:0	0x9	Transmitter rising edge compensation circuitry data value
RX_CTL	6:5	0x0	Receiver rising edge PHY control value 00=Apply RX_CALCOMP directly as the compensation 01=Apply RX_COMPDATA directly as the compensation 10=Apply the sum of RX_CALCOMP and RX_COMPDATA 11=Apply the diff of RX_CALCOMP and RX_COMPDATA
RESERVED_7	7	0x0	
RX_CALCCOMP (R)	12:8	0x9	Calculated compensation value for the receiver
RESERVED_14_13	14:13	0x0	Bit [14]=CfgHTiu_HT_RX_COMPOVR Bit [13]=CfgHTiu_HT_RX_FCOMPCYC
SUCU	15	0x0	Speeda up the compensation update 0=Link PHY compensation values are allowed to changed every 1ms 1=Link PHY compensation values are allowed to changed every 1us

Field Name	Bits	Default	Description

ICGSMAF	23:16	0x0	Internal clock gating system management
			   0=No power reduction
			   1=IC power is reduced through gatind of internal clocks

REVERVED_25to24 (R)	25:24	0x0	
RESERVED_29to26	29:26	0x0	

SULS	30	0x0	Speeds up the connection sequence for frequency change
			   0=PLL lock timer is 100 us
			   1=PLL lock timer is 1us

CGEN	31	0x0	Enables clock gating
			   0=Internal clock gating is disabled
			   1=Internal clock gating is enabled

NB_HT_LINK_COMMAND - RW - 32 bits - nbconfig:0xC4			
Field Name	**Bits**	**Default**	**Description**
CAP_ID (R)	7:0	0x8	Specifies the capability ID for the link configuration space
NEXT_PTR	15:8	0x0	Read only register pointing to the next item in the capability list
BASE_UNIT_ID	20:16	0x0	Specifies the link protocol base Unit ID. Relocating the base Unit ID is not supported
UNIT_ID_COUNT (R)	25:21	0xc	Specifies the number of Unit IDs used by the chip
MASTER_HOST (R)	26	0x0	Should always be set to 0
DEFAULT_DIRECTION (R)	27	0x0	Should always be set to 0
DROP_ON_UNINIT_LINK	28	0x0	Should always be set to 0
SLAVE_PRIMARY_TYPE (R)	31:29	0x0	Read only
HT Link command			

NB_HT_LINK_CONF_CNTL - RW - 32 bits - nbconfig:0xC8			
Field Name	**Bits**	**Default**	**Description**

CRC_FLOOD_ENABLE	1	0x0	Flood enable
			   0=CRC errors do not result in a sync flood
			   1=CRC errors result in a sync flood

CRC_ERROR_COMMAND	3	0x0	CRC error command
			   0=Transmitter CRC value match the values calculated per the link specification
			   1=The link tranmission logic generates erroneous CRC value

LINK_FAILURE	4	0x0	This bit is set when a CRC error is detected. It is cleared by PWROK
INIT_COMPLETE	5	0x0	This bit is set when low level link initialization has successfully completed. If the device on the other side is unable to properly perform link initilization, then the bit is not set.
END_OF_CHAIN (R)	6	0x1	Read write 1 only 1=Fix to 1
TRANSMITTER_OFF	7	0x0	Read-write 1 only 1=No output signals on the link toggle. The input link receivers are disabled and pins may float
CRC_ERROR_DETECTED	9:8	0x0	Read. Set by hardware. Bit [9] applies to upper byte of the link, and bit [8] applies to the lower byte. When this bit is one, the hardware has detected a CRC error on the incoming link. It is cleared by PWROK

	13	0x0	
LDT3S_ENABLE	13	0x0	Link three state enable 0=During disconnect sequence. The link transmitter is driven but in underfined state 1=During disconnect sequence. The link transmitter is placed into high impedance state. It is cleared by PWROK
EXTENDED_CNTL_TIME	14	0x0	Specifies the time in which the control is held 0=At least 16 bit time 1=About 50 microseconds. It is cleared by PWROK
MAX_LINK_WIDTH_IN (R)	18:16	0x1	Specifies the operating width of the incoming to be 16 bits for side A
MAX_LINK_WIDTH_OUT (R)	22:20	0x1	Specifies the operating width of the outgoing to be 16 bits for side A
LINK_WIDTH_IN	26:24	0x0	Specifies the operating of the input width 000=8 bits 001=16 bits 100=2 bits 101=4 bits 111=Not connect. It is cleared by PWROK
LINK_WIDTH_OUT	30:28	0x0	Specifies the operating of the output width 000=8 bits 001=16 bits 100=2 bits 101=4 bits 111=Not connected. It is cleared by PWROK
HT link configuration control			

NB_HT_LINK_END - R - 32 bits - nbconfig:0xCC

Field Name	Bits	Default	Description
LINK_FAILURE	4	0x1	Device implement one link in the chain. Hardwired to 1
END_OF_CHAIN	6	0x1	Device implement one link in the chain. Hardwired to 1
TRANSMITTER_OFF	7	0x1	Device implement one link in the chain. Hardwired to 1
RESERVED_8_31	31:8	0x0	

NB_HT_LINK_FREQ_CAP_A - RW - 32 bits - nbconfig:0xD0

Field Name	Bits	Default	Description
MINOR_REVISION (R)	4:0	0x5	
MAJOR_REVISION (R)	7:5	0x1	
LINK_FREQUENCY_A	11:8	0x0	Specifies the link side A frequency 0h=200Mhz 2h=400Mhz 5h=800Mhz 6h=1000MHz. Cleared by PWROK Other selection (that are not shown) are reserved
LINK_FREQ_CAP_A	31:16	0x65	Indicates that A side of channel supports 200, 400, 800, and 1000 Mhz link frequency
HT link frequency channel A			

NB_HT_LINK_FREQ_CAP_B - R - 32 bits - nbconfig:0xD4			
Field Name	**Bits**	**Default**	**Description**
LINK_DEVICE_FEATURE_CAP	7:0	0x2	Indicates which optional features are supported by the device
RESERVED	31:8	0x0	

NB_HT_MEMORY_BASE_UPPER - RW - 32 bits - nbconfig:0xDC			
Field Name	**Bits**	**Default**	**Description**
MEMORY_BASE_UPPER_8BIT	7:0	0x0	
MEMORY_LIMIT_UPPER_8BIT	15:8	0x0	
BUS_NUMBER (R)	23:16	0x0	

NB_PCI_ARB - RW - 32 bits - nbconfig:0x84			
Field Name	**Bits**	**Default**	**Description**

RCRB_ENABLE	0	0x0	Enables RCRB memory mapped cfg access through BAR1
			  0=Disable
			  1=Enable

PM2_SB_ENABLE	2	0x0	Enables PM2_CNTL(BAR2) IO mapped cfg write access to be broadcast to both NB and SB.
			  0=Disable
			  1=Enable

EV6MODE	4	0x0	EV6 Mode:
			Indicates that the PCI interfaces have to decode memory range from 640K to 1M.
			  0=Enable
			  1=Disable

_14M_HOLE	5	0x0	14M Memory Hole:
			Creates a hole in memory from 14 Mb to 15 Mb. This register is used by the PCI decode logic to know when to accept a cycle from an external PCI master. When set, the PCI decode logic does not assert a match for addresses falling in this range.
			  0=Disable
			  1=Enable

_15M_HOLE	6	0x0	15M Memory Hole:
			Creates a hole in memory from 15 Mb to 16 Mb. This register is used by the PCI decode logic to know when to accept a cycle from an external PCI master. When set, the PCI decode logic does not assert a match for addresses falling in this range.
			  0=Disable
			  1=Enable

PM_REG_ENABLE	7	0x0	Power Management Register Enable:
			Enables BAR2 IO access decoding.
			  0=Disable
			  1=Enable

PMEMode	8	0x0	PME message mode:
			0 means PME_Turn_Off is triggered by STP_GNT(S3) request from BIU.
			1 means PME_Turn_Off is triggered by writing 1 to PMETurnOff bit(0x84[9]).
			    0=Disable
			    1=Enable

PMETurnOff	9	0x0	PME_Turn_Off message trigger:
			In case PMEMode is set, write 1 to this bit will trigger a PME_Turn_Off messages to all downstream devices. This bit is reset only then the system power is off.
			    0=Disable
			    1=Enable

READ_DATA_ERROR_DISABLE	12	0x0	Not used in the RS690.
			    0=Enable
			    1=Disable

MDA_DEBUG	15	0x0	MDA Debug:
			This bit allows monochrome display adapters (MDA) to be used simultaneously with AGP cards for debug of AGP device drivers. The behavior of RS690 display adapters is a function of this bit and the VGA Enable in (D1:0x3C[19]) as follows:
			MDA Address Ranges:
			Memory: 0B0000h-0B7FFFh
			I/O: 3B4h, 3B5h, 3B8h, 3B9h, 3BAh, 3BFh
			VGA=0, MDA=0: All MDA and VGA references go to PCI
			VGA=0, MDA=1: Operation undefined
			VGA=1, MDA=0: All VGA references go to AGP, MDA only (I/O 3BFh) go to PCI
			VGA=1, MDA=1: All VGA references go to AGP, All MDA (including memory) go to PCI
			    0=Disable
			    1=Enable

BAR3BusRange	18:16	0x0	0 means BAR3[27:20] are all used for bus number decoding so BAR3 memory map range is [39:28]
			 1 means BAR3[20] is used for bus number decoding so memory map range is [39:21]
			 2 means BAR3[21:20] are used for bus number decoding so memory map range is [39:22]
			 3 means BAR3[22:20] are used for bus number decoding so memory range is [39:23]
			
			...
			 7 means [26:20] are used for bus number decoding so memory map range is [39:27]
			    0=Disable
			    1=Enable

AGP_VGA_BIOS	31:24	0x3	AGP VGA BIOS: Indicates that the corresponding (16K) segment should be mapped to AGP's PCI bus. Bit 24 corresponds to the addresses 0xC0000-0xC3FFF and bit 31 maps addresses 0xDC000-0xDFFFF to AGP's PCI interface. One or more of these bits should be set if the AGP graphics card has a ROM BIOS.
This register provides general PCI arbiter mode control			

NB_GC_STRAPS - RW - 32 bits - nbconfig:0x8C			
Field Name	**Bits**	**Default**	**Description**
EXTGFX_ENABLE	0	0x1	External Graphic optimization Enable. 1=HTiu external graphic optimization supported 0=HTiu external graphic optimization disable 0=Disable 1=Enable
INTGFX_ENABLE (R)	1	0x1	This bit is read only and it is the value of the e-fuse HW config bit. 0=The internal graphics logic is disabled 1=The internal graphics logic is enabled.
VGA_DISABLE	2	0x0	0=Enable 1=Disable
ID_DISABLE	3	0x0	0=Enable 1=Disable
APERTURE_SIZE	6:4	0x3	0=128MB 1=256MB 2=64MB 3=32MB 4=512MB 5=1GB 6=Reserved 7=Reserved
F1_MULTI_FUNC_ENABLE	7	0x0	
F2_MULTI_FUNC_ENABLE	8	0x0	
GFX_DEBUG_BAR_ENABLE	9	0x0	
GFX_DEBUG_DECODE_ENABLE	10	0x0	
ENINTb	11	0x0	
VE (R)	12	0x0	
EXT_MEM_EN	13	0x1	
BLANK_ROM	14	0x0	
POWER_ON_STRAPS	27:16	0x0	Extra strapping signals
MOBILE (R)	28	0x0	This is the value of the pin strap on the DAC_VSYNC pin during strap capture. The strap name is STRAP_MOBILE_GFX. This pinstrap changes the Device ID of the Internal Graphics Device and allows C3 functionality (STP_AGP#/AGP_BUSY#). When Pinstrap is 1, it selects the mobile graphics device ID. When Pinstrap is 0, it selects the desktop graphics device ID.
CHG_ID (R)	31:29	0x0	CHANGE_ID from nb_efuse.
Graphics Controller strap access register			

NB_TOP_OF_DRAM_SLOT1 - RW - 32 bits - nbconfig:0x90			
Field Name	**Bits**	**Default**	**Description**
TOP_OF_DRAM	31:23	0x0	PCI Memory Top: This 8-bit field is compared to the incoming PCI Bus master address to determine if a memory cycle falls within the RS690's DRAM region. The BIOS should write to this field following the completion of the memory sizing algorithm, after it has determined the total size of the installed memory.
This register is used to define the top of main system memory. It is used to compare the memory addresses of an external PCI master to determine if it is in the range of the RS690's system DRAM. If the address compares then the RS690 will respond to the bus master access by asserting DEVSEL#.			

NB_AGP_ADDRESS_SPACE_SIZE - RW - 32 bits - nbconfig:0xF8			
Field Name	**Bits**	**Default**	**Description**

GART_EN	0	0x0	GART Enable.
			When clear, GART is not valid in this system. The SBIOS will not allocate virtual address space for GART because the Host-PCI Bridge (Device 0) AGP Virtual Address Space (BAR1), offset 0x10, will be internally forced to 0. This bit must be set by the BIOS PCI enumeration routines. When set, GART is valid in this system. The SBIOS allocates virtual address space for GART based upon the value in bits [3:1] above.
			  0=Disable
			  1=Enable

VA_SIZE	3:1	0x0	Virtual Address Size. This field defines the virtual address space size to be allocated to GART by the SBIOS. Prior to the execution of the SBIOS memory mapping software, the SBIOS gets the amount of GART virtual address space required by the graphics controller. It sets these bits to the required value. Changing these bits automatically changes bits [30:25] in the Host-PCI Bridge (Device0) AGP Virtual Address Space Register (BAR1), offset 0x10. The size of GART virtual address space is always greater than, or equal to, the amount of physical system memory allocated to AGP in non-contiguous 4KB blocks. The amount of physical memory allocated to AGP is determined by the operating system software. [3] [2] [1] VA_Size 0 0 0 32 MB 0 0 1 64 MB 0 1 0 128 MB 0 1 1 256 MB 1 0 0 512 MB 1 0 1 1 Gig 1 1 0 2 Gig 1 1 1 Undefined
VGA_IA_EN	16	0x0	0=Disable 1=Enable
This register controls the size of the AGP aperture allocated by the BIOS, the GART functionality and the granularity of VGA address decoding.			

NB_AGP_MODE_CONTROL - RW - 32 bits - nbconfig:0xFC			
Field Name	**Bits**	**Default**	**Description**
POST_GART_Q_SIZE	18	0x0	Post GART Queue Size. When set, this bit forces the post GART queue structures to implement half the entry depth (for debug/performance analysis). 0=8 Entries 1=4 Entries
NONGART_SNOOP	19	0x0	Non GART Snoop. When set, this bit forces AGP accesses that are not in the GART range to cause system bus probes to the processor(s). When clear, AGP addresses that fall outside of the GART range do not cause probes. 0=Disable 1=Enable
AGP_RD_BUF_SIZE	20	0x0	AGP Read Buffer Size. When clear, the AGP read buffer contains 64 QWs of storage. When set, the AGP read buffer contains 32 QWs of storage (for debug/performance analysis). 0=64 QW 1=32 QW
This register controls specific features of the RS690's AGP implementation.			

NB_PCIE_INDX_ADDR - RW - 32 bits - nbconfig:0xE0			
Field Name	**Bits**	**Default**	**Description**
NB_PCIE_INDX_ADDR	7:0	0x0	Index register for the PCI Express common indirect registers
GFX_GPPSB_SEL	16	0x0	Select the PCIE core whose common indirect space is to be accessed. 0=External GFX PCIE core 1=General Purpose Port and southbridge PCIE core
Index register for the PCI Express common indirect registers.			

NB_PCIE_INDX_DATA - RW - 32 bits - nbconfig:0xE4			
Field Name	**Bits**	**Default**	**Description**
NB_PCIE_INDX_DATA	31:0	0x0	Data register for the PCI Express common indirect registers
Data Register used for the PCI Express common indirect registers.			

NB_MC_INDEX - RW - 32 bits - nbconfig:0xE8			
Field Name	**Bits**	**Default**	**Description**
NB_MC_IND_ADDR	8:0	0x0	
NB_MC_IND_WR_EN	9	0x0	0=Disable writes to NB_MC_DATA 1=Enable writes to NB_MC_DATA
Memory controller index register address.			

NB_MC_DATA - RW - 32 bits - nbconfig:0xEC			
Field Name	**Bits**	**Default**	**Description**
NB_MC_DATA	31:0	0x0	
Memory controller index register data.			

NB_CFG_Q_F1000_800 - RW - 8 bits - nbconfig:0x9C			
Field Name	**Bits**	**Default**	**Description**

CFG_Q_F1000_800	0	0x0	Set this bit, and 0x6 in LINK_FREQUENCY_A, to enable 1GHz mode during the next link frequency/width switch
			  0=Disable
			  1=Enable

spare_1	1	0x0	Spare bit. Presently not used
			  0=Disable
			  1=Enable

F1000_800_en	2	0x0	0=Disable 1=Enable

spare_7_3	7:3	0x0	Spare bit. Presently not used
			  0=Disable
			  1=Enable

Control bit			

PCIE_PDNB_CNTL - RW - 32 bits - NBMISCIND:0x7			
Field Name	**Bits**	**Default**	**Description**
ENABLE_CLKGATE_GFX_TXCLK	0	0x0	
ENABLE_CLKGATE_GFX_TXCLK_L0S	1	0x0	
ENABLE_CLKGATE_GFX_TXCLK_SND_RCV	2	0x0	
GFX_PERM2_TXCLK_STOP	3	0x0	
ENABLE_CLKGATE_GPPSB_TXCLK	4	0x0	
ENABLE_CLKGATE_GPPSB_TXCLK_L0S	5	0x0	
ENABLE_CLKGATE_GPPSB_TXCLK_SND_RCV	6	0x0	
GPPSB_PERM2_TXCLK_STOP	7	0x0	
GFX_TXCLK_SND_RCV_0_SEL	8	0x0	
spare_9	9	0x0	
GFX_TXCLK_SND_RCV_1_SEL	10	0x0	
spare_11	11	0x0	
GFX_TXCLK_SND_RCV_2_SEL	12	0x0	
spare_13	13	0x0	
GFX_TXCLK_SND_RCV_3_SEL	14	0x0	
spare_15	15	0x0	
GFX_TXCLK_SEL	16	0x0	
spare_17	17	0x0	
GPPSB_PDNB_DLY_SEL_GPPSB	19:18	0x0	
GFX_PDNB_DLY_SEL_GPPSB	21:20	0x0	
ALL_ELEC_IDLE_GPPSB	22	0x0	
ENABLE_PLL_LOCK_TIME_GPPSB	23	0x0	
IO_TXCLK0_CNTL	24	0x0	
ALL_ELEC_IDLE_GFX	25	0x0	
IO_TXCLK1_CNTL	26	0x0	

spare_27	27	0x0	
IO_TXCLK2_CNTL	28	0x0	
spare_29	29	0x0	
IO_TXCLK3_CNTL	30	0x0	
spare_31	31	0x0	
PCIE control register			

HTIU_NB_INDEX - RW - 32 bits - nbconfig:0xA8

Field Name	Bits	Default	Description
HTIU_NB_IND_ADDR	6:0	0x0	
HTIU_NB_IND_WR_EN	8	0x0	0=Disable writes to HTIU_NB_DATA 1=Enable writing to HTIU_NB_DATA

HTIU_NB_DATA - RW - 32 bits - nbconfig:0xAC

Field Name	Bits	Default	Description
HTIU_NB_DATA	31:0	0x0	

NB_BAR1_RCRB - RW - 32 bits - nbconfig:0x14

Field Name	Bits	Default	Description

MEM_IO (R)	0	0x0	Memory:
			This bit is hardwired to 0 to indicate that this base address register maps into memory space
			  0=Memory
			  1=I/O

TYPE (R)	2:1	0x0	Type: This bit field is hardwired to indicate that this base register is 32 bits wide and mapping can be performed anywhere in the 32-bit address space
PREFETCH_EN (R)	3	0x0	Unprefetchable: This bit is hardwired to 0 to indicate that this range is un-prefetchable
RCRB_BASE	31:12	0x0	Base Address High[31:12] This filed is used to define a 4K memory mapped root complex register block
Descriptor for memory mapped RCRB registers			

NB_ECC_CTRL - R - 32 bits - nbconfig:0x48

Field Name	Bits	Default	Description
NOT_IMPLEMENTED	31:0	0x0	The RS690 will not support ECC for system memory accesses.
Northbridge ECC Control Register			

NB_IOC_DEBUG - RW - 32 bits - NBMISCIND:0x1

Field Name	Bits	Default	Description
SLI_OVERWRITE_EN	0	0x0	1=Overwrite SLI strap inputs (enable dev3 p2p bridge access) 0=Takes SLI inputs to control dev3 bridge access. Note: dev3 access is also controlled by IOC_P2P_CNTL:Dev3BridgeDis(nbmiscind0x0C). If only IOC_P2P_CNTL:Dev3BridgeDis is 0, access to dev3 bridge is possible.
NB_IOC_DEBUG_RW	15:1	0x0	Spare Read/Write Control Bits
IOC_MultiReqVldErr (R)	16	0x0	Detect Multiple CPU Downstream Request Valid Error
IOC_MemMapCfgErr (R)	17	0x0	Detect Memory Map Cfg Access Format Error
NB_IOC_DEBUG_RO (R)	31:18	0x0	Spare Read Only Status Bits
IOC Debugging purpose registers			

DFT_CNTL0 - RW - 32 bits - NBMISCIND:0x5

Field Name	Bits	Default	Description
TEST_DEBUG_EN	0	0x0	
TEST_DEBUG_OUT_EN	3:1	0x0	
TEST_DEBUG_IDSEL	9:4	0x0	
TEST_DEBUG_MUX	15:10	0x0	
GPIO_DEBUG_BUS_MUX_SEL0	19:16	0x0	
GPIO_DEBUG_BUS_MUX_SEL1	23:20	0x1	
GPIO_DEBUG_BUS_MUX_SEL2	27:24	0x2	
GPIO_DEBUG_BUS_MUX_SEL3	31:28	0x3	
DFT control 0 register			

DFT_CNTL1 - RW - 32 bits - NBMISCIND:0x6

Field Name	Bits	Default	Description
TEST_DEBUG_COUNTER_EN	0	0x0	
TEST_DEBUG_IN_EN	1	0x0	
DEBUG_TESTCLKIN	2	0x0	
TEST_CLK0_INV	3	0x0	
DFT_MISC	15:4	0x0	
COM_PORT_OE	17:16	0x0	
COM_PORT_OUT	19:18	0x0	
COM_PORT_IN (R)	21:20	0x0	
DFT control 1 register			

IOCIsocMapAddr_LO - RW - 32 bits - NBMISCIND:0xE

Field Name	Bits	Default	Description
IsocMapAdd_LO	31:6	0x0	If the dma isoc address is invalid, it maps to this pre-defined address.
isoc channel address mapping			

IOCIsocMapAddr_HI - RW - 32 bits - NBMISCIND:0xF

Field Name	Bits	Default	Description
IsocMapAdd_HI	7:0	0x0	If the dma isoc address is invalid, it maps to this pre-defined address
isoc channel address mapping			

DFT_CNTL2 - R - 32 bits - NBMISCIND:0x10

Field Name	Bits	Default	Description
TEST_DEBUG_READBACK	15:0	0x0	
DFT control 2 register			

NB_TOM_PCI - RW - 32 bits - NBMISCIND:0x16

Field Name	Bits	Default	Description
SAME_AS_TOM_BIU	0	0x1	TOM of PCI equals TOM of BIU if this bit is 1
TOM_FOR_PCI	31:16	0x0	TOM for PCI
TOM for PCI			

NB_MMIOBASE - RW - 32 bits - NBMISCIND:0x17

Field Name	Bits	Default	Description
MMIOBASE	31:8	0x0	Register bits [31:8] define MMIOBASE [39:16], which is the MMIO base address.
Lower MMIO base			

NB_MMIOLIMIT - RW - 32 bits - NBMISCIND:0x18

Field Name	Bits	Default	Description
MMIOLIMIT	31:8	0x0	Register bits [31:8] define MMIOLIMIT [39:16], which is the MMIO LIMIT address.
High MMIO base			

NB_INTERRUPT_PIN - RW - 32 bits - NBMISCIND:0x1F

Field Name	Bits	Default	Description
REG_AP_SIZE	1:0	0x1	Sets the size of the core graphics memory mapped register aperture 11=256K 10=128K 01=64k 00=32K
GFX_INTERRUPT_PIN	2	0x0	0=Set the graphics interrupt pin to INTA# 1=Set the graphics interrupt pint to INTB#
F2_INTERRUPT_PIN	3	0x0	0=Set the F2 interrupt pin to INTA# 1=Set the F2 interrupt pint to INTB#
INTERRUPT register			

NB_PROG_DEVICE_REMAP_0 - RW - 32 bits - NBMISCIND:0x20

Field Name	Bits	Default	Description
NB_PROG_DEVMAP_EN	0	0x0	
IOC_PCIE_Dev_Remap_Dis	1	0x1	
GPP_PORTB_DEVMAP	7:4	0x0	
GPP_PORTC_DEVMAP	11:8	0x0	
GPP_PORTD_DEVMAP	15:12	0x0	
GPP_PORTE_DEVMAP	19:16	0x0	

IOC_LAT_PERF_CNTR_CNTL - RW - 32 bits - NBMISCIND:0x30

Field Name	Bits	Default	Description
LAT_PERF_CNTR_EN	0	0x0	Enables counter.
LAT_PERF_CNTR_FREEZE	1	0x0	Freezes average counter.
LAT_PERF_PATH_SEL	4:2	0x0	Selects path (snoop0, snoop1, nonsnoop0, nonsnoop1) to bring out to read back register.
LAT_PERF_CNTR_SEL	7:5	0x0	Selects counter (max, min, total reads, total time) to bring out to read back register.
DMA Latency counter control register			

IOC_LAT_PERF_CNTR_OUT - R - 32 bits - NBMISCIND:0x31

Field Name	Bits	Default	Description
LAT_PERF_CNTR	31:0	0x0	DMA Latency read back bits.
DMA Latency read back register			

PCIE_STRAP_REG2 - RW - 32 bits - NBMISCIND:0x39

Field Name	Bits	Default	Description
PCIE_STRAP_REG_Reserved	31:0	0x0	

NB_BROADCAST_BASE_LO - RW - 32 bits - NBMISCIND:0x3A

Field Name	Bits	Default	Description
GPU_FB_BROADCAST_BASE_LO	31:20	0x0	Broadcast base address [31:20].
Broadcast bass low address			

NB_BROADCAST_BASE_HI - RW - 32 bits - NBMISCIND:0x3B

Field Name	Bits	Default	Description
GPU_FB_BROADCAST_BASE_HI	31:0	0x0	Broadcast base address [63:32]
Broadcast base high address			

NB_BROADCAST_CNTL - RW - 32 bits - NBMISCIND:0x3C

Field Name	Bits	Default	Description
GPU_FB_BROADCAST_SIZE	7:0	0x0	Broadcast range size, unit is 8MB. 0x01=8MBytes 0x02=16Mbytes
GPU_FB_BROADCAST_PRIMARY	8	0x0	Define primary graphics device 0=Dev2 P2P bridge connects to primary 1=Dev3 P2P bridge
GPU_FB_BROADCAST_EN	9	0x0	Enables broadcast range
GPU_FB_BROADCAST_OFFSET	31:12	0x0	Offset between prefetchable base address and translated broadcast base.
Broadcast control register			

NB_APIC_P2P_CNTL - RW - 32 bits - NBMISCIND:0x3D

Field Name	Bits	Default	Description
APIC_D2_Enable	0	0x0	Enables Dev2 PCI bridge APIC range decoding. The CPU memory request with address[39:12] = 0x00_FECx_x is decoded and issued to each P2P bridge, depending on each bridge's APIC range setting. What is left in this range(0x00_FECx_x) that is not declared by any bridge is forwarded to the SB.
APIC_D3_Enable	1	0x0	Enables Dev3 PCI bridge APIC range decoding
APIC_D4_Enable	2	0x0	Enables Dev4 PCI bridge APIC range decoding
APIC_D5_Enable	3	0x0	Enables Dev5 PCI bridge APIC range decoding
APIC_D6_Enable	4	0x0	Enables Dev6 PCI bridge APIC range decoding
APIC_D7_Enable	5	0x0	Enables Dev7 PCI bridge APIC range decoding
PCI bridge APIC control register			

NB_APIC_P2P_RANGE_0 - RW - 32 bits - NBMISCIND:0x3E

Field Name	Bits	Default	Description
APIC_D2_Range	7:0	0x0	Defines bits [19:12] for Dev2 APIC range. Dev2 APIC range is Addr[39:12] = 20'h00_FEC, APIC_D2_Range[7:0]
APIC_D3_Range	15:8	0x0	Defines bits[19:12] for Dev3 APIC range. Dev3 APIC range is Addr[39:12] = 12'h00_FEC, APIC_D3_Range[7:0]
APIC_D4_Range	23:16	0x0	Defines bits [19:12] for Dev4 APIC range. Dev4 APIC range is Addr[39:12] = 12'h00_FEC, APIC_D4_Range[7:0]
APIC_D5_Range	31:24	0x0	Defines bits [19:12] for Dev5 APIC range. Dev5 APIC range is Addr[39:12] = 12'h00_FEC, APIC_D5_Range[7:0]
PCI bridge APIC range 0			

NB_APIC_P2P_RANGE_1 - RW - 32 bits - NBMISCIND:0x3F

Field Name	Bits	Default	Description
APIC_D6_Range	7:0	0x0	Defines bits [19:12] for Dev6 APIC range. Dev6 APIC range is Addr[39:12] = 20'h00_FEC, APIC_D6_Range[7:0]
APIC_D7_Range	15:8	0x0	Defines bits [19:12] for Dev7 APIC range. Dev7 APIC range is Addr[39:12] = 20'h00_FEC, APIC_D7_Range[7:0]
PCI bridge APIC range 1			

GPIO_PAD - RW - 32 bits - NBMISCIND:0x40			
Field Name	Bits	Default	Description
GPIO_TMDS_HPD_OR	0	0x0	
GPIO_DDC_DATA_OR	1	0x0	
GPIO_I2C_CLK_OR	2	0x0	
GPIO_I2C_DATA_OR	3	0x0	
GPIO_STRP_DATA_OR	4	0x0	
GPIO_DAC_SDA_OR	5	0x0	
GPIO_DAC_HSYNC_OR	6	0x0	
GPIO_DAC_VSYNC_OR	7	0x0	
GPIO_LVDS_ENA_BL_OR	8	0x0	
GPIO_LVDS_DIGON_OR	9	0x0	
GPIO_LVDS_BLON_OR	10	0x0	
GPIO_CPU_SLPb_OR	11	0x0	
PAD_0_spare_15_12	15:12	0x0	
GPIO_TMDS_HPD_A	16	0x0	
GPIO_DDC_DATA_A	17	0x0	
GPIO_I2C_CLK_A	18	0x0	
GPIO_I2C_DATA_A	19	0x0	
GPIO_STRP_DATA_A	20	0x0	
GPIO_DAC_SDA_A	21	0x0	
GPIO_DAC_HSYNC_A	22	0x0	
GPIO_DAC_VSYNC_A	23	0x0	
GPIO_LVDS_ENA_BL_A	24	0x0	
GPIO_LVDS_DIGON_A	25	0x0	
GPIO_LVDS_BLON_A	26	0x0	
GPIO_CPU_SLPb_A	27	0x0	
PAD_0_spare_31_28	31:28	0x0	
GPIO_PAD			

GPIO_PAD_CNTL_PU_PD - RW - 32 bits - NBMISCIND:0x41			
Field Name	Bits	Default	Description
GPIO_TMDS_HPD_PU	0	0x1	
GPIO_DDC_DATA_PU	1	0x1	
GPIO_I2C_CLK_PU	2	0x1	
GPIO_I2C_DATA_PU	3	0x1	
GPIO_STRP_DATA_PU	4	0x1	
GPIO_DAC_SDA_PU	5	0x1	
GPIO_DAC_HSYNC_PU	6	0x1	
GPIO_DAC_VSYNC_PU	7	0x1	
GPIO_LVDS_ENA_BL_PU	8	0x1	
GPIO_LVDS_DIGON_PU	9	0x1	
GPIO_LVDS_BLON_PU	10	0x1	
GPIO_CPU_SLPb_PU	11	0x1	
spare_15_12	15:12	0x0	
GPIO_TMDS_HPD_PD	16	0x0	
GPIO_DDC_DATA_PD	17	0x0	
GPIO_I2C_CLK_PD	18	0x0	
GPIO_I2C_DATA_PD	19	0x0	
GPIO_STRP_DATA_PD	20	0x0	
GPIO_DAC_SDA_PD	21	0x0	
GPIO_DAC_HSYNC_PD	22	0x0	
GPIO_DAC_VSYNC_PD	23	0x0	
GPIO_LVDS_ENA_BL_PD	24	0x0	
GPIO_LVDS_DIGON_PD	25	0x0	
GPIO_LVDS_BLON_PD	26	0x0	
GPIO_CPU_SLPb_PD	27	0x0	
spare_31_28	31:28	0x0	
GPIO_PAD_CNTL_PU_PD			

GPIO_PAD_SCHMEM_OE - RW - 32 bits - NBMISCIND:0x42			
Field Name	**Bits**	**Default**	**Description**
GPIO_TMDS_HPD_SCHMEN	0	0x1	
GPIO_DDC_DATA_SCHMEN	1	0x1	
GPIO_I2C_CLK_SCHMEN	2	0x1	
GPIO_I2C_DATA_SCHMEN	3	0x1	
GPIO_STRP_DATA_SCHMEN	4	0x1	
GPIO_DAC_SDA_SCHMEN	5	0x1	
GPIO_DAC_HSYNC_SCHMEN	6	0x1	
GPIO_DAC_VSYNC_SCHMEN	7	0x1	
GPIO_LVDS_ENA_BL_SCHMEN	8	0x1	
GPIO_LVDS_DIGON_SCHMEN	9	0x1	
GPIO_LVDS_BLON_SCGMEN	10	0x1	
GPIO_CPU_SLPb_SCHMEN	11	0x1	
spare_15_12	15:12	0x0	
GPIO_TMDS_HPD_OE	16	0x0	
GPIO_DDC_DATA_OE	17	0x0	
GPIO_I2C_CLK_OE	18	0x0	
GPIO_I2C_DATA_OE	19	0x0	
GPIO_STRP_DATA_OE	20	0x0	
GPIO_DAC_SDA_OE	21	0x0	
GPIO_DAC_HSYNC_OE	22	0x0	
GPIO_DAC_VSYNC_OE	23	0x0	
GPIO_LVDS_ENA_BL_OE	24	0x0	
GPIO_LVDS_DIGON_OE	25	0x0	
GPIO_LVDS_BLON_OE	26	0x0	
GPIO_CPU_SLPb_OE	27	0x0	
spare_31_28	31:28	0x0	
GPIO_PAD_SCHMEM_OE			

GPIO_PAD_SP_SN - RW - 32 bits - NBMISCIND:0x43			
Field Name	**Bits**	**Default**	**Description**
GPIO_SRP	0	0x1	
GPIO_SRN	1	0x1	
GPIO_SP_3	2	0x0	
GPIO_SP_2	3	0x0	
GPIO_SP_1	4	0x1	
GPIO_SP_0	5	0x1	
GPIO_SN_3	6	0x0	
GPIO_SN_2	7	0x0	
GPIO_SN_1	8	0x1	
GPIO_SN_0	9	0x1	
GPIO_PAD_SP_SN			

DFT_VIP_IO_GPIO - RW - 32 bits - NBMISCIND:0x44			
Field Name	**Bits**	**Default**	**Description**
DFT_GPIO_OE	5:0	0x0	
DFT_GPIO_A	13:8	0x0	
DFT_GPIO_Y (R)	21:16	0x0	
VIP_IO_TVCLKIN_GPIO_EN	24	0x0	
VIP_IO_TVCLKIN_GPIO_A	25	0x0	
VIP_IO_TVCLKIN_GPIO_Y (R)	26	0x0	

DFT_VIP_IO_GPIO_OR - RW - 32 bits - NBMISCIND:0x45			
Field Name	**Bits**	**Default**	**Description**
DFT_GPIO_OR	5:0	0x0	
VIP_IO_TVCLKIN_GPIO_OR	8	0x0	

NB_MC_IND_INDEX - RW - 32 bits - nbconfig:0x70			
Field Name	**Bits**	**Default**	**Description**
MC_IND_ADDR	15:0	0x0	
MC_IND_SEQ_RBS_0	16	0x0	0=Do not access sequencer+gfx return bus block 0 (channels A+B) 1=Access sequencer+gfx return bus block 0 (channels A+B)
MC_IND_SEQ_RBS_1	17	0x0	0=Do not access sequencer+gfx return bus block 1 (channels C+D) 1=Access sequencer+gfx return bus block 1 (channels C+D)
MC_IND_SEQ_RBS_2	18	0x0	0=Do not access sequencer+gfx return bus block 2 (channels E+F) 1=Access sequencer+gfx return bus block 2 (channels E+F)
MC_IND_SEQ_RBS_3	19	0x0	0=Do not access sequencer+gfx return bus block 3 (channels G+H) 1=Access sequencer+gfx return bus block 3 (channels G+H)
MC_IND_AIC_RBS	20	0x0	0=Do not access aic+cpvf and glb return bus block 1=Access aic+cpvf and glb return bus block
MC_IND_CITF_ARB0	21	0x0	0=Do not access client MCT interface+arbitration block 1=Access client MCT interface+arbitration block
MC_IND_CITF_ARB1	22	0x0	0=Do not access client MCB interface+arbitration block 1=Access client MCB interface+arbitration block
MC_IND_WR_EN	23	0x0	0=Disable write capability (read only) 1=Enable write capability
MC_IND_RD_INV	24	0x0	0=Do not invert data on return bus 1=Invert data on return bus
Index register for accessing MC indirect registers in mmreg (mcind) space. Note: Only mcind 0x10-38 are accessible			

NB_MC_IND_DATA - RW - 32 bits - nbconfig:0x74			
Field Name	**Bits**	**Default**	**Description**
MC_IND_DATA	31:0	0x0	
Data register for accessing MC indirect registers in mmreg (mcind) space. Note: Only mcind 0x10-38 are accessible			

NB_IOC_CFG_CNTL - RW - 32 bits - nbconfig:0x7C			
Field Name	**Bits**	**Default**	**Description**

FORCE_INTGFX_DISABLE	0	0x0	When set to 1 this bit will override the e-fuse HW Config bit to disable the internal GFX bridge, regardless of the actual state of the e-fuse bit. This will disable the APC bridge access if present.
			  0=Normal
			  1=Disable

spare_29_0	29:1	0x0	

NB_BAR3_PCIEXP_REG_WREN	30	0x0	Enables writes to the BAR3 register.
			  0=Disable
			  1=Enable

IOC CFG control register			

IOC_PCIE_D2_CSR_Count - RW - 32 bits - NBMISCIND:0x50			
Field Name	**Bits**	**Default**	**Description**
CsrDelayCount	23:0	0x0	
CsrLimitCount	31:24	0x0	

IOC_PCIE_D2_CNTL - RW - 32 bits - NBMISCIND:0x51			
Field Name	**Bits**	**Default**	**Description**
DmaFixRelaxOrder	0	0x0	
DmaForceSnoop	1	0x0	
DmaFixAttrEn	2	0x0	
P2pDis	3	0x0	
BMSetDis	7	0x0	
XactOrder	8	0x1	
BlockNonSp	9	0x0	
BlockSnoop	10	0x0	
MstRelaxOrder	11	0x0	
MstRelaxOrderEn	12	0x0	
MstNSoopEn	13	0x0	
ExtDevPlug	16	0x0	
ExtDevCsrEn	17	0x0	
CsrEnable	18	0x0	
IntSelMod	19	0x0	
SetPowEn	20	0x0	

IOC_PCIE_D3_CSR_Count - RW - 32 bits - NBMISCIND:0x52			
Field Name	**Bits**	**Default**	**Description**
CsrDelayCount	23:0	0x0	
CsrLimitCount	31:24	0x0	

IOC_PCIE_D3_CNTL - RW - 32 bits - NBMISCIND:0x53

Field Name	Bits	Default	Description
DmaFixRelaxOrder	0	0x0	
DmaForceSnoop	1	0x0	
DmaFixAttrEn	2	0x0	
P2pDis	3	0x0	
BMSetDis	7	0x0	
XactOrder	8	0x1	
BlockNonSp	9	0x0	
BlockSnoop	10	0x0	
MstRelaxOrder	11	0x0	
MstRelaxOrderEn	12	0x0	
MstNSoopEn	13	0x0	
ExtDevPlug	16	0x0	
ExtDevCsrEn	17	0x0	
CsrEnable	18	0x0	
IntSelMod	19	0x0	
SetPowEn	20	0x0	

IOC_PCIE_D4_CSR_Count - RW - 32 bits - NBMISCIND:0x54

Field Name	Bits	Default	Description
CsrDelayCount	23:0	0x0	
CsrLimitCount	31:24	0x0	

IOC_PCIE_D4_CNTL - RW - 32 bits - NBMISCIND:0x55

Field Name	Bits	Default	Description
DmaFixRelaxOrder	0	0x0	
DmaForceSnoop	1	0x0	
DmaFixAttrEn	2	0x0	
P2pDis	3	0x0	
BMSetDis	7	0x0	
XactOrder	8	0x1	
BlockNonSp	9	0x0	
BlockSnoop	10	0x0	
MstRelaxOrder	11	0x0	
MstRelaxOrderEn	12	0x0	
MstNSoopEn	13	0x0	
ExtDevPlug	16	0x0	
ExtDevCsrEn	17	0x0	
CsrEnable	18	0x0	
IntSelMod	19	0x0	
SetPowEn	20	0x0	

IOC_PCIE_D5_CSR_Count - RW - 32 bits - NBMISCIND:0x56

Field Name	Bits	Default	Description
CsrDelayCount	23:0	0x0	
CsrLimitCount	31:24	0x0	

IOC_PCIE_D5_CNTL - RW - 32 bits - NBMISCIND:0x57			
Field Name	**Bits**	**Default**	**Description**
DmaFixRelaxOrder	0	0x0	
DmaForceSnoop	1	0x0	
DmaFixAttrEn	2	0x0	
P2pDis	3	0x0	
BMSetDis	7	0x0	
XactOrder	8	0x1	
BlockNonSp	9	0x0	
BlockSnoop	10	0x0	
MstRelaxOrder	11	0x0	
MstRelaxOrderEn	12	0x0	
MstNSoopEn	13	0x0	
ExtDevPlug	16	0x0	
ExtDevCsrEn	17	0x0	
CsrEnable	18	0x0	
IntSelMod	19	0x0	
SetPowEn	20	0x0	

IOC_PCIE_D6_CSR_Count - RW - 32 bits - NBMISCIND:0x58			
Field Name	**Bits**	**Default**	**Description**
CsrDelayCount	23:0	0x0	
CsrLimitCount	31:24	0x0	

IOC_PCIE_D6_CNTL - RW - 32 bits - NBMISCIND:0x59			
Field Name	**Bits**	**Default**	**Description**
DmaFixRelaxOrder	0	0x0	
DmaForceSnoop	1	0x0	
DmaFixAttrEn	2	0x0	
P2pDis	3	0x0	
BMSetDis	7	0x0	
XactOrder	8	0x1	
BlockNonSp	9	0x0	
BlockSnoop	10	0x0	
MstRelaxOrder	11	0x0	
MstRelaxOrderEn	12	0x0	
MstNSoopEn	13	0x0	
ExtDevPlug	16	0x0	
ExtDevCsrEn	17	0x0	
CsrEnable	18	0x0	
IntSelMod	19	0x0	
SetPowEn	20	0x0	

IOC_PCIE_D7_CSR_Count - RW - 32 bits - NBMISCIND:0x5A			
Field Name	**Bits**	**Default**	**Description**
CsrDelayCount	23:0	0x0	
CsrLimitCount	31:24	0x0	

IOC_PCIE_D7_CNTL - RW - 32 bits - NBMISCIND:0x5B			
Field Name	**Bits**	**Default**	**Description**
DmaFixRelaxOrder	0	0x0	
DmaForceSnoop	1	0x0	
DmaFixAttrEn	2	0x0	
P2pDis	3	0x0	
BMSetDis	7	0x0	
XactOrder	8	0x1	
BlockNonSp	9	0x0	
BlockSnoop	10	0x0	
MstRelaxOrder	11	0x0	
MstRelaxOrderEn	12	0x0	
MstNSoopEn	13	0x0	
ExtDevPlug	16	0x0	
ExtDevCsrEn	17	0x0	
CsrEnable	18	0x0	
IntSelMod	19	0x0	
SetPowEn	20	0x0	

StrapsOutputMux_0 - RW - 32 bits - NBMISCIND:0x60			
Field Name	**Bits**	**Default**	**Description**
StrapsOutputMux_0	31:0	0x0	Registered straps from strap block.
StrapsOutputMux_0			

StrapsOutputMux_1 - RW - 32 bits - NBMISCIND:0x61			
Field Name	**Bits**	**Default**	**Description**
StrapsOutputMux_1	31:0	0x0	Registered straps from strap block.
StrapsOutputMux_1			

StrapsOutputMux_2 - RW - 32 bits - NBMISCIND:0x62			
Field Name	**Bits**	**Default**	**Description**
StrapsOutputMux_2	31:0	0x0	Registered straps from strap block.
StrapsOutputMux_2			

StrapsOutputMux_3 - RW - 32 bits - NBMISCIND:0x63

Field Name	Bits	Default	Description
StrapsOutputMux_3	31:0	0x0	Registered straps from strap block.
StrapsOutputMux_3			

StrapsOutputMux_4 - RW - 32 bits - NBMISCIND:0x64

Field Name	Bits	Default	Description
StrapsOutputMux_4	31:0	0x0	Registered straps from strap block.
StrapsOutputMux_4			

StrapsOutputMux_5 - R - 32 bits - NBMISCIND:0x65

Field Name	Bits	Default	Description
Spare	13:0	0x3400	
GPIO_GRP_SEL	15:14	0x0	
DEBUG_TESTMUX	21:16	0x0	
DEBUG_TESTSEL	27:22	0x5	
DEBUG_MEM_A_ENABLE	28	0x0	
STRAP_DEBUG_ENABLE	29	0x0	
EEP_TEST_DEBUG_BUS_EN	30	0x0	
EEP_IO_PLLS_STRAP_EN	31	0x0	
StrapsOutputMux_5			

StrapsOutputMux_6 - RW - 32 bits - NBMISCIND:0x66

Field Name	Bits	Default	Description
Enable_Pattern_Detector	0	0x0	
B_PRX_TOGGLE_EN	1	0x0	
B_PRX_PDNB	2	0x0	
B_PTX_PDNB	3	0x0	
STRAP_BIF_SYMALIGN_DIS_ELIDLE_GPPSB	4	0x1	
STRAP_BIF_SYMALIGN_MODE_GPPSB	5	0x1	
STRAP_BIF_ELAST_WATERMARK_GPPSB	7:6	0x0	
STRAP_BIF_TEST_TOGGLE_MODE_GFX	8	0x0	
STRAP_BIF_TEST_TOGGLE_MODE_GPPSB	9	0x0	
STRAP_BIF_BYPASS_SCRAMBLER_GPPSB	10	0x0	
STRAP_PHY_RX_INCAL_FORCE_GPPSB	11	0x0	
STRAP_BIF_SKIP_INTERVAL_SB	14:12	0x0	
STRAP_BIF_EXIT_LATENCY_SB	18:15	0x0	
STRAP_BIF_REVERSE_LC_LANES_SB	19	0x0	
STRAP_BIF_REVERSE_LANES_SB	20	0x0	
STRAP_BIF_REVERSE_ALL_GPPSB	21	0x0	
STRAP_BIF_FTS_yTSx_COUNT_SB	23:22	0x0	
STRAP_BIF_SHORT_yTSx_COUNT_SB	25:24	0x0	
STRAP_BIF_MED_yTSx_COUNT_SB	27:26	0x0	

STRAP_BIF_LONG_yTSx_COUNT_SB	29:28	0x0	
STRAP_BIF_BACKGROUND_IMP_CAL_GPPSB	30	0x0	
INCAL_STRAP_GPPSB	31	0x0	
StrapsOutputMux_6			

StrapsOutputMux_7 - RW - 32 bits - NBMISCIND:0x67			
Field Name	**Bits**	**Default**	**Description**
STRAP_BIF_BYPASS_RCVR_DET_SB	0	0x0	
STRAP_BIF_COMPLIANCE_DIS_SB	1	0x0	
STRAP_BIF_FORCE_COMPLIANCE_SB	2	0x0	
STRAP_BIF_FORCE_COMPLIANCE_GPP	3	0x0	
STRAP_BIF_LINK_CONFIG_GPPSB	7:4	0x4	
B_P90PLL_IBIAS_RD_GPPSB	9:8	0x1	
STRAP_BIF_RXC_THRESH	11:10	0x0	
spare_11	12	0x0	
STRAP_BIF_PHY_RCVRDET_3NF_GPPSB	13	0x1	
B_P90RX_INCAL_FORCE_GPPSB	14	0x0	
B_P90RX_CRFR_GPPSB	20:15	0x0	
B_P90RX_CRPHSIZE_GPPSB	22:21	0x2	
B_P90RX_CRFR_ON_GPPSB	23	0x1	
B_P90RX_CRFRSIZE_GPPSB	25:24	0x0	
B_P90RX_CLKG_EN_GPPSB	26	0x1	
B_PTX_PWRS_ENB_GPPSB	27	0x1	
B_PRX_LBACK_EN_GFX	28	0x0	
B_PRX_LBACK_EN_GPPSB	29	0x0	
B_P90RX_CROUT_SEL	30	0x1	
B_P90PLL_IBIAS_SEL_GPPSB	31	0x1	
StrapsOutputMux_7			

StrapsOutputMux_8 - RW - 32 bits - NBMISCIND:0x68			
Field Name	**Bits**	**Default**	**Description**
STRAP_INC_PLLCAL_PHASE	3:0	0x0	
B_PTX_DEEMPH_EN_GPPSB	4	0x1	
B_P90TX_DRV_STR_GPPSB	6:5	0x1	
B_P90TX_DEEMPH_STR_GFX	8:7	0x1	
B_P90TX_DEEMPH_STR_GPPSB	10:9	0x1	
B_P90TX_CLKG_EN_GPPSB	11	0x1	
B_P90RX_CRFR_BPASS_GFX	12	0x0	
B_P90RX_CRFR_BPASS_GPPSB	13	0x0	
B_P90PLL_FASTEN_GFX	14	0x1	
B_P90PLL_FASTEN_GPPSB	15	0x1	
B_P90RX_INCAL_GPPSB	23:16	0x0	
B_P90PLL_CLKF_GPPSB	30:24	0x7	
STRAP_BIF_BACKGROUND_IMP_CAL_GFX	31	0x0	
StrapsOutputMux_8			

StrapsOutputMux_9 - RW - 32 bits - NBMISCIND:0x69			
Field Name	**Bits**	**Default**	**Description**
B_P90PLL_IBIAS_GPPSB	9:0	0x0	
B_P90RX_CRCTRL_GPPSB	16:10	0x0	
B_P90RX_CRCTRL_BPASS_GPPSB	17	0x0	
B_P90PLL_CLKR_GPPSB	19:18	0x0	
B_P90PLL_RESET_GPPSB	20	0x0	
B_P90PLL_RESET_EN_GPPSB	21	0x0	
B_P90PLL_TEST_GPPSB	22	0x0	
STRAP_BIF_PAD_TX_MANUAL_IMPED ANCE_GPPSB	26:23	0x0	
STRAP_BIF_PAD_RX_MANUAL_IMPED ANCE_GPPSB	30:27	0x0	
INCAL_DONE_CONTROL	31	0x0	
StrapsOutputMux_9			

StrapsOutputMux_A - RW - 32 bits - NBMISCIND:0x6A			
Field Name	**Bits**	**Default**	**Description**
StrapsOutputMux_A	31:0	0x0	Registered straps from strap block.
StrapsOutputMux_A			

StrapsOutputMux_B - RW - 32 bits - NBMISCIND:0x6B			
Field Name	**Bits**	**Default**	**Description**
StrapsOutputMux_B	31:0	0x0	Registered straps from strap block.
StrapsOutputMux_B			

StrapsOutputMux_C - RW - 32 bits - NBMISCIND:0x6C			
Field Name	**Bits**	**Default**	**Description**
StrapsOutputMux_C	31:0	0x0	Registered straps from strap block.
StrapsOutputMux_C			

StrapsOutputMux_D - RW - 32 bits - NBMISCIND:0x6D			
Field Name	**Bits**	**Default**	**Description**
StrapsOutputMux_D	31:0	0x0	Registered straps from strap block.
StrapsOutputMux_D			

StrapsOutputMux_E - RW - 32 bits - NBMISCIND:0x6E			
Field Name	**Bits**	**Default**	**Description**
StrapsOutputMux_E	31:0	0x0	Registered straps from strap block.
StrapsOutputMux_E			

StrapsOutputMux_F - RW - 32 bits - NBMISCIND:0x6F			
Field Name	**Bits**	**Default**	**Description**
StrapsOutputMux_F	31:0	0x0	Registered straps from strap block.
StrapsOutputMux_F			

scratch_0 - RW - 32 bits - NBMISCIND:0x70			
Field Name	**Bits**	**Default**	**Description**
scratch_0	31:0	0x0	

scratch_1 - RW - 32 bits - NBMISCIND:0x71			
Field Name	**Bits**	**Default**	**Description**
scratch_1	31:0	0x0	

scratch_2 - RW - 32 bits - NBMISCIND:0x72			
Field Name	**Bits**	**Default**	**Description**
scratch_2	31:0	0x0	

scratch_3 - RW - 32 bits - NBMISCIND:0x73			
Field Name	**Bits**	**Default**	**Description**
scratch_3	31:0	0x0	

SCRATCH_4 - RW - 32 bits - NBMISCIND:0x74			
Field Name	**Bits**	**Default**	**Description**
SCRATCH_4	31:0	0x0	All of the bits in this register can be written to and read from, but it does not control anything.
SCRATCH_4			

SCRATCH_5 - RW - 32 bits - NBMISCIND:0x75			
Field Name	**Bits**	**Default**	**Description**
SCRATCH_5	31:0	0x0	All of the bits in this register can be written to and read from, but it does not control anything.
SCRATCH_5			

SCRATCH_6 - RW - 32 bits - NBMISCIND:0x76			
Field Name	**Bits**	**Default**	**Description**
SCRATCH_6	31:0	0x0	All of the bits in this register can be written to and read from, but it does not control anything.
SCRATCH_6			

SCRATCH_7 - RW - 32 bits - NBMISCIND:0x77			
Field Name	**Bits**	**Default**	**Description**
SCRATCH_7	31:0	0x0	All of the bits in this register can be written to and read from, but it does not control anything.
SCRATCH_7			

SCRATCH_8 - RW - 32 bits - NBMISCIND:0x78			
Field Name	**Bits**	**Default**	**Description**
SCRATCH_8	31:0	0x0	All of the bits in this register can be written to and read from, but it does not control anything.
SCRATCH_8			

SCRATCH_9 - RW - 32 bits - NBMISCIND:0x79			
Field Name	**Bits**	**Default**	**Description**
SCRATCH_9	31:0	0x0	All of the bits in this register can be written to and read from, but it does not control anything.
SCRATCH_9			

SCRATCH_A - RW - 32 bits - NBMISCIND:0x7A			
Field Name	**Bits**	**Default**	**Description**
SCRATCH_A	31:0	0x0	All of the bits in this register can be written to and read from, but it does not control anything.
SCRATCH_A			

DFT_SPARE - RW - 32 bits - NBMISCIND:0x7F			
Field Name	**Bits**	**Default**	**Description**
DFT_SPARE	31:0	0x0	

HTIU_CNTL_1 - RW - 32 bits - HTIUNBIND:0x0			
Field Name	**Bits**	**Default**	**Description**
HTIU_CONTROL_FIELDS	31:0	0x0	Reserved
HTIU control 1			

HTIU_CNTL_2 - RW - 32 bits - HTIUNBIND:0x1			
Field Name	**Bits**	**Default**	**Description**
HTIU_CONTROL_FIELDS	31:0	0x0	Reserved
HTIU control 2			

HTIU_PERF_CNTL - RW - 32 bits - HTIUNBIND:0x2			
Field Name	**Bits**	**Default**	**Description**
See register information below			

HTIU_PERF_EVENT_0	7:0	0x0	Select HTIU performance counter event 0

Select HTIU performance counter event 0
1 - Clocks
2 - Number of HT posted writes
3 - Number of HT non-posted writes
4 - Number of HT reads
5 - Command bus utilization between lra and ht_ioc_master
6 - Data bus utilization between lra and ht_ioc_master
7 - Number of HT read responses
8 - Number of HT tgtdone
9 - Clocks that posted write buffer is full
10 - Clocks that non-posted write buffer is full
11 - Number of times posted writes were split into multiple transactions
12 - Number of times non-posted writes were split into multiple transactions
13 - Clocks that ht_ioc_master stalled due to a lack of free command buffers in ioc
14 - Number of times a non-posted memory write was converted into a posted memory write
15 - Clocks that non-posted state machine was busy
16 - Clocks that response state machine was busy doing read response
17 - Clocks that response state machine was busy doing tgtdone
18 - Clocks that ht_ioc_master was idle
19 - Number of SCAS writes
20 - Number of clock cycles for which LDTSTOP is de-asserted i.e. LDTSTOP=1
21 - Number of HT upstream request (read/write)
22 - Number of HT upstream response (to K8)
23 - Number of HT upstream GFX request (read/write)
24 - Number of HT upstream DISP request (read)
25 - Number of HT upstream BIF request (read/write)
26 - Number of HT upstream Ext GFX request (read/write)
27 - Number of HT upstream SB request (read/write)
28 - Number of HT upstream PCIE3 request (read/write)
29 - Number of HT upstream PCIE4 request (read/write)
30 - Number of HT upstream PCIE5 request (read/write)
31 - Number of HT upstream PCIE6 request (read/write)
32 - Number of HT upstream PCIE7 request (read/write)
33 - Number of HT upstream IOC request (all ioc clients read/write)
34 - Number of HT upstream Target Done response (to K8)
35 - Number of HT upstream Read response (to K8)
36 - Number of HT upstream Posted request (write)
37 - Number of HT upstream Non-Posted request (read)
38 - Number of HT upstream ISOC request (read)
39 - Number of HT upstream Read request
40 - Number of HT upstream Byte Write request
41 - Number of GFX request accepted
42 - Clocks that GFX request waited on the interface
43 - Number of DISP request accepted
44 - Clocks that DISP request waited on the interface
45 - Number of IOC request accepted
46 - Clocks that IOC request waited on the interface
47 - Number of IOC response accepted
48 - Clocks that IOC response waited on the interface
49 - Number of HT upstream GFX DW optimized write
50 - Number of HT upstream IOC optimized byte write
51 - Number of HT upstream Posted request (write) with size =< 16 bytes
52 - Number of HT upstream Posted request (write) with size =< 32 bytes and > 16 bytes
53 - Number of HT upstream Posted request (write) with size =< 48 bytes and > 32 bytes
54 - Number of HT upstream Posted request (write) with size =< 64 bytes and > 48 bytes
55 - Number of HT upstream Non-Posted request (read) with size =< 16 bytes
56 - Number of HT upstream Non-Posted request (read) with size =< 32 bytes and > 16 bytes
57 - Number of HT upstream Non-Posted request (read) with size =< 48 bytes and > 32 bytes
58 - Number of HT upstream Non-Posted request (read) with size =< 64 bytes and > 48 bytes
59 - Number of HT upstream ISOC request (read) with size =< 16 bytes
60 - Number of HT upstream ISOC request (read) with size =< 32 bytes and > 16 bytes
61 - Number of HT upstream ISOC request (read) with size =< 48 bytes and > 32 bytes
62 - Number of HT upstream ISOC request (read) with size =< 64 bytes and > 48 bytes
63 - Number of HT upstream Read response (to K8) with size =< 16 bytes
64 - Number of HT upstream Read response (to K8) with size =< 32 bytes and > 16 bytes
65 - Number of HT upstream Read response (to K8) with size =< 48 bytes and > 32 bytes
66 - Number of HT upstream Read response (to K8) with size =< 64 bytes and > 48 bytes
67 - Number of HT upstream Byte Write request with size = 16 bytes
68 - Number of HT upstream Byte Write request with size = 32 bytes
69 - Number of HT upstream Ext GFX Coherent request (read/write)
70 - Number of HT upstream Ext GFX Non-Coherent request (read/write)
71 - Number of HT upstream SB + BIF + PCIE[7:3] Coherent request (read/write)
72 - Number of HT upstream SB + BIF + PCIE[7:3] Non-Coherent request (read/write)
73 - Clock that Upstream state machines are IDLE
74 - 79 - Reserved
80 - Response Command Bus utilization between lra and resp_path
81 - Response Data Bus utilization between lra and resp_path
82 - Number of MC dma responses
83 - Number of IOC dma responses
84 - Number of merged MC dma responses
85 - Number of MC 64-byte responses
86 - Number of MC 32-byte responses
87 - Number of MC 16-byte responses
88 - Number of IOC 64-byte responses
89 - Number of IOC 48-byte responses
90 - Number of IOC 32-byte responses
91 - Number of IOC 16-byte responses
92 - Clocks resp_path is idle
93 - 119 Reserved
120 - Master writes with 0->4 bytes of data (including mask)
121 - Master writes with 5->8 bytes of data (including mask)
122 - Master writes with 9->16 bytes of data (including mask)
123 - Master writes with 17->32 bytes of data (including mask)
124 - Master writes with 33->64 bytes of data (including mask)
125 - Master reads of 0->4 bytes
126 - Master reads of 5->8 bytes
127 - Master reads of 9->16 bytes

HTIU_PERF_EVENT_1	15:8	0x0	More performance counter events 128 - Master reads of 17->32 bytes 129 - Master reads of 33->64 bytes 130 - HTiu_CT_RPBusy: clock gating signal is Busy 131 - HTiu_CT_HTMBusy: clock gating signal is Busy 132 - HTiu_CT_RPIdle: clock gating signal is Idle 133 - HTiu_CT_HTMIdle: clock gating signal is Idle 134 - HTiu_CT_FCBIdle: clock gating signal is Idle 135 - HTiu_CT_FCBBusy: clock gating signal is Busy 136 - HTiu_CT_GCMIdle: clock gating signal is Idle 137 - HTiu_CT_GCMBusy: clock gating signal is Busy 138 - HTiu_CT_IOCMasterBusy: clock gating signal is Busy 139 - HTiu_CT_IOCBusy: clock gating signal is Busy 140 - HTiu_CT_IOCIdle: clock gating signal is Idle 141 - HTiu_CT_MCBusy: clock gating signal is Busy 142 - HTiu_CT_MCIdle: clock gating signal is Idle 143 - 149 - Reserved 150 - PerfCnt_SrcTag0UID1Rsp: indicates receipt of Response for UnitID 1 and SrcTag 0 151 - PerfCnt_SrcTag0UID2Rsp: indicates receipt of Response for UnitID 2 and SrcTag 0 152 - PerfCnt_SrcTag0UID3Rsp: indicates receipt of Response for UnitID 3 and SrcTag 0 153 - PerfCnt_SrcTag0UID4Rsp: indicates receipt of Response for UnitID 4 and SrcTag 0 154 - PerfCnt_SrcTag0UID5Rsp: indicates receipt of Response for UnitID 5 and SrcTag 0 155 - PerfCnt_SrcTag0UID6Rsp: indicates receipt of Response for UnitID 6 and SrcTag 0 156 - PerfCnt_SrcTag0UID7Rsp: indicates receipt of Response for UnitID 7 and SrcTag 0 157 - PerfCnt_SrcTag0UID8Rsp: indicates receipt of Response for UnitID 8 and SrcTag 0 158 - PerfCnt_SrcTag0UID9Rsp: indicates receipt of Response for UnitID 9 and SrcTag 0 159 - PerfCnt_SrcTag0UID10Rsp: indicates receipt of Response for UnitID 10 and SrcTag 0 160 - PerfCnt_SrcTag0UID11Rsp: indicates receipt of Response for UnitID 11 and SrcTag 0 161 - PerfCnt_SrcTag0UID12Rsp: indicates receipt of Response for UnitID 12 and SrcTag 0 162 - 223 - Reserved 224 - PerfCnt_read_GFX: DMA Read Request from GFX (to calculate per-request read latency) 225 - PerfCnt_read_DISP: DMA Read Request from DISP (to calculate per-request read latency) 226 - PerfCnt_read_BIF: DMA Read Request from BIF (to calculate per-request read latency) 227 - PerfCnt_read_PCIEGFX0: DMA Read Request from PCIEGFX0 (to calculate per-request read latency) 228 - PerfCnt_read_PCIEGFX1: DMA Read Request from PCIEGFX1 (to calculate per-request read latency) 229 - PerfCnt_read_PCIE4: DMA Read Request from PCIE4 (to calculate per-request read latency) 230 - PerfCnt_read_PCIE5: DMA Read Request from PCIE5 (to calculate per-request read latency) 231 - PerfCnt_read_PCIE6: DMA Read Request from PCIE6 (to calculate per-request read latency) 232 - PerfCnt_read_PCIE7: DMA Read Request from PCIE7 (to calculate per-request read latency) 233 - PerfCnt_read_SB: DMA Read Request from SB (to calculate per-request read latency) 234 - PerfCnt_read_AZALIA: DMA Read Request from AZALIA (to calculate per-request read latency) 235 - upto 255 Reserved Latency_240 - Counts the number of outstanding GFX Requests by adding all allocated tags Latency_241 - Counts the number of outstanding DSP Requests by adding all allocated tags Latency_242 - Counts the number of outstanding BIF Requests by adding all allocated tags Latency_243 - Counts the number of outstanding GFX0 Requests by adding all allocated tags Latency_244 - Counts the number of outstanding GFX1 Requests by adding all allocated tags Latency_245 - Counts the number of outstanding PCIE1X0 Requests by adding all allocated tags Latency_246 - Counts the number of outstanding PCIE1X1 Requests by adding all allocated tags Latency_247 - Counts the number of outstanding PCIE1X2 Requests by adding all allocated tags Latency_248 - Counts the number of outstanding PCIE1X3 Requests by adding all allocated tags Latency_249 - Counts the number of outstanding PCIESB Requests by adding all allocated tags Latency_250 - Counts the number of outstanding AZALIA Requests by adding all allocated tags Latency_251 - upto 255 Reserved
HTIU_PERF_COUNT_UPPER_0 (R)	23:16	0x0	Upper 8 bits of HTIU performance counter 0
HTIU_PERF_COUNT_UPPER_1 (R)	31:24	0x0	Upper 8 bits of HTIU performance counter 1
HTIU performance control			

HTIU_PERF_COUNT_0 - R - 32 bits - HTIUNBIND:0x3			
Field Name	**Bits**	**Default**	**Description**
HTIU_PERF_COUNT_0	31:0	0x0	Lower 32 bits of HTIU performance counter 0
HTIU performance counter 0			

HTIU_PERF_COUNT_1 - R - 32 bits - HTIUNBIND:0x4			
Field Name	**Bits**	**Default**	**Description**
HTIU_PERF_COUNT_1	31:0	0x0	Lower 32 bits of HTIU performance counter 1
HTIU performance counter 1			

HTIU_DEBUG - RW - 32 bits - HTIUNBIND:0x5			
Field Name	**Bits**	**Default**	**Description**
HTIU_DEBUG	31:0	0x0	Bits [31:5]=Reserved Bit [4]=Enable identifying GFX requests as GSM requests Bit [3]=Enable blocking of AllowLdtStop during HT link synchronization Bit [2]=Enable GSM mode fix to wait for outstanding reads to complete before allowing LDTSTOP to be asserted Bit [1]=Use 500ns LDTSTOP reconnection timer Bit [0]=Use 1.0us LDTSTOP reconnection timer
HTIU debug			

HTIU_DOWNSTREAM_CONFIG - RW - 32 bits - HTIUNBIND:0x6			
Field Name	**Bits**	**Default**	**Description**

HTdSafeIssue	0	0x1	Causes outstanding non-posted transactions to block the posted channel. It should be cleared to avoid a deadlock scenario
			  0=PW before NP done
			  1=PW after NP done

HTdPStreamEn	1	0x0	Downstream posted-write streaming
			  0=Disabled
			  1=Enable for higher performance

CfgHTiuRdRspPassPWMode	3:2	0x0	PassPW for upstream read responses
			  0=00 - From request packet
			  1=01 - From IOC
			  2=10 - Always 0
			  3=11 - Always 1

CfgHTiuTgtDonePassPWMode	5:4	0x0	PassPW for upstream tgtdone
			  0=00 - From request packet
			  1=01 - Normally 1 but 0 for I/O cycle
			  2=10 - Always 0
			  3=11 - Always 1

CfgHTiuReqPassPWMode	7:6	0x0	PassPW for downstream requests to IOC
			  0=00 - From request packet
			  1=01 - Reserved
			  2=10 - Always 0
			  3=11 - Always 1

CfgHTiuDisableNPDWait	8	0x0	This bit should always be set to 0 for proper operation
CfgHTiuPDStage2En	9	0x0	Enables larger buffer for downstream posted data and higher performance
CfgHTiuLockIOCArb	10	0x0	Lock IOC arbiter. Should always be set to 0
CfgHTiuHtdNoErr	11	0x0	Prevents the chipset from sending error bits in upstream responses to the CPU
CfgHtiuTxMaxRspCnt	12	0x0	Enables infinite response buffers. Setting this bit wastes upstream bandwidth
CfgHTiuLargeRspCnt	13	0x0	Enables 63 response buffer mode
ReqCompatModeDis	14	0x0	Disables Compat bit decoding in htiu. Should be set to 0 for proper operation
FIDStpGntDetect	15	0x0	Enables wait for display on StpGnt with FID SMAF detection. Should be disabled if no internal gfx
C3StpGntDetect	16	0x0	Enables wait for display on StpGnt with C3 SMAF detection. Should be disabled if no internal gfx
AllowNPPassPW	17	0x0	Enables PassPW functionality in non-posted transactions

	18	0x1	
FastNPAvail	18	0x1	Enables faster turnaround of NP buffer availability. Should be set to 1
GCMDelay	21:19	0x2	Delay between back-to-back transactions issued by GCM. Should not be set lower than 0x2
GCMPCDelay	24:22	0x2	Delay between back-to-back PC transactions issued by GCM. Should not be set lower than 0x2
DispIntAck	25	0x0	Ignores ACK from Display on StpGnt wait and generate ACK internally
PCIE_HT_NP_MEM_WRITE	26	0x0	Enables NP protocol over PCIE for memory-mapped writes targeting LPC. Set this bit to avoid a deadlock condition
SCAS_EN	27	0x0	Enables SCAS feature. All traffic between 1 and 2GB is mapped onto a special 64 byte storage space. Should be used for testing only
DbgCntrMode	28	0x0	Enables rotating htiu debug bus
Reserved_31_29	31:29	0x0	Bit [29]=Enables wider read to write pointer spacing in the CFF. This requires a link freq/width change Bit [30]=Enables a fix for tagging downstream NP requests Bit [31]=Enables HT Link operation in 600 MHz mode. Transmit Clock: 600 MHz; LCLK: 150 MHz 1=Enable 0=Disable (normal operating modes for link)
HTIU downstream configuration			

HTIU_UPSTREAM_CONFIG_0 - RW - 32 bits - HTIUNBIND:0x7			
Field Name	**Bits**	**Default**	**Description**
ioc_bw_opt_en	0	0x0	Optimizes IOC byte write by detecting Consecutive DW mask and translate the request to DW write 0=Disable 1=Enable
delay_STPCLK_en	1	0x1	Holds off upstream SMC STPCLK for FID message until DISP_ALLOW_LDTSTOP is asserted. During this time, only DISP can issue request 0=Disable 1=Enable
delay_FID_en	2	0x1	Holds off upstream SMC FID message until DISP_ALLOW_LDTSTOP is asserted. This bit should always be set to 0 0=Disable 1=Enable
c3_delay_gfx_count_en	3	0x1	Blocks off GFX client for only 128 cycles when holding SMC STPCLK for FID message 0=Disable 1=Enable
ups_igp_arb_en	4	0x0	Selects between GCM/IGP arbitration mode 0=GCM Mode (default) 1=IGP Mode
IGP_ALL_en	5	0x0	Selects between IGP AFC/ALL arbitration mode 0=IGP_AFC Mode 1=IGP_ALL Mode
IGP_ALL_PFC_en	6	0x1	Enables Early Posted Buffer check in IGP_ALL mode 0=Disable 1=Enable
GCM_flush_urgent_np_disp	7	0x1	Flush all Non-Posted DISP request first when received DISP urgent signal. This bit should always be set to 1. 0=Disable 1=Enable

Disp_Rsv_BufCnt	10:8	0x1	Number of Non-Posted buffer reserved for DISP request Min=0 Max=7 Note The default is 1.

drop_zero_mask_req	11	0x0	Drop byte write request that have all zero mask
			  0=Disable
			  1=Enable

disp_delay_en	12	0x0	Blocks off DISP request after N request sends for T amount of cycles to allow other client to process their request
			  0=Disable
			  1=Enable

spare_15_13	15:13	0x0	Bit [13]=Enable qualification of DISP urgent signal with its RTS signal Bit [14]=Force DISP request to be always urgent
disp_delay_cnt	23:16	0x10	T amount of Cycle that DISP request will wait. (Each unit here represent 16 LCLK)
disp_req_cnt	29:24	0x7	N DISP request send before wait
spare_31_30	31:30	0x0	Bit [30]=Enable Normal UnitID for STPCLK (FID or SB-Th) message Bit [31]=GFX Write Request PassPW enable
HTIU upstream configuration 0			

HTIU_UPSTREAM_CONFIG_1 - RW - 32 bits - HTIUNBIND:0x8			
Field Name	**Bits**	**Default**	**Description**
NP_DISP_urgt_pri	3:0	0x1	DISP urgent request priority in GCM Non-Posted arbitration (High = 0, Low = e, Don't care = f, Default = 1)
NP_DISP_tout_pri	7:4	0x5	DISP timeout request priority in GCM Non-Posted arbitration (High = 0, Low = e, Don't care = f, Default = 5)
NP_DISP_norm_pri	11:8	0x9	DISP normal request priority in GCM Non-Posted arbitration (High = 0, Low = e, Don't care = f, Default = 9)
NP_GFX_urgt_pri	15:12	0x2	GFX urgent request priority in GCM Non-Posted arbitration (High = 0, Low = e, Don't care = f, Default = 2)
NP_GFX_tout_pri	19:16	0x6	GFX timeout request priority in GCM Non-Posted arbitration (High = 0, Low = e, Don't care = f, Default = 6)
NP_GFX_norm_pri	23:20	0xa	GFX normal request priority in GCM Non-Posted arbitration (High = 0, Low = e, Don't care = f, Default = a)
NP_IOC_tout_pri	27:24	0x4	IOC timeout request priority in GCM Non-Posted arbitration (High = 0, Low = e, Don't care = f, Default = 4)
NP_IOC_norm_pri	31:28	0x8	IOC normal request priority in GCM Non-Posted arbitration (High = 0, Low = e, Don't care = f, Default = 8)
HTIU upstream configuration 1			

HTIU_UPSTREAM_CONFIG_2 - RW - 32 bits - HTIUNBIND:0x9			
Field Name	**Bits**	**Default**	**Description**
NP_RR_0_pri	3:0	0xf	Round Robin 0 or Efficient 0 priority in GCM Non-Posted arbitration (High = 0, Low = e, Don't care = f, Default = f)
NP_RR_1_pri	7:4	0x3	Round Robin 1 or Efficient 1 priority in GCM Non-Posted arbitration (High = 0, Low = e, Don't care = f, Default = 3)
NP_RR_2_pri	11:8	0x7	Round robin 2 or Efficient 2 priority in GCM Non-Posted arbitration (High = 0, Low = e, Don't care = f, Default = 7)

NP_rr_1_en	12	0x0	Enables NP Round Robin 1 Arbiter
			Note: The RR and EFF arbiter cannot be enabled at the same time.
			  0=Disable
			  1=Enable

NP_rr_2_en	13	0x0	Enables NP Round Robin 2 Arbiter
			Note: The RR and EFF arbiter cannot be enabled at the same time.
			  0=Disable
			  1=Enable

NP_Eff_1_en	14	0x0	Enables NP Efficiency 1 Arbiter
			Note: The RR and EFF arbiter cannot be enabled at the same time.
			  0=Disable
			  1=Enable

NP_Eff_2_en	15	0x0	Enable NP Efficiency 2 Arbiter
			Note: The RR and EFF arbiter cannot be enabled at the same time.
			  0=Disable
			  1=Enable

NP_rr_1_len	19:16	0xb	NP Round Robin 1 or NP Efficiency 1 pattern length
NP_rr_2_len	23:20	0xb	NP Round Robin 2 or NP Efficiency 2 pattern length
HTIU upstream configuration 2			

HTIU_UPSTREAM_CONFIG_3 - RW - 32 bits - HTIUNBIND:0xA			
Field Name	**Bits**	**Default**	**Description**

NP_rr_1_pat	31:0	0xaa5550 0	NP Round Robin 1 or Efficiency 1 select pattern
			(Every 2 bits represent 1 pattern)
			  00=RR order is Client A, B, C, D
			  01=RR order is Client B, C, D, A
			  10=RR order is Client C, D, A, B
			  11=RR order is Client D, A, B, C

HTIU upstream configuration 3			

HTIU_UPSTREAM_CONFIG_4 - RW - 32 bits - HTIUNBIND:0xB			
Field Name	**Bits**	**Default**	**Description**

NP_rr_2_pat	31:0	0xaa5550 0	NP Round Robin 2 or Efficiency 2 select pattern
			(Every 2 bits represent 1 pattern)
			  00=RR order is Client A, B, C, D
			  01=RR order is Client B, C, D, A
			  10=RR order is Client C, D, A, B
			  11=RR order is Client D, A, B, C

HTIU upstream configuration 4			

HTIU_UPSTREAM_CONFIG_5 - RW - 32 bits - HTIUNBIND:0xC			
Field Name	Bits	Default	Description
P_GFX_urgt_pri	3:0	0x2	GFX urgent request priority in GCM Posted arbitration (High = 0, Low = e, Don't care = f, Default = 2)
P_GFX_tout_pri	7:4	0x6	GFX timeout request priority in GCM Posted arbitration (High = 0, Low = e, Don't care = f, Default = 6)
P_GFX_norm_pri	11:8	0xa	GFX normal request priority in GCM Posted arbitration (High = 0, Low = e, Don't care = f, Default = a)
P_IOC_tout_pri	15:12	0x4	IOC timeout request priority in GCM Posted arbitration (High = 0, Low = e, Don't care = f, Default = 4)
P_IOC_norm_pri	19:16	0x8	IOC normal request priority in GCM Posted arbitration (High = 0, Low = e, Don't care = f, Default = 8)
P_RR_0_pri	23:20	0xf	Round Robin 0 or Efficent 0 priority in GCM Posted arbitration (High = 0, Low = e, Don't care = f, Default = f)
P_RR_1_pri	27:24	0x3	Round Robin 1 or Efficent 1 priority in GCM Posted arbitration (High = 0, Low = e, Don't care = f, Default = 3)
P_RR_2_pri	31:28	0x7	Round robin 2 or Efficent 2 priority in GCM Posted arbitration (High = 0, Low = e, Don't care = f, Default = 7)
HTIU upstream configuration 5			

HTIU_UPSTREAM_CONFIG_6 - RW - 32 bits - HTIUNBIND:0xD			
Field Name	Bits	Default	Description
P_rr_1_en	0	0x0	Enables P Round Robin 1 Arbiter Note: The RR and EFF arbiter cannot be enabled at the same time. 0=Disable 1=Enable
P_Eff_1_en	1	0x0	Enables P Efficiency 1 Arbiter Note: The RR and EFF arbiter cannot be enabled at the same time. 0=Disable 1=Enable
P_rr_1_len	7:4	0xb	P Round Robin 1 or P Efficiency 1 pattern length
P_rr_1_client_a	11:8	0x6	NP/P Round Robin 1 Client A ID 0=DISP Urgent, 1=DISP Timeout, 2=DISP Normal 3=GFX Urgent, 4=GFX Timeout, 5=GFX Normal 6=IOC Timeout, 7=IOC Normal
P_rr_1_client_b	15:12	0x1	NP/P Round Robin 1 Client B ID 0=DISP Urgent, 1=DISP Timeout, 2=DISP Normal 3=GFX Urgent, 4=GFX Timeout, 5=GFX Normal 6=IOC Timeout, 7=OC Normal
P_rr_1_client_c	19:16	0x4	NP/P Round Robin 1 Client C ID 0=DISP Urgent, 1=DISP Timeout, 2=DISP Normal 3=GFX Urgent, 4=GFX Timeout, 5=GFX Normal 6=IOC Timeout, 7=IOC Normal
P_rr_1_client_d	23:20	0xf	NP/P Round Robin 1 Client D ID 0=DISP Urgent, 1=DISP Timeout, 2=DISP Normal 3=GFX Urgent, 4=GFX Timeout, 5=GFX Normal 6=IOC Timeout, 7=IOC Normal
HTIU upstream configuration 6			

HTIU_UPSTREAM_CONFIG_7 - RW - 32 bits - HTIUNBIND:0xE			
Field Name	**Bits**	**Default**	**Description**
P_rr_1_pat	31:0	0xaa5500	P Round Robin 1 or Efficiency 1 select pattern (Every 2 bits represent 1 pattern) 00=RR order is Client A, B, C, D 01=RR order is Client B, C, D, A 10=RR order is Client C, D, A, B 11=RR order is Client D, A, B, C
HTIU upstream configuration 7			

HTIU_UPSTREAM_CONFIG_8 - RW - 32 bits - HTIUNBIND:0xF			
Field Name	**Bits**	**Default**	**Description**
P_rr_2_en	0	0x0	Enables P Round Robin 2 Arbiter Note: The RR and EFF arbiter cannot be enabled at the same time. 0=Disable 1=Enable
P_Eff_2_en	1	0x0	Enables P Efficiency 2 Arbiter Note: The RR and EFF arbiter cannot be enabled at the same time. 0=Disable 1=Enable
P_rr_2_len	7:4	0xb	P Round Robin 2 or P Efficiency 2 pattern length
P_rr_2_client_a	11:8	0x7	NP/P Round Robin 2 Client A ID 0=DISP Urgent, 1=DISP Timeout, 2=DISP Normal 3=GFX Urgent, 4=GFX Timeout, 5=GFX Normal 6=IOC Timeout, 7=IOC Normal
P_rr_2_client_b	15:12	0x2	NP/P Round Robin 2 Client B ID 0=DISP Urgent, 1=DISP Timeout, 2=DISP Normal 3=GFX Urgent, 4=GFX Timeout, 5=GFX Normal 6=IOC Timeout, 7=IOC Normal
P_rr_2_client_c	19:16	0x5	NP/P Round Robin 2 Client C ID 0=DISP Urgent, 1=DISP Timeout, 2=DISP Normal 3=GFX Urgent, 4=GFX Timeout, 5=GFX Normal 6=IOC Timeout, 7=IOC Normal
P_rr_2_client_d	23:20	0xf	NP/P Round Robin 2 Client D ID 0=DISP Urgent, 1=DISP Timeout, 2=DISP Normal 3=GFX Urgent, 4=GFX Timeout, 5=GFX Normal 6=IOC Timeout, 7=IOC Normal
HTIU upstream configuration 8			

HTIU_UPSTREAM_CONFIG_9 - RW - 32 bits - HTIUNBIND:0x10			
Field Name	**Bits**	**Default**	**Description**
P_rr_2_pat	31:0	0xaa5500	P Round Robin 2 or Efficiency 2 select pattern (Every 2 bits represent 1 pattern) 00=RR order is Client A, B, C, D 01=RR order is Client B, C, D, A 10=RR order is Client C, D, A, B 11=RR order is Client D, A, B, C
HTIU upstream configuration 9			

HTIU_UPSTREAM_CONFIG_10 - RW - 32 bits - HTIUNBIND:0x11			
Field Name	**Bits**	**Default**	**Description**
GCM_NP_pri	2:0	0x3	GCM Non-Posted Request Priority (High = 0, Low = 6, Don't care = 7, Default = 3)
GCM_ISOC_pri	6:4	0x0	GCM Isochronous Request Priority (High = 0, Low = 6, Don't care = 7, Default = 0)
GCM_RSP_pri	10:8	0x1	GCM Response Priority (High = 0, Low = 6, Don't care = 7, Default = 1)
GCM_P_pri	14:12	0x4	GCM Posted Request Priority (High = 0, Low = 6, Don't care = 7, Default = 4)
GCM_RR_0_pri	18:16	0x2	GCM Round Robin 0 Priority (High = 0, Low = 6, Don't care = 7, Default = 2)
HTIU upstream configuration 10			

HTIU_UPSTREAM_CONFIG_11 - RW - 32 bits - HTIUNBIND:0x12			
Field Name	**Bits**	**Default**	**Description**
GCM_rr_0_en	0	0x0	Enables GCM Round Robin 0 Arbiter Note: The RR and EFF arbiter cannot be enabled at the same time. 0=Disable 1=Enable
GCM_Eff_0_en	1	0x0	Enables GCM Efficiency 0 Arbiter Note: The RR and EFF arbiter cannot be enabled at the same time. 0=Disable 1=Enable
GCM_rr_0_len	7:4	0x7	GCM Round Robin 0 or GCM Efficiency 0 pattern length
GCM_rr_0_client_a	11:8	0x1	GCM Round Robin 0 Client A ID 0=Isoc, 1=Non-Posted, 2=Response 3=Posted, 4=RR0/EFF0
GCM_rr_0_client_b	15:12	0x3	GCM Round Robin 0 Client B ID 0=Isoc, 1=Non-Posted, 2=Response, 3=Posted, 4=RR0/EFF0
GCM_rr_0_client_c	19:16	0x7	GCM Round Robin 0 Client C ID 0=Isoc, 1=Non-Posted, 2=Response, 3=Posted, 4=RR0/EFF0
GCM_rr_0_client_d	23:20	0x7	GCM Round Robin 0 Client D ID 0=Isoc, 1=Non-Posted, 2=Response, 3=Posted, 4=RR0/EFF0
HTIU upstream configuration 11			

HTIU_UPSTREAM_CONFIG_12 - RW - 32 bits - HTIUNBIND:0x13			
Field Name	**Bits**	**Default**	**Description**
GCM_rr_0_pat	31:0	0x55005500	GCM Round Robin 0 or GCM Efficiency 0 select pattern (Every 2 bits represent 1 pattern) 00=RR order is Client A, B, C, D 01=RR order is Client B, C, D, A 10=RR order is Client C, D, A, B 11=RR order is Client D, A, B, C
HTIU upstream configuration 12			

HTIU_UPSTREAM_CONFIG_13 - RW - 32 bits - HTIUNBIND:0x14			
Field Name	**Bits**	**Default**	**Description**
AFC_DISP_urgt_pri	3:0	0x1	DISP urgent request priority in IGP AFC/ALL arbitration (High = 0, Low = e, Don't care = f, Default = 1)
AFC_DISP_tout_pri	7:4	0x5	DISP timeout request priority in IGP AFC/ALL arbitration (High = 0, Low = e, Don't care = f, Default = 5)
AFC_DISP_norm_pri	11:8	0x9	DISP normal request priority in IGP AFC/ALL arbitration (High = 0, Low = e, Don't care = f, Default = 9)
AFC_GFX_urgt_pri	15:12	0x2	GFX urgent request priority in IGP AFC/ALL arbitration (High = 0, Low = e, Don't care = f, Default = 2)
AFC_GFX_tout_pri	19:16	0x6	GFX timeout request priority in IGP AFC/ALL arbitration (High = 0, Low = e, Don't care = f, Default = 6)
AFC_GFX_norm_pri	23:20	0xa	GFX normal request priority in IGP AFC/ALL arbitration (High = 0, Low = e, Don't care = f, Default = a)
AFC_IOC_tout_pri	27:24	0x4	IOC timeout request priority in IGP AFC/ALL arbitration (High = 0, Low = e, Don't care = f, Default = 4)
AFC_IOC_norm_pri	31:28	0x8	IOC normal request priority in IGP AFC/ALL arbitration (High = 0, Low = e, Don't care = f, Default = 8)
HTIU upstream configuration 13			

HTIU_UPSTREAM_CONFIG_14 - RW - 32 bits - HTIUNBIND:0x15			
Field Name	**Bits**	**Default**	**Description**
AFC_RR_0_pri	3:0	0x0	Round Robin 0 or Efficent 0 priority in IGP AFC/ALL arbitration (High = 0, Low = e, Don't care = f, Default = f)
AFC_RR_1_pri	7:4	0x3	Round Robin 1 or Efficent 1 priority in IGP AFC/ALL arbitration (High = 0, Low = e, Don't care = f, Default = 3)
AFC_RR_2_pri	11:8	0x7	Round robin 2 or Efficent 2 priority in IGP AFC/ALL arbitration (High = 0, Low = e, Don't care = f, Default = 7)
AFC_rr_0_en	12	0x0	Enables AFC/ALL Round Robin 0 Arbiter 0=Disable 1=Enable
AFC_rr_0_len	15:13	0x7	AFC/ALL Round Robin 0 or Efficiency 0 pattern length
AFC_rr_0_client_a	19:16	0x0	AFC/ALL Round Robin 0 Client A ID 0=DISP Urgent, 1=DISP Timeout, 2=DISP Normal 3=GFX Urgent, 4=GFX Timeout, 5=GFX Normal 6=IOC Timeout, 7=IOC Normal
AFC_rr_0_client_b	23:20	0x3	AFC/ALL Round Robin 0 Client B ID 0=DISP Urgent, 1=DISP Timeout, 2=DISP Normal 3=GFX Urgent, 4=GFX Timeout, 5=GFX Normal 6=IOC Timeout, 7=IOC Normal
AFC_rr_0_pat	31:24	0xf0	AFC/ALL Round Robin 0 or Efficiency 0 select pattern 0=RR order is Client A, B 1=RR order is Client B, A.
HTIU upstream configuration 14			

HTIU_UPSTREAM_CONFIG_15 - RW - 32 bits - HTIUNBIND:0x16			
Field Name	**Bits**	**Default**	**Description**
FCBBypassEn	0	0x0	This bit controls no hardware.

CRCDecodeFix	1	0x0	Enables the CRC Decoding fix
			  0=CRC Decoding fix is disabled
			  1=CRC Decoding fix is enabled

SplitTxPhyEn	2	0x0	Automatically disables the upper half of the HT transmitter when running in 8-bit output mode
			  0=In 8-bit mode the upper HT bus drives logical 0
			  1=In 8-bit mode the upper HT bus is tristated

SplitRxPhyEn	3	0x0	Automatically disables the upper half of the HT receiver when running in 8-bit input mode
			  0=In 8-bit mode, the upper HT receiver is enabled
			  1=In 8-bit mode, the upper HT receiver is disabled

TxClkGateEn	4	0x0	Dynamically gates the clock to the HT TX PHY
			  0=The clock to the HT TX PHY is always on
			  1=The clock to the HT TX PHY is shut off when LDTSTOP is asserted

HTIU_DEBUG2	31:5	0x0	This register is used to hold debug features Bit [0]=Enable GSM All mode where any DMA request will wake up the HT link (including display and graphics) Bits [26:1]=Reserved (controls no hardware)
HTIU upstream configuration 15			

HTIU_UPSTREAM_CONFIG_16 - RW - 32 bits - HTIUNBIND:0x17			
Field Name	**Bits**	**Default**	**Description**

AFC_rr_1_pat	31:0	0xaa5550 0	AFC/ALL Round Robin 1 or Efficiency 1 select pattern
			(Every 2 bits represent 1 pattern)
			  00=RR order is Client A, B, C, D
			  01=RR order is Client B, C, D, A
			  10=RR order is Client C, D, A, B
			  11=RR order is Client D, A, B, C

HTIU upstream configuration 16			

HTIU_UPSTREAM_CONFIG_17 - RW - 32 bits - HTIUNBIND:0x18			
Field Name	**Bits**	**Default**	**Description**

AFC_rr_2_en	0	0x0	Enables AFC/ALL Round Robin 2 Arbiter
			Note: The RR and EFF arbiter cannot be enabled at the same time.
			  0=Disable
			  1=Enable

AFC_Eff_2_en	1	0x0	Enables AFC/ALL Efficiency 1 Arbiter
			Note: The RR and EFF arbiter cannot be enabled at the same time.
			  0=Disable
			  1=Enable

AFC_rr_2_len	7:4	0xb	AFC/ALL Round Robin 2 or Efficiency 2 pattern length

AFC_rr_2_client_a	11:8	0x7	AFC/ALL Round Robin 2 Client A ID
			  0=DISP Urgent, 1=DISP Timeout, 2=DISP Normal
			  3=GFX Urgent, 4=GFX Timeout, 5=GFX Normal
			  6=IOC Timeout, 7=IOC Normal

AFC_rr_2_client_b	15:12	0x2	AFC/ALL Round Robin 2 Client B ID
			  0=DISP Urgent, 1=DISP Timeout, 2=DISP Normal
			  3=GFX Urgent, 4=GFX Timeout, 5=GFX Normal
			  6=IOC Timeout, 7=IOC Normal

AFC_rr_2_client_c	19:16	0x5	AFC/ALL Round Robin 2 Client C ID
			  0=DISP Urgent, 1=DISP Timeout, 2=DISP Normal
			  3=GFX Urgent, 4=GFX Timeout, 5=GFX Normal
			  6=IOC Timeout, 7=IOC Normal

AFC_rr_2_client_d	23:20	0xf	AFC/ALL Round Robin 2 Client D ID
			  0=DISP Urgent, 1=DISP Timeout, 2=DISP Normal
			  3=GFX Urgent, 4=GFX Timeout, 5=GFX Normal
			  6=IOC Timeout, 7=IOC Normal

HTIU upstream configuration 17			

HTIU_UPSTREAM_CONFIG_18 - RW - 32 bits - HTIUNBIND:0x19			
Field Name	**Bits**	**Default**	**Description**

AFC_rr_2_pat	31:0	0xaa5500 0	AFC/ALL Round Robin 2 or Efficiency 2 select pattern
			(Every 2 bits represent 1 pattern)
			  00=RR order is Client A, B, C, D
			  01=RR order is Client B, C, D, A
			  10=RR order is Client C, D, A, B
			  11=RR order is Client D, A, B, C

HTIU upstream configuration 18			

HTIU_UPSTREAM_CONFIG_19 - RW - 32 bits - HTIUNBIND:0x1A			
Field Name	**Bits**	**Default**	**Description**

IGP_ALLAFC_pri	0	0x1	Priority for AFC or ALL (request) in IGP mode
			  0=Highest
			  1=Lowest

IGP_RSP_pri	1	0x0	Priority for Response in IGP mode
			  0=Highest
			  1=Lowest

ioc_timeout_en	4	0x1	Internal IOC request timeout
			  0=Disable
			  1=Enable

gfx_timeout_en	5	0x1	Internal GFX request timeout
			  0=Disable
			  1=Enable

ioc_timeout_cnt	11:8	0x7	Internal IOC timeout counter value (each unit here represent 16 LCLK cycles)
gfx_timeout_cnt	15:12	0x7	Internal IOC timeout counter value (each unit here represent 16 LCLK cycles)

ioc_non_zero_SeqID	16	0x0	Changes IOC SeqID to match UnitID
			  0=Disable
			  1=Enable

gfx_non_zero_SeqID	17	0x0	Change GFX SeqID to match UnitID
			  0=Disable
			  1=Enable

ioc_only_mode_en	20	0x0	Bypasses buffer stage in GCM arb mode to improve latency. This feature is only available when in external GFX mode.
			   0=Disable
			   1=Enable

P_Rsv_BufCnt	21	0x1	Reserves Posted buffer for IGP ALL mode to improve performance
			   0=Reserve None
			   1=Reserve One

HTIU upstream configuration 19			

HTIU_UPSTREAM_CONFIG_20 - RW - 32 bits - HTIUNBIND:0x1B			
Field Name	**Bits**	**Default**	**Description**
PPG_EN	0	0x0	Enables HT TX PHY pattern generator. Used for testing only.
PPG_CTL	11:4	0x0	Pattern generator CTL bits for 8 bit-times
spare_31_12	31:12	0x0	Reserved. Should be set to 0
HTIU upstream configuration 20			

HTIU_UPSTREAM_CONFIG_21 - RW - 32 bits - HTIUNBIND:0x1C			
Field Name	**Bits**	**Default**	**Description**
PPG_CAD0	31:0	0x0	Pattern generator CAD bits [31:0]
HTIU upstream configuration 21			

HTIU_UPSTREAM_CONFIG_22 - RW - 32 bits - HTIUNBIND:0x1D			
Field Name	**Bits**	**Default**	**Description**
PPG_CAD1	31:0	0x0	Pattern generator CAD bits [63:32]
HTIU upstream configuration 22			

HTIU_UPSTREAM_CONFIG_23 - RW - 32 bits - HTIUNBIND:0x1E			
Field Name	**Bits**	**Default**	**Description**
PPG_CAD2	31:0	0x0	Pattern generator CAD bits [95:64]
HTIU upstream configuration 23			

HTIU_UPSTREAM_CONFIG_24 - RW - 32 bits - HTIUNBIND:0x1F			
Field Name	**Bits**	**Default**	**Description**
PPG_CAD3	31:0	0x0	Pattern generator CAD bits [128:96]
HTIU upstream configuration 24			

NB_LOWER_TOP_OF_DRAM2 - RW - 32 bits - HTIUNBIND:0x30			
Field Name	**Bits**	**Default**	**Description**
ENABLE	0	0x0	
LOWER_TOM2	31:23	0x0	
Top of lower Extended RAM			

NB_UPPER_TOP_OF_DRAM2 - RW - 32 bits - HTIUNBIND:0x31			
Field Name	**Bits**	**Default**	**Description**
UPPER_TOM2	7:0	0x0	
Top of upper Extended RAM			

NB_HTIU_CFG - RW - 32 bits - HTIUNBIND:0x32			
Field Name	**Bits**	**Default**	**Description**
spare_27_0	27:0	0x0	
NB_BAR3_PCIEXP_ENABLE	28	0x0	Enables PCI-E memory mapped register 0=Disable 1=Enable
spare_31_29	31:29	0x0	
HTIU control			

2.2 PCI Express Registers

PCIE_RESERVED - R - 32 bits - PCIEIND:0x0			
Field Name	Bits	Default	Description
PCIE_RESERVED	31:0	0xffffffff	This register field is reserved.

PCIE_SCRATCH - RW - 32 bits - PCIEIND:0x1			
Field Name	Bits	Default	Description
PCIE_SCRATCH	31:0	0x0	Software test register
Software test register.			

PCIE_CNTL - RW - 32 bits - PCIEIND:0x10			
Field Name	Bits	Default	Description
HWINIT_WR_LOCK	0	0x0	Hardware write lock. 0=HWInit registers unlocked 1=Lock HWInit registers
UR_ERR_REPORT_DIS	7	0x0	UR error reporting disable for TX
TX_CPU_HYPER_DIS	8	0x0	Disable HyperTransport compatibility features
PCIE_HT_NP_MEM_WRITE	9	0x0	Memory write mapping enable
RX_SB_ADJ_PAYLOAD_SIZE	12:10	0x2	SB payload size 2=16 bytes 3=32 bytes 4=64 bytes
RX_SB_COMPLETE_FULL_FIX	13	0x1	
RX_SB_REJECT_IF_FULL	14	0x0	
RX_RCB_REORDER_EN	16	0x1	RCB ordering enable 0=No re-ordering 1=Re-ordering
RX_RCB_INVALID_SIZE_DIS	17	0x1	RCB invalid size disable
RX_RCB_UNEXP_CPL_DIS	18	0x0	RCB unexpect cpl disable
RX_RCB_CPL_TIMEOUT_TEST_MODE	19	0x0	RCB cpl timeout test mode
TX_CPL_DEBUG	29:24	0x0	CPL debug
RX_CPL_POSTED_REQ_ORD_EN	31	0x1	CPL request ordering enable 0=Disable RX request ordering 1=Enable RX request ordering
PCIExpress control register			

PCIE_CONFIG_CNTL - RW - 32 bits - PCIEIND:0x11			
Field Name	Bits	Default	Description
CFG_ATI_REV_ID (R)	3:0	0x0	Metal mask programmable
DYN_CLK_LATENCY	7:4	0x7	Dynamic Clock Latency
PCIExpress Configuration Control register.			

PCIE_CI_CNTL - RW - 32 bits - PCIEIND:0x20			
Field Name	**Bits**	**Default**	**Description**

CI_BE_SPLIT_MODE	1:0	0x0	Byte enable splitting mode for master interface
			  0=Normal byte splitting rules for PCI-Express 1.0A
			  1=Force a split on QW boundary with maximum packet
			  length = 2
			  2=Bypass mode that forces full byte enables

CI_SLAVE_SPLIT_MODE	2	0x0	Completions split on Channels
			  0=RC - Full completions from Channel A or B
			  1=RC - Completions split on Channel A and B evenly

CI_SLAVE_GEN_USR_DIS	3	0x0	Sends USR for invalid addresses
			  0=Sends USR for invalid addresses
			  1=Disables slave from sending USR, and instead sends a
			  successful CMPLT_D with dummy data.

CI_MST_CMPL_DUMMY_DATA	4	0x1	0xDEADBEEF or 0xFFFFFFFF
			  0=0xDEADBEEF
			  1=0xFFFFFFFF

CI_MST_TAG_MODE	5	0x0	Incremental tag or first available tag
			  0=Incremental tag
			  1=First available tag

CI_SLV_RC_RD_REQ_SIZE	7:6	0x1	Slave read requests supported size to client.
			  0=32/64 byte requests supported
			  1=64 byte requests only
			  2=16/32/64

CI_SLV_ORDERING_DIS	8	0x0	Disables slave ordering logic
			  0=Enable slave ordering logic
			  1=Disable slave ordering logic

CI_RC_ORDERING_DIS	9	0x0	Disables RC ordering logic
			  0=Enable RC ordering logic
			  1=Disable RC ordering logic

CI_SLV_CPL_ALLOC_DIS	10	0x0	Slave CPL buffer is sub-divided or not
			  0=Slave CPL buffer is sub-divided between ports based
			  on number of lanes active
			  1=Slave CPL buffer is not sub-divided

Chip interface control register			

PCIE_BUS_CNTL - RW - 32 bits - PCIEIND:0x21			
Field Name	**Bits**	**Default**	**Description**

BUS_DBL_RESYNC	0	0x1	Double flop the sync module.
			  0=Normal
			  1=Add extra resynchronizing clock

PMI_BM_DIS	5	0x0	PMI Bus Master Disable
			  0=Normal
			  1=Disable

PMI_INT_DIS	6	0x0	PMI Interrupt Disable
			  0=Normal
			  1=Disable

IMMEDIATE_PMI_DIS	7	0x0	Immediate PMI Disable
			  0=Enable
			  1=Disable

PCI Express Bus Control register.			

PCIE_P_CNTL - RW - 32 bits - PCIEIND:0x40			
Field Name	**Bits**	**Default**	**Description**
P_PWRDN_EN	0	0x0	Enables powering down transmitter and receiver pads along with PLL macros.
P_SYMALIGN_MODE	1	0x0	Data Valid generation bit: iMODE=0 (Relax Mode): Update its symbol right away when detect any bit shift (i.e. data_valid will always assert). iMODE=1 (Aggressive Mode): Need confirmation before muxing out the data.
P_PLL_TEST_MODE	2	0x0	
P_PLL_PWRDN_IN_L1L23	3	0x0	Enables PLL powerdown in L1 or L23 Ready states, only if all the associated LC's are in Sates L1 / L23 corresponding to 4 / 2 lanes based on mpConfig and architecture.
P_PLL_BUF_PDNB	4	0x1	Disables 10X clock pad on a per PLL basis. It should be 1'b0 in order to activate this powersafe feature.
P_TXCLK_SND_PWRDN	5	0x0	Enables powering down TXCLK clock pads on the transmit side. Each clock pad corresponds to logic associated with 4 lanes.
P_TXCLK_RCV_PWRDN	6	0x0	Enables powering down TXCLK clock pads on the receive side. Each clock pad corresponds to logic associated with 4 lanes.
PI_SYMALIGN_DIS_ELIDLE	7	0x0	Symbol Alignment Statemachine control signal: iDIS_ELIDLE=0: ElectIdle assertion will be effective in state machine re-initialization. iDIS_ELIDLE=1: ElectIdle will be ineffective in state machine re-initialization
P_MASK_RCVR_EIDLE_EN	8	0x0	Enables EIDLE mask for powered down receivers.
P_PLL_PDNB	9	0x1	Enables PLL only (not the buffer) to power down in L1 or L23ready states.
RXP_XBAR_MUX0	17:16	0x0	Data routing cross bar mux - default 1'b0
RXP_XBAR_MUX1	19:18	0x1	Data routing cross bar mux - default 1'b1
RXP_XBAR_MUX2	21:20	0x2	Data routing cross bar mux - default 1'b2
RXP_XBAR_MUX3	23:22	0x3	Data routing cross bar mux - default 1'b3
PHY Control Register			

PCIE_P_BUF_STATUS - RW - 32 bits - PCIEIND:0x41			
Field Name	**Bits**	**Default**	**Description**
P_ELASTIC_BUF_OVERFLOW_0	0	0x0	Rx to Tx time domain hand-off buffer under/over flow: lane 0.
P_ELASTIC_BUF_OVERFLOW_1	1	0x0	Rx to Tx time domain hand-off buffer under/over flow: lane 1.
P_ELASTIC_BUF_OVERFLOW_2	2	0x0	Rx to Tx time domain hand-off buffer under/over flow: lane 2.
P_ELASTIC_BUF_OVERFLOW_3	3	0x0	Rx to Tx time domain hand-off buffer under/over flow: lane 3.
P_ELASTIC_BUF_OVERFLOW_4	4	0x0	Rx to Tx time domain hand-off buffer under/over flow: lane 4.
P_ELASTIC_BUF_OVERFLOW_5	5	0x0	Rx to Tx time domain hand-off buffer under/over flow: lane 5.
P_ELASTIC_BUF_OVERFLOW_6	6	0x0	Rx to Tx time domain hand-off buffer under/over flow: lane 6.
P_ELASTIC_BUF_OVERFLOW_7	7	0x0	Rx to Tx time domain hand-off buffer under/over flow: lane 7.
P_ELASTIC_BUF_OVERFLOW_8	8	0x0	Rx to Tx time domain hand-off buffer under/over flow: lane 8.
P_ELASTIC_BUF_OVERFLOW_9	9	0x0	Rx to Tx time domain hand-off buffer under/over flow: lane 9.
P_ELASTIC_BUF_OVERFLOW_10	10	0x0	Rx to Tx time domain hand-off buffer under/over flow: lane 10.
P_ELASTIC_BUF_OVERFLOW_11	11	0x0	Rx to Tx time domain hand-off buffer under/over flow: lane 11.
P_ELASTIC_BUF_OVERFLOW_12	12	0x0	Rx to Tx time domain hand-off buffer under/over flow: lane 12.
P_ELASTIC_BUF_OVERFLOW_13	13	0x0	Rx to Tx time domain hand-off buffer under/over flow: lane 13.
P_ELASTIC_BUF_OVERFLOW_14	14	0x0	Rx to Tx time domain hand-off buffer under/over flow: lane 14.
P_ELASTIC_BUF_OVERFLOW_15	15	0x0	Rx to Tx time domain hand-off buffer under/over flow: lane 15.
P_DESKEW_BUF_OVERFLOW_0	16	0x0	Symbol skew buffer over/underflow: lane 0.
P_DESKEW_BUF_OVERFLOW_1	17	0x0	Symbol skew buffer over/underflow: lane 1.
P_DESKEW_BUF_OVERFLOW_2	18	0x0	Symbol skew buffer over/underflow: lane 2.
P_DESKEW_BUF_OVERFLOW_3	19	0x0	Symbol skew buffer over/underflow: lane 3.
P_DESKEW_BUF_OVERFLOW_4	20	0x0	Symbol skew buffer over/underflow: lane 4.
P_DESKEW_BUF_OVERFLOW_5	21	0x0	Symbol skew buffer over/underflow: lane 5.
P_DESKEW_BUF_OVERFLOW_6	22	0x0	Symbol skew buffer over/underflow: lane 6.
P_DESKEW_BUF_OVERFLOW_7	23	0x0	Symbol skew buffer over/underflow: lane 7.
P_DESKEW_BUF_OVERFLOW_8	24	0x0	Symbol skew buffer over/underflow: lane 8.
P_DESKEW_BUF_OVERFLOW_9	25	0x0	Symbol skew buffer over/underflow: lane 9.
P_DESKEW_BUF_OVERFLOW_10	26	0x0	Symbol skew buffer over/underflow: lane 10.
P_DESKEW_BUF_OVERFLOW_11	27	0x0	Symbol skew buffer over/underflow: lane 11.
P_DESKEW_BUF_OVERFLOW_12	28	0x0	Symbol skew buffer over/underflow: lane 12.
P_DESKEW_BUF_OVERFLOW_13	29	0x0	Symbol skew buffer over/underflow: lane 13.
P_DESKEW_BUF_OVERFLOW_14	30	0x0	Symbol skew buffer over/underflow: lane 14.
P_DESKEW_BUF_OVERFLOW_15	31	0x0	Symbol skew buffer over/underflow: lane 15.
PHY Buffer Status register.			

PCIE_P_DECODER_STATUS - RW - 32 bits - PCIEIND:0x42			
Field Name	**Bits**	**Default**	**Description**
P_DECODE_ERR_0	0	0x0	Indicates which lane has the decoding error, i.e., can't decode the incoming data. Bit 15 => Lane 15 (0 = OK, 1 = Error), etc.
P_DECODE_ERR_1	1	0x0	Indicates which lane has the decoding error, i.e., can't decode the incoming data. Bit 15 => Lane 15 (0 = OK, 1 = Error), etc.
P_DECODE_ERR_2	2	0x0	Indicates which lane has the decoding error, i.e., can't decode the incoming data. Bit 15 => Lane 15 (0 = OK, 1 = Error), etc.
P_DECODE_ERR_3	3	0x0	Indicates which lane has the decoding error, i.e., can't decode the incoming data. Bit 15 => Lane 15 (0 = OK, 1 = Error), etc.
P_DECODE_ERR_4	4	0x0	Indicates which lane has the decoding error, i.e., can't decode the incoming data. Bit 15 => Lane 15 (0 = OK, 1 = Error), etc.
P_DECODE_ERR_5	5	0x0	Indicates which lane has the decoding error, i.e., can't decode the incoming data. Bit 15 => Lane 15 (0 = OK, 1 = Error), etc.
P_DECODE_ERR_6	6	0x0	Indicates which lane has the decoding error, i.e., can't decode the incoming data. Bit 15 => Lane 15 (0 = OK, 1 = Error), etc.
P_DECODE_ERR_7	7	0x0	Indicates which lane has the decoding error, i.e., can't decode the incoming data. Bit 15 => Lane 15 (0 = OK, 1 = Error), etc.
P_DECODE_ERR_8	8	0x0	Indicates which lane has the decoding error, i.e., can't decode the incoming data. Bit 15 => Lane 15 (0 = OK, 1 = Error), etc.
P_DECODE_ERR_9	9	0x0	Indicates which lane has the decoding error, i.e., can't decode the incoming data. Bit 15 => Lane 15 (0 = OK, 1 = Error), etc.
P_DECODE_ERR_10	10	0x0	Indicates which lane has the decoding error, i.e., can't decode the incoming data. Bit 15 => Lane 15 (0 = OK, 1 = Error), etc.
P_DECODE_ERR_11	11	0x0	Indicates which lane has the decoding error, i.e., can't decode the incoming data. Bit 15 => Lane 15 (0 = OK, 1 = Error), etc.
P_DECODE_ERR_12	12	0x0	Indicates which lane has the decoding error, i.e., can't decode the incoming data. Bit 15 => Lane 15 (0 = OK, 1 = Error), etc.
P_DECODE_ERR_13	13	0x0	Indicates which lane has the decoding error, i.e., can't decode the incoming data. Bit 15 => Lane 15 (0 = OK, 1 = Error), etc.
P_DECODE_ERR_14	14	0x0	Indicates which lane has the decoding error, i.e., can't decode the incoming data. Bit 15 => Lane 15 (0 = OK, 1 = Error), etc.
P_DECODE_ERR_15	15	0x0	Indicates which lane has the decoding error, i.e., can't decode the incoming data. Bit 15 => Lane 15 (0 = OK, 1 = Error), etc.
P_DISPARITY_ERR_0	16	0x0	Indicates which lane has the link error. Bit 15 => Lane 15 (0 = OK, 1 = Error), etc.
P_DISPARITY_ERR_1	17	0x0	Indicates which lane has the link error. Bit 15 => Lane 15 (0 = OK, 1 = Error), etc.
P_DISPARITY_ERR_2	18	0x0	Indicates which lane has the link error. Bit 15 => Lane 15 (0 = OK, 1 = Error), etc.
P_DISPARITY_ERR_3	19	0x0	Indicates which lane has the link error. Bit 15 => Lane 15 (0 = OK, 1 = Error), etc.
P_DISPARITY_ERR_4	20	0x0	Indicates which lane has the link error. Bit 15 => Lane 15 (0 = OK, 1 = Error), etc.

P_DISPARITY_ERR_5	21	0x0	Indicates which lane has the link error. Bit 15 => Lane 15 (0 = OK, 1 = Error), etc.
P_DISPARITY_ERR_6	22	0x0	Indicates which lane has the link error. Bit 15 => Lane 15 (0 = OK, 1 = Error), etc.
P_DISPARITY_ERR_7	23	0x0	Indicates which lane has the link error. Bit 15 => Lane 15 (0 = OK, 1 = Error), etc.
P_DISPARITY_ERR_8	24	0x0	Indicates which lane has the link error. Bit 15 => Lane 15 (0 = OK, 1 = Error), etc.
P_DISPARITY_ERR_9	25	0x0	Indicates which lane has the link error. Bit 15 => Lane 15 (0 = OK, 1 = Error), etc.
P_DISPARITY_ERR_10	26	0x0	Indicates which lane has the link error. Bit 15 => Lane 15 (0 = OK, 1 = Error), etc.
P_DISPARITY_ERR_11	27	0x0	Indicates which lane has the link error. Bit 15 => Lane 15 (0 = OK, 1 = Error), etc.
P_DISPARITY_ERR_12	28	0x0	Indicates which lane has the link error. Bit 15 => Lane 15 (0 = OK, 1 = Error), etc.
P_DISPARITY_ERR_13	29	0x0	Indicates which lane has the link error. Bit 15 => Lane 15 (0 = OK, 1 = Error), etc.
P_DISPARITY_ERR_14	30	0x0	Indicates which lane has the link error. Bit 15 => Lane 15 (0 = OK, 1 = Error), etc.
P_DISPARITY_ERR_15	31	0x0	Indicates which lane has the link error. Bit 15 => Lane 15 (0 = OK, 1 = Error), etc.
PHY Decoder Status register.			

PCIE_P_PLL_CNTL - RW - 32 bits - PCIEIND:0x44			
Field Name	**Bits**	**Default**	**Description**

P_VCOREF	1:0	0x0	Controls the signal generation used in calibrating PLL's
			  0=OFF
			  1=VDD/4
			  2=VDD/2
			  3=3VDD/4

P_CALREF	3:2	0x0	Controls the signal generation used in calibrating PLL's
			  0=OFF
			  1=VDD/2
			  2=2VDD/3
			  3=5VDD/6

PHY PLL Control register.			

PCIE_P_IMP_CNTL_STRENGTH - RW - 32 bits - PCIEIND:0x60			
Field Name	**Bits**	**Default**	**Description**
P_TX_STR_CNTL_READ_BACK (R)	3:0	0x0	Stores the readback value of current controller.
P_TX_IMP_CNTL_READ_BACK (R)	7:4	0x0	Stores the readback value of TX impedance controller.
P_RX_IMP_CNTL_READ_BACK (R)	11:8	0x0	Stores the readback value of RX impedance controller.
P_TX_STR_CNTL	19:16	0x7	Sets the initial default current strength to 4'b0111.
P_TX_IMP_CNTL	23:20	0x7	Default TX impedance control value.
P_RX_IMP_CNTL	27:24	0x7	Default RX impedance control value.
PI_HALT_IMP_CAL	28	0x0	

P_PAD_MANUAL_OVERRIDE	31	0x0	Enables Current and Impedance control values to override
			  0=Allow normal impedance compensation operation
			  1=Default to manual settings

PHY Impedance Control Strength register.			

PCIE_P_IMP_CNTL_UPDATE - RW - 32 bits - PCIEIND:0x61			
Field Name	**Bits**	**Default**	**Description**
P_IMP_PAD_UPDATE_RATE	4:0	0xf	PAD's update interval. 0=PHY130 (default 0xf) 1=PHY90 (default 0xe)
P_IMP_PAD_SAMPLE_DELAY	12:8	0x1	Sampling window.
P_IMP_PAD_INC_THRESHOLD	20:16	0x18	Incremental resolution.
P_IMP_PAD_DEC_THRESHOLD	28:24	0x8	Decremental resolution.
Impedance PAD defaults.			

PCIE_P_STR_CNTL_UPDATE - RW - 32 bits - PCIEIND:0x62			
Field Name	**Bits**	**Default**	**Description**
P_STR_PAD_UPDATE_RATE	4:0	0xf	PAD's update interval. 0=PHY130 (default 0xf) 1=PHY90 (default 0xe)
P_STR_PAD_SAMPLE_DELAY	12:8	0x1	Sampling window.
P_STR_PAD_INC_THRESHOLD	20:16	0x18	Incremental resolution.
P_STR_PAD_DEC_THRESHOLD	28:24	0x8	Decremental resolution.
Current PAD defaults.			

PCIE_P_PAD_MISC_CNTL - RW - 32 bits - PCIEIND:0x63			
Field Name	**Bits**	**Default**	**Description**
P_PAD_I_DUMMYOUT (R)	0	0x0	Input from analog - 0 if PMOS cur is stronger.
P_PAD_IMP_DUMMYOUT (R)	1	0x0	Input from analog - 0 if PMOS imp is stronger.
P_PAD_IMP_TESTOUT (R)	2	0x0	Input from analog - 1 if NMOS imp is stronger.
P_LINK_RETRAIN_ON_ERR_EN	3	0x0	Disables error counts in LaneDeskew if Symbol unlocking, Code Errors or Deskew Errors are detected.
Pad Miscellaneous Control registers.			

PCIE_P_PAD_FORCE_EN - RW - 32 bits - PCIEIND:0x64			
Field Name	**Bits**	**Default**	**Description**
B_PTX_PDNB_FEN	7:0	0x0	Forces B_PTX_PDNB to enable TX pad.
B_PRX_PDNB_FEN	15:8	0x0	Forces B_PRX_RDNB to enable RX pad.
B_PPLL_PDNB_FEN	19:16	0x0	Forces B_PPLL_PDNB to enable PLL.
B_PPLL_BUF_PDNB_FEN	23:20	0x0	Forces B_PPLL_BUF_PDNB to enable 10x driver in PLL.
B_PI_DREN_FEN	24	0x0	Forces B_PI_DREN to enable current calibration pad.
B_PBG_PDNB_FEN	25	0x0	Forces B_PBG_PDNB to enable Bandgap circuit in current calibration pad.
B_PIMP_TX_PDNB_FEN	26	0x0	Forces B_PIMP_TX_PDNB to enable TX impedance calibration pad.
B_PIMP_RX_PDNB_FEN	27	0x0	Forces B_PIMP_RX_PDNB to enable RX impedance calibration pad.
Powerdown enable signals used by the wrapper.			

PCIE_P_PAD_FORCE_DIS - RW - 32 bits - PCIEIND:0x65			
Field Name	**Bits**	**Default**	**Description**
B_PTX_PDNB_FDIS	7:0	0x0	Forces B_PTX_PDNB to disable TX pad.
B_PRX_PDNB_FDIS	15:8	0x0	Forces B_PRX_PDNB to disable RX pad.
B_PPLL_PDNB_FDIS	19:16	0x0	Forces B_PPLL_PDNB to disable PLL.
B_PPLL_BUF_PDNB_FDIS	23:20	0x0	Forces B_PPLL_BUF_PDNB to disable 10x driver in PLL.
B_PI_DREN_FDIS	24	0x0	Forces B_PI_DREN to disable current calibration pad.
B_PBG_PDNB_FDIS	25	0x0	Forces B_PBG_PDNB to disable Bandgap circuit in current calibration pad.
B_PIMP_TX_PDNB_FDIS	26	0x0	Forces B_PIMP_TX_PDNB to disable TX impedance calibration pad.
B_PIMP_RX_PDNB_FDIS	27	0x0	Forces B_PIMP_TX_PDNB to disable RX impedance calibration pad.
Powerdown disable signals used by the wrapper.			

PCIEP_RESERVED - R - 32 bits - PCIEIND_P:0x0			
Field Name	**Bits**	**Default**	**Description**
PCIEP_RESERVED	31:0	0xffffffff	This register field is reserved.

PCIEP_SCRATCH - RW - 32 bits - PCIEIND_P:0x1			
Field Name	**Bits**	**Default**	**Description**
PCIEP_SCRATCH	31:0	0x0	Scratch register.
Scratch register.			

PCIEP_PORT_CNTL - RW - 32 bits - PCIEIND_P:0x10			
Field Name	**Bits**	**Default**	**Description**
SLV_PORT_REQ_EN	0	0x1	Suspends all slave requests to client 0=Allow slave to be suspended 1=Ignore slave suspend signal
CI_SNOOP_OVERRIDE	1	0x0	Forces all slave requests to be snoop requests 0=Do not force all slave requests to be snoop requests 1=Force all slave requests to be snoop requests
HOTPLUG_MSG_EN	2	0x0	Enables hot-plug messages 0=Disable hot-plug messages 1=Enable hot-plug messages
NATIVE_PME_EN	3	0x1	Enables native PME 0=Disable native PME 1=Enable native PME
SEQNUM_DEBUG_MODE	4	0x0	Enables debug sequence number 0=Normal operation 1=Enable debug sequence number test mode
Port Control Register			

PCIE_TX_CNTL - RW - 32 bits - PCIEIND_P:0x20			
Field Name	**Bits**	**Default**	**Description**
TX_REPLAY_NUM_COUNT (R)	9:0	0x0	TX Replay Number Counter. Counter to keep track of the number of replays that have occurred.
TX_SNR_OVERRIDE	11:10	0x0	Snoop Not Required Override. Controls the Snoop bit for master requests 　0=Generate bit as normal 　1=Override equation, and always set bit 　2=Override equation, and always clear bit 　3=Invalid
TX_RO_OVERRIDE	13:12	0x0	Relaxed Ordering Override. Controls relaxed ordering bit for master requests 　0=Generate bit as normal 　1=Override equation, and always set bit 　2=Override equation, and always clear bit 　3=Invalid
TX_PACK_PACKET_DIS	14	0x0	Packet Packing Disable. Back-to-back packing of TLP and DLLP 　0=Place packets as close as allowable 　1=Place STP/SDP in lane 0 only
TX_GENERATE_CRC_ERR	15	0x0	Generates CRC errors from TX by zeroing CRC field. 　0=Generate proper CRC 　1=Generate bad CRC
TX_GAP_BTW_PKTS	18:16	0x0	Number of idle cycles between DLLP and TLP
TX_FLUSH_TLP_DIS	19	0x1	Disables flushing TLPs when Data Link is down 　0=Normal 　1=Disable
TX_CPL_PASS_P	20	0x1	Ordering rule: Let Completion Pass Posted 　0=No pass 　1=CPL pass
TX_NP_PASS_P	21	0x0	Ordering rule: Let Non-Posted Pass Posted 　0=no pass 　1=NP pass
TX_FC_UPDATE_TIMEOUT_SEL	25:24	0x2	Adjusts the length of the timeout interval before sending out flow control update 　0=Disable flow control 　1=4x clock cycle 　2=1024x clock cycle 　3=4096x clock cycle
TX_FC_UPDATE_TIMEOUT	31:26	0x7	Interval length to send flow control update
TX Control Register			

PCIE_TX_REQUESTER_ID - RW - 32 bits - PCIEIND_P:0x21			
Field Name	**Bits**	**Default**	**Description**
TX_REQUESTER_ID	15:0	0x0	Requester ID for Master transactions or Completer ID for Slave Completions
TX Requester ID Register			

PCIE_TX_VENDOR_SPECIFIC - RW - 32 bits - PCIEIND_P:0x22			
Field Name	**Bits**	**Default**	**Description**
TX_VENDOR_DATA	23:0	0x0	Writing to this register generates a Vendor Specific DLLP using Vendor Data for the payload
TX Vendor Specific DLLP			

PCIE_TX_REQUEST_NUM_CNTL - RW - 32 bits - PCIEIND_P:0x23			
Field Name	**Bits**	**Default**	**Description**
TX_NUM_P_ACK	5:0	0x10	Number of Posted requests sent out before ACK.
TX_NUM_P_ACK_EN	7	0x0	Enable for number of Posted requests sent out before ACK.
TX_NUM_NP_ACK	13:8	0x2	Number of Non-Posted requests sent out before ACK.
TX_NUM_NP_ACK_EN	15	0x0	Enable for number of Non-Posted requests sent out before ACK.
TX_NUM_CPL_ACK	21:16	0x1c	Number of Completions sent out before ACK.
TX_NUM_CPL_ACK_EN	23	0x0	Enable for number of Completions sent out before ACK.
TX_NUM_OUTSTANDING_NP	29:24	0x2	Number of Non-posted requests sent out before completion.
TX_NUM_OUTSTANDING_NP_EN	31	0x0	Enable for number of Non-posted requests sent out before completion.
TX Request Num Control Register			

PCIE_TX_SEQ - R - 32 bits - PCIEIND_P:0x24			
Field Name	**Bits**	**Default**	**Description**
TX_NEXT_TRANSMIT_SEQ	11:0	0x0	Next Transmit Sequence Number to send out.
TX_ACKD_SEQ	27:16	0x0	Last Acknowledged Sequence Number.
TX Sequence Register			

PCIE_TX_REPLAY - RW - 32 bits - PCIEIND_P:0x25			
Field Name	**Bits**	**Default**	**Description**
TX_REPLAY_NUM	9:0	0x3	Controls Replay Number before Link goes to Retrain.
TX_REPLAY_TIMER_OVERWRITE	15	0x0	Trigger for Replay Timer.
TX_REPLAY_TIMER	31:16	0x90	Replay Timer. When expired do Replay.
TX Replay Register			

PCIE_TX_ACK_LATENCY_LIMIT - RW - 32 bits - PCIEIND_P:0x26			
Field Name	**Bits**	**Default**	**Description**
TX_ACK_LATENCY_LIMIT	7:0	0x0	ACK Latency Limit for scheduling ACK DLLP transmission
TX_ACK_LATENCY_LIMIT_OVERWRITE	8	0x0	Uses the register value instead of the hardware value from the link width.
TX ACK Latency Limit			

PCIE_P_PORT_LANE_STATUS - RW - 32 bits - PCIEIND_P:0x50			
Field Name	Bits	Default	Description
PORT_LANE_REVERSAL (R)	0	0x0	Reverses lanes and controls signals associated with a port 0=Port Lane order is normal 1=Port Lane order is reversed
PHY_LINK_WIDTH (R)	6:1	0x0	Link Width 0=6'b00_0000 disabled 1=6'b00_0001 x1 2=6'b00_0010 x2 3=6'b00_0100 x4 4=6'b00_1000 x8 5=6'b01_0000 x12 6=6'b10_0000 x16
Port-Lane Status register.			

PCIE_FC_P - RW - 32 bits - PCIEIND_P:0x60			
Field Name	Bits	Default	Description
PD_CREDITS	7:0	0x8	Posted Data Flow Control Advertised Credits.
PH_CREDITS	15:8	0x2	Posted Header Flow Control Advertised Credits.
Posted Flow Control registers.			

PCIE_FC_NP - RW - 32 bits - PCIEIND_P:0x61			
Field Name	Bits	Default	Description
NPD_CREDITS	7:0	0x2	Non-Posted Data Flow Control Advertised Credits.
NPH_CREDITS	15:8	0x2	Non-Posted Header Flow Control Advertised Credits.
Non-Posted Flow Control registers.			

PCIE_FC_CPL - RW - 32 bits - PCIEIND_P:0x62			
Field Name	Bits	Default	Description
CPLD_CREDITS	7:0	0x0	Completion Data Flow Control Credits.
CPLH_CREDITS	15:8	0x0	Completion Header Flow Control Credits.
Completion Flow Control registers.			

PCIE_ERR_CNTL - RW - 32 bits - PCIEIND_P:0x6A			
Field Name	Bits	Default	Description
ERR_REPORTING_DIS	0	0x0	Disables PCI Express Advanced Error Reporting.
ERR_GEN_INTERRUPT	1	0x0	Enables Interrupt Generation for errors.
SYM_UNLOCKED_EN	2	0x0	Enables Reporting of Symbol Unlocked Errors. 0=Disable reporting unlocked symbol errors 1=Report unlocked symbol errors
Error Control registers.			

PCIE_RX_CNTL - RW - 32 bits - PCIEIND_P:0x70			
Field Name	**Bits**	**Default**	**Description**
RX_IGNORE_IO_ERR	0	0x0	Ignores Malformed I/O TLP Errors.
RX_IGNORE_BE_ERR	1	0x0	Ignores Malformed Byte Enable TLP Errors.
RX_IGNORE_MSG_ERR	2	0x0	Ignores Malformed Message Error.
RX_IGNORE_CRC_ERR	3	0x0	Ignores CRC Errors.
RX_IGNORE_CFG_ERR	4	0x0	Ignores Malformed Configuration Errors.
RX_IGNORE_CPL_ERR	5	0x0	Ignores Malformed Completion Errors.
RX_IGNORE_EP_ERR	6	0x0	Ignores Malformed EP Errors.
RX_IGNORE_LEN_MISMATCH_ERR	7	0x0	Ignores Malformed Length Mismatch Errors.
RX_IGNORE_MAX_PAYLOAD_ERR	8	0x0	Ignores Malformed Maximum Payload Errors.
RX_IGNORE_TC_ERR	9	0x0	Ignores Malformed Traffic Class Errors.
RX_IGNORE_CFG_UR	10	0x0	Reserved.
RX_IGNORE_IO_UR	11	0x0	Reserved.
RX_IGNORE_VEND0_UR	12	0x0	Ignores Vendor Type 0 Messages.
RX_NAK_IF_FIFO_FULL	13	0x0	Sends NAK if RX internal FIFO is full.
RX_GEN_ONE_NAK	14	0x1	Generates NAK only for the first bad packet until replayed.
RX_FC_INIT_FROM_REG	15	0x0	Flow Control Initialization from registers. 0=Init FC from FIFO sizes 1=Init FC from registers
RX_RCB_CPL_TIMEOUT	18:16	0x0	RCB cpl timeout. 0=Disable 1=50us 2=10ms 3=25ms 4=50ms 5=100ms 6=500ms 7=1ms
RX_RCB_CPL_TIMEOUT_MODE	19	0x0	
RX Control Register			

PCIE_RX_LASTACK_SEQNUM - R - 32 bits - PCIEIND_P:0x84			
Field Name	**Bits**	**Default**	**Description**
RX_LASTACK_SEQNUM	11:0	0x0	Last Acked sequence number.
RX Last Acked Sequence Number register.			

PCIE_LC_CNTL - RW - 32 bits - PCIEIND_P:0xA0			
Field Name	**Bits**	**Default**	**Description**
LC_CM_HI_ENABLE_COUNT	0	0x0	Enables count for CM_HIGH. When transmitter is to be turned on stop when the counter reaches CM_HI_COUNT_LIMIT_ON. If number of lanes = 1 or 2: CM_HI_COUNT_LIMIT_ON = 12 or 10. If number of lanes = 3 or 4: CM_HI_COUNT_LIMIT_ON = 10 or 12. If number of lanes > 4: CM_HI_COUNT_LIMIT_ON = 10 or 15.
LC_DONT_ENTER_L23_IN_D0	1	0x1	Do not enter L23 in D0 state.
LC_RESET_L_IDLE_COUNT_EN	2	0x0	Enables reset of electrical idle counter.
LC_RESET_LINK	3	0x0	

LC_L0S_INACTIVITY	11:8	0x0	L0s inactivity timer setting.
			0=25000000
			1=10
			2=20
			3=30
			4=50
			5=100
			6=250
			7=500
			8=1000
			9=2500
			10=10000
			11=25000
			12=100000
			13=250000
			14=1000000
LC_L1_INACTIVITY	15:12	0x0	L1 inactivity timer setting.
			0=250000000
			1=250
			2=500
			3=1000
			4=2500
			5=5000
			6=10000
			7=25000
			8=100000
			9=250000
			10=1000000
			11=2500000
			12=10000000
			13=25000000
			14=100000000
LC_PMI_TO_L1_DIS	16	0x0	Disables the transition to L1 caused by programming PMI_STATE to non-D0.
LC_INC_N_FTS_EN	17	0x0	Enables incrementing N_FTS for each transition to recovery.
LC_LOOK_FOR_IDLE_IN_L1L23	19:18	0x0	Controls the number of clocks to wait for Electrical Idle set in L1, L23.
			0=250
			1=100
			2=10000
			3=3000000
LC_FACTOR_IN_EXT_SYNC	20	0x0	Factors in the extended sync bit in the calculation for the replay timer adjustment.
LC_WAIT_FOR_PM_ACK_DIS	21	0x0	Disables waiting for PM_ACK in L23 ready entry handshake.
LC_WAKE_FROM_L23	22	0x0	For upstream component, wake the link from L23 ready
LC_L1_IMMEDIATE_ACK	23	0x0	Always ACK an ASPM L1 entry DLLP (i.e., never generate PM_NAK).
LC_ASPM_TO_L1_DIS	24	0x0	Disables ASPM L1.
LC_DELAY_COUNT	26:25	0x0	Controls the minimum amount of time to stay in L0s or L1.
			0=255/ 4095 (Power-down)
			1=1250 / 16383 (Power-down)
			2=5000/ 65535 (Power-down)
			3=25000 / 262143 (Power-down)
LC_DELAY_L0S_EXIT	27	0x0	Enables staying in L0s for a minimum time.
LC_DELAY_L1_EXIT	28	0x0	Enables staying in L1 for a minimum time.
LC_EXTEND_WAIT_FOR_EL_IDLE	29	0x1	Waits for Electrical idle in L1/L23 ready value.
LC_ESCAPE_L1L23_EN	30	0x0	Enables L1/L23 entry escape arcs.
LC_GATE_RCVR_IDLE	31	0x0	Ignores PHY Electrical idle detector.
Link Control Register			

PCIE_LC_STATE0 - R - 32 bits - PCIEIND_P:0xA5			
Field Name	**Bits**	**Default**	**Description**
LC_CURRENT_STATE	5:0	0x0	Current LC State.
LC_PREV_STATE1	13:8	0x0	1st Previous LC State.
LC_PREV_STATE2	21:16	0x0	2nd Previous LC State.
LC_PREV_STATE3	29:24	0x0	3rd Previous LC State.
Link Control State register.			

PCIE_LC_STATE1 - R - 32 bits - PCIEIND_P:0xA6			
Field Name	**Bits**	**Default**	**Description**
LC_PREV_STATE4	5:0	0x0	4th Previous LC State.
LC_PREV_STATE5	13:8	0x0	5th Previous LC State.
LC_PREV_STATE6	21:16	0x0	6th Previous LC State.
LC_PREV_STATE7	29:24	0x0	7th Previous LC State.
Link Control State register.			

PCIE_LC_STATE2 - R - 32 bits - PCIEIND_P:0xA7			
Field Name	**Bits**	**Default**	**Description**
LC_PREV_STATE8	5:0	0x0	8th Previous LC State.
LC_PREV_STATE9	13:8	0x0	9th Previous LC State.
LC_PREV_STATE10	21:16	0x0	10th Previous LC State.
LC_PREV_STATE11	29:24	0x0	11th Previous LC State.
Link Control State register.			

PCIE_LC_STATE3 - R - 32 bits - PCIEIND_P:0xA8			
Field Name	**Bits**	**Default**	**Description**
LC_PREV_STATE12	5:0	0x0	12th Previous LC State.
LC_PREV_STATE13	13:8	0x0	13th Previous LC State.
LC_PREV_STATE14	21:16	0x0	14th Previous LC State.
LC_PREV_STATE15	29:24	0x0	15th Previous LC State.
Link Control State register.			

PCIE_LC_STATE4 - R - 32 bits - PCIEIND_P:0xA9			
Field Name	**Bits**	**Default**	**Description**
LC_PREV_STATE16	5:0	0x0	16th Previous LC State.
LC_PREV_STATE17	13:8	0x0	17th Previous LC State.
LC_PREV_STATE18	21:16	0x0	18th Previous LC State.
LC_PREV_STATE19	29:24	0x0	19th Previous LC State.
Link Control State register.			

PCIE_LC_STATE5 - R - 32 bits - PCIEIND_P:0xAA			
Field Name	**Bits**	**Default**	**Description**
LC_PREV_STATE20	5:0	0x0	20th Previous LC State.
LC_PREV_STATE21	13:8	0x0	21st Previous LC State.
LC_PREV_STATE22	21:16	0x0	22nd Previous LC State.
LC_PREV_STATE23	29:24	0x0	23rd Previous LC State.
Link Control State register.			

PCIE_LC_TRAINING_CNTL - RW - 32 bits - PCIEIND_P:0xA1			
Field Name	**Bits**	**Default**	**Description**
LC_TRAINING_CNTL	3:0	0x0	Training control bits in training sets. 　0=Reserved 　1=Disable Link 　2=Loopback 　3=Disable Scrambling. The training control signal will be asserted in the TS when the associated bit is set to 1.
LC_LOOK_FOR_MORE_NON_MATCHING_TS1	4	0x0	Looks for more non-matching TS1 ordered sets.
LC_POWER_STATE (R)	10:8	0x0	Link Power state.
LC_EXTEND_WAIT_FOR_SKP	16	0x1	Extends the timer when in Rcv_L0s_Skp state. The bit is inverted before being used.
LC Training Control Register			

PCIE_LC_LINK_WIDTH_CNTL - RW - 32 bits - PCIEIND_P:0xA2			
Field Name	**Bits**	**Default**	**Description**
LC_LINK_WIDTH	2:0	0x6	Reserved.
LC_LINK_WIDTH_RD (R)	6:4	0x0	Read back link width.
LC_RECONFIG_ARC_MISSING_ESCAPE	7	0x0	Reserved.
LC_RECONFIG_NOW	8	0x0	Reserved.
LC_RECONFIG_LATER	9	0x0	Reserved.
LC_SHORT_RECONFIG_EN	11	0x0	Reserved.
Link Width Control.			

PCIE_LC_N_FTS_CNTL - RW - 32 bits - PCIEIND_P:0xA3			
Field Name	**Bits**	**Default**	**Description**
LC_XMIT_N_FTS	7:0	0xc	Number of FTS to override the strap value
LC_XMIT_N_FTS_OVERRIDE_EN	8	0x0	Enables the previous field to override the strap value.
LC_XMIT_N_FTS_LIMIT	23:16	0xff	Limits the number of FTS that can increment to when incrementing is enabled.
LC_N_FTS (R)	31:24	0x0	Number of FTS captured from the other end of the link.
LC Number of FTS Control			

PCIE_VENDOR_ID - RW - 16 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0x0]			
Field Name	**Bits**	**Default**	**Description**
VENDOR_ID (R)	15:0	0x1002	

PCIE_DEVICE_ID - R - 16 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0x2]			
Field Name	**Bits**	**Default**	**Description**
DEVICE_ID	15:0	0x0	

PCIE_COMMAND - RW - 16 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0x4]			
Field Name	**Bits**	**Default**	**Description**
IO_ACCESS_EN	0	0x0	0=Disable 1=Enable
MEM_ACCESS_EN	1	0x0	0=Disable 1=Enable
BUS_MASTER_EN	2	0x0	0=Disable 1=Enable
SPECIAL_CYCLE_EN (R)	3	0x0	0=Disable 1=Enable
MEM_WRITE_INVALIDATE_EN (R)	4	0x0	0=Disable 1=Enable
PAL_SNOOP_EN (R)	5	0x0	0=Disable 1=Enable
PARITY_ERROR_RESPONSE	6	0x0	0=Disable 1=Enable
AD_STEPPING (R)	7	0x0	0=Disable 1=Enable
SERR_EN	8	0x0	0=Disable 1=Enable
FAST_B2B_EN (R)	9	0x0	0=Disable 1=Enable
INT_DIS	10	0x0	0=Disable 1=Enable

PCIE_STATUS - RW - 16 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0x6]			
Field Name	**Bits**	**Default**	**Description**
INT_STATUS (R)	3	0x0	
CAP_LIST (R)	4	0x1	
PCI_66_EN (R)	5	0x0	
UDF_EN (R)	6	0x0	0=Disable 1=Enable
FAST_BACK_CAPABLE (R)	7	0x0	
MASTER_DATA_PARITY_ERROR (R)	8	0x0	0=Inactive 1=Active
DEVSEL_TIMING (R)	10:9	0x0	
SIGNAL_TARGET_ABORT (R)	11	0x0	0=No Abort 1=Target Abort
RECEIVED_TARGET_ABORT (R)	12	0x0	0=Inactive 1=Active

RECEIVED_MASTER_ABORT (R)	13	0x0	0=Inactive 1=Active
SIGNALED_SYSTEM_ERROR	14	0x0	0=No Error 1=SERR assert
PARITY_ERROR_DETECTED (R)	15	0x0	

PCIE_REVISION_ID - R - 8 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0x8]

Field Name	Bits	Default	Description
MINOR_REV_ID	3:0	0x0	
MAJOR_REV_ID	7:4	0x0	

PCIE_REGPROG_INF - RW - 8 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0x9]

Field Name	Bits	Default	Description
REG_LEVEL_PROG_INF (R)	7:0	0x0	

PCIE_SUB_CLASS - R - 8 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0xA]

Field Name	Bits	Default	Description
SUB_CLASS_INF	7:0	0x0	

PCIE_BASE_CODE - R - 8 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0xB]

Field Name	Bits	Default	Description
BASE_CLASS_CODE	7:0	0x0	

PCIE_CACHE_LINE - RW - 8 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0xC]

Field Name	Bits	Default	Description
CACHE_LINE_SIZE	7:0	0x0	

PCIE_LATENCY - RW - 8 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0xD]			
Field Name	**Bits**	**Default**	**Description**
LATENCY_TIMER (R)	7:0	0x0	

PCIE_HEADER - RW - 8 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0xE]			
Field Name	**Bits**	**Default**	**Description**
HEADER_TYPE (R)	6:0	0x1	
DEVICE_TYPE (R)	7	0x0	0=Single-Function Device 1=Multi-Function Device

PCIE_BIST - RW - 8 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0xF]			
Field Name	**Bits**	**Default**	**Description**
BIST_COMP (R)	3:0	0x0	
BIST_STRT (R)	6	0x0	
BIST_CAP (R)	7	0x0	

SUB_BUS_NUMBER_LATENCY - RW - 32 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0x18]			
Field Name	**Bits**	**Default**	**Description**
PRIMARY_BUS	7:0	0x0	Primary Bus Number register records the bus number of the PCI bus segment to which the primary interface of the bridge is connected.
SECONDARY_BUS	15:8	0x0	Secondary Bus Number register records the bus number of the PCIE bus segment to which the secondary interface of the bridge is connected.
SUB_BUS_NUM	23:16	0x0	Subordinate Bus Number register records the bus number of the highest numbered PCI bus segment which is behind the bridge.
SECONDARY_LATENCY_TIMER (R)	31:24	0x0	The register field does not apply to PCI Express. It is hardwired to 0.
Subordinate Bus Number Latency			

IO_BASE_LIMIT - RW - 16 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0x1C]

Field Name	Bits	Default	Description
IO_BASE_TYPE (R)	3:0	0x1	0=16-bit 1=32-bit
IO_BASE	7:4	0x0	I/O Base Register
IO_LIMIT_TYPE (R)	11:8	0x1	0=16-bit 1=32-bit
IO_LIMIT	15:12	0x0	I/O Limit Register
I/O Base Register Limit is used by the bridge to determine when to forward I/O transactions from one interface to the other.			

SECONDARY_STATUS - RW - 16 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0x1E]

Field Name	Bits	Default	Description
CAP_LIST (R)	4	0x0	Indicates the presence of an extended capability list item. Since all PCI Express devices are required to implement the PCI Express capability structure, this bit must be set to 1.
PCI_66_EN (R)	5	0x0	This bit does not apply to PCI Express. It is hardwired to 0.
UDF_EN (R)	6	0x0	User Defined Status Enable. 0=Disable 1=Enable
FAST_BACK_CAPABLE (R)	7	0x0	This bit does not apply to PCI Express. It is hardwired to 0.
MASTER_DATA_PARITY_ERROR	8	0x0	This bit is set by Requestor if its Parity Error Enable bit is set and either of the following two conditions occurs: 1) Requestor receives a Completion marked poisoned 2) Requestor poisons a write Request 0=No error 1=Parity error
DEVSEL_TIMING (R)	10:9	0x0	This register field does not apply to PCI Express. It is hardwired to 0.
SIGNAL_TARGET_ABORT (R)	11	0x0	This bit is set when a device completes a Request using Completer Abort Completion Status. 0=No Abort 1=Target Abort asserted
RECEIVED_TARGET_ABORT	12	0x0	This bit is set when a Requestor receives a Completion with Unsupported Request Completion Status. 0=No CA Received 1=Received Completion Abort
RECEIVED_MASTER_ABORT	13	0x0	This bit is set when a Requestor receives a Completion with Unsupported Request Completion Status. 0=No UR Received 1=Received Unsupported Request
RECEIVED_SYSTEM_ERROR	14	0x0	This bit reports the detection of an system error on the secondary interface of the bridge. 1 is asserted if a system error has been detected. 0=No Error 1=Sent Error Message
PARITY_ERROR_DETECTED	15	0x0	This bit is set when a device sends an ERR_FATAL or ERR_NONFATAL Message, and the SERR Enable bit in the Command register is 1. 0=No Error 1=Received Poisoned TLP
Secondary Status Register. These bits reflect status conditions of the secondary interface			

MEM_BASE_LIMIT - RW - 32 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0x20]

Field Name	Bits	Default	Description
MEM_BASE_TYPE (R)	3:0	0x0	0=32-bit 1=64-bit
MEM_BASE_31_20	15:4	0x0	
MEM_LIMIT_TYPE (R)	19:16	0x0	0=32-bit 1=64-bit
MEM_LIMIT_31_20	31:20	0x0	
Memory Limit Register defines a memory mapped I/O address range which is used by the bridge to determine when to forward memory transactions from one interface to the other.			

PREF_BASE_LIMIT - RW - 32 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0x24]

Field Name	Bits	Default	Description
PREF_MEM_BASE_TYPE (R)	3:0	0x1	0=32-bit 1=64-bit
PREF_MEM_BASE_31_20	15:4	0x0	
PREF_MEM_LIMIT_TYPE (R)	19:16	0x1	0=32-bit 1=64-bit
PREF_MEM_LIMIT_31_20	31:20	0x0	
Prefetchable Memory Base Limit indicates 64-bit addresses are supported.			

PREF_BASE_UPPER - RW - 32 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0x28]

Field Name	Bits	Default	Description
PREF_BASE_UPPER	31:0	0x0	

PREF_LIMIT_UPPER - RW - 32 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0x2C]

Field Name	Bits	Default	Description
PREF_LIMIT_UPPER	31:0	0x0	

IO_BASE_LIMIT_HI - RW - 32 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0x30]

Field Name	Bits	Default	Description
IO_BASE_31_16	15:0	0x0	Note: Bits [15:9] of this field are hardwired to 0.
IO_LIMIT_31_16	31:16	0x0	Note: Bits [15:9] of this field are hardwired to 0.

IRQ_BRIDGE_CNTL - RW - 16 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0x3E]			
Field Name	**Bits**	**Default**	**Description**
PARITY_RESPONSE_EN	0	0x0	Parity Error Response Enable controls the response to Poisoned TLPs.
SERR_EN	1	0x0	System Error Enable controls the forwarding of ERR_COR, ERR_NONFATAL and ERR_FATAL from secondary to primary
ISA_EN	2	0x0	ISA Enable modifies the response by the bridge to ISA I/O addresses.
VGA_EN	3	0x0	VGA Enable modifies the response by the bridge to VGA compatible addresses.
MASTER_ABORT_MODE (R)	5	0x0	Master Abort Mode does not apply to PCI Express. Hardwired to 0.

SECONDARY_BUS_RESET	6	0x0	Secondary Bus Reset triggers a hot reset on the corresponding PCI Express Port.
			  0=Run
			  1=Reset

FAST_B2B_EN (R)	7	0x0	Fast Back-to-Back Transactions Enable does not apply to PCI Express. Hardwired to 0.
			  0=Disable
			  1=Enable

Bridge Control Register			

CAP_PTR - RW - 32 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0x34]			
Field Name	**Bits**	**Default**	**Description**
CAP_PTR (R)	7:0	0x50	Pointer to a linked list of additional capabilities implemented by this device. 50=Point to PM Capability
Capability Pointer			

PCIE_INTERRUPT_LINE - RW - 8 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0x3C]			
Field Name	**Bits**	**Default**	**Description**
INTERRUPT_LINE	7:0	0xff	

PCIE_INTERRUPT_PIN - RW - 8 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0x3D]			
Field Name	**Bits**	**Default**	**Description**
INTERRUPT_PIN	7:0	0x0	Note: Bits [7:3] of this field are hardwired to 0.

<table>
<tr><td colspan="4">PMI_CAP_LIST - RW - 16 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4
pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0x50]</td></tr>
<tr><td>Field Name</td><td>Bits</td><td>Default</td><td>Description</td></tr>
<tr><td>CAP_ID (R)</td><td>7:0</td><td>0x1</td><td>Capability ID Must be set to 01h.
  1=PCIE Power Management Registers</td></tr>
<tr><td>NEXT_PTR (R)</td><td>15:8</td><td>0x58</td><td>Next Capability Pointer.</td></tr>
<tr><td colspan="4">Power Management Capbility List</td></tr>
</table>

<table>
<tr><td colspan="4">PMI_CAP - RW - 16 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4
pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0x52]</td></tr>
<tr><td>Field Name</td><td>Bits</td><td>Default</td><td>Description</td></tr>
<tr><td>VERSION (R)</td><td>2:0</td><td>0x3</td><td>Version.
  3=PMI Spec 1.2</td></tr>
<tr><td>PME_CLOCK (R)</td><td>3</td><td>0x0</td><td>This bit does not apply to PCI Express. It is hardwired to 0.</td></tr>
<tr><td>DEV_SPECIFIC_INIT (R)</td><td>5</td><td>0x0</td><td>Device Specific Initialization</td></tr>
<tr><td>AUX_CURRENT</td><td>8:6</td><td>0x0</td><td>AUX Current</td></tr>
<tr><td>D1_SUPPORT (R)</td><td>9</td><td>0x0</td><td>D1 Support
  1=Support D1 PM State.</td></tr>
<tr><td>D2_SUPPORT (R)</td><td>10</td><td>0x0</td><td>D2 Support
  1=Support D2 PM State.</td></tr>
<tr><td>PME_SUPPORT (R)</td><td>15:11</td><td>0x19</td><td>For a device, this indicates the power states in which the device may generate a PME.</td></tr>
<tr><td colspan="4">Power Management Capabilities Register</td></tr>
</table>

<table>
<tr><td colspan="4">PMI_STATUS_CNTL - RW - 32 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4
pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0x54]</td></tr>
<tr><td>Field Name</td><td>Bits</td><td>Default</td><td>Description</td></tr>
<tr><td>POWER_STATE</td><td>1:0</td><td>0x0</td><td>Power State.</td></tr>
<tr><td>NO_SOFT_RESET (R)</td><td>3</td><td>0x0</td><td></td></tr>
<tr><td>PME_EN</td><td>8</td><td>0x0</td><td>PME Enable.</td></tr>
<tr><td>DATA_SELECT</td><td>12:9</td><td>0x0</td><td>Data Select.</td></tr>
<tr><td>DATA_SCALE (R)</td><td>14:13</td><td>0x0</td><td>Data Scale.</td></tr>
<tr><td>PME_STATUS</td><td>15</td><td>0x0</td><td>PME Status.</td></tr>
<tr><td>B2_B3_SUPPORT (R)</td><td>22</td><td>0x0</td><td>B2/B3 support does not apply to PCI Express. It is hardwired to 0.</td></tr>
<tr><td>BUS_PWR_EN (R)</td><td>23</td><td>0x0</td><td>Bus Power/Clock Control Enable Does not apply to PCI Express. Hardwired to 0.</td></tr>
<tr><td>PMI_DATA (R)</td><td>31:24</td><td>0x0</td><td>Data.</td></tr>
<tr><td colspan="4">Power Management Status/Control Register</td></tr>
</table>

PCIE_CAP_LIST - RW - 16 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0x58]			
Field Name	**Bits**	**Default**	**Description**
CAP_ID (R)	7:0	0x10	Indicates the PCI Express Capability structure. This field must return a Capability ID of 10h indicating that this is a PCI Express Capability structure. 10=PCI Express capable
NEXT_PTR (R)	15:8	0x80	Next Capability Pointer. The offset to the next PCI capability structure or 00h if no other items exist in the linked list of capabilities.
The PCI Express Capability List register enumerates the PCI Express Capability structure in the PCI 2.3 configuration space capability list.			

PCIE_CAP - RW - 16 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0x5A]			
Field Name	**Bits**	**Default**	**Description**
VERSION (R)	3:0	0x1	Indicates PCI-SIG defined PCI Express capability structure version number. 0=PCI Express Cap Version

DEVICE_TYPE (R)	7:4	0x4	Indicates the type of PCI Express logical device.
			  0=PCI Express Endpoint
			  4=PCI Express RootComplex

SLOT_IMPLEMENTED	8	0x0	Indicates that the PCI Express Link associated with this Port is connected to a slot
INT_MESSAGE_NUM (R)	13:9	0x0	Interrupt Message Number.
The PCI Express Capabilities register identifies PCI Express device type and associated capabilities.			

DEVICE_CAP - RW - 32 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0x5C]			
Field Name	**Bits**	**Default**	**Description**
MAX_PAYLOAD_SUPPORT (R)	2:0	0x0	Indicates the maximum payload size that the device can support for TLPs. 0=128B size
PHANTOM_FUNC (R)	4:3	0x0	Indicates the support for use of unclaimed function numbers to extend the number of outstanding transactions allowed by logically combining unclaimed function numbers with the Tag identifier. 0=No Phantom Functions
EXTENDED_TAG (R)	5	0x1	Indicates the maximum supported size of the Tag field as a Requester. 0=8 Bit Tag Supported
L0S_ACCEPTABLE_LATENCY (R)	8:6	0x0	Indicates the acceptable total latency that an Endpoint can withstand due to the transition from L0s state to the L0 state.
L1_ACCEPTABLE_LATENCY (R)	11:9	0x0	Indicates the acceptable latency that an Endpoint can withstand due to the transition from L1 state to the L0 state.
ROLE_BASED_ERR_REPORTING (R)	15	0x0	0=Role-Based Error Reporting Disabled 1=Role-Based Error Reporting Enabled

CAPTURED_SLOT_POWER_LIMIT (R)	25:18	0x0	(Upstream Ports only) In combination with the Slot Power Limit Scale value, specifies the upper limit on power supplied by slot.
CAPTURED_SLOT_POWER_SCALE (R)	27:26	0x0	Specifies the scale used for the Slot Power Limit Value.
The Device Capabilities register identifies PCI Express device specific capabilities.			

DEVICE_CNTL - RW - 16 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0x60]			
Field Name	**Bits**	**Default**	**Description**

CORR_ERR_EN	0	0x0	Controls the reporting of correctable errors. The default value of this field is 0.
			  0=Disable
			  1=Enable

NON_FATAL_ERR_EN	1	0x0	Controls the reporting of Non-fatal errors. The default value of this field is 0.
			  0=Disable
			  1=Enable

FATAL_ERR_EN	2	0x0	Controls the reporting of Fatal errors. The default value of this field is 0.
			  0=Disable
			  1=Enable

USR_REPORT_EN	3	0x0	Enables the reporting of Unsupported Requests. The default value of this field is 0.
			  0=Disable
			  1=Enable

RELAXED_ORD_EN	4	0x1	If this bit is set, the device is permitted to set the Relaxed Ordering bit in the Attributes field of transactions it initiates that do not require strong write ordering. The default value of this bit is 1.
			  0=Disable
			  1=Enable

MAX_PAYLOAD_SIZE	7:5	0x0	Sets maximum TLP payload size for the device. The default value of this field is 000b. 0=128B size

EXTENDED_TAG_EN	8	0x0	Enables a device to use an 8-bit Tag field as a requester. If the bit is cleared, the device is restricted to a 5-bit Tag field. The default value of this field is 0.
			  0=Disable
			  1=Enable

PHANTOM_FUNC_EN (R)	9	0x0	Enables a device to use unclaimed functions as Phantom Functions to extend the number of outstanding transaction identifiers. If the bit is cleared, the device is not allowed to use Phantom Functions.
			  0=Disable
			  1=Enable

AUX_POWER_PM_EN (R)	10	0x0	Enables a device to draw AUX power independent of PME AUX power.
			  0=Disable
			  1=Enable

NO_SNOOP_EN	11	0x1	If this bit is set to 1, the device is permitted to set the No Snoop bit in the Requester Attributes of transactions it initiates that do not require hardware enforced cache coherency. The default value of this bit is 1.
			  0=Disable
			  1=Enable

MAX_REQUEST_SIZE (R)	14:12	0x0	Sets the maximum Read Request size for the Device as a Requester. The default value of this field is 010b. 0=128B size
BRIDGE_CFG_RETRY_EN (R)	15	0x0	0=Disable 1=Enable
The Device Control register controls PCI Express device specific parameters.			

DEVICE_STATUS - RW - 16 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0x62]

Field Name	Bits	Default	Description
CORR_ERR	0	0x0	Indicates status of correctable errors detected.
NON_FATAL_ERR	1	0x0	Indicates status of Nonfatal errors detected.
FATAL_ERR	2	0x0	Indicates status of Fatal errors detected.
USR_DETECTED	3	0x0	Indicates that the device received an Unsupported Request.
AUX_PWR	4	0x0	Devices that require AUX power report this bit as set if AUX power is detected by the device.
TRANSACTIONS_PEND (R)	5	0x0	Endpoints: This bit, when set, indicates that the device has issued Non-Posted Requests which have not been completed. Root and Switch Ports: This bit, when set, indicates that a Port has issued Non-Posted Requests on its own behalf (using the Port's own Requester ID) which have not been completed.
The Device Status register provides information about PCI Express device specific parameters.			

LINK_CAP - RW - 32 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0x64]

Field Name	Bits	Default	Description
LINK_SPEED (R)	3:0	0x1	Indicates the maximum Link speed of the given PCI Express Link. 1=2.5 Gb/s

LINK_WIDTH (R)	9:4	0x0	Indicates the maximum width of the given PCI Express Link.
			    1=x1
			    2=x2
			    4=x4
			    8=x8
			    12=x12
			    16=x16
			    32=x32

PM_SUPPORT (R)	11:10	0x3	Indicates the level of ASPM supported on the given PCI Express Link.
L0S_EXIT_LATENCY (R)	14:12	0x1	Indicates the L0s exit latency for the given PCI Express Link. The value reported indicates the length of time this Port requires to complete transition from L0s to L0.
L1_EXIT_LATENCY (R)	17:15	0x2	Indicates the L0s exit latency for the given PCI Express Link. The value reported indicates the length of time this Port requires to complete transition from L0s to L0.
CLOCK_POWER_MANAGEMENT (R)	18	0x0	
SURPRISE_DOWN_ERR_REPORTING_EN (R)	19	0x0	
DL_ACTIVE_REPORTING_CAPABLE (R)	20	0x1	
PORT_NUMBER (R)	31:24	0x0	Indicates the PCI Express Port number for the given PCI Express Link.
The Link Capabilities register identifies PCI Express Link specific capabilities.			

LINK_CNTL - RW - 16 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0x68]			
Field Name	Bits	Default	Description

PM_CONTROL	1:0	0x0	Controls the level of ASPM supported on the given PCI Express Link. Defined encodings are as follows:
			  00b=Disabled
			  01b=L0s Entry Enabled
			  10b=L1 Entry Enabled
			  11b=L0s and L1 Entry Enabled

READ_CPL_BOUNDARY (R)	3	0x0	Read Completion Boundary. Indicates the RCB value for the Root Port.
			  0=64 Byte
			  1=128 Byte

LINK_DIS	4	0x0	Disables the Link when set to 1b. The default value of this field is 0b.
RETRAIN_LINK (W)	5	0x0	A write of 1b to this bit initiates Link retraining by directing the Physical Layer LTSSM to the Recovery state. Reads of this bit always return 0b.
COMMON_CLOCK_CFG	6	0x0	Indicates that this component and the component at the opposite end of this Link are operating with a distributed common reference clock. The default value of this field is 0b.
EXTENDED_SYNC	7	0x0	Forces the transmission of 4096 FTS ordered sets in the L0s state, followed by a single SKP ordered set.
CLOCK_POWER_MANAGEMENT_EN (R)	8	0x0	
The Link Control register controls PCI Express Link specific parameters.			

LINK_STATUS - RW - 16 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0x6A]			
Field Name	Bits	Default	Description
NEGOTIATED_LINK_SPEED (R)	3:0	0x1	Indicates the negotiated Link speed of the given PCI Express Link 0=2.5 Gb/s

NEGOTIATED_LINK_WIDTH (R)	9:4	0x0	This field indicates the negotiated width of the given PCI Express Link. The defined encodings are as follows: 000001b X1, 000010b X2, 000100b X4, 001000b X8, 001100b X12, 010000b X16, and 100000b X32. All other encodings are reserved.
			  1=x1
			  2=x2
			  4=x4
			  8=x8
			  12=x12
			  16=x16
			  32=x32

LINK_TRAINING (R)	11	0x0	This read-only bit indicates that Link training is in progress (Physical Layer LTSSM in Configuration or Recovery state), or that 1b was written to the Retrain Link bit but Link training has not yet begun. The hardware clears this bit once Link training is complete.

SLOT_CLOCK_CFG (R)	12	0x1	This bit indicates that the component uses the same physical reference clock that the platform provides on the connector. If the device uses an independent clock, irrespective of the presence of a reference on the connector, this bit must be clear.
			   0=Diff Clock
			   1=Same Clock

DL_ACTIVE (R)	13	0x0	
The Link Status register provides information about PCI Express Link specific parameters.			

SLOT_CAP - RW - 32 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0x6C]			
Field Name	**Bits**	**Default**	**Description**
ATTN_BUTTON_PRESENT (R)	0	0x0	Indicates that an Attention Button is implemented on the chassis for this slot.
PWR_CONTROLLER_PRESENT (R)	1	0x0	Indicates that a Power Controller is implemented for this slot.
MRL_SENSOR_PRESENT (R)	2	0x0	Indicates that an Manually-operated Retention Latch Sensor is implemented on the chassis for this slot.
ATTN_INDICATOR_PRESENT (R)	3	0x0	Indicates that an Attention Indicator is implemented on the chassis for this slot.
PWR_INDICATOR_PRESENT (R)	4	0x0	Indicates that a Power Indicator is implemented on the chassis for this slot.
HOTPLUG_SURPRISE	5	0x0	Indicates that a device present in this slot might be removed from the system without any prior notification.
HOTPLUG_CAPABLE	6	0x0	Indicates that this slot is capable of supporting Hot-Plug operations.
SLOT_PWR_LIMIT_VALUE	14:7	0x0	In combination with the Slot Power Limit Scale value, this register field specifies the upper limit on power supplied by slot.
SLOT_PWR_LIMIT_SCALE	16:15	0x0	Specifies the scale used for the Slot Power Limit Value
ELECTROMECH_INTERLOCK_PRESENT	17	0x0	
NO_COMMAND_COMPLETED_SUPPORTED	18	0x0	
PHYSICAL_SLOT_NUM	31:19	0x0	This hardware initialized field indicates the physical slot number attached to this Port.
The Slot Capabilities register identifies PCI Express slot specific capabilities.			

SLOT_CNTL - RW - 16 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0x70]			
Field Name	**Bits**	**Default**	**Description**
ATTN_BUTTON_PRESSED_EN	0	0x0	Enables the generation of Hot-Plug interrupt or wakeup event on an attention button pressed event.
PWR_FAULT_DETECTED_EN (R)	1	0x0	
MRL_SENSOR_CHANGED_EN (R)	2	0x0	
PRESENCE_DETECT_CHANGED_EN	3	0x0	Enables the generation of Hot-Plug interrupt or wakeup event on a presence detect changed event.
COMMAND_COMPLETED_INTR_EN	4	0x0	Enables the generation of Hot-Plug interrupt when a command is completed by the Hot-Plug Controller.
HOTPLUG_INTR_EN	5	0x0	Enables the generation of Hot-Plug interrupt on enabled Hot-Plug events.

ATTN_INDICATOR_CNTL	7:6	0x3	Reads to this register return the current state of the Attention Indicator. Writes to this register set the Attention Indicator.
PWR_INDICATOR_CNTL	9:8	0x3	Reads to this register return the current state of the Power Indicator. Writes to this register set the Power Indicator.
PWR_CONTROLLER_CNTL (R)	10	0x0	When read this register returns the current state of the Power applied to the slot. When written it sets the power state of the slot per the defined encodings.
ELECTOMECH_INTERLOCK_CNTL (R)	11	0x0	
DL_STATE_CHANGED_EN	12	0x0	
The Slot Control register controls PCI Express Slot specific parameters			

SLOT_STATUS - RW - 16 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0x72]			
Field Name	**Bits**	**Default**	**Description**
ATTN_BUTTON_PRESSED	0	0x0	This bit is set when the attention button is pressed.
PRESENCE_DETECT_CHANGED	3	0x0	This bit is set when a Presence Detect change is detected.
COMMAND_COMPLETED	4	0x0	This bit is set when the Hot-Plug Controller completes an issued command.
PRESENCE_DETECT_STATE (R)	6	0x0	Indicates the presence of a card in the slot.
ELECTROMECH_INTERLOCK_STATUS (R)	7	0x0	
DL_STATE_CHANGED	8	0x0	
The Slot Status register provides information about PCI Express Slot specific parameters			

ROOT_CNTL - RW - 16 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0x74]			
Field Name	**Bits**	**Default**	**Description**
SERR_ON_CORR_ERR_EN	0	0x0	System Error on Correctable Error Enable. indicates that a System Error should be generated if a correctable error is reported by any of the devices in the hierarchy associated with this Root Port.
SERR_ON_NONFATAL_ERR_EN	1	0x0	System Error on Non-Fatal Error Enable. Indicates that a System Error should be generated if a Non-fatal error is reported by any of the devices in the hierarchy associated with this Root Port.
SERR_ON_FATAL_ERR_EN	2	0x0	System Error on Fatal Error Enable. Indicates that a System Error should be generated if a Fatal error is reported by any of the devices in the hierarchy associated with this Root Port.
PM_INTERRUPT_EN	3	0x0	PME Interrupt Enable. Enables interrupt generation upon receipt of a PME Message.
CRS_SOFTWARE_VISIBILITY_EN	4	0x0	
The Root Control register controls PCI Express Root Complex specific parameters.			

ROOT_STATUS - RW - 32 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0x78]			
Field Name	**Bits**	**Default**	**Description**
PME_REQUESTOR_ID (R)	15:0	0x0	Indicates the PCI requestor ID of the last PME requestor.
PME_STATUS	16	0x0	Indicates that PME was asserted by the requestor ID indicated in the PME Requestor ID field.
PME_PENDING (R)	17	0x0	This read-only bit indicates that another PME is pending when the PME Status bit is set.
The Root Status register provides information about PCI Express device specific parameters.			

MSI_CAP_LIST - R - 16 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0x80]			
Field Name	**Bits**	**Default**	**Description**
CAP_ID	7:0	0x5	Identifies if a device function is MSI capable.
NEXT_PTR	15:8	0xb0	Pointer to the next item on the capabilities list.
Message Signaled Interrupt Capability Registers			

PCIE_MSI_MSG_CNTL - RW - 16 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0x82]			
Field Name	**Bits**	**Default**	**Description**
MSI_EN	0	0x0	0=Disable 1=Enable
MSI_MULTI_CAP (R)	3:1	0x0	0=1 message allocated 1=2 messages allocated 2=4 messages allocated 3=8 messages allocated 4=16 messages allocated 5=32 messages allocated 6=Reserved 7=Reserved
MSI_MULTI_EN	6:4	0x0	0=1 message allocated 1=2 messages allocated 2=4 messages allocated 3=8 messages allocated 4=16 messages allocated 5=32 messages allocated 6=Reserved 7=Reserved
MSI_64BIT (R)	7	0x0	0=Not capable of generating 1 64-bit message address 1=Capable of generating 1 64-bit message address

PCIE_MSI_MSG_ADDR_LO - RW - 32 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0x84]			
Field Name	**Bits**	**Default**	**Description**
MSI_MSG_ADDR_LO	31:2	0x0	

PCIE_MSI_MSG_ADDR_HI - RW - 32 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0x88]			
Field Name	**Bits**	**Default**	**Description**
MSI_MSG_ADDR_HI (R)	31:0	0x0	

PCIE_MSI_MSG_DATA_64 - RW - 16 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0x8C]			
Field Name	**Bits**	**Default**	**Description**
MSI_DATA_64 (R)	15:0	0x0	

PCIE_MSI_MSG_DATA - RW - 32 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0x88]			
Field Name	**Bits**	**Default**	**Description**
MSI_DATA	15:0	0x0	

CRS_TIMER - RW - 32 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0x90]			
Field Name	**Bits**	**Default**	**Description**
CRS_DELAY	23:0	0x0	
CRS_LIMIT	31:24	0x0	
Configuration Request Retry Status Timer			

IOC_CNTL - RW - 32 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0x94]			
Field Name	**Bits**	**Default**	**Description**
SLV_FORCE_RO	0	0x0	Slave Force Relaxed Ordering.
SLV_FORCE_SNOOP	1	0x0	Slave Force Snoop / Non-Snoop.
SLV_FORCE_ATTR_ENABLE	2	0x0	Slave Force Attribute Enable.
SLV_P2P_DIS	3	0x0	Slave Peer-to-Peer Disable.
BM_SET_DIS	7	0x0	Bus Master Set Disable.
MST_STRICT_ORDER	8	0x0	Master Strict Ordering.
MST_BLOCK_NSNOOP	9	0x0	Master Block Non-Snoop.
MST_BLOCK_SNOOP	10	0x0	Master Block Snoop.
MST_RO_FORCE	11	0x0	Master Force Relaxed Ordering.
MST_RO_ENABLE	12	0x0	Master Enable Relaxed Ordering.
MST_NS_ENABLE	13	0x0	Master Non-Snoop Enable.
EXT_DEV_PRESENCE_DET	16	0x0	
EXT_DEV_CRC_ENABLE	17	0x0	
CRS_ENABLE	18	0x0	
INT_ABCD_EFGH	19	0x0	Interrupt Vector.
SET_PWR_MSG_ENABLE	20	0x0	
I/O Control			

SSID_CAP_LIST - RW - 32 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0xB0]			
Field Name	**Bits**	**Default**	**Description**
CAP_ID (R)	7:0	0xd	Capability ID.
NEXT_PTR (R)	15:8	0xb8	Pointer to next capability register.
Subsystem ID Capability List			

SSID_ID - RW - 32 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0xB4]			
Field Name	**Bits**	**Default**	**Description**
SUBSYSTEM_VENDOR	15:0	0x0	Subsystem Vendor.
SUBSYSTEM_ID	31:16	0x0	Subsystem ID.
Subsystem ID			

MSI_MAP - RW - 32 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0xB8]			
Field Name	**Bits**	**Default**	**Description**
CAP_ID (R)	7:0	0x8	Identifies the function as message signaled interrupt capable. This field is read only
NEXT_PTR (R)	15:8	0x0	Pointer to the next item in the capabilities list. Must be NULL for the final item in the list. This field is read only.
EN (R)	16	0x1	
FIXD (R)	17	0x1	
CAP_TYPE (R)	31:27	0x15	
MSI Mapping Capability Register			

PCIE_PORT_INDEX - RW - 32 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0xE0]			
Field Name	**Bits**	**Default**	**Description**
PCIE_INDEX	7:0	0x0	Index of bifdecp.
Index register for the PCI Express port indirect registers			

PCIE_PORT_DATA - RW - 32 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0xE4]			
Field Name	**Bits**	**Default**	**Description**
PCIE_DATA	31:0	0x0	Data of bifdecp.
Data register for the PCI Express port indirect registers			

PCIE_ENH_ADV_ERR_RPT_CAP_HDR - RW - 32 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0x140]			
Field Name	**Bits**	**Default**	**Description**
CAP_ID (R)	15:0	0x1	This field is a PCI-SIG defined ID number that indicates the nature and format of the extended capability.
CAP_VER (R)	19:16	0x1	This field is a PCI-SIG defined version number that indicates the version of the capability structure present.
NEXT_PTR (R)	31:20	0x0	This field contains the offset to the next PCI Express capability structure or 000h if no other items exist in the linked list of capabilities.
Advanced Error Reporting Enhanced Capability header			

PCIE_UNCORR_ERR_STATUS - RW - 32 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0x144]			
Field Name	**Bits**	**Default**	**Description**
DLP_ERR_STATUS	4	0x0	Data Link Protocol Error Status.
SURPDN_ERR_STATUS	5	0x0	
PSN_ERR_STATUS	12	0x0	Poisoned TLP Status.
FC_ERR_STATUS	13	0x0	Flow Control Protocol Error Status.
CPL_TIMEOUT_STATUS	14	0x0	Completion Timeout Status.
CPL_ABORT_ERR_STATUS	15	0x0	Completer Abort Status.
UNEXP_CPL_STATUS	16	0x0	Unexpected Completion Status.
RCV_OVFL_STATUS	17	0x0	Receiver Overflow Status.
MAL_TLP_STATUS	18	0x0	Malformed TLP Status.
ECRC_ERR_STATUS	19	0x0	ECRC Error Status.
UNSUPP_REQ_ERR_STATUS	20	0x0	Unsupported Request Error Status.
The Uncorrectable Error Status register reports error status of individual error sources on a PCI Express device.			

PCIE_UNCORR_ERR_MASK - RW - 32 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0x148]			
Field Name	**Bits**	**Default**	**Description**
DLP_ERR_MASK	4	0x0	Data Link Protocol Error Mask.
SURPDN_ERR_MASK	5	0x0	
PSN_ERR_MASK	12	0x0	Poisoned TLP Mask.
FC_ERR_MASK	13	0x0	Flow Control Protocol Error Mask.
CPL_TIMEOUT_MASK	14	0x0	Completion Timeout Mask.
CPL_ABORT_ERR_MASK	15	0x0	Completer Abort Mask.
UNEXP_CPL_MASK	16	0x0	Unexpected Completion Mask.
RCV_OVFL_MASK	17	0x0	Receiver Overflow Mask.
MAL_TLP_MASK	18	0x0	Malformed TLP Mask.
ECRC_ERR_MASK	19	0x0	ECRC Error Mask.
UNSUPP_REQ_ERR_MASK	20	0x0	Unsupported Request Error Mask
The Uncorrectable Error Mask register controls the reporting of individual errors by the device to the PCI Express Root Complex via a PCI Express error Message.			

PCIE_UNCORR_ERR_SEVERITY - RW - 32 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0x14C]			
Field Name	**Bits**	**Default**	**Description**
DLP_ERR_SEVERITY	4	0x1	Data Link Protocol Error Severity.
SURPDN_ERR_SEVERITY	5	0x1	
PSN_ERR_SEVERITY	12	0x0	Poisoned TLP Severity.
FC_ERR_SEVERITY	13	0x1	Flow Control Protocol Error Severity.
CPL_TIMEOUT_SEVERITY	14	0x0	Completion Timeout Error Severity.
CPL_ABORT_ERR_SEVERITY	15	0x0	Completer Abort Error Severity.
UNEXP_CPL_SEVERITY	16	0x0	Unexpected Completion Error Severity.
RCV_OVFL_SEVERITY	17	0x1	Receiver Overflow Error Severity.
MAL_TLP_SEVERITY	18	0x1	Malformed TLP Severity.
ECRC_ERR_SEVERITY	19	0x0	ECRC Error Severity.
UNSUPP_REQ_ERR_SEVERITY	20	0x0	Unsupported Request Error Severity.
The Uncorrectable Error Severity register controls whether an individual error is reported as a Nonfatal or Fatal error.			

PCIE_CORR_ERR_STATUS - RW - 32 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0x150]			
Field Name	**Bits**	**Default**	**Description**
RCV_ERR_STATUS	0	0x0	Receiver Error Status.
BAD_TLP_STATUS	6	0x0	Bad TLP Status.
BAD_DLLP_STATUS	7	0x0	Bad DLLP Status.
REPLAY_NUM_ROLLOVER_STATUS	8	0x0	REPLAY_NUM Rollover Status.
REPLAY_TIMER_TIMEOUT_STATUS	12	0x0	Replay Timer Timeout Status.
ADVISORY_NONFATAL_ERR_STATUS	13	0x0	
The Correctable Error Status register reports error status of individual correctable error sources on a PCI Express device.			

PCIE_CORR_ERR_MASK - RW - 32 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0x154]			
Field Name	**Bits**	**Default**	**Description**
RCV_ERR_MASK	0	0x0	Receiver Error Mask.
BAD_TLP_MASK	6	0x0	Bad TLP Mask.
BAD_DLLP_MASK	7	0x0	Bad DLLP Mask.
REPLAY_NUM_ROLLOVER_MASK	8	0x0	REPLAY_NUM Rollover Mask.
REPLAY_TIMER_TIMEOUT_MASK	12	0x0	Replay Timer Timeout Mask.
ADVISORY_NONFATAL_ERR_MASK	13	0x1	
The Correctable Error Mask register controls reporting of individual correctable errors by device to the PCI Express Root Complex via a PCI Express error Message.			

PCIE_ADV_ERR_CAP_CNTL - RW - 32 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0x158]			
Field Name	**Bits**	**Default**	**Description**
FIRST_ERR_PTR (R)	4:0	0x0	The First Error Pointer is a read-only register that identifies the bit position of the first error reported in the Uncorrectable Error Status register.
ECRC_GEN_CAP (R)	5	0x0	Indicates that the device is capable of generating ECRC.
ECRC_GEN_EN	6	0x0	Enables ECRC generation. Default value of this field is 0.
ECRC_CHECK_CAP (R)	7	0x0	Indicates that the device is capable of checking ECRC.
ECRC_CHECK_EN	8	0x0	Enables ECRC checking. Default value of this field is 0.
Advanced Error Capabilities and Control Register			

PCIE_HDR_LOG0 - R - 32 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0x15C]			
Field Name	**Bits**	**Default**	**Description**
TLP_HDR	31:0	0x0	TLP Header 1st DW.
Header Log Register captures the Header for the TLP corresponding to a detected error;			

PCIE_HDR_LOG1 - R - 32 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0x160]			
Field Name	**Bits**	**Default**	**Description**
TLP_HDR	31:0	0x0	TLP Header 2nd DW.
Header Log Register			

PCIE_HDR_LOG2 - R - 32 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0x164]			
Field Name	**Bits**	**Default**	**Description**
TLP_HDR	31:0	0x0	TLP Header 3rd DW.
Header Log Register			

PCIE_HDR_LOG3 - R - 32 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0x168]			
Field Name	**Bits**	**Default**	**Description**
TLP_HDR	31:0	0x0	TLP Header 4th DW.
Header Log Register			

PCIE_ROOT_ERR_CMD - RW - 32 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0x16C]			
Field Name	**Bits**	**Default**	**Description**
CORR_ERR_REP_EN	0	0x0	Correctable Error Reporting Enable. Enables the generation of an interrupt when a correctable error is reported by any of the devices in the hierarchy associated with this Root Port.
NONFATAL_ERR_REP_EN	1	0x0	Non-Fatal Error Reporting Enable. Enables the generation of an interrupt when a Non-fatal error is reported by any of the devices in the hierarchy associated with this Root Port.
FATAL_ERR_REP_EN	2	0x0	Fatal Error Reporting Enable. Enables the generation of an interrupt when a Fatal error is reported by any of the devices in the hierarchy associated with this Root Port.
Root Error Command Register			

PCIE_ROOT_ERR_STATUS - RW - 32 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0x170]			
Field Name	**Bits**	**Default**	**Description**
ERR_CORR_RCVD	0	0x0	Set when a correctable error Message is received and this bit is not already set. The default value of this field is 0.
MULT_ERR_CORR_RCVD	1	0x0	Set when a correctable error Message is received and ERR_COR Received is already set. The default value of this field is 0.
ERR_FATAL_NONFATAL_RCVD	2	0x0	Set when either a Fatal or a Non-fatal error Message is received and this bit is not already set. The default value of this field is 0.

MULT_ERR_FATAL_NONFATAL_RCVD	3	0x0	Set when either a Fatal or a Non-fatal error is received and ERR_FATAL/NONFATAL Received is already set. The default value of this field is 0.
FIRST_UNCORRECTABLE_FATAL	4	0x0	Set to 1b when the first Uncorrectable error Message received is for a Fatal error. The default value of this field is 0.
NONFATAL_ERROR_MSG_RCVD	5	0x0	Set to 1b when one or more Non-Fatal Uncorrectable error Messages have been received. The default value of this field is 0.
FATAL_ERROR_MSG_RCVD	6	0x0	Set to 1b when one or more Fatal Uncorrectable error Messages have been received. The default value of this field is 0.
ADV_ERR_INT_MSG_NUM (R)	31:27	0x0	Advanced Error Interrupt Message Number.
Root Error Status Register			

PCIE_ERR_SRC_ID - RW - 32 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0x174]			
Field Name	**Bits**	**Default**	**Description**
ERR_COR_SRC_ID (R)	15:0	0x0	Loaded with the Requestor ID indicated in the received ERR_COR Message when the ERR_COR Received register is not already set. The default value of this field is 0.
ERR_FATAL_NONFATAL_SRC_ID (R)	31:16	0x0	Loaded with the Requestor ID indicated in the received ERR_FATAL or ERR_NONFATAL Message when the ERR_FATAL/NONFATAL Received register is not already set. The default value of this field is 0
The Error Source Identification register identifies the source (Requestor ID) of first correctable and uncorrectable (Non-fatal/Fatal) errors reported in the Root Error Status register.			

PCIE_VC0_RESOURCE_CAP - R - 32 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0x110]			
Field Name	**Bits**	**Default**	**Description**
PORT_ARB_CAP	7:0	0x0	Indicates the types of Port Arbitration supported by the VC resource.
REJECT_SNOOP_TRANS	15	0x0	When set to 0, transactions with or without the No Snoop bit set within the TLP Header are allowed on this VC.
MAX_TIME_SLOTS	21:16	0x0	Indicates the maximum number of time slots that the VC resource is capable of supporting.
PORT_ARB_TABLE_OFFSET	31:24	0x0	Indicates the location of the Port Arbitration Table associated with the VC resource.
VC0 Resource Capability Register			

PCIE_VC0_RESOURCE_CNTL - RW - 32 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0x114]

Field Name	Bits	Default	Description
TC_VC_MAP_TC0 (R)	0	0x1	Indicates the TCs that are mapped to the VC resource.
TC_VC_MAP_TC1_7	7:1	0x7f	Indicates the TCs that are mapped to the VC resource.
LOAD_PORT_ARB_TABLE (R)	16	0x0	Updates the Port Arbitration logic from the Port Arbitration Table for the VC resource.
PORT_ARB_SELECT	19:17	0x0	Configures the VC resource to provide a particular Port Arbitration service.
VC_ID (R)	26:24	0x0	Assigns a VC ID to the VC resource.
VC_ENABLE (R)	31	0x1	Enables a Virtual Channel.
VC0 Resource Control Register			

PCIE_VC0_RESOURCE_STATUS - R - 16 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0x11A]

Field Name	Bits	Default	Description
PORT_ARB_TABLE_STATUS	0	0x0	Indicates the coherency status of the Port Arbitration Table associated with the VC resource.
VC_NEGOTIATION_PENDING	1	0x1	Indicates whether the Virtual Channel negotiation (initialization or disabling) is in pending state.
VC0 Resource Status Register			

PCIE_DEBUG_CNTL - RW - 32 bits - PCIEIND:0x12

Field Name	Bits	Default	Description

DEBUG_PORT_EN	7:0	0x1	Debug Bus Port Enable
			  1=Port A
			  2=Port B
			  4=Port C
			  8=Port D
			  16=Port E
			  32=Port F
			  64=Port G
			  128=Port H

DEBUG_SELECT	8	0x0	Debug Bus Select - for additional muxing (e.g. VC0 vs. VC1)
Debug Bus Control Register			

PCIE_WPR_CNTL - RW - 32 bits - PCIEIND:0x30			
Field Name	**Bits**	**Default**	**Description**
WPR_RESET_HOT_RST_EN	0	0x1	Enables Hot Reset feature.
WPR_RESET_LNK_DWN_EN	1	0x0	Enables Link down reset feature.
WPR_RESET_LNK_DIS_EN	2	0x1	Enables Link disable reset feature.
WPR_RESET_COR_EN	3	0x0	Enables external CORE reset feature.
WPR_RESET_REG_EN	4	0x0	Enables external REGISTER reset feature.
WPR_RESET_STY_EN	5	0x0	Enables external Stickybit Register reset feature.
WPR_RESET_PHY_EN	6	0x0	Enables external PHY reset feature.
WPR Control Register			

PCIE_PERF_LATENCY_CNTL - RW - 32 bits - PCIEIND:0x70			
Field Name	**Bits**	**Default**	**Description**

TIMER_EN	0	0x0	Enables Latency Timer
			  0=Disable timer
			  1=Enable timer

TIMER_SHADOW_WR (W)	1	0x0	Shadow Register Write.
			Write 1 to update shadow registers
			  0=N/A
			  1=Write 1 to shadow write

TIMER_RESET (W)	2	0x0	Resets Latency Timer.
			Write 1 to clear latency timer counters
			  0=N/A
			  1=Write 1 to reset

PORT_NUM	6:4	0x0	Port Number.
			Should always be programmed to 000
			  0=Port 0
			  1=Port 1
			  2=Port 2
			  3=Port 3
			  4=Port 4
			  5=Port 5

PORT_MODE	7	0x0	Port Mode.
			Should always be programmed to 0
			  0=All ports
			  1=Single port

SNOOP	8	0x0	Excludes/Includes Snoop requests
			  0=Do not include snoop requests
			  1=Include snoop requests

NO_SNOOP	9	0x0	Excludes/Includes Non-Snoop requests
			  0=Do not include no snoop requests
			  1=Include no snoop requests

MEM_REQ	10	0x0	Excludes/Includes Memory requests
			  0=Do not include MEM requests
			  1=Include MEM requests

CFG_IO_REQ	11	0x0	Excludes/Includes CFG and I/O requests
			  0=Do not include CFG or I/O requests
			  1=Include CFG or I/O requests

REQ_ID_MODE	12	0x0	Requester ID Mode.
			Unfiltered/Filtered by Requester ID
			  0=Do not filter by requester ID
			  1=Filter by requester ID

TAG_MODE	13	0x0	Tag Mode.
			Unfiltered/Filters by Tag
			  0=Do not filter by tag
			  1=Filter by tag

CPL_MODE	14	0x0	Completion Mode.
			First Data/Last Data
			  0=First Data
			  1=Last Data

TRAFFIC_CLASS	23:16	0x0	Traffic Class filter bits
Latency Timer Control Register			

PCIE_PERF_LATENCY_REQ_ID - RW - 32 bits - PCIEIND:0x71

Field Name	Bits	Default	Description
REQUESTER_ID	15:0	0x0	Requester ID Value
REQUESTER_MASK	31:16	0xffff	Requester ID Mask
Filter to select requests for a particular Requester ID			

PCIE_PERF_LATENCY_TAG - RW - 32 bits - PCIEIND:0x72

Field Name	Bits	Default	Description
TAG	7:0	0x0	Tag Value
TAG_MASK	15:8	0xff	Tag Mask
Filter to select requests for a particular Tag			

PCIE_PERF_LATENCY_THRESHOLD - RW - 32 bits - PCIEIND:0x73

Field Name	Bits	Default	Description
THRESHOLD	15:0	0xffff	Latency Threshold value in TXCLKs
Latency Threshold used to count requests outside of acceptable time limit			

PCIE_PERF_LATENCY_MAX - R - 32 bits - PCIEIND:0x74

Field Name	Bits	Default	Description
PEAK	15:0	0x0	Number of TXCLKs for peak latency request
REQUESTER_ID	31:16	0x0	Requester ID for peak latency request
Current peak latency time with Requester ID			

PCIE_PERF_LATENCY_TIMER_LO - R - 32 bits - PCIEIND:0x75

Field Name	Bits	Default	Description
TIMER_LO	31:0	0x0	Lower 32 bits of cumulative latency timer
Counter for cumulative request latency - LOWER BITS			

PCIE_PERF_LATENCY_TIMER_HI - R - 32 bits - PCIEIND:0x76			
Field Name	**Bits**	**Default**	**Description**
TIMER_HI	31:0	0x0	Upper 32 bits of cumulative latency timer. Note: Bits [31:16] of this field are hardwired to 0.
Counter for cumulative request latency - UPPER BITS			

PCIE_PERF_LATENCY_COUNTER0 - R - 32 bits - PCIEIND:0x77			
Field Name	**Bits**	**Default**	**Description**
NUM_REQ	31:0	0x0	Number of requests measured
Counter for number of requests measured			

PCIE_PERF_LATENCY_COUNTER1 - R - 32 bits - PCIEIND:0x78			
Field Name	**Bits**	**Default**	**Description**
NUM_EXCEED	31:0	0x0	Number of requests exceeding latency threshold
Counter for number of requests exceeding latency threshold			

PCIE_PRBS23_BITCNT_0 - RW - 32 bits - PCIEIND:0xD0			
Field Name	**Bits**	**Default**	**Description**
PRBS23_BITCNT_0	31:0	0x0	

PCIE_PRBS23_BITCNT_1 - RW - 32 bits - PCIEIND:0xD1			
Field Name	**Bits**	**Default**	**Description**
PRBS23_BITCNT_1	31:0	0x0	

PCIE_PRBS23_BITCNT_2 - RW - 32 bits - PCIEIND:0xD2			
Field Name	**Bits**	**Default**	**Description**
PRBS23_BITCNT_2	31:0	0x0	

PCIE_PRBS23_BITCNT_3 - RW - 32 bits - PCIEIND:0xD3			
Field Name	**Bits**	**Default**	**Description**
PRBS23_BITCNT_3	31:0	0x0	

PCIE_PRBS23_BITCNT_4 - RW - 32 bits - PCIEIND:0xD4			
Field Name	**Bits**	**Default**	**Description**
PRBS23_BITCNT_4	31:0	0x0	

PCIE_PRBS23_BITCNT_5 - RW - 32 bits - PCIEIND:0xD5			
Field Name	**Bits**	**Default**	**Description**
PRBS23_BITCNT_5	31:0	0x0	

PCIE_PRBS23_BITCNT_6 - RW - 32 bits - PCIEIND:0xD6			
Field Name	**Bits**	**Default**	**Description**
PRBS23_BITCNT_6	31:0	0x0	

PCIE_PRBS23_BITCNT_7 - RW - 32 bits - PCIEIND:0xD7			
Field Name	**Bits**	**Default**	**Description**
PRBS23_BITCNT_7	31:0	0x0	

PCIE_PRBS23_BITCNT_8 - RW - 32 bits - PCIEIND:0xD8			
Field Name	**Bits**	**Default**	**Description**
PRBS23_BITCNT_8	31:0	0x0	

PCIE_PRBS23_BITCNT_9 - RW - 32 bits - PCIEIND:0xD9			
Field Name	**Bits**	**Default**	**Description**
PRBS23_BITCNT_9	31:0	0x0	

PCIE_PRBS23_BITCNT_10 - RW - 32 bits - PCIEIND:0xDA			
Field Name	**Bits**	**Default**	**Description**
PRBS23_BITCNT_10	31:0	0x0	

PCIE_PRBS23_BITCNT_11 - RW - 32 bits - PCIEIND:0xDB			
Field Name	**Bits**	**Default**	**Description**
PRBS23_BITCNT_11	31:0	0x0	

PCIE_PRBS23_BITCNT_12 - RW - 32 bits - PCIEIND:0xDC			
Field Name	**Bits**	**Default**	**Description**
PRBS23_BITCNT_12	31:0	0x0	

PCIE_PRBS23_BITCNT_13 - RW - 32 bits - PCIEIND:0xDD			
Field Name	**Bits**	**Default**	**Description**
PRBS23_BITCNT_13	31:0	0x0	

PCIE_PRBS23_BITCNT_14 - RW - 32 bits - PCIEIND:0xDE			
Field Name	**Bits**	**Default**	**Description**
PRBS23_BITCNT_14	31:0	0x0	

PCIE_PRBS23_BITCNT_15 - RW - 32 bits - PCIEIND:0xDF			
Field Name	**Bits**	**Default**	**Description**
PRBS23_BITCNT_15	31:0	0x0	

PCIE_PRBS23_ERRCNT_0 - R - 32 bits - PCIEIND:0xE0			
Field Name	**Bits**	**Default**	**Description**
PRBS23_ERRCNT_0	31:0	0x0	

PCIE_PRBS23_ERRCNT_1 - R - 32 bits - PCIEIND:0xE1			
Field Name	**Bits**	**Default**	**Description**
PRBS23_ERRCNT_1	31:0	0x0	

PCIE_PRBS23_ERRCNT_2 - R - 32 bits - PCIEIND:0xE2			
Field Name	**Bits**	**Default**	**Description**
PRBS23_ERRCNT_2	31:0	0x0	

PCIE_PRBS23_ERRCNT_3 - R - 32 bits - PCIEIND:0xE3			
Field Name	**Bits**	**Default**	**Description**
PRBS23_ERRCNT_3	31:0	0x0	

PCIE_PRBS23_ERRCNT_4 - R - 32 bits - PCIEIND:0xE4			
Field Name	**Bits**	**Default**	**Description**
PRBS23_ERRCNT_4	31:0	0x0	

PCIE_PRBS23_ERRCNT_5 - R - 32 bits - PCIEIND:0xE5			
Field Name	**Bits**	**Default**	**Description**
PRBS23_ERRCNT_5	31:0	0x0	

PCIE_PRBS23_ERRCNT_6 - R - 32 bits - PCIEIND:0xE6			
Field Name	**Bits**	**Default**	**Description**
PRBS23_ERRCNT_6	31:0	0x0	

PCIE_PRBS23_ERRCNT_7 - R - 32 bits - PCIEIND:0xE7			
Field Name	**Bits**	**Default**	**Description**
PRBS23_ERRCNT_7	31:0	0x0	

PCIE_PRBS23_ERRCNT_8 - R - 32 bits - PCIEIND:0xE8			
Field Name	**Bits**	**Default**	**Description**
PRBS23_ERRCNT_8	31:0	0x0	

PCIE_PRBS23_ERRCNT_9 - R - 32 bits - PCIEIND:0xE9			
Field Name	**Bits**	**Default**	**Description**
PRBS23_ERRCNT_9	31:0	0x0	

PCIE_PRBS23_ERRCNT_10 - R - 32 bits - PCIEIND:0xEA			
Field Name	**Bits**	**Default**	**Description**
PRBS23_ERRCNT_10	31:0	0x0	

PCIE_PRBS23_ERRCNT_11 - R - 32 bits - PCIEIND:0xEB			
Field Name	**Bits**	**Default**	**Description**
PRBS23_ERRCNT_11	31:0	0x0	

PCIE_PRBS23_ERRCNT_12 - R - 32 bits - PCIEIND:0xEC			
Field Name	**Bits**	**Default**	**Description**
PRBS23_ERRCNT_12	31:0	0x0	

PCIE_PRBS23_ERRCNT_13 - R - 32 bits - PCIEIND:0xED			
Field Name	**Bits**	**Default**	**Description**
PRBS23_ERRCNT_13	31:0	0x0	

PCIE_PRBS23_ERRCNT_14 - R - 32 bits - PCIEIND:0xEE			
Field Name	**Bits**	**Default**	**Description**
PRBS23_ERRCNT_14	31:0	0x0	

PCIE_PRBS23_ERRCNT_15 - R - 32 bits - PCIEIND:0xEF			
Field Name	**Bits**	**Default**	**Description**
PRBS23_ERRCNT_15	31:0	0x0	

PCIE_PRBS23_CLR - RW - 32 bits - PCIEIND:0xF0

Field Name	Bits	Default	Description
PRBS23_CLR	15:0	0x0	

PCIE_PRBS23_ERRSTAT - R - 32 bits - PCIEIND:0xF1

Field Name	Bits	Default	Description
PRBS23_ERRSTAT	15:0	0x0	

PCIE_PRBS23_LOCKED - R - 32 bits - PCIEIND:0xF2

Field Name	Bits	Default	Description
PRBS23_LOCKED	15:0	0x0	

PCIE_PRBS23_FREERUN - RW - 32 bits - PCIEIND:0xF3

Field Name	Bits	Default	Description
PRBS23_FREERUN	15:0	0x0	

PCIE_PRBS23_LOCK_CNT - RW - 32 bits - PCIEIND:0xF4

Field Name	Bits	Default	Description
PRBS23_LOCK_CNT	4:0	0x0	

PCIE_PRBS23_EN - RW - 32 bits - PCIEIND:0xF5

Field Name	Bits	Default	Description
PRBS23_EN	0	0x0	

PCIE_P90RX_PRBS_CLR - RW - 32 bits - PCIEIND:0xF6

Field Name	Bits	Default	Description
P90RX_PRBS_CLR	15:0	0x0	

PCIE_P90_BRX_PRBS_ER - R - 32 bits - PCIEIND:0xF7

Field Name	Bits	Default	Description
P90_BRX_PRBS_ER	15:0	0x0	

PCIE_P90TX_PRBS_EN - RW - 32 bits - PCIEIND:0xF8

Field Name	Bits	Default	Description
P90TX_PRBS_EN	15:0	0x0	

PCIE_B_P90_CNTL - RW - 32 bits - PCIEIND:0xF9

Field Name	Bits	Default	Description
B_P90IMP_BACKUP	3:0	0x0	
B_P90PLL_BACKUP	31:12	0x0	

PCIE_TX_VENDOR_SPECIFIC - RW - 32 bits - PCIEIND_P:0x22

Field Name	Bits	Default	Description
TX_VENDOR_DATA	23:0	0x0	Writing to this register generates a Vendor Specific DLLP using Vendor Data for the payload.
TX Vendor Specific DLLP			

PCIE_TX_ACK_LATENCY_LIMIT - RW - 32 bits - PCIEIND_P:0x26

Field Name	Bits	Default	Description
TX_ACK_LATENCY_LIMIT	7:0	0x0	ACK Latency Limit for scheduling ACK DLLP transmission.
TX_ACK_LATENCY_LIMIT_OVERWRITE	8	0x0	Use register value instead of hardware value from link width.
TX ACK Latency Limit			

PCIE_TX_CREDITS_CONSUMED_P - R - 32 bits - PCIEIND_P:0x30

Field Name	Bits	Default	Description
TX_CREDITS_CONSUMED_PD	11:0	0x0	For posted TLP data, total number of FC units consumed by TLP transmission made since FC initialization, modulo 4096.
TX_CREDITS_CONSUMED_PH	23:16	0x0	For posted TLP header, total number of FC units consumed by TLP transmission made since FC initialization, modulo 256.
TX Credits Consumed Register (Posted)			

PCIE_TX_CREDITS_CONSUMED_NP - R - 32 bits - PCIEIND_P:0x31			
Field Name	**Bits**	**Default**	**Description**
TX_CREDITS_CONSUMED_NPD	11:0	0x0	For non-posted TLP data, total number of FC units consumed by TLP transmission made since FC initialization, modulo 4096.
TX_CREDITS_CONSUMED_NPH	23:16	0x0	For non-posted TLP header, total number of FC units consumed by TLP transmission made since FC initialization, modulo 256.
TX Credits Consumed Register (Non-Posted)			

PCIE_TX_CREDITS_CONSUMED_CPL - R - 32 bits - PCIEIND_P:0x32			
Field Name	**Bits**	**Default**	**Description**
TX_CREDITS_CONSUMED_CPLD	11:0	0x0	For completion TLP data, total number of FC units consumed by TLP transmission made since FC initialization, modulo 4096.
TX_CREDITS_CONSUMED_CPLH	23:16	0x0	For completion TLP header, total number of FC units consumed by TLP transmission made since FC initialization, modulo 256.
TX Credits Consumed Register (Completion)			

PCIE_TX_CREDITS_LIMIT_P - R - 32 bits - PCIEIND_P:0x33			
Field Name	**Bits**	**Default**	**Description**
TX_CREDITS_LIMIT_PD	11:0	0x0	For posted TLP data, total number of FC units advertised by the receiver since FC initialization, modulo 4096.
TX_CREDITS_LIMIT_PH	23:16	0x0	For posted TLP header, total number of FC units advertised by the receiver since FC initialization, modulo 256.
TX Credits Limit Register (Posted)			

PCIE_TX_CREDITS_LIMIT_NP - R - 32 bits - PCIEIND_P:0x34			
Field Name	**Bits**	**Default**	**Description**
TX_CREDITS_LIMIT_NPD	11:0	0x0	For non-posted TLP data, total number of FC units advertised by the receiver since FC initialization, modulo 4096.
TX_CREDITS_LIMIT_NPH	23:16	0x0	For non-posted TLP header, total number of FC units advertised by the receiver since FC initialization, modulo 256.
TX Credits Limit Register (Non-Posted)			

PCIE_TX_CREDITS_LIMIT_CPL - R - 32 bits - PCIEIND_P:0x35			
Field Name	**Bits**	**Default**	**Description**
TX_CREDITS_LIMIT_CPLD	11:0	0x0	For completion TLP data, total number of FC units advertised by the receiver since FC initialization, modulo 4096.
TX_CREDITS_LIMIT_CPLH	23:16	0x0	For completion TLP header, total number of FC units advertised by the receiver since FC initialization, modulo 256.
TX Credits Limit Register (Completion)			

PCIE_RX_VENDOR_SPECIFIC - R - 32 bits - PCIEIND_P:0x72			
Field Name	**Bits**	**Default**	**Description**
RX_VENDOR_DATA	23:0	0x0	Writing to this register will re-arm to capture the next Vendor Specific DLLP.
RX_VENDOR_STATUS	24	0x0	Indicates that a Vendor Specific DLLP was decoded, and Vendor Data was captured.
RX Vendor Specific DLLP			

PCIE_RX_CREDITS_ALLOCATED_P - R - 32 bits - PCIEIND_P:0x80			
Field Name	**Bits**	**Default**	**Description**
RX_CREDITS_ALLOCATED_PD	11:0	0x0	For posted TLP data, the number of FC units granted to transmitter since initialization, modulo 4096.
RX_CREDITS_ALLOCATED_PH	23:16	0x0	For posted TLP header, the number of FC units granted to transmitter since initialization, modulo 256.
RX Credits Allocated Register (Posted)			

PCIE_RX_CREDITS_ALLOCATED_NP - R - 32 bits - PCIEIND_P:0x81			
Field Name	**Bits**	**Default**	**Description**
RX_CREDITS_ALLOCATED_NPD	11:0	0x0	For non-posted TLP data, the number of FC units granted to transmitter since initialization, modulo 4096.
RX_CREDITS_ALLOCATED_NPH	23:16	0x0	For non-posted TLP header, the number of FC units granted to transmitter since initialization, modulo 256.
RX Credits Allocated Register (Non-Posted)			

PCIE_RX_CREDITS_ALLOCATED_CPL - R - 32 bits - PCIEIND_P:0x82			
Field Name	**Bits**	**Default**	**Description**
RX_CREDITS_ALLOCATED_CPLD	11:0	0x0	For completion TLP data, the number of FC units granted to transmitter since initialization, modulo 4096.
RX_CREDITS_ALLOCATED_CPLH	23:16	0x0	For completion TLP header, the number of FC units granted to transmitter since initialization, modulo 256.
RX Credits Allocated Register (Completion)			

PCIE_RX_CREDITS_RECEIVED_P - R - 32 bits - PCIEIND_P:0x83

Field Name	Bits	Default	Description
RX_CREDITS_RECEIVED_PD	11:0	0x0	For posted TLP data, the number of FC units consumed by valid TLP received since initialization, modulo 4096.
RX_CREDITS_RECEIVED_PH	23:16	0x0	For posted TLP header, the number of FC units consumed by valid TLP received since initialization, modulo 256.
RX Credits Received Register (Posted)			

PCIE_RX_CREDITS_RECEIVED_NP - R - 32 bits - PCIEIND_P:0x84

Field Name	Bits	Default	Description
RX_CREDITS_RECEIVED_NPD	11:0	0x0	For non-posted TLP data, the number of FC units consumed by valid TLP received since initialization, modulo 4096.
RX_CREDITS_RECEIVED_NPH	23:16	0x0	For non-posted TLP header, the number of FC units consumed by valid TLP received since initialization, modulo 256.
RX Credits Received Register (Non-Posted)			

PCIE_RX_CREDITS_RECEIVED_CPL - R - 32 bits - PCIEIND_P:0x85

Field Name	Bits	Default	Description
RX_CREDITS_RECEIVED_CPLD	11:0	0x0	For completion TLP data, the number of FC units consumed by valid TLP received since initialization, module 4096.
RX_CREDITS_RECEIVED_CPLH	23:16	0x0	For completion TLP header, the number of FC units consumed by valid TLP received since initialization, module 256.
RX Credits Received Register (Completion)			

PCIE_LC_N_FTS_CNTL - RW - 32 bits - PCIEIND_P:0xA3

Field Name	Bits	Default	Description
LC_XMIT_N_FTS	7:0	0xc	Number of FTS to override the strap values
LC_XMIT_N_FTS_OVERRIDE_EN	8	0x0	Enables the previous field to override the strap value.
LC_XMIT_N_FTS_LIMIT	23:16	0xff	Limits that the number of FTS can increment to when incrementing is enabled.
LC_N_FTS (R)	31:24	0x0	Number of FTS captured from the other end of the link.
LC Number of FTS Control			

ROOT_CNTL - RW - 16 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0x74]			
Field Name	**Bits**	**Default**	**Description**
SERR_ON_CORR_ERR_EN	0	0x0	System Error on Correctable Error Enable. Indicates that a System Error should be generated if a correctable error is reported by any of the devices in the hierarchy associated with this Root Port.
SERR_ON_NONFATAL_ERR_EN	1	0x0	System Error on Non-Fatal Error Enable. Indicates that a System Error should be generated if a Non-fatal error is reported by any of the devices in the hierarchy associated with this Root Port.
SERR_ON_FATAL_ERR_EN	2	0x0	System Error on Fatal Error Enable. Indicates that a System Error should be generated if a Fatal error is reported by any of the devices in the hierarchy associated with this Root Port.
PM_INTERRUPT_EN	3	0x0	PME Interrupt Enable. Enables interrupt generation upon receipt of a PME Message.
CRS_SOFTWARE_VISIBILITY_EN	4	0x0	
The Root Control register controls PCI Express Root Complex specific parameters.			

ROOT_CAP - RW - 16 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0x76]			
Field Name	**Bits**	**Default**	**Description**
CRS_SOFTWARE_VISIBILITY (R)	0	0x1	

MSI_CAP_LIST - R - 16 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0x80]			
Field Name	**Bits**	**Default**	**Description**
CAP_ID	7:0	0x5	Identifies if a device function is MSI capable.
NEXT_PTR	15:8	0xb0	Pointer to the next item on the capabilities list.
Message Signaled Interrupt Capability Registers			

PCIE_CFG_SCRATCH - RW - 32 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0xC0]			
Field Name	**Bits**	**Default**	**Description**
SCRATCH	31:0	0x0	PCI Express Scratch register

PCIE_VC_ENH_CAP_HDR - R - 32 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0x100]			
Field Name	**Bits**	**Default**	**Description**
CAP_ID	15:0	0x2	This field is a PCI-SIG defined ID number that indicates the nature and format of the extended capability.
CAP_VER	19:16	0x1	This field is a PCI-SIG defined version number that indicates the version of the capability structure present.
NEXT_PTR	31:20	0x140	This field contains the offset to the next PCI Express capability structure or 000h if no other items exist in the linked list of capabilities.
Virtual Channel Enhanced Capability Header			

PCIE_PORT_VC_CAP_REG1 - R - 32 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0x104]			
Field Name	**Bits**	**Default**	**Description**
EXT_VC_COUNT	2:0	0x0	Indicates the number of (extended) Virtual Channels in addition to the default VC supported by the device. This field is valid for all devices.
LOW_PRIORITY_EXT_VC_COUNT	6:4	0x0	Indicates the number of (extended) Virtual Channels in addition to the default VC belonging to the low-priority VC group
REF_CLK	9:8	0x0	Indicates the reference clock for Virtual Channels that support time-based WRR Port Arbitration.
PORT_ARB_TABLE_ENTRY_SIZE	11:10	0x0	Indicates the size (in bits) of Port Arbitration table entry in the device.
Port VC Capability Register 1			

PCIE_PORT_VC_CAP_REG2 - R - 32 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0x108]			
Field Name	**Bits**	**Default**	**Description**
VC_ARB_CAP	7:0	0x0	Indicates the types of VC Arbitration supported by the device for the Low Priority Virtual Channel group
VC_ARB_TABLE_OFFSET	31:24	0x0	Indicates the location of the VC Arbitration Table.
Port VC Capability Register 2			

PCIE_PORT_VC_CNTL - RW - 16 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0x10C]			
Field Name	**Bits**	**Default**	**Description**
LOAD_VC_ARB_TABLE (R)	0	0x0	Used for software to update the VC Arbitration Table.
VC_ARB_SELECT	3:1	0x0	Used for software to configure the VC arbitration by selecting one of the supported VC Arbitration schemes
Port VC Control Register			

PCIE_PORT_VC_STATUS - R - 16 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0x10E]			
Field Name	**Bits**	**Default**	**Description**
VC_ARB_TABLE_STATUS	0	0x0	Indicates the coherency status of the VC Arbitration Table
Port VC Status Register			

PCIE_VC1_RESOURCE_CAP - R - 32 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0x11C]			
Field Name	**Bits**	**Default**	**Description**
PORT_ARB_CAP	7:0	0x0	Indicates types of Port Arbitration supported by the VC resource.
REJECT_SNOOP_TRANS	15	0x1	When set to zero, transactions with or without the No Snoop bit set within the TLP Header are allowed on this VC
MAX_TIME_SLOTS	21:16	0x0	Indicates the maximum number of time slots that the VC resource is capable of supporting
PORT_ARB_TABLE_OFFSET	31:24	0x0	Indicates the location of the Port Arbitration Table associated with the VC resource.
VC1 Resource Capability Register			

PCIE_VC1_RESOURCE_CNTL - RW - 32 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0x120]			
Field Name	**Bits**	**Default**	**Description**
TC_VC_MAP_TC0 (R)	0	0x0	Indicates the TCs that are mapped to the VC resource
TC_VC_MAP_TC1_7	7:1	0x0	Indicates the TCs that are mapped to the VC resource
LOAD_PORT_ARB_TABLE (R)	16	0x0	Updates the Port Arbitration logic from the Port Arbitration Table for the VC resource.
PORT_ARB_SELECT	19:17	0x0	Configures the VC resource to provide a particular Port Arbitration service.
VC_ID	26:24	0x0	Assigns a VC ID to the VC resource
VC_ENABLE	31	0x0	Enables a Virtual Channel.
VC1 Resource Control Register			

PCIE_VC1_RESOURCE_STATUS - R - 16 bits - [pcieConfigDev10 pcieConfigDev2 pcieConfigDev3 pcieConfigDev4 pcieConfigDev5 pcieConfigDev6 pcieConfigDev7 pcieConfigDev8,pcieConfigDev9:0x124]			
Field Name	**Bits**	**Default**	**Description**
PORT_ARB_TABLE_STATUS	0	0x0	Indicates the coherency status of the Port Arbitration Table associated with the VC resource.
VC_NEGOTIATION_PENDING	1	0x1	Indicates whether the Virtual Channel negotiation (initialization or disabling) is in pending state.
VC1 Resource Status Register			

2.3   Graphics Controller Configuration Registers

DEVICE_ID - R - 16 bits - [gcconfig:0x2] [MMReg:0x5002]			
Field Name	**Bits**	**Default**	**Description**
DEVICE_ID	15:0	0x0	Device Identification.

VENDOR_ID - R - 16 bits - [gcconfig:0x0] [MMReg:0x5000]			
Field Name	**Bits**	**Default**	**Description**
VENDOR_ID	15:0	0x1002	Vendor Identification

COMMAND - RW - 16 bits - [gcconfig:0x4] [MMReg:0x5004]:R			
Field Name	**Bits**	**Default**	**Description**
IO_ACCESS_EN	0	0x0	1=Enable IO Space access
MEM_ACCESS_EN	1	0x0	1=Enable MEM Space access
BUS_MASTER_EN	2	0x0	1=Enable Core Busmastering
SPECIAL_CYCLE_EN (R)	3	0x0	Fix=0. No support for special cycles.
MEM_WRITE_INVALIDATE_EN (R)	4	0x0	Fix=0. No support for memory write and invalidate.
PAL_SNOOP_EN (R)	5	0x0	Fix=0. No palette snooping.
PARITY_ERROR_EN	6	0x0	0=PERR# is not asserted. Continue normal operation
SERR_EN	8	0x0	0=Disable SERR# driver
FAST_B2B_EN (R)	9	0x0	1=Master is allowed to generate back-to-back transactions to different agents 0=Back-to-back transactions only allowed to same agent
INT_DIS	10	0x0	0=Enable INTx# assertion 1=Disables the assertion of INTx#

STATUS - RW - 16 bits - [gcconfig:0x6] [MMReg:0x5006]:R			
Field Name	**Bits**	**Default**	**Description**
INT_STATUS (R)	3	0x0	State of the Interrupt
CAP_LIST (R)	4	0x1	0=No Capabilities exist 1=Capability pointer found at 0x34
PCI_66_EN (R)	5	0x0	0=33MHz Capable 1=66MHz Capable
FAST_BACK_CAPABLE (R)	7	0x0	0=Not capable of accepted back-to-back transactions 1=Capable of accepting back-to-back transactions
DEVSEL_TIMING (R)	10:9	0x0	00=Fast 01=Medium 10=Slow 11=Reserved
RECEIVED_MASTER_ABORT	13	0x0	Master address did not decode. Write '1' to clear.

REVISION_ID - R - 8 bits - [gcconfig:0x8] [MMReg:0x5008]			
Field Name	**Bits**	**Default**	**Description**
MINOR_REV_ID	3:0	0x0	Revision Identification
MAJOR_REV_ID	7:4	0x0	Revision Identification

IO_BASE - RW - 32 bits - [gcconfig:0x20] [MMReg:0x5020]:R			
Field Name	**Bits**	**Default**	**Description**
BLOCK_IO_BIT (R)	0	0x1	0=Memory space 1=IO space
IO_BASE	31:8	0x0	Base address register for IO

ADAPTER_ID_W - RW - 32 bits - [gcconfig:0x4C] [MMReg:0x504C]:R			
Field Name	**Bits**	**Default**	**Description**
SUBSYSTEM_VENDOR_ID	15:0	0x1002	Desired subsystem vendor ID.
SUBSYSTEM_ID	31:16	0x7941	Desired subsystem ID.

BASE_CODE - R - 8 bits - [gcconfig:0xB] [MMReg:0x500B]			
Field Name	**Bits**	**Default**	**Description**
BASE_CLASS_CODE	7:0	0x3	FIXED. 3=Display controller

ADAPTER_ID - R - 32 bits - [gcconfig:0x2C] [MMReg:0x502C]			
Field Name	**Bits**	**Default**	**Description**
SUBSYSTEM_VENDOR_ID *(mirror of ADAPTER_ID_W:SUBSYSTEM_VENDOR_ID)*	15:0	0x0	Device Identification.
SUBSYSTEM_ID *(mirror of ADAPTER_ID_W:SUBSYSTEM_ID)*	31:16	0x0	Device Identification.

SUB_CLASS - R - 8 bits - [gcconfig:0xA] [MMReg:0x500A]			
Field Name	**Bits**	**Default**	**Description**
SUB_CLASS_INF	7	0x0	FIXED. 0=VGA Compatible

BIST - R - 8 bits - [gcconfig:0xF] [MMReg:0x500F]			
Field Name	**Bits**	**Default**	**Description**
BIST_COMP	3:0	0x0	BIST (Built-in Self Test) register. Not supported.
BIST_STRT	6	0x0	BIST (Built-in Self Test) register. Not supported.
BIST_CAP	7	0x0	BIST (Built-in Self Test) register. Not supported.

CAPABILITIES_PTR - R - 32 bits - [gcconfig:0x34] [MMReg:0x5034]			
Field Name	**Bits**	**Default**	**Description**
CAP_PTR	7:0	0x50	Capabilities Pointer.

CONFIG_CNTL - RW - 32 bits - [IOReg,MMReg:0xE0]			
Field Name	**Bits**	**Default**	**Description**

CFG_VGA_RAM_EN
 	
(mirror of GENMO_WT:VGA_RAM_EN)
	8	0x0	Enables Memory cycles to VGA.
			    0=Disable
			    1=Enable

CFG_VGA_IO_DIS	9	0x0	Allows register cycles to VGA.
CFG_ATI_REV_ID	19:16	0x0	Core Revision ID.

CONFIG_MEMSIZE - RW - 32 bits - [IOReg,MMReg:0xF8]			
Field Name	**Bits**	**Default**	**Description**
CONFIG_MEMSIZE	31:0	0x0	Scratch register for the BIOS to inform driver memory size. Note: Bits [19:0] of this field are hardwired to 0.

CONFIG_APER_SIZE - R - 32 bits - [MMReg:0x108]			
Field Name	**Bits**	**Default**	**Description**
APER_SIZE	31:0	0x0	FB Aperture size readback. Note: Bits [23:0] of this field are hardwired to 0.

CONFIG_REG_APER_SIZE - R - 32 bits - [MMReg:0x114]

Field Name	Bits	Default	Description
REG_APER_SIZE	18:0	0x8000	MMReg Aperture Size readback.

HEADER - R - 8 bits - [gcconfig:0xE] [MMReg:0x500E]

Field Name	Bits	Default	Description
HEADER_TYPE	6:0	0x0	FIXED. 0x0=Type 00h space header
DEVICE_TYPE	7	0x0	FIXED. 1=Multifunction device

INTERRUPT_LINE - RW - 8 bits - [gcconfig:0x3C] [MMReg:0x503C]:R

Field Name	Bits	Default	Description
INTERRUPT_LINE	7:0	0xff	Scratch Register used to communicate routing information.

INTERRUPT_PIN - R - 8 bits - [gcconfig:0x3D] [MMReg:0x503D]

Field Name	Bits	Default	Description
INTERRUPT_PIN	3:0	0x1	1=INTA# 2=INTB#

LATENCY - RW - 8 bits - [gcconfig:0xD] [MMReg:0x500D]:R

Field Name	Bits	Default	Description
LATENCY_TIMER	7:0	0x0	Specifies in units of PCI bus clocks the value of the Latency Timer.

MAX_LATENCY - R - 8 bits - [gcconfig:0x3F] [MMReg:0x503F]

Field Name	Bits	Default	Description
MAX_LAT	7:0	0x0	Desired value for the Latency Timer. 0=No major requirements

REGPROG_INF - R - 8 bits - [gcconfig:0x9] [MMReg:0x5009]

Field Name	Bits	Default	Description
REG_LEVEL_PROG_INF	7:0	0x0	FIXED. 0=A_0000 through B_0000. I/O 3B0h to 3BBh, 3C0h to 3DFh and all aliases.

CACHE_LINE - RW - 8 bits - [gcconfig:0xC] [MMReg:0x500C]:R

Field Name	Bits	Default	Description
CACHE_LINE_SIZE	7:0	0x0	Specifies the system cacheline size in units of DWORDs.

MIN_GRANT - R - 8 bits - [gcconfig:0x3E] [MMReg:0x503E]

Field Name	Bits	Default	Description
MIN_GNT	7:0	0x0	Length of desired burst period assuming 33MHz. 0=No major requirements

MEM_BASE_LO - RW - 32 bits - [gcconfig:0x10] [MMReg:0x5010]:R

Field Name	Bits	Default	Description
BLOCK_MEM_BIT (R)	0	0x0	0=Memory space 1=IO space
BLOCK_MEM_TYPE (R)	2:1	0x2	10=Locate anywhere in 64 bit address space
PFTCH_MEM_EN (R)	3	0x1	1=Prefetchable
MEM_BASE_LO	31:25	0x0	Lower Memory Base Address

MEM_BASE_HI - RW - 32 bits - [gcconfig:0x14] [MMReg:0x5014]:R

Field Name	Bits	Default	Description
MEM_BASE_HI	31:0	0x0	Upper Memory Base Address.

REG_BASE_LO - RW - 32 bits - [gcconfig:0x18] [MMReg:0x5018]:R

Field Name	Bits	Default	Description
BLOCK_REG_BIT (R)	0	0x0	0=Memory space 1=IO space
BLOCK_REG_TYPE (R)	2:1	0x2	10=locate anywhere in 64 bit address space
PFTCH_REG_EN (R)	3	0x0	0=Not prefetchable
REG_BASE_LO	31:16	0x0	Lower Register Base Address

REG_BASE_HI - RW - 32 bits - [gcconfig:0x1C] [MMReg:0x501C]:R

Field Name	Bits	Default	Description
REG_BASE_HI	31:0	0x0	Upper Register Base Address

MSI_CAP_ID - R - 8 bits - [gcconfig:0x80] [MMReg:0x5080]

Field Name	Bits	Default	Description
MSI_CAP_ID	7:0	0x5	MSI Capability ID.

MSI_NXT_CAP_PTR - R - 8 bits - [gcconfig:0x81] [MMReg:0x5081]

Field Name	Bits	Default	Description
MSI_NXT_CAP_PTR	7:0	0x0	The last item in capabilities list.

MSI_MSG_CNTL - RW - 16 bits - [gcconfig:0x82] [MMReg:0x5082]:R

Field Name	Bits	Default	Description
MSI_EN	0	0x0	1=Enable MSI messaging
MSI_MULTMSG_CAP (R)	3:1	0x0	The number of requested messages.
MSI_MULTMSG_EN	6:4	0x0	000=1 message allocated 001=2 messages allocated 010=4 messages allocated 011=8 messages allocated 100=16 messages allocated 101=32 messages allocated 110=Reserved 111=Reserved
MSI_64BIT (R)	7	0x1	64 bit messaging enabled.

MSI_MSG_ADDR_LO - RW - 32 bits - [gcconfig:0x84] [MMReg:0x5084]:R

Field Name	Bits	Default	Description
MSI_MSG_ADDR_LO	31:2	0x0	System-specified message lower address.

MSI_MSG_ADDR_HI - RW - 32 bits - [gcconfig:0x88] [MMReg:0x5088]:R

Field Name	Bits	Default	Description
MSI_MSG_ADDR_HI	31:0	0x0	System-specified message upper address.

MSI_MSG_DATA - RW - 16 bits - [gcconfig:0x8C] [MMReg:0x508C]:R

Field Name	Bits	Default	Description
MSI_DATA	15:0	0x0	System-specified message.

F1_VENDOR_ID - R - 16 bits - [gcconfig:0x100] [MMReg:0x5100]

Field Name	Bits	Default	Description
F1_VENDOR_ID	15:0	0x1002	Vendor ID register.

F1_DEVICE_ID - R - 16 bits - [gcconfig:0x102] [MMReg:0x5102]

Field Name	Bits	Default	Description
F1_DEVICE_ID	15:0	0x0	Device ID register.

F1_COMMAND - RW - 16 bits - [gcconfig:0x104] [MMReg:0x5104]:R

Field Name	Bits	Default	Description
F1_MEM_ACCESS_EN	1	0x0	1=Enable MEM Space access
F1_BUS_MASTER_EN	2	0x0	1=Enable Core Busmastering

F1_STATUS - R - 16 bits - [gcconfig:0x106] [MMReg:0x5106]

Field Name	Bits	Default	Description
F1_CAP_LIST	4	0x1	0=No Capabilities exist 1=Capability pointer found at 0x34

F1_REVISION_ID - R - 8 bits - [gcconfig:0x108] [MMReg:0x5108]

Field Name	Bits	Default	Description
F1_MINOR_REV_ID	3:0	0x0	Revision Identification.
F1_MAJOR_REV_ID	7:4	0x0	Revision Identification.

F1_REGPROG_INF - R - 8 bits - [gcconfig:0x109] [MMReg:0x5109]

Field Name	Bits	Default	Description
F1_REG_LEVEL_PROG_INF	7:0	0x0	Reserved.

F1_SUB_CLASS - R - 8 bits - [gcconfig:0x10A] [MMReg:0x510A]			
Field Name	**Bits**	**Default**	**Description**
F1_SUB_CLASS_INF	7	0x1	Fixed. 1=XGA Compatible

F1_BASE_CODE - R - 8 bits - [gcconfig:0x10B] [MMReg:0x510B]			
Field Name	**Bits**	**Default**	**Description**
F1_BASE_CLASS_CODE	7:0	0x3	Fixed. 3=Display Controller

F1_CACHE_LINE - RW - 8 bits - [gcconfig:0x10C] [MMReg:0x510C]:R			
Field Name	**Bits**	**Default**	**Description**
F1_CACHE_LINE_SIZE	7:0	0x0	Specifies the system cacheline size in units of DWORDs

F1_LATENCY - RW - 8 bits - [gcconfig:0x10D] [MMReg:0x510D]:R			
Field Name	**Bits**	**Default**	**Description**
F1_LATENCY_TIMER	7:0	0x0	Specifies in units of PCI bus clocks the value of the Latency Timer.

F1_HEADER - R - 8 bits - [gcconfig:0x10E] [MMReg:0x510E]			
Field Name	**Bits**	**Default**	**Description**
F1_HEADER_TYPE	6:0	0x0	Reserved. See F0 configuration space.
F1_DEVICE_TYPE	7	0x0	Reserved. See F0 configuration space.

F1_BIST - R - 8 bits - [gcconfig:0x10F] [MMReg:0x510F]			
Field Name	**Bits**	**Default**	**Description**
F1_BIST_COMP	3:0	0x0	BIST (Built-in Self Test) register. Not supported.
F1_BIST_STRT	6	0x0	BIST (Built-in Self Test) register. Not supported.
F1_BIST_CAP	7	0x0	BIST (Built-in Self Test) register. Not supported.

F1_REG_BASE_LO - RW - 32 bits - [gcconfig:0x110] [MMReg:0x5114]:R

Field Name	Bits	Default	Description
F1_BLOCK_REG_BIT (R)	0	0x0	0=Memory space 1=IO space
F1_BLOCK_REG_TYPE (R)	2:1	0x2	10=locate anywhere in 64 bit address space
F1_PFTCH_REG_EN (R)	3	0x0	0=Not prefetchable
F1_REG_BASE_LO	31:16	0x0	Lower Register Base Address

F1_REG_BASE_HI - RW - 32 bits - [gcconfig:0x114] [MMReg:0x511C]:R

Field Name	Bits	Default	Description
F1_REG_BASE_HI	31:0	0x0	Upper Register Base Address

F1_ADAPTER_ID - R - 32 bits - [gcconfig:0x12C] [MMReg:0x512C]

Field Name	Bits	Default	Description
F1_SUBSYSTEM_VENDOR_ID *(mirror of ADAPTER_ID_W:SUBSYSTEM_VENDOR_ID)*	15:0	0x0	Device Identification.
F1_SUBSYSTEM_ID *(mirror of F1_ADAPTER_ID_W:F1_SUBSYSTEM_ID)*	31:16	0x0	Device Identification.

F1_CAPABILITIES_PTR - R - 32 bits - [gcconfig:0x134] [MMReg:0x5134]

Field Name	Bits	Default	Description
F1_CAP_PTR	7:0	0x50	Capabilities Pointer

F1_INTERRUPT_LINE - RW - 8 bits - [gcconfig:0x13C] [MMReg:0x513C]:R

Field Name	Bits	Default	Description
F1_INTERRUPT_LINE	7:0	0x0	Scratch Register used to communicate routing information.

F1_INTERRUPT_PIN - R - 8 bits - [gcconfig:0x13D] [MMReg:0x513D]

Field Name	Bits	Default	Description
F1_INTERRUPT_PIN	3:0	0x1	1=INTA# 2=INTB#

F1_MIN_GRANT - R - 8 bits - [gcconfig:0x13E] [MMReg:0x513E]			
Field Name	**Bits**	**Default**	**Description**
F1_MIN_GNT	7:0	0x0	Length of desired burst period assuming 33MHz. 0=No major requirements

F1_MAX_LATENCY - R - 8 bits - [gcconfig:0x13F] [MMReg:0x513F]			
Field Name	**Bits**	**Default**	**Description**
F1_MAX_LAT	7:0	0x0	Desired value for the Latency Timer 0=No major requirements

F1_PMI_CAP_ID - R - 8 bits - [gcconfig:0x150] [MMReg:0x5150]			
Field Name	**Bits**	**Default**	**Description**
F1_PMI_CAP_ID	7:0	0x1	

F1_PMI_NXT_CAP_PTR - R - 8 bits - [gcconfig:0x151] [MMReg:0x5151]			
Field Name	**Bits**	**Default**	**Description**
F1_PMI_NXT_CAP_PTR	7:0	0x0	The last item.

F1_PMI_PMC_REG - R - 16 bits - [gcconfig:0x152] [MMReg:0x5152]			
Field Name	**Bits**	**Default**	**Description**
F1_PMI_VERSION	2:0	0x2	
F1_PMI_PME_CLOCK	3	0x0	
F1_PMI_DEV_SPECIFIC_INIT	5	0x0	
F1_PMI_D1_SUPPORT	9	0x1	
F1_PMI_D2_SUPPORT	10	0x1	
F1_PMI_PME_SUPPORT	15:11	0x0	

F1_PMI_DATA - R - 8 bits - [gcconfig:0x157] [MMReg:0x5157]			
Field Name	**Bits**	**Default**	**Description**
F1_PMI_DATA	7:0	0x0	

PMI_STATUS - RW - 16 bits - [gcconfig:0x54] [MMReg:0x5054]:R

Field Name	Bits	Default	Description

PMI_POWER_STATE	1:0	0x0	2-bit field used to determine the current power state and to set a new power state.
			
			READ_BACK
			  00=D0 state
			  01=D1 state
			  10=D2 state
			  11=D3 state
			
			WRITE
			  00=D0 state
			  01=D1 state
			  10=D2 state
			  11=D3 state

PMI_PME_EN (R)	8	0x0	PME not supported
PMI_DATA_SELECT (R)	12:9	0x0	Data select not implemented
PMI_DATA_SCALE (R)	14:13	0x0	Data scale not implemented
PMI_PME_STATUS (R)	15	0x0	PME not supported

F1_ADAPTER_ID_W - RW - 32 bits - [gcconfig:0x14C] [MMReg:0x514C]:R

Field Name	Bits	Default	Description
F1_SUBSYSTEM_ID	31:16	0x7939	Desired F1 subsystem ID.

F1_PMI_STATUS - RW - 16 bits - [gcconfig:0x154] [MMReg:0x5154]:R

Field Name	Bits	Default	Description
F1_PMI_POWER_STATE	1:0	0x0	
F1_PMI_PME_EN (R)	8	0x0	
F1_PMI_DATA_SELECT (R)	12:9	0x0	
F1_PMI_DATA_SCALE (R)	14:13	0x0	
F1_PMI_PME_STATUS (R)	15	0x0	

F2_VENDOR_ID - R - 16 bits - [gcconfig:0x200] [MMReg:0x5200]

Field Name	Bits	Default	Description
F2_VENDOR_ID	15:0	0x1002	Vendor ID register

F2_DEVICE_ID - R - 16 bits - [gcconfig:0x202] [MMReg:0x5202]

Field Name	Bits	Default	Description
F2_DEVICE_ID	15:0	0x0	Device ID register

F2_COMMAND - RW - 16 bits - [gcconfig:0x204] [MMReg:0x5204]:R			
Field Name	**Bits**	**Default**	**Description**
F2_MEM_ACCESS_EN	1	0x0	1=Enable MEM Space access
F2_BUS_MASTER_EN	2	0x0	1=Enable Core Busmastering
F2_INTR_DIS	10	0x0	0=Enable INTx# assertion
			1=Disable the assertion of INTx#

F2_STATUS - R - 16 bits - [gcconfig:0x206] [MMReg:0x5206]			
Field Name	**Bits**	**Default**	**Description**
F2_INT_STATUS	3	0x0	State of the Interrupt
F2_CAP_LIST	4	0x1	0=No Capabilities exist
			1=Capability pointer found at 0x34
F2_DEVSEL_TIMING	10:9	0x0	00=Fast
			01=Medium
			10=Slow
			11=Reserved

F2_REVISION_ID - R - 8 bits - [gcconfig:0x208] [MMReg:0x5208]			
Field Name	**Bits**	**Default**	**Description**
F2_MINOR_REV_ID	3:0	0x0	Revision ID register
F2_MAJOR_REV_ID	7:4	0x0	Revision ID register

F2_REGPROG_INF - R - 8 bits - [gcconfig:0x209] [MMReg:0x5209]			
Field Name	**Bits**	**Default**	**Description**
F2_REG_LEVEL_PROG_INF	7:0	0x0	Reserved

F2_SUB_CLASS - R - 8 bits - [gcconfig:0x20A] [MMReg:0x520A]			
Field Name	**Bits**	**Default**	**Description**
F2_SUB_CLASS_INF	7:0	0x3	FIXED.
			3=Other multimedia device

F2_BASE_CODE - R - 8 bits - [gcconfig:0x20B] [MMReg:0x520B]			
Field Name	**Bits**	**Default**	**Description**
F2_BASE_CLASS_CODE	7:0	0x4	FIXED. 4 = Multimedia device

F2_CACHE_LINE - RW - 8 bits - [gcconfig:0x20C] [MMReg:0x520C]:R			
Field Name	**Bits**	**Default**	**Description**
F2_CACHE_LINE_SIZE	7:0	0x0	CacheLine Size register.

F2_LATENCY - RW - 8 bits - [gcconfig:0x20D] [MMReg:0x520D]:R			
Field Name	**Bits**	**Default**	**Description**
F2_LATENCY_TIMER	7:0	0x0	Latency Timer register.

F2_HEADER - R - 8 bits - [gcconfig:0x20E] [MMReg:0x520E]			
Field Name	**Bits**	**Default**	**Description**
F2_HEADER_TYPE	6:0	0x0	Reserved. See F0 config space
F2_DEVICE_TYPE	7	0x0	Reserved. See F0 config space

F2_BIST - R - 8 bits - [gcconfig:0x20F] [MMReg:0x520F]			
Field Name	**Bits**	**Default**	**Description**
F2_BIST_COMP	3:0	0x0	BIST (Built-in Self Test) register, not supported
F2_BIST_STRT	6	0x0	BIST (Built-in Self Test) register, not supported
F2_BIST_CAP	7	0x0	BIST (Built-in Self Test) register, not supported

F2_REG_BASE_LO - RW - 32 bits - [gcconfig:0x210] [MMReg:0x5210]:R			
Field Name	**Bits**	**Default**	**Description**
F2_BLOCK_REG_BIT (R)	0	0x0	0=Memory space 1=IO space
F2_BLOCK_REG_TYPE (R)	2:1	0x2	10=Locate anywhere in 64 bit address space
F2_PFTCH_REG_EN (R)	3	0x0	0=Not prefetchable
F2_REG_BASE_LO	31:14	0x0	Lower Register Base Address

F2_REG_BASE_HI - RW - 32 bits - [gcconfig:0x214] [MMReg:0x5214]:R

Field Name	Bits	Default	Description
F2_REG_BASE_HI	31:0	0x0	Upper Register Base Address

F2_ADAPTER_ID - R - 32 bits - [gcconfig:0x22C] [MMReg:0x522C]

Field Name	Bits	Default	Description
F2_SUBSYSTEM_VENDOR_ID *(mirror of F2_ADAPTER_ID_W:F2_SUBSYSTEM_VENDOR_ID)*	15:0	0x0	Device Identification
F2_SUBSYSTEM_ID *(mirror of F2_ADAPTER_ID_W:F2_SUBSYSTEM_ID)*	31:16	0x0	Device Identification

F2_CAPABILITIES_PTR - R - 32 bits - [gcconfig:0x234] [MMReg:0x5234]

Field Name	Bits	Default	Description
F2_CAP_PTR	7:0	0x50	Capabilities Pointer

F2_INTERRUPT_LINE - RW - 8 bits - [gcconfig:0x23C] [MMReg:0x523C]:R

Field Name	Bits	Default	Description
F2_INTERRUPT_LINE	7:0	0x0	Scratch Register used to communicate routing information

F2_INTERRUPT_PIN - R - 8 bits - [gcconfig:0x23D] [MMReg:0x523D]

Field Name	Bits	Default	Description
F2_INTERRUPT_PIN	3:0	0x1	1=INTA# 2=INTB#

F2_MIN_GRANT - R - 8 bits - [gcconfig:0x23E] [MMReg:0x523E]

Field Name	Bits	Default	Description
F2_MIN_GNT	7:0	0x0	Length of desired burst period assuming 33MHz 0=No major requirements

F2_MAX_LATENCY - R - 8 bits - [gcconfig:0x23F] [MMReg:0x523F]

Field Name	Bits	Default	Description
F2_MAX_LAT	7:0	0x0	Desired value for Latency Timer 0=No major requirements

F2_ADAPTER_ID_W - RW - 32 bits - [gcconfig:0x24C] [MMReg:0x524C]:R

Field Name	Bits	Default	Description
F2_SUBSYSTEM_VENDOR_ID	15:0	0x1002	Desired subsystem vendor ID.
F2_SUBSYSTEM_ID	31:16	0x0	Desired subsystem ID.

F2_PMI_CAP_ID - R - 8 bits - [gcconfig:0x250] [MMReg:0x5250]

Field Name	Bits	Default	Description
F2_PMI_CAP_ID	7:0	0x1	FIX=0x1 per spec

F2_PMI_NXT_CAP_PTR - R - 8 bits - [gcconfig:0x251] [MMReg:0x5251]

Field Name	Bits	Default	Description
F2_PMI_NXT_CAP_PTR	7:0	0x60	Next item is MSI

F2_PMI_PMC_REG - R - 16 bits - [gcconfig:0x252] [MMReg:0x5252]

Field Name	Bits	Default	Description
F2_PMI_VERSION	2:0	0x2	Revision 1.1 supported
F2_PMI_PME_CLOCK	3	0x0	PME clock not required
F2_PMI_DEV_SPECIFIC_INIT	5	0x0	No special initialization required
F2_PMI_D1_SUPPORT	9	0x0	D1 state not supported
F2_PMI_D2_SUPPORT	10	0x0	D2 state not supported
F2_PMI_PME_SUPPORT	15:11	0x0	No PME support

F2_PMI_STATUS - RW - 16 bits - [gcconfig:0x254] [MMReg:0x5254]:R			
Field Name	**Bits**	**Default**	**Description**

F2_PMI_POWER_STATE	1:0	0x0	2-bit field used to determine the current power state and to set a new power state.
			
			READ_BACK
			  00=D0 state
			  01=D1 state
			  10=D2 state
			  11=D3 state
			
			WRITE
			  00=D0 state
			  01=D1 state
			  10=D2 state
			  11=D3 state

F2_PMI_PME_EN (R)	8	0x0	PME not supported
F2_PMI_DATA_SELECT (R)	12:9	0x0	Data select not implemented
F2_PMI_DATA_SCALE (R)	14:13	0x0	Data scale not implemented
F2_PMI_PME_STATUS (R)	15	0x0	PME not supported

F2_PMI_DATA - R - 8 bits - [gcconfig:0x257] [MMReg:0x5257]			
Field Name	**Bits**	**Default**	**Description**
F2_PMI_DATA	7:0	0x0	Not implemented

F2_MSI_CAP_ID - R - 8 bits - [gcconfig:0x260] [MMReg:0x5260]			
Field Name	**Bits**	**Default**	**Description**
F2_MSI_CAP_ID	7:0	0x5	MSI Capability ID

F2_MSI_NXT_CAP_PTR - R - 8 bits - [gcconfig:0x261] [MMReg:0x5261]			
Field Name	**Bits**	**Default**	**Description**
F2_MSI_NXT_CAP_PTR	7:0	0x0	The last item in capabilities list.

F2_MSI_MSG_CNTL - RW - 16 bits - [gcconfig:0x262] [MMReg:0x5262]:R			
Field Name	**Bits**	**Default**	**Description**
F2_MSI_EN	0	0x0	1=Enable MSI messaging
F2_MSI_MULTMSG_CAP (R)	3:1	0x0	The number of requested messages.
F2_MSI_MULTMSG_EN	6:4	0x0	000=1 message allocated 001=2 messages allocated 010=4 messages allocated 011=8 messages allocated 100=16 messages allocated 101=32 messages allocated =n110=reserved 111=Reserved
F2_MSI_64BIT (R)	7	0x1	64 messaging enabled

F2_MSI_MSG_ADDR_LO - RW - 32 bits - [gcconfig:0x264] [MMReg:0x5264]:R			
Field Name	**Bits**	**Default**	**Description**
F2_MSI_MSG_ADDR_LO	31:2	0x0	System-specified message lower address.

F2_MSI_MSG_ADDR_HI - RW - 32 bits - [gcconfig:0x268] [MMReg:0x5268]:R			
Field Name	**Bits**	**Default**	**Description**
F2_MSI_MSG_ADDR_HI	31:0	0x0	System-specified message upper address.

F2_MSI_MSG_DATA - RW - 16 bits - [gcconfig:0x26C] [MMReg:0x526C]:R			
Field Name	**Bits**	**Default**	**Description**
F2_MSI_DATA	15:0	0x0	System-specified message.

2.4 Bus Interface Control/Status Registers

MM_INDEX - RW - 32 bits - [IOReg,MMReg:0x0]			
Field Name	**Bits**	**Default**	**Description**
MM_ADDR	30:0	0x0	Index address to Frame buffer or MM register. Note: Bits [1:0] of this field are hardwired to 0.
MM_APER	31	0x0	0=Register Aperture 1=Linear Aperture

MM_DATA - RW - 32 bits - [IOReg,MMReg:0x4]			
Field Name	**Bits**	**Default**	**Description**
MM_DATA	31:0	0x0	Index Data field

GENENB - R - 8 bits - VGA_IO:0x3C3			
Field Name	**Bits**	**Default**	**Description**
BLK_IO_BASE	7:0	0x0	Mirror of F0 IO_BASE.

GENMO_WT - W - 8 bits - [MMReg,VGA_IO:0x3C2]			
Field Name	**Bits**	**Default**	**Description**
GENMO_MONO_ADDRESS_B	0	0x0	VGA addressing mode. 0=Monochrome emulation, regs at 0x3Bx 1=Color/Graphic emulation, regs at 0x3Dx
VGA_RAM_EN	1	0x0	Enables/disables CPU access to video RAM at VGA aperture. 0=Disable 1=Enable
VGA_CKSEL	3:2	0x0	Selects pixel clock frequency to use in VGA modes. Used when CRTC_GEN_CNTL.CRTC_EXT_DISP_EN=0. See CLOCK_CNTL_INDEX.PPLL_DIV_SEL for non-VGA mode pixel clock selection. 0=25.1744MHz (640 Pels) 1=28.3212MHz (720 Pels) 2=Reserved 3=Reserved
ODD_EVEN_MD_PGSEL	5	0x0	This bit is used in odd/even display modes (A/N modes: 0, 1, 2, 3, and 7). This bit is ignored when either bit GRA06[1] or SEQ4[3] are enabled. It is used to determine if the VGA aperture maps into the lower (even) or upper (odd) page of memory. 0=Selects odd (high) memory locations 1=Selects even (low) memory locations

	Bits	Default	

VGA_HSYNC_POL	6	0x0	Determines the polarity of horizontal sync (HSYNC) for VGA modes.
			   0=HSYNC pulse active high
			   1=HSYNC pulse active low
			The convention of VGA is to use active low VSYNC for 400 (and 200) and 480 line modes. Active high is normally used for 350 line modes.

VGA_VSYNC_POL	7	0x0	Determines the polarity of vertical sync (VSYNC) for VGA modes.
			   0=VSYNC pulse active high
			   1=VSYNC pulse active low
			The convention of VGA is to use active high VSYNC for 400 (and 200) line modes. Active low is normally used for 350 and 480 line modes.

Miscellaneous Output Register (Write)			

GENMO_RD - R - 8 bits - [MMReg,VGA_IO:0x3CC]			
Field Name	**Bits**	**Default**	**Description**
GENMO_MONO_ADDRESS_B *(mirror of GENMO_WT:GENMO_MONO_ADDRESS_B)*	0	0x0	VGA addressing mode.
VGA_RAM_EN *(mirror of GENMO_WT:VGA_RAM_EN)*	1	0x0	Enables/disables CPU access to video RAM at VGA aperture.
VGA_CKSEL *(mirror of GENMO_WT:VGA_CKSEL)*	3:2	0x0	Selects pixel clock frequency to use.
ODD_EVEN_MD_PGSEL *(mirror of GENMO_WT:ODD_EVEN_MD_PGSEL)*	5	0x0	This bit is used in odd/even display modes (A/N modes: 0, 1, 2, 3, and 7). This bit is ignored when either bit GRA06[1] or SEQ4[3] are enabled. It is used to determine if the VGA aperture maps into the lower (even) or upper (odd) page of memory.

VGA_HSYNC_POL
 	
(mirror of GENMO_WT:VGA_HSYNC_POL)
	6	0x0	Determines the polarity of horizontal sync (HSYNC) for VGA modes.
			   0=HSYNC pulse active high
			   1=HSYNC pulse active low
			The convention of VGA is to use active low VSYNC for 400 (and 200) and 480 line modes. Active high is normally used for 350 line modes.

VGA_VSYNC_POL
 	
(mirror of GENMO_WT:VGA_VSYNC_POL)
	7	0x0	Determines the polarity of vertical sync (VSYNC) for VGA modes.
			   0=VSYNC pulse active high
			   1=VSYNC pulse active low
			The convention of VGA is to use active high VSYNC for 400 (and 200) line modes. Active low is normally used for 350 and 480 line modes.

Miscellaneous Output Register (Read)			

2.5   Power Management Registers

PMI_CAP_ID - R - 8 bits - [gcconfig:0x50] [MMReg:0x5050]			
Field Name	**Bits**	**Default**	**Description**
PMI_CAP_ID	7:0	0x1	FIX=0x1 per spec.

PMI_NXT_CAP_PTR - R - 8 bits - [gcconfig:0x51] [MMReg:0x5051]			
Field Name	**Bits**	**Default**	**Description**
PMI_NXT_CAP_PTR	7:0	0x80	Next item is MSI.

PMI_PMC_REG - R - 16 bits - [gcconfig:0x52] [MMReg:0x5052]			
Field Name	**Bits**	**Default**	**Description**
PMI_VERSION	2:0	0x2	Revision 1.1 supported.
PMI_PME_CLOCK	3	0x0	PME clock not required.
PMI_DEV_SPECIFIC_INIT	5	0x0	No special initialization required.
PMI_D1_SUPPORT	9	0x1	D1 state supported.
PMI_D2_SUPPORT	10	0x1	D2 state supported.
PMI_PME_SUPPORT	15:11	0x0	No PME support.

PMI_DATA - R - 8 bits - [gcconfig:0x57] [MMReg:0x5057]			
Field Name	**Bits**	**Default**	**Description**
PMI_DATA	7:0	0x0	Not implemented.

2.6   System Clock Configuration Space Registers

OSC_CONTROL - RW - 32 bits - clkconfig:0x40			
Field Name	**Bits**	**Default**	**Description**

OSC_EN	0	0x1	Scratch: This register bit can be written to, and read from, but it does not control anything.
			  0=Disable
			  1=Enable

XTAL_LOW_GAIN	1	0x0	Scratch: This register bit can be written to, and read from, but it does not control anything.
			  0=High Gain
			  1=Low Gain

Reserved0 (R)	3	0x0	Scratch: This register bit can be written to, and read from, but it does not control anything.

CPU_STOP_ENABLE	4	0x0	Scratch: This register bit can be written to, and read from, but it does not control anything.
			  0=Disable
			  1=Enable

DC_STOP_ENABLE	5	0x0	Scratch: This register bit can be written to, and read from, but it does not control anything.
			  0=Disable
			  1=Enable

GFX_REFCLK_OE_TOGGLE	6	0x0	Scratch: This register bit can be written to, and read from, but it does not control anything.
GPP_REFCLK_OE_TOGGLE	7	0x0	Scratch: This register bit can be written to, and read from, but it does not control anything.
SB_REFCLK_OE_TOGGLE	8	0x0	Scratch: This register bit can be written to, and read from, but it does not control anything.
Reserved1 (R)	11	0x0	Scratch: This register bit can be written to, and read from, but it does not control anything.
CPUCLK_SE_OE_TOGGLE	12	0x0	Scratch: This register bit can be written to, and read from, but it does not control anything.
CPUCLK_DIFF_OE_TOGGLE	13	0x0	Scratch: This register bit can be written to, and read from, but it does not control anything.
REF_14M_OE_TOGGLE	14	0x0	Scratch: This register bit can be written to, and read from, but it does not control anything.

ON_CHIP_CLOCK_GENERATOR (R)	18	0x0	Scratch: This register bit can be written to, and read from, but it does not control anything.
			  0=External clock
			  1=Internal clock

SYSCLK_OE_TOGGLE	19	0x0	Scratch: This register bit can be written to, and read from, but it does not control anything.
MEMCLK_OE_TOGGLE	20	0x0	Scratch: This register bit can be written to, and read from, but it does not control anything.
Scratch register			

GC_CLK_CNTRL - RW - 8 bits - clkconfig:0x74			
Field Name	**Bits**	**Default**	**Description**
CG_BCLKSTATE	0	0x0	Program the IG register bit as follows: (1) Set to 0 to force BCLK on within M10.CG block (2) Set to 1 to allow CG to stop clks for power management sleep sequencing. 0=Run 1=Allow GC Shutdown Sequence
GC_STATE (R)	4:3	0x0	To restart the GC program the following: (1) Clear CG_BCLKSTATE to force the internal BCLK (in GC) to run. (2) Write BIF:PM_STATUS[PMI_POWER_STATE] to 2'b00 to start WAKEUP sequence. (3) Wait until GC_STATE reports a value of 2'b00. (4) Wait 100 us before sending more GC requests to GC. (5) Set bit CG_BCLKSTATE to allow state transition. 0=GC has transitioned to D0 1= 2= 3=GC has transitioned to suspend and 61us later all BCLK in the GC will stop
STOP_GC_REQ (R)	5	0x0	In order to suspend the GC perform the following: (1) Set bit CG_CLKSTATE to allow state transition stopping BCLK when SUSPEND is reached. (2) Set BIF:PM_STATUS[PMI_POWER_STATE] to 0x02 to start SUSPEND sequence (into D2). (3) Wait until the state transition is complete, either by reading BIF:PM_STATUS[PMI_POWER_STATE] and verifying that it changed to 2'b10, or by checking GC_STATE for a value of 2'b11. This indicates that the GC has transitioned to suspend and 61 us later all BCLK in GC will stop. (4) This can be verified by reading STOP_GC_REQ - this bit will be set 61us before GC stops its clocks. When clocks are stopped, oCG_CT_BCLK_STOPPED=1. 0=GC has not stopped its clocks 1=GCs clocks will stop within 61us
Graphics Controller Clock Control			

SCRATCH_1_CLKCFG - RW - 32 bits - clkconfig:0x78			
Field Name	**Bits**	**Default**	**Description**
SCRATCH_1	31:0	0x0	

SCRATCH_2_CLKCFG - RW - 32 bits - clkconfig:0x7C			
Field Name	**Bits**	**Default**	**Description**
SCRATCH_2	31:0	0x0	

SCRATCH_CLKCFG - RW - 32 bits - clkconfig:0x84			
Field Name	**Bits**	**Default**	**Description**
SCRATCH	31:0	0x0	All of the bits in this register can be both written to, and read from, but the register does not control anything.
Scratch register for the CLKCFG register space.			

CLKGATE_DISABLE2 - RW - 32 bits - clkconfig:0x8C			
Field Name	**Bits**	**Default**	**Description**
CLKGATE_DIS_MCB	0	0x1	Disables clock gating for MCLK1X going to arbiterB and rbs
CLKGATE_DIS_MCGR	1	0x1	Disables clock gating for MCLK1X going to cic interface
CLKGATE_DIS_MCSQA	2	0x1	Disables clock gating for MCLK1X going to sequencerA
CLKGATE_DIS_MCSQB	3	0x1	Disables clock gating for MCLK1X going to sequencerB
CLKGATE_DIS_MCIOA	4	0x1	Disables clock gating for MCLK1X going to ioA
CLKGATE_DIS_MCIOB	5	0x1	Disables clock gating for MCLK1X going to ioB
CLKGATE_DIS_BIU_NB1ACLK	8	0x1	Scratch: This register bit can be written to, and read from, but it does not control anything.
CLKGATE_DIS_BIU_NB1BCLK	9	0x1	Scratch: This register bit can be written to, and read from, but it does not control anything.
CLKDATE_DIS_BIU_MEMA	10	0x1	Scratch: This register bit can be written to, and read from, but it does not control anything.
CLKDATE_DIS_BIU_MEMB	11	0x1	Scratch: This register bit can be written to, and read from, but it does not control anything.
CLKGATE_DIS_BIU_PAD	12	0x1	Scratch: This register bit can be written to, and read from, but it does not control anything.
CLKGATE_DIS_IOC_CCLK_MST	13	0x1	Scratch: This register bit can be written to, and read from, but it does not control anything.
CLKGATE_DIS_IOC_CCLK_SLV	14	0x1	Scratch: This register bit can be written to, and read from, but it does not control anything.
CLKGATE_DIS_BIU_IOPLL4X	18	0x1	Disables clock gating for SCLK4X going to IOPADS
GFX_SCLK_DISABLE	20	0x0	Disables GFX engine clock
GFX_DISPCLK_DISABLE	21	0x0	Disables GFX display clock
CFG_CT_DISABLE_MCCLK1X_SVL	22	0x1	
CFG_CT_DISABLE_MCCLK1X_M2C	23	0x1	
iCFG_CT_DISABLE_CCLK_BIF	24	0x1	Disables clock gating for CCLK going to BIF branch
CFG_CT_DISABLE_MCLK_BIF	25	0x1	Disables clock gating for MCLK going to BIF branch
MC_DELAY_TIMER_EXTEND	30	0x0	Extend delay timer for MEMORY clocks 0=16 clocks 1=32 clocks
Register Description.			

CLKGATE_DISABLE - RW - 32 bits - clkconfig:0x94			
Field Name	**Bits**	**Default**	**Description**
CLKGATE_DIS_MCA	0	0x1	Disables clock gating for MCLK1X going to arbiterA and rbs 0=Enable 1=Disable
CPUCLK_STOP_MISC	1	0x1	Disables CPUCLK_STOP stopping CFG and IG2R6 BCLK and CCLK 0=Enable 1=Disable
CLKGATE_DIS_MC1	2	0x1	This register bit is not used. 0=Enable 1=Disable

CLKGATE_DIS_MC2	3	0x1	Disables clock gating for MCLK1X to NB
			  0=Enable
			  1=Disable

DIS_CPUCLK_STOP_BIU	4	0x1	Disables CPUCLK_STOP stopping BIU clocks
			  0=Enable
			  1=Disable

SPARE_7	7	0x0	0=Enable 1=Disable

ENABLE_ANALOG_DLLs	8	0x1	Scratch: This register bit can be written to, and read from, but it does not control anything.
			  0=Disable
			  1=Enable

CLKGATE_DIS_RAMCLK	9	0x1	This register bit is not used.
			  0=Enable
			  1=Disable

CLKGATE_DIS_BIU_MEM	10	0x1	Scratch: This register bit can be written to, and read from, but it does not control anything.
			  0=Enable
			  1=Disable

CLKGATE_DIS_BIU_NB1CLK	11	0x1	Scratch: This register bit can be written to, and read from, but it does not control anything.
			  0=Enable
			  1=Disable

CLKGATE_DIS_BIU_NB2CLK	12	0x1	Scratch: This register bit can be written to, and read from, but it does not control anything.
			  0=Enable
			  1=Disable

CLKGATE_DIS_PCIE_GPCLK	13	0x1	Scratch: This register bit can be written to, and read from, but it does not control anything.
			  0=Enable
			  1=Disable

CLKGATE_DIS_PCIE_GCLK	14	0x1	Scratch: This register bit can be written to, and read from, but it does not control anything.
			  0=Enable
			  1=Disable

CLKGATE_DIS_PCIE_SBCLK	15	0x1	Scratch: This register bit can be written to, and read from, but it does not control anything.
			  0=Enable
			  1=Disable

CLKGATE_DIS_GFX_TXCLK	16	0x1	Scratch: This register bit can be written to, and read from, but it does not control anything.
			  0=Enable
			  1=Disable

CLKGATE_DIS_GPP_TXCLK	17	0x1	Scratch: This register bit can be written to, and read from, but it does not control anything.
			  0=Enable
			  1=Disable

CLKGATE_DIS_SB_TXCLK	18	0x1	Scratch: This register bit can be written to, and read from, but it does not control anything.
			  0=Enable
			  1=Disable

CLKGATE_DIS_GFX_TXCLK_L0S	19	0x1	Scratch: This register bit can be written to, and read from, but it does not control anything.
			  0=Enable
			  1=Disable

CLKGATE_DIS_SB_TXCLK_L0S	20	0x1	Scratch: This register bit can be written to, and read from, but it does not control anything.
			  0=Enable
			  1=Disable

CLKGATE_DIS_GPP_TXCLK_L0S	21	0x1	Scratch: This register bit can be written to, and read from, but it does not control anything. 0=Enable 1=Disable
CLKGATE_DIS_GFX_CCLK	22	0x1	Disables clock gating for PCIE graphics CCLK 0=Enable 1=Disable
CLKGATE_DIS_GFX_MCLK	23	0x1	Disables clock gating for PCIE graphics MCLK 0=Enable 1=Disable
CLKGATE_DIS_GPPSB_CCLK	24	0x1	Disables clock gating for PCIE General Purpose and southbridge CCLK 0=Enable 1=Disable
CLKGATE_DIS_GPPSB_MCLK	25	0x1	Disables clock gating for PCIE General Purpose and southbridge MCLK 0=Enable 1=Disable
CLKGATE_DIS_CFG_S1X	28	0x1	Disables clock gating for SCLK1X going to cfg 0=Enable 1=Disable
CLKGATE_DIS_CFG_B1X	29	0x1	0=Enable 1=Disable
DEEP_S1_DISABLE	30	0x1	If enabled, S1 mode (CPU_STOP active) will power down SPLL, BPLL, and MPLL; otherwise, S1 mode will gate clocks only. 0=Enable 1=Disable
Register Description.			

CLK_TOP_PERF_CNTL - RW - 32 bits - clkconfig:0xAC			
Field Name	**Bits**	**Default**	**Description**
CLK_TOP_EVENT_SEL_0	7:0	0x0	Performance counter 0 event select 0 = Counter disable 1 = MCLK cycles 2 = MC graphics MCLK idle 3 = 4 = MC arbiter A MCLK idle 5 = MC arbiter B MCLK idle 6 = MC sequencer A MCLK idle 7 = MC sequencer B MCLK idle 8 = MC northbridge MCLK idle 9 = MC arbiter A MCLK stop a = MC arbiter B MCLK stop b = MC controller MCLK stop c = MC northbridge MCLK stop d = BIU MCLK stop e = MC graphics MCLK stop f = MC sequencer A MCLK stop 10 = MC sequencer B MCLK stop 11 = MC IO A MCLK stop 12 = MC IO B MCLK stop 13 = 14 = 15 = BIU MCLK stop 16 = BIU MCLK A stop 17 = BIU MCLK B stop 18 = Core voltage at low state 19 = BIU to MC channel A RTS 1a = BIU to MC channel B RTS 1b = MC to BIU channel A RTR 1c = MC to BIU channel B RTR 1d = (BIU to MC channel A RTS) & (MC to BIU channel A RTR) 1e = (BIU to MC channel B RTS) & (MC to BIU channel B RTR) 1f = (MC arbiter A MCLK idle) & (MC sequencer A MCLK idle) 20 = (MC arbiter B MCLK idle) & (MC sequencer B MCLK idle) 21 = (MC graphics MCLK idle) & (MC northbridge MCLK idle) 22 = (MC sequencer A MCLK idle) & (MC sequencer B MCLK idle) 23 = IOC MCLK stop 24 = PCIE GFX MCLK stop 25 = PCIE GPPSB MCLK stop 26-3f = Reserved 40 = Counter disable 41 = CCLK cycles 42 = BIU CCLK idle 43 = BIU CCLK busy 44 = CPU STOP assertion 45 = BIU S2K CCLK stop 46 = BIU NB1 A CCLK stop 47 = BIU NB1 B CCLK stop 48 = IOPAD CCLK stop 49 = IOSPLL CCLK4X stop 4a = BIU PII CCLK stop 4b = EXTCPU CCLK stop 4c = 4d = 4e = IG2R6 CCLK stop 4f = CFG CCLK stop 50 = 51 = 52 = 53 = 54 = (BIU CCLK idle) & not(BIU CCLK BUSY) 55 = (BIU NB1 A CCLK stop) & (BIU NB1 B CCLK stop) 56 = (BIU S2K CCLk stop) & (BIU PII CCLK stop) 57-7f = Reserved 80 = counter disable 81 = BCLK cycles 82 = 83 = 84 = 85 = 86 = 87 = 88 = 89 = 8a = 8b = 8c = 8d = 8e = 8f = IG2R6 BCLK stop 90 = 91 = 92 = 93 = 94 = 95-ff = Reserved

CLK_TOP_EVENT_SEL_1	15:8	0x0	Performance counter 1 event select. Note: It has the same definition as above.
CLK_TOP_UPPER_COUNT_0 (R)	23:16	0x0	Performance counter 0 upper bits readback.
CLK_TOP_UPPER_COUNT_1 (R)	31:24	0x0	Performance counter 1 upper bits readback.
Performance counter event select.			

CLK_CFG_HTPLL_CNTL - RW - 32 bits - clkconfig:0xD4			
Field Name	**Bits**	**Default**	**Description**
CLK_CFG_HTPLL_IPCP	2:0	0x4	
CLK_CFG_HTPLL_IDB1CLK0SC	5:3	0x5	
CLK_CFG_HTPLL_IDB1CLK3SC	8:6	0x5	
CLK_CFG_HTPLL_IDB4CLKSC	11:9	0x5	
CLK_CFG_HTPLL_ITXCLKSC	14:12	0x7	
CLK_CFG_HTPLL_IVCO_MODE	16:15	0x0	
CLK_CFG_HTPLL_IPLL_CTL	21:17	0x0	
CLK_CFG_HTPLL_ITMONEN	22	0x0	
CLK_CFG_HTPLL_PWDN	23	0x0	
iCFG_HT_HTPLL_ITXCLKINV	24	0x0	
iCFG_HT_HTPLL_ICLK0SEL	25	0x0	
iCFG_HT_HTPLL_ICLK3SEL	26	0x0	
iCFG_HT_HTPLL_IVCOREF	28:27	0x0	
iCFG_HT_HTPLL_ICALREF	30:29	0x0	
iCFG_HT_HTPLL_ITSTCLK	31	0x0	

CLK_TOP_SPARE_A - RW - 32 bits - clkconfig:0xE0			
Field Name	**Bits**	**Default**	**Description**
MCLK_SWITCH_GFX_EN	0	0x0	
spare_7_1	7:1	0x0	Bit [1]=REG_ENABLE_ASYNC_OPT Bit [2]=Switch MC GUI & HOST IDLES to 1
CFG_B1X_CPUSTOP_DIS	8	0x0	Scratch: This register bit can be written to, and read from, but it does not control anything.
CFG_S1X_CPUSTOP_DIS	9	0x0	Scratch: This register bit can be written to, and read from, but it does not control anything.
spare_15_10	15:10	0x0	
OSC_PU	16	0x1	Scratch: This register bit can be written to, and read from, but it does not control anything.
OSC_PD	17	0x0	Scratch: This register bit can be written to, and read from, but it does not control anything.
OSC_SRP	18	0x1	Scratch: This register bit can be written to, and read from, but it does not control anything.
OSC_SRN	19	0x1	Scratch: This register bit can be written to, and read from, but it does not control anything.
OSC_SP	23:20	0x4	Scratch: This register bit can be written to, and read from, but it does not control anything.
OSC_SN	27:24	0x7	Scratch: This register bit can be written to, and read from, but it does not control anything.
spare_31_28	31:28	0x0	
Misc. register for clk_top.			

CLK_TOP_SPARE_B - RW - 32 bits - clkconfig:0xE4			
Field Name	**Bits**	**Default**	**Description**
CLK_TOP_SPARE_B_0	0	0x0	Stops permanent MCLK branch
CLKGATE_DIS_MCSQA_DEBUG	1	0x0	Disables extra gating condition for MCLK1X going to MC Sequencer A
CLKGATE_DIS_MCSQB_DEBUG	2	0x0	Disables extra gating condition for MCLK1X going to MC Sequencer B
OSCOUT_OE	3	0x0	Scratch: This register bit can be written to, and read from, but it does not control anything.
TESTCLK_MODO	4	0x0	Scratch: This register bit can be written to, and read from, but it does not control anything.
TESTCLK_OE	5	0x0	Scratch: This register bit can be written to, and read from, but it does not control anything.

CLK_TOP_SPARE_B	31:6	0x0	Bit [14]: Vertical blanking switch select for mclk switching
			    0=Prim display
			    1=Sec display
			Bit [15]: Enable mclk switching synced with vertical blank from display
			Bits [31:16]: To be defined

Misc. register for clk_top.			

CLK_TOP_SPARE_C - RW - 32 bits - clkconfig:0xE8			
Field Name	**Bits**	**Default**	**Description**
EXTEND_IOC_PM_TIMER	0	0x0	
SPARE_1	1	0x0	
HTPLL_IBIAS_AND_IOVERCLOCK	8:2	0x0	
SPARE_11to9	11:9	0x0	
CT_DISABLE_CLKGATE_HTIU_LCLK_RX	12	0x0	
CT_DISABLE_DYNAMIC_CLKGATE_HTIU_LCLK_RX	13	0x0	
DISABLE_TXPHY_LCLK_GATING	14	0x0	
SPARE_15	15	0x0	
HTPLL_IPCP_BIT3	16	0x0	
SPARE_31to17	31:17	0x0	
Misc. register for clk_top.			

CLK_TOP_SPARE_D - RW - 32 bits - clkconfig:0xEC			
Field Name	**Bits**	**Default**	**Description**
OSCOUT_OUT (R)	0	0x0	OSCOUT pad readback.
CLK_TOP_SPARE_D (R)	31:1	0x0	To be defined.
Misc. status register for clk_top.			

CFG_CT_CLKGATE_HTIU - RW - 32 bits - clkconfig:0xF8			
Field Name	**Bits**	**Default**	**Description**
DISABLE_CLKGATE_HTIU_LCLK_HTM	0	0x1	
DISABLE_DYNAMIC_CLKGATE_HTIU_LCLK_HTM	1	0x1	
DISABLE_CLKGATE_HTIU_LCLK_RP	2	0x1	
DISABLE_DYNAMIC_CLKGATE_HTIU_LCLK_RP	3	0x1	
DISABLE_CLKGATE_HTIU_LCLK_FCB	4	0x1	
DISABLE_DYNAMIC_CLKGATE_HTIU_LCLK_FCB	5	0x1	
DISABLE_CLKGATE_HTIU_LCLK_GCM	6	0x1	
DISABLE_DYNAMIC_CLKGATE_HTIU_LCLK_GCM	7	0x1	
DISABLE_CLKGATE_HTIU_LCLK_NB1	8	0x1	
DISABLE_DYNAMIC_CLKGATE_HTIU_LCLK_NB1	9	0x1	
DISABLE_CLKGATE_HTIU_LCLK_NB2	10	0x1	
DISABLE_DYNAMIC_CLKGATE_HTIU_LCLK_NB2	11	0x1	
ILF_MODE	13:12	0x0	

CPLL_CONTROL - RW - 32 bits - clkconfig:0x44			
Field Name	**Bits**	**Default**	**Description**
CPLL_REFSEL	0	0x0	CPU PLL reference clock select Default is 100MHz PCIE reference clock
CPLL_REF_DELAY	1	0x0	not used
CPLL_VCO_DELAY	2	0x0	not used
CPLL_SKEW4X	5:3	0x0	4X output clock skew control
CPLL_SKEW2X	8:6	0x0	2X output clock skew control
CPLL_SKEW1X_CORE	11:9	0x0	not used
CPLL_CTL	16:12	0x0	IPLL_CTL[4] enables calibration override. When IPLL_CTL[4]=0, the four calibration bits are set by the calibration loop. When IPLL_CTL[4]=1, the four bits are set through IPLL_CTL[3:0].
CDLL_FREQ_SEL	20:17	0x0	Not used
CPLL_LF_MODE	24:21	0x0	Loop filter mode setting
RESERVED	27:25	0x0	
CPLL_MODE (R)	31:28	0x0	VCO operating mode flags

CLK_TOP_PWM4_CTRL - RW - 32 bits - clkconfig:0x4C			
Field Name	**Bits**	**Default**	**Description**
CT_PWM4_NumberOfCyclesInPeriod	11:0	0x0	
CT_PWM4_NumberOfHighCyclesInPeriod	23:12	0x0	
CT_PWM4_en	24	0x0	
CT_PWM4_io_oe	25	0x0	

CLK_TOP_PWM5_CTRL - RW - 32 bits - clkconfig:0x50			
Field Name	**Bits**	**Default**	**Description**
CT_PWM5_NumberOfCyclesInPeriod	11:0	0x0	
CT_PWM5_NumberOfHighCyclesInPeriod	23:12	0x0	
CT_PWM5_en	24	0x0	
CT_PWM5_io_oe	25	0x0	

DELAY_SET_IOC_CCLK - RW - 32 bits - clkconfig:0x5C			
Field Name	**Bits**	**Default**	**Description**
DELAY_SET_ioc_cclk_mst	4:0	0x2	
DELAY_SET_ioc_cclk_slv	9:5	0x2	
Delay register			

CT_DISABLE_BIU - RW - 32 bits - clkconfig:0x68			
Field Name	**Bits**	**Default**	**Description**
BIU_NB1_CPUSTOP_DIS	0	0x1	
BIU_NB2_CPUSTOP_DIS	1	0x1	
BIU_CCLK_C3	2	0x1	
BIU_MCLK_C3	3	0x1	
BIU_CCLK_IO_PAD	4	0x1	
SYNC_DBL_FLP_EN	5	0x0	
DELAY_SET_gpp_cclk	10:6	0x2	
DELAY_SET_gpp_mclk	15:11	0x2	
iCFG_CT_DISABLE_BIU_IO_CCLK4X_P	16	0x1	
iCFG_CT_DISABLE_BIU_IO_CCLK4X_N	17	0x1	
Disable BIU Control			

CPLL_CONTROL3 - RW - 32 bits - clkconfig:0x70			
Field Name	**Bits**	**Default**	**Description**
DLL_BIAS	2:0	0x1	Bias current trim. IBIAS[1:0].
			00=-9%
			01=0%
			10=+12%
			11=+25%
			Default=01
DLL_CPP	4:3	0x0	Control charge pump source current, 0 off, 1 on
DLL_CPN	6:5	0x0	Control charge pump sink current, 0 off, 1 on
VCOREF	8:7	0x0	VCO input reference voltage setting. Controlled dynamically during calibration.
CALREF	10:9	0x0	2nd VCO input reference voltage setting. Controlled dynamically during calibration.
SKEW_REF	12:11	0x0	1X reference clock (O1XT) skew control
SKEW_FB	14:13	0x0	1X feedback clock (O1XT) skew control
REF_DELAY	19:15	0x0	Reference frequency delay setting
FB_DELAY	24:20	0x0	Feedback clock delay setting
RESERVED	31:25	0x1	Bit [0] Select calibration or manual setting for charge pump current mirror.
			0=Select manual setting
			1=Select calibration setting
CPP control3			

CPLL_CONTROL2 - RW - 32 bits - clkconfig:0x98			
Field Name	**Bits**	**Default**	**Description**
CPLL_SKEW1XA	2:0	0x0	1XA output clock (O1XA) skew control
CPLL_SKEW1XB	5:3	0x0	1XB output clock (O1XB) skew control
CPLL_IOBUFSEL	6	0x1	Not used
CPLL_SPARE	11:7	0x0	Not used
CPLL_FLOAT	16:12	0x0	Not used
RESERVED	20:17	0x0	Reserved
CPLL_CP_RB (R)	24:21	0x0	Charge-pump current setting read back
CPLL_VCO_MODE_RB (R)	26:25	0x0	VCO mode setting read back
CPLL_FWDIV_RB (R)	28:27	0x0	Divide by 1/2/3/4 forward divider ratio read back.
			00=Divide by 1
			01=Divide by 2
			10=Divide by 3
			11=Divide by 4
STRAP_FREQ_SPEED (R)	31:29	0x0	Frequency detector read back.
			000=100MHz
			001=133MHz
			010=166MHz
			011=200MHz
			100=266MHz
			101=333MHz
CPPL control2			

clk_top_pwm1_ctrl - RW - 32 bits - clkconfig:0xB0			
Field Name	**Bits**	**Default**	**Description**
ct_pwm1_NumberOfCyclesInPeriod	11:0	0x0	
ct_pwm1_NumberOfHighCyclesInPeriod	23:12	0x0	
ct_pwm1_en	24	0x0	
ct_pwm1_io_oe	25	0x0	
clk_top_pwm1_ctrl			

clk_top_pwm2_ctrl - RW - 32 bits - clkconfig:0xB4			
Field Name	**Bits**	**Default**	**Description**
ct_pwm2_NumberOfCyclesInPeriod	11:0	0x0	
ct_pwm2_NumberOfHighCyclesInPeriod	23:12	0x0	
ct_pwm2_en	24	0x0	
ct_pwm2_io_oe	25	0x0	
clk_top_pwm2_ctrl			

clk_top_test_ctrl - RW - 32 bits - clkconfig:0xB8			
Field Name	**Bits**	**Default**	**Description**
ct_test_clk_sel	5:0	0x0	
ct_test_clk_en	6	0x0	
ct_test_clk_oe	7	0x0	
ct_test_clk_spare	31:16	0x0	
clk_top_test_ctrl			

CLK_TOP_THERMAL_ALERT_INTR_EN - RW - 32 bits - clkconfig:0xC0			
Field Name	**Bits**	**Default**	**Description**
THERMAL_ALERT_INTR_EN	0	0x0	
spare_1_31	31:1	0x0	
This register is for THERMAL_ALERT_INTR_EN			

CLK_TOP_THERMAL_ALERT_STATUS - RW - 32 bits - clkconfig:0xC4			
Field Name	**Bits**	**Default**	**Description**
THERMAL_ALERT_STATUS	0	0x0	
spare_1_31	31:1	0x0	
This regsister is for THERMAL_ALERT_STATUS			

CLK_TOP_THERMAL_ALERT_WAIT_WINDOW - RW - 32 bits - clkconfig:0xC8			
Field Name	**Bits**	**Default**	**Description**
THERMAL_ALERT_WAIT_WINDOW	29:0	0x0	
spare_30_31	31:30	0x0	
This register is for THERMAL_ALERT_WAIT_WINDOW			

clk_top_pwm3_ctrl - RW - 32 bits - clkconfig:0xCC			
Field Name	**Bits**	**Default**	**Description**
ct_pwm3_en	0	0x0	
ct_pwm3_NumberOfCyclesInPeriod	12:1	0x0	
ct_pwm3_NumberOfHighCyclesInPeriod	24:13	0x0	
ct_pwm3_io_oe	25	0x0	
This register is for pwm3_ctrl			

clk_top_spare_pll - RW - 32 bits - clkconfig:0xD0			
Field Name	**Bits**	**Default**	**Description**
ct_spare_pll_ctl	31:0	0x0	
This register is spare			

2.7 APC Configuration Space Registers

PCI Bus 0 - Device 1 Registers

APC_VENDOR_ID - R - 16 bits - apcconfig:0x0			
Field Name	Bits	Default	Description
VENDOR_ID	15:0	0x1002	Vendor ID. This 16-bit field identifies the manufacturer of the device: Advanced Micro Devices, Inc.

APC_DEVICE_ID - R - 16 bits - apcconfig:0x2			
Field Name	Bits	Default	Description
DEVICE_ID	15:0	0x7912	Device Identifier This 16-bit field is assigned by the device manufacturer and identifies the type of device. The current northbridge Device ID assignment is 7912.

APC_COMMAND - RW - 16 bits - apcconfig:0x4			
Field Name	Bits	Default	Description

IO_ACCESS_EN	0	0x0	I/O Access Enable.
			This bit is always 0 because the RS690 does not respond to I/O cycles on the PCI Bus.
			  0=Disable
			  1=Enable

MEM_ACCESS_EN	1	0x0	Memory Access Enable.
			Controls whether PCI memory accesses to system memory are accepted.
			  0=Disable
			  1=Enable

BUS_MASTER_EN	2	0x0	Bus Master Enable.
			This bit is always set, indicating that the RS690 is allowed to act as a bus master on the PCI Bus.
			  0=Disable
			  1=Enable

SPECIAL_CYCLE_EN (R)	3	0x0	Special Cycle.
			This bit is always 0 because the RS690 ignores PCI special cycles.
			  0=Disable
			  1=Enable

MEM_WRITE_INVALIDATE_EN (R)	4	0x0	Memory Write and Invalidate Enable.
			This bit is always 0 because the RS690 does not generate memory write and invalidate commands.
			  0=Disable
			  1=Enable

PAL_SNOOP_EN (R)	5	0x0	VGA Palette Snoop Enable. This bit is always 0 indicating that the RS690 does not snoop the VGA palette address range. 0=Disable 1=Enable
PARITY_ERROR_EN (R)	6	0x0	Parity Error Response. This bit is always 0 because the RS690 does not report data parity errors. 0=Disable 1=Enable
Reserved0 (R)	7	0x0	0=Disable 1=Enable
SERR_EN	8	0x0	System Error Enable. Controls the assertion of SERR#. 0=Disable 1=Enable
FAST_B2B_EN (R)	9	0x0	Fast Back-to-Back to Different Devices Enable. This bit is always 0, because the RS690 does not allow the generation of fast back-to-back transactions to different agents. 0=Disable 1=Enable
Reserved (R)	15:10	0x0	This bit is reserved in PCI 2.3. It is hardwired to 0.
The AGP/PCI Command and Status register provides coarse control over the PCI-PCI bridge function within the RS690. This register controls the ability to generate and respond to PCI cycles on both the AGP bus and the PCI bus.			

APC_STATUS - RW - 16 bits - apcconfig:0x6			
Field Name	**Bits**	**Default**	**Description**
Reserved (R)	3:0	0x0	
CAP_LIST (R)	4	0x1	Capabilities List This bit is set to indicate that this device's configuration space supports a capabilities list.
PCI_66_EN (R)	5	0x1	66-MHz Capable Indicate that the RS690 supports 66 MHz PCI operation
UDF_EN (R)	6	0x0	User-Definable Features This bit is always 0 indicating that UDF is not supported by the RS690. 0=Disable 1=Enable
FAST_BACK_CAPABLE (R)	7	0x0	Fast Back-to-Back Capable This bit is always 0 indicating that the RS690 as a target is not capable of accepting fast back-to-back transactions when the transactions are not to the same agent.
DEVSEL_TIMING (R)	10:9	0x1	DEVSEL# Timing This bit field defines the timing of DEVSEL# on the RS690. The device only supports medium DEVSEL# timing.
SIGNAL_TARGET_ABORT (R)	11	0x0	Signaled Target Abort This bit is always 0 because the RS690 does not terminate transactions with target aborts. 0=No Abort 1=Target Abort asserted

RECEIVED_TARGET_ABORT (R)	12	0x0	Received Target Abort
			This bit is set by whenever a CPU to PCI transaction (except for a special cycle) is terminated due to a target-abort. This bit is cleared by writing a 1.
			  0=Inactive
			  1=Active

RECEIVED_MASTER_ABORT (R)	13	0x0	Received Master Abort
			This bit is set whenever a CPU to PCI transaction (except for a special cycle) is terminated due to a master-abort. This bit is cleared by writing a 1.
			  0=Inactive
			  1=Active

SIGNALED_SYSTEM_ERROR	14	0x0	Signaled System Error
			This bit is set whenever the RS690 generates a System Error and asserts the SERR# line (currently only GART Error). This bit is cleared by writing a 1.
			  0=No Error
			  1=SERR asserted

PARITY_ERROR_DETECTED (R)	15	0x0	Detected Parity Error This bit is always 0 because the RS690 does not support data parity checking.
The AGP/PCI Command and Status register provides coarse control over the PCI-PCI bridge function within the RS690. This register controls the ability to generate and respond to PCI cycles on both the AGP bus and the PCI bus.			

APC_REVISION_ID - R - 8 bits - apcconfig:0x8			
Field Name	**Bits**	**Default**	**Description**
MINOR_REV_ID	3:0	0x0	Identifies the stepping number of the device.
MAJOR_REV_ID	7:4	0x0	Identifies the revision number of the device.
Revision Identification.			

APC_REGPROG_INF - R - 8 bits - apcconfig:0x9			
Field Name	**Bits**	**Default**	**Description**
REG_LEVEL_PROG_INF	7:0	0x0	Indicates a PCI/PCI bridge.
Program Interface.			

APC_SUB_CLASS - R - 8 bits - apcconfig:0xA			
Field Name	**Bits**	**Default**	**Description**
SUB_CLASS_INF	7:0	0x4	4=Indicates a PCI/PCI bridge
Sub-Class Code.			

APC_BASE_CODE - R - 8 bits - apcconfig:0xB			
Field Name	**Bits**	**Default**	**Description**
BASE_CLASS_CODE	7:0	0x6	Indicates a general bridge device.
Class Code.			

APC_CACHE_LINE - R - 8 bits - apcconfig:0xC			
Field Name	**Bits**	**Default**	**Description**
CACHE_LINE_SIZE	7:0	0x0	
Cache Line Size.			

APC_LATENCY - RW - 8 bits - apcconfig:0xD			
Field Name	**Bits**	**Default**	**Description**
LATENCY_TIMER	7:0	0x0	This bit field defines the minimum amount of time in PCI clock cycles that the bus master can retain ownership of the bus. This is mandatory for masters that are capable of performing a burst consisting of more than two data phases.
Latency Timer.			

APC_HEADER - R - 8 bits - apcconfig:0xE			
Field Name	**Bits**	**Default**	**Description**
HEADER_TYPE	7:0	0x1	Bits [6:5] are 0, indicating that Type 00 Configuration Space Header format is supported.
Header Type.			

APC_BIST - R - 8 bits - apcconfig:0xF			
Field Name	**Bits**	**Default**	**Description**
BIST_COMP	3:0	0x0	
BIST_STRT	6	0x0	
BIST_CAP	7	0x0	
Built-in-self-test.			

APC_SUB_BUS_NUMBER_LATENCY - RW - 32 bits - apcconfig:0x18			
Field Name	**Bits**	**Default**	**Description**
PRIMARY_BUS	7:0	0x0	Primary Bus Number: Records the number of the PCI bus that the primary interface of the bridge is connected to. The bridge uses this to decode type 1 configuration transactions on the secondary interface that should be converted to Special Cycle transactions on the primary interface.
SECONDARY_BUS	15:8	0x0	Secondary Bus Number: Records the number of the PCI bus that the secondary interface of the bridge is connected to. The bridge uses this to determine when to respond to type 1 configuration transactions on the primary interface and convert them to type 0 transactions on the secondary interface.
SUB_BUS_NUMBER	23:16	0x0	Sub-Bus Number: Records the number of the highest numbered PCI bus that is behind (or subordinate to) a bridge. The bridge uses this in conjunction with the Secondary Bus Number register to determine when to respond to type 1 configuration transactions on the primary interface and to pass them on to the secondary interface.
SECONDARY_LATENCY_TIMER	31:24	0x0	Secondary Latency Timer: Adheres to the definition of the Latency Timer in the PCI Local Bus Specification, but only applies to the secondary interface of a PCI to PCI bridge.
Sub bus number and secondary bus latency timer.			

APC_AGP_PCI_IOBASE_LIMIT - RW - 16 bits - apcconfig:0x1C			
Field Name	**Bits**	**Default**	**Description**
IO_BASE_R (R)	3:0	0x1	
IO_BASE	7:4	0x0	
IO_LIMIT_R (R)	11:8	0x1	
IO_LIMIT	15:12	0x0	

APC_AGP_PCI_STATUS - RW - 16 bits - apcconfig:0x1E			
Field Name	**Bits**	**Default**	**Description**
CAP_LIST (R)	4	0x0	
_66M (R)	5	0x1	
UDF_EN (R)	6	0x0	0=Disable 1=Enable
FAST_B2B_CAPABLE (R)	7	0x0	
DATA_PERR (R)	8	0x0	
DEVSEL_TIMING (R)	10:9	0x1	
SIGNAL_TARGET_ABORT (R)	11	0x0	0=No Abort 1=Target Abort asserted
TARGET_ABORT	12	0x0	0=Inactive 1=Active

MASTER_ABORT	13	0x0	0=Inactive 1=Active
SYSTEM_ERROR	14	0x0	0=No Error 1=SERR asserted
PARITY_ERROR (R)	15	0x0	

APC_AGP_PCI_MEMORY_LIMIT_BASE - RW - 32 bits - apcconfig:0x20			
Field Name	**Bits**	**Default**	**Description**
MEM_BASE_31_20	15:4	0x0	
MEM_LIMIT_31_20	31:20	0x0	

APC_AGP_PCI_PREFETCHABLE_LIMIT_BASE - RW - 32 bits - apcconfig:0x24			
Field Name	**Bits**	**Default**	**Description**
PREF_MEM_BASE_R (R)	3:0	0x1	0h=32-bit memory decoder, 1h=64-bit memory decoder.
PREF_MEM_BASE_31_20	15:4	0x0	Prefetchable Memory Base Address: Prefetchable Memory Base Address defines the base address of the prefetchable address range used by the AGP target (graphics controller) where control registers and FIFO-like communication interfaces are mapped. Bits [15:4] correspond to address bits [31:20]. The lower 20 bits of the address are assumed to be 0. The memory address range adheres to 1-Mbyte alignment and granularity.
PREF_MEM_LIMIT_R (R)	19:16	0x1	0h=32-bit memory decoder, 1h=64-bit memory decoder.
PREF_MEM_LIMIT_31_20	31:20	0x0	Prefetchable Memory Limit Address: Prefetchable Memory Limit Address defines the top address of the prefetchable address range used by the AGP target (graphics controller) where control registers and FIFO-like communication interfaces are mapped. The lower 20 bits of address are assumed to be 0xFFFFF. The memory address range adheres to 1-Mbyte alignment and granularity.
This register defines the base and the size of the prefetchable memory area within the AGP address space.			

APC_AGP_PCI_PREFETCHABLE_BASE_Upper - RW - 32 bits - apcconfig:0x28			
Field Name	**Bits**	**Default**	**Description**
PREF_MEM_BASE_39_32	7:0	0x0	
This register defines the upper base of prefetchable memory area.			

APC_AGP_PCI_PREFETCHABLE_LIMIT_Upper - RW - 32 bits - apcconfig:0x2C			
Field Name	**Bits**	**Default**	**Description**
PREF_MEM_LIMIT_39_32	7:0	0x0	
This register defines the upper limit of prefetchable memory area.			

APC_AGP_PCI_IO_LIMIT_BASE_HI - RW - 32 bits - apcconfig:0x30			
Field Name	**Bits**	**Default**	**Description**
IO_BASE_31_16	15:0	0x0	I/O Base: This field defines the base (inclusive) of 25-bit I/O addresses that are passed to the AGP/PCI bus. Note: Bits [9:15] of this field are hardwired to 0.
IO_LIMIT_31_16	31:16	0x0	I/O Limit: This field defines the upper limit (inclusive) of 25-bit I/O addresses that are passed to the AGP/PCI bus. Note: Bits [9:15] of this field are hardwired to 0.
This set of registers define the valid range of 32-bit I/O addresses that are allowed to be forwarded from the host to the AGP/PCI. Note: if this register is 0, 32-bit addressing mode is effectively disabled.			

APC_CAPABILITIES_PTR - R - 32 bits - apcconfig:0x34			
Field Name	**Bits**	**Default**	**Description**
CAP_PTR	7:0	0x44	This field contains a byte offset into a device's configuration space containing the first item in the capabilities list. If no next item exists, then it is set to null. It is hardwired to 0xB0 to indicate SSID capabilities.
Capabilities Pointer			

APC_AGP_PCI_IRQ_BRIDGE_CTRL - RW - 32 bits - apcconfig:0x3C			
Field Name	**Bits**	**Default**	**Description**
INT_LINE	7:0	0x0	Interrupt Line. Communicates interrupt line routing information. This field is a simple R/W field that allows the BIOS to program to the required value.
INT_PIN	15:8	0x0	Interrupt Pin. Indicates which interrupt pin the PCI to PCI bridge uses. Note: This field is R/W depending on the value of the IntPinCntl bit (Bit [1] of Dev 1:0x40). Refer to Dev1:0x40 for more details. The ability to write to this field is supported in order to allow the BIOS to program to the required value. The RS690 HW does not use this field internally in any way.
PARITY_RESPONSE_EN (R)	16	0x0	Parity Response Enable. The RS690 does not support parity.
SERR_EN	17	0x0	SERR Enable. Forwards the secondary interface SERR# assertions to the primary interface. This bit must be set, along with the SERR Enable bit (Dev 1:F0:0x04), to allow an AGP SERR# to be propagated to the RS690 PCI SERR# pin.

ISA_EN	18	0x0	ISA Enable.
			Modifies the response by the bridge to ISA I/O addresses. This applies only to I/O addresses that are enabled by the I/O Base and I/O Limit registers, and are in the first 64 Kbytes of PCI I/O address space (0000 0000h to 0000 FFFFh).
			When set, the bridge will block any forwarding from primary to secondary of I/O transactions addressing the last 768 bytes in each 1-Kbyte block. In the opposite direction (secondary to primary), I/O transactions are forwarded if they address the last 768 bytes in each 1-Kbyte block.
			  0=Forwards all I/O addresses in the address range defined by the I/O Base and I/O Limit registers.
			  1=Blocks forwarding of ISA I/O addresses in the address range defined by the I/O Base & I/O Limit registers that are in the first 64 Kbytes of PCI I/O address space (top 768 bytes of each 1-Kbyte block).

VGA_EN	19	0x0	VGA Enable. Affects the response by the bridge to compatible VGA addresses. When it is set, the bridge will decode and forward the following accesses on the primary interface to the secondary interface. Memory accesses in the range: 0xA0000 to 0xBFFFF. I/O Address where AD[9:0] are in the ranges: 0x3B0 to 0x3BB and 0x3C0 to 0x3DF (inclusive of ISA address aliases - AD[15:10] are not decoded).
VGA_16_EN	20	0x0	VGA IO 16-bit decoding enable. When set, the northbridge decodes address [15:10] for the VGA IO space. When cleared, the address [15:10] is not decoded for the VGA IO space.
MASTER_ABORT_MODE	21	0x0	Master Abort Mode. Determines the behavior of the PCI to PCI bridge when a master abort termination occurs on either interface when the bridge is the master of the transaction.

SECONDARY_BUS_RESET	22	0x0	Secondary Bus Reset.
			Forces the assertion on the RST# secondary interface.
			  00=Run
			  01=Reset

FAST_B2B_CAPABLE	23	0x0	Fast Back-to-Back Capable:
			This bit is always 0 indicating that the RS690, as a master, is not capable of generating fast back-to-back transactions to different agents on the secondary bus.
			  00=Not Capable
			  01=Capable

APC_MISC_DEVICE_CTRL - RW - 32 bits - apcconfig:0x40			
Field Name	**Bits**	**Default**	**Description**
INT_PIN_CTRL	0	0x0	0=Read-Only 1=Read-Writeable
ApcOrderDisable	1	0x0	If not set, the APC ordering rule is forced. If set, then the APC ordering rule is not forced. 0=Enable 1=Disable
ApcP2PDis	2	0x0	If not set, P2P memory writes target at internal graphics is enabled. 0=Enable 1=Disable
ApcIntSelMode	3	0x0	If set, Interrupt ABCE will be mapped as EFGH.
StpAgpMode	4	0x0	If not set, PMArbDis = STP_AGP. If set, only STP_AGP_Assert message could trigger STP_AGP.
ApcBMSetDis	5	0x0	If not set, the falling edge of BIF_MST_IDLE# will trigger BM_Set message if BM_STS was 0. (Note: BMMsgEn has to be set first to enable BM_Set message generation) 0=Enable 1=Disable
ApcBMSetDis_AGPBUSY	6	0x0	If not set, AGP_BUSY will trigger BM_Set message if BM_STS is 0. (Note: BMMsgEn has to be set first to enable BM_Set message generation) 0=Enable 1=Disable

APC_HT_MSI_CAP - R - 32 bits - apcconfig:0x44			
Field Name	**Bits**	**Default**	**Description**
CAP_ID	7:0	0x8	
CAP_POINTER	15:8	0xb0	
EN	16	0x1	
Fixd	17	0x1	
RESERVED_26_18	26:18	0x0	
CAPABILITY_TYPE	31:27	0x15	

APC_ADAPTER_ID_W - RW - 32 bits - apcconfig:0x4C			
Field Name	**Bits**	**Default**	**Description**
SUBSYSTEM_VENDOR_ID	15:0	0x1002	
SUBSYSTEM_ID	31:16	0x7912	
Subsystem Vendor ID and Subsystem ID write register.			

APC_SSID_CAP_ID - R - 32 bits - apcconfig:0xB0			
Field Name	**Bits**	**Default**	**Description**
CAP_ID	7:0	0xd	CapID
NEXT_PTR	15:8	0x80	Pointer to the next item in the capabilities list.
Reserved	31:16	0x0	
This read-only register describes the SSID implemented (1.2).			

APC_SSID - R - 32 bits - apcconfig:0xB4			
Field Name	**Bits**	**Default**	**Description**
SUBSYSTEM_VENDOR_ID *(mirror of APC_ADAPTER_ID_W:SUBSYSTEM_VENDOR_ID)*	15:0	0x0	
SUBSYSTEM_ID *(mirror of APC_ADAPTER_ID_W:SUBSYSTEM_ID)*	31:16	0x0	
Subsystem Vendor ID and Subsystem ID register.			

2.8   Side-Port Memory Controller Registers

MC_GENERAL_PURPOSE - RW - 32 bits - NBMCIND:0x0			
Field Name	**Bits**	**Default**	**Description**
MEM_AIC_CONT_REQ_G1	3:0	0x0	Number of consecutive AGP/PCI requests for group 1 clients (G3D0R, G3D0W, G3D1R, G3D1W, GTX0R) 0=Single request 15=16 requests in row
MEM_AIC_CONT_REQ_G2	7:4	0x0	Number of consecutive AGP/PCI requests for group 2 clients (HDPW, CPW, DISP2R, HDPR, CPR, OVLYR, DISPR, IDCTR) 0=Single request 15=16 requests in row
MEM_GART_SYNCHRO_FIFO	8	0x1	N/A
MEM_GART_2DW	9	0x1	N/A
MEM_SUS_STAT_EN	10	0x0	When TVCLKIN is used as the SUS_STATb signal this bit must be set to 1; else this bit is set to 0
MEM_D3_RBS_IDLE	11	0x0	
MEM_D3_MCB_IDLE	12	0x0	
RBS_SP_64BYTE_RTR4	13	0x0	
REG_RD_DELAY	18:16	0x3	
STUTTER_IGNORE_C3	19	0x0	
MC_INIT_COMPLETE	31	0x0	As long as this bit is 0, the MC will not accept requests from the clients. This is used primarily to block requests when the MC might mishandle them, such as when the FB or AGP apertures are undefined or unstable. 0=Register Initialization Not Complete 1=Register Initialization Complete
Memory controller general purpose register.			

MC_MISC_CNTL - RW - 32 bits - NBMCIND:0x18			
Field Name	**Bits**	**Default**	**Description**
DISABLE_GTW	1	0x0	N/A
DBL_FLOP_EN	2	0x0	
GART_INDEX_REG_EN	12	0x0	This bit switches between MMGART registers and MCIND GART registers when NOT in AGP3.x/enhanced mode. Bits [4:3] of NBCFG:NBCNTL, NBMISCIND 0x0 (AGP30ENHANCED, AGP30ENHANCED) must be 00 for this register to take effect. 0=Use mmgart registers. 1=Use mcind gart registers.
BLOCK_GFX_D3_EN	14	0x1	
DEBUGBUS_CYCLE_EN	31	0x0	Enables all available debug bus signals to cycle every 16 clocks. 0=Disable 1=Enable
Miscellaneous controls for memory controller			

K8_FB_LOCATION - RW - 32 bits - NBMCIND:0x1E			
Field Name	**Bits**	**Default**	**Description**
K8_FB_START	31:0	0x0	This register indicates the start of the frame buffer in the K8's system memory. The frame buffer in system memory is not allowed to span across 4G boundaries. Note: Bits [4:0] of this field are hardwired to 0.
Start of frame buffer in shared K8 system memory.			

NB_MC_DEBUG - RW - 32 bits - NBMCIND:0x1F			
Field Name	**Bits**	**Default**	**Description**
Reserved0	2:0	0x0	0=Reserved
RBS_STALL_FIFO	3	0x0	0=Normal operation 1=Do not pop data out of read_bus_switch FIFO
Reserved1	4	0x0	0=Reserved
NC_DEBUG_MUX	14:8	0x0	0=Debug bus mux select
MC_DEBUG_EN	15	0x0	0=Disable 1=Enable
TESTBUS_INT (R)	31:16	0x0	Read back of the debug bus value.

MC_PM_CNTL - RW - 32 bits - NBMCIND:0x26			
Field Name	**Bits**	**Default**	**Description**
AUTO_CLOCK_THROTTLING	0	0x0	For internal graphic clients. 0=Clock throttling state is set by THROTTLE_STATE_SETTING register 1=Clock throttling state is set by the input signals from clk top.
CLOCK_THROTTLING_EN	1	0x0	For internal graphic clients. 0=Disable clock throttling function 1=Enable clock throttling function
THROTTLE_STATE_SETTING	3:2	0x0	For internal graphic clients. 00=No blocking 01=Block the incoming requests 64 clock cycles every 128 clock cycles. 10=Block the incoming requests 96 clock cycles every 128 clock cycles. 11=Block the incoming requests 112 clock cycles every 128 clock cycles.
AUTO_CLOCK_THROTTLING_NB	4	0x0	For internal graphic clients. 0=Clock throttling state is set by THROTTLE_STATE_SETTING_NB register 1=Clock throttling state is set by the input signals from clk_top
CLOCK_THROTTLING_EN_NB	5	0x0	For NB clients 0=Disable clock throttling function 1=Enable clock throttling function

THROTTLE_STATE_SETTING_NB	7:6	0x0	For NB clients
			  00=No blocking
			  01=Block the incoming requests 64 clock cycles every
			  128 clock cycles.
			  10=Block the incoming requests 96 clock cycles every
			  128 clock cycles.
			  11=Block the incoming requests 112 clock cycles every
			  128 clock cycles.

BLACKOUT_NB_DELAY	8	0x0	Delay the NB blackout request from clk_top
			  0=Delay 1 clock cycle
			  1=Delay 2 clock cycles.

THROTTLE_READ_EN	9	0x0	Enables clock throttling feature to block both NB and graphic read requests (except display and display2 requests).
			  0=Disable
			  1=Enable

THROTTLE_WRITE_EN	10	0x0	Enables clock throttling feature to block both NB and graphic write requests.
			  0=Disable
			  1=Enable

THROTTLE_DISP_EN	11	0x0	Enables clock throttling feature to block both display and display2 requests.
			  0=Disable
			  1=Enable

Power management refresh control & clock throttling.			

GART_FEATURE_ID - RW - 32 bits - NBMCIND:0x2B			
Field Name	**Bits**	**Default**	**Description**
REV_ID	7:0	0x0	This field contains the Revision ID. Read Only = 01 Note: Bits [1:0] of this field are hardwired to 0.
VAL_CAP	8	0x0	This bit is set to indicate that the RS690 supports the detection of Valid Bit errors Read Only = 1 0=N/A
LINK_CAP	9	0x0	This bit is always low, indicating that GART Entry Multiple Pages are not Supported Read Only = 0 00=N/A
P2P_CAP	10	0x0	This bit is hardwired to 0 to indicate that the RS690 only implements those PCI-PCI Bridge commands required to implement AGP (the RS690 does not implement a complete PCI2.2 compliant PCI-PCI bridge between PCI and AGP). 00=N/A

HANG_EN	11	0x0	When set, illegal GART entries fetched by the GTW logic will force the RS690 to hang.
			  0=Do not hang state machine on invalid page table
			  1=Hang state machine

GARV_ERR_EN	16	0x0	When set, the RS690 will assert SERR when a graphics device attempts to access a page in AGP memory which is not valid (Valid Bit Error). A valid bit error will cause the GART Table walk state machine to hang. The processor can still access memory after that if it does not use GART address space 00=N/A

SB_STB_TOGGLE_DETECT_DISABLE	17	0x0	When set, this bit disables the AGP Sideband strobe toggle detect logic. This bit must be set for normal operation. 00=N/A

TLB_ENABLE	18	0x0	When set, this bit enables the caching of GART TLB entries.
			  0=TLB caching disabled
			  1=TLB caching enabled

P2P_ENABLE	19	0x0	This bit is hardwired to 0 to indicate that the RS690 only implements those PCI-PCI Bridge commands required to implement AGP (the RS690 does not implement a complete PCI2.2 compliant PCI-PCI bridge between PCI and AGP) 00=N/A

VAL_ERROR (R)	24	0x0	When set, this bit indicates that a Valid Bit Error has been detected and SERR has been asserted.
			Initial State=0.
			  0=OK
			  1=Valid Bit Error

GTW_LAC_EN	25	0x0	When set, this bit turns on the GTW's Look-Ahead_Cache, which caches previous 32-byte Page Table Access.
			  0=Disable GTW's LAC
			  1=Enable GTW's LAC

GART_CACHE_STATUS	26	0x0	When set, the GART cache has been enabled by software. When clear, the GART cache is disabled. Initial State=0. 00=N/A
P2P_STATUS	27	0x0	This bit is hardwired to zero to indicate that the RS690 only implements those PCI-PCI Bridge commands required to implement AGP (RS690) does not implement a complete PCI 2.2 compliant PCI-PCI bridge between PCI and AGP) 0=N/A

VALID_BIT_ERROR_ID (R)	29:28	0x0	These bits are used to determine the source of the valid bit error. The values are as follows.
			  00=AGP
			  01=CPU 0
			  10=Undefined
			  11=PCI / AGP's PCI
			Initial State=00
			  0=00 - PDQry
			  1=01 - PTQry
			  2=10 - GtwLACHit
			  3=11 - GtwQWait

LV1_INDEX	30	0x0	Level 1 Index:
			GART Index Scheme Control. When set to 1, this bit enables the 1-level GART Mode. When cleared to 0, 2-level GART Mode is enabled
			  0=2 Level GART
			  1=1 Level GART

PDC_EN	31	0x0	Page Directory Cache Enable:
			GART Page Directory Cache Enable. This bit is used only in the 2-Level GART Mode. It has no effect in the 1-Level GART Mode. The GART Directory is enabled only when both this bit and the AGP Features Control Register (offset 02h of the memory-mapped Features and Capabilities Register) bit 2, 'GART Cache Enable' are 1s. This bit is included for performance studies and debug.
			  0=Disable Page Directory Cache
			  1=Enable Page Directory Cache

GART Feature and Capability Register			

GART_BASE - RW - 32 bits - NBMCIND:0x2C			
Field Name	Bits	Default	Description
DIRECTORY_BASE_HI	11:4	0x0	Bits [39:32] of GART directory base.
DIRECTORY_BASE_LO	31:12	0x0	Bits [31:12] of GART directory base.
GART Directory Base Address, 4 kB granularity.			

GART_CACHE_SZBASE - R - 32 bits - NBMCIND:0x2D			
Field Name	Bits	Default	Description
GART_CACHE_SIZE	31:0	0x10	Hardwired to 0x00000010
GART Cache Size Number of entries.			

GART_CACHE_CNTRL - RW - 32 bits - NBMCIND:0x2E			
Field Name	Bits	Default	Description

GART_CACHE_INVALIDATE_W (W)	0	0x0	When set to 1, the entire GART Directory and Table Cache is invalidated. When the operation is completed, set this bit to 0.
			  0=No change
			  1=Clear Tlb

GART_CACHE_INVALIDATE_R (R)	0	0x0	When GART_CACHE_INVALIDATE_W is set to 1, GART_CACHE_INVALIDATE_R will toggle from 1 to 0 when the operation is completed.
			  0=Done Clear
			  1=Clear Pending

GART Cache Control Register			

GART_CACHE_ENTRY_CNTRL - RW - 32 bits - NBMCIND:0x2F			
Field Name	Bits	Default	Description
TIB_INV_ENT_R (R)	0	0x0	0=Invalidate Done 1=Invalidate Pending
TIB_INV_ENT_W (W)	0	0x0	0=No Invalidate 1=Invalidate Tlb
TIB_UPDATE_R (R)	1	0x0	0=Update Done 1=Update Pending
TIB_UPDATE_W (W)	1	0x0	0=No Update 1=Update Tlb
GART_TABLE_ENTRY_ADDRESS	31:12	0x0	Virtual address of GART entry to invalidate/update.
This register allows the driver to update/invalidate specific entries in the GART cache.			

GART_ERROR_0 - RW - 32 bits - NBMCIND:0x30			
Field Name	**Bits**	**Default**	**Description**
INVALID_WRITE (R)	1:0	0x0	0=Write attempted to addr with WrValid not set 1=No error
INVALID_WRITE_ADDR (R)	15:2	0x0	Address of an AGP write request that hit an invalid aperture page.
INVALID_READ (R)	17:16	0x0	0=Read attempted to addr with RdValid not set 1=No error
INVALID_READ_ADDR (R)	31:18	0x0	Address of an AGP read request that hit an invalid aperture page.

GART_ERROR_1 - RW - 32 bits - NBMCIND:0x31			
Field Name	**Bits**	**Default**	**Description**
INVALID_WRITE (R)	1:0	0x0	0=Write attempted to addr with WrValid not set 1=No error
INVALID_WRITE_ADDR (R)	15:2	0x0	Address of an AGP write request that hit an invalid aperture page.
INVALID_READ (R)	17:16	0x0	0=Read attempted to addr with RdValid not set 1=No error
INVALID_READ_ADDR (R)	31:18	0x0	Address of an AGP read request that hit an invalid aperture page.

GART_ERROR_2 - RW - 32 bits - NBMCIND:0x32			
Field Name	**Bits**	**Default**	**Description**
INVALID_WRITE (R)	1:0	0x0	0=Write attempted to addr with WrValid not set 1=No error
INVALID_WRITE_ADDR (R)	15:2	0x0	Address of an AGP write request that hit an invalid aperture page.
INVALID_READ (R)	17:16	0x0	0=Read attempted to addr with RdValid not set 1=No error
INVALID_READ_ADDR (R)	31:18	0x0	Address of an AGP read request that his an invalid aperture page.

GART_ERROR_3 - RW - 32 bits - NBMCIND:0x33			
Field Name	**Bits**	**Default**	**Description**
INVALID_WRITE (R)	1:0	0x0	0=Write attempted to addr with WrValid not set 1=No error
INVALID_WRITE_ADDR (R)	15:2	0x0	Address of an AGP write request that hit an invalid aperture page.
INVALID_READ (R)	17:16	0x0	0=Read attempted to addr with RdValid not set 1=No error
INVALID_READ_ADDR (R)	31:18	0x0	Address of an AGP read request that his an invalid aperture page.

GART_ERROR_4 - RW - 32 bits - NBMCIND:0x34			
Field Name	**Bits**	**Default**	**Description**
INVALID_WRITE (R)	1:0	0x0	0=Write attempted to addr with WrValid not set 1=No error
INVALID_WRITE_ADDR (R)	15:2	0x0	Address of an AGP write request that hit an invalid aperture page.
INVALID_READ (R)	17:16	0x0	0=Read attempted to addr with RdValid not set 1=No error
INVALID_READ_ADDR (R)	31:18	0x0	Address of an AGP read request that hit an invalid aperture page.

GART_ERROR_5 - RW - 32 bits - NBMCIND:0x35			
Field Name	**Bits**	**Default**	**Description**
INVALID_WRITE (R)	1:0	0x0	0=Write attempted to addr with WrValid not set 1=No error
INVALID_WRITE_ADDR (R)	15:2	0x0	Address of an AGP write request that hit an invalid aperture page.
INVALID_READ (R)	17:16	0x0	0=Read attempted to addr with RdValid not set 1=No error
INVALID_READ_ADDR (R)	31:18	0x0	Address of an AGP read request that hit an invalid aperture page.

GART_ERROR_6 - RW - 32 bits - NBMCIND:0x36			
Field Name	**Bits**	**Default**	**Description**
INVALID_WRITE (R)	1:0	0x0	0=Write attempted to addr with WrValid not set 1=No error
INVALID_WRITE_ADDR (R)	15:2	0x0	Address of an AGP write request that hit an invalid aperture page.
INVALID_READ (R)	17:16	0x0	0=Read attempted to addr with RdValid not set 1=No error
INVALID_READ_ADDR (R)	31:18	0x0	Address of an AGP read request that hit an invalid aperture page.

GART_ERROR_7 - RW - 32 bits - NBMCIND:0x37			
Field Name	**Bits**	**Default**	**Description**
INVALID_WRITE (R)	1:0	0x0	0=Write attempted to addr with WrValid not set 1=No error
INVALID_WRITE_ADDR (R)	15:2	0x0	Address of an AGP write request that hit an invalid aperture page.
INVALID_READ (R)	17:16	0x0	0=Read attempted to addr with RdValid not set 1=No error
INVALID_READ_ADDR (R)	31:18	0x0	Address of an AGP read request that hit an invalid aperture page.

AGP_ADDRESS_SPACE_SIZE - RW - 32 bits - NBMCIND:0x38			
Field Name	Bits	Default	Description
GART_EN	0	0x0	N/A
VA_SIZE	3:1	0x0	0=32 MB 1=64 MB 2=128 MB 3=256 MB 4=512 MB 5=1 GB 6=2 GB 7=Undefined
VGA_IA_EN	16	0x0	N/A

AGP_MODE_CONTROL - RW - 32 bits - NBMCIND:0x39			
Field Name	Bits	Default	Description
POST_GART_Q_SIZE	18	0x0	N/A
NONGART_SNOOP	19	0x0	N/A
AGP_RD_BUF_SIZE	20	0x0	N/A
REQ_TYPE_SNOOP	23:22	0x1	N/A
REQ_TYPE_SNOOP_EN	24	0x1	0=Enable snoop of gart-mapped physical address 1=Disable snoop

AIC_CTRL_SCRATCH - RW - 32 bits - NBMCIND:0x3A			
Field Name	Bits	Default	Description
TRANSLATE_EN	0	0x0	N/A. 0=N/A
DIS_OUT_OF_PCI_GART_ACCESS	1	0x0	0=Out of PCI GART access enabled. 1=Out of PCI GART access disabled.
RBB_AGP3X_LacDisable	2	0x0	0=GART LAC controlled by APC_AGP_CONTROL, TlbEn when in AGP3X mode. 1=GART LAC DISABLED when in AGP3X mode.
RBB_AGP3X_TlbDisable	3	0x0	0=GART client TLB controlled by APC_AGP_CONTROL, TlbEn when in AGP3X mode. 1=GART client TLB DISABLED when in AGP3X mode.
GART_LAC_EN_OVERIDE	4	0x0	0=Use LAC enable register bit of GART's mode of operation (mmgart or apcconfig). 1=Over-ride mmgart or apcconfig LAC enable register bits and use nbmcind 0.2B, GART_FEATURE_ID, bit [25].
GART_SNOOP_EN_OVERRIDE	5	0x0	0=Use snoop enable register bit of GART's mode of operation (mmgart or apcconfig). 1=Over-ride mmgart or apcconfig snoop enable register bits and use nbmcind 0x39, AGP_MODE_CONTROL, bit [24].
GART_INVALIDATE_OVERRIDE	6	0x0	0=Use cache invalidate register bit of GART's mode of operation (mmgart or apcconfig). 1=Over-ride mmgart or apcconfig cache invalidate register bits and use nbmcind 0x2E, GART_CACHE_CNTRL, bit [0].

GART_HANG_EN_OVERRIDE	7	0x0	0=Use hang enable register bit of gart's mode of operation (mmgart). 1=Over-ride mmgart or apcconfig hang enable register bits and use nbmcind 0x2E, GART_CACHE_CNTRL, bit [0].
DIS_ARB_AGP_FB	8	0x0	0=Enable mix APG and framebuffer 1=Disable mix APG and framebuffer

MC_GART_ERROR_ADDRESS - RW - 32 bits - NBMCIND:0x3B			
Field Name	**Bits**	**Default**	**Description**
MC_GART_ERROR_ADDRESS	31:0	0x0	Bits [31:0] of gart_error_address. Address that GART sends to mc arbiters or bif when clients try to access an invalid physical address.
Bits [31:0] of gart error_address.			

MC_GART_ERROR_ADDRESS_HI - RW - 32 bits - NBMCIND:0x3C			
Field Name	**Bits**	**Default**	**Description**
MC_GART_ERROR_ADDRESS_HI	7:0	0x0	Bits [39:40] of gart_error_address
Bits [39:40] of gart_error_address.			

MC_MISC_CNTL2 - RW - 32 bits - NBMCIND:0x4E			
Field Name	**Bits**	**Default**	**Description**
AGP_LATENCY_TIMER	3:0	0x0	Sets the latency timer for internal AGP.

AGP_FIFO_LEVEL_URG_EN	4	0x0	Enables internal AGP urgency based on FIFO level
			  0=Disable
			  1=Enable

AGP_FIFO_LEVEL_MAX	8:5	0x0	Specifies the FIFO level that triggers internal AGP as the urgent client. AgpFifoLevelUrgEn needs to be enabled.
AGP_FIFO_LEVEL_DRAIN	12:9	0x0	Specifies to what level FIFO needs to be drained before urgency for the internal AGP is turned off. AgpFifoLev
DELAY_EMPTY	21	0x0	
DELAY_NOT_FULL	22	0x0	
GFX_IDLE_LIMIT	28:23	0x4	Masks the bank for GFX_IDLE_LIMIT * 4 cycles in second level arbiter.

AgpPriorEn	31	0x0	Enables internal AGP as a priority client.
			  0=Disable
			  1=Enable

Miscellaneous controls(2) for memory controller			

MC_MISC_UMA_CNTL - RW - 32 bits - NBMCIND:0x5F			
Field Name	**Bits**	**Default**	**Description**
K8_40BIT_ADDR_EXTENSION	7:0	0x0	Upper fixed 8-bits of the 40-bit K8 address space. All addresses that are directed at the K8 frame buffer memory will be prefixed with this value.
GART_BYPASS	8	0x0	0=Enable gart table translations on chipset 1=Bypass gart table on chipset
GFX_64BYTE_MODE	9	0x0	
GFX_64BYTE_LAT	14:10	0x0	
GTW_COHERENCY	15	0x0	0=GTW requests will not be issued as a coherent request 1=GTW requests will be issued as a coherent request
READ_BUFFER_SIZE	23:16	0x80	Defines the size of Read Data Return Buffer in the read-bus-switch (max = 128, min = 8).
HDR_ROUTE_TO_DSP	24	0x0	1=HDP requests routed to display pipe. 0=HDP requests routed to graphics pipe. Def=0
GTW_ROUTE_TO_DSP	25	0x0	1=GTW requests routed to display pipe. 0=GTW requests routed to graphics pipe. Def=0 0=Disable 1=Enable
DSP_ROUTE_TO_GFX	26	0x0	1=Display requests routed to graphics pipe. 0=Display requests routed to display pipe. Def=0
USE_HDPW_LAT_INIT	27	0x0	1=Route HDP reads to isochronous display pipe after being block by HDP writes for a certain number of clocks (HDR_LAT_INIT_HDPW). 0=Disable.
USE_GFXW_LAT_INIT	28	0x0	1=Route HDP reads to isochronous display pipe after being block by any GFX writes for a certain number of clocks (HDR_LAT_INIT_GFXW). 0=Disable.
MCIFR_COHERENT	29	0x0	
NON_SNOOP_AZR_AIC_BP	30	0x0	
SIDE_PORT_PRESENT_W (W)	31	0x0	0=Sideport not present 1=Sideport present
SIDE_PORT_PRESENT_R (R)	31	0x0	0=Sideport not present 1=Sideport present

K8_DRAM_CS0_BASE - RW - 32 bits - NBMCIND:0x63			
Field Name	**Bits**	**Default**	**Description**
CSBE	0	0x1	0=Chip-Select Bank not enabled 1=Chip-Select Bank enabled
BaseAddrLo_Ext_RevF	8:5	0x0	
BaseAddrLo	15:9	0x0	This field is only used in optimized case (interleave mode) when all chip select banks are the same size and the type and the number of chip selects is a power of two. In this case, the memory is interleaved differently to avoid page conflicts.
BaseAddrHi_Ext_RevF	20:19	0x0	
BaseAddrHi	31:21	0x0	This field defines the top 11 address bits of a 40-bit address that defines the memory address space. These bits decode 32-Mbyte blocks of memory. In the non-interleaving mode, BaseAddrLo has a value of 0.
Mirror image of Opteron processor DRAM_CS_Base_Address register, Function 2: Offset 40h. Refer to BKDG for AMD64 and AMD Opteron.			

K8_DRAM_CS1_BASE - RW - 32 bits - NBMCIND:0x64			
Field Name	**Bits**	**Default**	**Description**
CSBE	0	0x1	0=Chip-Select Bank not enabled 1=Chip-Select Bank enabled
BaseAddrLo_Ext_RevF	8:5	0x0	
BaseAddrLo	15:9	0x0	See the description for the corresponding field in K8_DRAM_CS0_BASE
BaseAddrHi_Ext_RevF	20:19	0x0	
BaseAddrHi	31:21	0x20	See the description for the corresponding field in K8_DRAM_CS0_BASE
Mirror image of Opteron processor DRAM_CS_Base_Address register, Function 2: Offset 44h. Refer to BKDG for AMD64 and AMD Opteron.			

K8_DRAM_CS2_BASE - RW - 32 bits - NBMCIND:0x65			
Field Name	**Bits**	**Default**	**Description**
CSBE	0	0x1	0=Chip-Select Bank not enabled 1=Chip-Select Bank enabled
BaseAddrLo_Ext_RevF	8:5	0x0	
BaseAddrLo	15:9	0x0	See the description for the corresponding field in K8_DRAM_CS0_BASE
BaseAddrHi_Ext_RevF	20:19	0x0	
BaseAddrHi	31:21	0x40	See the description for the corresponding field in K8_DRAM_CS0_BASE
Mirror image of Opteron processor DRAM_CS_Base_Address register, Function 2: Offset 48h. Refer to BKDG for AMD64 and AMD Opteron.			

K8_DRAM_CS3_BASE - RW - 32 bits - NBMCIND:0x66			
Field Name	**Bits**	**Default**	**Description**
CSBE	0	0x1	0=Chip-Select Bank not enabled 1=Chip-Select Bank enabled
BaseAddrLo_Ext_RevF	8:5	0x0	
BaseAddrLo	15:9	0x0	See the description for the corresponding field in K8_DRAM_CS0_BASE
BaseAddrHi_Ext_RevF	20:19	0x0	
BaseAddrHi	31:21	0x60	See the description for the corresponding field in K8_DRAM_CS0_BASE
Mirror image of Opteron processor DRAM_CS_Base_Address register, Function 2: Offset 4Ch. Refer to BKDG for AMD64 and AMD Opteron.			

K8_DRAM_CS4_BASE - RW - 32 bits - NBMCIND:0x67			
Field Name	**Bits**	**Default**	**Description**
CSBE	0	0x0	0=Chip-Select Bank not enabled 1=Chip-Select Bank enabled
BaseAddrLo_Ext_RevF	8:5	0x0	
BaseAddrLo	15:9	0x0	See the description for the corresponding field in K8_DRAM_CS0_BASE
BaseAddrHi_Ext_RevF	20:19	0x0	
BaseAddrHi	31:21	0x80	See the description for the corresponding field in K8_DRAM_CS0_BASE
Mirror image of Opteron processor DRAM_CS_Base_Address register, Function 2: Offset 50h. Refer to BKDG for AMD64 and AMD Opteron.			

K8_DRAM_CS5_BASE - RW - 32 bits - NBMCIND:0x68			
Field Name	**Bits**	**Default**	**Description**
CSBE	0	0x0	0=Chip-Select Bank not enabled 1=Chip-Select Bank enabled
BaseAddrLo_Ext_RevF	8:5	0x0	
BaseAddrLo	15:9	0x0	See the description for the corresponding field in K8_DRAM_CS0_BASE
BaseAddrHi_Ext_RevF	20:19	0x0	
BaseAddrHi	31:21	0x80	See the description for the corresponding field in K8_DRAM_CS0_BASE
Mirror image of Opteron processor DRAM_CS_Base_Address register, Function 2: Offset 54h. Refer to BKDG for AMD64 and AMD Opteron.			

K8_DRAM_CS6_BASE - RW - 32 bits - NBMCIND:0x69			
Field Name	**Bits**	**Default**	**Description**
CSBE	0	0x0	0=Chip-Select Bank not enabled 1=Chip-Select Bank enabled
BaseAddrLo_Ext_RevF	8:5	0x0	
BaseAddrLo	15:9	0x0	See the description for the corresponding field in K8_DRAM_CS0_BASE
BaseAddrHi_Ext_RevF	20:19	0x0	
BaseAddrHi	31:21	0x80	See the description for the corresponding field in K8_DRAM_CS0_BASE
Mirror image of Opteron processor DRAM_CS_Base_Address register, Function 2: Offset 58h. Refer to BKDG for AMD64 and AMD Opteron.			

K8_DRAM_CS7_BASE - RW - 32 bits - NBMCIND:0x6A

Field Name	Bits	Default	Description
CSBE	0	0x0	0=Chip-Select Bank not enabled 1=Chip-Select Bank enabled
BaseAddrLo_Ext_RevF	8:5	0x0	
BaseAddrLo	15:9	0x0	See the description for the corresponding field in K8_DRAM_CS0_BASE
BaseAddrHi_Ext_RevF	20:19	0x0	
BaseAddrHi	31:21	0x80	See the description for the corresponding field in K8_DRAM_CS0_BASE
Mirror image of Opteron processor DRAM_CS_Base_Address register, Function 2: Offset 5Ch. Refer to BKDG for AMD64 and AMD Opteron.			

K8_DRAM_CS0_MASK - RW - 32 bits - NBMCIND:0x6B

Field Name	Bits	Default	Description
AddrMaskLo_Ext_RevF	8:5	0xf	
AddrMaskLo	15:9	0x7f	This field specifies the addresses to be excluded for the optimized case descried in the Base Address bit definitions (see description for register K8_DRAM_CS0_BASE).
AddrMaskHi_Ext_RevF	20:19	0x3	
AddrMaskHi	29:21	0x1f	This field defines the top Address Mask bits. The bits with an address mask of 1 are excluded from the address comparison. This allows the memory block size to be larger than 32 Mbytes. If Address Mask bit 25 is set to 1, the memory block size is 64 Mbytes.
Mirror image of Opteron processor DRAM_CS_Mask register, Function 2: Offset 60h.			

K8_DRAM_CS1_MASK - RW - 32 bits - NBMCIND:0x6C

Field Name	Bits	Default	Description
AddrMaskLo_Ext_RevF	8:5	0xf	
AddrMaskLo	15:9	0x7f	See the description for the corresponding field in K8_DRAM_CS0_MASK
AddrMaskHi_Ext_RevF	20:19	0x3	
AddrMaskHi	29:21	0x1f	See the description for the corresponding field in K8_DRAM_CS0_MASK
Mirror image of Opteron processor DRAM_CS_Mask register, Function 2: Offset 64h. Refer to BKDG for AMD64 and AMD Opteron.			

K8_DRAM_CS2_MASK - RW - 32 bits - NBMCIND:0x6D

Field Name	Bits	Default	Description
AddrMaskLo_Ext_RevF	8:5	0xf	
AddrMaskLo	15:9	0x7f	See the description for the corresponding field in K8_DRAM_CS0_MASK
AddrMaskHi_Ext_RevF	20:19	0x3	
AddrMaskHi	29:21	0x1f	See the description for the corresponding field in K8_DRAM_CS0_MASK
Mirror image of Opteron processor DRAM_CS_Mask register, Function 2: Offset 68h. Refer to BKDG for AMD64 and AMD Opteron.			

K8_DRAM_CS3_MASK - RW - 32 bits - NBMCIND:0x6E			
Field Name	**Bits**	**Default**	**Description**
AddrMaskLo_Ext_RevF	8:5	0xf	
AddrMaskLo	15:9	0x7f	See the description for the corresponding field in K8_DRAM_CS0_MASK
AddrMaskHi_Ext_RevF	20:19	0x3	
AddrMaskHi	29:21	0x1f	See the description for the corresponding field in K8_DRAM_CS0_MASK
Mirror image of Opteron processor DRAM_CS_Mask register, Function 2: Offset 6Ch. Refer to BKDG for AMD64 and AMD Opteron.			

K8_DRAM_CS4_MASK - RW - 32 bits - NBMCIND:0x6F			
Field Name	**Bits**	**Default**	**Description**
AddrMaskLo	15:9	0x7f	See the description for the corresponding field in K8_DRAM_CS0_MASK
AddrMaskHi	29:21	0x1ff	See the description for the corresponding field in K8_DRAM_CS0_MASK
Mirror image of Opteron processor DRAM_CS_Mask register, Function 2: Offset 70h. Refer to BKDG for AMD64 and AMD Opteron.			

K8_DRAM_CS5_MASK - RW - 32 bits - NBMCIND:0x70			
Field Name	**Bits**	**Default**	**Description**
SPARE_70 (R)	7:0	0x0	Reserved.
AddrMaskLo	15:9	0x7f	See description for corresponding field in K8_DRAM_CS0_MASK
AddrMaskHi	29:21	0x1ff	See description for corresponding field in K8_DRAM_CS0_MASK
Mirror image of Opteron processor DRAM_CS_Mask register, Function 2: Offset 74h. Refer to BKDG for AMD64 and AMD Opteron.			

K8_DRAM_CS6_MASK - RW - 32 bits - NBMCIND:0x71			
Field Name	**Bits**	**Default**	**Description**
SPARE_71	7:0	0x0	Reserved
AddrMaskLo	15:9	0x7f	See the description for the corresponding field in K8_DRAM_CS0_MASK.
AddrMaskHi	29:21	0x1ff	See the description for the corresponding field in K8_DRAM_CS0_MASK.
Mirror image of Opteron processor DRAM_CS_Mask register, Function 2:Offset 78h. Refer to BKDG for AMD64 and AMD Opteron.			

K8_DRAM_CS7_MASK - RW - 32 bits - NBMCIND:0x72			
Field Name	**Bits**	**Default**	**Description**
SPARE_72	7:0	0x0	Reserved
AddrMaskLo	15:9	0x7f	See the description for the corresponding field in K8_DRAM_CS0_MASK.
AddrMaskHi	29:21	0x1ff	See the description for the corresponding field in K8_DRAM_CS0_MASK.
Mirror image of Opteron processor DRAM_CS_Mask register, Function 2:Offset 7Ch. Refer to BKDG for AMD64 and AMD Opteron.			

K8_DRAM_BANK_ADDR_MAPPING - RW - 32 bits - NBMCIND:0x73			
Field Name	**Bits**	**Default**	**Description**
CS01	3:0	0x5	0=32MB 1=64MB 2=128MB 3=256MB 4=512MB 5=1GB 6=2GB 7=Reserved
CS23	7:4	0x5	0=32MB 1=64MB 2=128MB 3=256MB 4=512MB 5=1GB 6=2GB 7=Reserved
CS45	11:8	0x0	0=32MB 1=64MB 2=128MB 3=256MB 4=512MB 5=1GB 6=2GB 7=Reserved
CS67	15:12	0x0	0=32MB 1=64MB 2=128MB 3=256MB 4=512MB 5=1GB 6=2GB 7=Reserved

SPARE_73	27:16	0x0	SPARE_73 [1:0] are used to select which read client will be monitored to receive an average value of request latency in MCLK. The select decode is as follows:
			
			  2'b00=gtx0r
			  2'bx1=g3d1r
			  2'b10=g3d0r
			
			The programming sequence to turn on the latency monitor is the same procedure as turning on the performance counters for channelB: set MC1_PERF_CNTL.EVENT0_SEL = 8'h7e and MC1_PERF_CNTL.EVENT1_SEL = 8'h7f which choose the two performance counters.
			
			To get the average value, divide:
			{MC1_PERF_CNTL.COUNTER0_UPPER, MC1_PERF_COUNT0}
			by
			{MC1_PERF_CNTL.COUNTER1_UPPER, MC1_PERF_COUNT1}.
			
			SPARE_73[5:2] are used to XOR (g3d1r and g3d1w) address[16:13].This is a one-to-one mapping where SPARE_73[2] is XOR'd with address[13] and SPARE_73[3] is XOR'd with SPARE_73[14], and so on. The address bit to XOR will be determined by the address bits used to define bank select in the K8 memory controller. The purpose of XOR'ing the address bit is to improve the odds that requests will go to different banks when multiple clients are making requests in parallel.

RevF_Mode	28	0x0	
AddrDecMode	30	0x1	0=RevC 1=RevD
MemWidth	31	0x0	0=64-bit interface 1=128-bit interface

MC_MPLL_CONTROL - RW - 32 bits - NBMCIND:0x74			
Field Name	**Bits**	**Default**	**Description**
MPLL_CAL_TRIGGER	0	0x0	Memory PLL calibration trigger. Set from 0 to 1 to start calibration.

MPLL_LOCKED (R)	1	0x0	Memory PLL locking read back status.
			  0=No lock
			  1=PLL lock

MPLL_SKEW1X_CORE	4:2	0x0	This register field is not used.
MPLL_SKEW2	7:5	0x0	2X output clock (O2X) skew control
MPLL_SKEW1	10:8	0x0	1X output clock (O1X) skew control
MPLL_SKEW_DLY	14:11	0x0	This register field is not used.
MPLL_DLL_CLEN	15	0x0	This register bit is not used.
MPLL_DLL_PWDN	16	0x0	Core-clock tree cancellation DLL power-down
MPLL_SKEW_TREE	19:17	0x0	This register field is not used.
MPLL_VCOREF	23:20	0x0	VCO input reference voltage setting
MPLL_CALREF	27:24	0x0	2nd VCO input reference voltage setting

MPLL_BYPASS	28	0x0	Bypass mode enable for test clocks.
			0=Normal operation
			1=Bypass mode
			  0=Disable
			  1=Enable

MPLL_POWERDOWN_DLY	30:29	0x0	This register field is not used.
			  0=1 ms
			  1=2 ms
			  2=4 ms
			  3=8 ms

MPLL_POWERDOWN	31	0x0	Power-down Enable.
			0=Normal operation
			1=Power down
			  0=Run
			  1=Power Down

This register controls the Memory PLL. The divider fields will assume the default values based on power-on-strap options. To change the frequency, this register can be written by the CPU.			

MC_MPLL_CONTROL2 - RW - 32 bits - NBMCIND:0x75			
Field Name	**Bits**	**Default**	**Description**
MPLL_FBDIV	8:0	0x0	Comprises the 3-bit CMOS divider followed by the 6-bit CMOS divider. Bits [2:0] control the 3-bit CMOS divider and bits [8:3] control the 6-bit CMOS divider.
MPLL_REFDIV	13:9	0x0	Reference clock input divider ratio from 1 to 32.
MPLL_POSTDIV	15:14	0x0	Divide by 1/2/3/4 post divider ratio.
MPLL_CP	19:16	0x0	Charge-pump current setting.
MPLL_VCO_MODE	21:20	0x0	VCO mode setting
RESERVED	23:22	0x0	
MPLL_DLL_FRE_SEL	27:24	0x0	This register field is not used.
MPLL_LF_MODE	31:28	0x0	Loop filter mode setting.
This register controls the memory PLL frequency.			

<table>
<tr><th colspan="4">MC_MPLL_CONTROL3 - RW - 32 bits - NBMCIND:0x76</th></tr>
<tr><th>Field Name</th><th>Bits</th><th>Default</th><th>Description</th></tr>
<tr><td>MPLL_REF_DELAY</td><td>1:0</td><td>0x0</td><td>This register field is not used.</td></tr>
<tr><td>MPLL_VCO_DELAY</td><td>3:2</td><td>0x0</td><td>This register field is not used.</td></tr>
<tr><td>MPLL_CTL</td><td>8:4</td><td>0x0</td><td>Misc. PLL programming bits. IPLL_CTL[4] enables calibration override. When IPLL_CTL[4] = 0, the four calibration bits are set by the calibration loop. When IPLL_CTL[4]=1, the four bits are set through IPLL_CTL[3:0].</td></tr>
<tr><td>MPLL_IOBUFSEL</td><td>9</td><td>0x1</td><td>This register bit is not used.</td></tr>
<tr><td>MPLL_REFCLK_SEL</td><td>10</td><td>0x0</td><td>Reference clock input select. 0 chooses IREF_1X, 1 chooses ITCLK_1X</td></tr>
<tr><td>MPLL_BIAS</td><td>12:11</td><td>0x1</td><td>Bias current trim. IBIAS[1:0]. 00=-8%, 01=0%, 10=+12%, 11=+25%</td></tr>
<tr><td>MPLL_SPARE</td><td>27:13</td><td>0x0</td><td>Bit [4:0]=Spare pins reserved for PLL.
Bit [7:5]=Programmable current control for SCL for PLL.
000= -20%
001= -10%
010=0%
011=10%
100=20%
101=30%
110=40%
111=50%
Default=010
Bit [9:8]=Programmable current control for SCL for DLL.
00 = 0%
01=10%
10=20%
11=30%
Default=00</td></tr>
<tr><td>MPLL_MODE (R)</td><td>31:28</td><td>0x0</td><td>VCO operating mode status flags.</td></tr>
<tr><td colspan="4">This register controls the memory PLL.</td></tr>
</table>

<table>
<tr><th colspan="4">MC_MPLL_FREQ_CONTROL - RW - 32 bits - NBMCIND:0x77</th></tr>
<tr><th>Field Name</th><th>Bits</th><th>Default</th><th>Description</th></tr>
<tr><td>MPLL_PM_EN</td><td>0</td><td>0x0</td><td>Dynamic MCLK switch enable</td></tr>
<tr><td>MPLL_FREQ_SEL</td><td>1</td><td>0x0</td><td>0=Use normal MPLL registers to set memory frequency.
1=Use PM MPLL registers to set memory frequency</td></tr>
<tr><td>DISP_BLANK_CNTL</td><td>3:2</td><td>0x2</td><td>0=No blanking during frequency switch.
1=Blank assertion only.
2=Blank assertion and deassertion.
3=register control blank.</td></tr>
<tr><td>DISP_BLANK_VAL</td><td>4</td><td>0x0</td><td>Register control blank value.</td></tr>
<tr><td>MEM_SELF_REFRESH_ONLY</td><td>5</td><td>0x0</td><td>0=Self refresh is followed by frequency switching.
1=Self refresh only.</td></tr>
<tr><td>PM_SWITCHMCLK_BUSY (R)</td><td>6</td><td>0x0</td><td>0=MCLK is stable
1=MCLK switching is in progress</td></tr>
<tr><td>PM_FREQ_CNTL_RESET</td><td>7</td><td>0x0</td><td>Reset dynamic MCLK state machine</td></tr>
<tr><td>PM_MPLL_CP</td><td>11:8</td><td>0x0</td><td>PM mode Charge-pump current setting.</td></tr>
<tr><td>PM_MPLL_VCO_MODE</td><td>13:12</td><td>0x0</td><td>PM mode VCO mode setting</td></tr>
<tr><td>RESERVED14</td><td>15:14</td><td>0x0</td><td></td></tr>
<tr><td>PM_MPLL_LF_MODE</td><td>19:16</td><td>0x0</td><td>PM mode Loop filter mode setting.</td></tr>
<tr><td>PM_MPLL_DLL_FRE_SEL</td><td>23:20</td><td>0x0</td><td>This register field is not used.</td></tr>
</table>

RESERVED24	27:24	0x0	
MPLL_SLOWMCLK	28	0x0	0=MCLK is equal to or faster than CCLK in normal mode 1=MCLK is slower than CCLK in normal mode
PM_MPLL_SLOWMCLK	29	0x0	0=MCLK is equal to or faster than CCLK in PM mode 1=MCLK is slower than CCLK in PM mode
DLL_CORE_TEST_CLK	30	0x0	Bring it out on channel B CKE 3
RESERVED31	31	0x0	
Register Description.			

MC_MPLL_SEQ_CONTROL - RW - 32 bits - NBMCIND:0x78

Field Name	Bits	Default	Description
MPLL_RESET_PULSE_WIDTH	3:0	0x1	This register field is not used.
MDLL_RESET_PULSE_WIDTH	7:4	0x1	This register field is not used.
MPLL_CAL_S_TIME	11:8	0x4	VCO calibration setup time = MPLL_CAL_S_TIME * 512 * 10 ns
MPLL_CAL_H_TIME	15:12	0x5	VCO calibration hold time = MPLL_CAL_H_TIME * 4 * 10 ns
MPLL_LOCK_TIME	23:16	0x50	MPLL lock time = MPLL_LOCK_TIME * 256 * 10 ns
MDLL_LOCK_TIME	31:24	0x50	MDLL lock time = MDLL_LOCK_TIME * 256 * 10 ns
Register Description.			

MC_MPLL_DIV_CONTROL - RW - 32 bits - NBMCIND:0x79

Field Name	Bits	Default	Description
PM_MPLL_FBDIV	8:0	0x0	PM mode feedback divider
PM_MPLL_REFDIV	13:9	0x0	PM mode reference divider
PM_MPLL_POSTDIV	15:14	0x0	PM mode post divider

MPLL_DLL_CPP	17:16	0x0	Control charge pump source current,
			  0=Off
			  1=On

MPLL_DLL_CPN	19:18	0x0	Control charge pump sink current,
			  0=Off
			  1=On

MPLL_DLL_CPCAL_SEL	20	0x1	Select calibration or manual setting for charge pump current mirror.
			  0=Select manual setting
			  1=Select calibration setting

RESERVED	31:21	0x0	Bits [1:0]: Memory DLL reference clock skew control.
			Bits [3:2]: Memory DLL feedback clock skew control.
			Bit [4]:
			  1=Enable pre-clock tree PLL clock on MEMA ODT3 pad.
			Bit [5]:
			  1=Enable post-clock tree PLL clock on MEMA ODT2 pad.

Register Description.			

MC_MCLK_CONTROL - RW - 32 bits - NBMCIND:0x7A			
Field Name	**Bits**	**Default**	**Description**
CLKGATE_DIS_MCA	0	0x1	Disables clock gating for MCLK1X going to arbiterA and rbs
CLKGATE_DIS_MCB	1	0x1	Disables clock gating for MCLK1X going to arbiterB and rbs
CLKGATE_DIS_MCGR	2	0x1	Disables clock gating for MCLK1X going to cic interface
CLKGATE_DIS_MCSQA	3	0x1	Disables clock gating for MCLK1X going to sequencerA
CLKGATE_DIS_MCIOA	4	0x1	Disables clock gating for MCLK1X going to ioA
MC_DELAY_TIMER_EXTEND	5	0x0	Extend delay timer for MEMORY clocks 　0=16 clocks 　1=32 clocks
CLKGATE_DIS_LCLK_MC	6	0x1	Disables clock gating for LCLK_MC going to mc.
MPLL_DELAY	13:8	0x1	Interval of updating MPLL feedback divider.
SPARE0	23:16	0x0	Reserved.
DELAY_SET_MCLK	28:24	0xf	Extend delay timer for MCLK1X branches from 0 to 32 clocks.
CLKGATE_DIS_MC	29	0x1	
CLKGATE_DIS_MCIO	30	0x1	
Register Description.			

MC_UMA_HDR_LAT_INIT - RW - 32 bits - NBMCIND:0x7B			
Field Name	**Bits**	**Default**	**Description**
HDR_LAT_INIT_HDPW	15:0	0x20	Number of clocks to block HDP reads behind HDP writes before sending it down isochronous display pipe.
HDR_LAT_INIT_GFXW	31:16	0x20	Number of clocks to block HDP reads behind GFX writes before sending it down isochronous display pipe.

MC_UMA_GRP_CNTL - RW - 32 bits - NBMCIND:0x7C			
Field Name	**Bits**	**Default**	**Description**
GRP_BP_WM	2:0	0x7	There is a 16-entry CAM used for grouping requests, if the number of occupied entries exceeds GRP_BP_WM*2, all these entries will be marked as EJT and thus will be popped whenever they reach the bottom of the CAM and the status of the timer does not matter.
GRP_BP_RANGE	19:4	0xfffc	N/A
GRP_BP_ENABLE	20	0x1	N/A
GRP_DISABLE	21	0x0	1=Grouping function is disabled. 　0=Grouping function is enabled
GRP_GTW_EJECT	22	0x0	GTW requests are not grouped since no new request will be issued until response data is received. Since no grouping is done, it will be marked as EJT as soon as the request is entered into the CAM. GTW requests will go through grouping CAM if we disable DSP_GTW mode
GRP_PRI_EJECT	23	0x0	Priority lines from GTW or AGP are qualified with request valid signals and since these requests are priority, they are marked EJT and will not have to tolerate higher latency due to timer (not timing out yet) and will be popped out as soon as they fall to the bottom of the CAM.
GRP_URG_EJECT	24	0x0	All urgent lines are qualified with request valid signals and since these requests are urgent, they are marked EJT and will not have to tolerate higher latency due to timer (not timing out yet) and will be popped out as soon as they fall to the bottom of the CAM.

GRP_OPTS	31:25	0x0	xxxxxx1: If the new request finds a match with an entry not pointed to by the CAM read pointer, and even though this entry is marked as RDY, grouping will take place. xxxxx10: If the new request finds a match with an entry not pointed to by the CAM read pointer and even though this entry is marked as RDY and EJT, grouping will take place. xxxx1xx: With this bit set to 1'b1, the timer counts down every clock on condition that the next pipe stage is ready and the grouping FIFO does not have request to forward. With this bit set to 1'b0 the latency counter counts down every clock. xxx1xxx: All entries in the CAM will be ejected if the CAM becomes FULL. xx1xxxx: Mark all valid entries in CAM as EJT if the number of valid entries equal or exceed a pre-set watermark. x1xxxxx: Mark the entry as EJT if that entry is valid and not ready and is not doing the same (read/write) operation as the latest request.

MC_UMA_GRP_TMR - RW - 32 bits - NBMCIND:0x7D			
Field Name	Bits	Default	Description
GRP_RREQ_TMR_INIT	7:0	0x8	The maximum latency of a read request incurred by grouping.
GRP_WREQ_TMR_INIT	15:8	0x8	The maximum latency of a write request incurred by grouping.
GRP_TX_RREQ_TMR_INIT	23:16	0x8	The maximum latency of texture read request incurred by grouping.
SPARE0	31:24	0x0	Reserved.

MC_MISC_UMA_CNTL2 - RW - 32 bits - NBMCIND:0x7E			
Field Name	Bits	Default	Description
DISP_SLICE_COUNT	3:0	0x4	In this mode, high priority real-time requesters (display1, display2, overlay) will win consecutively for N times before switch to the next requester, where N is the register field. The order is display1, followed by display2, and followed by overlay.
SPARE0	7:4	0x0	Reserved
GFX_GTW_PRI	8	0x0	0=GFX GTW request will not be issued as priority 1=GFX GTW request will be issued to HT arbiter as priority
GFX_GTW_URG	9	0x0	0=GFX GTW request will not be issued as urgent 1=GFX GTW request will be issued to HT arbiter as urgent
GFX_FIXED_OVER_RRBIN	10	0x0	0=GFX Round-robbin arbitration scheme is chosen over fixed priority arbitration 1=GFX Fixed priority arbitration scheme is chosen over round-robbin arbitration
GFX_FIXED_PRI_SCHEM	14:12	0x0	0=GFX GTW will have priority over GFX 1=Reserved
DSP_GTW_PRI	15	0x0	0=DSP GTW request will not be issued as priority 1=DSP GTW request will be issued to HT arbiter as priority
DSP_GTW_URG	16	0x0	0=DSP GTW request will not be issued as urgent 1=DSP GTW request will be issued to HT arbiter as urgent

DSP_FIXED_OVER_RRBIN	17	0x0	0=DSP Round-robin arbitration scheme is chosen over fixed priority arbitration 1=DSP Fixed priority arbitration scheme is chosen over round-robbin arbitration
DSP_FIXED_PRI_SCHEM	21:19	0x0	0=DSP GTW will have priority over GFX 1=Reserved
UMA_SYNC_MODE	22	0x1	0=Asynchronous: MCLK ! = LCLK 1=Synchronous: MCLK = LCLK
LOCK_TO_2CYC	23	0x0	0=MC_GFX and MC_DSP streams can issue request to HTIU anytime 1=MC_GFX and MC_DSP streams' requests are locked to every other LCLK
UMA_EFF23	24	0x0	0=Original generation of EFF2 and EFF3 in UMA path 1=EFF2 and EFF3 are swapped in UMA path to allow read/write interleave

SPARE1	31:25	0x0	Bit [0]:
			  0=Bypass CurStTup2 double flop.
			  1=Do not bypass.
			Bit [1]:
			  0=Enable ECO for Rapid flush bug.
			  1=Disable ECO.
			Bit [2]:
			  0=Enable use of MCGART flush strobe in gtw.
			  1=Disable.
			Bit [3]:
			  0=Enable Flush ECO.
			  1=Disable Flush ECO.
			Bit [4]:
			  0=Gate off PmArbDis going into gart state machine.
			  1=Do not gate off PmArbDis.

MC_UMA_WC_GRP_TMR - RW - 32 bits - NBMCIND:0x80			
Field Name	**Bits**	**Default**	**Description**
GRP_G3D0W_TMR_INIT	7:0	0x8	The maximum latency of a G3D0W write request incurred by grouping.
GRP_G3D1W_TMR_INIT	15:8	0x8	The maximum latency of a G3D1W write request incurred by grouping.

MC_UMA_WC_GRP_CNTL - RW - 32 bits - NBMCIND:0x81			
Field Name	**Bits**	**Default**	**Description**
GRP_G3D0W_BP_WM	2:0	0x7	An 8-entry CAM is used for grouping G3D0W write requests. If the number of occupied entries exceeds GRP_G3D0W_BP_WM*2, then all of these entries will be marked as EJT (eject) and will therefore be ejected whenever they reach the bottom of the CAM, and the status of the timer does not matter.
GRP_G3D0W_URG_EJECT	3	0x0	1'b1: G3D0W urgent requests will be marked as EJT (eject), and will be ejected as soon as these marked entries hit the bottom of CAM FIFO. 1'b0:G3D0W urgent requests will not be marked as EJT(eject), and they are treated as normal requests.
GRP_G3D0W_GRP_ENABLE	4	0x0	1'b1: G3D0W write requests will be routed through the grouper and will be grouped. 1'b0: G3D0W requests will bypass the grouper.
GRP_G3D0W_OPTS	14:8	0x0	xxxxxx1: If the new G3D0W request finds a match with an entry not pointed to by the CAM read pointer, and even though this entry is marked as RDY, grouping will take place. xxxxx10: If the new G3D0W request finds a match with an entry not pointed to by the CAM read pointer, and even though this entry is marked as RDY and EJT, grouping will take place. xxxx1xx: If 1'b1, then the timer counts down every clock on the condition that the next pipe stage is ready and the grouping FIFO does not have request to forward. If 1'b0, then the latency counter counts down every clock. xxx1xxx: All entries in the CAM will be ejected if the CAM becomes FULL. xx1xxxx: Mark all valid entries in CAM as EJT (eject) if the number of valid entries equal or exceed a pre-set watermark. x1xxxxx: Mark the entry as EJT (eject) if that entry is valid, not ready, and is not doing the same (read/write) operation as the latest request.
GRP_G3D1W_BP_WM	18:16	0x7	An 8-entry CAM is used for grouping G3D1W write requests. If the number of occupied entries exceeds GRP_G3D1W_BP_WM*2, then all these entries will be marked as EJT (eject), and will therefore be ejected whenever they reach the bottom of the CAM, and the status of the timer does not matter.
GRP_G3D1W_URG_EJECT	20	0x0	1'b1: G3D1W urgent requests will be marked as EJT (eject), and will be ejected as soon as these marked entries hit the bottom of CAM FIFO. 1'b0: G3D0W urgent requests will not be marked as EJT(eject), and they are treated as normal requests

GRP_G3D1W_OPTS	30:24	0x0	xxxxxx1: If the new G3D1W request finds a match with an entry not pointed to by the CAM read pointer, and even though this entry is marked as RDY, grouping will take place. xxxxx10: If the new G3D1W request finds a match with an entry not pointed to by the CAM read pointer, and even though this entry is marked as RDY and EJT, grouping will take place. xxxx1xx: If 1'b1, then the timer counts down every clock on the condition that the next pipe stage is ready and the grouping FIFO does not have request to forward. If 1'b0, then the latency counter counts down every clock. xxx1xxx: All entries in the CAM will be ejected if the CAM becomes FULL. xx1xxxx: Mark all valid entries in CAM as EJT (eject) if the number of valid entries equal or exceed a pre-set watermark. x1xxxxx: Mark the entry as EJT (eject) if that entry is valid, not ready, and is not doing the same (read/write) operation as the latest request.
GRP_G3D1W_GRP_ENABLE	31	0x0	1'b1: G3D1W write requests will be routed through the grouper and will be grouped. 1'b0: G3D1W requests will bypass the grouper.

MC_UMA_RW_GRP_TMR - RW - 32 bits - NBMCIND:0x82			
Field Name	**Bits**	**Default**	**Description**
GRP_G3D0R_TMR_INIT	7:0	0x8	The maximum latency of a G3D0R read request incurred by grouping.
GRP_G3D1R_TMR_INIT	15:8	0x8	The maximum latency of a G3D1R read request incurred by grouping.
GRP_GTX0R_TMR_INIT	23:16	0x8	The maximum latency of a GTX0R read request incurred by grouping.
GRP_E2R_TMR_INIT	31:24	0x8	The maximum latency of a E2R read request incurred by grouping.

MC_UMA_RW_G3DR_GRP_CNTL - RW - 32 bits - NBMCIND:0x83			
Field Name	**Bits**	**Default**	**Description**
GRP_G3D0R_BP_WM	2:0	0x7	An 8-entry CAM is used for grouping G3D0R write requests. If the number of occupied entries exceeds GRP_G3D0R_BP_WM*2, then all of these entries will be marked as EJT (eject), and will therefore be ejected whenever they reach the bottom of the CAM, and the status of the timer does not matter.
GRP_G3D0R_URG_EJECT	3	0x0	This bit is reserved.
GRP_G3D0R_GRP_ENABLE	4	0x0	1'b1: G3D0R write requests will be routed through the grouper and will be grouped. 1'b0: G3D0R requests will bypass the grouper.

GRP_G3D0R_OPTS	14:8	0x0	xxxxxx1: If the new G3D0R request finds a match with an entry not pointed to by the CAM read pointer, and even though this entry is marked as RDY, grouping will take place. xxxxx10: If the new G3D0R request finds a match with an entry not pointed to by the CAM read pointer, and even though this entry is marked as RDY and EJT, grouping will take place. xxxx1xx: If 1'b1, then the timer counts down every clock on the condition that the next pipe stage is ready and the grouping FIFO does not have request to forward. If 1'b0, then the latency counter counts down every clock. xxx1xxx: All entries in the CAM will be ejected if the CAM becomes FULL. xx1xxxx: Mark all valid entries in CAM as EJT (eject) if the number of valid entries equal or exceed a pre-set watermark. x1xxxxx: Mark the entry as EJT (eject) if that entry is valid, not ready, and is not doing the same (read/write) operation as the latest request.
GRP_G3D1R_BP_WM	18:16	0x7	An 8-entry CAM is used for grouping G3D1R write requests. If the number of occupied entries exceeds GRP_G3D1R_BP_WM*2, then all of these entries will be marked as EJT (eject), and will therefore be ejected whenever they reach the bottom of the CAM, and the status of the timer does not matter.
GRP_G3D1R_URG_EJECT	20	0x0	This bit is reserved.
GRP_G3D1R_OPTS	30:24	0x0	xxxxxx1: If the new G3D1R request finds a match with an entry not pointed to by the CAM read pointer, and even though this entry is marked as RDY, grouping will take place. xxxxx10: If the new G3D1R request finds a match with an entry not pointed to by the CAM read pointer, and even though this entry is marked as RDY and EJT, grouping will take place. xxxx1xx: If 1'b1, then the timer counts down every clock on the condition that the next pipe stage is ready and the grouping FIFO does not have request to forward. If 1'b0, then the latency counter counts down every clock. xxx1xxx: All entries in the CAM will be ejected if the CAM becomes FULL. xx1xxxx: Mark all valid entries in CAM as EJT (eject) if the number of valid entries equal or exceed a pre-set watermark. x1xxxxx: Mark the entry as EJT (eject) if that entry is valid, not ready, and is not doing the same (read/write) operation as the latest request.
GRP_G3D1R_GRP_ENABLE	31	0x0	1'b1: G3D1R write requests will be routed through the grouper and will be grouped. 1'b0: G3D1R requests will bypass the grouper.

MC_UMA_RW_TXR_E2R_GRP_CNTL - RW - 32 bits - NBMCIND:0x84			
Field Name	**Bits**	**Default**	**Description**
GRP_GTX0R_BP_WM	2:0	0x7	An 8-entry CAM is used for grouping GTX0R write requests. If the number of occupied entries exceeds GRP_GTX0R_BP_WM*2, then all of these entries will be marked as EJT (eject) and will therefore be ejected whenever they reach the bottom of the CAM, and the status of the timer does not matter.
GRP_GTX0R_URG_EJECT	3	0x0	This bit is reserved.
GRP_GTX0R_GRP_ENABLE	4	0x0	1'b1: GTX0R write requests will be routed through the grouper and will be grouped. 1'b0: GTX0R requests will bypass the grouper.
GRP_GTX0R_OPTS	14:8	0x0	xxxxxx1: If the new GTX0R request finds a match with an entry not pointed to by the CAM read pointer, and even though this entry is marked as RDY, grouping will take place. xxxxx10: If the new GTX0R request finds a match with an entry not pointed to by the CAM read pointer, and even though this entry is marked as RDY and EJT (eject), grouping will take place. xxxx1xx: If 1'b1, then the timer counts down every clock on the condition that the next pipe stage is ready and the grouping FIFO does not have request to forward. If 1'b0, then the latency counter counts down every clock. xxx1xxx: All entries in the CAM will be ejected if the CAM becomes FULL. xx1xxxx: Mark all valid entries in CAM as EJT (eject) if the number of valid entries equal or exceed a pre-set watermark. x1xxxxx: Mark the entry as EJT (eject) if that entry is valid, not ready, and is not doing the same (read/write) operation as the latest request.
GRP_E2R_BP_WM	18:16	0x7	An 8-entry CAM is used for grouping E2R write requests. If the number of occupied entries exceeds GRP_E2R_BP_WM*2, then all of these entries will be marked as EJT (eject) and will therefore be ejected whenever they reach the bottom of the CAM, and the status of the timer does not matter.
GRP_E2R_URG_EJECT	20	0x0	1'b1: E2R urgent and priority requests will be marked as EJT (eject) and will be ejected as soon as these marked entries hit the bottom of CAM FIFO. 1'b0: E2R urgent and priority requests will not be marked as EJT(eject) and they are treated as normal requests

GRP_E2R_OPTS	30:24	0x0	xxxxxx1: If the new E2R request finds a match with an entry not pointed to by the CAM read pointer, and even though this entry is marked as RDY, grouping will take place. xxxxx10: If the new E2R request finds a match with an entry not pointed to by the CAM read pointer, and even though this entry is marked as RDY and EJT (eject), grouping will take place. xxxx1xx: If 1'b1, then the timer counts down every clock on the condition that the next pipe stage is ready and the grouping FIFO does not have request to forward. If 1'b0, then the latency counter counts down every clock. xxx1xxx: All entries in the CAM will be ejected if the CAM becomes FULL. xx1xxxx: Mark all valid entries in CAM as EJT (eject) if the number of valid entries equal or exceed a pre-set watermark. x1xxxxx: Mark the entry as EJT (eject) if that entry is valid, not ready, and is not doing the same (read/write) operation as the latest request.
GRP_E2R_GRP_ENABLE	31	0x0	1'b1: E2R write requests will be routed through the grouper and will be grouped. 1'b0: E2R requests will bypass the grouper.

MC_UMA_AGP_GRP_CNTL - RW - 32 bits - NBMCIND:0x85			
Field Name	**Bits**	**Default**	**Description**
GRP_AGP_BP_WM	2:0	0x7	An 8-entry CAM is used for grouping AGP write requests. If the number of occupied entries exceeds GRP_AGP_BP_WM*2, then all of these entries will be marked as EJT (eject) and will therefore be ejected whenever they reach the bottom of the CAM, and the status of the timer does not matter.
GRP_AGP_URG_EJECT	3	0x0	1'b1: AGP urgent and priority requests will be marked as EJT (eject) and will be ejected as soon as these marked entries hit the bottom of CAM FIFO. 1'b0: AGP urgent and priority requests will not be marked as EJT(eject) and they are treated as normal requests
GRP_AGP_GRP_ENABLE	4	0x0	1'b1: AGP write requests will be routed through the grouper and will be grouped. 1'b0: AGP requests will bypass the grouper.

GRP_AGP_OPTS	14:8	0x0	xxxxxx1: If the new AGP request finds a match with an entry not pointed to by the CAM read pointer, and even though this entry is marked as RDY, grouping will take place. xxxxx10: If the new AGP request finds a match with an entry not pointed to by the CAM read pointer, and even though this entry is marked as RDY and EJT (eject), grouping will take place. xxxx1xx: If 1'b1, then the timer counts down every clock on the condition that the next pipe stage is ready and the grouping FIFO does not have request to forward. If 1'b0, then the latency counter counts down every clock. xxx1xxx: All entries in the CAM will be ejected if the CAM becomes FULL. xx1xxxx: Mark all valid entries in CAM as EJT (eject) if the number of valid entries equal or exceed a pre-set watermark. x1xxxxx: Mark the entry as EJT (eject) if that entry is valid, not ready, and is not doing the same (read/write) operation as the latest request.
GRP_AGP_TMR_INIT	23:16	0x8	The maximum latency of a AGP read request incurred by grouping.

MC_UMA_DUALCH_CNTL - RW - 32 bits - NBMCIND:0x86			
Field Name	**Bits**	**Default**	**Description**
DUAL_CHANNEL_EN	0	0x0	1'b1: Enables write-channel path. All G3D0W and G3D1W requests will be forwarded to this path, and all other client requests will be forwarded to the default UMA path. 1'b0: All requests will be forwarded to the default UMA path.
IO_ORDER_TAG_EN	1	0x0	1'b1: Requests from both the write-channel path and the UMA path will be tagged before being forwarded to the HTIU interface. These request order tags provide the IO order for the HTIU arbiter. 1'b0: No tagging will be done, and the request order tags will be ignored by the HTIU arbiter.
IO_ORDER_WCH_WACK_EN	2	0x0	1'b1: HTIU will return the WACK signals after arbitrating IDCTW or HDPW requests to MC. MC keeps track of how many HDPW or IDCTW are not committed yet. 1'b0: HTIU does not return the WACK signal to the dedicated write port.
IO_ORDER_RWCH_WACK_EN	3	0x0	1'b1: HTIU returns WACK signal (for each write-channel path request committed to the link) to MC. If 1'b0, then MC ignores the WACK signal. 1'b0: HTIU does not return the WACK signal to the (RW) graphics port.
R1C_W2X_EN	4	0x0	1'b1: Read requests will be forwarded every clock cycle at the MC/HTIU interface, and a 32 byte write request will be forwarded every clock. 1'b0: Revert back to 2 clocks for each read and write request.

| ASYNC_FIFO_BYPASS | 5 | 0x0 | 1'b1: All new mode switching bits will be loaded and take effect immediately.
1'b0: All new mode switching bits will be loaded upon seeing internal mc_idle signal.
The new mode switches are as follows:
DUAL_CHANNEL_EN, IO_ORDER_TAG_EN, IO_ORDER_WCH_WACK_EN, IO_ORDER_RWCH_WACK_EN, R1C_W2X_EN, and all client interface GRP_ENABLEs. |

NB_MEM_CH_CNTL2 - RW - 32 bits - NBMCIND:0x1B			
Field Name	**Bits**	**Default**	**Description**
K8_INTERLEAVE_SIZE	7:0	0x0	This field is to specify the interleave size of FB on the UMA side. The unit is 1Mbyte.
Memory Control channel register2			

NB_MEM_CH_CNTL0 - RW - 32 bits - NBMCIND:0x1C			
Field Name	**Bits**	**Default**	**Description**

INTERLEAVE_MODE	1:0	0x0	This field defines the interleave mode between memory channels. In 'Coarse interleaved' mode the primary channel, which is SP, occupies the lower part of system memory address space. In 'Interleaved' mode memory access alternates between both channels (every 128 bytes or 256 bytes).
			  0=Single Channel
			  1=Fine Interleaved
			  2=Reserved
			  3=Coarse Interleaved

PRIMARY_CHANNEL	2	0x1	The primary channel will be SP always under dual-channel configuration. The only case that UMA would be the primary channel is under the UMA-only configuration. The memory controller uses that information to properly interleave accesses between channels.
			  0=Channel A
			  1=Channel B

NUMBER_CHANNEL	3	0x0	This specifies single/dual memory channel mode
			  0=One channel
			  1=Two channels

BANK_2_MAP	7:4	0x6	Memory bank bit 2 mapping, address bits 7 to 20 can be used, for values being 0 to 13. The default value is 6 meaning address bit 13 is used as bank[0]
BANK_0_MAP	15:12	0x4	Memory bank bit 0 mapping, address bits 7 to 20 can be used, for values being 0 to 13. The default value is 4 meaning address bit 11 is used as bank[0]
BANK_1_MAP	19:16	0x5	Memory bank bit 1 mapping, address bits 7 to 20 can be used, for values being 0 to 13. The default value is 5 meaning address bit 12 is used as bank[1]
INTERLEAVE_START	31:20	0x0	The address space below Interleave-Start will be mapped to the Primary-Channel and will be treated as if operating in single channel mode.
Memory Control channel register0			

NB_MEM_CH_CNTL1 - RW - 32 bits - NBMCIND:0x1D			
Field Name	**Bits**	**Default**	**Description**
INTERLEAVE_END	11:0	0x0	The address space above Interleave-End will be mapped to the Secondary-Channel, which is UMA, and will be treated as if operating in single channel mode.
INTERLEAVE_RATIO	19:12	0xaa	This 8-bit register defines the ratio of arbitration between SP and UMA. 0 means that SP will win the arbitration and 1 means that UMA will win the arbitration. For example, the value 11100000 will have SP being selected for 5 consecutive times and UMA being selected for the rest of the three times.

INTERLEAVE_PAGE_SIZE	28	0x0	Every 128 bytes or 256 bytes, the channel select logic will be activated and re-map the FB requests between two channels. It will only take effect under the dual-channel configuration.
			  0=128 bytes
			  1=256 bytes

Memory Control channel register1			

MC_MISC_CNTL3 - RW - 32 bits - NBMCIND:0x4F			
Field Name	**Bits**	**Default**	**Description**
GFXR_LAT	7:0	0x2	Valid range is 0x1 to 0x7E
GTXR_LAT	15:8	0x2	Valid range is 0x1 to 0x7E
GFXW_LAT	23:16	0x2	Valid range is 0x1 to 0x7E
GFXR_NOWAIT_MODE	24	0x0	
GTXR_NOWAIT_MODE	25	0x0	
GFXW_NOWAIT_MODE	26	0x0	
Miscellaneous controls(3) for memory controller			

MC_UMA_WC_GRP_TMR - RW - 32 bits - NBMCIND:0x80			
Field Name	**Bits**	**Default**	**Description**
GRP_G3D0W_TMR_INIT	7:0	0x8	The maximum latency of a G3D0W write request incurred by grouping
GRP_G3D1W_TMR_INIT	15:8	0x8	The maximum latency of a G3D1W write request incurred by grouping

MC_UMA_WC_GRP_CNTL - RW - 32 bits - NBMCIND:0x81			
Field Name	**Bits**	**Default**	**Description**
GRP_G3D0W_BP_WM	2:0	0x7	A 8-entry CAM is used for grouping G3D0W write requests, if the number of occupied entries exceeds GRP_G3D0W_BP_WM*2, all these entries will be marked as EJT and thus will be ejected whenever they reach the bottom of the CAM and the status of the timer does not matter.
GRP_G3D0W_URG_EJECT	3	0x0	1'b1: G3D0W urgent requests will be marked as EJT (eject) and will be ejected as soon as these marked entries hit the bottom of CAM FIFO. 1'b0:G3D0W urgent requests will not be marked as EJT(eject) and they are treated as normal requests
GRP_G3D0W_GRP_ENABLE	4	0x0	1'b1: G3D0W write requests will be routed through the grouper and will be grouped. 1'b0: G3D0W requests will bypass the grouper.
GRP_G3D0W_OPTS	14:8	0x0	xxxxxx1: If the new G3D0W request finds a match with an entry not pointed to by the CAM read pointer, and even though this entry is marked as RDY, grouping will take place. xxxxx10: If the new G3D0W request finds a match with an entry not pointed to by the CAM read pointer and even though this entry is marked as RDY and EJT, grouping will take place. xxxx1xx: If 1'b1, the timer counts down every clock on condition that the next pipe stage is ready and the grouping FIFO does not have request to forward. If 1'b0 the latency counter counts down every clock. xxx1xxx: All entries in the CAM will be ejected if the CAM becomes FULL. xx1xxxx: Mark all valid entries in CAM as EJT if the number of valid entries equal or exceed a pre-set watermark. x1xxxxx: Mark the entry as EJT if that entry is valid and not ready and is not doing the same (read/write) operation as the latest request.
GRP_G3D1W_BP_WM	18:16	0x7	A 8-entry CAM is used for grouping G3D1W write requests, if the number of occupied entries exceeds GRP_G3D1W_BP_WM*2, all these entries will be marked as EJT and thus will be ejected whenever they reach the bottom of the CAM and the status of the timer does not matter.
GRP_G3D1W_URG_EJECT	20	0x0	1'b1: G3D1W urgent requests will be marked as EJT (eject) and will be ejected as soon as these marked entries hit the bottom of CAM FIFO. 1'b0: G3D0W urgent requests will not be marked as EJT(eject) and they are treated as normal requests.

| GRP_G3D1W_OPTS | 30:24 | 0x0 | xxxxxx1: If the new G3D1W request finds a match with an entry not pointed to by the CAM read pointer, and even though this entry is marked as RDY, grouping will take place.
xxxxx10: If the new G3D1W request finds a match with an entry not pointed to by the CAM read pointer and even though this entry is marked as RDY and EJT, grouping will take place.
xxxx1xx: If 1'b1, the timer counts down every clock on condition that the next pipe stage is ready and the grouping FIFO does not have request to forward. If 1'b0 the latency counter counts down every clock.
xxx1xxx: All entries in the CAM will be ejected if the CAM becomes FULL.
xx1xxxx: Mark all valid entries in CAM as EJT if the number of valid entries equal or exceed a pre-set watermark.
x1xxxxx: Mark the entry as EJT if that entry is valid and not ready and is not doing the same (read/write) operation as the latest request. |
| GRP_G3D1W_GRP_ENABLE | 31 | 0x0 | 1'b1: G3D1W write requests will be routed through the grouper and will be grouped.
1'b0: G3D1W requests will bypass the grouper. |

MC_UMA_RW_GRP_TMR - RW - 32 bits - NBMCIND:0x82

Field Name	Bits	Default	Description
GRP_G3D0R_TMR_INIT	7:0	0x8	The maximum latency of a G3D0R read request incurred by grouping
GRP_G3D1R_TMR_INIT	15:8	0x8	The maximum latency of a G3D1R read request incurred by grouping
GRP_GTX0R_TMR_INIT	23:16	0x8	The maximum latency of a GTX0R read request incurred by grouping
GRP_E2R_TMR_INIT	31:24	0x8	The maximum latency of a E2R read request incurred by grouping

MC_UMA_RW_G3DR_GRP_CNTL - RW - 32 bits - NBMCIND:0x83			
Field Name	**Bits**	**Default**	**Description**
GRP_G3D0R_BP_WM	2:0	0x7	A 8-entry CAM is used for grouping G3D0R write requests, if the number of occupied entries exceeds GRP_G3D0R_BP_WM*2, all these entries will be marked as EJT and thus will be ejected whenever they reach the bottom of the CAM and the status of the timer does not matter.
GRP_G3D0R_URG_EJECT	3	0x0	Reserved
GRP_G3D0R_GRP_ENABLE	4	0x0	1'b1: G3D0R write requests will be routed through the grouper and will be grouped. 1'b0: G3D0R requests will bypass the grouper.
GRP_G3D0R_OPTS	14:8	0x0	xxxxxx1: If the new G3D0R request finds a match with an entry not pointed to by the CAM read pointer, and even though this entry is marked as RDY, grouping will take place. xxxxx10: If the new G3D0R request finds a match with an entry not pointed to by the CAM read pointer and even though this entry is marked as RDY and EJT, grouping will take place. xxxx1xx: If 1'b1, the timer counts down every clock on condition that the next pipe stage is ready and the grouping FIFO does not have request to forward. If 1'b0 the latency counter counts down every clock. xxx1xxx: All entries in the CAM will be ejected if the CAM becomes FULL. xx1xxxx: Mark all valid entries in CAM as EJT if the number of valid entries equal or exceed a pre-set watermark. x1xxxxx: Mark the entry as EJT if that entry is valid and not ready and is not doing the same (read/write) operation as the latest request.
GRP_G3D1R_BP_WM	18:16	0x7	A 8-entry CAM is used for grouping G3D1R write requests, if the number of occupied entries exceeds GRP_G3D1R_BP_WM*2, all these entries will be marked as EJT and thus will be ejected whenever they reach the bottom of the CAM and the status of the timer does not matter.
GRP_G3D1R_URG_EJECT	20	0x0	Reserved

GRP_G3D1R_OPTS	30:24	0x0	xxxxxx1: If the new G3D1R request finds a match with an entry not pointed to by the CAM read pointer, and even though this entry is marked as RDY, grouping will take place. xxxxx10: If the new G3D1R request finds a match with an entry not pointed to by the CAM read pointer and even though this entry is marked as RDY and EJT, grouping will take place. xxxx1xx: If 1'b1, the timer counts down every clock on condition that the next pipe stage is ready and the grouping FIFO does not have request to forward. If 1'b0 the latency counter counts down every clock. xxx1xxx: All entries in the CAM will be ejected if the CAM becomes FULL. xx1xxxx: Mark all valid entries in CAM as EJT if the number of valid entries equal or exceed a pre-set watermark. x1xxxxx: Mark the entry as EJT if that entry is valid and not ready and is not doing the same (read/write) operation as the latest request.
GRP_G3D1R_GRP_ENABLE	31	0x0	1'b1: G3D1R write requests will be routed through the grouper and will be grouped. 1'b0: G3D1R requests will bypass the grouper.

MC_UMA_RW_TXR_E2R_GRP_CNTL - RW - 32 bits - NBMCIND:0x84			
Field Name	**Bits**	**Default**	**Description**
GRP_GTX0R_BP_WM	2:0	0x7	A 8-entry CAM is used for grouping GTX0R write requests, if the number of occupied entries exceeds GRP_GTX0R_BP_WM*2, all these entries will be marked as EJT and thus will be ejected whenever they reach the bottom of the CAM and the status of the timer does not matter.
GRP_GTX0R_URG_EJECT	3	0x0	Reserved
GRP_GTX0R_GRP_ENABLE	4	0x0	1'b1: GTX0R write requests will be routed through the grouper and will be grouped. 1'b0: GTX0R requests will bypass the grouper.
GRP_GTX0R_OPTS	14:8	0x0	xxxxxx1: If the new GTX0R request finds a match with an entry not pointed to by the CAM read pointer, and even though this entry is marked as RDY, grouping will take place. xxxxx10: If the new GTX0R request finds a match with an entry not pointed to by the CAM read pointer and even though this entry is marked as RDY and EJT, grouping will take place. xxxx1xx: If 1'b1, the timer counts down every clock on condition that the next pipe stage is ready and the grouping FIFO does not have request to forward. If 1'b0 the latency counter counts down every clock. xxx1xxx: All entries in the CAM will be ejected if the CAM becomes FULL. xx1xxxx: Mark all valid entries in CAM as EJT if the number of valid entries equal or exceed a pre-set watermark. x1xxxxx: Mark the entry as EJT if that entry is valid and not ready and is not doing the same (read/write) operation as the latest request.
GRP_E2R_BP_WM	18:16	0x7	A 8-entry CAM is used for grouping E2R write requests, if the number of occupied entries exceeds GRP_E2R_BP_WM*2, all these entries will be marked as EJT and thus will be ejected whenever they reach the bottom of the CAM and the status of the timer does not matter.
GRP_E2R_URG_EJECT	20	0x0	1'b1: E2R urgent and priority requests will be marked as EJT (eject) and will be ejected as soon as these marked entries hit the bottom of CAM FIFO. 1'b0: E2R urgent and priority requests will not be marked as EJT(eject) and they are treated as normal requests

GRP_E2R_OPTS	30:24	0x0	xxxxxx1: If the new E2R request finds a match with an entry not pointed to by the CAM read pointer, and even though this entry is marked as RDY, grouping will take place. xxxxx10: If the new E2R request finds a match with an entry not pointed to by the CAM read pointer and even though this entry is marked as RDY and EJT, grouping will take place. xxxx1xx: If 1'b1, the timer counts down every clock on condition that the next pipe stage is ready and the grouping FIFO does not have request to forward. If 1'b0 the latency counter counts down every clock. xxx1xxx: All entries in the CAM will be ejected if the CAM becomes FULL. xx1xxxx: Mark all valid entries in CAM as EJT if the number of valid entries equal or exceed a pre-set watermark. x1xxxxx: Mark the entry as EJT if that entry is valid and not ready and is not doing the same (read/write) operation as the latest request.
GRP_E2R_GRP_ENABLE	31	0x0	1'b1: E2R write requests will be routed through the grouper and will be grouped. 1'b0: E2R requests will bypass the grouper.

MC_UMA_AGP_GRP_CNTL - RW - 32 bits - NBMCIND:0x85			
Field Name	**Bits**	**Default**	**Description**
GRP_AGP_BP_WM	2:0	0x7	A 8-entry CAM is used for grouping AGP write requests, if the number of occupied entries exceeds GRP_AGP_BP_WM*2, all these entries will be marked as EJT and thus will be ejected whenever they reach the bottom of the CAM and the status of the timer does not matter.
GRP_AGP_URG_EJECT	3	0x0	1'b1: AGP urgent and priority requests will be marked as EJT (eject) and will be ejected as soon as these marked entries hit the bottom of CAM FIFO. 1'b0: AGP urgent and priority requests will not be marked as EJT(eject) and they are treated as normal requests
GRP_AGP_GRP_ENABLE	4	0x0	1'b1: AGP write requests will be routed through the grouper and will be grouped. 1'b0: AGP requests will bypass the grouper.
GRP_AGP_OPTS	14:8	0x0	xxxxxx1: If the new AGP request finds a match with an entry not pointed to by the CAM read pointer, and even though this entry is marked as RDY, grouping will take place. xxxxx10: If the new AGP request finds a match with an entry not pointed to by the CAM read pointer and even though this entry is marked as RDY and EJT, grouping will take place. xxxx1xx: If 1'b1, the timer counts down every clock on condition that the next pipe stage is ready and the grouping FIFO does not have request to forward. If 1'b0 the latency counter counts down every clock. xxx1xxx: All entries in the CAM will be ejected if the CAM becomes FULL. xx1xxxx: Mark all valid entries in CAM as EJT if the number of valid entries equal or exceed a pre-set watermark. x1xxxxx: Mark the entry as EJT if that entry is valid and not ready and is not doing the same (read/write) operation as the latest request.
GRP_AGP_TMR_INIT	23:16	0x8	The maximum latency of a AGP read request incurred by grouping.

MC_UMA_DUALCH_CNTL - RW - 32 bits - NBMCIND:0x86			
Field Name	**Bits**	**Default**	**Description**
DUAL_CHANNEL_EN	0	0x0	1'b1: enable write-channel path, all G3D0W and G3D1W requests will be forwarded to this path, and all other clients' requests will be forwarded to the default UMA path. 1'b0: all requests will be forwarded to the default UMA path.
IO_ORDER_TAG_EN	1	0x0	1'b1: requests from both write-channel path and UMA path will be tagged before being forwarded to HTIU interface, these requests order tags provide the IO order for HTIU arbiter. 1'b0: no tagging will be done and the request order tags will be ignored by HTIU arbiter.
IO_ORDER_WCH_WACK_EN	2	0x0	1'b1: HTIU will return WACK signals after arbitrating IDCTW or HDPW requests to MC. MC keeps track of how many HDPW or IDCTW are not committed yet. 1'b0: HTIU does not return WACK signal to dedicated write port
IO_ORDER_RWCH_WACK_EN	3	0x0	1'b1: HTIU returns WACK signal (for each write-channel path request committed to the link) to MC. If 1'b0, MC ignores the WACK signal. 1'b0: HTIU does not return WACK signal to (RW) graphics port
R1C_W2X_EN	4	0x0	1'b1: read requests will be forwarded every clock cycle at the MC/HTIU interface, and a 32 bytes write request will be forwarded every clock. 1'b0: revert back to 2 clocks for each read and write request.
ASYNC_FIFO_BYPASS	5	0x0	Original intent was to use this bit to bypass some async FIFO.But it's now used differently. 1'b1: all new mode switching bits will be loaded and take effect immediately. 1'b0: all new mode switching bits will be loaded upon seeing internal mc_idle signal. The new mode switches are: DUAL_CHANNEL_EN, IO_ORDER_TAG_EN, IO_ORDER_WCH_WACK_EN, IO_ORDER_RWCH_WACK_EN, R1C_W2X_EN and all client interface GRP_ENABLE/s

MC_SYSTEM_STATUS - RW - 32 bits - NBMCIND:0x90			
Field Name	**Bits**	**Default**	**Description**
MC_SYSTEM_IDLE (R)	0	0x0	Indicates that there are no pending or in-process memory requests. This includes all pending or in-process requests to system memory. 　0=Not Idle 　1=Idle
MC_SEQUENCER_IDLE (R)	1	0x0	Indicates that there are no pending or in-process frame buffer requests. Does not include status on pending or in-process requests to system memory. 　0=Not Idle 　1=Idle
MC_ARBITER_IDLE (R)	2	0x0	Indicates that there are no pending or in-process frame buffer requests. Does not include status on pending or in-process requests to system memory. 　0=Not Idle 　1=Idle
MC_SELECT_PM (R)	3	0x0	Memory power management selection read back
RESERVED4 (R)	7:4	0x0	
RESERVED8 (R)	11:8	0x0	
RESERVED12 (R)	15:12	0x0	
MCA_INIT_EXECUTED (R)	16	0x0	Channel A SDRAM Init in Process: Indicates that the last MCA_INIT_EXECUTE operation has completed for the A channel. Do not initiate a new MCA_INIT_EXECUTE operation until 'Ready' is indicated. 　0=SDRAM Init in Process 　1=Ready
MCA_IDLE (R)	17	0x0	Channel A memory controller idle. 　0=Not idle 　1=Idle
MCA_SEQ_IDLE (R)	18	0x0	Channel A memory controller sequencer idle. 　0=Not Idle 　1=Idle
MCA_ARB_IDLE (R)	19	0x0	Channel A memory controller arbiter idle. 　0=Not Idle 　1=Idle
RESERVED20 (R)	31:20	0x0	
Memory controller system status			

MC_INTFC_GENERAL_PURPOSE - RW - 32 bits - NBMCIND:0x91			
Field Name	**Bits**	**Default**	**Description**
MC_STARTUP	0	0x0	Setting this bit forces the MC's SDRAM mode state machine from the initial power-on state into the 'operating' state. This bit needs to be set after initial power up, before the system memory can be accessed.
MC_RESTART	1	0x0	Setting this bit forces the MC's SDRAM mode state machine from the initial power-on state into the 'parked' state. This bit needs to be set after initial power up if the SDRAM is in self-refresh mode after a 'suspend-to-RAM' operation. After the mode state machine has reached the 'parked' state, the memory will be taken out of 'self-refresh' as soon as the hardware signal DC_STOP has been deasserted and the state machine will transition into the 'operating' state.
MC_POWERED_UP	2	0x0	All clocks ready. This bit must be set on power up after initializing all clocks in order to proceed with MC initialization. When 0, force CKE low, and tristate all other signals.
MC_POWERED_UP2	3	0x0	All clocks ready. This bit must be set after power up, on self refresh exit, after initializing all clocks in order to proceed with MC initialization. When 0, force CKE low, and tristate all other signals.

MC_PWRDN_MODE	5:4	0x0	Selects the source for the power down event
			    0=DC_STOP/SUSTAT
			    1=CPU Special Cycle (AMD)
			    2=Both
			    3=None

MC_POWER_DOWN	6	0x0	Setting this bit forces the MC's SDRAM mode state machine from the 'operating' state into the 'parked' state. The parking sequence takes a certain time and the processor needs to monitor the state machine to make sure that the 'parked' state has been reached before the power to the NB core is removed.
MC_GFX_PWRDN_ENABLE	7	0x0	Enables power down for external graphics

MC_SUSPEND_DISABLE	8	0x0	This bit disables suspend
			    0=Suspend enabled
			    1=Suspend disabled

MC_SUSPEND_TRISTATE	9	0x1	This bit enables tristate in suspend
			    0=Do not tristate in suspend
			    1=Tristate in suspend

MC_SUSPEND_CLEAN_MC	10	0x0	When going to suspend, clean MC, no stuck requests in MC.
MC_SUSPEND_DYNAMIC	11	0x0	Dynamic self refresh when cpu in s3 and display in shutter mode.
MC_SUSPEND_DELAY	15:12	0x8	Delay to enter self refresh when cpu in s3 and display in shutter mode, x4 clocks.
RESERVED16	19:16	0x0	
MC_TCLKS	23:20	0x1	Memory clock settling time - memory spec - register x16 clocks.
MC_TDLLR	27:24	0x8	DLL reset pulse - 1us - register x64 clocks.
MC_TDLLL	31:28	0x8	DLL lock time - 500 clock - register x64 clocks.
Memory controller general purpose register			

MC_INTFC_IMP_CTRL_CNTL - RW - 32 bits - NBMCIND:0x92			
Field Name	**Bits**	**Default**	**Description**
MC_IC_UPDATE_RATE	4:0	0x18	Update rate MCLK*2**n 0x0=Minimum 0x1F=Maximum
RESERVED5	7:5	0x0	
MC_IC_SAMPLE_RATE	12:8	0x10	Sample rate MCLK*2**n 0x0=Minimum 0x1F=Maximum
RESERVED13	15:13	0x0	
MC_IC_SAMPLE_SETTLE	19:16	0x8	Sample settle MCLK*2**n 0x0=Minimum 0xF=Maximum
MC_IC_INC_THRESHOLD	23:20	0x8	Number of over samples to increase strength 0x0=0 0xF=15
MC_IC_DEC_THRESHOLD	27:24	0x8	Number of under samples to decrease strength 0x0=0 0xF=15
MC_IC_OSC	28	0x0	Impedance controller oscillation mode 0=Stay at higher strength when oscillate 1=Oscillate when oscillate
MC_IC_SUSPEND	29	0x0	Impedance controller on/off in self refresh 0=Impedance controller on in self refresh 1=Impedance controller off in self refresh
RESERVED30	30	0x0	
MC_IC_ENABLE	31	0x0	Impedance controller enable 0=Off 1=On
Memory controller impedance controller setting			

MC_INTFC_IMP_CTRL_REF - RW - 32 bits - NBMCIND:0x93			
Field Name	**Bits**	**Default**	**Description**
MC_STRENGTH_N_REF	3:0	0xb	Reference N strength 0x0=Weakest 0xF=Strongest
MC_STRENGTH_P_REF	7:4	0xb	Reference P strength 0x0=Weakest 0xF=Strongest
MC_STR_READ_BACK_N_REF (R)	11:8	0x0	Reference N strength read back 0x0=Weakest 0xF=Strongest
MC_STR_READ_BACK_P_REF (R)	15:12	0x0	Reference P strength read back 0x0=Weakest 0xF=Strongest
MC_IC_N_LOCKED (R)	16	0x0	Impedance controller N strength locked read back 0x0=Not locked 0x1=Locked
MC_IC_P_LOCKED (R)	17	0x0	Impedance controller P strength locked read back 0x0=Not locked 0x1=Locked
MC_IC_N_OSCILLATION (R)	18	0x0	Impedance controller N strength oscillation read back 0x0=No oscillation 0x1=Oscillation

MC_IC_P_OSCILLATION (R)	19	0x0	Impedance controller P strength oscillation read back 0x0=No oscillation 0x1=Oscillation
RESERVED20	31:20	0x0	
Memory controller impedance controller reference strength and read back			

MC_LATENCY_COUNT_CNTL - RW - 32 bits - NBMCIND:0x94

Field Name	Bits	Default	Description
CLIENT_SEL	3:0	0x0	Select which clients to measure latency. 4'b0000:g3d0r 4'b0001:g3d1r 4'b0010:tx0r 4'b0011:cpr 4'b0100:vfr 4'b0101:idctr 4'b0110:hdpr 4'b0111:e2r 4'b1000:mcifr 4'b1001:dmifr 4'b1010:avpr 4'b1011:ptr 4'b1100:azr 4'b1101:g3d0w 4'b1110:g3d1w
RD_CLI_EOB_DIS	17:4	0x0	
WR_CLI_EOB_DIS	27:18	0x0	
ALL_CLI_EOB_DIS	28	0x0	
RESERVED	31:29	0x0	
Controls for latency counter (average latency is measured from sclk performance counter events 0x84 and 0x85			

MC_LATENCY_COUNT_EVENT - R - 32 bits - NBMCIND:0x95

Field Name	Bits	Default	Description
MIN_LATENCY	15:0	0x0	Minimum latency during the period of enabling sclk performance counter events 0x84 and 0x85
MAX_LATENCY	31:16	0x0	Maximum latency during the period of enabling sclk performance counter events 0x84 and 0x85
Min/Max latency readback from latency counter			

MCS_PERF_COUNT0 - R - 32 bits - NBMCIND:0x96

Field Name	Bits	Default	Description
MCS_COUNTER0	31:0	0x0	Lower 32 bits of Event0 counter
Memory controller performance counter for Event0 in SCLK			

MCS_PERF_COUNT1 - R - 32 bits - NBMCIND:0x97

Field Name	Bits	Default	Description
MCS_COUNTER1	31:0	0x0	Lower 32 bits of Event1 counter
Memory controller performance counter for Event1 in SCLK			

MCS_PERF_CNTL - RW - 32 bits - NBMCIND:0x98			
Field Name	**Bits**	**Default**	**Description**
MCS_EVENT0_SEL	7:0	0x0	Event0 selection: TBD
MCS_EVENT1_SEL	15:8	0x0	Event1 selection: Same definition as above
MCS_COUNTER0_UPPER (R)	23:16	0x0	Upper 8 bits of Event0 counter
MCS_COUNTER1_UPPER (R)	31:24	0x0	Upper 8 bits of Event1 counter
Memory controller performance counter control for SCLK			

MC_AZ_DEFAULT_ADDR - RW - 32 bits - NBMCIND:0x99			
Field Name	**Bits**	**Default**	**Description**
AZ_DEFAULT_ADDR	31:0	0x0	Azalia reads or writes that don't match the chipset apertures will be sent to this address. It represents [39:8] of the default address and [7:0] are taken to be 0.
Default read/write address for Azalia			

MCA_MEMORY_INIT_MRS - RW - 32 bits - NBMCIND:0xA0			
Field Name	**Bits**	**Default**	**Description**
MCA_MODE_REG	19:0	0x0	Value to be loaded into the memory mode or the extended mode register. [14:0]=Address [14:0] [15]=Reserved [18:16]=Bank [2:0] [19]=Reserved
MCA_INIT_CS_MRS	23:20	0xf	Channel A CS to be initialized 4'b0001=CS0/ 4'b0010= CS1/ 4'b0100=CS2/ 4'b1000=CS3/
MCA_INIT_SEQ	28:24	0x0	Initialization sequence selection for execution 0=Whole initialization sequence selected for execution 1-31=Initialization sequence selected for execution
MCA_INIT_IDLE	29	0x0	Forces MC channel A idle before initialization execution. 0=MC not forced idle before initialization execution 1=MC forced idle before initialization execution
MCA_INIT_COMPLETE	30	0x0	As long as this bit is '0', the MCA will not accept requests from the clients. It is used primarily to block requests when the MCA might mishandle them, such as when the FB or AGP apertures are undefined or unstable. 0=Register Initialization Not Complete 1=Register Initialization Complete
MCA_INIT_EXECUTE	31	0x0	The MC will execute software initialization command or whole hardware initialization sequence on a transition from 0 to 1 for memory controller MCA 0=Normal 1=Execute initialization command
Memory controller A initialization			

MCA_MEMORY_INIT_EMRS - RW - 32 bits - NBMCIND:0xA1			
Field Name	**Bits**	**Default**	**Description**
MCA_EXT_MODE_REG	19:0	0x10000	Value to be loaded in memory extended mode register in nominal mode with initialization sequence. Does not matter for step by step execution. 　[14:0]=Address [14:0] 　[15]=Reserved 　[18:16]=Bank [2:0] 　[19]=Reserved
MCA_INIT_CS_EMRS	23:20	0xf	Channel A CS to be initialized 　4'b0001=CS0/ 　4'b0010= CS1/ 　4'b0100=CS2/ 　4'b1000=CS3/
MCA_INIT_DLL	24	0x1	Enables the execution of the memory DLL reset mode register command for the nominal mode initialization sequence.
MCA_INIT_OCD	25	0x0	Drive 0/1 for OCD drive extended mode register command for nominal mode initialization sequence.
MCA_INIT_ZQC	26	0x0	Initializes ZQC one by one CS (nominal) or all CS together. 　0=Increment CS counter for each ZQC command 　executed in the same initialization sequence 　1=SEND ZQC command to all CS
MCA_INIT_MPR	27	0x0	Enables MPR read.
MCA_INIT_DQSS	28	0x0	Strobe sample by internal clock enable 　0=Strobe sample by internal clock disabled 　1=Strobe sample by internal clock enabled
MCA_INIT_OCDX	29	0x0	DDR3 optional OCD execution from EMRS2 A[11:9] instead of DDR2 OCD execution from MRS A[9:8]. 　0=DDR2 OCD 　1=DDR3 OCD
RESERVED30	31:30	0x0	
Memory controller A initialization extension			

MCA_MEMORY_INIT_EMRS2 - RW - 32 bits - NBMCIND:0xA2			
Field Name	**Bits**	**Default**	**Description**
MCA_EXT2_MODE_REG	19:0	0x20000	Value to be loaded in memory second extended mode register in nominal mode with initialization sequence. Does not matter for step by step execution. 　[14:0]=Address [14:0] 　[15]=Reserved 　[18:16]=Bank [2:0] 　[19]=Reserved
MCA_INIT_CS_EMRS2	23:20	0xf	Channel A CS to be initialized 　4'b0001=CS0/ 　4'b0010=CS1/ 　4'b0100=CS2/ 　4'b1000=CS3/

MCA_TWLODTEN	27:24	0x4	DDR3 ODT write levelization, tDQSS margining, x4 clocks 0=0 clock 1=1 clock 2=2 clock 3=3 clock … 13=13 clock 14=14 clock 15=15 clock
MCA_TWLDQSEN	31:28	0x7	DDR3 ODT write levelization, tDQSS margining, x4 clocks 0=0 clock 1=1 clock 2=2 clock 3=3 clock … 13=13 clock 14=14 clock 15=15 clock
Memory controller A initialization extension			

MCA_MEMORY_INIT_EMRS3 - RW - 32 bits - NBMCIND:0xA3			
Field Name	**Bits**	**Default**	**Description**
MCA_EXT3_MODE_REG	19:0	0x30000	Value to be loaded in memory third extended mode register in nominal mode with initialization sequence. Does not matter for step by step execution. [14:0]=Address [14:0] [15]=Reserved [18:16]=Bank [2:0] [19]=Reserved
MCA_INIT_CS_EMRS3	23:20	0xf	Channel A CS to be initialized 4'b0001=CS0/ 4'b0010=CS1/ 4'b0100=CS2/ 4'b1000=CS3/
MCA_TWLMRD	27:24	0xa	DDR3 ODT write levelization, tDQSS margining, x4 clocks 0=0 clock 1=1 clock 2=2 clock 3=3 clock … 13=13 clock 14=14 clock 15=15 clock
MCA_TDLL	31:28	0x4	Channel A DLL reset time, x64 clocks
Memory controller A initialization extension			

MCA_MEMORY_INIT_SEQUENCE_1 - RW - 32 bits - NBMCIND:0xA4			
Field Name	**Bits**	**Default**	**Description**
MCA_INIT_SEQ_OP_1	3:0	0x1	Operation #1 to be executed in memory initialization sequence.
MCA_INIT_SEQ_OP_2	7:4	0x5	Operation #2 to be executed in memory initialization sequence.
MCA_INIT_SEQ_OP_3	11:8	0x8	Operation #3 to be executed in memory initialization sequence.
MCA_INIT_SEQ_OP_4	15:12	0x4	Operation #4 to be executed in memory initialization sequence.
MCA_INIT_SEQ_OP_5	19:16	0x2	Operation #5 to be executed in memory initialization sequence.
MCA_INIT_SEQ_OP_6	23:20	0x2	Operation #6 to be executed in memory initialization sequence.
MCA_INIT_SEQ_OP_7	27:24	0x2	Operation #7 to be executed in memory initialization sequence.
MCA_INIT_SEQ_OP_8	31:28	0x2	Operation #8 to be executed in memory initialization sequence.

Memory controller A initialization sequence first chunk.

Initialization operation selection:
  0=NOP
  1=PRECHARGE ALL
  2=REFRESH
  3=ZQC
  4=MRS
  5=EMRS
  6=EMRS2
  7=EMRS3
  8=MRS DLL reset
  9=EMRS OCD default
  A=OCD adjust
  B=OCD drive
  C=Write levelization
  D=NOP 10 clocks
  E=NOP 50 clocks
  F=NOP 255 clocks

MCA_MEMORY_INIT_SEQUENCE_2 - RW - 32 bits - NBMCIND:0xA5			
Field Name	**Bits**	**Default**	**Description**
MCA_INIT_SEQ_OP_9	3:0	0x0	Operation #9 to be executed in memory initialization sequence.
MCA_INIT_SEQ_OP_10	7:4	0x0	Operation #10 to be executed in memory initialization sequence.
MCA_INIT_SEQ_OP_11	11:8	0x0	Operation #11 to be executed in memory initialization sequence.
MCA_INIT_SEQ_OP_12	15:12	0x0	Operation #12 to be executed in memory initialization sequence.
MCA_INIT_SEQ_OP_13	19:16	0x0	Operation #13 to be executed in memory initialization sequence.
MCA_INIT_SEQ_OP_14	23:20	0x0	Operation #14 to be executed in memory initialization sequence.
MCA_INIT_SEQ_OP_15	27:24	0x0	Operation #15 to be executed in memory initialization sequence.
MCA_INIT_SEQ_OP_16	31:28	0x0	Operation #16 to be executed in memory initialization sequence.

Memory controller A initialization sequence second chunk.
Initialization operation selection:
  0=NOP
  1=PRECHARGE ALL
  2=REFRESH
  3=ZQC
  4=MRS
  5=EMRS
  6=EMRS2
  7=EMRS3
  8=MRS DLL reset
  9=EMRS OCD default
  A=OCD adjust
  B=OCD drive
  C=Write levelization
  D=NOP 10 clocks
  E=NOP 50 clocks
  F=NOP 255 clocks			

MCA_MEMORY_INIT_SEQUENCE_3 - RW - 32 bits - NBMCIND:0xA6			
Field Name	**Bits**	**Default**	**Description**
MCA_INIT_SEQ_OP_17	3:0	0x0	Operation #17 to be executed in memory initialization sequence.
MCA_INIT_SEQ_OP_18	7:4	0x0	Operation #18 to be executed in memory initialization sequence.
MCA_INIT_SEQ_OP_19	11:8	0x0	Operation #19 to be executed in memory initialization sequence.
MCA_INIT_SEQ_OP_20	15:12	0x0	Operation #20 to be executed in memory initialization sequence.
MCA_INIT_SEQ_OP_21	19:16	0x0	Operation #21 to be executed in memory initialization sequence.
MCA_INIT_SEQ_OP_22	23:20	0x0	Operation #22 to be executed in memory initialization sequence.
MCA_INIT_SEQ_OP_23	27:24	0x0	Operation #23 to be executed in memory initialization sequence.
MCA_INIT_SEQ_OP_24	31:28	0x0	Operation #24 to be executed in memory initialization sequence.

Memory controller A initialization sequence third chunk.

Initialization operation selection:
  0=NOP
  1=PRECHARGE ALL
  2=REFRESH
  3=ZQC
  4=MRS
  5=EMRS
  6=EMRS2
  7=EMRS3
  8=MRS DLL reset
  9=EMRS OCD default
  A=OCD adjust
  B=OCD drive
  C=Write levelization
  D=NOP 10 clocks
  E=NOP 50 clocks
  F=NOP 255 clocks

MCA_MEMORY_INIT_SEQUENCE_4 - RW - 32 bits - NBMCIND:0xA7			
Field Name	**Bits**	**Default**	**Description**
MCA_INIT_SEQ_OP_25	3:0	0x0	Operation #25 to be executed in memory initialization sequence.
MCA_INIT_SEQ_OP_26	7:4	0x0	Operation #26 to be executed in memory initialization sequence.
MCA_INIT_SEQ_OP_27	11:8	0x0	Operation #27 to be executed in memory initialization sequence.
MCA_INIT_SEQ_OP_28	15:12	0x0	Operation #28 to be executed in memory initialization sequence.
MCA_INIT_SEQ_OP_29	19:16	0x0	Operation #29 to be executed in memory initialization sequence.
MCA_INIT_SEQ_OP_30	23:20	0x0	Operation #30 to be executed in memory initialization sequence.
MCA_INIT_SEQ_OP_31	27:24	0x0	Operation #31 to be executed in memory initialization sequence.
MCA_INIT_SEQ_OP_32	31:28	0x0	Operation #32 to be executed in memory initialization sequence.

Memory controller A initialization sequence fourth chunk.
Initialization operation selection:
  0=NOP
  1=PRECHARGE ALL
  2=REFRESH
  3=ZQC
  4=MRS
  5=EMRS
  6=EMRS2
  7=EMRS3
  8=MRS DLL reset
  9=EMRS OCD default
  A=OCD adjust
  B=OCD drive
  C=Write levelization
  D=NOP 10 clocks
  E=NOP 50 clocks
  F=NOP 255 clocks

MCA_TIMING_PARAMETERS_1 - RW - 32 bits - NBMCIND:0xA8			
Field Name	**Bits**	**Default**	**Description**
MCA_RD_LAT	3:0	0x4	Memory CAS Latency 0=0 clock (not supported) 1=1 clock (not supported) 2=2 clock 3=3 clock 4=4 clock 5=5 clock 6=6 clock 7=7 clock
MCA_WR_LAT	7:4	0x3	Memory Write Latency 0=0 clock (not supported) 1=1 clock 2=2 clock 3=3 clock 4=4 clock 5=5 clock 6=6 clock 7=7 clock
MCA_TRCDR	11:8	0x8	Active to Read delay 0=0 clock 1=1 clock 2=2 clock 3=3 clock … 13=13 clock 14=14 clock 15=15 clock
MCA_TRCDW	15:12	0x8	Active to Write delay 0=0 clock 1=1 clock 2=2 clock 3=3 clock … 13=13 clock 14=14 clock 15=15 clock
MCA_TRP	19:16	0x8	Precharge command period 0=0 clock 1=1 clock 2=2 clock 3=3 clock … 13=13 clock 14=14 clock 15=15 clock
MCA_TRTP	23:20	0x4	Internal Read to Precharge command delay 0=0 clock 1=1 clock 2=2 clock 3=3 clock 4=4 clock 5=5 clock 6=6 clock 7=7 clock

MCA_TWR	27:24	0x8	Write recovery time
			  0=0 clock
			  1=1 clock
			  2=2 clock
			  3=3 clock
			
			  …
			  13=13 clock
			  14=14 clock
			  15=15 clock

MCA_TRRD	31:28	0x6	Active bank A to Active bank B command period
			  0=0 clock
			  1=1 clock
			  2=2 clock
			  3=3 clock
			  4=4 clock
			  5=5 clock
			  6=6 clock
			  7=7 clock

Memory controller A timing parameters, set 1			

MCA_TIMING_PARAMETERS_2 - RW - 32 bits - NBMCIND:0xA9			
Field Name	**Bits**	**Default**	**Description**

MCA_TRAS	7:0	0x18	Active to Precharge command
			  0=0 clock
			  1=1 clock
			  2=2 clock
			  3=3 clock
			
			  …
			  29=29 clock
			  30=30 clock
			  31=31 clock

MCA_TRC	15:8	0x20	Row Cycle time. Active to Active/Auto-Refresh command period
			  0=0 clock
			  1=1 clock
			  2=2 clock
			  3=3 clock
			
			  …
			  125=125 clock
			  126=126 clock
			  127=127 clock

MCA_TRFC	23:16	0x28	Auto-Refresh to Active/Auto-Refresh command period
			  0=0 clock
			  1=1 clock
			  2=2 clock
			  3=3 clock
			
			  …
			  125=125 clock
			  126=126 clock
			  127=127 clock

MCA_TREFI	31:24	0x10	1 memory refresh is performed every TREFI*64 MCLK cycles.
Memory controller A timing parameters, set 2			

MCA_TIMING_PARAMETERS_3 - RW - 32 bits - NBMCIND:0xAA			
Field Name	**Bits**	**Default**	**Description**
MCA_TRTR_CS	3:0	0x1	Read to Read command to different CS 0=0 clock 1=1 clock 2=2 clock 3=3 clock 4=4 clock 5=5 clock 6=6 clock 7=7 clock
MCA_TRTW	7:4	0x2	Read to Write bus turnaround 0=0 clock 1=1 clock 2=2 clock 3=3 clock 4=4 clock 5=5 clock 6=6 clock 7=7 clock
MCA_TWTR	11:8	0x4	Internal Write to Read command delay 0=0 clock 1=1 clock 2=2 clock 3=3 clock 4=4 clock 5=5 clock 6=6 clock 7=7 clock
MCA_TWTR_CS	15:12	0x2	Write to Read command to different CS 0=0 clock 1=1 clock 2=2 clock 3=3 clock 4=4 clock 5=5 clock 6=6 clock 7=7 clock
MCA_TWTW_CS	19:16	0x1	Write to Write command to different CS 0=0 clock 1=1 clock 2=2 clock 3=3 clock 4=4 clock 5=5 clock 6=6 clock 7=7 clock
MCA_TCCD	23:20	0x2	CAS to CAS command delay 0=0 clock 1=1 clock 2=2 clock 3=3 clock … 13=13 clock 14=14 clock 15=15 clock

MCA_TCKE	27:24	0x3	CKE minimum high and low pulse width 0=0 clock 1=1 clock 2=2 clock 3=3 clock 4=4 clock 5=5 clock 6=6 clock 7=7 clock
MCA_TXP	31:28	0x2	Exit precharge power down to any valid command 0=0 clock 1=1 clock 2=2 clock 3=3 clock 4=4 clock 5=5 clock 6=6 clock 7=7 clock
Memory controller A timing parameters, set 3			

MCA_TIMING_PARAMETERS_4 - RW - 32 bits - NBMCIND:0xAB			
Field Name	**Bits**	**Default**	**Description**
MCA_TXARDS	3:0	0x6	Exit active power down to read command 0=0 clock 1=1 clock 2=2 clock 3=3 clock … 13=13 clock 14=14 clock 15=15 clock
MCA_TAXPD	7:4	0x8	ODT power down exit latency 0=0 clock 1=1 clock 2=2 clock 3=3 clock … 13=13 clock 14=14 clock 15=15 clock
MCA_TRPALL	11:8	0x2	Precharge all for 8 bank memories 0=0 clock 1=1 clock 2=2 clock 3=3 clock … 13=13 clock 14=14 clock 15=15 clock

MCA_TFAW	15:12	0x2	Back to back activate rolling window
			0=0 clock
			1=1 clock
			2=2 clock
			3=3 clock
			…
			13=13 clock
			14=14 clock
			15=15 clock
MCA_TZQCL	19:16	0x8	Impedance calibration long timing, can be merged with DLL time, x64 clocks.
MCA_TZQCS	23:20	0x4	Impedance calibration short timing, x16 clocks.
MCA_TZQCI	27:24	0x1	Impedance calibration interval, x256 refresh cycles.
MCA_TMRD	31:28	0x2	Mode register set command cycle time
			0=0 clock
			1=1 clock
			...
			15=15 clock
Memory controller A timing parameters, set 4			

MCA_MEMORY_TYPE - RW - 32 bits - NBMCIND:0xAC			
Field Name	**Bits**	**Default**	**Description**
MCA_MODE_CS0	3:0	0x0	MCA CS0 memory size
			0=Unpopulated chip select
			4=32MB (16Mbx16)
			5=64MB (32Mbx8)
			6=128MB (64Mbx8)
			10=256MB (512Mb, x16)
			11=512MB (1Gb, x16)
MCA_AP_BIT	4	0x0	MCA Auto Precharge bit
			0=A10
			1=A8
RESERVED5	7:5	0x0	
MCA_MODE_CS1	11:8	0x0	MCA CS1 memory size
			0=Unpopulated chip select
RESERVED12	15:12	0x0	
MCA_MODE_CS2	19:16	0x0	MCA CS2 memory size
			0=Unpopulated chip select
RESERVED20	23:20	0x0	
MCA_MODE_CS3	27:24	0x0	MCA CS3 memory size
			0=Unpopulated chip select
RESERVED28	31:28	0x0	
Memory controller A memory size and type			

MCA_CKE_MUX_SELECT - RW - 32 bits - NBMCIND:0xAD			
Field Name	**Bits**	**Default**	**Description**
MCA_MUX_SELECT_CKE0	3:0	0x1	Channel A CKE0 mux select
			4'b0001=CS0/
			4'b0010=CS1/
			4'b0100=CS2/
			4'b1000=CS3/

MCA_MUX_SELECT_CKE1	7:4	0x2	Channel A CKE1 mux select 4'b0001=CS0/ 4'b0010=CS1/ 4'b0100=CS2/ 4'b1000=CS3/
MCA_MUX_SELECT_CKE2	11:8	0x4	Channel A CKE2 mux select 4'b0001=CS0/ 4'b0010=CS1/ 4'b0100=CS2/ 4'b1000=CS3/
MCA_MUX_SELECT_CKE3	15:12	0x8	Channel A CKE3 mux select 4'b0001=CS0/ 4'b0010=CS1/ 4'b0100=CS2/ 4'b1000=CS3/
RESERVED16	31:16	0x0	
Memory controller A mux select CKE			

MCA_ODT_MUX_SELECT - RW - 32 bits - NBMCIND:0xAE			
Field Name	**Bits**	**Default**	**Description**
MCA_MUX_SELECT_ODTR0	3:0	0x1	Channel A ODT0 read mux select 4'b0001=CS0/ 4'b0010=CS1/ 4'b0100=CS2/ 4'b1000=CS3/
MCA_MUX_SELECT_ODTR1	7:4	0x2	Channel A ODT1 read mux select 4'b0001=CS0/ 4'b0010=CS1/ 4'b0100=CS2/ 4'b1000=CS3/
MCA_MUX_SELECT_ODTR2	11:8	0x4	Channel A ODT2 read mux select 4'b0001=CS0/ 4'b0010=CS1/ 4'b0100=CS2/ 4'b1000=CS3/
MCA_MUX_SELECT_ODTR3	15:12	0x8	Channel A ODT3 read mux select 4'b0001=CS0/ 4'b0010=CS1/ 4'b0100=CS2/ 4'b1000=CS3/
MCA_MUX_SELECT_ODTW0	19:16	0x1	Channel A ODT0 write mux select 4'b0001=CS0/ 4'b0010=CS1/ 4'b0100=CS2/ 4'b1000=CS3/
MCA_MUX_SELECT_ODTW1	23:20	0x2	Channel A ODT1 write mux select 4'b0001=CS0/ 4'b0010=CS1/ 4'b0100=CS2/ 4'b1000=CS3/
MCA_MUX_SELECT_ODTW2	27:24	0x4	Channel A ODT2 write mux select 4'b0001=CS0/ 4'b0010=CS1/ 4'b0100=CS2/ 4'b1000=CS3/

MCA_MUX_SELECT_ODTW3	31:28	0x8	Channel A ODT3 write mux select 4'b0001=CS0/ 4'b0010=CS1/ 4'b0100=CS2/ 4'b1000=CS3/
Memory controller A mux select ODT			

MCA_SEQ_PERF_CNTL - RW - 32 bits - NBMCIND:0xAF			
Field Name	**Bits**	**Default**	**Description**
MCA_IDLE_CHANGE_MIN	4:0	0x0	Channel A idle change minimum. Under dynamic mode this field and MCA_IDLE_LIMIT specify the lower bound of the limit. limit(min) = (4*MCA_IDLE_LIMIT) + MCA_IDLE_CHNAGE_MIN cycles.
RESERVED5	7:5	0x0	
MCA_IDLE_CHANGE_MAX	12:8	0x0	Channel A idle change maximum. Under dynamic mode this field and MCA_IDLE_LIMIT specify the upper bound of the limit. limit(max) = (4*MCA_IDLE_LIMIT) + MCA_IDLE_CHANGE_MAX cycles.
MCA_CMD_FIFO_EOB_OFF	13	0x0	Channel A command fifo end-of-burst. 0=Command fifo end-of-burst disabled 1=Command fifo end-of-burst enabled
RESERVED14	14	0x0	
MCA_ACTV_HI_PRI	15	0x0	Channel A hi priority activate. 0=Hi priority activate disabled 1=High priority activate enabled
MCA_IDLE_LIMIT	20:16	0x4	Channel A idle limit. The value of this field determines how long a page will be kept open after last page hit. 0x1F=No page open limit Otherwise limit=(4*MCA_IDLE_LIMIT) cycles
MCA_CMD_FIFO_EOB_ON	21	0x0	Channel A command fifo end-of-burst. 0=Command fifo end-of-burst disabled 1=Command fifo end-of-burst enabled
MCA_EARLY_ACTIVATE	22	0x0	Channel A early activate. 0=Early activate disabled 1=Early activate enabled
MCA_IDLE_LIMIT_DYNAMIC	23	0x0	Channel A idle limit dynamic. 0=Dynamic idle limit disabled 1=Dynamic idle limit enabled
MCA_CMD_FIFO_DEPTH	25:24	0x0	Channel A command FIFO depth. 0=1 entry 1=2 entries 2=3 entries 3=4 entries
MCA_BIU_RD_BYPASS_WR	26	0x0	Channel A BIU read bypass write. 0=Bypass disabled 1=Bypass enabled
MCA_BIU_RD_BYPASS_STALL	27	0x0	Channel A BIU read bypass stall 1 clock until timers OK. 0=Stall disabled 1=Stall enabled
MCA_BIU_RD_BYPASS_MAX	31:28	0x0	Channel A BIU read bypass maximum number. 0=Disabled BIU read bypass 1-14=Number of BIU read bypass 15=Unlimited number of BIU read bypass
Memory controller A sequencer performance control			

MCA_SEQ_CONTROL - RW - 32 bits - NBMCIND:0xB0			
Field Name	**Bits**	**Default**	**Description**
MCA_SEQ_MCIFR_URG_EN	0	0x0	Channel A urgent MCIF read. If mcif read is urgent and it is found in the command fifo then flush it out. 　0=Disable flushing out of urgent mcif reads 　1=Enable flushing out of urgent mcif reads
MCA_SEQ_DMIFR_URG_EN	1	0x0	Channel A urgent DMIF read. If dmif read is urgent and it is found in the command fifo then flush it out. 　0=Disable flushing out of urgent dmif reads 　1=Enable flushing out of urgent dmif reads
MCA_SEQ_AZR_URG_EN	2	0x0	Channel A urgent AZ read. If az read is urgent and it is found in the command fifo then flush it out. 　0=Disable flushing out of urgent az reads 　1=Enable flushing out of urgent az reads
MCA_SEQ_BIUW_URG_EN	3	0x0	Channel A urgent BIU write. If biu write is urgent and it is found in the command fifo then flush it out. 　0=Disable flushing out of urgent biu writes 　1=Enable flushing out of urgent biu writes
MCA_DQ_PRE	5:4	0x0	Write data preamble / postamble 　0=Low 　1=High 　2=Opposite of first / last data 　3=The same as first / last data
MCA_AP_DISABLE	6	0x0	Channel A auto precharge disable 　0=Auto recharge enabled 　1=Auto precharge disabled
MCA_CKE_FOR_ODT	7	0x0	Channel A ODT CKE stall 　0=No stall 　1=Stall
MCA_BURST_LENGTH_8	8	0x0	Channel A Burst Length 　0=Burst Length 4 　1=Burst Length 8
MCA_2T_TIMING	9	0x0	Channel A timing mode 　0=1T timing 　1=2T timing
MCA_3T_TIMING	10	0x0	Channel A timing mode 　0=1T timing 　1=3T timing
RESERVED11	11	0x0	
RESERVED12	19:12	0x0	
MCA_TCKED	23:20	0x8	Channel A CKE time delay, time from CKE condition to CKE low, x4 clocks 　0=0 clock 　1=1 clock 　2=2 clock 　3=3 clock 　4=4 clock 　5=5 clock 　6=6 clock 　7=7 clock

MCA_TTRSTD	27:24	0x8	Channel A tristate time delay, time from tristate condition to tristate, x4 clocks
			  0=0 clock
			  1=1 clock
			  2=2 clock
			  3=3 clock
			  4=4 clock
			  5=5 clock
			  6=6 clock
			  7=7 clock

MCA_TTRST	31:28	0x4	Channel A tristate time, time from tristate to full drive
			  0=0 clock
			  1=1 clock
			  2=2 clock
			  3=3 clock
			  4=4 clock
			  5=5 clock
			  6=6 clock
			  7=7 clock

Memory controller A sequencer control			

MCA_RECEIVING - RW - 32 bits - NBMCIND:0xB1			
Field Name	**Bits**	**Default**	**Description**

MCA_DQ_TRANSFER	3:0	0x4	Channel A read data transfer from strobe flops to core clock flops
			  0=CL+0clock
			  1=CL+1clock
			  2=CL+2clock
			  3=CL+3clock
			  4=CL+4clock

MCA_DQS_RST_PLS	5:4	0x2	Channel A read strobe reset pulse
			  0=Quarter pulse, Quarter position
			  1=Half pulse, Quarter position
			  2=Half pulse, Half position
			  3=Reserved

MCA_DQ_DQS_REC_DYNAMIC	6	0x0	Channel A data and strobe receiver enable control
			  0=Always enabled
			  1=Enabled for read only

RESERVED7	7	0x0	
RESERVED8	11:8	0x0	

MCA_IN_TERM_START_DQ	12	0x0	Channel A data input termination turning on for read preceded by write
			  0=Turning on half clock after OE off
			  1=Turning on full clock after OE off

MCA_IN_TERM_STOP_DQ	13	0x0	Channel A data input termination turning off for read followed by write
			  0=Turning off half clock before OE on
			  1=Turning off full clock before OE on

MCA_IN_TERM_START_DQS	14	0x0	Channel A strobe input termination turning on for read preceded by write
			  0=Turning on half clock after OE off
			  1=Turning on full clock after OE off

MCA_IN_TERM_STOP_DQS	15	0x0	Channel A strobe input termination turning off for read followed by write
			  0=Turning off half clock before OE on
			  1=Turning off full clock before OE on

MCA_IN_TERM_N_DQ	18:16	0x3	Channel A data input N termination, 3 pull-down resistors 300 Ohm
			  0=Termination off
			  1=300 Ohm pull-down
			  3=150 Ohm pull-down
			  7=100 Ohm pull-down

RESERVED19	19	0x0	

MCA_IN_TERM_P_DQ	22:20	0x3	Channel A data input P termination, 3 pull-up resistors 300 Ohm
			  0=Termination off
			  1=300 Ohm pull-up
			  3=150 Ohm pull-up
			  7=100 Ohm pull-up

RESERVED23	23	0x0	

MCA_IN_TERM_N_DQS	26:24	0x3	Channel A strobe input N termination, 3 pull-down resistors 300 Ohm
			  0=Termination off
			  1=300 Ohm pull-down
			  3=150 Ohm pull-down
			  7=100 Ohm pull-down

RESERVED27	27	0x0	

MCA_IN_TERM_P_DQS	30:28	0x3	Channel A strobe input P termination, 3 pull-up resistors 300 Ohm
			0=Termination off
			1=300 Ohm pull-up
			3=150 Ohm pull-up
			7=100 Ohm pull-up
RESERVED31	31	0x0	
Memory controller A receiving control			

MCA_IN_TIMING_DQS_3210 - RW - 32 bits - NBMCIND:0xB2			
Field Name	**Bits**	**Default**	**Description**
MCA_DQS_ARRIVAL_0	4:0	0x6	Channel A byte 0 input strobe reset removal edge
			0=CL
			1=CL+0.25
			2=CL+0.50
			3=CL+0.75
			4=CL+1.00
			5=CL+1.25
			6=CL+1.50
			7=CL+1.75
			8=CL+2.00
			9=CL+2.25
			10=CL+2.50
			11=CL+2.75
			12=CL+3.00
			13=CL+3.25
			14=CL+3.50
			15=CL+3.75
			16=CL+4.00
			17=CL+4.25
RESERVED5	7:5	0x0	
MCA_DQS_ARRIVAL_1	12:8	0x6	Channel A byte 1 input strobe reset removal edge
			0=CL
			1=CL+0.25
			2=CL+0.50
			3=CL+0.75
			4=CL+1.00
			5=CL+1.25
			6=CL+1.50
			7=CL+1.75
			8=CL+2.00
			9=CL+2.25
			10=CL+2.50
			11=CL+2.75
			12=CL+3.00
			13=CL+3.25
			14=CL+3.50
			15=CL+3.75
			16=CL+4.00
			17=CL+4.25
RESERVED13	15:13	0x0	

MCA_DQS_ARRIVAL_2	20:16	0x6	Channel A byte 2 input strobe reset removal edge
			0=CL
			1=CL+0.25
			2=CL+0.50
			3=CL+0.75
			4=CL+1.00
			5=CL+1.25
			6=CL+1.50
			7=CL+1.75
			8=CL+2.00
			9=CL+2.25
			10=CL+2.50
			11=CL+2.75
			12=CL+3.00
			13=CL+3.25
			14=CL+3.50
			15=CL+3.75
			16=CL+4.00
			17=CL+4.25
RESERVED21	23:21	0x0	
MCA_DQS_ARRIVAL_3	28:24	0x6	Channel A byte 3 input strobe reset removal edge
			0=CL
			1=CL+0.25
			2=CL+0.50
			3=CL+0.75
			4=CL+1.00
			5=CL+1.25
			6=CL+1.50
			7=CL+1.75
			8=CL+2.00
			9=CL+2.25
			10=CL+2.50
			11=CL+2.75
			12=CL+3.00
			13=CL+3.25
			14=CL+3.50
			15=CL+3.75
			16=CL+4.00
			17=CL+4.25
RESERVED29	31:29	0x0	
Channel A input strobe gating timing			

MCA_IN_TIMING_DQS_7654 - RW - 32 bits - NBMCIND:0xB3			
Field Name	**Bits**	**Default**	**Description**
MCA_DQS_ARRIVAL_4	4:0	0x6	Channel A byte 4 input strobe reset removal edge 0=CL 1=CL+0.25 2=CL+0.50 3=CL+0.75 4=CL+1.00 5=CL+1.25 6=CL+1.50 7=CL+1.75 8=CL+2.00 9=CL+2.25 10=CL+2.50 11=CL+2.75 12=CL+3.00 13=CL+3.25 14=CL+3.50 15=CL+3.75 16=CL+4.00 17=CL+4.25
RESERVED5	7:5	0x0	
MCA_DQS_ARRIVAL_5	12:8	0x6	Channel A byte 5 input strobe reset removal edge 0=CL 1=CL+0.25 2=CL+0.50 3=CL+0.75 4=CL+1.00 5=CL+1.25 6=CL+1.50 7=CL+1.75 8=CL+2.00 9=CL+2.25 10=CL+2.50 11=CL+2.75 12=CL+3.00 13=CL+3.25 14=CL+3.50 15=CL+3.75 16=CL+4.00 17=CL+4.25
RESERVED13	15:13	0x0	

MCA_DQS_ARRIVAL_6	20:16	0x6	Channel A byte 6 input strobe reset removal edge
			  0=CL
			  1=CL+0.25
			  2=CL+0.50
			  3=CL+0.75
			  4=CL+1.00
			  5=CL+1.25
			  6=CL+1.50
			  7=CL+1.75
			  8=CL+2.00
			  9=CL+2.25
			  10=CL+2.50
			  11=CL+2.75
			  12=CL+3.00
			  13=CL+3.25
			  14=CL+3.50
			  15=CL+3.75
			  16=CL+4.00
			  17=CL+4.25

RESERVED21	23:21	0x0	

MCA_DQS_ARRIVAL_7	28:24	0x6	Channel A byte 7 input strobe reset removal edge
			  0=CL
			  1=CL+0.25
			  2=CL+0.50
			  3=CL+0.75
			  4=CL+1.00
			  5=CL+1.25
			  6=CL+1.50
			  7=CL+1.75
			  8=CL+2.00
			  9=CL+2.25
			  10=CL+2.50
			  11=CL+2.75
			  12=CL+3.00
			  13=CL+3.25
			  14=CL+3.50
			  15=CL+3.75
			  16=CL+4.00
			  17=CL+4.25

RESERVED29	31:29	0x0	
Channel A input strobe gating timing			

MCA_DRIVING - RW - 32 bits - NBMCIND:0xB4			
Field Name	**Bits**	**Default**	**Description**
MCA_CK_ENABLE	5:0	0x0	Channel A clock pair select, enable 　0=Particular clock pair disabled 　1=Particular clock pair enabled
MCA_CKE_ENABLE	6	0x0	Channel A CKE enable 　0=CKE disabled, forced low 　1=CKE enabled, high or dynamic
MCA_CKE_DYNAMIC	7	0x0	Channel A CKE dynamic 　0=CKE high when enabled 　1=CKE dynamic when enabled, high or low depending 　on activity, active or precharge power down
MCA_ODT_ENABLE	8	0x0	Channel A ODT enable 　0=ODT forced 0 　1=ODT enabled
MCA_ODT_DYNAMIC	9	0x1	Channel A ODT dynamic 　0=ODT forced 1 if enabled 　1=ODT dynamic if enabled
MCA_ODT_READ	10	0x0	Channel A ODT enable for read 　0=ODT disabled for read 　1=ODT enabled for read
MCA_ODT_WRITE	11	0x1	Channel A ODT enable for write 　0=ODT disabled for write 　1=ODT enabled for write
MCA_ODTR_POSITION	13:12	0x0	Channel A ODT read position When ODTX 0, read latency dependent When ODTX 1, read command dependent 　0=ODT start at RL-3 for ODTX 0, ODT start at RD for 　ODTX1 　1=ODT start at RL-2 for ODTX 0, ODT start at RD+1 for 　ODTX 1 　2/3=1 clock later
MCA_ODTR_LENGTH	15:14	0x0	Channel A ODT read length 　0=ODT length BL/2+1 　1=ODT length BL/2+2 　2/3=1 clock longer
MCA_ODTW_POSITION	17:16	0x0	Channel A ODT write position When ODTX 0, write latency dependent When ODTX 1, write command dependent 　0=ODT start at WL-3 for ODTX 0, ODT start at WR for 　ODTX1 　1=ODT start at WL-2 for ODTX 0, ODT start at WR+1 for 　ODTX 1 　2/3=1 clock later
MCA_ODTW_LENGTH	19:18	0x0	Channel A ODT write length 　0=ODT length BL/2+1 　1=ODT length BL/2+2 　2/3=1 clock longer
MCA_ODT_STALL	20	0x0	Channel A ODT stall first write 　0=No stall 　1=Stall
MCA_ODTX	21	0x0	Channel A ODTX enable 　0=ODTX disable 　1=ODTX enable
MCA_ODTX_1T	22	0x0	Channel A ODTX 1T 　0=1T/2T/3T 　1=1T

MCA_ODTX_POSITION	23	0x0	Channel A ODTX position 0=ODTX start as set with ODT_START 1=ODT start one clock later then set with ODT_START
MCA_DQS_PRE	25:24	0x1	Channel A strobe output preamble 0=0.5 clock 1=1 clock 2=1.5 clock 3=2 clock
MCA_DQS_POST	27:26	0x1	Channel A strobe output postamble 0=0.5 clock 1=1 clock 2=1.5 clock 3=2 clock
MCA_DQSX_PRE	28	0x0	Channel A DQS preamble pulse 0=Preamble low 1=Preamble pulse
MCA_DQSX_POST	29	0x0	Channel A DQS postamble pulse 0=As set with DQS_POST 1=One clock extended DQS_POST
MCA_DQSX_PRE_HI	30	0x0	Channel A DQS preamble/postamble high 0=Preamble low 1=Preamble high
RESERVED31	31	0x0	
Memory controller A driving control			

MCA_OUT_TIMING - RW - 32 bits - NBMCIND:0xB5			
Field Name	**Bits**	**Default**	**Description**
MCA_OUT_TIMING_CK	2:0	0x4	Channel A clock output timing 0= -1 clock delay 1= -3/4 clock delay 2= -1/2 clock delay 3= -1/4 clock delay 4=0 clock delay 5=1/4 clock delay 6=1/2 clock delay 7=3/4 clock delay
MCA_PAD_BYPASS_CK	3	0x1	Channel A clock bypassing pad flops 0=Through pad flops 1=Bypass pad flops
MCA_OUT_TIMING_CKE	6:4	0x5	Channel A CKE output timing 0= -1 clock delay 1= -3/4 clock delay 2= -1/2 clock delay 3= -1/4 clock delay 4=0 clock delay 5=1/4 clock delay 6=1/2 clock delay 7=3/4 clock delay
MCA_PAD_BYPASS_CKE	7	0x1	Channel A CKE bypassing pad flops 0=Through pad flops 1=Bypass pad flops

MCA_OUT_TIMING_CS	10:8	0x5	Channel A CS output timing 0= -1 clock delay 1= -3/4 clock delay 2= -1/2 clock delay 3= -1/4 clock delay 4=0 clock delay 5=1/4 clock delay 6=1/2 clock delay 7=3/4 clock delay
MCA_PAD_BYPASS_CS	11	0x1	Channel A CS bypassing pad flops 0=Through pad flops 1=Bypass pad flops
MCA_OUT_TIMING_CMD	14:12	0x5	Channel A address and command output timing 0= -1 clock delay 1= -3/4 clock delay 2= -1/2 clock delay 3= -1/4 clock delay 4=0 clock delay 5=1/4 clock delay 6=1/2 clock delay 7=3/4 clock delay
MCA_PAD_BYPASS_CMD	15	0x1	Channel A address and command bypassing pad flops 0=Through pad flops 1=Bypass pad flops
MCA_OUT_TIMING_ODT	18:16	0x5	Channel A ODT output timing 0= -1 clock delay 1= -3/4 clock delay 2= -1/2 clock delay 3= -1/4 clock delay 4=0 clock delay 5=1/4 clock delay 6=1/2 clock delay 7=3/4 clock delay
MCA_PAD_BYPASS_ODT	19	0x1	Channel A ODT bypassing pad flops 0=Through pad flops 1=Bypass pad flops
MCA_OUT_TIMING_DQ	22:20	0x3	Channel A data and mask output timing 0= -1 clock delay 1= -3/4 clock delay 2= -1/2 clock delay 3= -1/4 clock delay 4=0 clock delay 5=1/4 clock delay 6=1/2 clock delay 7=3/4 clock delay
MCA_PAD_BYPASS_DQ	23	0x1	Channel A data and mask bypassing pad flops 0=Through pad flops 1=Bypass pad flops
MCA_OUT_TIMING_DQS	26:24	0x4	Channel A strobe output timing 0= -1 clock delay 1= -3/4 clock delay 2= -1/2 clock delay 3= -1/4 clock delay 4=0 clock delay 5=1/4 clock delay 6=1/2 clock delay 7=3/4 clock delay
MCA_PAD_BYPASS_DQS	27	0x1	Channel A strobe bypassing pad flops 0=Through pad flops 1=Bypass pad flops

MCA_OUT_TIMING_XXX	30:28	0x0	Channel A XXX output timing
			0= -1 clock delay
			1= -3/4 clock delay
			2= -1/2 clock delay
			3= -1/4 clock delay
			4=0 clock delay
			5=1/4 clock delay
			6=1/2 clock delay
			7=3/4 clock delay
MCA_PAD_BYPASS_XXX	31	0x1	Channel A XXX bypassing pad flops
			0=Through pad flops
			1=Bypass pad flops
Memory controller A output timing			

MCA_OUT_TIMING_DQ - RW - 32 bits - NBMCIND:0xB6			
Field Name	**Bits**	**Default**	**Description**
MCA_OUT_TIMING_DQ_B0	3:0	0x3	Channel A byte 0 data and mask output timing
			0= -1 clock delay
			1= -3/4 clock delay
			2= -1/2 clock delay
			3= -1/4 clock delay
			4=0 clock delay
			5=1/4 clock delay
			6=1/2 clock delay
			7=3/4 clock delay
MCA_OUT_TIMING_DQ_B1	7:4	0x3	Channel A byte 1 data and mask output timing
			0= -1 clock delay
			1= -3/4 clock delay
			2= -1/2 clock delay
			3= -1/4 clock delay
			4=0 clock delay
			5=1/4 clock delay
			6=1/2 clock delay
			7=3/4 clock delay
MCA_OUT_TIMING_DQ_B2	11:8	0x3	Channel A byte 2 data and mask output timing
			0= -1 clock delay
			1= -3/4 clock delay
			2= -1/2 clock delay
			3= -1/4 clock delay
			4=0 clock delay
			5=1/4 clock delay
			6=1/2 clock delay
			7=3/4 clock delay
MCA_OUT_TIMING_DQ_B3	15:12	0x3	Channel A byte 3 data and mask output timing
			0= -1 clock delay
			1= -3/4 clock delay
			2= -1/2 clock delay
			3= -1/4 clock delay
			4=0 clock delay
			5=1/4 clock delay
			6=1/2 clock delay
			7=3/4 clock delay

MCA_OUT_TIMING_DQ_B4	19:16	0x3	Channel A byte 4 data and mask output timing 0= -1 clock delay 1= -3/4 clock delay 2= -1/2 clock delay 3= -1/4 clock delay 4=0 clock delay 5=1/4 clock delay 6=1/2 clock delay 7=3/4 clock delay
MCA_OUT_TIMING_DQ_B5	23:20	0x3	Channel A byte 5 data and mask output timing 0= -1 clock delay 1= -3/4 clock delay 2= -1/2 clock delay 3= -1/4 clock delay 4=0 clock delay 5=1/4 clock delay 6=1/2 clock delay 7=3/4 clock delay
MCA_OUT_TIMING_DQ_B6	27:24	0x3	Channel A byte 6 data and mask output timing 0= -1 clock delay 1= -3/4 clock delay 2= -1/2 clock delay 3= -1/4 clock delay 4=0 clock delay 5=1/4 clock delay 6=1/2 clock delay 7=3/4 clock delay
MCA_OUT_TIMING_DQ_B7	31:28	0x3	Channel A byte 7 data and mask output timing 0= -1 clock delay 1= -3/4 clock delay 2= -1/2 clock delay 3= -1/4 clock delay 4=0 clock delay 5=1/4 clock delay 6=1/2 clock delay 7=3/4 clock delay
Channel A output data and mask timing			

MCA_OUT_TIMING_DQS - RW - 32 bits - NBMCIND:0xB7			
Field Name	**Bits**	**Default**	**Description**
MCA_OUT_TIMING_DQS_0	3:0	0x4	Channel A byte 0 strobe output timing 0= -1 clock delay 1= -3/4 clock delay 2= -1/2 clock delay 3= -1/4 clock delay 4=0 clock delay 5=1/4 clock delay 6=1/2 clock delay 7=3/4 clock delay
MCA_OUT_TIMING_DQS_1	7:4	0x4	Channel A byte 1 strobe output timing 0= -1 clock delay 1= -3/4 clock delay 2= -1/2 clock delay 3= -1/4 clock delay 4=0 clock delay 5=1/4 clock delay 6=1/2 clock delay 7=3/4 clock delay
MCA_OUT_TIMING_DQS_2	11:8	0x4	Channel A byte 2 strobe output timing 0= -1 clock delay 1= -3/4 clock delay 2= -1/2 clock delay 3= -1/4 clock delay 4=0 clock delay 5=1/4 clock delay 6=1/2 clock delay 7=3/4 clock delay
MCA_OUT_TIMING_DQS_3	15:12	0x4	Channel A byte 3 strobe output timing 0= -1 clock delay 1= -3/4 clock delay 2= -1/2 clock delay 3= -1/4 clock delay 4=0 clock delay 5=1/4 clock delay 6=1/2 clock delay 7=3/4 clock delay
MCA_OUT_TIMING_DQS_4	19:16	0x4	Channel A byte 4 strobe output timing 0= -1 clock delay 1= -3/4 clock delay 2= -1/2 clock delay 3= -1/4 clock delay 4=0 clock delay 5=1/4 clock delay 6=1/2 clock delay 7=3/4 clock delay
MCA_OUT_TIMING_DQS_5	23:20	0x4	Channel A byte 5 strobe output timing 0= -1 clock delay 1= -3/4 clock delay 2= -1/2 clock delay 3= -1/4 clock delay 4=0 clock delay 5=1/4 clock delay 6=1/2 clock delay 7=3/4 clock delay

MCA_OUT_TIMING_DQS_6	27:24	0x4	Channel A byte 6 strobe output timing 0= -1 clock delay 1= -3/4 clock delay 2= -1/2 clock delay 3= -1/4 clock delay 4=0 clock delay 5=1/4 clock delay 6=1/2 clock delay 7=3/4 clock delay
MCA_OUT_TIMING_DQS_7	31:28	0x4	Channel A byte 7 strobe output timing 0= -1 clock delay 1= -3/4 clock delay 2= -1/2 clock delay 3= -1/4 clock delay 4=0 clock delay 5=1/4 clock delay 6=1/2 clock delay 7=3/4 clock delay
Channel A output strobe timing			

MCA_STRENGTH_N - RW - 32 bits - NBMCIND:0xB8			
Field Name	**Bits**	**Default**	**Description**
MCA_STRENGTH_N_CK	3:0	0xb	Channel A clock (nominal and complement) strength N driver 0=Minimum strength 15=Maximum strength
MCA_STRENGTH_N_CKE	7:4	0xb	Channel A CKE strength N driver 0=Minimum strength 15=Maximum strength
MCA_STRENGTH_N_CS	11:8	0xb	Channel A CS strength N driver 0=Minimum strength 15=Maximum strength
MCA_STRENGTH_N_CMD	15:12	0xb	Channel A RAS/CAS/WE and address strength N driver 0=Minimum strength 15=Maximum strength
MCA_STRENGTH_N_ODT	19:16	0xb	Channel A ODT strength N driver 0=Minimum strength 15=Maximum strength
MCA_STRENGTH_N_DQ	23:20	0xb	Channel A data and mask strength N driver 0=Minimum strength 15=Maximum strength
MCA_STRENGTH_N_DQS	27:24	0xb	Channel A strobe (nominal and complement) strength N driver 0=Minimum strength 15=Maximum strength
MCA_STRENGTH_N_XXX	31:28	0xb	Channel A spare strength N driver 0=Minimum strength 15=Maximum strength
Memory controller A strength N			

MCA_STRENGTH_P - RW - 32 bits - NBMCIND:0xB9			
Field Name	**Bits**	**Default**	**Description**
MCA_STRENGTH_P_CK	3:0	0xb	Channel A clock (nominal and complement) strength P driver 　0=Minimum strength 　15=Maximum strength
MCA_STRENGTH_P_CKE	7:4	0xb	Channel A CKE strength P driver 　0=Minimum strength 　15=Maximum strength
MCA_STRENGTH_P_CS	11:8	0xb	Channel A CS strength P driver 　0=Minimum strength 　15=Maximum strength
MCA_STRENGTH_P_CMD	15:12	0xb	Channel A RAS/CAS/WE and address strength P driver 　0=Minimum strength 　15=Maximum strength
MCA_STRENGTH_P_ODT	19:16	0xb	Channel A ODT strength P driver 　0=Minimum strength 　15=Maximum strength
MCA_STRENGTH_P_DQ	23:20	0xb	Channel A data and mask strength P driver 　0=Minimum strength 　15=Maximum strength
MCA_STRENGTH_P_DQS	27:24	0xb	Channel A strobe (nominal and complement) strength P driver 　0=Minimum strength 　15=Maximum strength
MCA_STRENGTH_P_XXX	31:28	0xb	Channel A spare strength P driver 　0=Minimum strength 　15=Maximum strength
Memory controller A strength P			

MCA_STRENGTH_STEP - RW - 32 bits - NBMCIND:0xBA			
Field Name	**Bits**	**Default**	**Description**
MCA_STR_STEP_N_CK	1:0	0x1	Channel A clock (nominal and complement) impedance controller adjustment step for strength N driver 　0=0 step, no adjustment 　1=1 step, adjustment the same as reference 　2=2 step, higher than reference adjustment 　3=3 step, higher than reference adjustment
MCA_STR_STEP_P_CK	3:2	0x1	Channel A clock (nominal and complement) impedance controller adjustment step for strength P driver 　0=0 step, no adjustment 　1=1 step, adjustment the same as reference 　2=2 step, higher than reference adjustment 　3=3 step, higher than reference adjustment
MCA_STR_STEP_N_CKE	5:4	0x1	Channel A CKE impedance controller adjustment step for strength N driver 　0=0 step, no adjustment 　1=1 step, adjustment the same as reference 　2=2 step, higher than reference adjustment 　3=3 step, higher than reference adjustment

MCA_STR_STEP_P_CKE	7:6	0x1	Channel A CKE impedance controller adjustment step for strength P driver
			  0=0 step, no adjustment
			  1=1 step, adjustment the same as reference
			  2=2 step, higher than reference adjustment
			  3=3 step, higher than reference adjustment

MCA_STR_STEP_N_CS	9:8	0x1	Channel A CS impedance controller adjustment step for strength N driver
			  0=0 step, no adjustment
			  1=1 step, adjustment the same as reference
			  2=2 step, higher than reference adjustment
			  3=3 step, higher than reference adjustment

MCA_STR_STEP_P_CS	11:10	0x1	Channel A CS impedance controller adjustment step for strength P driver
			  0=0 step, no adjustment
			  1=1 step, adjustment the same as reference
			  2=2 step, higher than reference adjustment
			  3=3 step, higher than reference adjustment

MCA_STR_STEP_N_CMD	13:12	0x1	Channel A RAS/CAS/WE and address impedance controller adjustment step for strength N driver
			  0=0 step, no adjustment
			  1=1 step, adjustment the same as reference
			  2=2 step, higher than reference adjustment
			  3=3 step, higher than reference adjustment

MCA_STR_STEP_P_CMD	15:14	0x1	Channel A RAS/CAS/WE and address impedance controller adjustment step for strength P driver
			  0=0 step, no adjustment
			  1=1 step, adjustment the same as reference
			  2=2 step, higher than reference adjustment
			  3=3 step, higher than reference adjustment

MCA_STR_STEP_N_ODT	17:16	0x1	Channel A ODT impedance controller adjustment step for strength N driver
			  0=0 step, no adjustment
			  1=1 step, adjustment the same as reference
			  2=2 step, higher than reference adjustment
			  3=3 step, higher than reference adjustment

MCA_STR_STEP_P_ODT	19:18	0x1	Channel A ODT impedance controller adjustment step for strength P driver
			  0=0 step, no adjustment
			  1=1 step, adjustment the same as reference
			  2=2 step, higher than reference adjustment
			  3=3 step, higher than reference adjustment

MCA_STR_STEP_N_DQ	21:20	0x1	Channel A data and mask impedance controller adjustment step for strength N driver
			  0=0 step, no adjustment
			  1=1 step, adjustment the same as reference
			  2=2 step, higher than reference adjustment
			  3=3 step, higher than reference adjustment

MCA_STR_STEP_P_DQ	23:22	0x1	Channel A data and mask impedance controller adjustment step for strength P driver
			  0=0 step, no adjustment
			  1=1 step, adjustment the same as reference
			  2=2 step, higher than reference adjustment
			  3=3 step, higher than reference adjustment

MCA_STR_STEP_N_DQS	25:24	0x1	Channel A strobe (nominal and complement) impedance controller adjustment step for strength N driver
			  0=0 step, no adjustment
			  1=1 step, adjustment the same as reference
			  2=2 step, higher than reference adjustment
			  3=3 step, higher than reference adjustment

MCA_STR_STEP_P_DQS	27:26	0x1	Channel A strobe (nominal and complement) impedance controller adjustment step for strength P driver 0=0 step, no adjustment 1=1 step, adjustment the same as reference 2=2 step, higher than reference adjustment 3=3 step, higher than reference adjustment
MCA_STR_STEP_N_XXX	29:28	0x1	Channel A spare impedance controller adjustment step for strength N driver 0=0 step, no adjustment 1=1 step, adjustment the same as reference 2=2 step, higher than reference adjustment 3=3 step, higher than reference adjustment
MCA_STR_STEP_P_XXX	31:30	0x1	Channel A spare impedance controller adjustment step for strength P driver 0=0 step, no adjustment 1=1 step, adjustment the same as reference 2=2 step, higher than reference adjustment 3=3 step, higher than reference adjustment
Memory controller A impedance controller adjustment step for strength			

MCA_STRENGTH_READ_BACK_N - RW - 32 bits - NBMCIND:0xBB			
Field Name	**Bits**	**Default**	**Description**
MCA_STR_READ_BACK_N_CK (R)	3:0	0x0	Channel A clock (nominal and complement) read back strength N driver 0=Minimum strength 15=Maximum strength
MCA_STR_READ_BACK_N_CKE (R)	7:4	0x0	Channel A CKE read back strength N driver 0=Minimum strength 15=Maximum strength
MCA_STR_READ_BACK_N_CS (R)	11:8	0x0	Channel A CS read back strength N driver 0=Minimum strength 15=Maximum strength
MCA_STR_READ_BACK_N_CMD (R)	15:12	0x0	Channel A RAS/CAS/WE and address read back strength N driver 0=Minimum strength 15=Maximum strength
MCA_STR_READ_BACK_N_ODT (R)	19:16	0x0	Channel A ODT read back strength N driver 0=Minimum strength 15=Maximum strength
MCA_STR_READ_BACK_N_DQ (R)	23:20	0x0	Channel A data and mask read back strength N driver 0=Minimum strength 15=Maximum strength
MCA_STR_READ_BACK_N_DQS (R)	27:24	0x0	Channel A strobe (nominal and complement) read back strength N driver 0=Minimum strength 15=Maximum strength
MCA_STR_READ_BACK_N_XXX (R)	31:28	0x0	Channel A spare read back strength N driver 0=Minimum strength 15=Maximum strength
Memory controller A strength N read back			

MCA_STRENGTH_READ_BACK_P - RW - 32 bits - NBMCIND:0xBC			
Field Name	**Bits**	**Default**	**Description**
MCA_STR_READ_BACK_P_CK (R)	3:0	0x0	Channel A clock (nominal and complement) read back strength P driver 　0=Minimum strength 　15=Maximum strength
MCA_STR_READ_BACK_P_CKE (R)	7:4	0x0	Channel A CKE read back strength P driver 　0=Minimum strength 　15=Maximum strength
MCA_STR_READ_BACK_P_CS (R)	11:8	0x0	Channel A CS read back strength P driver 　0=Minimum strength 　15=Maximum strength
MCA_STR_READ_BACK_P_CMD (R)	15:12	0x0	Channel A RAS/CAS/WE and address read back strength P driver 　0=Minimum strength 　15=Maximum strength
MCA_STR_READ_BACK_P_ODT (R)	19:16	0x0	Channel A ODT read back strength P driver 　0=Minimum strength 　15=Maximum strength
MCA_STR_READ_BACK_P_DQ (R)	23:20	0x0	Channel A data and mask read back strength P driver 　0=Minimum strength 　15=Maximum strength
MCA_STR_READ_BACK_P_DQS (R)	27:24	0x0	Channel A strobe (nominal and complement) read back strength P driver 　0=Minimum strength 　15=Maximum strength
MCA_STR_READ_BACK_P_XXX (R)	31:28	0x0	Channel A spare read back strength P driver 　0=Minimum strength 　15=Maximum strength
Memory controller A strength P read back			

MCA_PREAMP - RW - 32 bits - NBMCIND:0xBD			
Field Name	**Bits**	**Default**	**Description**
MCA_PREAMP_EN_CK	0	0x1	Channel A clock (nominal and complement) preamplification enable 　0=Preamplification disabled 　1=Preamplification enabled
MCA_PREAMP_ALWAYS_CK	1	0x1	Channel A clock (nominal and complement) preamplification always on when enabled 　0=Preamplification conditional 　1=Preamplification always on
MCA_PREAMP_HALF_CLK_CK	2	0x0	Channel A clock (nominal and complement) preamplification duration, if enabled and not always on 　0=Preamplification for one 2x clock 　1=Preamplification for half 2x clock
MCA_PREAMP_TWO_CLK_CK	3	0x0	Channel A clock (nominal and complement) preamplification condition, if enabled and not always on 　0=Preamplification when signal stable for one 1x clock 　1=Preamplification when signal stable for two 1x clock
MCA_PREAMP_EN_CKE	4	0x1	Channel A CKE preamplification enable 　0=Preamplification disabled 　1=Preamplification enabled

MCA_PREAMP_ALWAYS_CKE	5	0x1	Channel A CKE preamplification always on when enabled
			    0=Preamplification conditional
			    1=Preamplification always on

MCA_PREAMP_HALF_CLK_CKE	6	0x0	Channel A CKE preamplification duration, if enabled and not always on
			    0=Preamplification for one 2x clock
			    1=Preamplification for half 2x clock

MCA_PREAMP_TWO_CLK_CKE	7	0x0	Channel A CKE preamplification condition, if enabled and not always on
			    0=Preamplification when signal stable for one 1x clock
			    1=Preamplification when signal stable for two 1x clock

MCA_PREAMP_EN_CS	8	0x1	Channel A CS preamplification enable
			    0=Preamplification disabled
			    1=Preamplification enabled

MCA_PREAMP_ALWAYS_CS	9	0x1	Channel A CS preamplification always on when enabled
			    0=Preamplification conditional
			    1=Preamplification always on

MCA_PREAMP_HALF_CLK_CS	10	0x0	Channel A CS preamplification duration, if enabled and not always on
			    0=Preamplification for one 2x clock
			    1=Preamplification for half 2x clock

MCA_PREAMP_TWO_CLK_CS	11	0x0	Channel A CS preamplification condition, if enabled and not always on
			    0=Preamplification when signal stable for one 1x clock
			    1=Preamplification when signal stable for two 1x clock

MCA_PREAMP_EN_CMD	12	0x1	Channel A RAS/CAS/WE and address preamplification enable
			    0=Preamplification disabled
			    1=Preamplification enabled

MCA_PREAMP_ALWAYS_CMD	13	0x1	Channel A RAS/CAS/WE and address preamplification always on when enabled
			    0=Preamplification conditional
			    1=Preamplification always on

MCA_PREAMP_HALF_CLK_CMD	14	0x0	Channel A RAS/CAS/WE and address preamplification duration, if enabled and not always on
			    0=Preamplification for one 2x clock
			    1=Preamplification for half 2x clock

MCA_PREAMP_TWO_CLK_CMD	15	0x0	Channel A RAS/CAS/WE and address preamplification condition, if enabled and not always on
			    0=Preamplification when signal stable for one 1x clock
			    1=Preamplification when signal stable for two 1x clock

MCA_PREAMP_EN_ODT	16	0x1	Channel A ODT preamplification enable
			    0=Preamplification disabled
			    1=Preamplification enabled

MCA_PREAMP_ALWAYS_ODT	17	0x1	Channel A ODT preamplification always on when enabled
			    0=Preamplification conditional
			    1=Preamplification always on

MCA_PREAMP_HALF_CLK_ODT	18	0x0	Channel A ODT preamplification duration, if enabled and not always on
			    0=Preamplification for one 2x clock
			    1=Preamplification for half 2x clock

MCA_PREAMP_TWO_CLK_ODT	19	0x0	Channel A ODT preamplification condition, if enabled and not always on
			    0=Preamplification when signal stable for one 1x clock
			    1=Preamplification when signal stable for two 1x clock

MCA_PREAMP_EN_DQ	20	0x1	Channel A data and mask preamplification enable
			    0=Preamplification disabled
			    1=Preamplification enabled

MCA_PREAMP_ALWAYS_DQ	21	0x1	Channel A data and mask preamplification always on when enabled 0=Preamplification conditional 1=Preamplification always on
MCA_PREAMP_HALF_CLK_DQ	22	0x0	Channel A data and mask preamplification duration, if enabled and not always on 0=Preamplification for one 2x clock 1=Preamplification for half 2x clock
MCA_PREAMP_TWO_CLK_DQ	23	0x0	Channel A data and mask preamplification condition, if enabled and not always on 0=Preamplification when signal stable for one 1x clock 1=Preamplification when signal stable for two 1x clock
MCA_PREAMP_EN_DQS	24	0x1	Channel A strobe (nominal and complement) preamplification enable 0=Preamplification disabled 1=Preamplification enabled
MCA_PREAMP_ALWAYS_DQS	25	0x1	Channel A strobe (nominal and complement) preamplification always on when enabled 0=Preamplification conditional 1=Preamplification always on
MCA_PREAMP_HALF_CLK_DQS	26	0x0	Channel A strobe (nominal and complement) preamplification duration, if enabled and not always on 0=Preamplification for one 2x clock 1=Preamplification for half 2x clock
MCA_PREAMP_TWO_CLK_DQS	27	0x0	Channel A clock strobe (nominal and complement) preamplification condition, if enabled and not always on 0=Preamplification when signal stable for one 1x clock 1=Preamplification when signal stable for two 1x clock
MCA_PREAMP_EN_XXX	28	0x1	Channel A XXX preamplification enable 0=Preamplification disabled 1=Preamplification enabled
MCA_PREAMP_ALWAYS_XXX	29	0x1	Channel A XXX preamplification always on when enabled 0=Preamplification conditional 1=Preamplification always on
MCA_PREAMP_HALF_CLK_XXX	30	0x0	Channel A XXX preamplification duration, if enabled and not always on 0=Preamplification for one 2x clock 1=Preamplification for half 2x clock
MCA_PREAMP_TWO_CLK_XXX	31	0x0	Channel A XXX preamplification condition, if enabled and not always on 0=Preamplification when signal stable for one 1x clock 1=Preamplification when signal stable for two 1x clock
Memory controller A driver preamplification control			

MCA_PREAMP_N - RW - 32 bits - NBMCIND:0xBE			
Field Name	**Bits**	**Default**	**Description**
MCA_PREAMP_N_CK	3:0	0xb	Channel A clock (nominal and complement) preamp strength N driver 0=Minimum strength 15=Maximum strength
MCA_PREAMP_N_CKE	7:4	0xb	Channel A CKE preamp strength N driver 0=Minimum strength 15=Maximum strength
MCA_PREAMP_N_CS	11:8	0xb	Channel A CS preamp strength N driver 0=Minimum strength 15=Maximum strength
MCA_PREAMP_N_CMD	15:12	0xb	Channel A RAS/CAS/WE and address preamp strength N driver 0=Minimum strength 15=Maximum strength
MCA_PREAMP_N_ODT	19:16	0xb	Channel A ODT preamp strength N driver 0=Minimum strength 15=Maximum strength
MCA_PREAMP_N_DQ	23:20	0xb	Channel A data and mask preamp strength N driver 0=Minimum strength 15=Maximum strength
MCA_PREAMP_N_DQS	27:24	0xb	Channel A strobe (nominal and complement) preamp strength N driver 0=Minimum strength 15=Maximum strength
MCA_PREAMP_N_XXX	31:28	0xb	Channel A spare preamp strength N driver 0=Minimum strength 15=Maximum strength
Memory controller A preamp strength N			

MCA_PREAMP_P - RW - 32 bits - NBMCIND:0xBF			
Field Name	**Bits**	**Default**	**Description**

MCA_PREAMP_P_CK	3:0	0xb	Channel A clock (nominal and complement) preamp strength P driver
			  0=Minimum strength
			  15=Maximum strength

MCA_PREAMP_P_CKE	7:4	0xb	Channel A CKE preamp strength P driver
			  0=Minimum strength
			  15=Maximum strength

MCA_PREAMP_P_CS	11:8	0xb	Channel A CS preamp strength P driver
			  0=Minimum strength
			  15=Maximum strength

MCA_PREAMP_P_CMD	15:12	0xb	Channel A RAS/CAS/WE and address preamp strength P driver
			  0=Minimum strength
			  15=Maximum strength

MCA_PREAMP_P_ODT	19:16	0xb	Channel A ODT preamp strength P driver
			  0=Minimum strength
			  15=Maximum strength

MCA_PREAMP_P_DQ	23:20	0xb	Channel A data and mask preamp strength P driver
			  0=Minimum strength
			  15=Maximum strength

MCA_PREAMP_P_DQS	27:24	0xb	Channel A strobe (nominal and complement) preamp strength P driver
			  0=Minimum strength
			  15=Maximum strength

MCA_PREAMP_P_XXX	31:28	0xb	Channel A spare preamp strength P driver
			  0=Minimum strength
			  15=Maximum strength

Memory controller A preamp strength P			

MCA_PREAMP_STEP - RW - 32 bits - NBMCIND:0xC0			
Field Name	**Bits**	**Default**	**Description**

MCA_PRE_STEP_N_CK	1:0	0x1	Channel A clock (nominal and complement) impedance controller adjustment step for strength N driver
			  0=0 step, no adjustment
			  1=1 step, adjustment the same as reference
			  2=2 step, higher than reference adjustment
			  3=3 step, higher than reference adjustment

MCA_PRE_STEP_P_CK	3:2	0x1	Channel A clock (nominal and complement) impedance controller adjustment step for strength P driver
			  0=0 step, no adjustment
			  1=1 step, adjustment the same as reference
			  2=2 step, higher than reference adjustment
			  3=3 step, higher than reference adjustment

MCA_PRE_STEP_N_CKE	5:4	0x1	Channel A CKE impedance controller adjustment step for strength N driver
			  0=0 step, no adjustment
			  1=1 step, adjustment the same as reference
			  2=2 step, higher than reference adjustment
			  3=3 step, higher than reference adjustment

MCA_PRE_STEP_P_CKE	7:6	0x1	Channel A CKE impedance controller adjustment step for strength P driver
			  0=0 step, no adjustment
			  1=1 step, adjustment the same as reference
			  2=2 step, higher than reference adjustment
			  3=3 step, higher than reference adjustment

MCA_PRE_STEP_N_CS	9:8	0x1	Channel A CS impedance controller adjustment step for strength N driver
			  0=0 step, no adjustment
			  1=1 step, adjustment the same as reference
			  2=2 step, higher than reference adjustment
			  3=3 step, higher than reference adjustment

MCA_PRE_STEP_P_CS	11:10	0x1	Channel A CS impedance controller adjustment step for strength P driver
			  0=0 step, no adjustment
			  1=1 step, adjustment the same as reference
			  2=2 step, higher than reference adjustment
			  3=3 step, higher than reference adjustment

MCA_PRE_STEP_N_CMD	13:12	0x1	Channel A RAS/CAS/WE and address impedance controller adjustment step for strength N driver
			  0=0 step, no adjustment
			  1=1 step, adjustment the same as reference
			  2=2 step, higher than reference adjustment
			  3=3 step, higher than reference adjustment

MCA_PRE_STEP_P_CMD	15:14	0x1	Channel A RAS/CAS/WE and address impedance controller adjustment step for strength P driver
			  0=0 step, no adjustment
			  1=1 step, adjustment the same as reference
			  2=2 step, higher than reference adjustment
			  3=3 step, higher than reference adjustment

MCA_PRE_STEP_N_ODT	17:16	0x1	Channel A ODT impedance controller adjustment step for strength N driver
			  0=0 step, no adjustment
			  1=1 step, adjustment the same as reference
			  2=2 step, higher than reference adjustment
			  3=3 step, higher than reference adjustment

MCA_PRE_STEP_P_ODT	19:18	0x1	Channel A ODT impedance controller adjustment step for strength P driver
			  0=0 step, no adjustment
			  1=1 step, adjustment the same as reference
			  2=2 step, higher than reference adjustment
			  3=3 step, higher than reference adjustment

MCA_PRE_STEP_N_DQ	21:20	0x1	Channel A data and mask impedance controller adjustment step for strength N driver
			  0=0 step, no adjustment
			  1=1 step, adjustment the same as reference
			  2=2 step, higher than reference adjustment
			  3=3 step, higher than reference adjustment

MCA_PRE_STEP_P_DQ	23:22	0x1	Channel A data and mask impedance controller adjustment step for strength P driver
			  0=0 step, no adjustment
			  1=1 step, adjustment the same as reference
			  2=2 step, higher than reference adjustment
			  3=3 step, higher than reference adjustment

MCA_PRE_STEP_N_DQS	25:24	0x1	Channel A strobe (nominal and complement) impedance controller adjustment step for strength N driver
			  0=0 step, no adjustment
			  1=1 step, adjustment the same as reference
			  2=2 step, higher than reference adjustment
			  3=3 step, higher than reference adjustment

MCA_PRE_STEP_P_DQS	27:26	0x1	Channel A strobe (nominal and complement) impedance controller adjustment step for strength P driver
			  0=0 step, no adjustment
			  1=1 step, adjustment the same as reference
			  2=2 step, higher than reference adjustment
			  3=3 step, higher than reference adjustment

MCA_PRE_STEP_N_XXX	29:28	0x1	Channel A spare impedance controller adjustment step for strength N driver
			  0=0 step, no adjustment
			  1=1 step, adjustment the same as reference
			  2=2 step, higher than reference adjustment
			  3=3 step, higher than reference adjustment

MCA_PRE_STEP_P_XXX	31:30	0x1	Channel A spare impedance controller adjustment step for strength P driver
			  0=0 step, no adjustment
			  1=1 step, adjustment the same as reference
			  2=2 step, higher than reference adjustment
			  3=3 step, higher than reference adjustment

Memory controller A impedance controller adjustment step for preamp			

MCA_PREBUF_SLEW_N - RW - 32 bits - NBMCIND:0xC1			
Field Name	**Bits**	**Default**	**Description**

MCA_PREBUF_SLEW_N_CK	3:0	0x0	Channel A clock (nominal and complement) prebuffer slew N control
			  0=Slow edge
			  15=Fast edge

MCA_PREBUF_SLEW_N_CKE	7:4	0x0	Channel A CKE prebuffer slew N control
			  0=Slow edge
			  15=Fast edge

MCA_PREBUF_SLEW_N_CS	11:8	0x0	Channel A CS prebuffer slew N control
			  0=Slow edge
			  15=Fast edge

MCA_PREBUF_SLEW_N_CMD	15:12	0x0	Channel A RAS/CAS/WE and address prebuffer slew N control
			  0=Slow edge
			  15=Fast edge

MCA_PREBUF_SLEW_N_ODT	19:16	0x0	Channel A ODT prebuffer slew N control
			  0=Slow edge
			  15=Fast edge

MCA_PREBUF_SLEW_N_DQ	23:20	0x0	Channel A data and mask prebuffer slew N control
			  0=Slow edge
			  15=Fast edge

MCA_PREBUF_SLEW_N_DQS	27:24	0x0	Channel A strobe (nominal and complement) prebuffer slew N control
			  0=Slow edge
			  15=Fast edge

MCA_PREBUF_SLEW_N_XXX	31:28	0x0	Channel A spare prebuffer slew N control
			  0=Slow edge
			  15=Fast edge

Channel A prebuffer slew N control			

MCA_PREBUF_SLEW_P - RW - 32 bits - NBMCIND:0xC2			
Field Name	**Bits**	**Default**	**Description**
MCA_PREBUF_SLEW_P_CK	3:0	0x0	Channel A clock (nominal and complement) prebuffer slew P control 　0=Slow edge 　15=Fast edge
MCA_PREBUF_SLEW_P_CKE	7:4	0x0	Channel A CKE prebuffer slew P control 　0=Slow edge 　15=Fast edge
MCA_PREBUF_SLEW_P_CS	11:8	0x0	Channel A CS prebuffer slew P control 　0=Slow edge 　15=Fast edge
MCA_PREBUF_SLEW_P_CMD	15:12	0x0	Channel A RAS/CAS/WE and address prebuffer slew P control 　0=Slow edge 　15=Fast edge
MCA_PREBUF_SLEW_P_ODT	19:16	0x0	Channel A ODT prebuffer slew P control 　0=Slow edge 　15=Fast edge
MCA_PREBUF_SLEW_P_DQ	23:20	0x0	Channel A data and mask prebuffer slew P control 　0=Slow edge 　15=Fast edge
MCA_PREBUF_SLEW_P_DQS	27:24	0x0	Channel A strobe (nominal and complement) prebuffer slew P control 　0=Slow edge 　15=Fast edge
MCA_PREBUF_SLEW_P_XXX	31:28	0x0	Channel A spare prebuffer slew P control 　0=Slow edge 　15=Fast edge
Channel A prebuffer slew P control			

MCA_GENERAL_PURPOSE - RW - 32 bits - NBMCIND:0xC3			
Field Name	**Bits**	**Default**	**Description**
MCA_TRST_FORCE	0	0x0	Channel A all signals tristate force 　0=Nominal 　1=Tristate
MCA_TRST_DYNAMIC	1	0x0	Channel A all signals tristate when dynamic CKE low, except clock running and ODT low 　0=Nominal 　1=Tristate
MCA_TRST_CK	2	0x0	Channel A tristate clock when tristate dynamic CKE low 　0=Nominal 　1=Tristate
MCA_TRST_DLL	3	0x0	Channel A reset memory DLL after exiting tristate dynamic CKE low with clock tristate 　0=Do not reset memory DLL 　1=Reset memory DLL
MCA_TRST_SELFREF	4	0x0	Channel A enter self refresh when tristate dynamic CKE low 　0=Do not do anything 　1=Enter self refresh
MCA_DQ_DQS_FORCE_TERM	5	0x0	Channel A force ASIC DQ and DQS pads termination force 　0=Nominal operation, termination on during read only 　1=Termination on always

MCA_DQ_DQS_FORCE_LOW	6	0x0	Channel A force ASIC DQ and DQS pads drive low
			   0=Nominal operation
			   1=Force drive low DQ/DQS

MCA_DQ_DQS_FORCE_HIGH	7	0x0	Channel A force ASIC DQ and DQS pads drive high
			   0=Nominal operation
			   1=Force drive high DQ/DQS

MCA_DLL_PWRDN	8	0x1	Channel A all DLL master power down
MCA_DLL_RESET	9	0x1	Channel A all DLL master reset
MCA_DLL_TEST	10	0x0	Channel A all DLL master test
MCA_REF_DISABLE	11	0x1	Disables refreshing when set
MCA_REF_URGENCY	15:12	0x6	Number of pending refreshes until refresh becomes urgent.
MCA_IO_BIAS_CK	16	0x0	Enables MC IO CK bias current.
MCA_IO_BIAS_CKE	17	0x0	Enables MC IO CKE bias current.
MCA_IO_BIAS_CS	18	0x0	Enables MC IO CS bias current.
MCA_IO_BIAS_CMD	19	0x0	Enables MC IO CMD bias current.
MCA_IO_BIAS_ODT	20	0x0	Enables MC IO ODT bias current.
MCA_IO_BIAS_DQ	21	0x0	Enables MC IO DQ bias current.
MCA_IO_BIAS_DQS	22	0x0	Enables MC IO DQS bias current.
MCA_IO_BIAS_XXX	23	0x0	Enables MC IO XXX bias current.
MCA_REF_HI_PRI	24	0x0	Enables hi priority refreshes.
MCA_OE_CKE	25	0x1	Enables MC IO CKE OE: 0 = tristate CKE, 1 = output CKE
MCA_OE_ODT	26	0x1	Enables MC IO CKE ODT: 0 = tristate CKE, 1 = output ODT
RESERVED25	31:27	0x0	
Memory controller A general purpose control			

MCA_GENERAL_PURPOSE_2 - RW - 32 bits - NBMCIND:0xC4

Field Name	Bits	Default	Description
RESERVED	31:0	0x0	
Memory controller A general purpose control 2			

MCA_OCD_CONTROL - RW - 32 bits - NBMCIND:0xC5

Field Name	Bits	Default	Description
MCA_OCD_CONTROL_BYTE0	3:0	0x0	Channel A OCD control data BYTE 0
MCA_OCD_CONTROL_BYTE1	7:4	0x0	Channel A OCD control data BYTE 0
MCA_OCD_CONTROL_BYTE2	11:8	0x0	Channel A OCD control data BYTE 0
MCA_OCD_CONTROL_BYTE3	15:12	0x0	Channel A OCD control data BYTE 0
MCA_OCD_CONTROL_BYTE4	19:16	0x0	Channel A OCD control data BYTE 0
MCA_OCD_CONTROL_BYTE5	23:20	0x0	Channel A OCD control data BYTE 0
MCA_OCD_CONTROL_BYTE6	27:24	0x0	Channel A OCD control data BYTE 0
MCA_OCD_CONTROL_BYTE7	31:28	0x0	Channel A OCD control data BYTE 0
Memory controller A OCD control data			

MCA_DQ_DQS_READ_BACK - RW - 32 bits - NBMCIND:0xC6			
Field Name	**Bits**	**Default**	**Description**
MCA_READ_BACK_BYTE0 (R)	0	0x0	Channel A read back data byte 0 0=All 0 when OCD drive 0, some 0 when OCD drive 1 1=Some 1 when OCD drive 0, all 1 when OCD drive 1
MCA_READ_BACK_BYTE1 (R)	1	0x0	Channel A read back data byte 1 0=All 0 when OCD drive 0, some 0 when OCD drive 1 1=Some 1 when OCD drive 0, all 1 when OCD drive 1
MCA_READ_BACK_DQS0 (R)	8	0x0	Channel A read back strobe byte 0 0=0 1=1
MCA_READ_BACK_DQS1 (R)	9	0x0	Channel A read back strobe byte 1 0=0 1=1
MCA_READ_BACK_DQ_LSB (R)	23:16	0x0	Channel A read back data LSB bits 7:0 0=0 1=1
MCA_READ_BACK_DQ_MSB (R)	31:24	0x0	Channel A read back data MSB bits 15:8 0=0 1=1
Memory controller A data and strobe read back			

MCA_DQS_CLK_READ_BACK - RW - 32 bits - NBMCIND:0xC7			
Field Name	**Bits**	**Default**	**Description**
MCA_SAMPLE_RISE1_DQS0 (R)	0	0x0	Channel A read strobe 0 sampled with first internal clock rising edge.
MCA_SAMPLE_FALL1_DQS0 (R)	1	0x0	Channel A read strobe 0 sampled with first internal clock falling edge.
MCA_SAMPLE_RISE2_DQS0 (R)	2	0x0	Channel A read strobe 0 sampled with second internal clock rising edge.
MCA_SAMPLE_FALL2_DQS0 (R)	3	0x0	Channel A read strobe 0 sampled with second internal clock falling edge.
MCA_SAMPLE_RISE1_DQS1 (R)	4	0x0	Channel A read strobe 1 sampled with first internal clock rising edge.
MCA_SAMPLE_FALL1_DQS1 (R)	5	0x0	Channel A read strobe 1 sampled with first internal clock falling edge.
MCA_SAMPLE_RISE2_DQS1 (R)	6	0x0	Channel A read strobe 1 sampled with second internal clock rising edge.
MCA_SAMPLE_FALL2_DQS1 (R)	7	0x0	Channel A read strobe 1 sampled with second internal clock falling edge.
MCA_SAMPLE_RISE1_DQS2 (R)	8	0x0	Channel A read strobe 2 sampled with first internal clock rising edge.
MCA_SAMPLE_FALL1_DQS2 (R)	9	0x0	Channel A read strobe 2 sampled with first internal clock falling edge.
MCA_SAMPLE_RISE2_DQS2 (R)	10	0x0	Channel A read strobe 2 sampled with second internal clock rising edge.
MCA_SAMPLE_FALL2_DQS2 (R)	11	0x0	Channel A read strobe 2 sampled with second internal clock falling edge.
MCA_SAMPLE_RISE1_DQS3 (R)	12	0x0	Channel A read strobe 3 sampled with first internal clock rising edge.
MCA_SAMPLE_FALL1_DQS3 (R)	13	0x0	Channel A read strobe 3 sampled with first internal clock falling edge.
MCA_SAMPLE_RISE2_DQS3 (R)	14	0x0	Channel A read strobe 3 sampled with second internal clock rising edge.

MCA_SAMPLE_FALL2_DQS3 (R)	15	0x0	Channel A read strobe 3 sampled with second internal clock falling edge.
MCA_SAMPLE_RISE1_DQS4 (R)	16	0x0	Channel A read strobe 4 sampled with first internal clock rising edge.
MCA_SAMPLE_FALL1_DQS4 (R)	17	0x0	Channel A read strobe 4 sampled with first internal clock falling edge.
MCA_SAMPLE_RISE2_DQS4 (R)	18	0x0	Channel A read strobe 4 sampled with second internal clock rising edge.
MCA_SAMPLE_FALL2_DQS4 (R)	19	0x0	Channel A read strobe 4 sampled with second internal clock falling edge.
MCA_SAMPLE_RISE1_DQS5 (R)	20	0x0	Channel A read strobe 5 sampled with first internal clock rising edge.
MCA_SAMPLE_FALL1_DQS5 (R)	21	0x0	Channel A read strobe 5 sampled with first internal clock falling edge.
MCA_SAMPLE_RISE2_DQS5 (R)	22	0x0	Channel A read strobe 5 sampled with second internal clock rising edge.
MCA_SAMPLE_FALL2_DQS5 (R)	23	0x0	Channel A read strobe 5 sampled with second internal clock falling edge.
MCA_SAMPLE_RISE1_DQS6 (R)	24	0x0	Channel A read strobe 6 sampled with first internal clock rising edge.
MCA_SAMPLE_FALL1_DQS6 (R)	25	0x0	Channel A read strobe 6 sampled with first internal clock falling edge.
MCA_SAMPLE_RISE2_DQS6 (R)	26	0x0	Channel A read strobe 6 sampled with second internal clock rising edge.
MCA_SAMPLE_FALL2_DQS6 (R)	27	0x0	Channel A read strobe 6 sampled with second internal clock falling edge.
MCA_SAMPLE_RISE1_DQS7 (R)	28	0x0	Channel A read strobe 7 sampled with first internal clock rising edge.
MCA_SAMPLE_FALL1_DQS7 (R)	29	0x0	Channel A read strobe 7 sampled with first internal clock falling edge.
MCA_SAMPLE_RISE2_DQS7 (R)	30	0x0	Channel A read strobe 7 sampled with second internal clock rising edge.
MCA_SAMPLE_FALL2_DQS7 (R)	31	0x0	Channel A read strobe 7 sampled with second internal clock falling edge.
Memory controller A read strobe sampled by internal clock read back			

MCA_MEMORY_INIT_MRS_PM - RW - 32 bits - NBMCIND:0xC8			
Field Name	**Bits**	**Default**	**Description**

MCA_MODE_REG_PM	19:0	0x0	Value to be loaded in memory mode register in power management mode.
			  [14:0]=Address [14:0]
			  [15]=Reserved
			  [18:16]=Bank [2:0]
			  [19]=Reserved

MCA_INIT_CS_MRS_PM	23:20	0xf	Channel A CS to be initialized in power management mode.
			  4'b0001=CS0/
			  4'b0010= CS1/
			  4'b0100=CS2/
			  4'b1000=CS3/

MCA_DQ_TRANSFER_PM	27:24	0x4	Channel N read data transfer from strobe flops to core clock flops in power management mode.n 0 = CL+0clock
			  1=CL+1clock
			  2=CL+2clock
			  3=CL+3clock
			  4=CL+4clock

MCA_REF_URGENCY_PM	31:28	0x6	Number of pending refreshes until refresh becomes urgent in power management mode.
Memory controller power management control MRS			

MCA_MEMORY_INIT_EMRS_PM - RW - 32 bits - NBMCIND:0xC9			
Field Name	**Bits**	**Default**	**Description**

MCA_EXT_MODE_REG_PM	19:0	0x10000	Value to be loaded in memory extended mode register in power management mode.
			  [14:0] = Address [14:0]
			  [15] = Reserved
			  [18:16] = Bank [2:0]
			  [19] = Reserved

MCA_INIT_CS_EMRS_PM	23:20	0xf	Channel A CS to be initialized in power management mode.
			  4'b0001=CS0/
			  4'b0010=CS1/
			  4'b0100=CS2/
			  4'b1000=CS3/

MCA_INIT_DLL_PM	24	0x1	Enables execution of memory DLL reset mode register command for power management mode initialization sequence

MCA_CKE_DYNAMIC_PM	25	0x0	Channel A CKE dynamic in power management
			  0=CKE high when enabled
			  1=CKE dynamic when enabled, high or low depending on activity, active or precharge power down

MCA_TRST_DYNAMIC_PM	26	0x0	Channel A all signals tristate when CKE low, except clock running and ODT low, active and precharge power down in power management mode
			  0=Nominal
			  1=Tristate

MCA_TRST_CK_PM	27	0x0	Channel A tristate clock when tristate dynamic CKE low in power management mode
			  0=Nominal
			  1=Tristate

MCA_TRST_SELFREF_PM	28	0x0	Channel A enter self refresh when tristate dynamic CKE low in power management mode
			  0=Do not do anything
			  1=Enter self refresh

MCA_ODT_STALL_PM	29	0x0	Channel A ODT stall first write in power management mode
			  0=No stall
			  1=Stall

MCA_2T_TIMING_PM	30	0x0	Channel A timing in power management mode.
			  0=1T timing
			  1=2T timing

MCA_3T_TIMING_PM	31	0x0	Channel A timing in power management mode.
			  0=1T timing
			  1=3T timing

Memory controller power management control EMRS			

MCA_MEMORY_INIT_EMRS2_PM - RW - 32 bits - NBMCIND:0xCA			
Field Name	**Bits**	**Default**	**Description**

MCA_EXT2_MODE_REG_PM	19:0	0x20000	Value to be loaded in memory extended mode register in power management mode.
			  [14:0]=Address [14:0]
			  [15]=Reserved
			  [18:16]=Bank [2:0]
			  [19]=Reserved

MCA_INIT_CS_EMRS2_PM	23:20	0xf	Channel A CS to be initialized in power management mode.
			  4'b0001=CS0/
			  4'b0010=CS1/
			  4'b0100=CS2/
			  4'b1000=CS3/

MCA_ODTR_POSITION_PM	25:24	0x0	Channel A ODT read position
			When ODTX 0, read latency dependent
			When ODTX 1, read command dependent
			  0=ODT start at RL-3 for ODTX 0, ODT start at RD for ODTX1
			  1=ODT start at RL-2 for ODTX 0, ODT start at RD+1 for ODTX 1
			  2/3=1 clock later

MCA_ODTW_POSITION_PM	27:26	0x0	Channel A ODT write position
			When ODTX 0, write latency dependent
			When ODTX 1, write command dependent
			  0=ODT start at WL-3 for ODTX 0, ODT start at WR for ODTX1
			  1=ODT start at WL-2 for ODTX 0, ODT start at WR+1 for ODTX 1
			  2/3=1 clock later

RESERVED28	31:28	0x0	
Memory controller power management control EMRS2			

MCA_MEMORY_INIT_EMRS3_PM - RW - 32 bits - NBMCIND:0xCB			
Field Name	**Bits**	**Default**	**Description**
MCA_EXT3_MODE_REG_PM	19:0	0x30000	Value to be loaded in memory extended mode register in power management mode. [14:0]=Address [14:0] [15]=Reserved [18:16]=Bank [2:0] [19]=Reserved
MCA_INIT_CS_EMRS3_PM	23:20	0xf	Channel A CS to be initialized in power management mode. 4'b0001=CS0/ 4'b0010=CS1/ 4'b0100=CS2/ 4'b1000=CS3/
RESERVED24	31:24	0x0	
Memory controller power management control EMRS3			

MCA_TIMING_PARAMETERS_1_PM - RW - 32 bits - NBMCIND:0xCC			
Field Name	**Bits**	**Default**	**Description**
MCA_RD_LAT_PM	3:0	0x4	Memory CAS Latency 0=0 clock (not supported) 1=1 clock (not supported) 2=2 clock 3=3 clock 4=4 clock 5=5 clock 6=6 clock 7=7 clock
MCA_WR_LAT_PM	7:4	0x3	Memory Write Latency 0=0 clock (not supported) 1=1 clock 2=2 clock 3=3 clock 4=4 clock 5=5 clock 6=6 clock 7=7 clock
MCA_TRCDR_PM	11:8	0x8	Active to Read delay 0=0 clock 1=1 clock 2=2 clock 3=3 clock … 13=13 clock 14=14 clock 15=15 clock

MCA_TRCDW_PM	15:12	0x8	Active to Write delay 0=0 clock 1=1 clock 2=2 clock 3=3 clock … 13=13 clock 14=14 clock 15=15 clock
MCA_TRP_PM	19:16	0x8	Precharge command period 0=0 clock 1=1 clock 2=2 clock 3=3 clock … 13=13 clock 14=14 clock 15=15 clock
MCA_TRTP_PM	23:20	0x4	Internal Read to Precharge command delay 0=0 clock 1=1 clock 2=2 clock 3=3 clock 4=4 clock 5=5 clock 6=6 clock 7=7 clock
MCA_TWR_PM	27:24	0x8	Write recovery time 0=0 clock 1=1 clock 2=2 clock 3=3 clock … 13=13 clock 14=14 clock 15=15 clock
MCA_TRRD_PM	31:28	0x6	Active bank A to Active bank B command period 0=0 clock 1=1 clock 2=2 clock 3=3 clock 4=4 clock 5=5 clock 6=6 clock 7=7 clock
Memory controller A timing parameters in power management mode, set 1			

MCA_TIMING_PARAMETERS_2_PM - RW - 32 bits - NBMCIND:0xCD			
Field Name	**Bits**	**Default**	**Description**

MCA_TRAS_PM	7:0	0x18	Active to Precharge command
			   0=0 clock
			   1= clock
			   2=2 clock
			   3=3 clock
			
			   …
			   29=29 clock
			   30=30 clock
			   31=31 clock

MCA_TRC_PM	15:8	0x20	Row Cycle time, Active to Active/Auto-Refresh command period
			   0=0 clock
			   1=1 clock
			   2=2 clock
			   3=3 clock
			
			   …
			   125=125 clock
			   126=126 clock
			   127=127 clock

MCA_TRFC_PM	23:16	0x28	Auto-Refresh to Active/Auto-Refresh command period
			   0=0 clock
			   1=1 clock
			   2=2 clock
			   3=3 clock
			
			   …
			   125=125 clock
			   126=126 clock
			   127=127 clock

MCA_TREFI_PM	31:24	0x10	1 memory refresh is performed every TREFI*64 MCLK cycles.
Memory controller A timing parameters in power management mode, set 2			

MCA_TIMING_PARAMETERS_3_PM - RW - 32 bits - NBMCIND:0xCE			
Field Name	**Bits**	**Default**	**Description**
MCA_TRTR_CS_PM	3:0	0x1	Read to Read command to different CS 0=0 clock 1=1 clock 2=2 clock 3=3 clock 4=4 clock 5=5 clock 6=6 clock 7=7 clock
MCA_TRTW_PM	7:4	0x2	Read to Write bus turnaround 0=0 clock 1=1 clock 2=2 clock 3=3 clock 4=4 clock 5=5 clock 6=6 clock 7=7 clock
MCA_TWTR_PM	11:8	0x4	Internal Write to Read command delay 0=0 clock 1=1 clock 2=2 clock 3=3 clock 4=4 clock 5=5 clock 6=6 clock 7=7 clock
MCA_TWTR_CS_PM	15:12	0x2	Write to Read command to different CS 0=0 clock 1=1 clock 2=2 clock 3=3 clock 4=4 clock 5=5 clock 6=6 clock 7=7 clock
MCA_TWTW_CS_PM	19:16	0x1	Write to Write command to different CS 0=0 clock 1=1 clock 2=2 clock 3=3 clock 4=4 clock 5=5 clock 6=6 clock 7=7 clock
MCA_TCCD_PM	23:20	0x2	CAS to CAS command delay 0=0 clock 1=1 clock 2=2 clock 3=3 clock … 13=13 clock 14=14 clock 15=15 clock

MCA_TCKE_PM	27:24	0x3	CKE minimum high and low pulse width
			0=0 clock
			1=1 clock
			2=2 clock
			3=3 clock
			4=4 clock
			5=5 clock
			6=6 clock
			7=7 clock
MCA_TXP_PM	31:28	0x3	Exit precharge power down to any valid command
			0=0 clock
			1=1 clock
			2=2 clock
			3=3 clock
			4=4 clock
			5=5 clock
			6=6 clock
			7=7 clock
Memory controller A timing parameters in power management mode, set 3			

MCA_TIMING_PARAMETERS_4_PM - RW - 32 bits - NBMCIND:0xCF			
Field Name	**Bits**	**Default**	**Description**
MCA_TXARDS_PM	3:0	0x6	Exit active power down to read command
			0=0 clock
			1=1 clock
			2=2 clock
			3=3 clock
			…
			13=13 clock
			14=14 clock
			15=15 clock
MCA_TAXPD_PM	7:4	0x8	ODT power down exit latency
			0=0 clock
			1=1 clock
			2=2 clock
			3=3 clock
			…
			13=13 clock
			14=14 clock
			15=15 clock
MCA_TRPALL_PM	11:8	0x2	Precharge all for 8 bank memories
			0=0 clock
			1=1 clock
			2=2 clock
			3=3 clock
			…
			13=13 clock
			14=14 clock
			15=15 clock

MCA_TFAW_PM	15:12	0x2	Back to back activate rolling window
			  0=0 clock
			  1=1 clock
			  2=2 clock
			  3=3 clock
			  …
			  13=13 clock
			  14=14 clock
			  15=15 clock

MCA_TZQCL_PM	19:16	0x8	Impedance calibration long timing, can be merged with DLL time, x64 clocks.
MCA_TZQCS_PM	23:20	0x4	Impedance calibration short timing, x16 clocks.
MCA_TZQCI_PM	27:24	0x1	Impedance calibration interval, x256 refresh cycles.

MCA_TMRD_PM	31:28	0x2	Mode register set command cycle time
			  0=0 clock
			  1=1 clock
			  ...
			  15=15 clock

Memory controller A timing parameters in power management mode, set 4			

MCA_IN_TIMING_DQS_3210_PM - RW - 32 bits - NBMCIND:0xD0			
Field Name	**Bits**	**Default**	**Description**

MCA_DQS_ARRIVAL_0_PM	4:0	0x6	Channel A byte 0 input strobe reset removal edge in power management mode
			  0=CL
			  1=CL+0.25
			  2=CL+0.50
			  3=CL+0.75
			  4=CL+1.00
			  5=CL+1.25
			  6=CL+1.50
			  7=CL+1.75
			  8=CL+2.00
			  9=CL+2.25
			  10=CL+2.50
			  11=CL+2.75
			  12=CL+3.00
			  13=CL+3.25
			  14=CL+3.50
			  15=CL+3.75
			  16=CL+4.00
			  17=CL+4.25

RESERVED5	7:5	0x0	

MCA_DQS_ARRIVAL_1_PM	12:8	0x6	Channel A byte 1 input strobe reset removal edge in power management mode
			  0=CL
			  1=CL+0.25
			  2=CL+0.50
			  3=CL+0.75
			  4=CL+1.00
			  5=CL+1.25
			  6=CL+1.50
			  7=CL+1.75
			  8=CL+2.00
			  9=CL+2.25
			  10=CL+2.50
			  11=CL+2.75
			  12=CL+3.00
			  13=CL+3.25
			  14=CL+3.50
			  15=CL+3.75
			  16=CL+4.00
			  17=CL+4.25

RESERVED13	15:13	0x0	

MCA_DQS_ARRIVAL_2_PM	20:16	0x6	Channel A byte 2 input strobe reset removal edge in power management mode
			  0=CL
			  1=CL+0.25
			  2=CL+0.50
			  3=CL+0.75
			  4=CL+1.00
			  5=CL+1.25
			  6=CL+1.50
			  7=CL+1.75
			  8=CL+2.00
			  9=CL+2.25
			  10=CL+2.50
			  11=CL+2.75
			  12=CL+3.00
			  13=CL+3.25
			  14=CL+3.50
			  15=CL+3.75
			  16=CL+4.00
			  17=CL+4.25

RESERVED21	23:21	0x0	

	28:24	0x6	Channel A byte 3 input strobe reset removal edge in power management mode
MCA_DQS_ARRIVAL_3_PM			0=CL 1=CL+0.25 2=CL+0.50 3=CL+0.75 4=CL+1.00 5=CL+1.25 6=CL+1.50 7=CL+1.75 8=CL+2.00 9=CL+2.25 10=CL+2.50 11=CL+2.75 12=CL+3.00 13=CL+3.25 14=CL+3.50 15=CL+3.75 16=CL+4.00 17=CL+4.25
RESERVED29	31:29	0x0	
Channel A input strobe gating timing in power management mode			

MCA_IN_TIMING_DQS_7654_PM - RW - 32 bits - NBMCIND:0xD1			
Field Name	**Bits**	**Default**	**Description**
MCA_DQS_ARRIVAL_4_PM	4:0	0x6	Channel A byte 4 input strobe reset removal edge in power management mode 0=CL 1=CL+0.25 2=CL+0.50 3=CL+0.75 4=CL+1.00 5=CL+1.25 6=CL+1.50 7=CL+1.75 8=CL+2.00 9=CL+2.25 10=CL+2.50 11=CL+2.75 12=CL+3.00 13=CL+3.25 14=CL+3.50 15=CL+3.75 16=CL+4.00 17=CL+4.25
RESERVED5	7:5	0x0	

MCA_DQS_ARRIVAL_5_PM	12:8	0x6	Channel A byte 5 input strobe reset removal edge in power management mode
			0=CL
			1=CL+0.25
			2=CL+0.50
			3=CL+0.75
			4=CL+1.00
			5=CL+1.25
			6=CL+1.50
			7=CL+1.75
			8=CL+2.00
			9=CL+2.25
			10=CL+2.50
			11=CL+2.75
			12=CL+3.00
			13=CL+3.25
			14=CL+3.50
			15=CL+3.75
			16=CL+4.00
			17=CL+4.25
RESERVED13	15:13	0x0	
MCA_DQS_ARRIVAL_6_PM	20:16	0x6	Channel A byte 6 input strobe reset removal edge in power management mode
			0=CL
			1=CL+0.25
			2=CL+0.50
			3=CL+0.75
			4=CL+1.00
			5=CL+1.25
			6=CL+1.50
			7=CL+1.75
			8=CL+2.00
			9=CL+2.25
			10=CL+2.50
			11=CL+2.75
			12=CL+3.00
			13=CL+3.25
			14=CL+3.50
			15=CL+3.75
			16=CL+4.00
			17=CL+4.25
RESERVED21	23:21	0x0	

MCA_DQS_ARRIVAL_7_PM	28:24	0x6	Channel A byte 7 input strobe reset removal edge in power management mode
			  0=CL
			  1=CL+0.25
			  2=CL+0.50
			  3=CL+0.75
			  4=CL+1.00
			  5=CL+1.25
			  6=CL+1.50
			  7=CL+1.75
			  8=CL+2.00
			  9=CL+2.25
			  10=CL+2.50
			  11=CL+2.75
			  12=CL+3.00
			  13=CL+3.25
			  14=CL+3.50
			  15=CL+3.75
			  16=CL+4.00
			  17=CL+4.25

RESERVED29	31:29	0x0	
Channel A input strobe gating timing in power management mode			

MCA_OUT_TIMING_DQ_PM - RW - 32 bits - NBMCIND:0xD2			
Field Name	**Bits**	**Default**	**Description**

MCA_OUT_TIMING_DQ_B0_PM	3:0	0x3	Channel A byte 0 data and mask output timing in power management mode
			  0= -1 clock delay
			  1= -3/4 clock delay
			  2= -1/2 clock delay
			  3= -1/4 clock delay
			  4=0 clock delay
			  5=1/4 clock delay
			  6=1/2 clock delay
			  7=3/4 clock delay

MCA_OUT_TIMING_DQ_B1_PM	7:4	0x3	Channel A byte 1 data and mask output timing in power management mode
			  0= -1 clock delay
			  1= -3/4 clock delay
			  2= -1/2 clock delay
			  3= -1/4 clock delay
			  4=0 clock delay
			  5=1/4 clock delay
			  6=1/2 clock delay
			  7=3/4 clock delay

MCA_OUT_TIMING_DQ_B2_PM	11:8	0x3	Channel A byte 2 data and mask output timing in power management mode
			  0= -1 clock delay
			  1= -3/4 clock delay
			  2= -1/2 clock delay
			  3= -1/4 clock delay
			  4=0 clock delay
			  5=1/4 clock delay
			  6=1/2 clock delay
			  7=3/4 clock delay

MCA_OUT_TIMING_DQ_B3_PM	15:12	0x3	Channel A byte 3 data and mask output timing in power management mode 0= -1 clock delay 1= -3/4 clock delay 2= -1/2 clock delay 3= -1/4 clock delay 4=0 clock delay 5=1/4 clock delay 6=1/2 clock delay 7=3/4 clock delay
MCA_OUT_TIMING_DQ_B4_PM	19:16	0x3	Channel A byte 4 data and mask output timing in power management mode 0= -1 clock delay 1= -3/4 clock delay 2= -1/2 clock delay 3= -1/4 clock delay 4=0 clock delay 5=1/4 clock delay 6=1/2 clock delay 7=3/4 clock delay
MCA_OUT_TIMING_DQ_B5_PM	23:20	0x3	Channel A byte 5 data and mask output timing in power management mode 0= -1 clock delay 1= -3/4 clock delay 2= -1/2 clock delay 3= -1/4 clock delay 4=0 clock delay 5=1/4 clock delay 6=1/2 clock delay 7=3/4 clock delay
MCA_OUT_TIMING_DQ_B6_PM	27:24	0x3	Channel A byte 6 data and mask output timing in power management mode 0= -1 clock delay 1= -3/4 clock delay 2= -1/2 clock delay 3= -1/4 clock delay 4=0 clock delay 5=1/4 clock delay 6=1/2 clock delay 7=3/4 clock delay
MCA_OUT_TIMING_DQ_B7_PM	31:28	0x3	Channel A byte 7 data and mask output timing in power management mode 0= -1 clock delay 1= -3/4 clock delay 2= -1/2 clock delay 3= -1/4 clock delay 4=0 clock delay 5=1/4 clock delay 6=1/2 clock delay 7=3/4 clock delay
Channel A output data and mask timing in power management mode			

MCA_OUT_TIMING_DQS_PM - RW - 32 bits - NBMCIND:0xD3			
Field Name	**Bits**	**Default**	**Description**
MCA_OUT_TIMING_DQS_0_PM	3:0	0x4	Channel A byte 0 strobe output timing in power management mode 0= -1 clock delay 1= -3/4 clock delay 2= -1/2 clock delay 3= -1/4 clock delay 4=0 clock delay 5=1/4 clock delay 6=1/2 clock delay 7=3/4 clock delay
MCA_OUT_TIMING_DQS_1_PM	7:4	0x4	Channel A byte 1 strobe output timing in power management mode 0= -1 clock delay 1= -3/4 clock delay 2= -1/2 clock delay 3= -1/4 clock delay 4=0 clock delay 5=1/4 clock delay 6=1/2 clock delay 7=3/4 clock delay
MCA_OUT_TIMING_DQS_2_PM	11:8	0x4	Channel A byte 2 strobe output timing in power management mode 0= -1 clock delay 1= -3/4 clock delay 2= -1/2 clock delay 3= -1/4 clock delay 4=0 clock delay 5=1/4 clock delay 6=1/2 clock delay 7=3/4 clock delay
MCA_OUT_TIMING_DQS_3_PM	15:12	0x4	Channel A byte 3 strobe output timing in power management mode 0= -1 clock delay 1= -3/4 clock delay 2= -1/2 clock delay 3= -1/4 clock delay 4=0 clock delay 5=1/4 clock delay 6=1/2 clock delay 7=3/4 clock delay
MCA_OUT_TIMING_DQS_4_PM	19:16	0x4	Channel A byte 4 strobe output timing in power management mode 0 = -1 clock delay 1 = -3/4 clock delay 2 = -1/2 clock delay 3 = -1/4 clock delay 4 = 0 clock delay 5 = 1/4 clock delay 6 = 1/2 clock delay 7 = 3/4 clock delay

MCA_OUT_TIMING_DQS_5_PM	23:20	0x4	Channel A byte 5 strobe output timing in power management mode
			  0= -1 clock delay
			  1= -3/4 clock delay
			  2= -1/2 clock delay
			  3= -1/4 clock delay
			  4=0 clock delay
			  5=1/4 clock delay
			  6=1/2 clock delay
			  7=3/4 clock delay

MCA_OUT_TIMING_DQS_6_PM	27:24	0x4	Channel A byte 6 strobe output timing in power management mode
			  0= -1 clock delay
			  1= -3/4 clock delay
			  2= -1/2 clock delay
			  3= -1/4 clock delay
			  4=0 clock delay
			  5=1/4 clock delay
			  6=1/2 clock delay
			  7=3/4 clock delay

MCA_OUT_TIMING_DQS_7_PM	31:28	0x4	Channel A byte 7 strobe output timing in power management mode
			  0= -1 clock delay
			  1= -3/4 clock delay
			  2= -1/2 clock delay
			  3= -1/4 clock delay
			  4=0 clock delay
			  5=1/4 clock delay
			  6=1/2 clock delay
			  7=3/4 clock delay

Channel A output strobe timing in power management mode			

MCA_MISCELLANEOUS - RW - 32 bits - NBMCIND:0xD4			
Field Name	**Bits**	**Default**	**Description**
RESERVED	31:0	0x0	
Channel A miscellaneous			

MCA_MISCELLANEOUS_2 - RW - 32 bits - NBMCIND:0xD5			
Field Name	**Bits**	**Default**	**Description**
RESERVED	31:0	0x0	
Channel A miscellaneous 2			

MCA_MX1X2X_DQ - RW - 32 bits - NBMCIND:0xD6			
Field Name	**Bits**	**Default**	**Description**
MCA_MX1X2X_DQ_B0	1:0	0x0	Channel A byte 0 output data/mask phase range 0=Nominal, inverted 1x clock 1=Quarter clock delay, 1x clock sampled with 2x rising edge clock and resampled with 2x falling edge clock 2=Half clock delay, 1x clock 3=Three quarters clock delay, inverted 1x clock sampled with 2x rising edge clock and resampled with 2x falling edge clock
MCA_MX1X2X_DQ_B1	3:2	0x0	Channel A byte 1 output data/mask phase range 0=Nominal, inverted 1x clock 1=Quarter clock delay, 1x clock sampled with 2x rising edge clock and resampled with 2x falling edge clock 2=Half clock delay, 1x clock 3=Three quarters clock delay, inverted 1x clock sampled with 2x rising edge clock and resampled with 2x falling edge clock
MCA_MX1X2X_DQ_B0_PM	17:16	0x0	Channel A byte 0 output data/mask phase range in power management mode 0=Nominal, inverted 1x clock 1=Quarter clock delay, 1x clock sampled with 2x rising edge clock and resampled with 2x falling edge clock 2=Half clock delay, 1x clock 3=Three quarters clock delay, inverted 1x clock sampled with 2x rising edge clock and resampled with 2x falling edge clock
MCA_MX1X2X_DQ_B1_PM	19:18	0x0	Channel A byte 1 output data/mask phase range in power management mode 0=Nominal, inverted 1x clock 1=Quarter clock delay, 1x clock sampled with 2x rising edge clock and resampled with 2x falling edge clock 2=Half clock delay, 1x clock 3=Three quarters clock delay, inverted 1x clock sampled with 2x rising edge clock and resampled with 2x falling edge clock
Channel A output data/mask phase range			

MCA_MX1X2X_DQS - RW - 32 bits - NBMCIND:0xD7			
Field Name	**Bits**	**Default**	**Description**
MCA_MX1X2X_DQS_0	1:0	0x0	Channel A byte 0 output strobe phase range 0=Nominal, inverted 1x clock 1=Quarter clock delay, 1x clock sampled with 2x rising edge clock and resampled with 2x falling edge clock 2=Half clock delay, 1x clock 3=Three quarters clock delay, inverted 1x clock sampled with 2x rising edge clock and resampled with 2x falling edge clock
MCA_MX1X2X_DQS_1	3:2	0x0	Channel A byte 1 output strobe phase range 0=Nominal, inverted 1x clock 1=Quarter clock delay, 1x clock sampled with 2x rising edge clock and resampled with 2x falling edge clock 2=Half clock delay, 1x clock 3=Three quarters clock delay, inverted 1x clock sampled with 2x rising edge clock and resampled with 2x falling edge clock
MCA_MX1X2X_DQS_0_PM	17:16	0x0	Channel A byte 0 output strobe phase range in power management mode 0=Nominal, inverted 1x clock 1=Quarter clock delay, 1x clock sampled with 2x rising edge clock and resampled with 2x falling edge clock 2=Half clock delay, 1x clock 3=Three quarters clock delay, inverted 1x clock sampled with 2x rising edge clock and resampled with 2x falling edge clock
MCA_MX1X2X_DQS_1_PM	19:18	0x0	Channel A byte 1 output strobe phase range in power management mode 0=Nominal, inverted 1x clock 1=Quarter clock delay, 1x clock sampled with 2x rising edge clock and resampled with 2x falling edge clock 2=Half clock delay, 1x clock 3=Three quarters clock delay, inverted 1x clock sampled with 2x rising edge clock and resampled with 2x falling edge clock
Channel A output strobe phase range			

MCA_DLL_MASTER_0 - RW - 32 bits - NBMCIND:0xD8			
Field Name	**Bits**	**Default**	**Description**
MCA_DLL_ADJ_MSTR_0	7:0	0x78	Channel A byte 0 DLL master. 160 (0xA0)
MCA_DLL_TSTCTRL_0	13:8	0x0	Channel A byte 0 DLL test/control select.
MCA_DLL_PWRDN_0	14	0x0	Channel A byte 0 DLL power down.
MCA_DLL_RESET_0	15	0x0	Channel A byte 0 DLL reset.
MCA_DLL_ADJ_MSTR_0_PM	23:16	0x78	Channel A byte 0 DLL master in power management mode. 160 (0xA0)
RESERVED24	30:24	0x0	
MCA_DLL_RESET_0_PM	31	0x0	Channel A byte 0 DLL reset in power management mode.
Channel A byte 0 DLL master			

MCA_DLL_MASTER_1 - RW - 32 bits - NBMCIND:0xD9			
Field Name	**Bits**	**Default**	**Description**
MCA_DLL_ADJ_MSTR_1	7:0	0x78	Channel A byte 1 DLL master. 160 (0xA0)
MCA_DLL_TSTCTRL_1	13:8	0x0	Channel A byte 1 DLL test/control select.
MCA_DLL_PWRDN_1	14	0x0	Channel A byte 1 DLL power down.
MCA_DLL_RESET_1	15	0x0	Channel A byte 1 DLL reset.
MCA_DLL_ADJ_MSTR_1_PM	23:16	0x78	Channel A byte 1 DLL master in power management mode. 160 (0xA0)
RESERVED24	30:24	0x0	
MCA_DLL_RESET_1_PM	31	0x0	Channel A byte 1 DLL reset in power management mode.
Channel A byte 1 DLL master			

MCA_DLL_SLAVE_RD_0 - RW - 32 bits - NBMCIND:0xE0			
Field Name	**Bits**	**Default**	**Description**
MCA_DLL_ADJ_DQSR_0	7:0	0x24	Channel A byte 0 input strobe rising edge phase. 46 (0x2E) , half 2x , quarter 1x 126 (0x7E) , full 2x , half 1x
MCA_DLL_ADJ_DQSR_0_PM	23:16	0x24	Channel A byte 0 input strobe rising edge phase in power management mode. 46 (0x2E) , half 2x , quarter 1x
Channel A byte 0 input strobe phase			

MCA_DLL_SLAVE_RD_1 - RW - 32 bits - NBMCIND:0xE1			
Field Name	**Bits**	**Default**	**Description**
MCA_DLL_ADJ_DQSR_1	7:0	0x24	Channel A byte 1 input strobe rising edge phase. 46 (0x2E) , half 2x , quarter 1x 126 (0x7E) , full 2x , half 1x
MCA_DLL_ADJ_DQSR_1_PM	23:16	0x24	Channel A byte 1 input strobe rising edge phase in power management mode. 46 (0x2E) , half 2x , quarter 1x
Channel A byte 1 input strobe phase			

MCA_DLL_SLAVE_WR_0 - RW - 32 bits - NBMCIND:0xE8			
Field Name	**Bits**	**Default**	**Description**
MCA_DLL_ADJ_DQ_B0	7:0	0x60	Channel A byte 0 data and mask output phase. 46 (0x2E) , half 2x , quarter 1x 126 (0x7E) , full 2x , half 1x
MCA_DLL_ADJ_DQ_B0_PM	23:16	0x60	Channel A byte 0 data and mask output phase in power management mode. 46 (0x2E) , half 2x , quarter 1x 126 (0x7E) , full 2x , half 1x
Channel A byte 0 output phase			

MCA_DLL_SLAVE_WR_1 - RW - 32 bits - NBMCIND:0xE9			
Field Name	**Bits**	**Default**	**Description**
MCA_DLL_ADJ_DQ_B1	7:0	0x60	Channel A byte 1 data and mask output phase. 46 (0x2E) , half 2x , quarter 1x 126 (0x7E) , full 2x , half 1x
MCA_DLL_ADJ_DQ_B1_PM	23:16	0x60	Channel A byte 1 data and mask output phase in power management mode. 46 (0x2E) , half 2x , quarter 1x 126 (0x7E) , full 2x , half 1x
Channel A byte 1 output phase			

MCA_RESERVED_0 - RW - 32 bits - NBMCIND:0xF0			
Field Name	**Bits**	**Default**	**Description**
RESERVED	31:0	0x0	
Memory controller reserved for future use			

MCA_RESERVED_1 - RW - 32 bits - NBMCIND:0xF1			
Field Name	**Bits**	**Default**	**Description**
RESERVED	31:0	0x0	
Memory controller reserved for future use			

MCA_RESERVED_2 - RW - 32 bits - NBMCIND:0xF2			
Field Name	**Bits**	**Default**	**Description**
RESERVED	31:0	0x0	
Memory controller reserved for future use			

MCA_RESERVED_3 - RW - 32 bits - NBMCIND:0xF3			
Field Name	**Bits**	**Default**	**Description**
RESERVED	31:0	0x0	
Memory controller reserved for future use			

MCA_RESERVED_4 - RW - 32 bits - NBMCIND:0xF4			
Field Name	**Bits**	**Default**	**Description**
RESERVED	31:0	0x0	
Memory controller reserved for future use			

MCA_RESERVED_5 - RW - 32 bits - NBMCIND:0xF5			
Field Name	**Bits**	**Default**	**Description**
RESERVED	31:0	0x0	
Memory controller reserved for future use			

MCA_RESERVED_6 - RW - 32 bits - NBMCIND:0xF6			
Field Name	**Bits**	**Default**	**Description**
RESERVED	31:0	0x0	
Memory controller reserved for future use			

MCA_RESERVED_7 - RW - 32 bits - NBMCIND:0xF7			
Field Name	**Bits**	**Default**	**Description**
RESERVED	31:0	0x0	
Memory controller reserved for future use			

MCA_RESERVED_8 - RW - 32 bits - NBMCIND:0xF8			
Field Name	**Bits**	**Default**	**Description**
RESERVED	31:0	0x0	
Memory controller reserved for future use			

MCA_RESERVED_9 - RW - 32 bits - NBMCIND:0xF9			
Field Name	**Bits**	**Default**	**Description**
RESERVED	31:0	0x0	
Memory controller reserved for future use			

MCA_RESERVED_A - RW - 32 bits - NBMCIND:0xFA			
Field Name	**Bits**	**Default**	**Description**
RESERVED	31:0	0x0	
Memory controller reserved for future use			

MCA_RESERVED_B - RW - 32 bits - NBMCIND:0xFB			
Field Name	**Bits**	**Default**	**Description**
RESERVED	31:0	0x0	
Memory controller reserved for future use			

MCA_RESERVED_C - RW - 32 bits - NBMCIND:0xFC			
Field Name	**Bits**	**Default**	**Description**
RESERVED	31:0	0x0	
Memory controller reserved for future use			

MCA_RESERVED_D - RW - 32 bits - NBMCIND:0xFD			
Field Name	**Bits**	**Default**	**Description**
RESERVED	31:0	0x0	
Memory controller reserved for future use			

MCA_RESERVED_E - RW - 32 bits - NBMCIND:0xFE			
Field Name	**Bits**	**Default**	**Description**
RESERVED	31:0	0x0	
Memory controller reserved for future use			

MCA_RESERVED_F - RW - 32 bits - NBMCIND:0xFF			
Field Name	**Bits**	**Default**	**Description**
RESERVED	31:0	0x0	
Memory controller reserved for future use			

MCCFG_FB_LOCATION - RW - 32 bits - NBMCIND:0x100			
Field Name	**Bits**	**Default**	**Description**
MC_FB_START	15:0	0x0	Start of local frame buffer section in the internal address space. Note: Bits [5:0] of this field are hardwired to 0.
MC_FB_TOP	31:16	0x3f	Top of local frame buffer section in the internal address space. Note: Bits [5:0] of this field are hardwired to 1.
This register defines the base address and the top of memory of the reserved memory area that is allocated to the frame buffer			

MCCFG_AGP_LOCATION - RW - 32 bits - NBMCIND:0x101			
Field Name	**Bits**	**Default**	**Description**
MC_AGP_START	15:0	0x0	Start location of AGP aperture. Note: Bits [5:0] of this field are hardwired to 0.
MC_AGP_TOP	31:16	0x3f	Top location within AGP aperture. Note: Bits [5:0] of this field are hardwired to 1.
Defines the location of AGP in the chip internal address space			

MCCFG_AGP_BASE - RW - 32 bits - NBMCIND:0x102			
Field Name	**Bits**	**Default**	**Description**
AGP_BASE_ADDR	31:0	0x0	When a request falls in the internal AGP aperture (MC_AGP_LOCATION), a relative address is formed by stripping off MC_AGP_START. AGP_BASE_ADDR is added to the relative address to create the address in the host system. Note: Bits [21:0] of this field are hardwired to 0.
Specifies the base location of AGP space in the host system.			

MCCFG_AGP_BASE_2 - RW - 32 bits - NBMCIND:0x103			
Field Name	**Bits**	**Default**	**Description**
AGP_BASE_ADDR_2	3:0	0x0	Used to represents AGB Base address above 4 GBytes and up to 32 GBytes.
This is used for handling 32 Gbytes AGP Base Address. The 4 bits field represents the 4 MSBs. It extends the AGP_BASE to 36 bits instead of 32 bits.			

MC_INIT_MISC_LAT_TIMER - RW - 32 bits - NBMCIND:0x104			
Field Name	**Bits**	**Default**	**Description**
MC_CPR_INIT_LAT	3:0	0x0	Raises the service priority after VALUE * 32 MCLKs to prevent staleness of CPR requests.
MC_VF_INIT_LAT	7:4	0x0	Raises the service priority after VALUE * 32 MCLKs to prevent staleness of VF requests.
MC_DISP0R_INIT_LAT	11:8	0x0	Raises the service priority after VALUE * 32 MCLKs to prevent staleness of DISP0R requests.
MC_DISP1R_INIT_LAT	15:12	0x0	Raises the service priority after VALUE * 32 MCLKs to prevent staleness of DISP0R requests.
MC_FIXED_INIT_LAT	19:16	0x0	Raises the service priority after VALUE * 32 MCLKs to prevent staleness of FIXED requests.
MC_E2R_INIT_LAT	23:20	0x0	Raises the service priority after VALUE * 32 MCLKs to prevent staleness of E2R requests.
SAME_PAGE_PRIO	27:24	0xf	Used by the memory controller efficiency arbitration. It stays on the same page until the time exceeds the same_page_priority number. Indicates the consecutive page hits that are necessary to be able to hide page-misses to another bank.
MC_GLOBW_INIT_LAT	31:28	0x0	Raises service priority after VALUE * 32 MCLKs to prevent staleness of Global Write FIFO requests
For read clients such as CP, VF, DISP0, DISP1 and E2, there is a latency timer per client. For the other clients who compete in the real-time arbiter, there is a single latency timer for the one winner. The latency timer is programmable for each client. When a request is received, the latency timer starts. If the timer expires before the request wins arbitration, then the request is elevated to a higher priority. The purpose here is to prevent requests from becoming stale simply because they are not efficient. The display latency timer is intended to address its high bandwidth requirements for high performance display modes. Since the display is a periodic requester, the latency timer can be set to a rate slightly above the average rate. The effect will be that the memory controller will attempt to provide a somewhat regular data flow to the display client. The purpose is to prevent the display from needing to set its URGENCY flag, which will reduce the overall performance of the memory controller. It is anticipated that only very-high performance display modes will need this feature, so the register setting will normally be static. Provisions should be made in SW to re-program this field for high-performance display modes.			

MC_INIT_GFX_LAT_TIMER - RW - 32 bits - NBMCIND:0x105

Field Name	Bits	Default	Description
MC_G3D0R_INIT_LAT	3:0	0x0	Raises the service priority after VALUE * 16 MCLKs to prevent staleness of G3D0R requests.
MC_G3D1R_INIT_LAT	7:4	0x0	Raises the service priority after VALUE * 16 MCLKs to prevent staleness of G3D1R requests.
MC_G3D2R_INIT_LAT	11:8	0x0	Raises the service priority after VALUE * 16 MCLKs to prevent staleness of G3D2R requests.
MC_G3D3R_INIT_LAT	15:12	0x0	Raises the service priority after VALUE * 16 MCLKs to prevent staleness of G3D3R requests.
MC_TX0R_INIT_LAT	19:16	0x0	Raises the service priority after VALUE * 16 MCLKs to prevent staleness of TX0R requests.
MC_TX1R_INIT_LAT	23:20	0x0	Raises the service priority after VALUE * 16 MCLKs to prevent staleness of TX1R requests.
MC_GLOBR_INIT_LAT	27:24	0x0	Raises the service priority after VALUE * 32 MCLKs to prevent staleness of Global Read FIFO requests.
MC_GLOBW_FULL_LAT	31:28	0xf	Raises the service priority after VALUE * 16 MCLKs to delay urgency requests for Global Write FIFO requests.
For the graphics 3D clients, there is a latency timer per client. The latency timer period is programmable for each client. When a request is received, the latency timer starts. If the timer expires before the request wins arbitration, then the request is elevated to a higher priority. Then intent is to prevent requests from becoming stale simply because they are not efficient.			

MC_INIT_WR_LAT_TIMER - RW - 32 bits - NBMCIND:0x106

Field Name	Bits	Default	Description
MC_G3D0W_INIT_LAT	3:0	0xf	Raises the service priority after VALUE * 16 MCLKS. If zero, urgent when g3d0w interface fifo full.
MC_G3D1W_INIT_LAT	7:4	0xf	Raises the service priority after VALUE * 16 MCLKS. If zero, urgent when g3d1w interface fifo full.
MC_G3D2W_INIT_LAT	11:8	0xf	Raises the service priority after VALUE * 16 MCLKS. If zero, urgent when g3d2w interface fifo full.
MC_G3D3W_INIT_LAT	15:12	0xf	Raises the service priority after VALUE * 16 MCLKS. If zero, urgent when g3d3w interface fifo full.
MC_IDCTW_INIT_LAT	19:16	0x2	Raises the service priority after VALUE * 16 MCLKS. If zero, urgent when idctw interface fifo full.
MC_HDPW_INIT_LAT	23:20	0x2	Raises the service priority after VALUE * 16 MCLKS. If zero, urgent when hdpw interface fifo full.
MC_VIPW_INIT_LAT	27:24	0x2	Raises the service priority after VALUE * 16 MCLKS. If zero, urgent when vipw interface fifo full.
MC_CPW_INIT_LAT	31:28	0x2	Raises the service priority after VALUE * 16 MCLKS. If zero, urgent when cpw interface fifo full.
For all the write clients, there is a latency timer per client. The latency timer period is programmable for each client. When the interface fifo is full, the latency timer starts. If the timer expires before the request wins the first level arbitration, then the request is elevated to a higher priority. Then intent is to prevent the write requests become urgent all the time because the fifo is full.			

MC_ARB_CNTL - RW - 32 bits - NBMCIND:0x107			
Field Name	**Bits**	**Default**	**Description**

ONE_PAGE	0	0x0	If 1, then it is One Page mode. In the first level graphics read arbiter, it uses one page information for efficiency generation. This is the R300 architecture.
			If 0, then it is Four Page mode. It uses four pages instead of one in order to compute the memory efficiency info, one page per bank queue. In theory, this mode should improve memory efficiency and hence the graphics performance.
			    0=Four Pages mode in First Level GFX Arbiter
			    1=One Page mode in First Level GFX Arbiter, R300 mode

DISP0R_FIFO_LEVEL	1	0x1	In R300, it relies on the priority signal from the display unit, or the timesout counter, to change the display request to a high priority request. But, once the display unit asserts priority, it will stay in priority mode for a long time, which will hurt the memory efficiency. However, using the timesout counter by itself cannot fulfill the bandwidth requirement when in 1600x1200 @85Hz mode. This setting is added which may help to fulfill the display bw requirements without using priority signal.
			    0=Disable asserting urg request when interface fifo is almost full
			    1=Enable asserting urg request when interface fifo is almost full

DISP1R_FIFO_LEVEL	2	0x1	Similar to DISP0R_FIFO_LEVEL.
			    0=Disable asserting urg request when interface fifo is almost full
			    1=Enable asserting urg request when interface fifo is almost full

OV0R_FIFO_LEVEL	3	0x0	All other FIFO_LEVEL settings are added for completeness.
			    0=Disable asserting urg request when interface fifo is almost full
			    1=Enable asserting urg request when interface fifo is almost full

CPR_FIFO_LEVEL	4	0x0	All other FIFO_LEVEL settings are added for completeness.
			    0=Disable asserting urg request when interface fifo is almost full
			    1=Enable asserting urg request when interface fifo is almost full

VFR_FIFO_LEVEL	5	0x0	All other FIFO_LEVEL settings are added for completeness.
			    0=Disable asserting urg request when interface fifo is almost full
			    1=Enable asserting urg request when interface fifo is almost full

E2R_FIFO_LEVEL	6	0x0	All other FIFO_LEVEL settings are added for completeness.
			    0=Disable asserting urg request when interface fifo is almost full
			    1=Enable asserting urg request when interface fifo is almost full

IDCTR_FIFO_LEVEL	7	0x0	All other FIFO_LEVEL settings are added for completeness.
			  0=Disable asserting urg request when interface fifo is almost full
			  1=Enable asserting urg request when interface fifo is almost full

DIS_DISPACK	8	0x1	0=Enable the Display Ack Protocol, R300 mode 1=Disable the Display Ack Protocol for improving display BW
Miscellaneous controls for gfx arbiter			

MC_DEBUG_CNTL - RW - 32 bits - NBMCIND:0x108			
Field Name	**Bits**	**Default**	**Description**
MC_DEBUG_1_0	1:0	0x3	reserved

MC_DEBUG_3_2	3:2	0x0	Bit [0]:
			If 0, masking 8 cycles for bank access in write arbiter.
			If 1, masking 9 cycles for bank access in write arbiter.
			Bit [1]:
			If 0, masking 8 cycles for bank access in 2nd level arbiter,
			If 1, masking 9 cycles for bank access in 2nd level arbiter.
			Reserved for future use.
			  0=Masking bank access in 1st level wr, 2nd level arbiter for 8 cycles
			  1=Masking bank access in 1st level wr for 8 cycles, 2nd level arb for 9 cycles
			  2=Masking bank access in 1st level wr for 9 cycles, 2nd level arb for 8 cycles
			  3=Masking bank access in 1st level wr, 2nd level arbiter for 9 cycles

MC_DEBUG_7_4	7:4	0x0	Bit [0]:
			Write Flush Mode. In write flush mode, it will force 16 writes to be issued back to back with no interruption.
			  0=Disabled
			  1=Enabled write flush mode
			Bit [1]:
			Disable Same Page Priority Greater than N mode for write. In this mode, the write arbitration logic will ignore the SAME_PAGE_PRIO.
			Bit [2]:
			Masking the bank for 4 cycles instead of 8/9 in second level arbiter.
			Bit [3]:
			Reserved for future use.

MC_DEBUG_11_8	11:8	0x2	Bit [0]: If 1, enable sideport and UMA first and second arbiter stage to use fix order arbitration. If 0, round robbin arbitration is used. Bit [1]: If 1, enable sideport and UMA second arbiter stage to use efficiency based arbitration. If 0, round robbin arbitration is used.
MC_DEBUG_15_12	15:12	0x0	Reserved
MC_DEBUG_19_16	19:16	0x3	Reserved
MC_DEBUG_23_20	23:20	0x0	Reserved
MC_DEBUG_27_24	27:24	0xf	Reserved
MC_DEBUG_31_28	31:28	0x0	Reserved
Debug Register, added for performance tuning			

MC_BIST_CNTL0 - RW - 32 bits - NBMCIND:0x111			
Field Name	**Bits**	**Default**	**Description**
BIST_DONE (R)	0	0x0	Set to 0 when BIST_RUN or BIST_RESET_N is 0. Set to 1 when the bist read/write is done either normally or due to mismatch
BIST_MISMATCH_CYCLE (R)	3:1	0x0	Records the cycle which caused the mismatch. 3'b000: cycle1 of burst1; 3'b100: cycle1 of burst2; 3'b001: cycle2 of burst1; 3'b1001 cycle2 of burst2; 3'b010: cycle3 of burst1; 3'b110: cycle3 of burst2; 3'b011: cycle4 of burst1; 3'b111: cycle4 of burst2;
BIST_RUN	4	0x0	0=Disable 1=Enable
BIST_RESET_N	5	0x0	0=Resets mcbist, but does not disturb read-only mcbist values. 1=Active
BIST_MISMATCH_STATUS	7:6	0x0	0=Data (64 bit) mismatch info. Info would be ORed with subsequent reads 1=Keeps first mismatch data info as sticky 2=Address 32'd0,addr[26:0],5'd0 mismatch info. is updated at every mismatch 3=Keep first address info sticky
First control register of MCBIST			

MC_BIST_CNTL1 - RW - 32 bits - NBMCIND:0x112			
Field Name	**Bits**	**Default**	**Description**
BIST_MISMATCH_STKY (R)	0	0x0	0=When BIST_RUN is 0 1=Read mismatch
BIST_RDWR_EN	2:1	0x0	0=No op 1=Activate write client only 2=Activate read client only 3=Activate both read & write clients
BIST_SADDR_SEL	4:3	0x0	0=No op 1=Set start write-address 2=Set start read-address 3=Set both start read and start write addresses
BIST_CYC	7:5	0x0	0=No op 1=Run for 2 read (and/or write) bursts 2=Run for 4 read (and/or write) bursts 3=Reserved 4=Reserved 5=Reserved 6=Run for 32 read (and/or write) bursts 7=Run continuously until there is a mismatch-stop, or end-address stop
BIST_DATA_CMP	8	0x0	0=Read data is compared against expected data 1=Read data is not compared. No question of mismatch
BIST_MISMATCH_STOP	9	0x0	0=Do not stop if read mismatch 1=Stop if read mismatch
BIST_ADDR_BND	10	0x0	0=Use read address for end-address stop 1=Use write address for end-address stop

BIST_ADDR_LOOP	11	0x0	0=Stop based on BIST_CYC 1=Keep looping read (and/or write) operations between start and end addresses
BIST_WADDR_GEN	14:12	0x0	0=wr_addr[26:0] = wr_addr[26:0] + 1 1=wr_addr[26:0] = wr_addr[26:0] - 1 2=wr_addr[26:0] = wr_addr[26:0] + 4 3=wr_addr[26:0] = wr_addr[26:0] - 4 4=wr_addr[26:13] = wr_addr[26:13] + 1 5=wr_addr[26:13] = wr_addr[26:13] - 1 6=wr_addr[26:19] = wr_addr[26:19] + 1 7=No change in write address
BIST_RADDR_GEN	17:15	0x0	0=rd_addr[26:0] = rd_addr[26:0] + 1 1=rd_addr[26:0] = rd_addr[26:0] - 1 2=rd_addr[26:0] = rd_addr[26:0] + 4 3=rd_addr[26:0] = rd_addr[26:0] - 4 4=rd_addr[26:13] = rd_addr[26:13] + 1 5=rd_addr[26:13] = rd_addr[26:13] - 1 6=rd_addr[26:19] = rd_addr[26:19] + 1 7=No change in read address
BIST_END_ADDR	31:18	0x0	read/write upper address (addr[31:18])

Second control register of MCBIST. The bit field [31:5] of this register is also used as starting address (BIST_START_ADDR). Refer to bit field BIST_SADDR_SEL for details.

MC_BIST_MISMATCH_L - RW - 32 bits - NBMCIND:0x113

Field Name	Bits	Default	Description
BIST_MISMATCH_L (R)	31:0	0x0	Refer to BIST_MISMATCH_STATUS for setting.

Lower 32 bits of the 64 bits mcbist read mismatch info

MC_BIST_MISMATCH_H - RW - 32 bits - NBMCIND:0x114

Field Name	Bits	Default	Description
BIST_MISMATCH_H (R)	31:0	0x0	Refer to BIST_MISMATCH_STATUS for setting.

Upper 32 bits of the 64 bits mcbist read mismatch info

MC_BIST_PATTERN0L - RW - 32 bits - NBMCIND:0x115

Field Name	Bits	Default	Description
BIST_PATTERN0L	31:0	0x0	32 bit data pattern. Write only.

Lower half of DW0 (double word 0) of data pattern. MCBIST uses 8 user defined DWs to generate two consecutive data bursts - each of 4x64 bits.burst_one[255:0] = MC_BIST_PATTERN3H, MC_BIST_PATTERN3L, MC_BIST_PATTERN2H, MC_BIST_PATTERN2L, MC_BIST_PATTERN1H, MC_BIST_PATTERN1L, MC_BIST_PATTERN0H, MC_BIST_PATTERN0L. Similarly, burst-two is defined by other 8 registers. These registers are per mcbist engine based.

MC_BIST_PATTERN0H - RW - 32 bits - NBMCIND:0x116

Field Name	Bits	Default	Description
BIST_PATTERN0H	31:0	0x0	32 bit data pattern. Write only.

Refer to MC_BIST_PATTERN0L

MC_BIST_PATTERN1L - RW - 32 bits - NBMCIND:0x117

Field Name	Bits	Default	Description
BIST_PATTERN1L	31:0	0x0	32 bit data pattern. Write only.
Refer to MC_BIST_PATTERN0L			

MC_BIST_PATTERN1H - RW - 32 bits - NBMCIND:0x118

Field Name	Bits	Default	Description
BIST_PATTERN1H	31:0	0x0	32 bit data pattern. Write only.
Refer to MC_BIST_PATTERN0L			

MC_BIST_PATTERN2L - RW - 32 bits - NBMCIND:0x119

Field Name	Bits	Default	Description
BIST_PATTERN2L	31:0	0x0	32 bit data pattern. Write only.
Refer to MC_BIST_PATTERN0L			

MC_BIST_PATTERN2H - RW - 32 bits - NBMCIND:0x11A

Field Name	Bits	Default	Description
BIST_PATTERN2H	31:0	0x0	32 bit data pattern. Write only.
Refer to MC_BIST_PATTERN0L			

MC_BIST_PATTERN3L - RW - 32 bits - NBMCIND:0x11B

Field Name	Bits	Default	Description
BIST_PATTERN3L	31:0	0x0	32 bit data pattern. Write only.
Refer to MC_BIST_PATTERN0L			

MC_BIST_PATTERN3H - RW - 32 bits - NBMCIND:0x11C

Field Name	Bits	Default	Description
BIST_PATTERN3H	31:0	0x0	32 bit data pattern. Write only.
Refer to MC_BIST_PATTERN0L			

MC_BIST_PATTERN4L - RW - 32 bits - NBMCIND:0x11D

Field Name	Bits	Default	Description
BIST_PATTERN4L	31:0	0x0	32 bit data pattern. Write only.
Refer to MC_BIST_PATTERN0L			

MC_BIST_PATTERN4H - RW - 32 bits - NBMCIND:0x11E

Field Name	Bits	Default	Description
BIST_PATTERN4H	31:0	0x0	32 bit data pattern. Write only.
Refer to MC_BIST_PATTERN0L			

MC_BIST_PATTERN5L - RW - 32 bits - NBMCIND:0x11F

Field Name	Bits	Default	Description
BIST_PATTERN5L	31:0	0x0	32 bit data pattern. Write only.
Refer to MC_BIST_PATTERN0L			

MC_BIST_PATTERN5H - RW - 32 bits - NBMCIND:0x120

Field Name	Bits	Default	Description
BIST_PATTERN5H	31:0	0x0	32 bit data pattern. Write only.
Refer to MC_BIST_PATTERN0L			

MC_BIST_PATTERN6L - RW - 32 bits - NBMCIND:0x121

Field Name	Bits	Default	Description
BIST_PATTERN6L	31:0	0x0	32 bit data pattern. Write only.
Refer to MC_BIST_PATTERN0L			

MC_BIST_PATTERN6H - RW - 32 bits - NBMCIND:0x122

Field Name	Bits	Default	Description
BIST_PATTERN6H	31:0	0x0	32 bit data pattern. Write only.
Refer to MC_BIST_PATTERN0L			

MC_BIST_PATTERN7L - RW - 32 bits - NBMCIND:0x123

Field Name	Bits	Default	Description
BIST_PATTERN7L	31:0	0x0	32 bit data pattern. Write only.
Refer to MC_BIST_PATTERN0L			

MC_BIST_PATTERN7H - RW - 32 bits - NBMCIND:0x124

Field Name	Bits	Default	Description
BIST_PATTERN7H	31:0	0x0	32 bit data pattern. Write only.
Refer to MC_BIST_PATTERN0L			

2.9   System GART Control Registers

RCRB_Enhanced_Capability_Header - RW - 32 bits - MMGartReg:0x0			
Field Name	**Bits**	**Default**	**Description**
PCIE_Extended_CapID (R)	15:0	0xffff	All Fs indicate the capability list has nothing.
Extended_CapVer (R)	19:16	0x0	The current Capability version is 3'b1.
Next_CapOff (R)	31:20	0x0	All 0s indicate there is no next enhanced capability list.
RCRB Feature and Capabilities Register			

2.10 Display Clock Control

Clock control registers

CLOCK_CNTL_INDEX - RW - 32 bits - [IOReg,MMReg:0x8]			
Field Name	**Bits**	**Default**	**Description**
PLL_ADDR	6:0	0x0	Register address.
PLL_WR_EN	7	0x0	0=Disable writes to CLOCK_CNTL_DATA
			1=Enable writing to CLOCK_CNTL_DATA
PPLL_DIV_SEL	9:8	0x0	0=PPLL_DIV0
			1=PPLL_DIV1
			2=PPLL_DIV2
			3=PPLL_DIV3
Clock generation block register index control.			

CLOCK_CNTL_DATA - RW - 32 bits - [IOReg,MMReg:0xC]			
Field Name	**Bits**	**Default**	**Description**
PLL_DATA	31:0	0x0	Register value.
Clock generation block register data			

PLL_TEST_CNTL - RW - 32 bits - CLKIND:0x21			
Field Name	**Bits**	**Default**	**Description**
TST_SRC_SEL	3:0	0x0	Source clock to be measured.
TST_REF_SEL	7:4	0x0	Clock used as a frequency reference.
REF_TEST_COUNT	14:8	0x0	Run TST_REF_SEL by number of cycles.
TST_RESET	15	0x0	Reset frequency counter.
TEST_COUNT (R)	31:17	0x0	Frequency output value.
PLL frequency measurement CNTL.			

SPLL_FUNC_CNTL - RW - 32 bits - CLKIND:0x0			
Field Name	**Bits**	**Default**	**Description**
SPLL_RESET	0	0x1	0=Run
			1=Reset
SPLL_SLEEP	1	0x0	0=Power Up
			1=Power Down
SPLL_REF_DIV	4:2	0x1	SPLL reference divider value.
SPLL_FB_DIV	12:5	0x46	SPLL feedback divider value.
SPLL_PULSEEN	13	0x0	0=Don't pulse clock
			1=Send the number of pulses indicated by PULSENUM
SPLL_PULSENUM	15:14	0x0	Number of pulses required by SPLL.
SPLL_SW_HILEN	19:16	0x0	Post divider value for SPLL (high pulse section).
SPLL_SW_LOLEN	23:20	0x0	Post divider value for SPLL (low pulse section).
SPLL_DIVEN	24	0x1	1=Enable PLL CLKOUT divider
SPLL_BYPASS_EN	25	0x1	1=Enable Bypass Clockout

SPLL_CHG_STATUS (R)	29	0x0	1=Previous write/change to SPLL_FUNC_CNTL register has been completed. SW should not issue another write to this register until this bit is asserted
SPLL_CTLREQ	30	0x0	1=For debugging purposes. When SW_DIR_CONTROL is set, asserting this bit will trigger an update of the PLL clock output mux control. Before writing to this bit, HILEN/LOLEN/PULSEEN/PULSENUM should already contain the new set of value
SPLL_CTLACK (R)	31	0x0	1=For debugging purposes. When SW_DIR_CONTROL is set, this value replicates the value of the CTLREQ once the command has been received and it is safe to send another request
SPLL Control register			

SPLL_BYPASSCLK_SEL - RW - 32 bits - CLKIND:0x1			
Field Name	**Bits**	**Default**	**Description**
SPLL_CLKOUT_SEL	5:0	0x6	1=BCLK 2=MCLK 4=DISP CLK 8=AUXSIN 32=INV BCLK

SPLL_CNTL_MODE - RW - 32 bits - CLKIND:0x2			
Field Name	**Bits**	**Default**	**Description**
SPLL_SW_DIR_CONTROL	0	0x1	1=SW controls the PLL directly. SW will make sure the way they program SPLL_FUNC_CNTL register follows the PLL's requested protocol

SPLL_CLK_SEL - RW - 32 bits - CLKIND:0x3			
Field Name	**Bits**	**Default**	**Description**
SPLL_REFCLK_SRC_SEL	0	0x0	0=Ref clock from GPIO 1=Ref clock from XTALIN
SPLL_TEST	1	0x0	1=Enable SPLL test mode
SPLL_FASTEN	2	0x1	1=Enable SPLL fast lock
SPLL_ENSAT	3	0x1	1=Enable saturation behavior

MPLL_FUNC_CNTL - RW - 32 bits - CLKIND:0x4			
Field Name	**Bits**	**Default**	**Description**
MPLL_RESET	0	0x1	0=Run 1=Reset
MPLL_SLEEP	1	0x0	0=Power Up 1=Power Down
MPLL_REF_DIV	4:2	0x1	MPLL reference divider value.
MPLL_FB_DIV	12:5	0x6f	MPLL feedback divider value.
MPLL_PULSEEN	13	0x0	0=Don't pulse clock 1=Send the number of pulses indicated by PULSENUM
MPLL_PULSENUM	15:14	0x0	Not used.
MPLL_SW_HILEN	19:16	0x0	Not used.
MPLL_SW_LOLEN	23:20	0x0	Not used.
MPLL_DIVEN	24	0x0	1=Enable PLL CLKOUT divider
MPLL_BYPASS_EN	25	0x1	1=Enable Bypass mode
MPLL_MCLK_SEL	26	0x0	1=Use MPLL output as mclk
MPLL_CHG_STATUS (R)	29	0x0	1=Previous write/change to MPLL_FUNC_CNTL register has been completed. SW should not issue another write to this register until this bit is asserted
MPLL_CTLREQ	30	0x0	1=For debugging purposes. When SW_DIR_CONTROL is set, asserting this bit will trigger an update of the PLL clock output mux control. Before writing to this bit, HILEN/LOLEN/PULSEEN/PULSENUM should already contain the new set of value
MPLL_CTLACK (R)	31	0x0	1=For debugging purposes. When SW_DIR_CONTROL is set, this value replicates the value of the CTLREQ once the command has been received and it is safe to send another request
MPLL Control register			

MPLL_BYPASSCLK_SEL - RW - 32 bits - CLKIND:0x5			
Field Name	**Bits**	**Default**	**Description**
MPLL_CLKOUT_SEL	5:0	0x6	1=BCLK 2=SCLK 4=DISP CLK 8=TEST YCLK 32=INV BCLK

MPLL_CNTL_MODE - RW - 32 bits - CLKIND:0x6			
Field Name	**Bits**	**Default**	**Description**
MPLL_SW_DIR_CONTROL	1	0x0	1=SW controls the PLL directly. SW will make sure the way they program MPLL_FUNC_CNTL register follows the PLL's requested protocol

MPLL_CLK_SEL - RW - 32 bits - CLKIND:0x7			
Field Name	**Bits**	**Default**	**Description**
MPLL_REFCLK_SRC_SEL	0	0x0	0=Ref clock from GPIO 1=Ref clock from XTALIN
MPLL_TEST	1	0x0	1=Enable MPLL test mode
MPLL_FASTEN	2	0x1	1=Enable MPLL fast lock
MPLL_ENSAT	3	0x1	1=Enable saturation behavior

GENERAL_PWRMGT - RW - 32 bits - CLKIND:0x8			
Field Name	**Bits**	**Default**	**Description**
GLOBAL_PWRMGT_EN	0	0x0	0=Dynamic power management off 1=Dynamic power management on
MOBILE_SU	2	0x0	0=Regular 1=Optimize power consumption in Suspend mode for mobile
SU_SUSTAIN_DISABLE	3	0x0	0=Sustain suspend until PLL lockup 1=Disable

SCLK_PWRMGT_CNTL - RW - 32 bits - CLKIND:0x9			
Field Name	**Bits**	**Default**	**Description**
SCLK_PWRMGT_OFF	0	0x0	0=SCLK power management on 1=SCLK power management off
SCLK_TURNOFF	1	0x0	1=Turn off SCLK, SW direct control, override HW pwrmgt control
SPLL_TURNOFF	2	0x0	1=Power down SPLL, SW direct control, override HW pwrmgt control
SPARE	3	0x0	
SU_SCLK_USE_BCLK	4	0x0	0=Use slower SCLK under suspend mode 1=Use BCLK as SCLK under suspend mode
ACCESS_REGS_IN_SUSPEND	5	0x0	0=Disable 1=Force all SCLK branches to allow accessing any registers in suspend mode

MCLK_PWRMGT_CNTL - RW - 32 bits - CLKIND:0xA			
Field Name	**Bits**	**Default**	**Description**
MPLL_PWRMGT_OFF	0	0x0	0=M domain clock power management off
YCLK_TURNOFF	1	0x0	0=Turn off YCLK
MPLL_TURNOFF	2	0x0	0=Enable M domain PLL to be turned off at power state D3
SU_MCLK_USE_BCLK	3	0x0	0=Shut down MCLK during suspend mode 1=Use BCLK as SCLK under suspend mode
DLL_READY	4	0x0	0=DLL is not ready 1=DLL is ready
MC_BUSY (R)	5	0x0	0=MC is idle 1=MC is not idle
MC_SWITCH	6	0x0	0=Source of memory clock is not changed 1=Source of memory clock is changed
MC_INT_CNTL	7	0x1	0=SW overwrite 1=HW control
MRDCKA_SLEEP	8	0x0	0=Enable Channel A DLL 1=PowerDown Channel A DLL
MRDCKB_SLEEP	9	0x0	0=Enable Channel B DLL 1=PowerDown Channel B DLL
MRDCKC_SLEEP	10	0x0	0=Enable Channel C DLL 1=PowerDown Channel C DLL
MRDCKD_SLEEP	11	0x0	0=Enable Channel D DLL 1=PowerDown Channel D DLL
MRDCKA_RESET	12	0x1	0=Enable Channel A DLL 1=Reset Channel A DLL
MRDCKB_RESET	13	0x1	0=Enable Channel B DLL 1=Reset Channel B DLL
MRDCKC_RESET	14	0x1	0=Enable Channel C DLL 1=Reset Channel C DLL
MRDCKD_RESET	15	0x1	0=Enable Channel D DLL 1=Reset Channel D DLL
DLL_READY_READ (R)	16	0x0	0=DLL is not ready 1=DLL is ready

DYN_PWRMGT_SCLK_CNTL - RW - 32 bits - CLKIND:0xB			
Field Name	**Bits**	**Default**	**Description**
ENGINE_DYNCLK_MODE	0	0x0	0=Treat engine as one single block 1=Provide clock for each engine block separately
SCLK_DYN_START_CNTL	1	0x1	0=SCLK starts 4 clocks after BUSY active 1=SCLK starts 1 clock after BUSY active
PROG_DELAY_OFFSET	9:2	0x0	This field is used to increase latency to turn on clocks/turn off clocks. The clock turnon/turnoff latency equals to (PROG_DELAY_OFFSET+1)*<client>_PROG_DELAY_VALUE
PROG_SHUTOFF_REVERT	10	0x0	1=Use revert value of PROG_DELAY_VALUE as shutoff counter value, only used when the corresponding client's PROG_SHUTOFF is set
DYN_STOP_LAT	14:11	0x5	Delay between idle state is detected until sclk is turned off
ACTIVE_ENABLE_LAT	19:15	0x5	Delay between clock_enable changes to cg_rbbm_active changes
STATIC_SCREEN_EN	20	0x0	1=Enable Static Screen Mode
CLIENT_SELECT_POWER_EN	21	0x0	1=Enable Client Based Power Request

LOWER_POWER_STATE (R)	22	0x0	1=CG is in Lower Power State based on client's request
STATIC_SCREEN_STATE (R)	23	0x0	1=CG is in static screen state
SW_NORMAL_POWER	24	0x0	1=Force to go back to normal power state
CLIENT_BUSY_GAP_LAT	29:25	0x8	0=Number of idle cycles allowed during 2 consecutive busy cycles
Dynamic clock gating control			

DYN_PWRMGT_SCLK_LENGTH - RW - 32 bits - CLKIND:0xC			
Field Name	**Bits**	**Default**	**Description**
NORMAL_POWER_SCLK_HILEN	3:0	0x0	Post divider value for full power mode(high pulse)
NORMAL_POWER_SCLK_LOLEN	7:4	0x0	Post divider value for full power mode(low pulse)
REDUCED_POWER_SCLK_HILEN	11:8	0x1	Post divider value for reduced power mode(high pulse)
REDUCED_POWER_SCLK_LOLEN	15:12	0x1	Post divider value for reduced power mode(low pulse)
POWER_D1_SCLK_HILEN	19:16	0x2	Post divider value for D1 mode(high pulse)
POWER_D1_SCLK_LOLEN	23:20	0x2	Post divider value for D1 mode(low pulse)
STATIC_SCREEN_HILEN	27:24	0x4	Post divider value for static screen mode(high pulse)
STATIC_SCREEN_LOLEN	31:28	0x4	Post divider value for static screen mode(low pulse)
Frequency control for different power stage			

DYN_SCLK_PWMEN_PIPE - RW - 32 bits - CLKIND:0xD			
Field Name	**Bits**	**Default**	**Description**
PIPE_2D_MASK	3:0	0x1	Mask the pipe which is used by 2D
PIPE_3D_MASK	7:4	0xf	Mask the pipe which is used by 3D
PIPE_3D_NOT_AUTO	8	0x1	0=Auto disable unused pipes' clk 1=Enable pipes' clk based on PIPE_3D_MASK field
Dynamic clock gating pipe control			

DYN_SCLK_VOL_CNTL - RW - 32 bits - CLKIND:0xE			
Field Name	**Bits**	**Default**	**Description**
IO_CG_VOLTAGE_DROP	0	0x0	0=Disable dynamic core voltage drop 1=Enable dynamic core voltage drop
VOLTAGE_DROP_SYNC	2	0x0	0=Disable synchronization of reduced speed SCLK and core voltage drop 1=Enable synchronization
VOLTAGE_DELAY_SEL	22:3	0x0	Delay (in sclk cycle) between voltage goes to normal until sclk speed goes back to normal.
Static screen mode voltage control			

CP_DYN_CNTL - RW - 32 bits - CLKIND:0xF			
Field Name	**Bits**	**Default**	**Description**
CP_FORCEON	0	0x1	0=Dynamic control CP sclk branch 1=Disable dynamic control of CP sclk branch
CP_MAX_DYN_STOP_LAT	1	0x1	0=Programmable dynamic stopping latency 1=Max dynamic stopping latency
CP_CLOCK_STATUS (R)	2	0x0	0=CP branch is off 1=CP branch is on
CP_PROG_SHUTOFF	3	0x0	1=CP branch shutoff with PROG_DELAY_VALUE delay
CP_PROG_DELAY_VALUE	11:4	0x1	Delay CP clock on/off by number of cycles

CP_LOWER_POWER_IDLE	19:12	0xff	Cnt CP idle for number of cycles before dropping the power level. Only used when CP_LOWER_POWER_IGNORE is set to 0.
CP_LOWER_POWER_IGNORE	20	0x1	1=CP not vote for going to lower power state
CP_NORMAL_POWER_IGNORE	21	0x1	1=CP not vote for going back to normal power state
SPARE	23:22	0x0	
CP_NORMAL_POWER_BUSY	31:24	0xf	Cnt CP busy for number of cycles before raising the power level. Only used when CP_NORMAL_POWER_IGNORE is set to 0.
CP dynamic clock gating control			

HDP_DYN_CNTL - RW - 32 bits - CLKIND:0x10

Field Name	Bits	Default	Description
HDP_FORCEON	0	0x1	0=Dynamic control HDP sclk branch 1=Disable dynamic control of HDP sclk branch
HDP_MAX_DYN_STOP_LAT	1	0x1	0=Programmable dynamic stopping latency 1=Max dynamic stopping latency
HDP_CLOCK_STATUS (R)	2	0x0	0=HDP branch is off 1=HDP branch is on
HDP_PROG_SHUTOFF	3	0x0	1=HDP branch shutoff with PROG_DELAY_VALUE delay
HDP_PROG_DELAY_VALUE	11:4	0x1	Delay HDP clock on/off by number of cycles
HDP_LOWER_POWER_IDLE	19:12	0xff	Cnt HDP idle for number of cycles before dropping the power level. Only used when HDP_LOWER_POWER_IGNORE is set to 0
HDP_LOWER_POWER_IGNORE	20	0x1	1=HDP not vote for going to lower power state
HDP_NORMAL_POWER_IGNORE	21	0x1	1=HDP not vote for going back to normal power state
SPARE	23:22	0x0	
HDP_NORMAL_POWER_BUSY	31:24	0xf	Cnt HDP busy for number of cycles before raising the power level. Only used when HDP_NORMAL_POWER_IGNORE is set to 0
HDP dynamic clock gating control			

E2_DYN_CNTL - RW - 32 bits - CLKIND:0x11

Field Name	Bits	Default	Description
E2_FORCEON	0	0x1	0=Dynamic control E2 sclk branch 1=Disable dynamic control of E2 sclk branch
E2_MAX_DYN_STOP_LAT	1	0x1	0=Programmable dynamic stopping latency 1=Max dynamic stopping latency
E2_CLOCK_STATUS (R)	2	0x0	0=E2 branch is off 1=E2 branch is on
E2_PROG_SHUTOFF	3	0x0	1=E2 branch shutoff with PROG_DELAY_VALUE delay
E2_PROG_DELAY_VALUE	11:4	0x1	Delay E2 clock on/off by number of cycles.
E2_LOWER_POWER_IDLE	19:12	0xff	Cnt E2 idle for number of cycles before dropping the power level. Only used when E2_LOWER_POWER_IGNORE is set to 0
E2_LOWER_POWER_IGNORE	20	0x1	1=E2 not vote for going to lower power state
E2_NORMAL_POWER_IGNORE	21	0x1	1=E2 not vote for going back to normal power state
SPARE	23:22	0x0	
E2_NORMAL_POWER_BUSY	31:24	0xf	Cnt E2 busy for number of cycles before raising the power level. Only used when E2_NORMAL_POWER_IGNORE is set to 0.
E2 dynamic clock gating control			

VIP_DYN_CNTL - RW - 32 bits - CLKIND:0x14			
Field Name	**Bits**	**Default**	**Description**
VIP_FORCEON	0	0x1	0=Dynamic control VIP sclk branch 1=Disable dynamic control of VIP sclk branch
VIP_MAX_DYN_STOP_LAT	1	0x1	0=Programmable dynamic stopping latency 1=Max dynamic stopping latency
VIP_CLOCK_STATUS (R)	2	0x0	0=VIP branch is off 1=VIP branch is on
VIP_PROG_SHUTOFF	3	0x0	1=VIP branch shutoff with PROG_DELAY_VALUE delay
VIP_PROG_DELAY_VALUE	11:4	0x1	Delay VIP clock on/off by number of cycles
VIP_LOWER_POWER_IDLE	19:12	0xff	Cnt VIP idle for number of cycles before dropping the power level. Only used when VIP_LOWER_POWER_IGNORE is set to 0.
VIP_LOWER_POWER_IGNORE	20	0x1	1=VIP not vote for going to lower power state
VIP_NORMAL_POWER_IGNORE	21	0x1	1=VIP not vote for going back to normal power state
SPARE	23:22	0x0	
VIP_NORMAL_POWER_BUSY	31:24	0xf	Cnt VIP busy for number of cycles before raising the power level. Only used when VIP_NORMAL_POWER_IGNORE is set to 0.
VIP dynamic clock gating control			

TCL_DYN_CNTL - RW - 32 bits - CLKIND:0x1A			
Field Name	**Bits**	**Default**	**Description**
TCL_FORCEON	0	0x1	0=Dynamic control CP sclk branch 1=Disable dynamic control of CP sclk branch
TCL_MAX_DYN_STOP_LAT	1	0x1	0=Programmable dynamic stopping latency 1=Max dynamic stopping latency
TCL_CLOCK_STATUS (R)	2	0x0	0=TCL branch is off 1=TCL branch is on
TCL_PROG_SHUTOFF	3	0x0	1=TCL branch shutoff with PROG_DELAY_VALUE delay
TCL_PROG_DELAY_VALUE	11:4	0x1	Delay TCL clock on/off by number of cycles.
TCL dynamic clock gating control			

GA_DYN_CNTL - RW - 32 bits - CLKIND:0x1B			
Field Name	**Bits**	**Default**	**Description**
GA_FORCEON	0	0x1	0=Dynamic control GA sclk branch 1=Disable dynamic control of GA sclk branch
GA_MAX_DYN_STOP_LAT	1	0x1	0=Programmable dynamic stopping latency 1=Max dynamic stopping latency
GA_CLOCK_STATUS (R)	2	0x0	0=GA branch is off 1=GA branch is on
GA_PROG_SHUTOFF	3	0x0	1=GA branch shutoff with PROG_DELAY_VALUE delay
GA_PROG_DELAY_VALUE	11:4	0x1	Delay GA clock on/off by number of cycles.
GA dynamic clock gating control			

SU_DYN_CNTL - RW - 32 bits - CLKIND:0x15

Field Name	Bits	Default	Description
SU_FORCEON	0	0x1	0=Dynamic control SU sclk branch 1=Disable dynamic control of SU sclk branch
SU_MAX_DYN_STOP_LAT	1	0x1	0=Programmable dynamic stopping latency 1=Max dynamic stopping latency
SU_CLOCK_STATUS (R)	2	0x0	0=SU branch is off 1=SU branch is on
SU_PROG_SHUTOFF	3	0x0	1=SU branch shutoff with PROG_DELAY_VALUE delay
SU_PROG_DELAY_VALUE	11:4	0x1	Delay SU clock on/off by number of cycles.

SU dynamic clock gating control

SC_DYN_CNTL - RW - 32 bits - CLKIND:0x18

Field Name	Bits	Default	Description
SC_FORCEON	0	0x1	0=Dynamic control SC sclk branch 1=Disable dynamic control of SC sclk branch
SC_MAX_DYN_STOP_LAT	1	0x1	0=Programmable dynamic stopping latency 1=Max dynamic stopping latency
SC_CLOCK_STATUS (R)	2	0x0	0=SC branch is off 1=SC branch is on
SC_PROG_SHUTOFF	3	0x0	1=SC branch shutoff with PROG_DELAY_VALUE delay
SC_PROG_DELAY_VALUE	11:4	0x1	Delay SC clock on/off by number of cycles.

SC dynamic clock gating control

RS_DYN_CNTL - RW - 32 bits - CLKIND:0x19

Field Name	Bits	Default	Description
RS_FORCEON	0	0x1	0=Dynamic control RS sclk branch 1=Disable dynamic control of RS sclk branch
RS_MAX_DYN_STOP_LAT	1	0x1	0=Programmable dynamic stopping latency 1=Max dynamic stopping latency
RS_CLOCK_STATUS (R)	2	0x0	0=RS branch is off 1=RS branch is on
RS_PROG_SHUTOFF	3	0x0	1=RS branch shutoff with PROG_DELAY_VALUE delay
RS_PROG_DELAY_VALUE	11:4	0x1	

FG_DYN_CNTL - RW - 32 bits - CLKIND:0x17

Field Name	Bits	Default	Description
FG_FORCEON	0	0x1	0=Dynamic control FG sclk branch 1=Disable dynamic control of FG sclk branch
FG_MAX_DYN_STOP_LAT	1	0x1	0=Programmable dynamic stopping latency 1=Max dynamic stopping latency
FG_CLOCK_STATUS (R)	2	0x0	0=FG branch is off 1=FG branch is on
FG_PROG_SHUTOFF	3	0x0	1=FG branch shutoff with PROG_DELAY_VALUE delay
FG_PROG_DELAY_VALUE	11:4	0x1	Delay FG clock on/off by number of cycles.

FG dynamic clock gating control

TX_DYN_CNTL - RW - 32 bits - CLKIND:0x27			
Field Name	**Bits**	**Default**	**Description**
TX_FORCEON	0	0x1	0=Dynamic control TX sclk branch 1=Disable dynamic control of TX sclk branch
TX_MAX_DYN_STOP_LAT	1	0x1	0=Programmable dynamic stopping latency 1=Max dynamic stopping latency
TX_CLOCK_STATUS (R)	2	0x0	0=TX branch is off 1=TX branch is on
TX_PROG_SHUTOFF	3	0x0	1=TX branch shutoff with PROG_DELAY_VALUE delay
TX_PROG_DELAY_VALUE	11:4	0x0	Delay TX clock on/off by number of cycles.
TX dynamic clock gating control			

US_DYN_CNTL - RW - 32 bits - CLKIND:0x28			
Field Name	**Bits**	**Default**	**Description**
US_FORCEON	0	0x1	0=Dynamic control US sclk branch 1=Disable dynamic control of US sclk branch
US_MAX_DYN_STOP_LAT	1	0x1	0=Programmable dynamic stopping latency 1=Max dynamic stopping latency
US_CLOCK_STATUS (R)	2	0x0	0=US branch is off 1=US branch is on
US_PROG_SHUTOFF	3	0x0	1=US branch shutoff with PROG_DELAY_VALUE delay
US_PROG_DELAY_VALUE	11:4	0x0	Delay US clock on/off by number of cycles.
US dynamic clock gating control			

MC_GUI_DYN_CNTL - RW - 32 bits - CLKIND:0x1D			
Field Name	**Bits**	**Default**	**Description**
MC_GUI_FORCEON	0	0x1	0=Dynamic control MC_GUI sclk branch 1=Disable dynamic control of MC_GUI sclk branch
MC_GUI_MAX_DYN_STOP_LAT	1	0x1	0=Programmable dynamic stopping latency 1=Max dynamic stopping latency
MC_GUI_CLOCK_STATUS (R)	2	0x0	0=MC_GUI branch is off 1=MC_GUI branch is on
MC_GUI_PROG_SHUTOFF	3	0x0	1=MC_GUI branch shutoff with PROG_DELAY_VALUE delay
MC_GUI_PROG_DELAY_VALUE	11:4	0x1	Delay MC_GUI clock on/off by number of cycles.
MC_GUI dynamic clock gating control			

MC_HOST_DYN_CNTL - RW - 32 bits - CLKIND:0x1E			
Field Name	**Bits**	**Default**	**Description**
MC_HOST_FORCEON	0	0x1	0=Dynamic control MC_HOST sclk branch 1=Disable dynamic control of MC_HOST sclk branch
MC_HOST_MAX_DYN_STOP_LAT	1	0x1	0=Programmable dynamic stopping latency 1=Max dynamic stopping latency
MC_HOST_CLOCK_STATUS (R)	2	0x0	0=MC_HOST branch is off 1=MC_HOST branch is on
MC_HOST_PROG_SHUTOFF	3	0x0	1=MC_HOST branch shutoff with PROG_DELAY_VALUE delay
MC_HOST_PROG_DELAY_VALUE	11:4	0x1	Delay MC_HOST clock on/off by number of cycles.
MC_HOST dynamic clock gating control			

MC_RBS_DYN_CNTL - RW - 32 bits - CLKIND:0x26			
Field Name	**Bits**	**Default**	**Description**
MC_RBS_FORCE	0	0x1	0=Dynamic control CP sclk branch 1=Disable dynamic control of CP sclk branch
MC_RBS_MAX_DYN_STOP_LAT	1	0x1	0=Programmable dynamic stopping latency 1=Max dynamic stopping latency
MC_RBS_CLOCK_STATUS (R)	2	0x0	0=MC_RBS branch is off 1=MC_RBS branch is on
MC_RBS_PROG_SHUTOFF	3	0x0	1=MC_RBS branch shutoff with PROG_DELAY_VALUE delay
MC_RBS_PROG_DELAY_VALUE	11:4	0x1	Delay MC_RBS clock on/off by number of cycles.
MC_RBS dynamic clock gating control			

CG_MISC_REG - RW - 32 bits - CLKIND:0x1F			
Field Name	**Bits**	**Default**	**Description**
STARTUP_COUNTER	11:0	0x28	Not used.
SYNCHRONIZER_COUNTER	15:12	0x8	For debugging purposes. Number of cycles to be used by the clock switch logic.
DISPCLK_FUNC_SEL	16	0x0	1=Use non functional display clock
SPARE	23:17	0x0	
Misc control			

CG_DEBUG - RW - 32 bits - CLKIND:0x20			
Field Name	**Bits**	**Default**	**Description**
TEST_MODE	0	0x0	1=Disable long internal timing to speed up regression tests

MCLK_MISC - RW - 32 bits - CLKIND:0x22			
Field Name	**Bits**	**Default**	**Description**
SPARE_0	1:0	0x0	
MRDCKA0_SOUTSEL	3:2	0x0	0=DLL output clock 1=QS pin 2=QS delayed 2 elements 3=QS delayed 4 elements
MRDCKA1_SOUTSEL	5:4	0x0	0=DLL output clock 1=QS pin 2=QS delayed 2 elements 3=QS delayed 4 elements
MRDCKB0_SOUTSEL	7:6	0x0	0=DLL output clock 1=QS pin 2=QS delayed 2 elements 3=QS delayed 4 elements
MRDCKB1_SOUTSEL	9:8	0x0	0=DLL output clock 1=QS pin 2=QS delayed 2 elements 3=QS delayed 4 elements
MRDCKC0_SOUTSEL	11:10	0x0	0=DLL output clock 1=QS pin 2=QS delayed 2 elements 3=QS delayed 4 elements
MRDCKC1_SOUTSEL	13:12	0x0	0=DLL output clock 1=QS pin 2=QS delayed 2 elements 3=QS delayed 4 elements
MRDCKD0_SOUTSEL	15:14	0x0	0=DLL output clock 1=QS pin 2=QS delayed 2 elements 3=QS delayed 4 elements
MRDCKD1_SOUTSEL	17:16	0x0	0=DLL output clock 1=QS pin 2=QS delayed 2 elements 3=QS delayed 4 elements
MCLK_NONFUNC_SEL	18	0x0	0=Select functional mclk source 1=Select non-functional mode mclk source
SPARE	31:19	0x0	

DLL_CNTL - RW - 32 bits - CLKIND:0x23			
Field Name	**Bits**	**Default**	**Description**
DLL_RESET_TIME	9:0	0x1f4	Number of cycles required to hold DLL reset high
DLL_LOCK_TIME	21:12	0xfa	Number of cycles required to wait for DLL get locked
DLL control register			

SPLL_TIME - RW - 32 bits - CLKIND:0x24			
Field Name	**Bits**	**Default**	**Description**
SPLL_LOCK_TIME	15:0	0x2000	
SPLL_RESET_TIME	31:16	0x1f4	

MPLL_TIME - RW - 32 bits - CLKIND:0x25			
Field Name	**Bits**	**Default**	**Description**
MPLL_LOCK_TIME	15:0	0x2000	
MPLL_RESET_TIME	31:16	0x1f4	

DYN_BACKBIAS_CNTL - RW - 32 bits - CLKIND:0x29			
Field Name	**Bits**	**Default**	**Description**
IO_CG_BACKBIAS_EN	0	0x0	0=Disable dynamic back bias switching 1=Enable dynamic back bias switching
BACKBIAS_SYNC	1	0x0	0=Disable synchronization of reduced speed SCLK and back bias switching 1=Enable synchronization
BACKBIAS_DELAY_SEL	22:3	0x0	Delay (in sclk cycle) between backbias disabled until sclk speed goes back to normal.
Static screen mode backbias control			

POLARITY_CNTL - RW - 32 bits - CLKIND:0x2A			
Field Name	**Bits**	**Default**	**Description**
IO_BACKBIAS_POLARITY	0	0x1	0=Negative 1=Positive
IO_VOLTAGE_REGULATOR_POLARITY	1	0x1	0=Negative 1=Positivie

OVERCLOCK_CNTL - RW - 32 bits - CLKIND:0x2B			
Field Name	**Bits**	**Default**	**Description**
OVERCLOCK_PROTECTION_SCLK	0	0x0	0=Disable 1=Enable
OVERCLOCK_PENALTY	13:4	0x10	

ERROR_STATUS - RW - 32 bits - CLKIND:0x2C			
Field Name	**Bits**	**Default**	**Description**
OVERCLOCK_DETECTION_SCLK (R)	0	0x0	0=No overclock for SCLK 1=SCLK overclock
OVERCLOCK_DETECTION_YCLK (R)	1	0x0	0=No overclock for YCLK 1=YCLK overclock
SPLL_UNLOCK (R)	2	0x0	
YPLL_UNLOCK (R)	3	0x0	

CC_FUSE_STRAPS_0 - R - 32 bits - CLKIND:0x2D			
Field Name	**Bits**	**Default**	**Description**
MAX_PIPES	1:0	0x0	0=4 1=3 2=2 3=1
OVERCLOCK_DIS	2	0x0	0=Enable Overclocking 1=Disable Overclocking
MOBILE_DIS	3	0x0	0=Enable Mobile 1=Disable Mobile
WS_DIS	4	0x0	0=Enable Workstation 1=Disable Workstation
MAX_MPS	7:5	0x0	0=8 1=7 2=6 3=5 4=4 5=3 6=2 7=1
BAD_PIPES	11:8	0x0	Bad Pipe Mask. Each set bit indicates that the corresponding pipe has been marked as bad.
MAX_MEM_CHANNELS	13:12	0x0	0=Four channels 1=Reserved 2=Two channels 3=One channel
ROM_DIS	14	0x0	0=Include ROM straps 1=Ignore ROM straps
DEBUG_DIS	15	0x0	0=Include DEBUG straps 1=Ignore DEBUG straps
MAX_SCLK	23:16	0x0	
MAX_MCLK	31:24	0x0	
Fuse Strap Values. Corresponds to on-die fuses 71-40. See CC_COMBINED_STRAPS_0 register for details.			

CC_FUSE_STRAPS_1 - R - 32 bits - CLKIND:0x2E			
Field Name	**Bits**	**Default**	**Description**
DEVICE_ID	15:0	0x0	
MAJOR_REV_ID	19:16	0x0	
MINOR_REV_ID	23:20	0x0	
ATI_REV_ID	27:24	0x0	
STRAP_MODE	29:28	0x0	0=4 PIPES/4 CHANNELS/8 VAPS 1=2 PIPES/2 CHANNELS/ALL VAPS 2=1 PIPE/2 CHANNELS/ALL VAPS
Fuse Strap Values. Corresponds to on-die fuses 103-72. See CC_COMBINED_STRAPS_1 values for details.			

CC_DEBUG_STRAPS_0 - RW - 32 bits - CLKIND:0x2F			
Field Name	**Bits**	**Default**	**Description**
MAX_PIPES	1:0	0x0	0=4 1=3 2=2 3=1
OVERCLOCK_DIS	2	0x0	0=Enable Overclocking 1=Disable Overclocking
MOBILE_DIS	3	0x0	0=Enable Mobile 1=Disable Mobile
WS_DIS	4	0x0	0=Enable Workstation 1=Disable Workstation
MAX_MPS	7:5	0x0	0=8 1=7 2=6 3=5 4=4 5=3 6=2 7=1
BAD_PIPES	11:8	0x0	
MAX_MEM_CHANNELS	13:12	0x0	0=Four channels 1=Reserved 2=Two channels 3=One channel
ROM_DIS	14	0x0	0=Include ROM straps 1=Ignore ROM straps
DEBUG_DIS	15	0x0	0=Include DEBUG straps 1=Ignore DEBUG straps
MAX_SCLK	23:16	0x0	
MAX_MCLK	31:24	0x0	

CC_DEBUG_STRAPS_1 - RW - 32 bits - CLKIND:0x30			
Field Name	**Bits**	**Default**	**Description**
DEVICE_ID	15:0	0x0	
MAJOR_REV_ID	19:16	0x0	
MINOR_REV_ID	23:20	0x0	
ATI_REV_ID	27:24	0x0	
STRAP_MODE	29:28	0x0	0=4 PIPES/4 CHANNELS/8 VAPS 1=2 PIPES/2 CHANNELS/ALL VAPS 2=1 PIPE/2 CHANNELS/ALL VAPS
Debug Strap Values. See CC_COMBINED_STRAPS_1 values for details.			

CC_IO_STRAPS - R - 32 bits - CLKIND:0x31			
Field Name	**Bits**	**Default**	**Description**
MAX_PIPES	1:0	0x0	0=4 1=3 2=2 3=1
OVERCLOCK_DIS	2	0x0	0=Enable Overclocking 1=Disable Overclocking
MOBILE_DIS	3	0x0	0=Enable Mobile 1=Disable Mobile
WS_DIS	4	0x0	0=Enable Workstation 1=Disable Workstation
DEVICE_ID	9:5	0x0	Device ID 5 LSBs.
MAX_MEM_CHANNELS	11:10	0x0	0=Four channels 1=Reserved 2=Two channels 3=One channel
IO Straps/Substrate Fuses. See CC_COMBINED_STRAPS_# registers for more details.			

CC_IO_STRAPS_22A - R - 32 bits - CLKIND:0x31			
Field Name	**Bits**	**Default**	**Description**
MAX_PIPES	0	0x0	0=2 1=1
EXTRA_0	1	0x0	
OVERCLOCK_DIS	2	0x0	0=Enable Overclocking 1=Disable Overclocking
MOBILE_DIS	3	0x0	0=Enable Mobile 1=Disable Mobile
WS_DIS	4	0x0	0=Enable Workstation 1=Disable Workstation
DEVICE_ID	9:5	0x0	Device ID 5 LSBs.
MAX_MEM_CHANNELS	10	0x0	0=Two channels 1=One channel
EXTRA_1	11	0x0	
EXTRA_2	12	0x0	
EXTRA_3	13	0x0	
EXTRA_4	14	0x0	
Obsolete. Use CC_IO_STRAPS. IO Straps/Substrate Fuses in CC_STRAP_MODE_22A. See CC_COMBINED_STRAPS_# registers for more details.			

CC_IO_STRAPS_12A - R - 32 bits - CLKIND:0x31			
Field Name	**Bits**	**Default**	**Description**
EXTRA_0	0	0x0	
EXTRA_1	1	0x0	
OVERCLOCK_DIS	2	0x0	0=Enable Overclocking 1=Disable Overclocking
MOBILE_DIS	3	0x0	0=Enable Mobile 1=Disable Mobile
WS_DIS	4	0x0	0=Enable Workstation 1=Disable Workstation
DEVICE_ID	9:5	0x0	Device ID 5 LSBs.
MAX_MEM_CHANNELS	10	0x0	0=Two channels 1=One channel
EXTRA_2	11	0x0	
EXTRA_3	12	0x0	
EXTRA_4	13	0x0	
EXTRA_5	14	0x0	
Obsolete. Use CC_IO_STRAPS. IO Straps/Substrate Fuses in CC_STRAP_MODE_12A. See CC_COMBINED_STRAPS_# registers for more details.			

CC_ROM_STRAPS - R - 32 bits - CLKIND:0x32			
Field Name	**Bits**	**Default**	**Description**
DEVICE_ID	15:0	0x0	
MAX_PIPES	17:16	0x0	0=4 1=3 2=2 3=1
OVERCLOCK_DIS	18	0x0	0=Enable Overclocking 1=Disable Overclocking
MOBILE_DIS	19	0x0	0=Enable Mobile 1=Disable Mobile
WS_DIS	20	0x0	0=Enable Workstation 1=Disable Workstation
MAX_MEM_CHANNELS	23:22	0x0	0=Four channels 1=Reserved 2=Two channels 3=One channel
BAD_PIPES	27:24	0x0	
Strap Values from ROM. See CC_COMBINED_STRAPS_# registers for details.			

CC_COMBINED_STRAPS_0 - R - 32 bits - CLKIND:0x33			
Field Name	**Bits**	**Default**	**Description**
MAX_PIPES	1:0	0x0	Maximum Number of Raster Pipes. Default: All 4 raster pipes (16 pixels) can be enabled by software. 0=4 1=3 2=2 3=1
OVERCLOCK_DIS	2	0x0	Enables a circuit to switch the core clock frequency to the PCIE reference clock when either the core, or the memory clock, frequency is detected to be above the value set by the MAX_SCLK or MAX_MCLK strap settings. Each clock is monitored independently, but only the core clock is throttled. Default: No overclock protection. 0=Enable Overclocking 1=Disable Overclocking
MOBILE_DIS	3	0x0	Disables LVDS. Default: LVDS can be enabled by software. 0=Enable Mobile 1=Disable Mobile
WS_DIS	4	0x0	Workstation Disable. Just informational. Default: Workstation features can be enabled by software. 0=Enable Workstation 1=Disable Workstation
MAX_MPS	7:5	0x0	0=8 1=7 2=6 3=5 4=4 5=3 6=2 7=1
BAD_PIPES	11:8	0x0	Bad Pipe Mask. Each bit position set to 1 indicates that the corresponding pipe has been marked as bad.
MAX_MEM_CHANNELS	13:12	0x0	Maximum number of memory channels that can be enabled by software. 0=Four channels 1=Reserved 2=Two channels 3=One channel
ROM_DIS	14	0x0	Disable ROM straps. Ignore the ROM straps when calculating the combined strap values. Default: ROM straps can affect strap values. 0=Include ROM straps 1=Ignore ROM straps
DEBUG_DIS	15	0x0	Disable debug strap settings. Setting this bit prevents software from setting Chip Configuration straps. This bit should be set for production parts. Default: Software can write debug strap settings. 0=Include DEBUG straps 1=Ignore DEBUG straps
MAX_SCLK	23:16	0x0	Maximum ratio of core clock to pcie reference clock in 4.4 fixed point. Default: 0 = 16 15/16.
MAX_MCLK	31:24	0x0	Maximum ratio of memory clock to pcie reference clock in 5.3 fixed point. Default: 0 = 32 7/8.
Working Set of Strap Values based on FUSE, IO, ROM and DEBUG Strap values.			

CC_COMBINED_STRAPS_1 - R - 32 bits - CLKIND:0x34			
Field Name	**Bits**	**Default**	**Description**
DEVICE_ID	15:0	0x0	PCI Device ID
MAJOR_REV_ID	19:16	0x0	PCI Major Revision ID
MINOR_REV_ID	23:20	0x0	PCI Minor Revision ID
ATI_REV_ID	27:24	0x0	Internal Revision ID
STRAP_MODE	29:28	0x0	Obsolete. The different strap modes allows the IO straps to be used for other purposes (in particular, identifying packages). For CC_STRAP_MODE_22A, use CC_IO_STRAP_22A to get the fuse values. For CC_STRAP_MODE_12A, use CC_IO_STRAP_12A. 0=4 PIPES/4 CHANNELS/8 VAPS 1=2 PIPES/2 CHANNELS/ALL VAPS 2=1 PIPE/2 CHANNELS/ALL VAPS
Working Chip Configuration Strap Values based on Fuse, I/O and ROM Strap values.			

CG_CLKPIN_CNTL - RW - 32 bits - CLKIND:0x35			
Field Name	**Bits**	**Default**	**Description**
OSC_EN	0	0x1	0=Disable Oscillation 1=Enable Oscillation
XTL_LOW_GAIN	1	0x1	0=High Gain 1=Low Gain
CG_CLK_TO_OUTPIN	2	0x0	0=Disabled 1=Send out selected clock for jitter test
OSC_USE_CORE	3	0x0	0=Pad routing OSC 1=Core routing OSC

VOL_DROP_CNT - RW - 32 bits - CLKIND:0x36			
Field Name	**Bits**	**Default**	**Description**
VOL_DROP_DELAY	31:0	0x100	Delay (in sclk cycle) between static screen condition is detected until the voltage is dropped.
Static screen mode voltage control			

BACKBIAS_ENABLE_CNT - RW - 32 bits - CLKIND:0x37			
Field Name	**Bits**	**Default**	**Description**
BB_ENABLE_DELAY	31:0	0x100	Delay (in sclk cycle) between static screen condition is detected until backbias is enabled.
Static screen mode backbias control			

CG_TC_JTAG_0 - RW - 32 bits - CLKIND:0x38			
Field Name	**Bits**	**Default**	**Description**
CG_TC_TMS	7:0	0x0	8 consecutive values for TMS. Bit [0] is sent first.
CG_TC_TDI	15:8	0x0	8 consecutive values for TDI. Bit [0] is sent first.
CG_TC_MODE	17:16	0x0	Indicates what clock should be used for TCK in the jtag transactions. 0=No Clock 1=PCIE Reference Clock / 4 2=PCIE Reference Clock / 10 3=PCIE Reference Clock / 20
CG_TC_TDO_MASK	31:24	0x0	A mask indicating whether the TDO value should be read back for a given JTAG cycle. Bit [0] corresponds to the first TDO sample. This mask can be used to prevent the readback of unknown values across the bus interface during simulation. This field can be set to all 1's on real hardware.
CG Interface to the Test Controller (TC) using IEEE JTAG protocol. This register can be written with 8 consecutive values for the inputs to the TC's JTAG port. These 8 inputs are sent at consecutive TCK clock edges. The final value is held for indefinitely many TCK clock edges until the next write to this register. The register can be used to walk through several states of the JTAG state machine and typically the state machine would be left in a 'paused' state. The TDO values sampled at the 8 edges for which input was provided is available for readback from the TC_CG_TDO field of the CG_TC_JTAG_1 register.			

CG_TC_JTAG_1 - R - 32 bits - CLKIND:0x39			
Field Name	**Bits**	**Default**	**Description**
TC_CG_TDO	7:0	0x0	8 consecutive sampled values of TDO. Bit [0] corresponds to the cycle that the first bit of CG_TC_JTAG_0.CG_TC_TMS and CG_TC_JTAG_0.CG_TC_TDI were sampled by the Test Controller.
TC_CG_DONE	31	0x0	Indicates whether the JTAG sequence has completed. 0=We have completed less than 8 JTAG cycles since the last write to CG_TC_JTAG_0 1=All 8 JTAG cycles have been completed since the last write to CG_TC_JTAG_0
TDO readback and status bits for the CG JTAG interface described in more detail in the CG_TC_JTAG_0 register description.			

FVTHROT_CNTRL_REG - RW - 32 bits - CLKIND:0x3A			
Field Name	**Bits**	**Default**	**Description**
DontWaitForFbDivWrap	0	0x0	
Minimum_Considered_Idle_Period	24:1	0x0	
Refresh_Rate_Divisor	26:25	0x0	
EnableFV_Throt	27	0x0	0=Enable frequency/voltage scaling
EnableFV_Update	28	0x0	0=Enable frequency/voltage updates
TrendSelMode	29	0x0	0=Determine trend using just last frame or last 4 frames
ForceTrendSel	30	0x0	0=Force up or down trend
EnableFV_ThrotIO	31	0x0	0=Enable the OE of the pad used for PWM.

FVTHROT_TARGET_REG - RW - 32 bits - CLKIND:0x3B			
Field Name	**Bits**	**Default**	**Description**
TargetIdleCount	23:0	0x0	

FVTHROT_COMPARE_BOUND1 - RW - 32 bits - CLKIND:0x3C			
Field Name	**Bits**	**Default**	**Description**
Compare1_Boundary	23:0	0x0	

FVTHROT_COMPARE_BOUND2 - RW - 32 bits - CLKIND:0x3D			
Field Name	**Bits**	**Default**	**Description**
Compare2_Boundary	23:0	0x0	

FVTHROT_COMPARE_BOUND3 - RW - 32 bits - CLKIND:0x3E			
Field Name	**Bits**	**Default**	**Description**
Compare3_Boundary	23:0	0x0	

FVTHROT_COMPARE_BOUND4 - RW - 32 bits - CLKIND:0x3F			
Field Name	**Bits**	**Default**	**Description**
Compare4_Boundary	23:0	0x0	

FVTHROT_UPTREND_COEF0 - RW - 32 bits - CLKIND:0x40			
Field Name	**Bits**	**Default**	**Description**
UpTrendCoefficient0	9:0	0x0	
UpTrendCoefficient1	19:10	0x0	
UpTrendCoefficient2	29:20	0x0	

FVTHROT_UPTREND_COEF1 - RW - 32 bits - CLKIND:0x41			
Field Name	**Bits**	**Default**	**Description**
UpTrendCoefficient3	9:0	0x0	
UpTrendCoefficient4	19:10	0x0	
UpTrendCoefficient5	29:20	0x0	

FVTHROT_UPTREND_COEF2 - RW - 32 bits - CLKIND:0x42			
Field Name	**Bits**	**Default**	**Description**
UpTrendCoefficient6	9:0	0x0	
UpTrendCoefficient7	19:10	0x0	
UpTrendCoefficient8	29:20	0x0	

FVTHROT_UPTREND_COEF3 - RW - 32 bits - CLKIND:0x43			
Field Name	**Bits**	**Default**	**Description**
UpTrendCoefficient9	9:0	0x0	
UpTrendCoefficient10	19:10	0x0	
UpTrendCoefficient11	29:20	0x0	

FVTHROT_UPTREND_COEF4 - RW - 32 bits - CLKIND:0x44			
Field Name	**Bits**	**Default**	**Description**
UpTrendCoefficient12	9:0	0x0	
UpTrendCoefficient13	19:10	0x0	
UpTrendCoefficient14	29:20	0x0	

FVTHROT_DOWNTREND_COEF0 - RW - 32 bits - CLKIND:0x45			
Field Name	**Bits**	**Default**	**Description**
DownTrendCoefficient0	9:0	0x0	
DownTrendCoefficient1	19:10	0x0	
DownTrendCoefficient2	29:20	0x0	

FVTHROT_DOWNTREND_COEF1 - RW - 32 bits - CLKIND:0x46			
Field Name	**Bits**	**Default**	**Description**
DownTrendCoefficient3	9:0	0x0	
DownTrendCoefficient4	19:10	0x0	
DownTrendCoefficient5	29:20	0x0	

FVTHROT_DOWNTREND_COEF2 - RW - 32 bits - CLKIND:0x47			
Field Name	**Bits**	**Default**	**Description**
DownTrendCoefficient6	9:0	0x0	
DownTrendCoefficient7	19:10	0x0	
DownTrendCoefficient8	29:20	0x0	

FVTHROT_DOWNTREND_COEF3 - RW - 32 bits - CLKIND:0x48			
Field Name	**Bits**	**Default**	**Description**
DownTrendCoefficient9	9:0	0x0	
DownTrendCoefficient10	19:10	0x0	
DownTrendCoefficient11	29:20	0x0	

FVTHROT_DOWNTREND_COEF4 - RW - 32 bits - CLKIND:0x49			
Field Name	**Bits**	**Default**	**Description**
DownTrendCoefficient12	9:0	0x0	
DownTrendCoefficient13	19:10	0x0	
DownTrendCoefficient14	29:20	0x0	

FVTHROT_FBDIV_REG0 - RW - 32 bits - CLKIND:0x4A			
Field Name	**Bits**	**Default**	**Description**
MinFeedbackDiv	11:0	0x0	
MaxFeedbackDiv	23:12	0x0	

FVTHROT_FBDIV_REG1 - RW - 32 bits - CLKIND:0x4B			
Field Name	**Bits**	**Default**	**Description**
MaxFeedbackStep	11:0	0x0	
StartingFeedbackDiv	23:12	0x0	
ForceFeedbackDiv	24	0x0	

FVTHROT_FBDIV_REG2 - RW - 32 bits - CLKIND:0x4C

Field Name	Bits	Default	Description
ForcedFeedbackDiv	11:0	0x0	
FbDivTimerVal	27:12	0x0	

FVTHROT_FB_UPSTEP_REG0 - RW - 32 bits - CLKIND:0x4D

Field Name	Bits	Default	Description
FeedbackDivUpStepsize1	11:0	0x0	
FeedbackDivUpStepsize2	23:12	0x0	

FVTHROT_FB_UPSTEP_REG1 - RW - 32 bits - CLKIND:0x4E

Field Name	Bits	Default	Description
FeedbackDivUpStepsize3	11:0	0x0	
FeedbackDivUpStepsize4	23:12	0x0	

FVTHROT_FB_DOWNSTEP_REG0 - RW - 32 bits - CLKIND:0x4F

Field Name	Bits	Default	Description
FeedbackDivDownStepsize1	11:0	0x0	
FeedbackDivDownStepsize2	23:12	0x0	

FVTHROT_FB_DOWNSTEP_REG1 - RW - 32 bits - CLKIND:0x50

Field Name	Bits	Default	Description
FeedbackDivDownStepsize3	11:0	0x0	
FeedbackDivDownStepsize4	23:12	0x0	

FVTHROT_PWM_CTRL_REG0 - RW - 32 bits - CLKIND:0x51

Field Name	Bits	Default	Description
StartingPWM_HighTime	11:0	0x0	
NumberOfCyclesInPeriod	23:12	0x0	
ForceStartingPWM_HighTime	24	0x0	
InvertPWM_Waveform	25	0x0	

FVTHROT_PWM_CTRL_REG1 - RW - 32 bits - CLKIND:0x52

Field Name	Bits	Default	Description
MinimumPWM_HighTime	11:0	0x0	
MaximumPWM_HighTime	23:12	0x0	

FVTHROT_PWM_UPSTEP_REG0 - RW - 32 bits - CLKIND:0x53

Field Name	Bits	Default	Description
PWM_HighTimeUpStepsize1	11:0	0x0	
PWM_HighTimeUpStepsize2	23:12	0x0	

FVTHROT_PWM_UPSTEP_REG1 - RW - 32 bits - CLKIND:0x54

Field Name	Bits	Default	Description
PWM_HighTimeUpStepsize3	11:0	0x0	
PWM_HighTimeUpStepsize4	23:12	0x0	

FVTHROT_PWM_DOWNSTEP_REG0 - RW - 32 bits - CLKIND:0x55

Field Name	Bits	Default	Description
PWM_HighTimeDownStepsize1	11:0	0x0	
PWM_HighTimeDownStepsize2	23:12	0x0	

FVTHROT_PWM_DOWNSTEP_REG1 - RW - 32 bits - CLKIND:0x56

Field Name	Bits	Default	Description
PWM_HighTimeDownStepsize3	11:0	0x0	
PWM_HighTimeDownStepsize4	23:12	0x0	

FVTHROT_STATUS_REG0 - R - 32 bits - CLKIND:0x57

Field Name	Bits	Default	Description
CurrentFeedbackDiv	11:0	0x0	
REG_CURRENT_PWM_HIGHTIME	23:12	0x0	
REG_COMPARE_RESULT	27:24	0x0	0=Last result of measured vs. target idle time comparison.
REG_UpDown	28	0x0	0=Current value of the UpDown indicator in the circuit.
PWM	29	0x0	0=Current value of the PWM output.

FVTHROT_STATUS_REG1 - R - 32 bits - CLKIND:0x58

Field Name	Bits	Default	Description
REG_LAST_ICOUNT	23:0	0x0	

FVTHROT_STATUS_REG2 - R - 32 bits - CLKIND:0x59

Field Name	Bits	Default	Description
REG_LAST_FILTERED_ICOUNT	23:0	0x0	

CG_SPLL_ANALOG_CTRL0 - RW - 32 bits - CLKIND:0x5A

Field Name	Bits	Default	Description
IVCOREF2	2:0	0x0	0=VCO Input 2 Voltage Control.
IVCOREF1	5:3	0x0	0=VCO Input 1 Voltage Control.
IVCO	13:6	0x87	0=VCO Gain/duty cycle adjustment.
IBIAS	15:14	0x0	0=Bias Generator Adjustment.
ILF	17:16	0x0	0=Loop Filter Adjustment.
IPCP	21:18	0x4	0=Charge Pump Adjustment.
IVCODIV	24:22	0x0	0=VCO Output Divider Setting.
ISPEC	27:25	0x0	0=Lock Detect Static Phase Error Control.
IACU	30:28	0x0	0=Lock Detect Analysis Unlock Control.
ILDRESET	31	0x0	0=Lock Detect Manual Reset.

CG_SPLL_ANALOG_CTRL1 - RW - 32 bits - CLKIND:0x5B

Field Name	Bits	Default	Description
IACL	2:0	0x0	0=Lock Detect Analysis Lock Control.
ITMONENVI	3	0x0	0=VI Access Point Enable.
ITMONENVC	4	0x0	0=VC Access Points Enable.
SPARE_BITS	31:5	0x0	

CG_INTGFX_MISC - RW - 32 bits - CLKIND:0x5C

Field Name	Bits	Default	Description
BIF_SCLK_GATING_EN	0	0x0	0=Enable BIF SCLK Gating
BCLK_FREQ_SEL	1	0x0	0=0: BCLK is 100MHz, 1: BCLK is SCLK/2
AZ_SCLK_GATING_EN	2	0x0	0=Enable Azalia SCLK Gating
AZ_D3D0_RST_EN	3	0x0	0=Enable reset pulse on Azalia exiting D3
CG_IO_DAC_SDA_GPIO_A	4	0x0	0=DAC_SDA GPIO A bit
CG_IO_DAC_SDA_GPIO_MASK	5	0x0	0=DAC_SDA GPIO Mask bit
CG_IO_DAC_SDA_GPIO_EN	6	0x0	0=DAC_SDA GPIO EN bit
CG_IO_DAC_SDA_GPIO_OD	7	0x0	0=DAC_SDA GPIO OD bit
CG_INTGFX_MISC_SPARE	31:8	0x0	

CG_INTGFX_SPARE_RO - R - 32 bits - CLKIND:0x5D

Field Name	Bits	Default	Description
INTGFX_SPARE_RO	31:0	0x0	

FVTHROT_PWM_FEEDBACK_DIV_REG1 - RW - 32 bits - CLKIND:0x5E

Field Name	Bits	Default	Description
Range0_PWMFeedbackDiv	11:0	0x0	
RangePWMFeedbackDivEn	12	0x0	0=Enable PWM Look Up As Function Of FbDiv
FVTHROT_PWM_FEEDBACK_DIV_REG 1_SPARE_BITS	31:13	0x0	

FVTHROT_PWM_FEEDBACK_DIV_REG2 - RW - 32 bits - CLKIND:0x5F

Field Name	Bits	Default	Description
Range1_PWMFeedbackDiv	11:0	0x0	
Range2_PWMFeedbackDiv	23:12	0x0	
FVTHROT_PWM_FEEDBACK_DIV_REG 2_SPARE_BITS	31:24	0x0	

FVTHROT_PWM_FEEDBACK_DIV_REG3 - RW - 32 bits - CLKIND:0x60

Field Name	Bits	Default	Description
Range0_PWM	11:0	0x0	
Range1_PWM	23:12	0x0	
FVTHROT_PWM_FEEDBACK_DIV_REG 3_SPARE_BITS	31:24	0x0	

FVTHROT_PWM_FEEDBACK_DIV_REG4 - RW - 32 bits - CLKIND:0x61

Field Name	Bits	Default	Description
Range2_PWM	11:0	0x0	
Range3_PWM	23:12	0x0	
FVTHROT_PWM_FEEDBACK_DIV_REG 4_SPARE_BITS	31:24	0x0	

FVTHROT_SPLL_PARAM_FEEDBACK_DIV_REG1 - RW - 32 bits - CLKIND:0x62			
Field Name	**Bits**	**Default**	**Description**
Range0_SpllParamFeedbackDiv	11:0	0x0	
RangeSpllParamFeedbackDivEn	12	0x0	0=Enable SPLL Param As Function Of FbDiv
FVTHROT_SPLL_PARAM_FEEDBACK_DIV_REG1_SPARE_BITS	31:13	0x0	

FVTHROT_SPLL_PARAM_FEEDBACK_DIV_REG2 - RW - 32 bits - CLKIND:0x63			
Field Name	**Bits**	**Default**	**Description**
Range1_SpllParamFeedbackDiv	11:0	0x0	
Range2_SpllParamFeedbackDiv	23:12	0x0	
FVTHROT_SPLL_PARAM_FEEDBACK_DIV_REG2_SPARE_BITS	31:24	0x0	

FVTHROT_SPLL_PARAM_FEEDBACK_DIV_REG3 - RW - 32 bits - CLKIND:0x64			
Field Name	**Bits**	**Default**	**Description**
Range0_SpllParam	15:0	0x0	
Range1_SpllParam	31:16	0x0	

FVTHROT_SPLL_PARAM_FEEDBACK_DIV_REG4 - RW - 32 bits - CLKIND:0x65			
Field Name	**Bits**	**Default**	**Description**
Range2_SpllParam	15:0	0x0	
Range3_SpllParam	31:16	0x0	

FVTHROT_SLOW_CLK_FEEDBACK_DIV_REG1 - RW - 32 bits - CLKIND:0x66			
Field Name	**Bits**	**Default**	**Description**
Range0_SlowClkFeedbackDiv	11:0	0x0	
RangeSlowClkFeedbackDivEn	12	0x0	0=Enable Slow Clk As Function Of FbDiv
FVTHROT_SLOW_CLK_FEEDBACK_DIV_REG1_SPARE_BITS	31:13	0x0	

FVTHROT_SCALE_FEEDBACK_DIV_REG1 - RW - 32 bits - CLKIND:0x67			
Field Name	**Bits**	**Default**	**Description**
Range0_ScaleFeedbackDiv	11:0	0x0	
Range1_ScaleFeedbackDiv	23:12	0x0	
RangeScaleFeedbackDivEn	24	0x0	0=Enable Feedback and Post Dividers Scaled As Function Of FVTHROT_FbDiv
FVTHROT_SCALE_FEEDBACK_DIV_REG1_SPARE_BITS	31:25	0x0	

2.11 DAC Control

VGA DAC Registers

DAC_DATA - RW - 8 bits - VGA_IO:0x3C9			
Field Name	**Bits**	**Default**	**Description**
DAC_DATA	7:0	0x0	VGA Palette (DAC) Data. Use DAC_R_INDEX and DAC_W_INDEX to set read or write mode, and entry to access. Access order is Red, Green, Blue, and then auto-increment occurs to next entry. DAC_8BIT_EN controls whether 6 or 8 bit access.
VGA Palette (DAC) Data.			

DAC_MASK - RW - 8 bits - VGA_IO:0x3C6			
Field Name	**Bits**	**Default**	**Description**

DAC_MASK	7:0	0x0	Masks off usage of individual palette index bits before pixel index is looked-up in the palette.
			  0=Do not use this bit of the index
			  1=Use this bit of the index
			Only has an effect in VGA emulation modes (CRTC_EXT_DISP_EN=0), not for VESA modes or extended display modes.

Palette index mask for VGA emulation modes.			

DAC_R_INDEX - RW - 8 bits - VGA_IO:0x3C7			
Field Name	**Bits**	**Default**	**Description**

DAC_R_INDEX	7:0	0x0	Write: Sets the index for a palette (DAC) read operation. Index auto-increments after every third read of DAC_DATA.
			Read: Indicates if palette in read or write mode.
			  0=Palette in write mode (DAC_W_INDEX last written).
			  3=Palette in read mode (DAC_R_INDEX last written).
			Also see DAC_W_INDEX.

Palette (DAC) Read Index.			

DAC_W_INDEX - RW - 8 bits - VGA_IO:0x3C8			
Field Name	**Bits**	**Default**	**Description**
DAC_W_INDEX	7:0	0x0	Sets the index for a palette (DAC) write operation. Index auto-increments after every third write of DAC_DATA. Also see DAC_R_INDEX.
Palette (DAC) Write Index.			

2.12 VGA Control/Status

GENFC_RD - R - 8 bits - VGA_IO:0x3CA			
Field Name	**Bits**	**Default**	**Description**

VSYNC_SEL_R
 	
(mirror of GENFC_WT:VSYNC_SEL_W)
	3	0x0	Vertical sync select (read).
			   0=Normal vertical sync
			   1=Sync is 'vertical sync' ORed with 'vertical display enable

Feature Control register (Read).			

GENFC_WT - W - 8 bits - [VGA_IO:0x3BA] [VGA_IO:0x3DA]			
Field Name	**Bits**	**Default**	**Description**

VSYNC_SEL_W	3	0x0	Vertical sync select (write).
			   0=Normal vertical sync
			   1=Sync is 'vertical sync' ORed with 'vertical display enable

Feature Control register (Read).			

GENMO_WT - W - 8 bits - VGA_IO:0x3C2			
Field Name	**Bits**	**Default**	**Description**

GENMO_MONO_ADDRESS_B	0	0x0	VGA addressing mode.
			   0=Monochrome emulation, regs at 0x3Bx
			   1=Color/Graphic emulation, regs at 0x3Dx

VGA_RAM_EN	1	0x0	Enables/Disables CPU access to video RAM at VGA aperture.
			   0=Disable
			   1=Enable

VGA_CKSEL	3:2	0x0	Selects pixel clock frequency to use in VGA modes. Used when CRTC_GEN_CNTL.CRTC_EXT_DISP_EN = 0. See CLOCK_CNTL_INDEX.PPLL_DIV_SEL for non-VGA mode pixel clock selection.
			   0=25.1744MHz (640 Pels)
			   1=28.3212MHz (720 Pels)
			   2=Reserved
			   3=Reserved

ODD_EVEN_MD_PGSEL	5	0x0	This bit is used in odd/even display modes (A/N modes: 0, 1, 2, 3, and 7). This bit is ignored when either bit GRA06[1] or SEQ4[3] are enabled.
			Used to determine if the VGA aperture maps into the lower (even) or upper (odd) page of memory.
			   0=Selects odd (high) memory locations
			   1=Selects even (low) memory locations

VGA_HSYNC_POL	6	0x0	Determines polarity of horizontal sync (HSYNC) for VGA modes.
			  0=HSYNC pulse active high
			  1=HSYNC pulse active low
			The convention of VGA is to use active low VSYNC for 400 (and 200) and 480 line modes. Active high is normally used for 350 line modes.

VGA_VSYNC_POL	7	0x0	Determines polarity of vertical sync (VSYNC) for VGA modes.
			  0=VSYNC pulse active high
			  1=VSYNC pulse active low
			The convention of VGA is to use active high VSYNC for 400 (and 200) line modes. Active low is normally used for 350 and 480 line modes.

Miscellaneous Output register (Write).			

GENMO_RD - R - 8 bits - VGA_IO:0x3CC			
Field Name	**Bits**	**Default**	**Description**
GENMO_MONO_ADDRESS_B *(mirror of GENMO_WT:GENMO_MONO_ADDRESS_B)*	0	0x0	VGA addressing mode.
VGA_RAM_EN *(mirror of GENMO_WT:VGA_RAM_EN)*	1	0x0	Enables/Disables CPU access to video RAM at VGA aperture.
VGA_CKSEL *(mirror of GENMO_WT:VGA_CKSEL)*	3:2	0x0	Selects pixel clock frequency to use.
ODD_EVEN_MD_PGSEL *(mirror of GENMO_WT:ODD_EVEN_MD_PGSEL)*	5	0x0	This bit is used in odd/even display modes (A/N modes: 0, 1, 2, 3, and 7). This bit is ignored when either bit GRA06[1] or SEQ4[3] are enabled. Used to determine if the VGA aperture maps into the lower (even) or upper (odd) page of memory.

VGA_HSYNC_POL
 	
(mirror of GENMO_WT:VGA_HSYNC_POL)
	6	0x0	Determines polarity of horizontal sync (HSYNC) for VGA modes.
			  0=HSYNC pulse active high
			  1=HSYNC pulse active low
			The convention of VGA is to use active low VSYNC for 400 (and 200) and 480 line modes. Active high is normally used for 350 line modes.

VGA_VSYNC_POL
 	
(mirror of GENMO_WT:VGA_VSYNC_POL)
	7	0x0	Determines polarity of vertical sync (VSYNC) for VGA modes.
			  0=VSYNC pulse active high
			  1=VSYNC pulse active low
			The convention of VGA is to use active high VSYNC for 400 (and 200) line modes. Active low is normally used for 350 and 480 line modes.

Miscellaneous Output register (Read).			

DAC_CNTL - RW - 32 bits - [IOReg,MMReg:0x58]			
Field Name	**Bits**	**Default**	**Description**
DAC_VGA_ADR_EN	13	0x0	Enables access of the palette (DAC) at the VGA I/O DAC addresses when in extended display modes (non-VGA, or CRTC_EXT_DISP_EN=1).
General control for the RGB DAC and palette.			

GENS0 - R - 8 bits - VGA_IO:0x3C2			
Field Name	**Bits**	**Default**	**Description**
SENSE_SWITCH	4	0x0	DAC comparator read back. Used for monitor detection. Mirror of DAC_CMP_OUTPUT@DAC_CNTL. See description there.
CRT_INTR	7	0x0	CRT Interrupt: 0=Vertical retrace interrupt is cleared 1=Vertical retrace interrupt is pending
Input Status 0 register.			

GENS1 - R - 8 bits - [VGA_IO:0x3BA] [VGA_IO:0x3DA]			
Field Name	**Bits**	**Default**	**Description**
NO_DIPLAY	0	0x0	Display enable. 0=Enable 1=Disable
VGA_VSTATUS	3	0x0	Vertical Retrace Status. 0=Vertical retrace not active 1=Vertical retrace active
PIXEL_READ_BACK	5:4	0x0	Diagnostic bits 0, 1 respectively. These two bits are connected to two of the eight colour outputs (P7:P0) of the attribute controller. Connections are controlled by ATTR12(5,4) as follows: 0=P2,P0 1=P5,P4 2=P3,P1 3=P7,P6
Input Status 1 register.			

2.13 VGA Sequencer

SEQ00 - RW - 8 bits - VGASEQIND:0x0			
Field Name	**Bits**	**Default**	**Description**

SEQ_RST0B	0	0x1	Synchronous reset bit 0:
			  0=Follows SEQ_RST1B
			  1=Sequencer runs unless SEQ_RST1B=0

SEQ_RST1B	1	0x1	Synchronous reset bit 1:
			  0=Disable character clock, display requests, and H/V syncs
			  1=Sequencer runs unless SEQ_RST0B=0

Reset register.			

SEQ01 - RW - 8 bits - VGASEQIND:0x1			
Field Name	**Bits**	**Default**	**Description**

SEQ_DOT8	0	0x1	8/9 Dot Clocks (Modes 1, 2, 3, and 7 use 9-dot characters. To change bit 0, GENVS(0) must be logical 0).
			  0=9 dot char clock. Modes 0, 1, 2, 3 & 7
			  1=8 dot char clock.

SEQ_SHIFT2	2	0x0	Shift load bits.
			  0=Load video serializer every clock, if SEQ_SHIFT4=0
			  1=Load video serializer every other clock, if SEQ_SHIFT4 = 0

SEQ_PCLKBY2	3	0x0	Dot Clock (typically, 320 and 360 horizontal modes use divide-by-2 to provide 40 column displays. To change this bit SEQ00[0:0] must be first set to zero).
			  0=Dot clock is normal
			  1=Dot clock is divided by 2

SEQ_SHIFT4	4	0x0	Shift load bits.
			  0 = SEQ_SHIFT2 determines serializer loading
			  1 = Load video serializer every fourth clock. Ignore SEQ_SHIFT2

SEQ_MAXBW	5	0x1	Screen off:
			  0=Normal. Screen on
			  1=Screen off and blanked. CPU has uninterrupted access to frame buffer

Clock Mode register.			

SEQ02 - RW - 8 bits - VGASEQIND:0x2			
Field Name	**Bits**	**Default**	**Description**

SEQ_MAP0_EN	0	0x0	Enables map 0
			  0=Disable write to memory map 0
			  1=Enable write to memory map 0

SEQ_MAP1_EN	1	0x0	Enables map 1
			  0=Disable write to memory map 1
			  1=Enable write to memory map 1

	Bits	Default	Description
SEQ_MAP2_EN	2	0x0	Enables map 2 　0=Disable write to memory map 2 　1=Enable write to memory map 2
SEQ_MAP3_EN	3	0x0	Enables map 3 　0=Disable write to memory map 3 　1=Enable write to memory map 3
Map Mask register.			

SEQ03 - RW - 8 bits - VGASEQIND:0x3			
Field Name	Bits	Default	Description
SEQ_FONT_B1	0	0x0	Character Map Select B Bit 1
SEQ_FONT_B2	1	0x0	Character Map Select B Bit 2
SEQ_FONT_A1	2	0x0	Character Map Select A Bit 1
SEQ_FONT_A2	3	0x0	Character Map Select A Bit 2
SEQ_FONT_B0	4	0x0	Character Map Select B Bit 0
SEQ_FONT_A0	5	0x0	Character Map Select A Bit 0
Character Map Select register.			

SEQ04 - RW - 8 bits - VGASEQIND:0x4			
Field Name	Bits	Default	Description
SEQ_256K	1	0x0	Extended memory. 1 indicates 256 KB of video memory is present. It also enables the character map selection in SEQ03. 　0=64KB memory present. Has no effect since 256KB always available 　1=256KB memory present
SEQ_ODDEVEN	2	0x0	Odd/Even 　0=Even CPU address (A0=0) accesses maps 0 and 2. Odd address accesses maps 1 and 3 　1=Enables sequential access to maps for odd/even modes. SEQ02 (Map Mask) selects which maps are used
SEQ_CHAIN	3	0x0	Chain (when logical 1, it takes priority over off/even mode bits SEQ04[2] and GRA05[4]. Unlike odd/even mode, SEQ04[2] is the only bit used to enable chain mode (double odd/even). Chain does not affect CRTC access to video memory. Odd/even bit SEQ04[2] should be the opposite of GRA05[4]. 　0=Enables sequential access to maps. SEQ02 (Map Mask) selects which maps are used 　1=For 256 color modes. Map select by CPU address bits A1:A0
Memory Mode register.			

SEQ8_IDX - RW - 8 bits - [MMReg,VGA_IO:0x3C4]			
Field Name	**Bits**	**Default**	**Description**
SEQ_IDX	2:0	0x0	This index points to one of the sequencer registers (SEQ_) at I/O port address 0x3C5, for the next SEQ read/write operation.
SEQ Index Register			

SEQ8_DATA - RW - 8 bits - [MMReg,VGA_IO:0x3C5]			
Field Name	**Bits**	**Default**	**Description**
SEQ_DATA	7:0	0x0	SEQ data indirect access.
SEQ Data Register			

2.14 VGA CRT

CRTC8_IDX - RW - 8 bits - [MMReg:0x3B4] [MMReg:0x3D4] [VGA_IO:0x3B4] [VGA_IO:0x3D4]			
Field Name	**Bits**	**Default**	**Description**
VCRTC_IDX *(mirror bits 0:5 of CRTC_EXT_CNTL:VCRTC_IDX_MASTER)*	5:0	0x0	This index points to one of the internal registers of the CRT controller (CRTC) at address 0x3?5, for the next CRTC read/write operation.
CRT Index Register			

CRTC8_DATA - RW - 8 bits - [MMReg:0x3B5] [MMReg:0x3D5] [VGA_IO:0x3B5] [VGA_IO:0x3D5]			
Field Name	**Bits**	**Default**	**Description**
VCRTC_DATA	7:0	0x0	CRTC data indirect access
CTRC Data Register			

CRT00 - RW - 8 bits - VGACRTIND:0x0			
Field Name	**Bits**	**Default**	**Description**
H_TOTAL	7:0	0x0	These bits define the active horizontal display in a scan line, including the retrace period. The value is five less than the total number of displayed characters in a scan line.
Horizontal Total register.			

CRT01 - RW - 8 bits - VGACRTIND:0x1			
Field Name	**Bits**	**Default**	**Description**
H_DISP_END	7:0	0x0	These bits define the active horizontal display in a scan line. The value is one less than the total number of displayed characters in a scan line.
Horizontal Display Enable End register.			

CRT02 - RW - 8 bits - VGACRTIND:0x2			
Field Name	**Bits**	**Default**	**Description**
H_BLANK_START	7:0	0x0	These bits define the horizontal character count that represents the character count in the active display area, plus the right border. In other words, the count is from the start of active display to the start of triggering of the H blanking pulse.
Start Horizontal Blanking register.			

CRT03 - RW - 8 bits - VGACRTIND:0x3			
Field Name	**Bits**	**Default**	**Description**
H_BLANK_END	4:0	0x0	H blanking bits 4-0 respectively. These are the five low-order bits (of six bits in total) of horizontal character count for triggering the end of the horizontal blanking pulse.
H_DE_SKEW	6:5	0x0	Display-enable skew: 　0=0Skew 　1=1Skew 　2=2Skew 　3=3Skew
CR10CR11_R_DIS_B	7	0x0	Compatibility Read: 　0=WrtOnlyToCRT10-11 　1=WrtRdToCRT10-11
End Horizontal Blanking register.			

CRT04 - RW - 8 bits - VGACRTIND:0x4			
Field Name	**Bits**	**Default**	**Description**
H_SYNC_START	7:0	0x0	These bits define the horizontal character count at which the horizontal retrace pulse becomes active.
Start Horizontal Retrace register.			

CRT05 - RW - 8 bits - VGACRTIND:0x5			
Field Name	**Bits**	**Default**	**Description**
H_SYNC_END	4:0	0x0	H Retrace Bits (these are the 5-bit result from the sum of CRT0 plus the width of the horizontal retrace pulse, in character clock units).
H_SYNC_SKEW	6:5	0x0	H Retrace Delay bits (these two bits skew the horizontal retrace pulse).
H_BLANK_END_B5	7	0x0	H blocking end bit 5 (this is the bit of the 6-bit character count for the H blanking end pulse). The other five low-order bits are CRT03[4:0].
End Horizontal Retrace register.			

CRT06 - RW - 8 bits - VGACRTIND:0x6			
Field Name	**Bits**	**Default**	**Description**
V_TOTAL	7:0	0x0	These are the eight low-order bits of the 10-bit vertical total register. The 2 high-order bits are CRT07[5:0] in the CRTC overflow register. The value of this register represents the total number of H raster scans plus vertical retrace (active display, blanking), minus two scan lines.
Vertical Total register.			

CRT07 - RW - 8 bits - VGACRTIND:0x7			
Field Name	**Bits**	**Default**	**Description**
V_TOTAL_B8	0	0x0	V Total Bit 8 (CRT06). Bit 8 of 10 bit vertical count for V Total. For functional description see CRT06 register.
V_DISP_END_B8	1	0x0	End V Display Bit 8 (CRT12). Bit 8 of 10-bit vertical count for V Display enable. For functional description see CRT12 register.
V_SYNC_START_B8	2	0x0	Start V Retrace Bit 8 (CRT10). Bit 8 of 10-bit vertical count for V Retrace start. For functional description see CRT10 register.
V_BLANK_START_B8	3	0x0	Start V Blanking Bit 8 (CRT15). Bit 8 of the 10-bit vertical count for V Blanking start. For functional description see CRT15 register.
LINE_CMP_B8	4	0x0	Line compare bit 8 (CRT18). Bit 8 of the 10-bit vertical count for line compare. For functional description see CRT18 register.
V_TOTAL_B9	5	0x0	V Total Bit 9 (CRT06). Bit 9 of 10-bit vertical count for V Total. For functional description see CRT06 register.
V_DISP_END_B9	6	0x0	End V Display Bit 9 (CRT12). Bit 9 of 10-bit vertical count for V Display enable end (for functional description see CRT12 register).
V_SYNC_START_B9	7	0x0	Start V Retrace Bit (CRT10). Bit 9 of 10-bit vertical count for V Retrace start. For functional description see CRT10 register.
CRTC Overflow register.			

CRT08 - RW - 8 bits - VGACRTIND:0x8			
Field Name	**Bits**	**Default**	**Description**
ROW_SCAN_START	4:0	0x0	Preset row scan bit 4:0. This register is used for software-controlled vertical scrolling in text or graphics modes. The value specifies the first line to be scanned after a V retrace (in the next frame). Each H Retrace pulse increments the counter by 1, up to the maximum scan line value programmed by CRT09, then the counter is cleared.
BYTE_PAN	6:5	0x0	Byte panning control bits 1 and 0 (respectively). Bits 6 and 5 extend the capability of byte panning (shifting) by up to three characters (for description H_PEL Panning register ATTR13).
Preset Row Scan register.			

CRT09 - RW - 8 bits - VGACRTIND:0x9			
Field Name	**Bits**	**Default**	**Description**
MAX_ROW_SCAN	4:0	0x0	Maximum scan line bits. These bits define a value that is the actual number of scan line per character minus 1.
V_BLANK_START_B9	5	0x0	Start V Blanking bit 9 (CRT15). Bit 9 of 10-bit vertical count for line compare. For functional description see CRT18 register.
LINE_CMP_B9	6	0x0	Line Compare Bit 9 (CRT18). Bit 9 of 10-bit vertical count for line compare. For functional description see CRT18 register.

DOUBLE_CHAR_HEIGHT	7	0x0	200/400 line scan. Note: H/V display and blanking timings etc. (in CRT00-CRT06 registers) are not affected.
			  0=200LineScan
			  1=400LineScan

Maximum Scan Line register.			

CRT0A - RW - 8 bits - VGACRTIND:0xA			
Field Name	**Bits**	**Default**	**Description**
CURSOR_START	4:0	0x0	Cursor start bits [4:0] (respectively). These bits define a value that is the starting scan line (on a character row) for the line cursor. The 5-bit value is equal to the actual number minus one. This value is used together with the Cursor End Bits CRT0B[4:0] to determine the height of the cursor. The cursor height in VGA does not wrap around (as in EGA) and is actually absent when the 'end' value is less than the 'start' value. In EGA when the 'end' value is less, the cursor is a full block cursor the same height as the character cell.

CURSOR_DISABLE	5	0x0	Cursor on/off.
			  0=On
			  1=Off

Cursor Start register.			

CRT0B - RW - 8 bits - VGACRTIND:0xB			
Field Name	**Bits**	**Default**	**Description**
CURSOR_END	4:0	0x0	Cursor end bits [4:0] (respectively). These bits define the ending scan row (on a character line) for the line cursor. In EGA, this 5-bit value is equal to the actual number of lines plus one. The cursor height in VGA does not wrap around (as in EGA) and is actually absent when the 'end' value is less than the 'start' value. In EGA when the 'end' value is less, the cursor is a full block cursor the same height as the character cell.
CURSOR_SKEW	6:5	0x0	Cursor skew bits [1:0] (respectively). These bits define the number of characters the cursor is to be shifted to the right (skewed) from the character pointed at by the cursor location (registers CRT0E and CRT0F), in VGA mode. Skew values, when in EGA mode, are enclosed in brackets.
Cursor End register.			

CRT0C - RW - 8 bits - VGACRTIND:0xC			
Field Name	**Bits**	**Default**	**Description**
DISP_START	7:0	0x0	SA bits [15:8]. These are the eight high-order bits of the 16-bit display buffer start location. The low order bits are contained in CRT0D. In split screen mode, CRT0C = CRT0D point to the starting location of screen A (top half) . The starting address for screen B is always zero.
Start Address (High Byte) register.			

CRT0D - RW - 8 bits - VGACRTIND:0xD			
Field Name	**Bits**	**Default**	**Description**
DISP_START	7:0	0x0	SA bits [7:0]. These are the eight low-order bits of the 16-bit display buffer start location. The high-order bits are contained in CRT0C. In split screen mode, CRT0C + CRT0D points to the starting location of screen A (top half.) The starting address for screen B is always zero.
Start Address (Low Byte) register.			

CRT0E - RW - 8 bits - VGACRTIND:0xE			
Field Name	**Bits**	**Default**	**Description**
CURSOR_LOC_HI	7:0	0x0	CA bits [15:8]. These are the eight high-order bits of the 16 bit cursor start address. The low-order CA bits are contained in CRT0F. This address is relative to the start of the physical display memory address pointed to by CRT0C + CRT0D. In other words, if CRT0C + CRT0D is changed, the cursor still points to the same character as before.
Cursor Location (High Byte) register.			

CRT0F - RW - 8 bits - VGACRTIND:0xF			
Field Name	**Bits**	**Default**	**Description**
CURSOR_LOC_LO	7:0	0x0	CA bits [7:0]. These are the eight low-order bits of the 16-bit cursor start address. The high-order CA bits are contained in CRT0E. This address is relative to the start of the physical display memory address pointed to by CRT0C + CRT0D. In other words, if CRT0C + T0D is changed, the cursor still points to the same character as before.
Cursor Location (Low Byte) register.			

CRT10 - RW - 8 bits - VGACRTIND:0x10			
Field Name	**Bits**	**Default**	**Description**
V_SYNC_START	7:0	0x0	Bits CRT10[7:0] are the eight low-order bits of the 10-bit vertical retrace start count. The two high-order bits are CRTt07[2:7], located in the CRTC overflow register. These bits define the horizontal scan count that triggers the V retrace pulse.
Start Vertical Retrace register.			

CRT11 - RW - 8 bits - VGACRTIND:0x11			
Field Name	**Bits**	**Default**	**Description**
V_SYNC_END	3:0	0x0	V Retrace End Bits [3:0]. Bits CRT11[0:3] define the horizontal scan count that triggers the end of the V Retrace pulse.
V_INTR_CLR	4	0x0	V Retrace Interrupt Set: 　0=VRetraceIntCleared 　1=Not Cleared
V_INTR_EN	5	0x0	V Retrace Interrupt Disabled: 　0=VRetraceIntEna 　1=Disable
SEL5_REFRESH_CYC	6	0x0	0=3 DRAM Refresh/Horz Line 1=5 DRAM Refresh/Horz Line
C0T7_WR_ONLY	7	0x0	Write Protect (CRT00-CRT06). All register bits, except CRTO7[4], are write protected. 　0=EnaWrtToCRT00-07 　1=C0T7B4WrtOnly
End Vertical Retrace register.			

CRT12 - RW - 8 bits - VGACRTIND:0x12			
Field Name	**Bits**	**Default**	**Description**
V_DISP_END	7:0	0x0	These are the eight low-order bits of the 10-bit register containing the horizontal scan count indicating where the active display on the screen should end. The high-order bits are CRT07 [1:6] in the CRT overflow register.
Vertical Display Enable End register.			

CRT13 - RW - 8 bits - VGACRTIND:0x13			
Field Name	**Bits**	**Default**	**Description**
DISP_PITCH	7:0	0x0	These bits define an offset value, equal to the logical line width of the screen (from the first character of the current line to the first character of the next line). Memory organization is dependent on the video mode. Bit CRT17[6] selects either byte or word mode. Bit CRT14[6], which overrides the byte/word mode setting, selects double-word mode when it is logical one. The first character of the next line is specified by the start address (CRT0C + CRT0D), plus the offset. The offset for byte mode is 2x CRT13, for word mode it is 4x, and for double word mode it is 8x.
Offset register.			

CRT14 - RW - 8 bits - VGACRTIND:0x14			
Field Name	**Bits**	**Default**	**Description**
UNDRLN_LOC	4:0	0x0	H Row Scan Bits [4:0]. These bits define the horizontal scan row, from the top of the characterline, that should be used for underlining. The 5-bit value is equal to the actual number, minus one.

ADDR_CNT_BY4	5	0x0	Count-by-4:
			  0=Char. Clock
			  1=CountBy4

DOUBLE_WORD	6	0x0	Double-Word Mode:
			  0=Disable
			  1=DoubleWordMdEna

Underline Location register.			

CRT15 - RW - 8 bits - VGACRTIND:0x15			
Field Name	**Bits**	**Default**	**Description**
V_BLANK_START	7:0	0x0	These are the eight low-order bits of the 10-bit vertical blanking start register. Bit [9] is CRT09[5]; and bit [8] is CRT07[3]. The 10 bits specify the starting location of the vertical blanking pulse, in units of horizontal scan lines. The value is equal to the actual number of displayed lines, minus one.
Start Vertical Blanking register.			

CRT16 - RW - 8 bits - VGACRTIND:0x16			
Field Name	**Bits**	**Default**	**Description**
V_BLANK_END	7:0	0x0	These bits define the point at which the end of the vertical blanking pulse needs to be triggered. The location is specified in units of horizontal scan lines. The value to be stored in this register is the seven low-order bits of the sum of 'pulse width count' plus the content of Start Vertical Blanking register (CRT15), minus one.
End Vertical Blanking register.			

CRT17 - RW - 8 bits - VGACRTIND:0x17			
Field Name	**Bits**	**Default**	**Description**
RA0_AS_A13B	0	0x0	Compatibility Mode.
RA1_AS_A14B	1	0x0	Select Row Scan Counter.
VCOUNT_BY2	2	0x0	Vertical_by_2. Note: When bit [2] is logical one, other vertical register values should be adjusted as well (CRT06, CRT10, CRT12, CRT15, and CRT18).
ADDR_CNT_BY2	3	0x0	Count_by_2. Note: This bit can be written to, and read from, but it has no effect.
WRAP_A15TOA0	5	0x0	Address Wrap. Note: This bit can be written to, and read from, but it has no effect.
BYTE_MODE	6	0x0	Byte/Word Mode. 0=WordMode 1=ByteMode
CRTC_SYNC_EN	7	0x0	H/V Retrace Enable. 0=Disable HVSync 1=EnaHVSync
CRT Mode register.			

CRT18 - RW - 8 bits - VGACRTIND:0x18			
Field Name	**Bits**	**Default**	**Description**
LINE_CMP	7:0	0x0	These bits are the eight low-order of the 10-bit line compare register. Bit [8] is CRT07[4], bit [9] is CRT09[6]. The value of this register is used to disable scrolling on a portion of the display screen, as when the split screen is active. When the vertical counter reaches this value, the memory address and row scan counters are cleared. The screen area above the line specified by the register is commonly called screen A. The screen below is screen B. Screen B cannot be scrolled, but it can be panned only together with screen A, controlled by the PEL panning compatibility bit ATTR10[5]. (For a description of this control bit see ATTR10[5].)
Line Compare register.			

CRT1E - R - 8 bits - VGACRTIND:0x1E			
Field Name	**Bits**	**Default**	**Description**
GRPH_DEC_RD1	1	0x0	This register is used to read back the graphics controller index decode.
Graphics Controller Index Decode register.			

CRT1F - R - 8 bits - VGACRTIND:0x1F			
Field Name	**Bits**	**Default**	**Description**
GRPH_DEC_RD0	7:0	0x0	This register is used to read back the graphics controller index decode.
Graphics Controller Index Decode register.			

CRT22 - R - 8 bits - VGACRTIND:0x22			
Field Name	**Bits**	**Default**	**Description**
GRPH_LATCH_DATA	7:0	0x0	This register is used to read the data in the Graphics Controller CPU data latches. The Graphics Controller Read Map Select register bits 0 and 1 determine which byte is read back.
RAM Data Latch Readback register.			

2.15 VGA Graphics

GRPH8_IDX - RW - 8 bits - [MMReg,VGA_IO:0x3CE]			
Field Name	**Bits**	**Default**	**Description**
GRPH_IDX	3:0	0x0	

GRPH8_DATA - RW - 8 bits - [MMReg,VGA_IO:0x3CF]			
Field Name	**Bits**	**Default**	**Description**
GRPH_DATA	7:0	0x0	GRPH data indirect access
GRPH Data Register			

GRA00 - RW - 8 bits - VGAGRPHIND:0x0			
Field Name	**Bits**	**Default**	**Description**
GRPH_SET_RESET0	0	0x0	Set/Reset Map 0.
GRPH_SET_RESET1	1	0x0	Set/Reset Map 1.
GRPH_SET_RESET2	2	0x0	Set/Reset Map 2.
GRPH_SET_RESET3	3	0x0	Set/Reset Map 3.
Set/Reset register.			

GRA01 - RW - 8 bits - VGAGRPHIND:0x1			
Field Name	**Bits**	**Default**	**Description**
GRPH_SET_RESET_ENA0	0	0x0	Enables Set/Reset Map 0.
GRPH_SET_RESET_ENA1	1	0x0	Enables Set/Reset Map 1.
GRPH_SET_RESET_ENA2	2	0x0	Enables Set/Reset Map 2.
GRPH_SET_RESET_ENA3	3	0x0	Enables Set/Reset Map 3.
Enable Set/Reset register.			

GRA02 - RW - 8 bits - VGAGRPHIND:0x2			
Field Name	**Bits**	**Default**	**Description**
GRPH_CCOMP	3:0	0x0	Colour Compare Map bits [3:0]. In Read mode (GRA05[3] being logical 1), the 4 bits from this register are compared with the 4-bit PEL value (made up of one bit from each map), from bit positions 0 through 7. As long as the colour don't care bits (GRA07[0:3]) for the respective maps are logical 1's, the compare takes place only on those bits of the PEL value, and the CPU reads a one for a match in that bit position. If the Colour Don't Care bit for one map is a logical zero, the latched data from the map is excluded from the compare, and only the remaining three bits are compared to generate bus data.
Colour Compare register.			

GRA03 - RW - 8 bits - VGAGRPHIND:0x3			
Field Name	**Bits**	**Default**	**Description**
GRPH_ROTATE	2:0	0x0	Rotate Count Bits [2:0]. Specifies the number of bit positions that the CPU data is to be rotated to the right, before doing the function selected by bits 3 and 4 above and subsequency bit mask select and write operations. Rotation is carried out only in write modes 0 and 3. In these two modes, the CPU data is rotated first, the operated only the function bits GRA03[4:3], the updated by the bit mask register GRA05.
GRPH_FN_SEL	4:3	0x0	Function Select Bits 1 and 2. These functions are performed on the CPU data before the selected bits are updated by the bit mask register, and then written to the display buffers. 　0=Replace 　1=AND 　2=OR 　3=XOR
Data Rotate register.			

GRA04 - RW - 8 bits - VGAGRPHIND:0x4			
Field Name	**Bits**	**Default**	**Description**
GRPH_RMAP	1:0	0x0	Read Mode 0 Only. The GRA controller returns the contents of one of the four latched buffer bytes to the CPU each time a CPU read loads these latches. The 2 bits (0 and 1) define a value that represents the bit map where the CPU is to read data. This is useful in transferring bit map data between the maps and the system RAM.
Read Map Select register.			

GRA05 - RW - 8 bits - VGAGRPHIND:0x5			
Field Name	**Bits**	**Default**	**Description**

GRPH_WRITE_MODE	1:0	0x0	Write Mode:
			  0=Write mode 0
			  1=Write mode 1
			  2=Write mode 2
			  3=Write mode 3

GRPH_READ1	3	0x0	Read Mode:
			  0=Read mode 0, byte oriented
			  1=Read mode 1, pixel oriented

CGA_ODDEVEN	4	0x0	Odd/Even Addressing Enable. Used to enable CGA emulation, this bit enables off/even addressing mode when it is a logical one. Normally, this bit and memory mode bit SEQ04[2] are set to agree with each other in enabling odd/even mode emulation.
			  0=Disable Odd/Even Addressing
			  1=Enable Odd/Even Addressing

GRPH_OES	5	0x0	Shift Register Mode. This bit controls how data from memory is loaded into the shift registers M0D0:M0D7, M1D0:M1D7; M2D0:M2D7, and M3D0:M3D7 are representations of this data.
			  0=Linear shift mode
			  1=Tiled shift mode

GRPH_PACK	6	0x0	256 Colour Mode. This bit also controls how data from memory is loaded into the shift registers.
			  0=Use shift register mode as per GRPH_OES
			  1=256 color mode, read as packed pixels, ignore GRPH_OES

Graphics Mode register.			

GRA06 - RW - 8 bits - VGAGRPHIND:0x6			
Field Name	**Bits**	**Default**	**Description**

GRPH_GRAPHICS	0	0x0	Graphics/Alphanumeric Mode
			  0=Alpha Numeric Mode
			  1=Graphics Mode

GRPH_ODDEVEN	1	0x0	Chains Odd Maps to Even
			  0=Normal
			  1=Chain Odd maps to Even

GRPH_ADRSEL	3:2	0x0	Memory Map Read Bits 1 and 0, respectively.
			  0=A0000-128K
			  1=A0000-64K
			  2=B0000-32K
			  3=B8000-32K

Graphics Miscellaneous register.			

GRA07 - RW - 8 bits - VGAGRPHIND:0x7			
Field Name	**Bits**	**Default**	**Description**

GRPH_XCARE0	0	0x0	Ignore Map 0
			  0=Ignore map 0
			  1=Use map 0 for read mode 1

GRPH_XCARE1	1	0x0	Ignore Map 1
			  0=Ignore map 1
			  1=Use map 1 for read mode 1

GRPH_XCARE2	2	0x0	Ignore Map 2
			  0=Ignore map 2
			  1=Use map 2 for read mode 1

GRPH_XCARE3	3	0x0	Ignore Map 3
			  0=Ignore map 3
			  1=Use map 3 for read mode 1

Colour Don't Care register.			

GRA08 - RW - 8 bits - VGAGRPHIND:0x8			
Field Name	**Bits**	**Default**	**Description**
GRPH_BMSK	7:0	0x0	Bit Mask.
Bit Mask register.			

2.16 VGA Attribute

ATTRX - RW - 8 bits - VGA_IO:0x3C0			
Field Name	**Bits**	**Default**	**Description**
ATTR_IDX	4:0	0x0	ATTR Index. This index points to one of the internal registers of the attribute controller (ATTR) at addresses 0x3C1/0x3C0, for the next ATTR read/write operation. Since both the index and data registers are at the same I/O, a pointer to the registers is necessary. This pointer can be initialized to point to the index register by a read of GENS1.
ATTR_PAL_RW_ENB	5	0x0	Palette Address Source. After loading the colour palette, this bit should be set to logical 1. 0=Processor to load 1=Memory data to access
Attribute Index register.			

ATTRDW - W - 8 bits - VGA_IO:0x3C0			
Field Name	**Bits**	**Default**	**Description**
ATTR_DATA	7:0	0x0	Attribute Data Write.
Attribute Data Write register.			

ATTRDR - R - 8 bits - VGA_IO:0x3C1			
Field Name	**Bits**	**Default**	**Description**
ATTR_DATA	7:0	0x0	Attribute Data Read.
Attribute Data Read register.			

ATTR00 - RW - 8 bits - VGAATTRIND:0x0			
Field Name	**Bits**	**Default**	**Description**
ATTR_PAL	5:0	0x0	Colour Bits [5:0] map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0, and is enabled for those bits set to logical 1.
Palette register 0.			

ATTR01 - RW - 8 bits - VGAATTRIND:0x1			
Field Name	**Bits**	**Default**	**Description**
ATTR_PAL	5:0	0x0	Colour Bits [5:0] map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0, and is enabled for those bits set to logical 1.
Palette register 1.			

ATTR02 - RW - 8 bits - VGAATTRIND:0x2			
Field Name	**Bits**	**Default**	**Description**
ATTR_PAL	5:0	0x0	Colour Bits [5:0] map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0, and is enabled for those bits set to logical 1.
Palette register 2.			

ATTR03 - RW - 8 bits - VGAATTRIND:0x3			
Field Name	**Bits**	**Default**	**Description**
ATTR_PAL	5:0	0x0	Colour Bits [5:0] map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0, and is enabled for those bits set to logical 1.
Palette register 3.			

ATTR04 - RW - 8 bits - VGAATTRIND:0x4			
Field Name	**Bits**	**Default**	**Description**
ATTR_PAL	5:0	0x0	Colour Bits [5:0] map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0, and is enabled for those bits set to logical 1.
Palette register 4.			

ATTR05 - RW - 8 bits - VGAATTRIND:0x5			
Field Name	**Bits**	**Default**	**Description**
ATTR_PAL	5:0	0x0	Colour Bits [5:0] map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0, and is enabled for those bits set to logical 1.
Palette register 5.			

ATTR06 - RW - 8 bits - VGAATTRIND:0x6			
Field Name	**Bits**	**Default**	**Description**
ATTR_PAL	5:0	0x0	Colour Bits [5:0] map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0, and is enabled for those bits set to logical 1.
Palette register 6.			

ATTR07 - RW - 8 bits - VGAATTRIND:0x7			
Field Name	**Bits**	**Default**	**Description**
ATTR_PAL	5:0	0x0	Colour Bits [5:0] map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0, and is enabled for those bits set to logical 1.
Palette register 7.			

ATTR08 - RW - 8 bits - VGAATTRIND:0x8			
Field Name	**Bits**	**Default**	**Description**
ATTR_PAL	5:0	0x0	Colour Bits [5:0] map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0, and is enabled for those bits set to logical 1.
Palette register 8.			

ATTR09 - RW - 8 bits - VGAATTRIND:0x9			
Field Name	**Bits**	**Default**	**Description**
ATTR_PAL	5:0	0x0	Colour Bits [5:0] map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0, and is enabled for those bits set to logical 1.
Palette register 9.			

ATTR0A - RW - 8 bits - VGAATTRIND:0xA			
Field Name	**Bits**	**Default**	**Description**
ATTR_PAL	5:0	0x0	Colour Bits [5:0] map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0, and is enabled for those bits set to logical 1.
Palette register Ah (10).			

ATTR0B - RW - 8 bits - VGAATTRIND:0xB			
Field Name	**Bits**	**Default**	**Description**
ATTR_PAL	5:0	0x0	Colour Bits [5:0] map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0, and is enabled for those bits set to logical 1.
Palette register Bh (11).			

ATTR0C - RW - 8 bits - VGAATTRIND:0xC			
Field Name	**Bits**	**Default**	**Description**
ATTR_PAL	5:0	0x0	Colour Bits [5:0] map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0, and is enabled for those bits set to logical 1.
Palette register Ch (12).			

ATTR0D - RW - 8 bits - VGAATTRIND:0xD			
Field Name	**Bits**	**Default**	**Description**
ATTR_PAL	5:0	0x0	Colour Bits [5:0] map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0, and is enabled for those bits set to logical 1.
Palette register Dh (13).			

ATTR0E - RW - 8 bits - VGAATTRIND:0xE			
Field Name	**Bits**	**Default**	**Description**
ATTR_PAL	5:0	0x0	Colour Bits [5:0] map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0, and is enabled for those bits set to logical 1.
Palette register Eh (14).			

ATTR0F - RW - 8 bits - VGAATTRIND:0xF			
Field Name	**Bits**	**Default**	**Description**
ATTR_PAL	5:0	0x0	Colour Bits [5:0] map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0, and is enabled for those bits set to logical 1.
Palette register Fh (15).			

ATTR10 - RW - 8 bits - VGAATTRIND:0x10			
Field Name	**Bits**	**Default**	**Description**

ATTR_GRPH_MODE	0	0x0	Graphics/Alphanumeric Mode.
			    0=Alphanumeric Mode
			    1=Graphic Mode

ATTR_MONO_EN	1	0x0	Monochrome/Colour Attributes Select:
			    0=Color Disp
			    1=MonoChrome Disp

ATTR_LGRPH_EN	2	0x0	Line Graphics Enable. Must be 0 for character fonts that do not use line graphics character codes for graphics. Zero will force the 9th dot to the background colour. One will allow the 8th bit of the line graphics characters to be stretched to the 9th dot.
			    0=Disable line graphics 8th dot stretch
			    1=Enable line graphics 8th dot stretch

ATTR_BLINK_EN	3	0x0	Blink Enable/Background Intensity:
			Selects whether bit [7] of the attribute controls intensity or blinking.
			    0=Intensity control
			    1=Blink control

ATTR_PANTOPONLY	5	0x0	PEL Panning Compatibility:
			    0=Panning both
			    1=Panning only the top half screen

ATTR_PCLKBY2	6	0x0	PEL Clock Select:
			    0=Shift register clocked every dot clock
			    1=For mode 13 (256 colour), 8 bits packed to form a pixel

ATTR_CSEL_EN	7	0x0	Alternate Colour Source:
			    0=Select ATTR00-0F bit 5:4 as P5 and P4
			    1=Select ATTR14 bit 1:0 as P5 and P4

Mode Control register.			

ATTR11 - RW - 8 bits - VGAATTRIND:0x11			
Field Name	**Bits**	**Default**	**Description**
ATTR_OVSC	7:0	0x0	Overscan Colour.
Overscan Colour register.			

ATTR12 - RW - 8 bits - VGAATTRIND:0x12			
Field Name	**Bits**	**Default**	**Description**

ATTR_MAP_EN	3:0	0x0	Enables Colour Map bits.
			    0=Disables data from respective map from being used for video output.
			    1=Enables data from respective map for use in video output.

ATTR_VSMUX	5:4	0x0	Video Status Mux bits 1:0. These are control bits for the multiplexer on colour bits P0-P7. The bit selection is also indicated at GENS1[5:4]:
			  00=P2, P0
			  01=P5, P4
			  10=P3, P1
			  11=P7, P6

Colour Map Enable register.			

ATTR13 - RW - 8 bits - VGAATTRIND:0x13			
Field Name	**Bits**	**Default**	**Description**
ATTR_PPAN	3:0	0x0	Shift Count Bits 3:0. The shift count value (0-8) indicates how many pixel positions to shift left. Shift in respective modes Count 0+,1+,2+,13 All other Value 3+,7,7+ 0 1 0 0 1 2 - 1 2 3 1 2 3 4 - 3 4 5 2 4 5 6 - 5 6 7 3 6 7 8 - 7 8 0 - -
Horizontal PEL Panning register.			

ATTR14 - RW - 8 bits - VGAATTRIND:0x14			
Field Name	**Bits**	**Default**	**Description**
ATTR_CSEL1	1:0	0x0	Colour bits P5 and P4, respectively. These are the colour output bits (instead of bits 5 and 4 of the internal palette registers ATTR00-0F) when the alternate colour source, bit ATTR10[7], is logical 1.
ATTR_CSEL2	3:2	0x0	Colour bits P7 and P6, respectively. These two bits are the two high-order bits of the 8-bit colour, used for rapid colour set switching (addressing different parts of the DAC colour lookup table). The lower order bits are in registers ATTR00-0F.
Colour Select register.			

2.17 TV Out

SD1_MAIN_CNTL - RW - 32 bits - [MMReg:0x5DFC]			
Field Name	**Bits**	**Default**	**Description**

SD1_TV_ASYNC_RST	0	0x1	This is an asynchronous reset for the SDTV1 encoder which gets retimed by TV1_CLK.
			  0=Normal operation
			  1=Hold the SDTV1 encoder at initialization state

SD1_RESYNC_ALWAYS	1	0x1	This bit determines whether the SDTV1 encoder responds to the secondary display synchronization pulse, SD1_FRAME_SYNC_PULSE. This pulse synchronizes the SDTV1 timing to the secondary display by setting the values listed in SD1_TIMING_H_COUNT_INIT, SD1_TIMING_V_F_COUNT_INIT, and SD1_TIMING_INTERNAL_INIT.
SD1_RESET_SCPHASE_TRIGGER	2	0x0	The retimed low to high transition of this bit will cause the SDTV1 sub-carrier sinusoidal to reset to zero, once, at the next SD1_FRAME_SYNC_PULSE occurrence. The tolerance of the separation of sub-carrier zero crossing and horizontal sync falling edge is +/- 40 degrees of sub-carrier. With pixel 0 marking the horiz. sync falling edge, adjustment of SD1_TIMING_H_COUNT_INIT.SD1_H_COUNT_INIT and the equivalent CRTC1_BACKEND_INIT_CNTL.CRTC1_BACKEND_INIT_X_START with the application of this trigger will change the separation. The formula is as follows: Hsync-SC separation in degrees = (modulo((SD1_H_COUNT_INIT + 2)/12)/12) * (-360) or (modulo((SD1_H_COUNT_INIT + 2)/12)/12) * (360) if modulo is less than 6. The first occurrence of SD1_FRAME_SYNC_PULSE after SD1_TV_ASYNC_RST goes low will also reset the sub-carrier sinusoidal and cause the same action.
SD1_FIELD_SYNC_TRIGGER	3	0x0	If SD1_MAIN_CNTL.SD1_FIELD_SYNC_CNTL = 1, the retimed low to high or high to low transition of this bit will cause the current SDTV1 field to repeat once. As an alternative to the hardware method, SD1_MAIN_CNTL.SD1_FIELD_SYNC_CNTL = 2 or 3, if software detects that the SDTV1 encoder is not on the same odd or even field as the incoming data, the use of the trigger will force an encoder repeat field and restore field synchronization
SD1_FIELD_SYNC_CNTL	5:4	0x0	This register controls SDTV1 encoder field manipulation for the purpose of field synchronization to upstream data in interlaced modes. Specifically the next encoded field will have the same polarity as the current one, causing an odd-odd or even-even sequence forcing a field sync.
SD1_ALT_PHASE_EN	6	0x1	This bit, when set, causes the SDTV1 encoder sub-carrier phase to alternate +/- 45 degrees between lines for the PAL operation standards.

SD1_INVERT_ALT_LINE	7	0x0	This bit determines the phase that the sub-carrier gets assigned at the first occurrence of SD1_FRAME_SYNC_PULSE after SD1_TV_ASYNC_RST goes low if SD1_SDTV0_DEBUG.SD1_SDTV0_DEBUG(16) = 0 or at every SD1_FRAME_SYNC_PULSE occurrence if SD1_SDTV0_DEBUG.SD1_SDTV0_DEBUG(16) = 1. Default of 0 is the normal setting.
SD1_MISC_REGS_LOCK	8	0x0	This bit allows software to lock out the update of the buffered version of various registers that could be changed on the fly during normal operation. This would prevent undetermined response of the controlled circuits because of otherwise asynchronous updates. The registers affected by this lock are: SD1_COL_SC_DENOMIN, SD1_COL_SC_INC, SD1_COL_SC_INC_CORR, SD1_SCM_COL_SC_DENOMIN, SD1_SCM_COL_SC_INC, SD1_SCM_COL_SC_INC_CORR, SD1_MAIN_CNTL.SD1_INVERT_ALT_LINE, SD1_LUMA_COMB_FILT_CNTL1.SD1_COMB_EN, and in register SD1_SCM_MOD_CNTL fields SD1_SCM_RST_DTO_ON_BLANK, SD1_SCM_INVERT_PHASE_EN, SD1_INVERT_SCM_3LINE, SD1_SCM_3LINE_INIT, and SD1_SCM_2LINE_EN
SD1_MISC_DOUBLEB_REGS_CNTL	10:9	0x0	Selects at which pixel in the SDTV1 frame the registers listed under SD1_MISC_REGS_LOCK will be updated to their buffered versions.
SD1_VBI_PASSTHRU_EN	11	0x0	Setting this bit high will allow the SDTV1 encoder to treat the Y data in the window as defined by registers SD1_TIMING_H_VBI_PASSTHRU, SD1_TIMING_V_VBI_PASSTHRU1, and SD1_TIMING_V_VBI_PASSTHRU2 as Vertical Blank Interval data services. Other than applying the gain as set by SD1_Y_AND_PASSTHRU_GAIN_SETTINGS.SD1_VBI_PASSTHRU_GAIN and filtering as set by SD1_TIMING_H_VBI_PASSTHRU_FILT_WINDOW, SD1_LUMA_FILT_CNTL.SD1_COMP_PASSTHRU_BLEND and SD1_SVID_PASSTHRU_BLEND, no other encoder function is applied to the data.
SD1_YPBPR_480I_EN	12	0x0	Setting this bit high will put the SDTV1 encoder into the Component 480 Interlaced operational mode. The YUV input data will be treated as YPbPr and each component will have the option of running through a simple 9 tap slew filter or passing straight through to the output, selectable by SD1_LUMA_FILT_CNTL.SD1_INSIDE_ACTIVE_SLEW_EN.
SD1_YPBPR_480P_EN	13	0x0	Setting this bit high will put the SDTV1 encoder into the Component 480 Progressive operational mode. The YUV input data will be treated as YPbPr and each component will have the option of running through a simple 5 tap slew filter or passing straight through to the output, selectable by SD1_LUMA_FILT_CNTL.SD1_INSIDE_ACTIVE_SLEW_EN.

SD1_RGB_OUTPUT_EN	14	0x0	Setting this bit high will allow the SDTV1 encoder to generate a RGB (with sync on green) version of the NTSC or PAL standard mode. The U and V data will have the color burst suppressed as well as pipeline delayed to match Y data for YUV to RGB conversion. The U and V data has the standard lowpass filtering, while the Y data filtering is controlled by SD1_LUMA_FILT_CNTL.SD1_SVIDY_OUT_BLEND. Selecting the RGB data for output to the DACs is set through register SD1_VIDOUT_MUX_CNTL.
SD1_BLANK_ON_RB_SEL	15	0x0	This controls the blank level of the Red and Blue outputs if SDTV1 is generating RGB outputs, SD1_RGB_OUTPUT_EN = 1. Only the Green output has the sync and will have the normal luma blank level as specified in SD1_LUMA_BLANK_SETUP_LEVELS.
SD1_PATTERN_GEN_EN	16	0x0	Controls the application of the internal pattern generator for the SDTV1 encoder.
SD1_PATTERN_GEN_SEL	19:17	0x0	Selects the type of test pattern for the SDTV1 encoder if SD1_PATTERN_GEN_EN = 1.
SD1_PIX_DELAY	25:20	0x2	Used to align the Luma and Chroma pipelining delays through the SDTV1 encoder. Either the Luma, Y data, or modulated Chroma, as selected by SD1_PIX_DELAY_SEL, is delayed from 0 to 16 TV1_CLK periods as indicated.
SD1_ALT_PHASE_RST_ON_SYNC	26	0x0	
SD1_PIX_DELAY_SEL	27	0x0	Used to select what will be delayed by SD1_PIX_DELAY TV1_CLK periods.
SD1_Y_1024_DATAIN_EN	29:28	0x0	Controls the manipulation of Y data at the input of the SDTV1 encoder to accommodate different data ranges. 00=Consider the input Y data range as 512, so multiply Y data by 2 01=Consider the input Y data range as 1024, so pass Y data untouched 02=Consider the input Y data range as 512 with -512 offset, so multiply Y data by 2 and add 512 03=Consider the input Y data range as 1024 with a -512 offset, so pass Y data with an addition of 512
SD1_U_1024_DATAIN_EN	30	0x0	Controls the manipulation of U data at the input of the SDTV1 encoder to accommodate different data ranges. 00=Consider the input U data range based on 512, so multiply U data by 2 01=Consider the input U data range based on 1024, so pass U data untouched
SD1_V_1024_DATAIN_EN	31	0x0	Controls the manipulation of V data at the input of the SDTV1 encoder to accommodate different data ranges. 00=Consider the input V data range based on 512, so multiply V data by 2 01=Consider the input V data range based on 1024, so pass V data untouched
This register contains a collection of various control bits for the second Standard Definition TV Encoder known as SDTV1			

SD1_TIMING_H_TOTAL - RW - 32 bits - [MMReg:0x5E04]

Field Name	Bits	Default	Description
SD1_H_TOTAL	11:0	0xd4c	Total number of pixels in each SDTV1 scan line = SD1_H_TOTAL + 1
This register specifies the number of pixels per SDTV1 encoded line			

SD1_TIMING_V_F_TOTAL - RW - 32 bits - [MMReg:0x5E08]

Field Name	Bits	Default	Description
SD1_V_TOTAL	10:0	0x270	Total number of lines in each SDTV1 frame = SD1_V_TOTAL + 1. A frame is defined as two fields for interlaced modes.
SD1_F_TOTAL	19:16	0x7	Total number of fields in each SDTV1 sequence = SD1_F_TOTAL + 1. The sequence is the number of fields required before the sub-carrier phase repeats, 4 fields in NTSC, 8 fields in PAL.
This register specifies the number of lines per frame and fields per sequence for SDTV1			

SD1_TIMING_H_COUNT - RW - 32 bits - [MMReg:0x5E0C]

Field Name	Bits	Default	Description
SD1_H_COUNT (R)	11:0	0x0	Read only field indicating the current horizontal pixel within the SDTV1 line being processed.
This register specifies the current SDTV1 horizontal TV1_CLK pixel count			

SD1_TIMING_V_F_COUNT - RW - 32 bits - [MMReg:0x5E10]

Field Name	Bits	Default	Description
SD1_V_COUNT (R)	10:0	0x0	Read only field indicating the current SDTV1 encoder line being processed.
SD1_F_COUNT (R)	19:16	0x0	Read only field indicating the current SDTV1 encoder field being processed.
This register specifies the current SDTV1 line and field counts			

SD1_TIMING_H_COUNT_INIT - RW - 32 bits - [MMReg:0x5E14]

Field Name	Bits	Default	Description
SD1_H_COUNT_INIT	11:0	0xa	Indicates the value that the horizontal pixel counter gets set to during reset, SD1_MAIN_CNTL.SD1_TV_ASYNC_RST = 1, or at frame synchronization, SD1_FRAME_SYNC_PULSE = 1.
This register specifies the initial SDTV1 horizontal pixel count			

SD1_TIMING_V_F_COUNT_INIT - RW - 32 bits - [MMReg:0x5E18]

Field Name	Bits	Default	Description
SD1_V_COUNT_INIT	10:0	0x26e	Indicates the line counter value set during reset, SD1_MAIN_CNTL.SD1_TV_ASYNC_RST = 1, or at frame synchronization, SD1_FRAME_SYNC_PULSE = 1.
SD1_F_COUNT_INIT	19:16	0x7	Indicates the field counter value set during reset, SD1_MAIN_CNTL.SD1_TV_ASYNC_RST = 1, or at frame synchronization, SD1_FRAME_SYNC_PULSE = 1.
This register specifies the initial SDTV1 line and field counts			

SD1_TIMING_INTERNAL_INIT - RW - 32 bits - [MMReg:0x5E1C]			
Field Name	**Bits**	**Default**	**Description**
SD1_H_HSYNC_INIT	0	0x1	Initial value of signal indicating the pixel position of the horizontal synchronization pulse.
SD1_V_HSYNC_INIT	1	0x1	Initial value of signal indicating the lines that contain horizontal synchronization pulses.
SD1_H_EQ_PULSE_INIT	2	0x0	Initial value of signal indicating the horizontal pixel positions of the equalization pulses.
SD1_H_SER_PULSE_INIT	3	0x0	Initial value of signal indicating the horizontal pixel positions of the seration pulses.
SD1_V_EQ_SER_INIT	4	0x1	Initial value of signal indicating the lines that contain equalization or seration pulses.
SD1_V_SER_INIT	5	0x0	Initial value of signal indicating the lines that contain seration pulses.
SD1_H_BURST_INIT	6	0x0	Initial value of signal indicating the horizontal pixel position of the sub-carrier burst.
SD1_V_BURST_INIT	7	0x0	Initial value of signal indicating the lines that contain sub-carrier bursts.
SD1_H_SETUP_INIT	8	0x0	Initial value of signal indicating the horizontal pixel position of data with setup in NTSC or the maximum excursion of data in other standards.
SD1_V_SETUP_INIT	9	0x1	Initial value of signal indicating the lines that have setup in NTSC or the maximum possible excursion of lines with active data in other standards.
SD1_V_ACTIVE_INIT	10	0x1	Initial value of signal indicating the lines that have active data.
This register specifies the initial values of various internal SDTV1 timing controls. These values are set during reset, SD1_MAIN_CNTL.SD1_TV_ASYNC_RST = 1, or at frame synchronization, SD1_FRAME_SYNC_PULSE = 1. The particular field is set active high if the positioning of the initial pixel within the frame, as indicated by SD1_H_COUNT_INIT, SD1_V_COUNT_INIT, and SD1_F_COUNT_INIT, would mean that the indicated control should be active, ex. SD1_H_HSYNC_INIT=1 if SD1_H_HSYNC_START < SD1_H_COUNT_INIT <= SD1_H_HSYNC_END and SD1_V_COUNT_INIT is outside the SD1_TIMING_V_EQUALIZATION lines.			

SD1_TIMING_H_HSYNC - RW - 32 bits - [MMReg:0x5E20]			
Field Name	**Bits**	**Default**	**Description**
SD1_H_HSYNC_START	11:0	0x0	The first pixel of the horizontal synchronization pulse in terms of TV1_CLK pixel count is SD1_H_HSYNC_START + 1.
SD1_H_HSYNC_END	27:16	0xfa	Indicates the last pixel of the horizontal synchronization pulse in terms of TV1_CLK pixel count.
This register indicates the timing points of the SDTV1 endcoder horizontal synchronization pulse			

SD1_TIMING_H_EQUALIZATION1 - RW - 32 bits - [MMReg:0x5E24]			
Field Name	**Bits**	**Default**	**Description**
SD1_H_EQ_PULSE_START1	11:0	0x0	The first pixel of the first equalization pulse in terms of TV1_CLK pixel count is SD1_H_EQ_PULSE_START1 + 1.
SD1_H_EQ_PULSE_END1	27:16	0x7d	Indicates the last pixel of the first equalization pulse in terms of TV1_CLK pixel count.
This register indicates the horizontal timing points of the first equalization pulse on the SDTV1 endcoder line.			

SD1_TIMING_H_EQUALIZATION2 - RW - 32 bits - [MMReg:0x5E28]			
Field Name	**Bits**	**Default**	**Description**
SD1_H_EQ_PULSE_START2	11:0	0x6a6	The first pixel of the second equalization pulse in terms of TV1_CLK pixel count is SD1_H_EQ_PULSE_START2 + 1.
SD1_H_EQ_PULSE_END2	27:16	0x723	Indicates the last pixel of the second equalization pulse in terms of TV1_CLK pixel count.
This register indicates the horizontal timing points of the second equalization pulse on the SDTV1 endcoder line.			

SD1_TIMING_H_SERATION1 - RW - 32 bits - [MMReg:0x5E2C]			
Field Name	**Bits**	**Default**	**Description**
SD1_H_SER_PULSE_START1	11:0	0x0	The first pixel of the first seration pulse in terms of TV1_CLK pixel count is SD1_H_SER_PULSE_START1 + 1.
SD1_H_SER_PULSE_END1	27:16	0x5ac	Indicates the last pixel of the first seration pulse in terms of TV1_CLK pixel count.
This register indicates the horizontal timing points of the first seration pulse on the SDTV1 endcoder line.			

SD1_TIMING_H_SERATION2 - RW - 32 bits - [MMReg:0x5E30]			
Field Name	**Bits**	**Default**	**Description**
SD1_H_SER_PULSE_START2	11:0	0x6a6	The first pixel of the second seration pulse in terms of TV1_CLK pixel count is SD1_H_SER_PULSE_START2 + 1.
SD1_H_SER_PULSE_END2	27:16	0xc52	Indicates the last pixel of the second seration pulse in terms of TV1_CLK pixel count.
This register indicates the horizontal timing points of the second seration pulse on the SDTV1 endcoder line			

SD1_TIMING_V_EQUALIZATION1 - RW - 32 bits - [MMReg:0x5E34]			
Field Name	**Bits**	**Default**	**Description**
SD1_V_EQ_PULSE_START1	11:0	0x4dd	SD1_V_EQ_PULSE_START1(10:1) indicates, in terms of line count, the first line containing an equalization pulse for the first field. If the LSB is 0, this first line has both equalization pulses or if 1, then only the second pulse (starts on second pulse).
SD1_V_EQ_PULSE_DUR1	26:15	0xf	SD1_V_EQ_PULSE_DUR1(4:1) + 1 indicates the number of lines that contain equalization or seration pulses for the first field, i.e. last line with a equalization pulse is SD1_V_EQ_PULSE_START1(10:1) + SD1_V_EQ_PULSE_DUR1(4:1). If the LSB is 0, this last line has only the first equalization pulse or if 1, then both pulses (ends on second pulse).
This register indicates the vertical timing points of the SDTV1 encoder equalization pulses in the first field			

SD1_TIMING_V_EQUALIZATION2 - RW - 32 bits - [MMReg:0x5E38]			
Field Name	**Bits**	**Default**	**Description**
SD1_V_EQ_PULSE_START2	11:0	0x26c	SD1_V_EQ_PULSE_START2(10:1) indicates, in terms of line count, the first line containing an equalization pulse for the second field. If the LSB is 0, this first line has both equalization pulses or if 1, then only the second pulse (starts on second pulse).
SD1_V_EQ_PULSE_DUR2	26:15	0xe	SD1_V_EQ_PULSE_DUR2(4:1) + 1 indicates the number of lines that contain equalization or seration pulses for the second field, i.e. last line with a equalization pulse is SD1_V_EQ_PULSE_START2(10:1) + SD1_V_EQ_PULSE_DUR2(4:1). If the LSB is 0, this last line has only the first equalization pulse or if 1, then both pulses (ends on second pulse).
This register indicates the vertical timing points of the SDTV1 encoder equalization pulses in the second field			

SD1_TIMING_V_SERATION1 - RW - 32 bits - [MMReg:0x5E3C]			
Field Name	**Bits**	**Default**	**Description**
SD1_V_SER_PULSE_START1	11:0	0x0	SD1_V_SER_PULSE_START1(10:1) indicates, in terms of line count, the first line containing a seration pulse for the first field. If the LSB is 0, this first line has both seration pulses or if 1, then only the second pulse (starts on second pulse).
SD1_V_SER_PULSE_DUR1	26:15	0x4	SD1_V_SER_PULSE_DUR1(3:1) + 1 indicates the number of lines that contain seration pulses for the first field, i.e. last line with a seration pulse is SD1_V_SER_PULSE_START1(10:1) + SD1_V_SER_PULSE_DUR1(3:1). If the LSB is 0, this last line has only the first seration pulse or if 1, then both pulses (ends on second pulse).
This register indicates the vertical timing points of the SDTV1 encoder seration pulses in the first field			

SD1_TIMING_V_SERATION2 - RW - 32 bits - [MMReg:0x5E40]			
Field Name	**Bits**	**Default**	**Description**
SD1_V_SER_PULSE_START2	11:0	0x271	SD1_V_SER_PULSE_START2(10:1) indicates, in terms of line count, the first line containing a seration pulse for the second field. If the LSB is 0, this first line has both seration pulses or if 1, then only the second pulse (starts on second pulse).
SD1_V_SER_PULSE_DUR2	26:15	0x5	SD1_V_SER_PULSE_DUR2(3:1) + 1 indicates the number of lines that contain seration pulses for the second field, i.e. last line with a seration pulse is SD1_V_SER_PULSE_START2(10:1) + SD1_V_SER_PULSE_DUR2(3:1). If the LSB is 0, this last line has only the first seration pulse or if 1, then both pulses (ends on second pulse).
This register indicates the vertical timing points of the SDTV1 encoder seration pulses in the second field			

SD1_TIMING_H_BURST - RW - 32 bits - [MMReg:0x5E44]			
Field Name	**Bits**	**Default**	**Description**
SD1_H_BURST_START	11:0	0x12a	The first pixel of the sub-carrier burst in terms of TV1_CLK pixel count is at SD1_H_BURST_START + 1. Note that for the SECAM standard, this field indicates the start of an advanced sub-carrier activation in order to suppress the initial amplitude spike: SD1_H_BURST_START = Specified SECAM sub-carrier pixel start - SD1_H_BURST_DUR.
SD1_H_BURST_DUR	23:16	0x78	SD1_H_BURST_DUR + 1 indicates the duration of the sub-carrier burst in terms of number of TV1_CLK pixels. The last sub-carrier burst pixel is at SD1_H_BURST_START + SD1_H_BURST_DUR. Note that for the SECAM standard, this field indicates the duration in TV1_CLK pixels of the internal turn-on sub-carrier spike suppression, see SD1_H_BURST_START description. Usually set to 30 or 40 in SECAM.
This register indicates the horizontal timing points of the sub-carrier burst on the SDTV1 endcoder line			

SD1_TIMING_V_BURST1 - RW - 32 bits - [MMReg:0x5E48]			
Field Name	**Bits**	**Default**	**Description**
SD1_V_BURST_START1	10:0	0x6	Indicates the first line containing a sub-carrier burst in the first field in terms of line count
SD1_V_BURST_END1	26:16	0x134	Indicates the last line containing a sub-carrier burst in the first field in terms of line count
SD1_ALT_BURST_BLANK_EN	28	0x1	This bit enables a different vertical burst blanking sequence for the third and fourth fields, as required in PAL systems.
SD1_ALT_V_BURST_START1	29	0x1	Adjusts the third field sub-carrier burst start line, ONLY if SD1_ALT_BURST_BLANK_EN = 1, usually set to 1.
SD1_ALT_V_BURST_END1	30	0x0	Adjusts the third field sub-carrier burst end line, ONLY if SD1_ALT_BURST_BLANK_EN = 1, usually set to 0.
This register indicates the vertical timing points of the SDTV1 encoder sub-carrier bursts in the first and third fields			

SD1_TIMING_V_BURST2 - RW - 32 bits - [MMReg:0x5E4C]			
Field Name	**Bits**	**Default**	**Description**
SD1_V_BURST_START2	10:0	0x13e	Indicates the first line containing a sub-carrier burst in the second field in terms of line count.
SD1_V_BURST_END2	26:16	0x26c	Indicates the last line containing a sub-carrier burst in the second field in terms of line count.
SD1_ALT_V_BURST_START2	28	0x0	Adjusts the fourth field sub-carrier burst start line, ONLY if SD1_ALT_BURST_BLANK_EN = 1, usually set to 0.
SD1_ALT_V_BURST_END2	29	0x0	Adjusts the fourth field sub-carrier burst end line, ONLY if SD1_ALT_BURST_BLANK_EN = 1, usually set to 0.
This register indicates the vertical timing points of the SDTV1 encoder sub-carrier bursts in the second and fourth fields			

SD1_TIMING_H_SETUP1 - RW - 32 bits - [MMReg:0x5E50]			
Field Name	**Bits**	**Default**	**Description**
SD1_H_SETUP_START1	11:0	0x22f	The first pixel of normal width active data in terms of TV1_CLK pixel count is SD1_H_SETUP_START1 + 1.
SD1_H_SETUP_END1	27:16	0xcfd	Indicates the last pixel of normal width active data in terms of TV1_CLK pixel count.
This register indicates the horizontal timing points of the full width active data, with (NTSC) or without a setup level, on the SDTV1 endcoder line			

SD1_TIMING_H_SETUP2 - RW - 32 bits - [MMReg:0x5E54]			
Field Name	**Bits**	**Default**	**Description**
SD1_H_SETUP_START2	11:0	0x6a6	The first pixel of partial width active data that starts later than normal, in terms of TV1_CLK pixel count, is SD1_H_SETUP_START2 + 1. This data would normally appear on the first line of the first field in PAL/SECAM and the first line of the second field in NTSC.
SD1_H_SETUP_END2	27:16	0x656	Indicates the last pixel of partial width active data that ends earlier than normal, in terms of TV1_CLK pixel count. This data would normally appear on the last line of the second field in PAL/SECAM and the last line of the first field in NTSC.
This register indicates the horizontal timing points of the partial width active data, with (NTSC) or without a setup level, on the SDTV1 endcoder line			

SD1_TIMING_V_SETUP1 - RW - 32 bits - [MMReg:0x5E58]			
Field Name	**Bits**	**Default**	**Description**
SD1_V_SETUP_START1	11:0	0x2d	SD1_V_SETUP_START1(10:1) indicates, in terms of line count, the first line where active data is allowed in the first field. If the LSB is 0, the active data on this first line has a horizontal pixel start point as listed in SD1_TIMING_H_SETUP1.SD1_H_SETUP_START1 or if 1, then it starts as listed in SD1_TIMING_H_SETUP2.SD1_H_SETUP_START2.
SD1_V_SETUP_END1	26:15	0x26a	SD1_V_SETUP_END1(10:1) indicates, in terms of line count, the last line where active data is allowed in the first field. If the LSB is 0, the active data on this last line has a horizontal pixel end point as listed in SD1_TIMING_H_SETUP1.SD1_H_SETUP_END1 or if 1, then it ends as listed in SD1_TIMING_H_SETUP2.SD1_H_SETUP_END2.
This register indicates the vertical timing points of the SDTV1 endcoder active data, with (NTSC) or without a setup level, in the first field			

SD1_TIMING_V_SETUP2 - RW - 32 bits - [MMReg:0x5E5C]			
Field Name	**Bits**	**Default**	**Description**
SD1_V_SETUP_START2	11:0	0x29e	SD1_V_SETUP_START2(10:1) indicates, in terms of line count, the first line where active data is allowed in the second field. If the LSB is 0, the active data on this first line has a horizontal pixel start point as listed in SD1_TIMING_H_SETUP1.SD1_H_SETUP_START1 or if 1, then it starts as listed in SD1_TIMING_H_SETUP2.SD1_H_SETUP_START2.
SD1_V_SETUP_END2	26:15	0x4dd	SD1_V_SETUP_END2(10:1) indicates, in terms of line count, the last line where active data is allowed in the second field. If the LSB is 0, the active data on this last line has a horizontal pixel end point as listed in SD1_TIMING_H_SETUP1.SD1_H_SETUP_END1 or if 1, then it ends as listed in SD1_TIMING_H_SETUP2.SD1_H_SETUP_END2.
This register indicates the vertical timing points of the SDTV1 endcoder active data, with (NTSC) or without a setup level, in the second field			

SD1_TIMING_H_ADV_ACTIVE - RW - 32 bits - [MMReg:0x5E60]			
Field Name	**Bits**	**Default**	**Description**
SD1_H_ADV_ACTIVE_START1	11:0	0x22d	The advanced active start pulse for normal width active data appears at pixel SD1_H_ADV_ACTIVE_START1 + 1, in terms of TV1_CLK pixel count.
SD1_H_ADV_ACTIVE_START2	27:16	0x6a4	The advanced active start pulse for partial width, late arrival active data appears at pixel SD1_H_ADV_ACTIVE_START2 + 1, in terms of TV1_CLK pixel count.
This register controls the generation of an advanced start pulse for every line with active data, as specified in SD1_TIMING_V_ACTIVE1 and SD1_TIMING_V_ACTIVE2. This start pulse is output from the SDTV1 encoder, but is used entirely for emulation purposes only			

SD1_TIMING_V_ACTIVE1 - RW - 32 bits - [MMReg:0x5E64]			
Field Name	**Bits**	**Default**	**Description**
SD1_V_ACTIVE_START1	11:0	0x2c	SD1_V_ACTIVE_START1(10:1) indicates, in terms of line count, the first line where active data is actually drawn in the first field. If the LSB is 0, the advanced active start pulse for this line appears as listed in SD1_TIMING_H_ADV_ACTIVE.SD1_H_ADV_ACTIVE_START1 or if 1, then as listed in SD1_TIMING_H_ADV_ACTIVE.SD1_H_ADV_ACTIVE_START2.
SD1_V_ACTIVE_END1	26:16	0x135	Indicates the last line where active data is actually drawn in the first field in terms of line count.
This register indicates the vertically cropped timing points of the SDTV1 endcoder active data in the first field. It represents the actual vertical limits of active data in the first field, which may be less than or equal to the standard specifications listed in SD1_TIMING_V_SETUP1. It indicates which lines to allow the advanced active start pulses, as specified by SD1_TIMING_H_ADV_ACTIVE, which lines to apply the test pattern if SD1_MAIN_CNTL.SD1_PATTERN_GEN_EN = 1, which lines to apply the active filters, as specified by SD1_TIMING_H_ACTIVE_FILT_WINDOW1 and SD1_TIMING_H_ACTIVE_FILT_WINDOW2, and which lines to comb if SD1_LUMA_COMB_FILT_CNTL1.SD1_COMB_EN = 1			

SD1_TIMING_V_ACTIVE2 - RW - 32 bits - [MMReg:0x5E68]			
Field Name	**Bits**	**Default**	**Description**
SD1_V_ACTIVE_START2	11:0	0x29e	SD1_V_ACTIVE_START2(10:1) indicates, in terms of line count, the first line where active data is actually drawn in the second field. If the LSB is 0, the advanced active start pulse for this line appears as listed in SD1_TIMING_H_ADV_ACTIVE.SD1_H_ADV_ACTIVE_START1 or if 1, then as listed in SD1_TIMING_H_ADV_ACTIVE.SD1_H_ADV_ACTIVE_START2.
SD1_V_ACTIVE_END2	26:16	0x26e	Indicates the last line where active data is actually drawn in the second field in terms of line count.
This register indicates the vertically cropped timing points of the SDTV1 endcoder active data in the second field. It represents the actual vertical limits of active data in the second field, which may be less than or equal to the standard specifications listed in SD1_TIMING_V_SETUP2. It indicates which lines to allow the advanced active start pulses, as specified by SD1_TIMING_H_ADV_ACTIVE, which lines to apply the test pattern if SD1_MAIN_CNTL.SD1_PATTERN_GEN_EN = 1, which lines to apply the active filters, as specified by SD1_TIMING_H_ACTIVE_FILT_WINDOW1 and SD1_TIMING_H_ACTIVE_FILT_WINDOW2, and which lines to comb if SD1_LUMA_COMB_FILT_CNTL1.SD1_COMB_EN = 1			

SD1_TIMING_H_ACTIVE_FILT_WINDOW1 - RW - 32 bits - [MMReg:0x5E8C]			
Field Name	**Bits**	**Default**	**Description**
SD1_H_ACTIVE_FILT_START1	11:0	0x22f	The first pixel to use the active data filter in terms of TV1_CLK pixel count is SD1_H_ACTIVE_FILT_START1 + 1. The setting is related to the pixel start of normal width data and the filter pipeline delay, so typical values are: SD1_TIMING_H_SETUP1.SD1_H_SETUP_START1 to SD1_TIMING_H_SETUP1.SD1_H_SETUP_START1 + pipeline delay/2(12).
SD1_H_ACTIVE_FILT_END1	27:16	0xd14	Indicates the last pixel to use the active data filter in terms of TV1_CLK pixel count. The setting is related to the end pixel of normal width data and the filter pipeline delay, so typical values are: SD1_TIMING_H_SETUP1.SD1_H_SETUP_END1 + pipeline delay/2(12) to SD1_TIMING_H_SETUP1.SD1_H_SETUP_END1 + pipeline delay(24).
This register indicates the horizontal timing points that must be applied to filter the full width active data on the SDTV1 endcoder line. It identifies the pixel window in which the Luminance filter settings, as specified by register SD1_LUMA_FILT_CNTL, apply.			

SD1_TIMING_H_ACTIVE_FILT_WINDOW2 - RW - 32 bits - [MMReg:0x5E90]			
Field Name	**Bits**	**Default**	**Description**
SD1_H_ACTIVE_FILT_START2	11:0	0x6a6	The first pixel to use the active data filter on a line where active data starts later than normal is SD1_H_ACTIVE_FILT_START2 + 1. The setting is related to the late pixel start of partial width data and the filter pipeline delay, so typical values are: SD1_TIMING_H_SETUP2.SD1_H_SETUP_START2 to SD1_TIMING_H_SETUP2.SD1_H_SETUP_START2 + pipeline delay/2(12).
SD1_H_ACTIVE_FILT_END2	27:16	0x66d	Indicates the last pixel to use the active data filter on a line where active data ends earlier than normal. The setting is related to the early end pixel of partial width data and the filter pipeline delay, so typical values are: SD1_TIMING_H_SETUP2.SD1_H_SETUP_END2 + pipeline delay/2(12) to SD1_TIMING_H_SETUP2.SD1_H_SETUP_END2 + pipeline delay(24).
This register indicates the horizontal timing points that must be applied to filter the partial width active data on the SDTV1 endcoder line. It identifies the pixel window in which the Luminance filter settings, as specified by register SD1_LUMA_FILT_CNTL, apply.			

SD1_TIMING_H_RUNIN_FILT_WINDOW - RW - 32 bits - [MMReg:0x5E94]			
Field Name	**Bits**	**Default**	**Description**
SD1_H_RUNIN_FILT_START	11:0	0x1c6	The first pixel to use the clk-runin filter in terms of TV1_CLK pixel count is SD1_H_RUNIN_FILT_START + 1.
SD1_H_RUNIN_FILT_END	27:16	0x430	Indicates the last pixel to use the clk-runin filter in terms of TV1_CLK pixel count.
Horizontal timing information for clk-runin filter window of the SDTV1 encoded VBI services CC and EDS. The clk-runin filter just passes the data untouched.			

SD1_Y_BREAK_POINT_SETTING - RW - 32 bits - [MMReg:0x5E98]			
Field Name	**Bits**	**Default**	**Description**
SD1_Y_GAIN_LIMIT	10:0	0x2ff	Gain (contrast) limit constant for the luminanace (Y) portion of the video signal. The range of this limiter is between 0 and 0x5FF.

SD1_Y_BREAK_EN	16	0x0	Enables/Disable the Y gain break. When enabled, the Y component of the video signal will be attenuated by one half, for the portion that exceeds the SD1_Y_GAIN_LIMIT value.
			  0=Disable
			  1=Enable

Contrast control register for Luminance portion of the video signal			

SD1_U_V_BREAK_POINT_SETTINGS - RW - 32 bits - [MMReg:0x5E9C]			
Field Name	**Bits**	**Default**	**Description**
SD1_U_GAIN_LIMIT	9:0	0x150	Gain (saturation) limit constant for the U portions of the chrominance video signal. The range of this limiter is between 0 and 0x17f.

SD1_U_BREAK_EN	12	0x0	Enables/Disable the U gain break. When enabled, the U components of the video signal will be attenuated by one half, for the portion that exceeds the SD1_U_GAIN_LIMIT value.
			  0=Disable
			  1=Enable

SD1_V_GAIN_LIMIT	25:16	0x1d7	Gain (saturation) limit constant for the V portions of the chrominance video signal. The range of this limiter is between 0 and 0x17f

SD1_V_BREAK_EN	28	0x0	Enables/Disable the V gain break. When enabled, the V components of the video signal will be attenuated by one half, for the portion that exceeds the SD1_V_GAIN_LIMIT value.
			  0=Disable
			  1=Enable

Saturation control register for the Chrominance portion of the video signal			

SD1_Y_AND_PASSTHRU_GAIN_SETTINGS - RW - 32 bits - [MMReg:0x5EA0]			
Field Name	**Bits**	**Default**	**Description**
SD1_Y_GAIN	8:0	0x100	Unsigned 1.8 bit gain (contrast) value for the luminanace (Y) portion of the video signal. The maximum value is 100110011 (gain = 1.20).
SD1_VBI_PASSTHRU_GAIN	24:16	0x100	Unsigned 1.8 bit gain (contrast) value for the VBI pass through signal. The maximum value is 100110011 (gain = 1.20).
Contains contrast information for luminance video			

SD1_U_AND_V_GAIN_SETTINGS - RW - 32 bits - [MMReg:0x5EA4]			
Field Name	**Bits**	**Default**	**Description**
SD1_U_GAIN	8:0	0x100	Unsigned 1.8 bit gain setting for the U portions of the chrominance video signal. The maximum value is 100100000 (gain = 1.125). Values over 1.125 will be limited to 1.125.
SD1_V_GAIN	24:16	0x100	Unsigned 1.8 bit gain setting for the V portions of the chrominance video signal. The maximum value is 100100000 (gain = 1.125). Values over 1.125 will be limited to 1.125.
Contains saturation information for chrominance video			

SD1_LUMA_BLANK_SETUP_LEVELS - RW - 32 bits - [MMReg:0x5EA8]			
Field Name	**Bits**	**Default**	**Description**
SD1_BLANK_LEVEL	8:0	0xeb	Indicates the digital value of the luminance blanking level and is defined as SD1_LUMA_SYNC_TIP_LEVELS.SD1_Y_SYNC_TIP_LEVEL + digital equivalent of blank above sync tip. This blank above sync tip can be calculated by converting the sync voltage: (Sync Amplitude/Full Range DAC Amplitude for given Standard) * 1023(full input range of DAC).
SD1_SETUP_LEVEL	24:16	0xeb	Indicates the digital value of the black level in NTSC and is defined as SD1_BLANK_LEVEL + digital equivalent of black above blank level. This black above blank can be calculated by converting the pedestal IRE: (Setup IRE/Full White IRE) * Full Digital White = (7.5/92.5) * 512 = 42. SD1_SETUP_LEVEL = SD1_BLANK_LEVEL for all standards but NTSC.
Indicates the SDTV1 luminance blank and setup levels for Composite, S-Video, 480i & 480p Component, and RGB with sync on green outputs			

SD1_RGB_OR_PBPR_BLANK_LEVEL - RW - 32 bits - [MMReg:0x5EAC]			
Field Name	**Bits**	**Default**	**Description**
SD1_RGB_OR_PBPR_BLANK_LEVEL	8:0	0xeb	Indicates the digital value of the luminance blanking level for Red and Blue if generating a RGB with sync on Green or the blank level for Pb & Pr, if set to a Component 480I or 480P mode. The mid range value of 512 is usually used in the PbPr case.
SDTV1 Blank Level register for RGB with sync on Green if SD1_MAIN_CNTL.SD1_BLANK_ON_RB_SEL = 1 or for Component Pb and Pr			

SD1_LUMA_SYNC_TIP_LEVELS - RW - 32 bits - [MMReg:0x5EB0]			
Field Name	**Bits**	**Default**	**Description**
SD1_Y_SYNC_TIP_LEVEL	8:0	0x10	Indicates the digital value of the luminance sync tip or synchronization level. Usually set at 16 to give a 20 mV margin above the zero DAC level.
SD1_PBPR_SYNC_TIP_LEVEL	24:16	0x111	Indicates the digital value of the Pb and Pr sync tip level and is defined as SD1_RGB_OR_PBPR_BLANK_LEVEL - digital equivalent of blank above sync tip. See the SD1_LUMA_BLANK_SETUP_LEVELS.SD1_BLANK_LEVEL description for the blank above sync tip calculation. If no synchronizing pulses are required for Pb and Pr, set SD1_PBPR_SYNC_TIP_LEVEL = SD1_RGB_OR_PBPR_BLANK_LEVEL.
SDTV1 Sync Tip register for Luminance or for Component Pb and Pr			

SD1_LUMA_FILT_CNTL - RW - 32 bits - [MMReg:0x5EB4]			
Field Name	**Bits**	**Default**	**Description**
SD1_YFLT_EN	0	0x1	Enables/Disables the Luminance filter
SD1_COMPY_OUT_BLEND	11:8	0x4	Controls sharpness blending of luma filters for Composite output. Bits [3:2] select the alternate filter: 00=Composite 01=S-video 10=1:1 Slew 11=Raw un-filtered data. Bits [1:0] controls a 2-bit alpha blend: 00=100% alternate filter 01=75% alternate filter, 25% base filter 10=50% alternate filter, 50% base filter 11=25% alternate filter, 75% base filter The Composite filter is the base filter for the Composite output.

SD1_SVIDY_OUT_BLEND	15:12	0x0	Controls sharpness blending of luma filters for S-Video output.
			Bits [3:2] select the alternate filter:
			  00=S-Video
			  01=Composite
			  10=1:1 Slew
			  11=Raw un-filtered data
			Bits [1:0] controls a 2-bit alpha blend:
			  00=100% alternate filter
			  01=75% alternate filter, 25% base filter
			  10=50% alternate filter, 50% base filter
			  11=25% alternate filter, 75% base filter
			The S-Video filter is the base filter for the S-Video output.

SD1_COMP_PASSTHRU_BLEND	19:16	0x0	Controls sharpness blending of luma filters for Composite VBI passthrough output.
			Bits [3:2] select the alternate filter:
			  00=Composite
			  01=S-video
			  10=1:1 Slew
			  11=Raw un-filtered data
			Bits [1:0] controls a 2-bit alpha blend:
			  00=100% alternate filter
			  01=75% alternate filter, 25% base filter
			  10=50% alternate filter, 50% base filter
			  11=25% alternate filter, 75% base filter
			The Composite filter is the base filter for the Composite VBI passthrough output.

SD1_SVID_PASSTHRU_BLEND	23:20	0x0	Controls sharpness blending of luma filters for S-Video VBI passthrough output.
			Bits [3:2] select the alternate filter:
			  00=S-Video,
			  01=Composite,
			  10=1:1 Slew,
			  11=Raw un-filtered data.
			Bits [1:0] controls a 2-bit alpha blend:
			  00=100% alternate filter,
			  01=75% alternate filter, 25% base filter,
			  10=50% alternate filter, 50% base filter,
			  11=5% alternate filter, 75% base filter.
			The S-Video filter is the base filter for the S-Video VBI passthrough output.

SD1_OUTSIDE_ACTIVE_SLEW_EN	24	0x1	Enables/Disables Slewing of the video signal during the blank region. If disabled, the blank region of the video signal will be filtered with the filter settings specified above (_BLEND) for the active portion of the video signal. If enabled the blank region of the video signal will be slewed
SD1_INSIDE_ACTIVE_SLEW_EN	25	0x0	Enables/Disables Slewing of the video signal during the active region. If disabled, the active portion of the video signal will be filtered with _BLEND settings specified bove. If enabled, the active portion of the video signal will be slewed and no other filter settings will apply
SD1_LUMA_DITHER_SEL	29:28	0x0	Control the addition of dither to Luminance data. Choices are truncate, round, dither with random number, dither with previous data
Specifies filter settings and dither settings (first) for Luminance video signal			

SD1_LUMA_COMB_FILT_CNTL1 - RW - 32 bits - [MMReg:0x5EB8]

Field Name	Bits	Default	Description
SD1_COMB_EN	0	0x0	Enable/Disables the Combing on composite video output
SD1_DISABLE_FIRST_LAST	1	0x0	Enable/Disables Combing on the first and last active lines of the composite video output
SD1_COMB_LINE_SEL	9:8	0x0	Selects between 3 line comb, or 2 line from upper or lower two pair of lines.
SD1_P2	21:16	0x0	Reference level for AGC. Nominal 0x20.
SD1_P3	30:24	0x0	Gain up value for AGC.
Comb filter register control 1			

SD1_LUMA_COMB_FILT_CNTL2 - RW - 32 bits - [MMReg:0x5EBC]

Field Name	Bits	Default	Description
SD1_P4	7:0	0x0	Lower clip limit or force for AGC multiplier.
SD1_P5	8	0x0	Select control curve multiplier inputs.
SD1_P6	21:16	0x0	Sets coring level for nominal signals.
SD1_P7	27:24	0x0	Controls the slope of the coring process to be below the P6 threshold.
Comb filter register control 2			

SD1_LUMA_COMB_FILT_CNTL3 - RW - 32 bits - [MMReg:0x5EC0]

Field Name	Bits	Default	Description
SD1_P10	5:0	0x0	Gain of bandpassed centre line to subtract from the Y for composite. Notch level.
SD1_P8	16:8	0x0	Sets the final gain level for the control signal. Diagonal false color level.
SD1_P9	26:20	0x0	Upper clip limit or force for final control signal.
Comb filter register control 3			

SD1_LUMA_COMB_FILT_CNTL4 - RW - 32 bits - [MMReg:0x5EC4]

Field Name	Bits	Default	Description
SD1_P11	5:0	0x0	Gain of checker board false color to subtract
SD1_FORCE_P9	8	0x0	Forces upper value for P9.
Comb filter register control 4			

SD1_VIDOUT_MUX_CNTL - RW - 32 bits - [MMReg:0x5EC8]			
Field Name	**Bits**	**Default**	**Description**

SD1_VIDEO_SELECT_MUX0_EN	0	0x1	Enables/Disables the output mux 0.
			  0=Send data 0
			  1=Send data as selected by RED_MX

SD1_VIDEO_SELECT_MUX1_EN	1	0x1	Enables/Disables the output mux 1.
			  0=Send data 0
			  1=Send data as selected by GRN_MX

SD1_VIDEO_SELECT_MUX2_EN	2	0x1	Enables/Disables the output mux 2.
			  0=Send data 0
			  1=Send data as selected by BLU_MX

SD1_VIDEO_SELECT_MUX0	7:4	0x1	Output Mux selection for first SDTV1 output, which is normally routed to the triple DAC output DAC4_CHROMA.
			  0=iSVID_Y
			  1=iSVID_C
			  2=iCOMP
			  3=iGREEN
			  4=iBLUE
			  5=iRED
			  6=iYPBPR_Y
			  7=iPB
			  8=iPR
			  9=irf_FORCE_DAC_DATA
			  10=iDBG_INPUT_Y
			  11=iDBG_GAINED_Y
			  12=iDBG_YFORFILT
			  13=iDBG_SYNCb
			  14=iDBG_END_OF_STANDARD_FRAME
			  15=iDBG_RGB_Y

SD1_VIDEO_SELECT_MUX1	11:8	0x2	Output Mux selection for second SDTV1 output, which is normally routed to the triple DAC output DAC6_COMP.
			  0=iSVID_Y
			  1=iSVID_C
			  2=iCOMP
			  3=iGREEN
			  4=iBLUE
			  5=iRED
			  6=iYPBPR_Y
			  7=iPB
			  8=iPR
			  9=irf_FORCE_DAC_DATA
			  10=iDBG_INPUT_Y
			  11=iDBG_GAINED_Y
			  12=iDBG_YFORFILT
			  13=iDBG_SYNCb
			  14=iDBG_END_OF_STANDARD_FRAME
			  15=iDBG_RGB_Y

SD1_VIDEO_SELECT_MUX2	15:12	0x0	Output Mux selection for third SDTV1 output, which is normally routed to the triple DAC output DAC5_LUMA.
			  0=iSVID_Y
			  1=iSVID_C
			  2=iCOMP
			  3=iGREEN
			  4=iBLUE
			  5=iRED
			  6=iYPBPR_Y
			  7=iPB
			  8=iPR
			  9=irf_FORCE_DAC_DATA
			  10=iDBG_INPUT_Y
			  11=iDBG_GAINED_Y
			  12=iDBG_YFORFILT
			  13=iDBG_SYNCb
			  14=iDBG_END_OF_STANDARD_FRAME
			  15=iDBG_RGB_Y

SD1_ENCODER_BYPASS_EN	28	0x0	0=Bypass Encoder with DC offset in U,V 1=Bypass Encoder without any changes
SD1_VIDEO_OUTPUT_DITHER_SEL	31:30	0x0	Controls the addition of dither to all the output. Choices are truncate, round, dither with random number, and dither with previous data.
SDTV1 encoder output selection control register			

SD1_FORCE_DAC_DATA - RW - 32 bits - [MMReg:0x5ECC]			
Field Name	**Bits**	**Default**	**Description**
SD1_FORCE_DAC_DATA	9:0	0x0	Specifies a 10 bit value to be routed to those DAC(s) with the corresponding output selection mux(SD1_VIDOUT_MUX_CNTL.SD1_VIDEO_SELECT_MUX1 to .SD1_VIDEO_SELECT_MUX2) set to 9. The following registers must also be programmed: DAC_MUX_OUT_CNTL.MUX_CNTL_EN = 0 and DTO1_VCLK_DENOMIN.DTO1_EN = 0.
This register allows data to be directly applied to the triple DACs			

SD1_CHROMA_MOD_CNTL - RW - 32 bits - [MMReg:0x5EF0]			
Field Name	**Bits**	**Default**	**Description**
SD1_U_BURST_LEVEL	8:0	0x1b2	U component burst level. For NTSC: -(20IRE/92.5IRE) * 512 =0x191. For PAL: -(Sin45)*(21.5/100IRE)*512 = 0x1B2.
SD1_V_BURST_LEVEL	24:16	0x4e	V component burst level. For NTSC: = 0x0. For PAL: (cos45)*(21.5IRE/100IRE)*512 = 0x4E.
SD1_COL_SC_SECOND_CORR_EN	26	0x0	When set to 1 in NTSC/PAL modes, the Sub-Carrier DTO Accumulator is incremented by a second correction set by SD1_SCM_COL_SC_INC_CORR and SD1_SCM_COL_SC_DENOMIN. 0=Normal Sub-Carrier DTO correction with SD1_COL_SC_DENOMIN, SD1_COL_SC_INC, and SD1_COL_SC_INC_CORR 1=Additional Sub-Carrier DTO correction controlled by SD1_SCM_COL_SC_DENOMIN, SD1_SCM_COL_SC_INC_CORR
SD1_CHROMA_PRE_MOD_DELAY_EN	27	0x0	When rf_PIX_DELAY_SEL = 0, it sets the pixel delay alignment of chrominance signal before or after modulation.
SD1_FORCE_BLACK_WHITE	29	0x0	Forces U and V values to be zero 0=Colour ON 1=Colour OFF
SD1_FORCE_BURST_ALWAYS	30	0x0	Active data will be ignored and Burst will be inserted all of the way through. 0=Normal Colour Burst production in encoder 1=Colour Burst fills the entire TV frame
SD1_UVFLT_EN	31	0x1	If enabled, U and V data gets filtered in U and V filters respectively, or else no filtering occurs. 0=Bypass U and V filters 1=Enable U and V filters
Chroma modulation control register			

SD1_COL_SC_DENOMIN - RW - 32 bits - [MMReg:0x5EF4]			
Field Name	**Bits**	**Default**	**Description**
SD1_COL_SC_DENOMIN	24:0	0x2	This register value determines when SD1_COL_SC_INC_CORR register value should be used as the Increment value for Sub-Carrier DTO Accumulator.
Denominator portion of the correction factor. This field is used in NTSC/PAL mode and during Secam DB component generation			

SD1_COL_SC_INC - RW - 32 bits - [MMReg:0x5EF8]			
Field Name	**Bits**	**Default**	**Description**
SD1_COL_SC_INC	28:0	0x15555 555	This is the increment value the Sub-Carrier DTO need to increment by every cycle except when the count of SD1_SCM_COL_SC_DENOMIN is reached. When the count of SD1_SCM_COL_SC_DENOMIN is reached, we will increment the accumulator by SD1_COL_SC_INC_CORR instead of COL_SC_INC. Note: Use ssdtve.cpp to program this field.
Increment value for Sub-Carrier DTO Accumulator. Used for NTSC/PAL sin/cos generation. In Secam mode, used for DB component generation			

SD1_COL_SC_INC_CORR - RW - 32 bits - [MMReg:0x5EFC]			
Field Name	**Bits**	**Default**	**Description**
SD1_COL_SC_INC_CORR	28:0	0x15555 556	SD1_COL_SC_INC register value plus the correction factor. This total value will be the new Sub-Carrier DTO Accumulator increment when a count determined by SD1_SCM_COL_SC_DENOMIN register field is reached.
Increment value for Sub-Carrier DTO Accumulator + Numerator portion of the required correction factor. This field is used in NTSC/PAL mode and during Secam DB component generation			

SD1_SCM_COL_SC_DENOMIN - RW - 32 bits - [MMReg:0x5F00]			
Field Name	**Bits**	**Default**	**Description**
SD1_SCM_COL_SC_DENOMIN	24:0	0x0	This register value determines when SD1_SCM_COL_SC_INC_CORR register value should be used as the Increment value for Sub-Carrier DTO Accumulator.
This field is used only for Secam DR component generation. Denominator portion of the correction factor			

SD1_SCM_COL_SC_INC - RW - 32 bits - [MMReg:0x5F04]			
Field Name	**Bits**	**Default**	**Description**
SD1_SCM_COL_SC_INC	28:0	0x1533a 6ae	This is the increment value the Sub-Carrier DTO need to increment by every cycle except when the count of SD1_SCM_COL_SC_DENOMIN is reached. When the count of SD1_SCM_COL_SC_DENOMIN is reached, we will increment the accumulator by SD1_SCM_COL_SC_INC_CORR instead of SD1_SCM_COL_SC_INC.
This field is used only for Secam DR component generation. Increment value for Sub-Carrier DTO Accumulator.			

SD1_SCM_COL_SC_INC_CORR - RW - 32 bits - [MMReg:0x5F08]			
Field Name	**Bits**	**Default**	**Description**
SD1_SCM_COL_SC_INC_CORR	28:0	0x1533a 6ae	SD1_COL_SC_INC register value plus the correction factor. This total value will be the new Sub-Carrier DTO Accumulator increment when a count determined by SD1_SCM_COL_SC_DENOMIN register field is reached.
Increment value for Sub-Carrier DTO Accumulator + Numerator portion of the required correction factor			

SD1_SCM_MOD_CNTL - RW - 32 bits - [MMReg:0x5F0C]			
Field Name	**Bits**	**Default**	**Description**
SD1_SCM_BURST_GAIN	11:0	0x203	This register field value determines the amplitude of DR and DB signals.
SD1_SCM_NOTCH_TUNER	21:16	0x2c	Sets the center of Secam high frequency subcarrier pre-emphasis filter at 4.286MHz frequency. Can be fine tuned in KHz granularity if required.
SD1_SCM_ENABLE	24	0x0	Enables Secam mode, thereby generating Secam DR/DB color components. Setting this field high will disable NTSC and PAL color modulation.
SD1_SCM_RST_DTO_ON_BLANK	25	0x0	Qualifier required to reset the Sub-Carrier DTO accumulator when in Secam mode. In Secam mode, DTO is reset during blanking period.
SD1_SCM_INVERT_PHASE_EN	26	0x0	Enables phase inversion of the DR and DB subcarriers.
SD1_INVERT_SCM_3LINE	27	0x0	Swaps inversions specific to fields.
SD1_SCM_3LINE_INIT	29:28	0x0	This field value is loaded into an internal mod 2 counter. If loaded by 0, the count values are 0,1,2 corresponding to phase values of 0,0,180. If loaded by 1, the count values are 1,2,0 corresponding to phase values of 0,180,0 and so on.
SD1_SCM_2LINE_EN	30	0x0	This field will set the internal counter into a mod 1 mode and the corresponding phase values are 0 and 180.
SD1_SCM_DTO_LIMIT_EN	31	0x1	When set, the frequency swing of DR/DB components will be limited to a specific range. The register fields SD1_SCM_MIN_DTO_SWING and SD1_SCM_MAX_DTO_SWING will set the range. If this field is not set, there will be no limit set on the frequency swing.
Secam modulation control register			

SD1_SCM_DB_DR_SCALE_FACTORS - RW - 32 bits - [MMReg:0x5F10]			
Field Name	**Bits**	**Default**	**Description**
SD1_SCM_DB_SCALE_FACTOR	15:0	0xa5f5	This field value is multiplied to the 'U' output of the low frequency pre-emphasis filter to generate the frequency deviation for the DB component.
SD1_SCM_DR_SCALE_FACTOR	31:16	0x8c99	This field value is multiplied to the 'V' output of the low frequency pre-emphasis filter to generate the frequency deviation for the DR component.
Used for generating the required frequency deviation for DR and DB components			

SD1_SCM_MIN_DTO_SWING - RW - 32 bits - [MMReg:0x5F14]

Field Name	Bits	Default	Description
SD1_SCM_MIN_DTO_SWING	27:0	0x9620639	Sets the minimum frequency swing. Will take effect only when SD1_SCM_DTO_LIMIT_EN register field is set.
Sets the minimum frequency swing for DR/DB components			

SD1_SCM_MAX_DTO_SWING - RW - 32 bits - [MMReg:0x5F18]

Field Name	Bits	Default	Description
SD1_SCM_MAX_DTO_SWING	27:0	0xb713ce4	Sets the maximum frequency swing. Will take effect only when SD1_SCM_DTO_LIMIT_EN register field is set.
Sets the maximum frequency swing for DR/DB components			

SD1_CRC_CNTL - RW - 32 bits - [MMReg:0x5F1C]

Field Name	Bits	Default	Description

SD1_CRC_EN	0	0x0	Enables the CRC signature generation on those output(s) as selected by SD1_CRC_DATAIN_SEL.
			  0=Reset/Disable
			  1=Enable

SD1_CRC_DATAIN_SEL	5:4	0x0	Selects the SDTV1 output(s) on which the CRC generation is to be performed.
			  0=V0V1V2
			  1=V0 only
			  2=V1 only
			  3=V2 only

SD1_RST_SC_ON_FSYNC_4CRC	7	0x0	Forces the sub-carrier to be reset at every frame synchronization pulse to allow CRC generation across something other than the standard number of fields per frame(4 for NTSC, 8 for PAL).
			  0=Normal free running Sub-Carrier
			  1=Enable reset of Sub-Carrier every Frame Sync

SD1_PROGRESSIVE_MODE_CRC	8	0x0	Selects interlaced of progressive mode CRC generation.
			  0=CRC generation for interlaced modes
			  1=CRC generation for progressive modes

Controls the production of CRC signatures from the SDTV1 encoder output(s)			

SD1_VIDEO_PORT_SIG - RW - 32 bits - [MMReg:0x5F20]

Field Name	Bits	Default	Description
SD1_CRC_SIG (R)	29:0	0x0	SD1_CRC_SIG(9:0)=CRC signature of VIDEO_0 output SD1_CRC_SIG(19:10)=CRC signature of VIDEO_1 output SD1_CRC_SIG(29:20)=CRC signature of VIDEO_2 output
Read only register containing the CRC signatures for VIDEO_0, VIDEO_1, and VIDEO_2 outputs of the SDTV1 encoder			

SD1_SDTV0_DEBUG - RW - 32 bits - [MMReg:0x5F28]			
Field Name	**Bits**	**Default**	**Description**
SD1_SDTV0_DEBUG	31:0	0xffff	SD1_SDTV0_DEBUG(31:0)=Unassigned SD1_SDTV0_DEBUG(16)=Enable TVVBI muxing to debug bus.
The bits in this register can be assigned control functions, if the debugging process yields additional needs			

SD1_COL_SC_PHASE_CNTL - RW - 32 bits - [MMReg:0x5FD4]			
Field Name	**Bits**	**Default**	**Description**
SD1_COL_SC_PHASE_INIT	15:0	0x0	Adds phase offset to the Sub-Carrier DTO.
Phase offset to the Sub-Carrier DTO			

SD1_LUMA_OFFSET_LIMIT - RW - 32 bits - [MMReg:0x5F8C]			
Field Name	**Bits**	**Default**	**Description**
SD1_LUMA_OFFSET	9:0	0x0	Luma offset value used in conjunction with SD1_Y_GAIN for color conversion.
SD1_LUMA_LIMIT	21:12	0x0	Luma limit used for color conversion
SD1_YC_OFFSET_LIMIT_BYPASS	24	0x0	0=Luma and chroma data are both offset. Luma data is limited. 1=Bypass offset/limiting logic and sign extend luma and chroma data.
Luma offset used for color conversion			

SD1_CHROMA_OFFSET - RW - 32 bits - [MMReg:0x5F90]			
Field Name	**Bits**	**Default**	**Description**
SD1_CHROMA_OFFSET	9:0	0x0	Chroma offset value used in conjunction with SD1_U_GAIN & SD1_V_GAIN for color conversion.
Chroma offset used for color conversion			

SD1_UPSAMPLE_MODE - RW - 32 bits - [MMReg:0x5F94]			
Field Name	**Bits**	**Default**	**Description**
SD1_FOUR_TAP_MODE	0	0x0	
SD1_UPSAMP_PICK_NEAR	4	0x0	

SD1_CRTC_HV_START - RW - 32 bits - [MMReg:0x5F98]			
Field Name	**Bits**	**Default**	**Description**
SD1_CRTC_H_START	12:0	0x0	CRTC horizontal capture frame pulse start.
SD1_CRTC_V_START	28:16	0x0	CRTC vertical capture frame pulse start. Please note that in interlace mode, CRTC counts every other line, while TVOUT counts every line.
CRTC capture pulse start location			

SD1_CRTC_TV_FRAMESTART_CNTL - RW - 32 bits - [MMReg:0x5F9C]			
Field Name	**Bits**	**Default**	**Description**
SD1_CRTC_TV_FRAMESTART_FREQ	1:0	0x0	0=TV FRAMESTART happens every 2 fields 1=TV FRAMESTART happens every 4 fields, NTSC standard 2=TV FRAMESTART happens every 8 fields, PAL standard 3=Reserved

HD_EMBEDDED_SYNC_CNTL - RW - 32 bits - [MMReg:0x5FA0]			
Field Name	**Bits**	**Default**	**Description**
HD_EMBED_SYNC_EN_Y_G	0	0x0	0=Disable embedded sync on Y/G. 1=Enable embedded sync on Y/G.
HD_EMBED_SYNC_EN_PB_B	1	0x0	0=Disable embedded sync on Pb/B. 1=Enable embedded sync on Pb/B.
HD_EMBED_SYNC_EN_PR_R	2	0x0	0=Disable embedded sync on Pr/R. 1=Enable embedded sync on Pr/R.
HD_TRILEVEL_SYNC_EN	3	0x0	0=Embedded sync only negative, if enabled. 1=Embedded sync neg. and pos., if enabled.
HD_DEBUG0	31:16	0x0	Reserved

HD_INCR - RW - 32 bits - [MMReg:0x5FA4]			
Field Name	**Bits**	**Default**	**Description**
HD_INCR_Y_G	9:0	0x0	Increment value for Y.
HD_INCR_PB_B_PR_R	25:16	0x0	Increment value for PB and PR.

HD_TRILEVEL_DUR - RW - 32 bits - [MMReg:0x5FA8]			
Field Name	**Bits**	**Default**	**Description**
HD_TRILEVEL_DUR_Y	10:0	0x0	Negative and positive sync level duration for Y.
HD_TRILEVEL_DUR_PBPR	26:16	0x0	Negative and positive sync level duration for PB and PR.

HD_POS_SYNC_LEVEL - RW - 32 bits - [MMReg:0x5FAC]			
Field Name	**Bits**	**Default**	**Description**
HD_POS_SYNC_LEVEL_Y_G	9:0	0x0	Positive sync value for Y.
HD_POS_SYNC_LEVEL_PB_B_PR_R	25:16	0x0	Positive sync value for PB and PR.

HD_BACKPORCH_DUR - RW - 32 bits - [MMReg:0x5FB0]			
Field Name	**Bits**	**Default**	**Description**
HD_BP_DUR_Y	10:0	0x0	Back porch duration for Y.
HD_BP_DUR_PBPR	26:16	0x0	Back porch duration for PB and PR.

HD_SERATION_DUR - RW - 32 bits - [MMReg:0x5FB4]			
Field Name	**Bits**	**Default**	**Description**
HD_SER_DUR_Y	10:0	0x0	Duration of seration pulse for Y.
HD_SER_DUR_PBPR	26:16	0x0	Duration of seration pulse for PB and PR.

2.18 LVTMA Registers

LVTMA_CRC_CNTL - RW - 32 bits - [MMReg:0x7AB0]			
Field Name	**Bits**	**Default**	**Description**
LVTMA_CRC_EN	0	0x0	Enable LVTMA CRC calculation. 0=Disable 1=Enable
LVTMA_CRC_CONT_EN	4	0x0	Select continuous or one-shot mode for primary CRC. 0=CRC is calculated over 1 frame 1=CRC is continuously calculated for every frame
LVTMA_CRC_ONLY_BLANKb	8	0x0	Determines whether primary CRC is calculated for the whole frame or only during non-blank period. 0=CRC calculated over entire field 1=CRC calculated only during BLANKb
LVTMA_CRC_FIELD	12	0x0	Controls which field polarity starts the LVTMA CRC block after LVTMA_CRC_EN is set to 1. Used only for interlaced mode CRCs. 0=Even field begins CRC calculation 1=Odd field begins CRC calculation
LVTMA_2ND_CRC_EN	16	0x0	Enable LVTMA 2nd CRC calculation. 0=Disable 1=Enable
LVTMA_2ND_CRC_LINK_SEL	20	0x0	Select which LVTM link to perform CRC on. 0=Perform CRC on link0 1=Perform CRC on link1
LVTMA_2ND_CRC_DATA_SEL	25:24	0x1	Select whether to perform CRC on all data or a subset of the video frame. 0=2ND CRC calculated over entire field 1=2ND CRC calculated only during video data enable (plus preamble and guard band in HDMI mode) 2=2ND CRC calculated over vertical blank region, including VBI preamble and guard band region, excluding horizontal blank 3=2ND CRC calculated only during audio data enable
Enable LVTMA CRC Calculation			

LVTMA_CRC_SIG_MASK - RW - 32 bits - [MMReg:0x7AB4]			
Field Name	**Bits**	**Default**	**Description**
LVTMA_CRC_SIG_BLUE_MASK	7:0	0xff	CRC mask bits for LVTMA blue component.
LVTMA_CRC_SIG_GREEN_MASK	15:8	0xff	CRC mask bits for LVTMA green component.
LVTMA_CRC_SIG_RED_MASK	23:16	0xff	CRC mask bits for LVTMA red component.
LVTMA_CRC_SIG_CONTROL_MASK	26:24	0x7	CRC mask bits for LVTMA control signals 3-bit input value: Bit 2=Vsync Bit 1=Hsync Bit 0=Data Enable
RGB and Control CRC Mask			

LVTMA_CRC_SIG_RGB - RW - 32 bits - [MMReg:0x7AB8]			
Field Name	**Bits**	**Default**	**Description**
LVTMA_CRC_SIG_BLUE (R)	7:0	0x0	CRC signature value for LVTMA blue component
LVTMA_CRC_SIG_GREEN (R)	15:8	0x0	CRC signature value for LVTMA green component
LVTMA_CRC_SIG_RED (R)	23:16	0x0	CRC signature value for LVTMA red component
LVTMA_CRC_SIG_CONTROL (R)	26:24	0x0	CRC signature value for LVTMA control signals3-bit input value: Bit 2=Vsync Bit 1=Hsync Bit 0=Data Enable
RGB and Control CRC Result			

LVTMA_2ND_CRC_RESULT - RW - 32 bits - [MMReg:0x7ABC]			
Field Name	**Bits**	**Default**	**Description**
LVTMA_2ND_CRC_RESULT (R)	29:0	0x0	LVTMA 2ND CRC readback

2.19 Miscellaneous Detailed Register Reference

AGP_BASE_2 - RW - 32 bits - MCIND:0x103			
Field Name	**Bits**	**Default**	**Description**
AGP_BASE_ADDR_2	3:0	0x0	

BIF_SLAVE_CNTL - RW - 32 bits - [MMReg:0x180C]			
Field Name	**Bits**	**Default**	**Description**
DISABLE_FAD_CALC	0	0x0	Disables the FAD (non_posted decode) calculation used in the previous versions of BIF.
DISABLE_NONPOSTED_CHECK	1	0x0	When asserted BIF Slave does not wait for non-posted completion to assert Ack or Commit.
DISABLE_HDP_OWORD_ACCESS	2	0x0	When asserted BIF Slave does not issue OctaWord writes to HDP.
SPARE_BIT_3	3	0x0	Reserved.
SWBF2_DBL_RSYNC_C	4	0x1	Double Sync Pointer on CCLK domain.
SWBF2_DBL_RSYNC_S	5	0x1	Double Sync Pointer on SCLK domain.
SWBRBBM_DBL_RSYNC_C	6	0x1	Double Sync Pointer on CCLK domain.
SWBRBBM_DBL_RSYNC_S	7	0x1	Double Sync Pointer on SCLK domain.
SWBHDP_DBL_RSYNC_B	8	0x1	Double Sync Pointer on BCLK domain.
SWBHDP_DBL_RSYNC_C	9	0x1	Double Sync Pointer on CCLK domain.
SWBCFG_DBL_RSYNC_B	10	0x1	Double Sync Pointer on BCLK domain.
SWBCFG_DBL_RSYNC_C	11	0x1	Double Sync Pointer on CCLK domain.
SRB_DBL_RSYNC_B	12	0x1	Double Sync Pointer on BCLK domain.
SRB_DBL_RSYNC_C	13	0x1	Double Sync Pointer on CCLK domain.
BIF_HDP_fifo_WATERMARK	15:14	0x3	Values less than 11 will reduce the number of available slots in FIFO.
BIF_SRB_fifo_WATERMARK	17:16	0x3	Values less than 11 will reduce the number of available slots in FIFO.
BIF_RBBM_fifo_WATERMARK	19:18	0x3	Values less than 11 will reduce the number of available slots in FIFO.
HDP_STATUS_DBL_FLOP_EN	20	0x1	Double Sync HDP status indicators on CCLK domain.
DISABLE_ALLSLAVE_AGPBUSY	21	0x0	Removes all slave requests from AGP_BUSY assertion.
DISABLE_CFGSLAVE_AGPBUSY	22	0x0	Removes CFG slave requests from AGP_BUSY assertion.
BIF_DEBUGBUS_CYCLE_EN	23	0x0	Write 1 to cycle through entire BIF Debug BUS.
DISABLE_HOLD_RBBM_READ	24	0x0	Write 1 to allow HI to issue multiple reads to RBBM.
BIF_WAIT_FOR_READ	25	0x0	Forces HI to wait for SRB completion on a read.
BIF_F2_fifo_WATERMARK	27:26	0x3	Values less than 11 will reduce the number of available slots in FIFO.
BIF_PERF_COUNT_0_CLK_SEL	29:28	0x0	Clock select for performance counter. 11=MCLK 10=SCLK 01=BCLK 00=CCLK
BIF_PERF_COUNT_1_CLK_SEL	31:30	0x0	Clock select for performance counter. 11=MCLK 10=SCLK 01=BCLK 00=CCLK

Field Name	Bits	Default	Description
PMI_IO_DISABLE	0	0x0	Power Management for IO cycles. Disabled in D1, D2, and D3 in ACPI only.
PMI_MEM_DISABLE	1	0x0	Power Management for MEM cycles. Disabled in D1, D2, and D3.
PMI_BM_DISABLE	2	0x0	Power Management for Bus Mastering. Disabled in D1, D2, and D3.
PMI_INT_DISABLE	3	0x0	Power Management for interrupts. Disabled in D1, D2, and D3.
BUS2_IMMEDIATE_PMI_DISABLE	4	0x0	0=Address decode using register value 1=Address decode using PM state value
PM_BUSY_ASSERTION	5	0x0	0=Block PM busy assertion 1=Allow Assertion of PM Busy signal to northbridge
IGNORE_WAIT4COH	6	0x0	Ignores the state of WAIT4COHERENCY after 26 bit counter assertion
IGNORE_RBBM_HIBUSY	7	0x0	Ignores the state of STAT_RBBM_HIBUSY after 32 cycles.
BUS2_VGA_REG_COHERENCY_DIS	8	0x0	Disables VGA register coherency checking.
BUS2_VGA_MEM_COHERENCY_DIS	9	0x0	Disables VGA memory coherency checking.
BUS2_HDP_REG_COHERENCY_DIS	10	0x0	Disables HDP register coherency checking.
BUS2_GUI_INITIATOR_COHERENCY_DIS	11	0x0	Disables GUI register coherency checking.
BUS2_HDP_MEM_COHERENCY_DIS	12	0x0	Disables HDP memory coherency checking.
BUS2_PMI_MULTIFUNC_SEL	13	0x0	0=Pick greater of F0 or F1 power state 1=Pick lesser of F0 or F1 power state
BUS_MASTER_DIS	14	0x1	1=Disables the GFX master path. Reads abort with FF's returned
ENABLE_RBBM_HIBUSY_CFG	15	0x0	Adds RBBM busy requirements to CFG cycles.
F0_F1_BM_PMI_SELECT	16	0x0	0=Allow busmaster access for F0 and F1 if only one is in D3 1=Disable busmaster access for F0 and F1 if only one is in D3
MST_BUSY (R)	17	0x0	GFX master machine busy status.
AIC_CNTL_HOLD_RD_fifo	18	0x0	Hold master read FIFO.
AIC_CNTL_HOLD_RQ_fifo	19	0x0	Hold master request FIFO.
MSI_REARM	20	0x0	Write a 0, then a 1 to re-arm MSI at the end of the interrupt routine.
DISABLE_OUTSTANDING_READ	21	0x0	0=Four outstanding reads 1=One outstanding read
REQ_DBL_RSYNC_C	22	0x1	0=Single sync flop to CCLK domain for master request path 1=Double sync flop to CCLK domain for master request path
REQ_DBL_RSYNC_M	23	0x1	0=Single sync flop to MCLK domain for master request path 1=Double sync flop to MCLK domain for master request path
CPL_DBL_RSYNC_M	24	0x1	0=Single sync flop to MCLK domain for master completion path 1=Double sync flop to MCLK domain for master completion path
CPL_DBL_RSYNC_C	25	0x1	0=Single sync flop to CCLK domain for master completion path 1=Double sync flop to CCLK domain for master completion path

Table header: **BUS_CNTL - RW - 32 bits - [IOReg,MMReg:0x30]**

CPL_DBL_RSYNC_S	26	0x1	0=Single sync flop to SCLK domain for master completion path 1=Double sync flop to SCLK domain for master completion path
BIF_BUS_CNTL_BIT_27	27	0x1	Reserved.
ENABLE_BREAKOUT	28	0x0	1=Low coherency lock in BIF to disengage after 26 bit counter assertion
BUS2_IMMEDIATE_PMI_ENABLE	29	0x1	0=Address decode using register value 1=Address decode using PM state value
BUS2_IMMEDIATE_PMI_ENABLE_REG	30	0x1	0=Register read back value matches PM state 1=Register read back value same as programmed value
BUS2_IMMEDIATE_PMI_DISABLE_REG	31	0x0	0=Register read back value matches PM state 1=Register read back value same as programmed value

BUS_CNTL1 - RW - 32 bits - [IOReg,MMReg:0x34]			
Field Name	**Bits**	**Default**	**Description**
HDP_READ_DELAY_CNT	7:0	0x32	Sets the amount of read delay after HDP write.
HDP_READ_DELAY_CNT_EN	8	0x1	Delays HDP reads after a write.
STEREOSYNC_EN	9	0x0	1=Enable Stereosync on LVDS_ENA_BL PAD
PM_MODE_SEL	10	0x0	0=ACPI 1=APM
GFX_BM_DIS	11	0x0	0=Allow busmastering for GFX client 1=Block GFX busmastering in MC
AZ_BM_DIS	12	0x0	0=Allow busmastering for AZ client 1=Block AZ busmastering in MC
GFX_INT_STATUS (R)	13	0x0	1=Outstanding GFX interrupt
AZ_INT_STATUS (R)	14	0x0	1=Outstanding AZ interrupt
BUS_DEBUG_BIT_15	15	0x0	Reserved.
MCLK_GATE_COUNTER	23:16	0x7	Number of idle cycles before dynamic MCLK is turned off.
BUS_DEBUG_BIT_24	24	0x1	Reserved.
BUS_DEBUG_BIT_25	25	0x1	Reserved.
BUS_DEBUG_BIT_26	26	0x1	Reserved.
BUS_DEBUG_BIT_27	27	0x1	Reserved.
BUS_DEBUG_BIT_28	28	0x1	Reserved.
BUS_DEBUG_BIT_29	29	0x1	Reserved.
BUS_DEBUG_BIT_30	30	0x1	Reserved.
BUS_DEBUG_BIT_31	31	0x1	Reserved.

VGA25_PPLL_POST_DIV_SRC - RW - 32 bits - [MMReg:0x384]			
Field Name	**Bits**	**Default**	**Description**
VGA25_PPLL_POST_DIV_SRC	0	0x0	Determines source of lvtmclk, pixclk and dvoclk PPLL outputs. 0=External source (input of reference divider) 1=Output clock of display PLL
Determines source of pixel clocks when VGA clock speed is 25.175MHz in VGA timing mode			

VGA25_PPLL_POST_DIV - RW - 32 bits - [MMReg:0x388]			
Field Name	**Bits**	**Default**	**Description**

VGA25_PPLL_POST_DIV	6:0	0x2e	Post divider value of display PLL.
			    0x0 - 0x1=Reserved (divide PLL output by 2)
			    0x2=Divide PLL output by 2
			    0x3=Divide PLL output by 3
			    0x4=Divide PLL output by 4
			    0x5=Divide PLL output by 5
			    ...
			    0x7f=Divide PLL output by 127

Post divider value of PLL clocks when VGA clock speed is 25.175MHz in VGA timing mode			

VGA_MEM_WRITE_PAGE_ADDR - RW - 32 bits - [IOReg,MMReg:0x38]			
Field Name	**Bits**	**Default**	**Description**
VGA_MEM_WRITE_PAGE0_ADDR	9:0	0x0	Write page 0 address.
VGA_MEM_WRITE_PAGE1_ADDR	25:16	0x0	Write page 1 address.
VGA write page register			

VGA_MEM_READ_PAGE_ADDR - RW - 32 bits - [IOReg,MMReg:0x3C]			
Field Name	**Bits**	**Default**	**Description**
VGA_MEM_READ_PAGE0_ADDR	9:0	0x0	Read page 0 address.
VGA_MEM_READ_PAGE1_ADDR	25:16	0x0	Read page 1 address.
VGA read page register			

BIOS_0_SCRATCH - RW - 32 bits - [IOReg,MMReg:0x10]			
Field Name	**Bits**	**Default**	**Description**
BIOS_SCRATCH	31:0	0x0	Scratch pad for BIOS information.
Scratch pad for BIOS information			

BIOS_1_SCRATCH - RW - 32 bits - [IOReg,MMReg:0x14]			
Field Name	**Bits**	**Default**	**Description**
BIOS_SCRATCH	31:0	0x0	Scratch pad for BIOS information.
Scratch pad for BIOS information			

BIOS_2_SCRATCH - RW - 32 bits - [IOReg,MMReg:0x18]			
Field Name	**Bits**	**Default**	**Description**
BIOS_SCRATCH	31:0	0x0	Scratch pad for BIOS information.
Scratch pad for BIOS information			

BIOS_3_SCRATCH - RW - 32 bits - [IOReg,MMReg:0x1C]			
Field Name	**Bits**	**Default**	**Description**
BIOS_SCRATCH	31:0	0x0	Scratch pad for BIOS information.
Scratch pad for BIOS information			

BIOS_4_SCRATCH - RW - 32 bits - [IOReg,MMReg:0x20]			
Field Name	**Bits**	**Default**	**Description**
BIOS_SCRATCH	31:0	0x0	Scratch pad for BIOS information.
Scratch pad for BIOS information			

BIOS_5_SCRATCH - RW - 32 bits - [IOReg,MMReg:0x24]			
Field Name	**Bits**	**Default**	**Description**
BIOS_SCRATCH	31:0	0x0	Scratch pad for BIOS information.
Scratch pad for BIOS information			

BIOS_6_SCRATCH - RW - 32 bits - [IOReg,MMReg:0x28]			
Field Name	**Bits**	**Default**	**Description**
BIOS_SCRATCH	31:0	0x0	Scratch pad for BIOS information.
Scratch pad for BIOS information			

BIOS_7_SCRATCH - RW - 32 bits - [IOReg,MMReg:0x2C]			
Field Name	**Bits**	**Default**	**Description**
BIOS_SCRATCH	31:0	0x0	Scratch pad for BIOS information.
Scratch pad for BIOS information			

MEDIA_0_SCRATCH - RW - 32 bits - [IOReg,MMReg:0xB0]			
Field Name	**Bits**	**Default**	**Description**
MEDIA_0_SCRATCH	31:0	0x0	Scratch pad for multimedia driver information.
Scratch pad for multimedia driver information			

MEDIA_1_SCRATCH - RW - 32 bits - [IOReg,MMReg:0xB4]			
Field Name	**Bits**	**Default**	**Description**
MEDIA_1_SCRATCH	31:0	0x0	Scratch pad for multimedia driver information.
Scratch pad for multimedia driver information			

BIOS_8_SCRATCH - RW - 32 bits - [IOReg,MMReg:0xC0]			
Field Name	**Bits**	**Default**	**Description**
BIOS_SCRATCH	31:0	0x0	Scratch pad for BIOS information.
Scratch pad for BIOS information			

BIOS_9_SCRATCH - RW - 32 bits - [IOReg,MMReg:0xC4]			
Field Name	**Bits**	**Default**	**Description**
BIOS_SCRATCH	31:0	0x0	Scratch pad for BIOS information.
Scratch pad for BIOS information			

BIOS_10_SCRATCH - RW - 32 bits - [IOReg,MMReg:0xC8]			
Field Name	**Bits**	**Default**	**Description**
BIOS_SCRATCH	31:0	0x0	Scratch pad for BIOS information.
Scratch pad for BIOS information			

BIOS_11_SCRATCH - RW - 32 bits - [IOReg,MMReg:0xCC]			
Field Name	**Bits**	**Default**	**Description**
BIOS_SCRATCH	31:0	0x0	Scratch pad for BIOS information.
Scratch pad for BIOS information			

BIOS_12_SCRATCH - RW - 32 bits - [IOReg,MMReg:0xD0]			
Field Name	**Bits**	**Default**	**Description**
BIOS_SCRATCH	31:0	0x0	Scratch pad for BIOS information.
Scratch pad for BIOS information			

BIOS_13_SCRATCH - RW - 32 bits - [IOReg,MMReg:0xD4]			
Field Name	**Bits**	**Default**	**Description**
BIOS_SCRATCH	31:0	0x0	Scratch pad for BIOS information.
Scratch pad for BIOS information			

BIOS_14_SCRATCH - RW - 32 bits - [IOReg,MMReg:0xD8]			
Field Name	**Bits**	**Default**	**Description**
BIOS_SCRATCH	31:0	0x0	Scratch pad for BIOS information.
Scratch pad for BIOS information			

BIOS_15_SCRATCH - RW - 32 bits - [IOReg,MMReg:0xDC]			
Field Name	**Bits**	**Default**	**Description**
BIOS_SCRATCH	31:0	0x0	Scratch pad for BIOS information.
Scratch pad for BIOS information			

CONFIG_XSTRAP - RW - 32 bits - [IOReg,MMReg:0xE4]			
Field Name	**Bits**	**Default**	**Description**

VGA_DISABLE (R)	0	0x0	STRAP VALUE READBACK
			  0=VGA enabled
			  1=int gfx will abort VGA requests

ENINTB (R)	3	0x0	STRAP VALUE READBACK
			  0=Interrupts enabled
			  1=Interrupts disabled

ID_DISABLE (R)	14	0x0	STRAP VALUE READBACK
			  0=Normal
			  1=int gfx disabled

AP_SIZE (R)	18:16	0x0	STRAP VALUE READBACK
			  000=128M
			  001=256M
			  010=64M
			  011=32M
			  100=512M
			  101=1G

BUSCFG (R)	26:24	0x0	STRAP VALUE READBACK
			  0=BondingOption_INT_GFX
			  1=Reserved
			  2=ext gfx enable

CONFIG_MEM_BASE_LO - R - 32 bits - [MMReg:0x100]			
Field Name	**Bits**	**Default**	**Description**
CFG_MEM_BASE_LO	31:0	0x0	MEM_BASE_LO readback. Note: Bits [24:0] of this field are hardwired to 0.

CONFIG_MEM_BASE_HI - R - 32 bits - [MMReg:0x104]			
Field Name	**Bits**	**Default**	**Description**
CFG_MEM_BASE_HI	31:0	0x0	MEM_BASE_HI readback.

CONFIG_REG_BASE_LO - R - 32 bits - [MMReg:0x10C]			
Field Name	**Bits**	**Default**	**Description**
CFG_REG_BASE_LO	31:16	0x0	REG_BASE_LO readback.

CONFIG_REG_BASE_HI - R - 32 bits - [MMReg:0x110]			
Field Name	**Bits**	**Default**	**Description**
CFG_REG_BASE_HI	31:0	0x0	REG_BASE_HI readback.

HDP_FB_LOCATION - RW - 32 bits - [MMReg:0x134]			
Field Name	**Bits**	**Default**	**Description**
HDP_FB_START	15:0	0x0	Defines the location of the frame buffer in the internal address space. The internal address space has 32 address bits. It should have the same value as MC_FB_START, and must be aligned on 256B boundary Note: Bits [7:0] of this field are hardwired to 0.
Frame Buffer Location			

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Appendix A
Cross-Referenced Index

A.1 Quick Cross-Referenced Index

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For users of the PDF version of this document: in the tables below, click on the *name* of a register to go to the description of that register found in *Chapter 2*.

A.2 Index Registers Sorted by Name

Table 2-1 Index Registers Sorted by Name

Name	Address	Secondary Address	Additional Address	Page
ATTRX	*VGA_IO\:0x3C0*			*2-316*
CLOCK_CNTL_DATA	*IOReg:0xC*	*MMReg:0xC*		*2-267*
CLOCK_CNTL_INDEX	*IOReg:0x8*	*MMReg:0x8*		*2-267*
CRTC8_DATA	*MMReg:0x3B5*	*MMReg:0x3D5*	*VGA_IO:0x3B5 VGA_IO:0x3D5:IO :0x3D5*	*2-303*
CRTC8_IDX	*MMReg:0x3B4*	*MMReg:0x3D4*	*VGA_IO:0x3B4 VGA_IO:0x3D4:O: 0x3D4*	*2-303*
DAC_DATA	*VGA_IO\:0x3C9*			*2-296*
DAC_R_INDEX	*VGA_IO\:0x3C7*			*2-296*
DAC_W_INDEX	*VGA_IO\:0x3C8*			*2-296*
GRPH8_DATA	*MMReg:0x3CF*	*VGA_IO:0x3CF*		*2-312*
GRPH8_IDX	*MMReg:0x3CE*	*VGA_IO:0x3CE*		*2-312*
HTIU_NB_DATA	*nbconfig:0xAC*			*2-26*
HTIU_NB_INDEX	*nbconfig:0xA8*			*2-26*
MM_DATA	*IOReg:0x4*	*MMReg:0x4*		*2-127*
MM_INDEX	*IOReg:0x0*	*MMReg:0x0*		*2-127*
NB_MC_DATA	*nbconfig\:0xEC*			*2-25*
NB_MC_IND_DATA	*nbconfig:0x74*			*2-33*
NB_MC_IND_INDEX	*nbconfig:0x70*			*2-33*
NB_MC_INDEX	*nbconfig\:0xE8*			*2-24*
NB_MISC_DATA	*nbconfig\:0x64*			*2-7*
NB_MISC_INDEX	*nbconfig\:0x60*			*2-7*
NB_PCIE_INDX_ADDR	*nbconfig\:0xE0*			*2-24*
NB_PCIE_INDX_DATA	*nbconfig\:0xE4*			*2-24*
PCIE_PORT_DATA	*pcieConfigDev[10:2]\:0xE4*			*2-89*
PCIE_PORT_INDEX	*pcieConfigDev[10:2]\:0xE0*			*2-89*
SEQ8_DATA	*MMReg:0x3C5*	*VGA_IO:0x3C5*		*2-302*
SEQ8_IDX	*MMReg:0x3C4*	*VGA_IO:0x3C4*		*2-302*

A.3   All Registers Sorted By Name

Table 2-2   All Registers Sorted By Name

Name	Address	Secondary Address	Additional Address	Page
ADAPTER_ID	gcconfig:0x2C	MMReg:0x502C		2-111
ADAPTER_ID_W	gcconfig:0x4C	MMReg:0x504C:R		2-111
AGP_ADDRESS_SPACE_SIZE	NBMCIND\:0x38			2-160
AGP_BASE_2	MCIND:0x103			2-350
AGP_MODE_CONTROL	NBMCIND\:0x39			2-160
AIC_CTRL_SCRATCH	NBMCIND:0x3A			2-160
APC_ADAPTER_ID_W	apcconfig\:0x4C			2-151
APC_AGP_PCI_IO_LIMIT_BASE_HI	apcconfig\:0x30			2-149
APC_AGP_PCI_IOBASE_LIMIT	apcconfig\:0x1C			2-147
APC_AGP_PCI_IRQ_BRIDGE_CTRL	apcconfig\:0x3C			2-149
APC_AGP_PCI_MEMORY_LIMIT_BASE	apcconfig\:0x20			2-148
APC_AGP_PCI_PREFETCHABLE_BASE_Upper	apcconfig\:0x28			2-148
APC_AGP_PCI_PREFETCHABLE_LIMIT_BASE	apcconfig:0x24			2-148
APC_AGP_PCI_PREFETCHABLE_LIMIT_Upper	apcconfig\:0x2C			2-148
APC_AGP_PCI_STATUS	apcconfig:0x1E			2-147
APC_BASE_CODE	apcconfig\:0xB			2-146
APC_BIST	apcconfig\:0xF			2-146
APC_CACHE_LINE	apcconfig\:0xC			2-146
APC_CAPABILITIES_PTR	apcconfig:0x34			2-149
APC_COMMAND	apcconfig\:0x4			2-143
APC_DEVICE_ID	apcconfig:0x2			2-143
APC_HEADER	apcconfig\:0xE			2-146
APC_HT_MSI_CAP	apcconfig:0x44			2-151
APC_LATENCY	apcconfig\:0xD			2-146
APC_MISC_DEVICE_CTRL	apcconfig:0x40			2-151
APC_REGPROG_INF	apcconfig\:0x9			2-145
APC_REVISION_ID	apcconfig\:0x8			2-145
APC_SSID	apcconfig\:0xB4			2-152
APC_SSID_CAP_ID	apcconfig\:0xB0			2-152
APC_STATUS	apcconfig:0x6			2-144
APC_SUB_BUS_NUMBER_LATENCY	apcconfig\:0x18			2-147
APC_SUB_CLASS	apcconfig\:0xA			2-145
APC_VENDOR_ID	apcconfig\:0x0			2-143
ATTR00	VGAATTRIND\:0x0			2-316
ATTR01	VGAATTRIND\:0x1			2-317

Table 2-2 All Registers Sorted By Name

Name	Address	Secondary Address	Additional Address	Page
ATTR02	VGAATTRIND\:0x2			2-317
ATTR03	VGAATTRIND\:0x3			2-317
ATTR04	VGAATTRIND\:0x4			2-317
ATTR05	VGAATTRIND\:0x5			2-317
ATTR06	VGAATTRIND\:0x6			2-318
ATTR07	VGAATTRIND\:0x7			2-318
ATTR08	VGAATTRIND\:0x8			2-318
ATTR09	VGAATTRIND\:0x9			2-318
ATTR0A	VGAATTRIND\:0xA			2-318
ATTR0B	VGAATTRIND\:0xB			2-319
ATTR0C	VGAATTRIND\:0xC			2-319
ATTR0D	VGAATTRIND\:0xD			2-319
ATTR0E	VGAATTRIND\:0xE			2-319
ATTR0F	VGAATTRIND\:0xF			2-319
ATTR10	VGAATTRIND\:0x10			2-320
ATTR11	VGAATTRIND\:0x11			2-320
ATTR12	VGAATTRIND\:0x12			2-320
ATTR13	VGAATTRIND\:0x13			2-321
ATTR14	VGAATTRIND\:0x14			2-321
ATTRDR	VGA_IO\:0x3C1			2-316
ATTRDW	VGA_IO\:0x3C0			2-316
ATTRX	VGA_IO\:0x3C0			2-316
BACKBIAS_ENABLE_CNT	CLKIND:0x37			2-285
BASE_CODE	gcconfig:0xB	MMReg:0x500B		2-111
BIF_SLAVE_CNTL	MMReg:0x180C			2-350
BIOS_0_SCRATCH	IOReg:0x10	MMReg:0x10		2-353
BIOS_1_SCRATCH	IOReg:0x14	MMReg:0x14		2-353
BIOS_10_SCRATCH	IOReg:0xC8	MMReg:0xC8		2-355
BIOS_11_SCRATCH	IOReg:0xCC	MMReg:0xCC		2-355
BIOS_12_SCRATCH	IOReg:0xD0	MMReg:0xD0		2-355
BIOS_13_SCRATCH	IOReg:0xD4	MMReg:0xD4		2-355
BIOS_14_SCRATCH	IOReg:0xD8	MMReg:0xD8		2-355
BIOS_15_SCRATCH	IOReg:0xDC	MMReg:0xDC		2-356
BIOS_2_SCRATCH	IOReg:0x18	MMReg:0x18		2-353
BIOS_3_SCRATCH	IOReg:0x1C	MMReg:0x1C		2-354
BIOS_4_SCRATCH	IOReg:0x20	MMReg:0x20		2-354
BIOS_5_SCRATCH	IOReg:0x24	MMReg:0x24		2-354
BIOS_6_SCRATCH	IOReg:0x28	MMReg:0x28		2-354
BIOS_7_SCRATCH	IOReg:0x2C	MMReg:0x2C		2-354
BIOS_8_SCRATCH	IOReg:0xC0	MMReg:0xC0		2-355
BIOS_9_SCRATCH	IOReg:0xC4	MMReg:0xC4		2-355

Table 2-2 All Registers Sorted By Name

Name	Address	Secondary Address	Additional Address	Page
BIST	*gcconfig:0xF*	*MMReg:0x500F*		*2-112*
BUS_CNTL	*IOReg:0x30*	*MMReg:0x30*		*2-351*
BUS_CNTL1	*IOReg:0x34*	*MMReg:0x34*		*2-352*
CACHE_LINE	*gcconfig:0xC*	*MMReg:0x500C:R*		*2-114*
CAP_PTR	*pcieConfigDev[10:2]\:0x34*			*2-78*
CAPABILITIES_PTR	*gcconfig:0x34*	*MMReg:0x5034*		*2-112*
CC_COMBINED_STRAPS_0	*CLKIND:0x33*			*2-284*
CC_COMBINED_STRAPS_1	*CLKIND:0x34*			*2-285*
CC_DEBUG_STRAPS_0	*CLKIND:0x2F*			*2-281*
CC_DEBUG_STRAPS_1	*CLKIND:0x30*			*2-282*
CC_FUSE_STRAPS_0	*CLKIND:0x2D*			*2-280*
CC_FUSE_STRAPS_1	*CLKIND:0x2E*			*2-281*
CC_IO_STRAPS	*CLKIND:0x31*			*2-282*
CC_IO_STRAPS_12A	*CLKIND:0x31*			*2-283*
CC_IO_STRAPS_22A	*CLKIND:0x31*			*2-282*
CC_ROM_STRAPS	*CLKIND:0x32*			*2-283*
CFG_CT_CLKGATE_HTIU	*clkconfig:0xF8*			*2-138*
CG_CLKPIN_CNTL	*CLKIND:0x35*			*2-285*
CG_DEBUG	*CLKIND:0x20*			*2-277*
CG_INTGFX_MISC	*CLKIND:0x5C*			*2-292*
CG_INTGFX_SPARE_RO	*CLKIND:0x5D*			*2-293*
CG_MISC_REG	*CLKIND:0x1F*			*2-277*
CG_SPLL_ANALOG_CTRL0	*CLKIND:0x5A*			*2-292*
CG_SPLL_ANALOG_CTRL1	*CLKIND:0x5B*			*2-292*
CG_TC_JTAG_0	*CLKIND:0x38*			*2-286*
CG_TC_JTAG_1	*CLKIND:0x39*			*2-286*
CLK_CFG_HTPLL_CNTL	*clkconfig\:0xD4*			*2-136*
CLK_TOP_PERF_CNTL	*clkconfig:0xAC*			*2-135*
clk_top_pwm1_ctrl	*clkconfig:0xB0*			*2-141*
clk_top_pwm2_ctrl	*clkconfig:0xB4*			*2-141*
clk_top_pwm3_ctrl	*clkconfig:0xCC*			*2-142*
CLK_TOP_PWM4_CTRL	*clkconfig:0x4C*			*2-138*
CLK_TOP_PWM5_CTRL	*clkconfig:0x50*			*2-139*
CLK_TOP_SPARE_A	*clkconfig:0xE0*			*2-136*
CLK_TOP_SPARE_B	*clkconfig:0xE4*			*2-137*
CLK_TOP_SPARE_C	*clkconfig:0xE8*			*2-137*
CLK_TOP_SPARE_D	*clkconfig:0xEC*			*2-137*
clk_top_spare_pll	*clkconfig:0xD0*			*2-142*
clk_top_test_ctrl	*clkconfig:0xB8*			*2-141*
CLK_TOP_THERMAL_ALERT_INTR_EN	*clkconfig:0xC0*			*2-141*

Table 2-2 All Registers Sorted By Name

Name	Address	Secondary Address	Additional Address	Page
CLK_TOP_THERMAL_ALERT_STATUS	*clkconfig:0xC4*			*2-141*
CLK_TOP_THERMAL_ALERT_WAIT_WINDOW	*clkconfig:0xC8*			*2-142*
CLKGATE_DISABLE	*clkconfig:0x94*			*2-132*
CLKGATE_DISABLE2	*clkconfig:0x8C*			*2-132*
CLOCK_CNTL_DATA	*IOReg:0xC*	*MMReg:0xC*		*2-267*
CLOCK_CNTL_INDEX	*IOReg:0x8*	*MMReg:0x8*		*2-267*
COMMAND	*gcconfig:0x4*	*MMReg:0x5004:R*		*2-110*
CONFIG_APER_SIZE	*MMReg\:0x108*			*2-112*
CONFIG_CNTL	*IOReg\:0xE0*	*MMReg\:0xE0*		*2-112*
CONFIG_MEM_BASE_HI	*MMReg:0x104*			*2-356*
CONFIG_MEM_BASE_LO	*MMReg:0x100*			*2-356*
CONFIG_MEMSIZE	*IOReg\:0xF8*	*MMReg\:0xF8*		*2-112*
CONFIG_REG_APER_SIZE	*MMReg:0x114*			*2-113*
CONFIG_REG_BASE_HI	*MMReg:0x110*			*2-357*
CONFIG_REG_BASE_LO	*MMReg:0x10C*			*2-356*
CONFIG_XSTRAP	*IOReg:0xE4*	*MMReg:0xE4*		*2-356*
CP_DYN_CNTL	*CLKIND:0xF*			*2-272*
CPLL_CONTROL	*clkconfig:0x44*			*2-138*
CPLL_CONTROL2	*clkconfig:0x98*			*2-140*
CPLL_CONTROL3	*clkconfig:0x70*			*2-140*
CRS_TIMER	*pcieConfigDev[10:2]\:0x90*			*2-87*
CRT00	*VGACRTIND\:0x0*			*2-303*
CRT01	*VGACRTIND\:0x1*			*2-303*
CRT02	*VGACRTIND\:0x2*			*2-303*
CRT03	*VGACRTIND\:0x3*			*2-304*
CRT04	*VGACRTIND\:0x4*			*2-304*
CRT05	*VGACRTIND\:0x5*			*2-304*
CRT06	*VGACRTIND\:0x6*			*2-305*
CRT07	*VGACRTIND\:0x7*			*2-305*
CRT08	*VGACRTIND\:0x8*			*2-306*
CRT09	*VGACRTIND\:0x9*			*2-306*
CRT0A	*VGACRTIND\:0xA*			*2-306*
CRT0B	*VGACRTIND\:0xB*			*2-307*
CRT0C	*VGACRTIND\:0xC*			*2-307*
CRT0D	*VGACRTIND\:0xD*			*2-307*
CRT0E	*VGACRTIND\:0xE*			*2-307*
CRT0F	*VGACRTIND\:0xF*			*2-308*
CRT10	*VGACRTIND\:0x10*			*2-308*
CRT11	*VGACRTIND\:0x11*			*2-308*
CRT12	*VGACRTIND\:0x12*			*2-309*

Table 2-2 All Registers Sorted By Name

Name	Address	Secondary Address	Additional Address	Page
CRT13	*VGACRTIND\:0x13*			*2-309*
CRT14	*VGACRTIND\:0x14*			*2-309*
CRT15	*VGACRTIND\:0x15*			*2-309*
CRT16	*VGACRTIND\:0x16*			*2-310*
CRT17	*VGACRTIND\:0x17*			*2-310*
CRT18	*VGACRTIND\:0x18*			*2-310*
CRT1E	*VGACRTIND\:0x1E*			*2-311*
CRT1F	*VGACRTIND\:0x1F*			*2-311*
CRT22	*VGACRTIND\:0x22*			*2-311*
CRTC8_DATA	*MMReg:0x3B5*	*MMReg:0x3D5*	*VGA_IO:0x3B5 VGA_IO:0x3D5:I O:0x3D5*	*2-303*
CRTC8_IDX	*MMReg:0x3B4*	*MMReg:0x3D4*	*VGA_IO:0x3B4 VGA_IO:0x3D4: O:0x3D4*	*2-303*
CT_DISABLE_BIU	*clkconfig:0x68*			*2-139*
DAC_CNTL	*IOReg:0x58*	*MMReg:0x58*		*2-299*
DAC_DATA	*VGA_IO\:0x3C9*			*2-296*
DAC_MASK	*VGA_IO\:0x3C6*			*2-296*
DAC_R_INDEX	*VGA_IO\:0x3C7*			*2-296*
DAC_W_INDEX	*VGA_IO\:0x3C8*			*2-296*
DELAY_SET_IOC_CCLK	*clkconfig:0x5C*			*2-139*
DEVICE_CAP	*pcieConfigDev[10:2]\:0x5C*			*2-80*
DEVICE_CNTL	*pcieConfigDev[10:2]\:0x60*			*2-81*
DEVICE_ID	*gcconfig:0x2*	*MMReg:0x5002*		*2-110*
DEVICE_STATUS	*pcieConfigDev[10:2]\:0x62*			*2-82*
DFT_CNTL0	*NBMISCIND:0x5*			*2-27*
DFT_CNTL1	*NBMISCIND:0x6*			*2-27*
DFT_CNTL2	*NBMISCIND:0x10*			*2-28*
DFT_SPARE	*NBMISCIND:0x7F*			*2-43*
DFT_VIP_IO_GPIO	*NBMISCIND:0x44*			*2-32*
DFT_VIP_IO_GPIO_OR	*NBMISCIND:0x45*			*2-33*
DLL_CNTL	*CLKIND:0x23*			*2-278*
DYN_BACKBIAS_CNTL	*CLKIND:0x29*			*2-279*
DYN_PWRMGT_SCLK_CNTL	*CLKIND:0xB*			*2-271*
DYN_PWRMGT_SCLK_LENGTH	*CLKIND:0xC*			*2-272*
DYN_SCLK_PWMEN_PIPE	*CLKIND:0xD*			*2-272*
DYN_SCLK_VOL_CNTL	*CLKIND:0xE*			*2-272*
E2_DYN_CNTL	*CLKIND:0x11*			*2-273*
ERROR_STATUS	*CLKIND:0x2C*			*2-280*
F1_ADAPTER_ID	*gcconfig:0x12C*	*MMReg:0x512C*		*2-118*

Table 2-2 All Registers Sorted By Name

Name	Address	Secondary Address	Additional Address	Page
F1_ADAPTER_ID_W	gcconfig:0x14C	MMReg:0x514C:R		2-120
F1_BASE_CODE	gcconfig:0x10B	MMReg:0x510B		2-117
F1_BIST	gcconfig:0x10F	MMReg:0x510F		2-117
F1_CACHE_LINE	gcconfig:0x10C	MMReg:0x510C:R		2-117
F1_CAPABILITIES_PTR	gcconfig:0x134	MMReg:0x5134		2-118
F1_COMMAND	gcconfig:0x104	MMReg:0x5104:R		2-116
F1_DEVICE_ID	gcconfig:0x102	MMReg:0x5102		2-116
F1_HEADER	gcconfig:0x10E	MMReg:0x510E		2-117
F1_INTERRUPT_LINE	gcconfig:0x13C	MMReg:0x513C:R		2-118
F1_INTERRUPT_PIN	gcconfig:0x13D	MMReg:0x513D		2-118
F1_LATENCY	gcconfig:0x10D	MMReg:0x510D:R		2-117
F1_MAX_LATENCY	gcconfig:0x13F	MMReg:0x513F		2-119
F1_MIN_GRANT	gcconfig:0x13E	MMReg:0x513E		2-119
F1_PMI_CAP_ID	gcconfig:0x150	MMReg:0x5150		2-119
F1_PMI_DATA	gcconfig:0x157	MMReg:0x5157		2-119
F1_PMI_NXT_CAP_PTR	gcconfig:0x151	MMReg:0x5151		2-119
F1_PMI_PMC_REG	gcconfig:0x152	MMReg:0x5152		2-119
F1_PMI_STATUS	gcconfig:0x154	MMReg:0x5154:R		2-120
F1_REG_BASE_HI	gcconfig:0x114	MMReg:0x511C:R		2-118
F1_REG_BASE_LO	gcconfig:0x110	MMReg:0x5114:R		2-118
F1_REGPROG_INF	gcconfig:0x109	MMReg:0x5109		2-116
F1_REVISION_ID	gcconfig:0x108	MMReg:0x5108		2-116
F1_STATUS	gcconfig:0x106	MMReg:0x5106		2-116
F1_SUB_CLASS	gcconfig:0x10A	MMReg:0x510A		2-117
F1_VENDOR_ID	gcconfig:0x100	MMReg:0x5100		2-116
F2_ADAPTER_ID	gcconfig:0x22C	MMReg:0x522C		2-123
F2_ADAPTER_ID_W	gcconfig:0x24C	MMReg:0x524C:R		2-124
F2_BASE_CODE	gcconfig:0x20B	MMReg:0x520B		2-122
F2_BIST	gcconfig:0x20F	MMReg:0x520F		2-122
F2_CACHE_LINE	gcconfig:0x20C	MMReg:0x520C:R		2-122
F2_CAPABILITIES_PTR	gcconfig:0x234	MMReg:0x5234		2-123
F2_COMMAND	gcconfig:0x204	MMReg:0x5204:R		2-121
F2_DEVICE_ID	gcconfig:0x202	MMReg:0x5202		2-120
F2_HEADER	gcconfig:0x20E	MMReg:0x520E		2-122
F2_INTERRUPT_LINE	gcconfig:0x23C	MMReg:0x523C:R		2-123
F2_INTERRUPT_PIN	gcconfig:0x23D	MMReg:0x523D		2-123
F2_LATENCY	gcconfig:0x20D	MMReg:0x520D:R		2-122
F2_MAX_LATENCY	gcconfig:0x23F	MMReg:0x523F		2-124
F2_MIN_GRANT	gcconfig:0x23E	MMReg:0x523E		2-123
F2_MSI_CAP_ID	gcconfig:0x260	MMReg:0x5260		2-125
F2_MSI_MSG_ADDR_HI	gcconfig:0x268	MMReg:0x5268:R		2-126

Table 2-2 All Registers Sorted By Name

Name	Address	Secondary Address	Additional Address	Page
F2_MSI_MSG_ADDR_LO	*gcconfig:0x264*	*MMReg:0x5264:R*		*2-126*
F2_MSI_MSG_CNTL	*gcconfig:0x262*	*MMReg:0x5262:R*		*2-126*
F2_MSI_MSG_DATA	*gcconfig:0x26C*	*MMReg:0x526C:R*		*2-126*
F2_MSI_NXT_CAP_PTR	*gcconfig:0x261*	*MMReg:0x5261*		*2-125*
F2_PMI_CAP_ID	*gcconfig:0x250*	*MMReg:0x5250*		*2-124*
F2_PMI_DATA	*gcconfig:0x257*	*MMReg:0x5257*		*2-125*
F2_PMI_NXT_CAP_PTR	*gcconfig:0x251*	*MMReg:0x5251*		*2-124*
F2_PMI_PMC_REG	*gcconfig:0x252*	*MMReg:0x5252*		*2-124*
F2_PMI_STATUS	*gcconfig:0x254*	*MMReg:0x5254:R*		*2-125*
F2_REG_BASE_HI	*gcconfig:0x214*	*MMReg:0x5214:R*		*2-123*
F2_REG_BASE_LO	*gcconfig:0x210*	*MMReg:0x5210:R*		*2-122*
F2_REGPROG_INF	*gcconfig:0x209*	*MMReg:0x5209*		*2-121*
F2_REVISION_ID	*gcconfig:0x208*	*MMReg:0x5208*		*2-121*
F2_STATUS	*gcconfig:0x206*	*MMReg:0x5206*		*2-121*
F2_SUB_CLASS	*gcconfig:0x20A*	*MMReg:0x520A*		*2-121*
F2_VENDOR_ID	*gcconfig:0x200*	*MMReg:0x5200*		*2-120*
FG_DYN_CNTL	*CLKIND:0x17*			*2-275*
FVTHROT_CNTRL_REG	*CLKIND:0x3A*			*2-286*
FVTHROT_COMPARE_BOUND1	*CLKIND:0x3C*			*2-287*
FVTHROT_COMPARE_BOUND2	*CLKIND:0x3D*			*2-287*
FVTHROT_COMPARE_BOUND3	*CLKIND:0x3E*			*2-287*
FVTHROT_COMPARE_BOUND4	*CLKIND:0x3F*			*2-287*
FVTHROT_DOWNTREND_COEF0	*CLKIND:0x45*			*2-288*
FVTHROT_DOWNTREND_COEF1	*CLKIND:0x46*			*2-289*
FVTHROT_DOWNTREND_COEF2	*CLKIND:0x47*			*2-289*
FVTHROT_DOWNTREND_COEF3	*CLKIND:0x48*			*2-289*
FVTHROT_DOWNTREND_COEF4	*CLKIND:0x49*			*2-289*
FVTHROT_FB_DOWNSTEP_REG0	*CLKIND:0x4F*			*2-290*
FVTHROT_FB_DOWNSTEP_REG1	*CLKIND:0x50*			*2-290*
FVTHROT_FB_UPSTEP_REG0	*CLKIND:0x4D*			*2-290*
FVTHROT_FB_UPSTEP_REG1	*CLKIND:0x4E*			*2-290*
FVTHROT_FBDIV_REG0	*CLKIND:0x4A*			*2-289*
FVTHROT_FBDIV_REG1	*CLKIND:0x4B*			*2-289*
FVTHROT_FBDIV_REG2	*CLKIND:0x4C*			*2-290*
FVTHROT_PWM_CTRL_REG0	*CLKIND:0x51*			*2-290*
FVTHROT_PWM_CTRL_REG1	*CLKIND:0x52*			*2-291*
FVTHROT_PWM_DOWNSTEP_REG 0	*CLKIND:0x55*			*2-291*
FVTHROT_PWM_DOWNSTEP_REG 1	*CLKIND:0x56*			*2-291*
FVTHROT_PWM_FEEDBACK_DIV_ REG1	*CLKIND:0x5E*			*2-293*

Table 2-2 All Registers Sorted By Name

Name	Address	Secondary Address	Additional Address	Page
FVTHROT_PWM_FEEDBACK_DIV_REG2	*CLKIND:0x5F*			*2-293*
FVTHROT_PWM_FEEDBACK_DIV_REG3	*CLKIND:0x60*			*2-293*
FVTHROT_PWM_FEEDBACK_DIV_REG4	*CLKIND:0x61*			*2-293*
FVTHROT_PWM_UPSTEP_REG0	*CLKIND:0x53*			*2-291*
FVTHROT_PWM_UPSTEP_REG1	*CLKIND:0x54*			*2-291*
FVTHROT_SCALE_FEEDBACK_DIV_REG1	*CLKIND:0x67*			*2-295*
FVTHROT_SLOW_CLK_FEEDBACK_DIV_REG1	*CLKIND:0x66*			*2-294*
FVTHROT_SPLL_PARAM_FEEDBACK_DIV_REG1	*CLKIND:0x62*			*2-294*
FVTHROT_SPLL_PARAM_FEEDBACK_DIV_REG2	*CLKIND:0x63*			*2-294*
FVTHROT_SPLL_PARAM_FEEDBACK_DIV_REG3	*CLKIND:0x64*			*2-294*
FVTHROT_SPLL_PARAM_FEEDBACK_DIV_REG4	*CLKIND:0x65*			*2-294*
FVTHROT_STATUS_REG0	*CLKIND:0x57*			*2-291*
FVTHROT_STATUS_REG1	*CLKIND:0x58*			*2-292*
FVTHROT_STATUS_REG2	*CLKIND:0x59*			*2-292*
FVTHROT_TARGET_REG	*CLKIND:0x3B*			*2-287*
FVTHROT_UPTREND_COEF0	*CLKIND:0x40*			*2-287*
FVTHROT_UPTREND_COEF1	*CLKIND:0x41*			*2-288*
FVTHROT_UPTREND_COEF2	*CLKIND:0x42*			*2-288*
FVTHROT_UPTREND_COEF3	*CLKIND:0x43*			*2-288*
FVTHROT_UPTREND_COEF4	*CLKIND:0x44*			*2-288*
GA_DYN_CNTL	*CLKIND:0x1B*			*2-274*
GART_BASE	*NBMCIND\:0x2C*			*2-157*
GART_CACHE_CNTRL	*NBMCIND:0x2E*			*2-157*
GART_CACHE_ENTRY_CNTRL	*NBMCIND\:0x2F*			*2-157*
GART_CACHE_SZBASE	*NBMCIND\:0x2D*			*2-157*
GART_ERROR_0	*NBMCIND\:0x30*			*2-158*
GART_ERROR_1	*NBMCIND\:0x31*			*2-158*
GART_ERROR_2	*NBMCIND\:0x32*			*2-158*
GART_ERROR_3	*NBMCIND\:0x33*			*2-158*
GART_ERROR_4	*NBMCIND\:0x34*			*2-159*
GART_ERROR_5	*NBMCIND\:0x35*			*2-159*
GART_ERROR_6	*NBMCIND\:0x36*			*2-159*
GART_ERROR_7	*NBMCIND\:0x37*			*2-159*
GART_FEATURE_ID	*NBMCIND:0x2B*			*2-155*

Table 2-2 All Registers Sorted By Name

Name	Address	Secondary Address	Additional Address	Page
GC_CLK_CNTRL	*clkconfig:0x74*			*2-131*
GENENB	*VGA_IO\:0x3C3*			*2-127*
GENERAL_PWRMGT	*CLKIND:0x8*			*2-270*
GENFC_RD	*VGA_IO\:0x3CA*			*2-297*
GENFC_WT	*VGA_IO\:0x3BA*	*VGA_IO\:0x3DA*		*2-297*
GENMO_RD	*MMReg:0x3CC*	*VGA_IO:0x3CC*		*2-128*
GENMO_RD	*VGA_IO\:0x3CC*			*2-298*
GENMO_WT	*MMReg:0x3C2*	*VGA_IO:0x3C2*		*2-127*
GENMO_WT	*VGA_IO\:0x3C2*			*2-297*
GENS0	*VGA_IO\:0x3C2*			*2-299*
GENS1	*VGA_IO\:0x3BA*	*VGA_IO\:0x3DA*		*2-299*
GPIO_PAD	*NBMISCIND:0x40*			*2-31*
GPIO_PAD_CNTL_PU_PD	*NBMISCIND:0x41*			*2-31*
GPIO_PAD_SCHMEM_OE	*NBMISCIND:0x42*			*2-32*
GPIO_PAD_SP_SN	*NBMISCIND:0x43*			*2-32*
GRA00	*VGAGRPHIND\:0x0*			*2-312*
GRA01	*VGAGRPHIND\:0x1*			*2-312*
GRA02	*VGAGRPHIND\:0x2*			*2-313*
GRA03	*VGAGRPHIND\:0x3*			*2-313*
GRA04	*VGAGRPHIND\:0x4*			*2-313*
GRA05	*VGAGRPHIND\:0x5*			*2-314*
GRA06	*VGAGRPHIND\:0x6*			*2-314*
GRA07	*VGAGRPHIND\:0x7*			*2-315*
GRA08	*VGAGRPHIND\:0x8*			*2-315*
GRPH8_DATA	*MMReg:0x3CF*	*VGA_IO:0x3CF*		*2-312*
GRPH8_IDX	*MMReg:0x3CE*	*VGA_IO:0x3CE*		*2-312*
HD_BACKPORCH_DUR	*MMReg:0x5FB0*			*2-347*
HD_EMBEDDED_SYNC_CNTL	*MMReg:0x5FA0*			*2-346*
HD_INCR	*MMReg:0x5FA4*			*2-346*
HD_POS_SYNC_LEVEL	*MMReg:0x5FAC*			*2-347*
HD_SERATION_DUR	*MMReg:0x5FB4*			*2-347*
HD_TRILEVEL_DUR	*MMReg:0x5FA8*			*2-346*
HDP_DYN_CNTL	*CLKIND:0x10*			*2-273*
HDP_FB_LOCATION	*MMReg:0x134*			*2-357*
HEADER	*gcconfig:0xE*	*MMReg:0x500E*		*2-113*
HTIU_CNTL_1	*HTIUNBIND:0x0*			*2-43*
HTIU_CNTL_2	*HTIUNBIND:0x1*			*2-43*
HTIU_DEBUG	*HTIUNBIND:0x5*			*2-46*
HTIU_DOWNSTREAM_CONFIG	*HTIUNBIND:0x6*			*2-46*
HTIU_NB_DATA	*nbconfig:0xAC*			*2-26*
HTIU_NB_INDEX	*nbconfig:0xA8*			*2-26*

Table 2-2 All Registers Sorted By Name

Name	Address	Secondary Address	Additional Address	Page
HTIU_PERF_CNTL	HTIUNBIND:0x2			2-43
HTIU_PERF_COUNT_0	HTIUNBIND:0x3			2-45
HTIU_PERF_COUNT_1	HTIUNBIND:0x4			2-45
HTIU_UPSTREAM_CONFIG_0	HTIUNBIND:0x7			2-47
HTIU_UPSTREAM_CONFIG_1	HTIUNBIND:0x8			2-48
HTIU_UPSTREAM_CONFIG_10	HTIUNBIND:0x11			2-52
HTIU_UPSTREAM_CONFIG_11	HTIUNBIND:0x12			2-52
HTIU_UPSTREAM_CONFIG_12	HTIUNBIND:0x13			2-52
HTIU_UPSTREAM_CONFIG_13	HTIUNBIND:0x14			2-53
HTIU_UPSTREAM_CONFIG_14	HTIUNBIND:0x15			2-53
HTIU_UPSTREAM_CONFIG_15	HTIUNBIND:0x16			2-54
HTIU_UPSTREAM_CONFIG_16	HTIUNBIND:0x17			2-54
HTIU_UPSTREAM_CONFIG_17	HTIUNBIND:0x18			2-54
HTIU_UPSTREAM_CONFIG_18	HTIUNBIND:0x19			2-55
HTIU_UPSTREAM_CONFIG_19	HTIUNBIND:0x1A			2-55
HTIU_UPSTREAM_CONFIG_2	HTIUNBIND:0x9			2-48
HTIU_UPSTREAM_CONFIG_20	HTIUNBIND:0x1B			2-56
HTIU_UPSTREAM_CONFIG_21	HTIUNBIND:0x1C			2-56
HTIU_UPSTREAM_CONFIG_22	HTIUNBIND:0x1D			2-56
HTIU_UPSTREAM_CONFIG_23	HTIUNBIND:0x1E			2-56
HTIU_UPSTREAM_CONFIG_24	HTIUNBIND:0x1F			2-56
HTIU_UPSTREAM_CONFIG_3	HTIUNBIND:0xA			2-49
HTIU_UPSTREAM_CONFIG_4	HTIUNBIND:0xB			2-49
HTIU_UPSTREAM_CONFIG_5	HTIUNBIND:0xC			2-50
HTIU_UPSTREAM_CONFIG_6	HTIUNBIND:0xD			2-50
HTIU_UPSTREAM_CONFIG_7	HTIUNBIND:0xE			2-51
HTIU_UPSTREAM_CONFIG_8	HTIUNBIND:0xF			2-51
HTIU_UPSTREAM_CONFIG_9	HTIUNBIND:0x10			2-51
INTERRUPT_LINE	gcconfig:0x3C	MMReg:0x503C:R		2-113
INTERRUPT_PIN	gcconfig:0x3D	MMReg:0x503D		2-113
IO_BASE	gcconfig:0x20	MMReg:0x5020:R		2-111
IO_BASE_LIMIT	pcieConfigDev[10:2]\:0x1C			2-76
IO_BASE_LIMIT_HI	pcieConfigDev[10:2]\:0x30			2-77
IOC_CNTL	pcieConfigDev[10:2]\:0x94			2-88
IOC_DMA_ARBITER	NBMISCIND\:0x9			2-10
IOC_LAT_PERF_CNTR_CNTL	NBMISCIND:0x30			2-29
IOC_LAT_PERF_CNTR_OUT	NBMISCIND:0x31			2-29
IOC_P2P_CNTL	NBMISCIND:0xC			2-11
IOC_PCIE_CNTL	NBMISCIND:0xB			2-10
IOC_PCIE_CSR_Count	NBMISCIND\:0xA			2-10
IOC_PCIE_D2_CNTL	NBMISCIND:0x51			2-34

Table 2-2 All Registers Sorted By Name

Name	Address	Secondary Address	Additional Address	Page
IOC_PCIE_D2_CSR_Count	NBMISCIND:0x50			2-34
IOC_PCIE_D3_CNTL	NBMISCIND:0x53			2-35
IOC_PCIE_D3_CSR_Count	NBMISCIND:0x52			2-34
IOC_PCIE_D4_CNTL	NBMISCIND:0x55			2-35
IOC_PCIE_D4_CSR_Count	NBMISCIND:0x54			2-35
IOC_PCIE_D5_CNTL	NBMISCIND:0x57			2-36
IOC_PCIE_D5_CSR_Count	NBMISCIND:0x56			2-35
IOC_PCIE_D6_CNTL	NBMISCIND:0x59			2-36
IOC_PCIE_D6_CSR_Count	NBMISCIND:0x58			2-36
IOC_PCIE_D7_CNTL	NBMISCIND:0x5B			2-37
IOC_PCIE_D7_CSR_Count	NBMISCIND:0x5A			2-37
IOCIsocMapAddr_HI	NBMISCIND:0xF			2-28
IOCIsocMapAddr_LO	NBMISCIND:0xE			2-27
IRQ_BRIDGE_CNTL	pcieConfigDev[10:2]\:0x3E			2-78
K8_DRAM_BANK_ADDR_MAPPING	NBMCIND\:0x73			2-167
K8_DRAM_CS0_BASE	NBMCIND:0x63			2-162
K8_DRAM_CS0_MASK	NBMCIND:0x6B			2-165
K8_DRAM_CS1_BASE	NBMCIND:0x64			2-163
K8_DRAM_CS1_MASK	NBMCIND:0x6C			2-165
K8_DRAM_CS2_BASE	NBMCIND:0x65			2-163
K8_DRAM_CS2_MASK	NBMCIND:0x6D			2-165
K8_DRAM_CS3_BASE	NBMCIND:0x66			2-163
K8_DRAM_CS3_MASK	NBMCIND:0x6E			2-166
K8_DRAM_CS4_BASE	NBMCIND:0x67			2-164
K8_DRAM_CS4_MASK	NBMCIND:0x6F			2-166
K8_DRAM_CS5_BASE	NBMCIND:0x68			2-164
K8_DRAM_CS5_MASK	NBMCIND:0x70			2-166
K8_DRAM_CS6_BASE	NBMCIND:0x69			2-164
K8_DRAM_CS6_MASK	NBMCIND\:0x71			2-166
K8_DRAM_CS7_BASE	NBMCIND:0x6A			2-165
K8_DRAM_CS7_MASK	NBMCIND\:0x72			2-167
K8_FB_LOCATION	NBMCIND\:0x1E			2-154
LATENCY	gcconfig:0xD	MMReg:0x500D:R		2-113
LINK_CAP	pcieConfigDev[10:2]\:0x64			2-82
LINK_CNTL	pcieConfigDev[10:2]\:0x68			2-83
LINK_STATUS	pcieConfigDev[10:2]\:0x6A			2-83
LVTMA_2ND_CRC_RESULT	MMReg:0x7ABC			2-349
LVTMA_CRC_CNTL	MMReg:0x7AB0			2-348
LVTMA_CRC_SIG_MASK	MMReg:0x7AB4			2-348
LVTMA_CRC_SIG_RGB	MMReg:0x7AB8			2-349
MAX_LATENCY	gcconfig:0x3F	MMReg:0x503F		2-113

Table 2-2 All Registers Sorted By Name

Name	Address	Secondary Address	Additional Address	Page
MC_ARB_CNTL	NBMCIND:0x107			2-260
MC_AZ_DEFAULT_ADDR	NBMCIND:0x99			2-195
MC_BIST_CNTL0	NBMCIND:0x111			2-262
MC_BIST_CNTL1	NBMCIND:0x112			2-262
MC_BIST_MISMATCH_H	NBMCIND:0x114			2-263
MC_BIST_MISMATCH_L	NBMCIND:0x113			2-263
MC_BIST_PATTERN0H	NBMCIND:0x116			2-263
MC_BIST_PATTERN0L	NBMCIND:0x115			2-263
MC_BIST_PATTERN1H	NBMCIND:0x118			2-264
MC_BIST_PATTERN1L	NBMCIND:0x117			2-264
MC_BIST_PATTERN2H	NBMCIND:0x11A			2-264
MC_BIST_PATTERN2L	NBMCIND:0x119			2-264
MC_BIST_PATTERN3H	NBMCIND:0x11C			2-264
MC_BIST_PATTERN3L	NBMCIND:0x11B			2-264
MC_BIST_PATTERN4H	NBMCIND:0x11E			2-265
MC_BIST_PATTERN4L	NBMCIND:0x11D			2-264
MC_BIST_PATTERN5H	NBMCIND:0x120			2-265
MC_BIST_PATTERN5L	NBMCIND:0x11F			2-265
MC_BIST_PATTERN6H	NBMCIND:0x122			2-265
MC_BIST_PATTERN6L	NBMCIND:0x121			2-265
MC_BIST_PATTERN7H	NBMCIND:0x124			2-265
MC_BIST_PATTERN7L	NBMCIND:0x123			2-265
MC_DEBUG_CNTL	NBMCIND:0x108			2-261
MC_GART_ERROR_ADDRESS	NBMCIND\:0x3B			2-161
MC_GART_ERROR_ADDRESS_HI	NBMCIND\:0x3C			2-161
MC_GENERAL_PURPOSE	NBMCIND:0x0			2-153
MC_GUI_DYN_CNTL	CLKIND:0x1D			2-276
MC_HOST_DYN_CNTL	CLKIND:0x1E			2-277
MC_INIT_GFX_LAT_TIMER	NBMCIND:0x105			2-259
MC_INIT_MISC_LAT_TIMER	NBMCIND:0x104			2-258
MC_INIT_WR_LAT_TIMER	NBMCIND:0x106			2-259
MC_INTFC_GENERAL_PURPOSE	NBMCIND:0x91			2-192
MC_INTFC_IMP_CTRL_CNTL	NBMCIND:0x92			2-193
MC_INTFC_IMP_CTRL_REF	NBMCIND:0x93			2-193
MC_LATENCY_COUNT_CNTL	NBMCIND:0x94			2-194
MC_LATENCY_COUNT_EVENT	NBMCIND:0x95			2-194
MC_MCLK_CONTROL	NBMCIND:0x7A			2-172
MC_MISC_CNTL	NBMCIND:0x18			2-153
MC_MISC_CNTL2	NBMCIND:0x4E			2-161
MC_MISC_CNTL3	NBMCIND:0x4F			2-182
MC_MISC_UMA_CNTL	NBMCIND:0x5F			2-162

Table 2-2 All Registers Sorted By Name

Name	Address	Secondary Address	Additional Address	Page
MC_MISC_UMA_CNTL2	NBMCIND\:0x7E			2-173
MC_MPLL_CONTROL	NBMCIND:0x74			2-169
MC_MPLL_CONTROL2	NBMCIND:0x75			2-169
MC_MPLL_CONTROL3	NBMCIND:0x76			2-170
MC_MPLL_DIV_CONTROL	NBMCIND:0x79			2-171
MC_MPLL_FREQ_CONTROL	NBMCIND:0x77			2-170
MC_MPLL_SEQ_CONTROL	NBMCIND:0x78			2-171
MC_PM_CNTL	NBMCIND\:0x26			2-154
MC_RBS_DYN_CNTL	CLKIND:0x26			2-277
MC_SYSTEM_STATUS	NBMCIND:0x90			2-191
MC_UMA_AGP_GRP_CNTL	NBMCIND:0x85			2-179
MC_UMA_AGP_GRP_CNTL	NBMCIND:0x85			2-189
MC_UMA_DUALCH_CNTL	NBMCIND:0x86			2-180
MC_UMA_DUALCH_CNTL	NBMCIND:0x86			2-190
MC_UMA_GRP_CNTL	NBMCIND\:0x7C			2-172
MC_UMA_GRP_TMR	NBMCIND\:0x7D			2-173
MC_UMA_HDR_LAT_INIT	NBMCIND\:0x7B			2-172
MC_UMA_RW_G3DR_GRP_CNTL	NBMCIND:0x83			2-176
MC_UMA_RW_G3DR_GRP_CNTL	NBMCIND:0x83			2-185
MC_UMA_RW_GRP_TMR	NBMCIND:0x82			2-176
MC_UMA_RW_GRP_TMR	NBMCIND:0x82			2-184
MC_UMA_RW_TXR_E2R_GRP_CNTL	NBMCIND:0x84			2-178
MC_UMA_RW_TXR_E2R_GRP_CNTL	NBMCIND:0x84			2-187
MC_UMA_WC_GRP_CNTL	NBMCIND:0x81			2-175
MC_UMA_WC_GRP_CNTL	NBMCIND:0x81			2-183
MC_UMA_WC_GRP_TMR	NBMCIND:0x80			2-174
MC_UMA_WC_GRP_TMR	NBMCIND:0x80			2-182
MCA_CKE_MUX_SELECT	NBMCIND:0xAD			2-206
MCA_DLL_MASTER_0	NBMCIND:0xD8			2-253
MCA_DLL_MASTER_1	NBMCIND:0xD9			2-254
MCA_DLL_SLAVE_RD_0	NBMCIND:0xE0			2-254
MCA_DLL_SLAVE_RD_1	NBMCIND:0xE1			2-254
MCA_DLL_SLAVE_WR_0	NBMCIND:0xE8			2-254
MCA_DLL_SLAVE_WR_1	NBMCIND:0xE9			2-255
MCA_DQ_DQS_READ_BACK	NBMCIND:0xC6			2-235
MCA_DQS_CLK_READ_BACK	NBMCIND:0xC7			2-235
MCA_DRIVING	NBMCIND:0xB4			2-216
MCA_GENERAL_PURPOSE	NBMCIND:0xC3			2-233
MCA_GENERAL_PURPOSE_2	NBMCIND:0xC4			2-234

Table 2-2 All Registers Sorted By Name

Name	Address	Secondary Address	Additional Address	Page
MCA_IN_TIMING_DQS_3210	NBMCIND:0xB2			2-212
MCA_IN_TIMING_DQS_3210_PM	NBMCIND:0xD0			2-244
MCA_IN_TIMING_DQS_7654	NBMCIND:0xB3			2-214
MCA_IN_TIMING_DQS_7654_PM	NBMCIND:0xD1			2-246
MCA_MEMORY_INIT_EMRS	NBMCIND:0xA1			2-196
MCA_MEMORY_INIT_EMRS_PM	NBMCIND:0xC9			2-237
MCA_MEMORY_INIT_EMRS2	NBMCIND:0xA2			2-196
MCA_MEMORY_INIT_EMRS2_PM	NBMCIND:0xCA			2-238
MCA_MEMORY_INIT_EMRS3	NBMCIND:0xA3			2-197
MCA_MEMORY_INIT_EMRS3_PM	NBMCIND:0xCB			2-239
MCA_MEMORY_INIT_MRS	NBMCIND:0xA0			2-195
MCA_MEMORY_INIT_MRS_PM	NBMCIND:0xC8			2-237
MCA_MEMORY_INIT_SEQUENCE_1	NBMCIND:0xA4			2-198
MCA_MEMORY_INIT_SEQUENCE_2	NBMCIND:0xA5			2-199
MCA_MEMORY_INIT_SEQUENCE_3	NBMCIND:0xA6			2-200
MCA_MEMORY_INIT_SEQUENCE_4	NBMCIND:0xA7			2-201
MCA_MEMORY_TYPE	NBMCIND:0xAC			2-206
MCA_MISCELLANEOUS	NBMCIND:0xD4			2-251
MCA_MISCELLANEOUS_2	NBMCIND:0xD5			2-251
MCA_MX1X2X_DQ	NBMCIND:0xD6			2-252
MCA_MX1X2X_DQS	NBMCIND:0xD7			2-253
MCA_OCD_CONTROL	NBMCIND:0xC5			2-234
MCA_ODT_MUX_SELECT	NBMCIND:0xAE			2-207
MCA_OUT_TIMING	NBMCIND:0xB5			2-217
MCA_OUT_TIMING_DQ	NBMCIND:0xB6			2-219
MCA_OUT_TIMING_DQ_PM	NBMCIND:0xD2			2-248
MCA_OUT_TIMING_DQS	NBMCIND:0xB7			2-221
MCA_OUT_TIMING_DQS_PM	NBMCIND:0xD3			2-250
MCA_PREAMP	NBMCIND:0xBD			2-226
MCA_PREAMP_N	NBMCIND:0xBE			2-229
MCA_PREAMP_P	NBMCIND:0xBF			2-230
MCA_PREAMP_STEP	NBMCIND:0xC0			2-230
MCA_PREBUF_SLEW_N	NBMCIND:0xC1			2-232
MCA_PREBUF_SLEW_P	NBMCIND:0xC2			2-233
MCA_RECEIVING	NBMCIND:0xB1			2-211
MCA_RESERVED_0	NBMCIND:0xF0			2-255
MCA_RESERVED_1	NBMCIND:0xF1			2-255
MCA_RESERVED_2	NBMCIND:0xF2			2-255

Table 2-2 All Registers Sorted By Name

Name	Address	Secondary Address	Additional Address	Page
MCA_RESERVED_3	*NBMCIND:0xF3*			*2-255*
MCA_RESERVED_4	*NBMCIND:0xF4*			*2-255*
MCA_RESERVED_5	*NBMCIND:0xF5*			*2-256*
MCA_RESERVED_6	*NBMCIND:0xF6*			*2-256*
MCA_RESERVED_7	*NBMCIND:0xF7*			*2-256*
MCA_RESERVED_8	*NBMCIND:0xF8*			*2-256*
MCA_RESERVED_9	*NBMCIND:0xF9*			*2-256*
MCA_RESERVED_A	*NBMCIND:0xFA*			*2-256*
MCA_RESERVED_B	*NBMCIND:0xFB*			*2-256*
MCA_RESERVED_C	*NBMCIND:0xFC*			*2-257*
MCA_RESERVED_D	*NBMCIND:0xFD*			*2-257*
MCA_RESERVED_E	*NBMCIND:0xFE*			*2-257*
MCA_RESERVED_F	*NBMCIND:0xFF*			*2-257*
MCA_SEQ_CONTROL	*NBMCIND:0xB0*			*2-209*
MCA_SEQ_PERF_CNTL	*NBMCIND:0xAF*			*2-208*
MCA_STRENGTH_N	*NBMCIND:0xB8*			*2-222*
MCA_STRENGTH_P	*NBMCIND:0xB9*			*2-223*
MCA_STRENGTH_READ_BACK_N	*NBMCIND:0xBB*			*2-225*
MCA_STRENGTH_READ_BACK_P	*NBMCIND:0xBC*			*2-226*
MCA_STRENGTH_STEP	*NBMCIND:0xBA*			*2-223*
MCA_TIMING_PARAMETERS_1	*NBMCIND:0xA8*			*2-202*
MCA_TIMING_PARAMETERS_1_P M	*NBMCIND:0xCC*			*2-239*
MCA_TIMING_PARAMETERS_2	*NBMCIND:0xA9*			*2-203*
MCA_TIMING_PARAMETERS_2_P M	*NBMCIND:0xCD*			*2-241*
MCA_TIMING_PARAMETERS_3	*NBMCIND:0xAA*			*2-204*
MCA_TIMING_PARAMETERS_3_P M	*NBMCIND:0xCE*			*2-242*
MCA_TIMING_PARAMETERS_4	*NBMCIND:0xAB*			*2-205*
MCA_TIMING_PARAMETERS_4_P M	*NBMCIND:0xCF*			*2-243*
MCCFG_AGP_BASE	*NBMCIND:0x102*			*2-258*
MCCFG_AGP_BASE_2	*NBMCIND:0x103*			*2-258*
MCCFG_AGP_LOCATION	*NBMCIND:0x101*			*2-257*
MCCFG_FB_LOCATION	*NBMCIND:0x100*			*2-257*
MCLK_MISC	*CLKIND:0x22*			*2-278*
MCLK_PWRMGT_CNTL	*CLKIND:0xA*			*2-271*
MCS_PERF_CNTL	*NBMCIND:0x98*			*2-195*
MCS_PERF_COUNT0	*NBMCIND:0x96*			*2-194*
MCS_PERF_COUNT1	*NBMCIND:0x97*			*2-194*
MEDIA_0_SCRATCH	*IOReg:0xB0*	*MMReg:0xB0*		*2-354*

Table 2-2 All Registers Sorted By Name

Name	Address	Secondary Address	Additional Address	Page
MEDIA_1_SCRATCH	IOReg:0xB4	MMReg:0xB4		2-354
MEM_BASE_HI	gcconfig:0x14	MMReg:0x5014:R		2-114
MEM_BASE_LIMIT	pcieConfigDev[10:2]\:0x20			2-77
MEM_BASE_LO	gcconfig:0x10	MMReg:0x5010:R		2-114
MIN_GRANT	gcconfig:0x3E	MMReg:0x503E		2-114
MM_DATA	IOReg:0x4	MMReg:0x4		2-127
MM_INDEX	IOReg:0x0	MMReg:0x0		2-127
MPLL_BYPASSCLK_SEL	CLKIND:0x5			2-269
MPLL_CLK_SEL	CLKIND:0x7			2-270
MPLL_CNTL_MODE	CLKIND:0x6			2-269
MPLL_FUNC_CNTL	CLKIND:0x4			2-269
MPLL_TIME	CLKIND:0x25			2-279
MSI_CAP_ID	gcconfig:0x80	MMReg:0x5080		2-115
MSI_CAP_LIST	pcieConfigDev[10:2]\:0x80			2-86
MSI_CAP_LIST	pcieConfigDev[10:2]\:0x80			2-107
MSI_MAP	pcieConfigDev[10:2]\:0xB8			2-88
MSI_MSG_ADDR_HI	gcconfig:0x88	MMReg:0x5088:R		2-115
MSI_MSG_ADDR_LO	gcconfig:0x84	MMReg:0x5084:R		2-115
MSI_MSG_CNTL	gcconfig:0x82	MMReg:0x5082:R		2-115
MSI_MSG_DATA	gcconfig:0x8C	MMReg:0x508C:R		2-116
MSI_NXT_CAP_PTR	gcconfig:0x81	MMReg:0x5081		2-115
NB_ADAPTER_ID	nbconfig:0x2C			2-5
NB_ADAPTER_ID_W	nbconfig\:0x50			2-7
NB_AGP_ADDRESS_SPACE_SIZE	nbconfig\:0xF8			2-23
NB_AGP_MODE_CONTROL	nbconfig\:0xFC			2-24
NB_APIC_P2P_CNTL	NBMISCIND:0x3D			2-30
NB_APIC_P2P_RANGE_0	NBMISCIND:0x3E			2-30
NB_APIC_P2P_RANGE_1	NBMISCIND:0x3F			2-30
NB_BAR1_RCRB	nbconfig:0x14			2-26
NB_BAR2_PM2	nbconfig:0x18			2-4
NB_BAR3_PCIEXP_MMCFG	nbconfig:0x1C			2-5
NB_BAR3_UPPER_PCIEXP_MMCFG	nbconfig\:0x20			2-5
NB_BASE_CODE	nbconfig\:0xB			2-3
NB_BIST	nbconfig\:0xF			2-4
NB_BROADCAST_BASE_HI	NBMISCIND:0x3B			2-29
NB_BROADCAST_BASE_LO	NBMISCIND:0x3A			2-29
NB_BROADCAST_CNTL	NBMISCIND:0x3C			2-30
NB_CACHE_LINE	nbconfig:0xC			2-3
NB_CAPABILITIES_PTR	nbconfig:0x34			2-5
NB_CFG_Q_F1000_800	nbconfig:0x9C			2-25

Table 2-2 All Registers Sorted By Name

Name	Address	Secondary Address	Additional Address	Page
NB_CNTL	*NBMISCIND\:0x0*			*2-8*
NB_COMMAND	*nbconfig:0x4*			*2-1*
NB_DEVICE_ID	*nbconfig:0x2*			*2-1*
NB_ECC_CTRL	*nbconfig:0x48*			*2-26*
NB_EXSMRAM	*nbconfig:0x6A*			*2-15*
NB_FDHC	*nbconfig\:0x68*			*2-14*
NB_GC_STRAPS	*nbconfig:0x8C*			*2-22*
NB_HEADER	*nbconfig:0xE*			*2-4*
NB_HT_CLK_CNTL_RECEIVER_CO MP_CNTL	*nbconfig:0x80*			*2-17*
NB_HT_LINK_COMMAND	*nbconfig:0xC4*			*2-18*
NB_HT_LINK_CONF_CNTL	*nbconfig:0xC8*			*2-18*
NB_HT_LINK_END	*nbconfig:0xCC*			*2-19*
NB_HT_LINK_FREQ_CAP_A	*nbconfig:0xD0*			*2-19*
NB_HT_LINK_FREQ_CAP_B	*nbconfig:0xD4*			*2-20*
NB_HT_MEMORY_BASE_UPPER	*nbconfig:0xDC*			*2-20*
NB_HT_TRANS_COMP_CNTL	*nbconfig:0x94*			*2-17*
NB_HTIU_CFG	*HTIUNBIND:0x32*			*2-57*
NB_INTERRUPT_PIN	*NBMISCIND:0x1F*			*2-28*
NB_IOC_CFG_CNTL	*nbconfig:0x7C*			*2-34*
NB_IOC_DEBUG	*NBMISCIND:0x1*			*2-27*
NB_LATENCY	*nbconfig\:0xD*			*2-4*
NB_LOWER_TOP_OF_DRAM2	*HTIUNBIND:0x30*			*2-57*
NB_MC_DATA	*nbconfig\:0xEC*			*2-25*
NB_MC_DEBUG	*NBMCIND:0x1F*			*2-154*
NB_MC_IND_DATA	*nbconfig:0x74*			*2-33*
NB_MC_IND_INDEX	*nbconfig:0x70*			*2-33*
NB_MC_INDEX	*nbconfig\:0xE8*			*2-24*
NB_MEM_CH_CNTL0	*NBMCIND:0x1C*			*2-181*
NB_MEM_CH_CNTL1	*NBMCIND:0x1D*			*2-182*
NB_MEM_CH_CNTL2	*NBMCIND:0x1B*			*2-181*
NB_MISC_DATA	*nbconfig\:0x64*			*2-7*
NB_MISC_INDEX	*nbconfig\:0x60*			*2-7*
NB_MMIOBASE	*NBMISCIND:0x17*			*2-28*
NB_MMIOLIMIT	*NBMISCIND:0x18*			*2-28*
NB_PCI_ARB	*nbconfig:0x84*			*2-20*
NB_PCI_CTRL	*nbconfig:0x4C*			*2-6*
NB_PCIE_INDX_ADDR	*nbconfig\:0xE0*			*2-24*
NB_PCIE_INDX_DATA	*nbconfig\:0xE4*			*2-24*
NB_PMCR	*nbconfig\:0x6B*			*2-15*
NB_PROG_DEVICE_REMAP_0	*NBMISCIND:0x20*			*2-29*

Table 2-2 All Registers Sorted By Name

Name	Address	Secondary Address	Additional Address	Page
NB_REGPROG_INF	nbconfig\:0x9			2-3
NB_REVISION_ID	nbconfig:0x8			2-3
NB_SMRAM	nbconfig:0x69			2-14
NB_SPARE1	NBMISCIND\:0x2			2-8
NB_STATUS	nbconfig:0x6			2-2
NB_STRAP_READ_BACK	nbconfig:0x6C			2-15
NB_STRAPS_READBACK_DATA	NBMISCIND\:0x4			2-9
NB_STRAPS_READBACK_MUX	NBMISCIND\:0x3			2-9
NB_SUB_CLASS	nbconfig\:0xA			2-3
NB_TOM_PCI	NBMISCIND:0x16			2-28
NB_TOP_OF_DRAM_SLOT1	nbconfig:0x90			2-22
NB_UPPER_TOP_OF_DRAM2	HTIUNBIND:0x31			2-57
NB_VENDOR_ID	nbconfig\:0x0			2-1
OSC_CONTROL	clkconfig:0x40			2-130
OVERCLOCK_CNTL	CLKIND:0x2B			2-279
PCIE_ADV_ERR_CAP_CNTL	pcieConfigDev[10:2]\:0x158			2-91
PCIE_B_P90_CNTL	PCIEIND:0xF9			2-103
PCIE_BASE_CODE	pcieConfigDev[10:2]\:0xB			2-74
PCIE_BIST	pcieConfigDev[10:2]\:0xF			2-75
PCIE_BUS_CNTL	PCIEIND\:0x21			2-59
PCIE_CACHE_LINE	pcieConfigDev[10:2]\:0xC			2-74
PCIE_CAP	pcieConfigDev[10:2]\:0x5A			2-80
PCIE_CAP_LIST	pcieConfigDev[10:2]\:0x58			2-80
PCIE_CFG_SCRATCH	pcieConfigDev[10:2]\:0xC0			2-107
PCIE_CI_CNTL	PCIEIND:0x20			2-59
PCIE_CNTL	PCIEIND:0x10			2-58
PCIE_COMMAND	pcieConfigDev[10:2]\:0x4			2-73
PCIE_CONFIG_CNTL	PCIEIND\:0x11			2-58
PCIE_CORR_ERR_MASK	pcieConfigDev[10:2]\:0x154			2-91
PCIE_CORR_ERR_STATUS	pcieConfigDev[10:2]\:0x150			2-90
PCIE_DEBUG_CNTL	PCIEIND:0x12			2-94
PCIE_DEVICE_ID	pcieConfigDev[10:2]\:0x2			2-73
PCIE_ENH_ADV_ERR_RPT_CAP_HDR	pcieConfigDev[10:2]\:0x140			2-89
PCIE_ERR_CNTL	PCIEIND_P\:0x6A			2-68
PCIE_ERR_SRC_ID	pcieConfigDev[10:2]\:0x174			2-93
PCIE_FC_CPL	PCIEIND_P\:0x62			2-68
PCIE_FC_NP	PCIEIND_P\:0x61			2-68
PCIE_FC_P	PCIEIND_P\:0x60			2-68
PCIE_HDR_LOG0	pcieConfigDev[10:2]\:0x15C			2-91
PCIE_HDR_LOG1	pcieConfigDev[10:2]\:0x160			2-91

Table 2-2 All Registers Sorted By Name

Name	Address	Secondary Address	Additional Address	Page
PCIE_HDR_LOG2	*pcieConfigDev[10:2]\:0x164*			*2-92*
PCIE_HDR_LOG3	*pcieConfigDev[10:2]\:0x168*			*2-92*
PCIE_HEADER	*pcieConfigDev[10:2]\:0xE*			*2-75*
PCIE_INTERRUPT_LINE	*pcieConfigDev[10:2]\:0x3C*			*2-78*
PCIE_INTERRUPT_PIN	*pcieConfigDev[10:2]\:0x3D*			*2-78*
PCIE_LATENCY	*pcieConfigDev[10:2]\:0xD*			*2-75*
PCIE_LC_CNTL	*PCIEIND_P:0xA0*			*2-69*
PCIE_LC_LINK_WIDTH_CNTL	*PCIEIND_P\:0xA2*			*2-72*
PCIE_LC_N_FTS_CNTL	*PCIEIND_P:0xA3*			*2-72*
PCIE_LC_N_FTS_CNTL	*PCIEIND_P:0xA3*			*2-106*
PCIE_LC_STATE0	*PCIEIND_P\:0xA5*			*2-71*
PCIE_LC_STATE1	*PCIEIND_P\:0xA6*			*2-71*
PCIE_LC_STATE2	*PCIEIND_P\:0xA7*			*2-71*
PCIE_LC_STATE3	*PCIEIND_P\:0xA8*			*2-71*
PCIE_LC_STATE4	*PCIEIND_P\:0xA9*			*2-71*
PCIE_LC_STATE5	*PCIEIND_P\:0xAA*			*2-71*
PCIE_LC_TRAINING_CNTL	*PCIEIND_P:0xA1*			*2-72*
PCIE_LINK_CFG	*NBMISCIND:0x8*			*2-9*
PCIE_MSI_MSG_ADDR_HI	*pcieConfigDev[10:2]\:0x88*			*2-87*
PCIE_MSI_MSG_ADDR_LO	*pcieConfigDev[10:2]\:0x84*			*2-87*
PCIE_MSI_MSG_CNTL	*pcieConfigDev[10:2]\:0x82*			*2-86*
PCIE_MSI_MSG_DATA	*pcieConfigDev[10:2]\:0x88*			*2-87*
PCIE_MSI_MSG_DATA_64	*pcieConfigDev[10:2]\:0x8C*			*2-87*
PCIE_NBCFG_REG0	*NBMISCIND:0x32*			*2-11*
PCIE_NBCFG_REG3	*NBMISCIND:0x33*			*2-12*
PCIE_NBCFG_REG4	*NBMISCIND:0x34*			*2-12*
PCIE_NBCFG_REG5	*NBMISCIND:0x35*			*2-13*
PCIE_NBCFG_REG6	*NBMISCIND:0x36*			*2-13*
PCIE_NBCFG_REG7	*NBMISCIND:0x37*			*2-13*
PCIE_NBCFG_REG8	*NBMISCIND:0x38*			*2-14*
PCIE_P_BUF_STATUS	*PCIEIND\:0x41*			*2-61*
PCIE_P_CNTL	*PCIEIND:0x40*			*2-60*
PCIE_P_DECODER_STATUS	*PCIEIND\:0x42*			*2-62*
PCIE_P_IMP_CNTL_STRENGTH	*PCIEIND\:0x60*			*2-63*
PCIE_P_IMP_CNTL_UPDATE	*PCIEIND\:0x61*			*2-64*
PCIE_P_PAD_FORCE_DIS	*PCIEIND\:0x65*			*2-65*
PCIE_P_PAD_FORCE_EN	*PCIEIND\:0x64*			*2-64*
PCIE_P_PAD_MISC_CNTL	*PCIEIND\:0x63*			*2-64*
PCIE_P_PLL_CNTL	*PCIEIND\:0x44*			*2-63*
PCIE_P_PORT_LANE_STATUS	*PCIEIND_P\:0x50*			*2-68*
PCIE_P_STR_CNTL_UPDATE	*PCIEIND\:0x62*			*2-64*

Table 2-2 All Registers Sorted By Name

Name	Address	Secondary Address	Additional Address	Page
PCIE_P90_BRX_PRBS_ER	PCIEIND:0xF7			2-103
PCIE_P90RX_PRBS_CLR	PCIEIND:0xF6			2-102
PCIE_P90TX_PRBS_EN	PCIEIND:0xF8			2-103
PCIE_PDNB_CNTL	NBMISCIND:0x7			2-25
PCIE_PERF_LATENCY_CNTL	PCIEIND:0x70			2-95
PCIE_PERF_LATENCY_COUNTER0	PCIEIND:0x77			2-97
PCIE_PERF_LATENCY_COUNTER1	PCIEIND:0x78			2-97
PCIE_PERF_LATENCY_MAX	PCIEIND:0x74			2-96
PCIE_PERF_LATENCY_REQ_ID	PCIEIND:0x71			2-96
PCIE_PERF_LATENCY_TAG	PCIEIND:0x72			2-96
PCIE_PERF_LATENCY_THRESHOLD	PCIEIND:0x73			2-96
PCIE_PERF_LATENCY_TIMER_HI	PCIEIND:0x76			2-97
PCIE_PERF_LATENCY_TIMER_LO	PCIEIND:0x75			2-96
PCIE_PORT_DATA	pcieConfigDev[10:2]\:0xE4			2-89
PCIE_PORT_INDEX	pcieConfigDev[10:2]\:0xE0			2-89
PCIE_PORT_VC_CAP_REG1	pcieConfigDev[10:2]\:0x104			2-108
PCIE_PORT_VC_CAP_REG2	pcieConfigDev[10:2]\:0x108			2-108
PCIE_PORT_VC_CNTL	pcieConfigDev[10:2]\:0x10C			2-108
PCIE_PORT_VC_STATUS	pcieConfigDev[10:2]\:0x10E			2-109
PCIE_PRBS23_BITCNT_0	PCIEIND:0xD0			2-97
PCIE_PRBS23_BITCNT_1	PCIEIND:0xD1			2-97
PCIE_PRBS23_BITCNT_10	PCIEIND:0xDA			2-98
PCIE_PRBS23_BITCNT_11	PCIEIND:0xDB			2-99
PCIE_PRBS23_BITCNT_12	PCIEIND:0xDC			2-99
PCIE_PRBS23_BITCNT_13	PCIEIND:0xDD			2-99
PCIE_PRBS23_BITCNT_14	PCIEIND:0xDE			2-99
PCIE_PRBS23_BITCNT_15	PCIEIND:0xDF			2-99
PCIE_PRBS23_BITCNT_2	PCIEIND:0xD2			2-97
PCIE_PRBS23_BITCNT_3	PCIEIND:0xD3			2-97
PCIE_PRBS23_BITCNT_4	PCIEIND:0xD4			2-98
PCIE_PRBS23_BITCNT_5	PCIEIND:0xD5			2-98
PCIE_PRBS23_BITCNT_6	PCIEIND:0xD6			2-98
PCIE_PRBS23_BITCNT_7	PCIEIND:0xD7			2-98
PCIE_PRBS23_BITCNT_8	PCIEIND:0xD8			2-98
PCIE_PRBS23_BITCNT_9	PCIEIND:0xD9			2-98
PCIE_PRBS23_CLR	PCIEIND:0xF0			2-102
PCIE_PRBS23_EN	PCIEIND:0xF5			2-102
PCIE_PRBS23_ERRCNT_0	PCIEIND:0xE0			2-99
PCIE_PRBS23_ERRCNT_1	PCIEIND:0xE1			2-99
PCIE_PRBS23_ERRCNT_10	PCIEIND:0xEA			2-101

Table 2-2 All Registers Sorted By Name

Name	Address	Secondary Address	Additional Address	Page
PCIE_PRBS23_ERRCNT_11	*PCIEIND:0xEB*			*2-101*
PCIE_PRBS23_ERRCNT_12	*PCIEIND:0xEC*			*2-101*
PCIE_PRBS23_ERRCNT_13	*PCIEIND:0xED*			*2-101*
PCIE_PRBS23_ERRCNT_14	*PCIEIND:0xEE*			*2-101*
PCIE_PRBS23_ERRCNT_15	*PCIEIND:0xEF*			*2-101*
PCIE_PRBS23_ERRCNT_2	*PCIEIND:0xE2*			*2-100*
PCIE_PRBS23_ERRCNT_3	*PCIEIND:0xE3*			*2-100*
PCIE_PRBS23_ERRCNT_4	*PCIEIND:0xE4*			*2-100*
PCIE_PRBS23_ERRCNT_5	*PCIEIND:0xE5*			*2-100*
PCIE_PRBS23_ERRCNT_6	*PCIEIND:0xE6*			*2-100*
PCIE_PRBS23_ERRCNT_7	*PCIEIND:0xE7*			*2-100*
PCIE_PRBS23_ERRCNT_8	*PCIEIND:0xE8*			*2-100*
PCIE_PRBS23_ERRCNT_9	*PCIEIND:0xE9*			*2-101*
PCIE_PRBS23_ERRSTAT	*PCIEIND:0xF1*			*2-102*
PCIE_PRBS23_FREERUN	*PCIEIND:0xF3*			*2-102*
PCIE_PRBS23_LOCK_CNT	*PCIEIND:0xF4*			*2-102*
PCIE_PRBS23_LOCKED	*PCIEIND:0xF2*			*2-102*
PCIE_REGPROG_INF	*pcieConfigDev[10:2]\:0x9*			*2-74*
PCIE_RESERVED	*PCIEIND\:0x0*			*2-58*
PCIE_REVISION_ID	*pcieConfigDev[10:2]\:0x8*			*2-74*
PCIE_ROOT_ERR_CMD	*pcieConfigDev[10:2]\:0x16C*			*2-92*
PCIE_ROOT_ERR_STATUS	*pcieConfigDev[10:2]\:0x170*			*2-92*
PCIE_RX_CNTL	*PCIEIND_P:0x70*			*2-69*
PCIE_RX_CREDITS_ALLOCATED_CPL	*PCIEIND_P:0x82*			*2-105*
PCIE_RX_CREDITS_ALLOCATED_NP	*PCIEIND_P:0x81*			*2-105*
PCIE_RX_CREDITS_ALLOCATED_P	*PCIEIND_P:0x80*			*2-105*
PCIE_RX_CREDITS_RECEIVED_CPL	*PCIEIND_P:0x85*			*2-106*
PCIE_RX_CREDITS_RECEIVED_NP	*PCIEIND_P:0x84*			*2-106*
PCIE_RX_CREDITS_RECEIVED_P	*PCIEIND_P:0x83*			*2-106*
PCIE_RX_LASTACK_SEQNUM	*PCIEIND_P\:0x84*			*2-69*
PCIE_RX_VENDOR_SPECIFIC	*PCIEIND_P:0x72*			*2-105*
PCIE_SCRATCH	*PCIEIND\:0x1*			*2-58*
PCIE_STATUS	*pcieConfigDev[10:2]\:0x6*			*2-73*
PCIE_STRAP_REG2	*NBMISCIND:0x39*			*2-14*
PCIE_STRAP_REG2	*NBMISCIND:0x39*			*2-29*
PCIE_SUB_CLASS	*pcieConfigDev[10:2]\:0xA*			*2-74*
PCIE_TX_ACK_LATENCY_LIMIT	*PCIEIND_P:0x26*			*2-67*
PCIE_TX_ACK_LATENCY_LIMIT	*PCIEIND_P:0x26*			*2-103*

Table 2-2 All Registers Sorted By Name

Name	Address	Secondary Address	Additional Address	Page
PCIE_TX_CNTL	PCIEIND_P:0x20			2-66
PCIE_TX_CREDITS_CONSUMED_CPL	PCIEIND_P:0x32			2-104
PCIE_TX_CREDITS_CONSUMED_NP	PCIEIND_P:0x31			2-104
PCIE_TX_CREDITS_CONSUMED_P	PCIEIND_P:0x30			2-103
PCIE_TX_CREDITS_LIMIT_CPL	PCIEIND_P:0x35			2-105
PCIE_TX_CREDITS_LIMIT_NP	PCIEIND_P:0x34			2-104
PCIE_TX_CREDITS_LIMIT_P	PCIEIND_P:0x33			2-104
PCIE_TX_REPLAY	PCIEIND_P:0x25			2-67
PCIE_TX_REQUEST_NUM_CNTL	PCIEIND_P:0x23			2-67
PCIE_TX_REQUESTER_ID	PCIEIND_P:0x21			2-66
PCIE_TX_SEQ	PCIEIND_P:0x24			2-67
PCIE_TX_VENDOR_SPECIFIC	PCIEIND_P:0x22			2-67
PCIE_TX_VENDOR_SPECIFIC	PCIEIND_P:0x22			2-103
PCIE_UNCORR_ERR_MASK	pcieConfigDev[10:2]\:0x148			2-90
PCIE_UNCORR_ERR_SEVERITY	pcieConfigDev[10:2]\:0x14C			2-90
PCIE_UNCORR_ERR_STATUS	pcieConfigDev[10:2]\:0x144			2-89
PCIE_VC_ENH_CAP_HDR	pcieConfigDev[10:2]\:0x100			2-108
PCIE_VC0_RESOURCE_CAP	pcieConfigDev[10:2]\:0x110			2-93
PCIE_VC0_RESOURCE_CNTL	pcieConfigDev[10:2]\:0x114			2-94
PCIE_VC0_RESOURCE_STATUS	pcieConfigDev[10:2]\:0x11A			2-94
PCIE_VC1_RESOURCE_CAP	pcieConfigDev[10:2]\:0x11C			2-109
PCIE_VC1_RESOURCE_CNTL	pcieConfigDev[10:2]\:0x120			2-109
PCIE_VC1_RESOURCE_STATUS	pcieConfigDev[10:2]\:0x124			2-109
PCIE_VENDOR_ID	pcieConfigDev[10:2]\:0x0			2-72
PCIE_WPR_CNTL	PCIEIND:0x30			2-95
PCIEP_PORT_CNTL	PCIEIND_P:0x10			2-65
PCIEP_RESERVED	PCIEIND_P\:0x0			2-65
PCIEP_SCRATCH	PCIEIND_P\:0x1			2-65
PLL_TEST_CNTL	CLKIND:0x21			2-267
PMI_CAP	pcieConfigDev[10:2]\:0x52			2-79
PMI_CAP_ID	gcconfig:0x50	MMReg:0x5050		2-129
PMI_CAP_LIST	pcieConfigDev[10:2]\:0x50			2-79
PMI_DATA	gcconfig:0x57	MMReg:0x5057		2-129
PMI_NXT_CAP_PTR	gcconfig:0x51	MMReg:0x5051		2-129
PMI_PMC_REG	gcconfig:0x52	MMReg:0x5052		2-129
PMI_STATUS	gcconfig:0x54	MMReg:0x5054:R		2-120
PMI_STATUS_CNTL	pcieConfigDev[10:2]\:0x54			2-79
POLARITY_CNTL	CLKIND:0x2A			2-279
PREF_BASE_LIMIT	pcieConfigDev[10:2]\:0x24			2-77
PREF_BASE_UPPER	pcieConfigDev[10:2]\:0x28			2-77

Table 2-2 All Registers Sorted By Name

Name	Address	Secondary Address	Additional Address	Page
PREF_LIMIT_UPPER	pcieConfigDev[10:2]\:0x2C			2-77
RCRB_Enhanced_Capability_Header	MMGartReg:0x0			2-266
REG_BASE_HI	gcconfig:0x1C	MMReg:0x501C:R		2-115
REG_BASE_LO	gcconfig:0x18	MMReg:0x5018:R		2-114
REGPROG_INF	gcconfig:0x9	MMReg:0x5009		2-114
REVISION_ID	gcconfig:0x8	MMReg:0x5008		2-111
ROOT_CAP	pcieConfigDev[10:2]\:0x76			2-107
ROOT_CNTL	pcieConfigDev[10:2]\:0x74			2-85
ROOT_CNTL	pcieConfigDev[10:2]\:0x74			2-107
ROOT_STATUS	pcieConfigDev[10:2]\:0x78			2-86
RS_DYN_CNTL	CLKIND:0x19			2-275
SC_DYN_CNTL	CLKIND:0x18			2-275
SCLK_PWRMGT_CNTL	CLKIND:0x9			2-270
scratch_0	NBMISCIND:0x70			2-41
scratch_1	NBMISCIND:0x71			2-41
SCRATCH_1_CLKCFG	clkconfig\:0x78			2-131
SCRATCH_1_NBCFG	nbconfig\:0x54			2-16
scratch_2	NBMISCIND:0x72			2-41
SCRATCH_2_CLKCFG	clkconfig\:0x7C			2-131
SCRATCH_2_NBCFG	nbconfig\:0x98			2-17
scratch_3	NBMISCIND:0x73			2-41
SCRATCH_4	NBMISCIND:0x74			2-41
SCRATCH_5	NBMISCIND:0x75			2-42
SCRATCH_6	NBMISCIND:0x76			2-42
SCRATCH_7	NBMISCIND:0x77			2-42
SCRATCH_8	NBMISCIND:0x78			2-42
SCRATCH_9	NBMISCIND:0x79			2-42
SCRATCH_A	NBMISCIND:0x7A			2-42
SCRATCH_CLKCFG	clkconfig\:0x84			2-132
SCRATCH_NBCFG	nbconfig\:0x78			2-16
SD1_CHROMA_MOD_CNTL	MMReg:0x5EF0			2-341
SD1_CHROMA_OFFSET	MMReg:0x5F90			2-345
SD1_COL_SC_DENOMIN	MMReg:0x5EF4			2-341
SD1_COL_SC_INC	MMReg:0x5EF8			2-342
SD1_COL_SC_INC_CORR	MMReg:0x5EFC			2-342
SD1_COL_SC_PHASE_CNTL	MMReg:0x5FD4			2-345
SD1_CRC_CNTL	MMReg:0x5F1C			2-344
SD1_CRTC_HV_START	MMReg:0x5F98			2-346
SD1_CRTC_TV_FRAMESTART_CNTL	MMReg:0x5F9C			2-346
SD1_FORCE_DAC_DATA	MMReg:0x5ECC			2-340

Table 2-2 All Registers Sorted By Name

Name	Address	Secondary Address	Additional Address	Page
SD1_LUMA_BLANK_SETUP_LEVELS	MMReg:0x5EA8			2-335
SD1_LUMA_COMB_FILT_CNTL1	MMReg:0x5EB8			2-338
SD1_LUMA_COMB_FILT_CNTL2	MMReg:0x5EBC			2-338
SD1_LUMA_COMB_FILT_CNTL3	MMReg:0x5EC0			2-338
SD1_LUMA_COMB_FILT_CNTL4	MMReg:0x5EC4			2-338
SD1_LUMA_FILT_CNTL	MMReg:0x5EB4			2-336
SD1_LUMA_OFFSET_LIMIT	MMReg:0x5F8C			2-345
SD1_LUMA_SYNC_TIP_LEVELS	MMReg:0x5EB0			2-336
SD1_MAIN_CNTL	MMReg:0x5DFC			2-322
SD1_RGB_OR_PBPR_BLANK_LEVEL	MMReg:0x5EAC			2-336
SD1_SCM_COL_SC_DENOMIN	MMReg:0x5F00			2-342
SD1_SCM_COL_SC_INC	MMReg:0x5F04			2-342
SD1_SCM_COL_SC_INC_CORR	MMReg:0x5F08			2-343
SD1_SCM_DB_DR_SCALE_FACTORS	MMReg:0x5F10			2-343
SD1_SCM_MAX_DTO_SWING	MMReg:0x5F18			2-344
SD1_SCM_MIN_DTO_SWING	MMReg:0x5F14			2-344
SD1_SCM_MOD_CNTL	MMReg:0x5F0C			2-343
SD1_SDTV0_DEBUG	MMReg:0x5F28			2-345
SD1_TIMING_H_ACTIVE_FILT_WINDOW1	MMReg:0x5E8C			2-333
SD1_TIMING_H_ACTIVE_FILT_WINDOW2	MMReg:0x5E90			2-333
SD1_TIMING_H_ADV_ACTIVE	MMReg:0x5E60			2-331
SD1_TIMING_H_BURST	MMReg:0x5E44			2-329
SD1_TIMING_H_COUNT	MMReg:0x5E0C			2-325
SD1_TIMING_H_COUNT_INIT	MMReg:0x5E14			2-325
SD1_TIMING_H_EQUALIZATION1	MMReg:0x5E24			2-326
SD1_TIMING_H_EQUALIZATION2	MMReg:0x5E28			2-327
SD1_TIMING_H_HSYNC	MMReg:0x5E20			2-326
SD1_TIMING_H_RUNIN_FILT_WINDOW	MMReg:0x5E94			2-334
SD1_TIMING_H_SERATION1	MMReg:0x5E2C			2-327
SD1_TIMING_H_SERATION2	MMReg:0x5E30			2-327
SD1_TIMING_H_SETUP1	MMReg:0x5E50			2-330
SD1_TIMING_H_SETUP2	MMReg:0x5E54			2-330
SD1_TIMING_H_TOTAL	MMReg:0x5E04			2-324
SD1_TIMING_INTERNAL_INIT	MMReg:0x5E1C			2-326
SD1_TIMING_V_ACTIVE1	MMReg:0x5E64			2-332
SD1_TIMING_V_ACTIVE2	MMReg:0x5E68			2-332
SD1_TIMING_V_BURST1	MMReg:0x5E48			2-329

Table 2-2 All Registers Sorted By Name

Name	Address	Secondary Address	Additional Address	Page
SD1_TIMING_V_BURST2	MMReg:0x5E4C			2-329
SD1_TIMING_V_EQUALIZATION1	MMReg:0x5E34			2-327
SD1_TIMING_V_EQUALIZATION2	MMReg:0x5E38			2-328
SD1_TIMING_V_F_COUNT	MMReg:0x5E10			2-325
SD1_TIMING_V_F_COUNT_INIT	MMReg:0x5E18			2-325
SD1_TIMING_V_F_TOTAL	MMReg:0x5E08			2-325
SD1_TIMING_V_SERATION1	MMReg:0x5E3C			2-328
SD1_TIMING_V_SERATION2	MMReg:0x5E40			2-328
SD1_TIMING_V_SETUP1	MMReg:0x5E58			2-330
SD1_TIMING_V_SETUP2	MMReg:0x5E5C			2-331
SD1_U_AND_V_GAIN_SETTINGS	MMReg:0x5EA4			2-335
SD1_U_V_BREAK_POINT_SETTINGS	MMReg:0x5E9C			2-334
SD1_UPSAMPLE_MODE	MMReg:0x5F94			2-345
SD1_VIDEO_PORT_SIG	MMReg:0x5F20			2-344
SD1_VIDOUT_MUX_CNTL	MMReg:0x5EC8			2-339
SD1_Y_AND_PASSTHRU_GAIN_SETTINGS	MMReg:0x5EA0			2-335
SD1_Y_BREAK_POINT_SETTING	MMReg:0x5E98			2-334
SECONDARY_STATUS	pcieConfigDev[10:2]\:0x1E			2-76
SEQ00	VGASEQIND\:0x0			2-300
SEQ01	VGASEQIND\:0x1			2-300
SEQ02	VGASEQIND\:0x2			2-300
SEQ03	VGASEQIND\:0x3			2-301
SEQ04	VGASEQIND\:0x4			2-301
SEQ8_DATA	MMReg:0x3C5	VGA_IO:0x3C5		2-302
SEQ8_IDX	MMReg:0x3C4	VGA_IO:0x3C4		2-302
SLOT_CAP	pcieConfigDev[10:2]\:0x6C			2-84
SLOT_CNTL	pcieConfigDev[10:2]\:0x70			2-84
SLOT_STATUS	pcieConfigDev[10:2]\:0x72			2-85
SPLL_BYPASSCLK_SEL	CLKIND:0x1			2-268
SPLL_CLK_SEL	CLKIND:0x3			2-268
SPLL_CNTL_MODE	CLKIND:0x2			2-268
SPLL_FUNC_CNTL	CLKIND:0x0			2-267
SPLL_TIME	CLKIND:0x24			2-279
SSID_CAP_LIST	pcieConfigDev[10:2]\:0xB0			2-88
SSID_ID	pcieConfigDev[10:2]\:0xB4			2-88
STATUS	gcconfig:0x6	MMReg:0x5006:R		2-110
StrapsOutputMux_0	NBMISCIND:0x60			2-37
StrapsOutputMux_1	NBMISCIND:0x61			2-37
StrapsOutputMux_2	NBMISCIND:0x62			2-37

Table 2-2 All Registers Sorted By Name

Name	Address	Secondary Address	Additional Address	Page
StrapsOutputMux_3	*NBMISCIND:0x63*			*2-38*
StrapsOutputMux_4	*NBMISCIND:0x64*			*2-38*
StrapsOutputMux_5	*NBMISCIND:0x65*			*2-38*
StrapsOutputMux_6	*NBMISCIND:0x66*			*2-38*
StrapsOutputMux_7	*NBMISCIND:0x67*			*2-39*
StrapsOutputMux_8	*NBMISCIND:0x68*			*2-39*
StrapsOutputMux_9	*NBMISCIND:0x69*			*2-40*
StrapsOutputMux_A	*NBMISCIND:0x6A*			*2-40*
StrapsOutputMux_B	*NBMISCIND:0x6B*			*2-40*
StrapsOutputMux_C	*NBMISCIND:0x6C*			*2-40*
StrapsOutputMux_D	*NBMISCIND:0x6D*			*2-40*
StrapsOutputMux_E	*NBMISCIND:0x6E*			*2-41*
StrapsOutputMux_F	*NBMISCIND:0x6F*			*2-41*
SU_DYN_CNTL	*CLKIND:0x15*			*2-275*
SUB_BUS_NUMBER_LATENCY	*pcieConfigDev[10:2]\:0x18*			*2-75*
SUB_CLASS	*gcconfig:0xA*	*MMReg:0x500A*		*2-112*
TCL_DYN_CNTL	*CLKIND:0x1A*			*2-274*
TX_DYN_CNTL	*CLKIND:0x27*			*2-276*
US_DYN_CNTL	*CLKIND:0x28*			*2-276*
VENDOR_ID	*gcconfig:0x0*	*MMReg:0x5000*		*2-110*
VGA_MEM_READ_PAGE_ADDR	*IOReg:0x3C*	*MMReg:0x3C*		*2-353*
VGA_MEM_WRITE_PAGE_ADDR	*IOReg:0x38*	*MMReg:0x38*		*2-353*
VGA25_PPLL_POST_DIV	*MMReg:0x388*			*2-353*
VGA25_PPLL_POST_DIV_SRC	*MMReg:0x384*			*2-352*
VIP_DYN_CNTL	*CLKIND:0x14*			*2-274*
VOL_DROP_CNT	*CLKIND:0x36*			*2-285*

A.4 All Registers Sorted By Address

Table 2-3 All Registers Sorted By Address

Address	Name	Secondary Address	Additional Address	Page
apcconfig:0x1E	APC_AGP_PCI_STATUS			2-147
apcconfig:0x2	APC_DEVICE_ID			2-143
apcconfig:0x24	APC_AGP_PCI_PREFETCHABLE_LIMIT_BASE			2-148
apcconfig:0x34	APC_CAPABILITIES_PTR			2-149
apcconfig:0x40	APC_MISC_DEVICE_CTRL			2-151
apcconfig:0x44	APC_HT_MSI_CAP			2-151
apcconfig:0x6	APC_STATUS			2-144
apcconfig\:0x0	APC_VENDOR_ID			2-143
apcconfig\:0x18	APC_SUB_BUS_NUMBER_LATENCY			2-147
apcconfig\:0x1C	APC_AGP_PCI_IOBASE_LIMIT			2-147
apcconfig\:0x20	APC_AGP_PCI_MEMORY_LIMIT_BASE			2-148
apcconfig\:0x28	APC_AGP_PCI_PREFETCHABLE_BASE_Upper			2-148
apcconfig\:0x2C	APC_AGP_PCI_PREFETCHABLE_LIMIT_Upper			2-148
apcconfig\:0x30	APC_AGP_PCI_IO_LIMIT_BASE_HI			2-149
apcconfig\:0x3C	APC_AGP_PCI_IRQ_BRIDGE_CTRL			2-149
apcconfig\:0x4	APC_COMMAND			2-143
apcconfig\:0x4C	APC_ADAPTER_ID_W			2-151
apcconfig\:0x8	APC_REVISION_ID			2-145
apcconfig\:0x9	APC_REGPROG_INF			2-145
apcconfig\:0xA	APC_SUB_CLASS			2-145
apcconfig\:0xB	APC_BASE_CODE			2-146
apcconfig\:0xB0	APC_SSID_CAP_ID			2-152
apcconfig\:0xB4	APC_SSID			2-152
apcconfig\:0xC	APC_CACHE_LINE			2-146
apcconfig\:0xD	APC_LATENCY			2-146
apcconfig\:0xE	APC_HEADER			2-146
apcconfig\:0xF	APC_BIST			2-146
clkconfig:0x40	OSC_CONTROL			2-130
clkconfig:0x44	CPLL_CONTROL			2-138
clkconfig:0x4C	CLK_TOP_PWM4_CTRL			2-138
clkconfig:0x50	CLK_TOP_PWM5_CTRL			2-139
clkconfig:0x5C	DELAY_SET_IOC_CCLK			2-139
clkconfig:0x68	CT_DISABLE_BIU			2-139
clkconfig:0x70	CPLL_CONTROL3			2-140
clkconfig:0x74	GC_CLK_CNTRL			2-131
clkconfig:0x8C	CLKGATE_DISABLE2			2-132

Table 2-3 All Registers Sorted By Address

Address	Name	Secondary Address	Additional Address	Page
clkconfig:0x94	CLKGATE_DISABLE			2-132
clkconfig:0x98	CPLL_CONTROL2			2-140
clkconfig:0xAC	CLK_TOP_PERF_CNTL			2-135
clkconfig:0xB0	clk_top_pwm1_ctrl			2-141
clkconfig:0xB4	clk_top_pwm2_ctrl			2-141
clkconfig:0xB8	clk_top_test_ctrl			2-141
clkconfig:0xC0	CLK_TOP_THERMAL_ALERT_INTR_EN			2-141
clkconfig:0xC4	CLK_TOP_THERMAL_ALERT_STATUS			2-141
clkconfig:0xC8	CLK_TOP_THERMAL_ALERT_WAIT_WINDOW			2-142
clkconfig:0xCC	clk_top_pwm3_ctrl			2-142
clkconfig:0xD0	clk_top_spare_pll			2-142
clkconfig:0xE0	CLK_TOP_SPARE_A			2-136
clkconfig:0xE4	CLK_TOP_SPARE_B			2-137
clkconfig:0xE8	CLK_TOP_SPARE_C			2-137
clkconfig:0xEC	CLK_TOP_SPARE_D			2-137
clkconfig:0xF8	CFG_CT_CLKGATE_HTIU			2-138
clkconfig\:0x78	SCRATCH_1_CLKCFG			2-131
clkconfig\:0x7C	SCRATCH_2_CLKCFG			2-131
clkconfig\:0x84	SCRATCH_CLKCFG			2-132
clkconfig\:0xD4	CLK_CFG_HTPLL_CNTL			2-136
CLKIND:0x0	SPLL_FUNC_CNTL			2-267
CLKIND:0x1	SPLL_BYPASSCLK_SEL			2-268
CLKIND:0x10	HDP_DYN_CNTL			2-273
CLKIND:0x11	E2_DYN_CNTL			2-273
CLKIND:0x14	VIP_DYN_CNTL			2-274
CLKIND:0x15	SU_DYN_CNTL			2-275
CLKIND:0x17	FG_DYN_CNTL			2-275
CLKIND:0x18	SC_DYN_CNTL			2-275
CLKIND:0x19	RS_DYN_CNTL			2-275
CLKIND:0x1A	TCL_DYN_CNTL			2-274
CLKIND:0x1B	GA_DYN_CNTL			2-274
CLKIND:0x1D	MC_GUI_DYN_CNTL			2-276
CLKIND:0x1E	MC_HOST_DYN_CNTL			2-277
CLKIND:0x1F	CG_MISC_REG			2-277
CLKIND:0x2	SPLL_CNTL_MODE			2-268
CLKIND:0x20	CG_DEBUG			2-277
CLKIND:0x21	PLL_TEST_CNTL			2-267
CLKIND:0x22	MCLK_MISC			2-278
CLKIND:0x23	DLL_CNTL			2-278
CLKIND:0x24	SPLL_TIME			2-279

Table 2-3 All Registers Sorted By Address

Address	Name	Secondary Address	Additional Address	Page
CLKIND:0x25	MPLL_TIME			2-279
CLKIND:0x26	MC_RBS_DYN_CNTL			2-277
CLKIND:0x27	TX_DYN_CNTL			2-276
CLKIND:0x28	US_DYN_CNTL			2-276
CLKIND:0x29	DYN_BACKBIAS_CNTL			2-279
CLKIND:0x2A	POLARITY_CNTL			2-279
CLKIND:0x2B	OVERCLOCK_CNTL			2-279
CLKIND:0x2C	ERROR_STATUS			2-280
CLKIND:0x2D	CC_FUSE_STRAPS_0			2-280
CLKIND:0x2E	CC_FUSE_STRAPS_1			2-281
CLKIND:0x2F	CC_DEBUG_STRAPS_0			2-281
CLKIND:0x3	SPLL_CLK_SEL			2-268
CLKIND:0x30	CC_DEBUG_STRAPS_1			2-282
CLKIND:0x31	CC_IO_STRAPS			2-282
CLKIND:0x31	CC_IO_STRAPS_12A			2-283
CLKIND:0x31	CC_IO_STRAPS_22A			2-282
CLKIND:0x32	CC_ROM_STRAPS			2-283
CLKIND:0x33	CC_COMBINED_STRAPS_0			2-284
CLKIND:0x34	CC_COMBINED_STRAPS_1			2-285
CLKIND:0x35	CG_CLKPIN_CNTL			2-285
CLKIND:0x36	VOL_DROP_CNT			2-285
CLKIND:0x37	BACKBIAS_ENABLE_CNT			2-285
CLKIND:0x38	CG_TC_JTAG_0			2-286
CLKIND:0x39	CG_TC_JTAG_1			2-286
CLKIND:0x3A	FVTHROT_CNTRL_REG			2-286
CLKIND:0x3B	FVTHROT_TARGET_REG			2-287
CLKIND:0x3C	FVTHROT_COMPARE_BOUND1			2-287
CLKIND:0x3D	FVTHROT_COMPARE_BOUND2			2-287
CLKIND:0x3E	FVTHROT_COMPARE_BOUND3			2-287
CLKIND:0x3F	FVTHROT_COMPARE_BOUND4			2-287
CLKIND:0x4	MPLL_FUNC_CNTL			2-269
CLKIND:0x40	FVTHROT_UPTREND_COEF0			2-287
CLKIND:0x41	FVTHROT_UPTREND_COEF1			2-288
CLKIND:0x42	FVTHROT_UPTREND_COEF2			2-288
CLKIND:0x43	FVTHROT_UPTREND_COEF3			2-288
CLKIND:0x44	FVTHROT_UPTREND_COEF4			2-288
CLKIND:0x45	FVTHROT_DOWNTREND_COEF0			2-288
CLKIND:0x46	FVTHROT_DOWNTREND_COEF1			2-289
CLKIND:0x47	FVTHROT_DOWNTREND_COEF2			2-289
CLKIND:0x48	FVTHROT_DOWNTREND_COEF3			2-289
CLKIND:0x49	FVTHROT_DOWNTREND_COEF4			2-289

Table 2-3 All Registers Sorted By Address

Address	Name	Secondary Address	Additional Address	Page
CLKIND:0x4A	FVTHROT_FBDIV_REG0			2-289
CLKIND:0x4B	FVTHROT_FBDIV_REG1			2-289
CLKIND:0x4C	FVTHROT_FBDIV_REG2			2-290
CLKIND:0x4D	FVTHROT_FB_UPSTEP_REG0			2-290
CLKIND:0x4E	FVTHROT_FB_UPSTEP_REG1			2-290
CLKIND:0x4F	FVTHROT_FB_DOWNSTEP_REG0			2-290
CLKIND:0x5	MPLL_BYPASSCLK_SEL			2-269
CLKIND:0x50	FVTHROT_FB_DOWNSTEP_REG1			2-290
CLKIND:0x51	FVTHROT_PWM_CTRL_REG0			2-290
CLKIND:0x52	FVTHROT_PWM_CTRL_REG1			2-291
CLKIND:0x53	FVTHROT_PWM_UPSTEP_REG0			2-291
CLKIND:0x54	FVTHROT_PWM_UPSTEP_REG1			2-291
CLKIND:0x55	FVTHROT_PWM_DOWNSTEP_REG0			2-291
CLKIND:0x56	FVTHROT_PWM_DOWNSTEP_REG1			2-291
CLKIND:0x57	FVTHROT_STATUS_REG0			2-291
CLKIND:0x58	FVTHROT_STATUS_REG1			2-292
CLKIND:0x59	FVTHROT_STATUS_REG2			2-292
CLKIND:0x5A	CG_SPLL_ANALOG_CTRL0			2-292
CLKIND:0x5B	CG_SPLL_ANALOG_CTRL1			2-292
CLKIND:0x5C	CG_INTGFX_MISC			2-292
CLKIND:0x5D	CG_INTGFX_SPARE_RO			2-293
CLKIND:0x5E	FVTHROT_PWM_FEEDBACK_DIV_REG1			2-293
CLKIND:0x5F	FVTHROT_PWM_FEEDBACK_DIV_REG2			2-293
CLKIND:0x6	MPLL_CNTL_MODE			2-269
CLKIND:0x60	FVTHROT_PWM_FEEDBACK_DIV_REG3			2-293
CLKIND:0x61	FVTHROT_PWM_FEEDBACK_DIV_REG4			2-293
CLKIND:0x62	FVTHROT_SPLL_PARAM_FEEDBACK_DIV_REG1			2-294
CLKIND:0x63	FVTHROT_SPLL_PARAM_FEEDBACK_DIV_REG2			2-294
CLKIND:0x64	FVTHROT_SPLL_PARAM_FEEDBACK_DIV_REG3			2-294
CLKIND:0x65	FVTHROT_SPLL_PARAM_FEEDBACK_DIV_REG4			2-294
CLKIND:0x66	FVTHROT_SLOW_CLK_FEEDBACK_DIV_REG1			2-294
CLKIND:0x67	FVTHROT_SCALE_FEEDBACK_DIV_REG1			2-295
CLKIND:0x7	MPLL_CLK_SEL			2-270
CLKIND:0x8	GENERAL_PWRMGT			2-270

Table 2-3 All Registers Sorted By Address

Address	Name	Secondary Address	Additional Address	Page
CLKIND:0x9	*SCLK_PWRMGT_CNTL*			*2-270*
CLKIND:0xA	*MCLK_PWRMGT_CNTL*			*2-271*
CLKIND:0xB	*DYN_PWRMGT_SCLK_CNTL*			*2-271*
CLKIND:0xC	*DYN_PWRMGT_SCLK_LENGTH*			*2-272*
CLKIND:0xD	*DYN_SCLK_PWMEN_PIPE*			*2-272*
CLKIND:0xE	*DYN_SCLK_VOL_CNTL*			*2-272*
CLKIND:0xF	*CP_DYN_CNTL*			*2-272*
gcconfig:0x0	*VENDOR_ID*	*MMReg:0x5000*		*2-110*
gcconfig:0x10	*MEM_BASE_LO*	*MMReg:0x5010:R*		*2-114*
gcconfig:0x100	*F1_VENDOR_ID*	*MMReg:0x5100*		*2-116*
gcconfig:0x102	*F1_DEVICE_ID*	*MMReg:0x5102*		*2-116*
gcconfig:0x104	*F1_COMMAND*	*MMReg:0x5104:R*		*2-116*
gcconfig:0x106	*F1_STATUS*	*MMReg:0x5106*		*2-116*
gcconfig:0x108	*F1_REVISION_ID*	*MMReg:0x5108*		*2-116*
gcconfig:0x109	*F1_REGPROG_INF*	*MMReg:0x5109*		*2-116*
gcconfig:0x10A	*F1_SUB_CLASS*	*MMReg:0x510A*		*2-117*
gcconfig:0x10B	*F1_BASE_CODE*	*MMReg:0x510B*		*2-117*
gcconfig:0x10C	*F1_CACHE_LINE*	*MMReg:0x510C:R*		*2-117*
gcconfig:0x10D	*F1_LATENCY*	*MMReg:0x510D:R*		*2-117*
gcconfig:0x10E	*F1_HEADER*	*MMReg:0x510E*		*2-117*
gcconfig:0x10F	*F1_BIST*	*MMReg:0x510F*		*2-117*
gcconfig:0x110	*F1_REG_BASE_LO*	*MMReg:0x5114:R*		*2-118*
gcconfig:0x114	*F1_REG_BASE_HI*	*MMReg:0x511C:R*		*2-118*
gcconfig:0x12C	*F1_ADAPTER_ID*	*MMReg:0x512C*		*2-118*
gcconfig:0x134	*F1_CAPABILITIES_PTR*	*MMReg:0x5134*		*2-118*
gcconfig:0x13C	*F1_INTERRUPT_LINE*	*MMReg:0x513C:R*		*2-118*
gcconfig:0x13D	*F1_INTERRUPT_PIN*	*MMReg:0x513D*		*2-118*
gcconfig:0x13E	*F1_MIN_GRANT*	*MMReg:0x513E*		*2-119*
gcconfig:0x13F	*F1_MAX_LATENCY*	*MMReg:0x513F*		*2-119*
gcconfig:0x14	*MEM_BASE_HI*	*MMReg:0x5014:R*		*2-114*
gcconfig:0x14C	*F1_ADAPTER_ID_W*	*MMReg:0x514C:R*		*2-120*
gcconfig:0x150	*F1_PMI_CAP_ID*	*MMReg:0x5150*		*2-119*
gcconfig:0x151	*F1_PMI_NXT_CAP_PTR*	*MMReg:0x5151*		*2-119*
gcconfig:0x152	*F1_PMI_PMC_REG*	*MMReg:0x5152*		*2-119*
gcconfig:0x154	*F1_PMI_STATUS*	*MMReg:0x5154:R*		*2-120*
gcconfig:0x157	*F1_PMI_DATA*	*MMReg:0x5157*		*2-119*
gcconfig:0x18	*REG_BASE_LO*	*MMReg:0x5018:R*		*2-114*
gcconfig:0x1C	*REG_BASE_HI*	*MMReg:0x501C:R*		*2-115*
gcconfig:0x2	*DEVICE_ID*	*MMReg:0x5002*		*2-110*
gcconfig:0x20	*IO_BASE*	*MMReg:0x5020:R*		*2-111*
gcconfig:0x200	*F2_VENDOR_ID*	*MMReg:0x5200*		*2-120*

Table 2-3 All Registers Sorted By Address

Address	Name	Secondary Address	Additional Address	Page
gcconfig:0x202	F2_DEVICE_ID	MMReg:0x5202		2-120
gcconfig:0x204	F2_COMMAND	MMReg:0x5204:R		2-121
gcconfig:0x206	F2_STATUS	MMReg:0x5206		2-121
gcconfig:0x208	F2_REVISION_ID	MMReg:0x5208		2-121
gcconfig:0x209	F2_REGPROG_INF	MMReg:0x5209		2-121
gcconfig:0x20A	F2_SUB_CLASS	MMReg:0x520A		2-121
gcconfig:0x20B	F2_BASE_CODE	MMReg:0x520B		2-122
gcconfig:0x20C	F2_CACHE_LINE	MMReg:0x520C:R		2-122
gcconfig:0x20D	F2_LATENCY	MMReg:0x520D:R		2-122
gcconfig:0x20E	F2_HEADER	MMReg:0x520E		2-122
gcconfig:0x20F	F2_BIST	MMReg:0x520F		2-122
gcconfig:0x210	F2_REG_BASE_LO	MMReg:0x5210:R		2-122
gcconfig:0x214	F2_REG_BASE_HI	MMReg:0x5214:R		2-123
gcconfig:0x22C	F2_ADAPTER_ID	MMReg:0x522C		2-123
gcconfig:0x234	F2_CAPABILITIES_PTR	MMReg:0x5234		2-123
gcconfig:0x23C	F2_INTERRUPT_LINE	MMReg:0x523C:R		2-123
gcconfig:0x23D	F2_INTERRUPT_PIN	MMReg:0x523D		2-123
gcconfig:0x23E	F2_MIN_GRANT	MMReg:0x523E		2-123
gcconfig:0x23F	F2_MAX_LATENCY	MMReg:0x523F		2-124
gcconfig:0x24C	F2_ADAPTER_ID_W	MMReg:0x524C:R		2-124
gcconfig:0x250	F2_PMI_CAP_ID	MMReg:0x5250		2-124
gcconfig:0x251	F2_PMI_NXT_CAP_PTR	MMReg:0x5251		2-124
gcconfig:0x252	F2_PMI_PMC_REG	MMReg:0x5252		2-124
gcconfig:0x254	F2_PMI_STATUS	MMReg:0x5254:R		2-125
gcconfig:0x257	F2_PMI_DATA	MMReg:0x5257		2-125
gcconfig:0x260	F2_MSI_CAP_ID	MMReg:0x5260		2-125
gcconfig:0x261	F2_MSI_NXT_CAP_PTR	MMReg:0x5261		2-125
gcconfig:0x262	F2_MSI_MSG_CNTL	MMReg:0x5262:R		2-126
gcconfig:0x264	F2_MSI_MSG_ADDR_LO	MMReg:0x5264:R		2-126
gcconfig:0x268	F2_MSI_MSG_ADDR_HI	MMReg:0x5268:R		2-126
gcconfig:0x26C	F2_MSI_MSG_DATA	MMReg:0x526C:R		2-126
gcconfig:0x2C	ADAPTER_ID	MMReg:0x502C		2-111
gcconfig:0x34	CAPABILITIES_PTR	MMReg:0x5034		2-112
gcconfig:0x3C	INTERRUPT_LINE	MMReg:0x503C:R		2-113
gcconfig:0x3D	INTERRUPT_PIN	MMReg:0x503D		2-113
gcconfig:0x3E	MIN_GRANT	MMReg:0x503E		2-114
gcconfig:0x3F	MAX_LATENCY	MMReg:0x503F		2-113
gcconfig:0x4	COMMAND	MMReg:0x5004:R		2-110
gcconfig:0x4C	ADAPTER_ID_W	MMReg:0x504C:R		2-111
gcconfig:0x50	PMI_CAP_ID	MMReg:0x5050		2-129
gcconfig:0x51	PMI_NXT_CAP_PTR	MMReg:0x5051		2-129

Table 2-3 All Registers Sorted By Address

Address	Name	Secondary Address	Additional Address	Page
gcconfig:0x52	*PMI_PMC_REG*	*MMReg:0x5052*		*2-129*
gcconfig:0x54	*PMI_STATUS*	*MMReg:0x5054:R*		*2-120*
gcconfig:0x57	*PMI_DATA*	*MMReg:0x5057*		*2-129*
gcconfig:0x6	*STATUS*	*MMReg:0x5006:R*		*2-110*
gcconfig:0x8	*REVISION_ID*	*MMReg:0x5008*		*2-111*
gcconfig:0x80	*MSI_CAP_ID*	*MMReg:0x5080*		*2-115*
gcconfig:0x81	*MSI_NXT_CAP_PTR*	*MMReg:0x5081*		*2-115*
gcconfig:0x82	*MSI_MSG_CNTL*	*MMReg:0x5082:R*		*2-115*
gcconfig:0x84	*MSI_MSG_ADDR_LO*	*MMReg:0x5084:R*		*2-115*
gcconfig:0x88	*MSI_MSG_ADDR_HI*	*MMReg:0x5088:R*		*2-115*
gcconfig:0x8C	*MSI_MSG_DATA*	*MMReg:0x508C:R*		*2-116*
gcconfig:0x9	*REGPROG_INF*	*MMReg:0x5009*		*2-114*
gcconfig:0xA	*SUB_CLASS*	*MMReg:0x500A*		*2-112*
gcconfig:0xB	*BASE_CODE*	*MMReg:0x500B*		*2-111*
gcconfig:0xC	*CACHE_LINE*	*MMReg:0x500C:R*		*2-114*
gcconfig:0xD	*LATENCY*	*MMReg:0x500D:R*		*2-113*
gcconfig:0xE	*HEADER*	*MMReg:0x500E*		*2-113*
gcconfig:0xF	*BIST*	*MMReg:0x500F*		*2-112*
HTIUNBIND:0x0	*HTIU_CNTL_1*			*2-43*
HTIUNBIND:0x1	*HTIU_CNTL_2*			*2-43*
HTIUNBIND:0x10	*HTIU_UPSTREAM_CONFIG_9*			*2-51*
HTIUNBIND:0x11	*HTIU_UPSTREAM_CONFIG_10*			*2-52*
HTIUNBIND:0x12	*HTIU_UPSTREAM_CONFIG_11*			*2-52*
HTIUNBIND:0x13	*HTIU_UPSTREAM_CONFIG_12*			*2-52*
HTIUNBIND:0x14	*HTIU_UPSTREAM_CONFIG_13*			*2-53*
HTIUNBIND:0x15	*HTIU_UPSTREAM_CONFIG_14*			*2-53*
HTIUNBIND:0x16	*HTIU_UPSTREAM_CONFIG_15*			*2-54*
HTIUNBIND:0x17	*HTIU_UPSTREAM_CONFIG_16*			*2-54*
HTIUNBIND:0x18	*HTIU_UPSTREAM_CONFIG_17*			*2-54*
HTIUNBIND:0x19	*HTIU_UPSTREAM_CONFIG_18*			*2-55*
HTIUNBIND:0x1A	*HTIU_UPSTREAM_CONFIG_19*			*2-55*
HTIUNBIND:0x1B	*HTIU_UPSTREAM_CONFIG_20*			*2-56*
HTIUNBIND:0x1C	*HTIU_UPSTREAM_CONFIG_21*			*2-56*
HTIUNBIND:0x1D	*HTIU_UPSTREAM_CONFIG_22*			*2-56*
HTIUNBIND:0x1E	*HTIU_UPSTREAM_CONFIG_23*			*2-56*
HTIUNBIND:0x1F	*HTIU_UPSTREAM_CONFIG_24*			*2-56*
HTIUNBIND:0x2	*HTIU_PERF_CNTL*			*2-43*
HTIUNBIND:0x3	*HTIU_PERF_COUNT_0*			*2-45*
HTIUNBIND:0x30	*NB_LOWER_TOP_OF_DRAM2*			*2-57*
HTIUNBIND:0x31	*NB_UPPER_TOP_OF_DRAM2*			*2-57*
HTIUNBIND:0x32	*NB_HTIU_CFG*			*2-57*

Table 2-3 All Registers Sorted By Address

Address	Name	Secondary Address	Additional Address	Page
HTIUNBIND:0x4	HTIU_PERF_COUNT_1			2-45
HTIUNBIND:0x5	HTIU_DEBUG			2-46
HTIUNBIND:0x6	HTIU_DOWNSTREAM_CONFIG			2-46
HTIUNBIND:0x7	HTIU_UPSTREAM_CONFIG_0			2-47
HTIUNBIND:0x8	HTIU_UPSTREAM_CONFIG_1			2-48
HTIUNBIND:0x9	HTIU_UPSTREAM_CONFIG_2			2-48
HTIUNBIND:0xA	HTIU_UPSTREAM_CONFIG_3			2-49
HTIUNBIND:0xB	HTIU_UPSTREAM_CONFIG_4			2-49
HTIUNBIND:0xC	HTIU_UPSTREAM_CONFIG_5			2-50
HTIUNBIND:0xD	HTIU_UPSTREAM_CONFIG_6			2-50
HTIUNBIND:0xE	HTIU_UPSTREAM_CONFIG_7			2-51
HTIUNBIND:0xF	HTIU_UPSTREAM_CONFIG_8			2-51
IOReg:0x0	MM_INDEX	MMReg:0x0		2-127
IOReg:0x10	BIOS_0_SCRATCH	MMReg:0x10		2-353
IOReg:0x14	BIOS_1_SCRATCH	MMReg:0x14		2-353
IOReg:0x18	BIOS_2_SCRATCH	MMReg:0x18		2-353
IOReg:0x1C	BIOS_3_SCRATCH	MMReg:0x1C		2-354
IOReg:0x20	BIOS_4_SCRATCH	MMReg:0x20		2-354
IOReg:0x24	BIOS_5_SCRATCH	MMReg:0x24		2-354
IOReg:0x28	BIOS_6_SCRATCH	MMReg:0x28		2-354
IOReg:0x2C	BIOS_7_SCRATCH	MMReg:0x2C		2-354
IOReg:0x30	BUS_CNTL	MMReg:0x30		2-351
IOReg:0x34	BUS_CNTL1	MMReg:0x34		2-352
IOReg:0x38	VGA_MEM_WRITE_PAGE_ADDR	MMReg:0x38		2-353
IOReg:0x3C	VGA_MEM_READ_PAGE_ADDR	MMReg:0x3C		2-353
IOReg:0x4	MM_DATA	MMReg:0x4		2-127
IOReg:0x58	DAC_CNTL	MMReg:0x58		2-299
IOReg:0x8	CLOCK_CNTL_INDEX	MMReg:0x8		2-267
IOReg:0xB0	MEDIA_0_SCRATCH	MMReg:0xB0		2-354
IOReg:0xB4	MEDIA_1_SCRATCH	MMReg:0xB4		2-354
IOReg:0xC	CLOCK_CNTL_DATA	MMReg:0xC		2-267
IOReg:0xC0	BIOS_8_SCRATCH	MMReg:0xC0		2-355
IOReg:0xC4	BIOS_9_SCRATCH	MMReg:0xC4		2-355
IOReg:0xC8	BIOS_10_SCRATCH	MMReg:0xC8		2-355
IOReg:0xCC	BIOS_11_SCRATCH	MMReg:0xCC		2-355
IOReg:0xD0	BIOS_12_SCRATCH	MMReg:0xD0		2-355
IOReg:0xD4	BIOS_13_SCRATCH	MMReg:0xD4		2-355
IOReg:0xD8	BIOS_14_SCRATCH	MMReg:0xD8		2-355
IOReg:0xDC	BIOS_15_SCRATCH	MMReg:0xDC		2-356
IOReg:0xE4	CONFIG_XSTRAP	MMReg:0xE4		2-356
IOReg\:0xE0	CONFIG_CNTL	MMReg\:0xE0		2-112

Table 2-3 All Registers Sorted By Address

Address	Name	Secondary Address	Additional Address	Page
IOReg\:0xF8	*CONFIG_MEMSIZE*	*MMReg\:0xF8*		*2-112*
MCIND:0x103	*AGP_BASE_2*			*2-350*
MMGartReg:0x0	*RCRB_Enhanced_Capability_Header*			*2-266*
MMReg:0x100	*CONFIG_MEM_BASE_LO*			*2-356*
MMReg:0x104	*CONFIG_MEM_BASE_HI*			*2-356*
MMReg:0x10C	*CONFIG_REG_BASE_LO*			*2-356*
MMReg:0x110	*CONFIG_REG_BASE_HI*			*2-357*
MMReg:0x114	*CONFIG_REG_APER_SIZE*			*2-113*
MMReg:0x134	*HDP_FB_LOCATION*			*2-357*
MMReg:0x180C	*BIF_SLAVE_CNTL*			*2-350*
MMReg:0x384	*VGA25_PPLL_POST_DIV_SRC*			*2-352*
MMReg:0x388	*VGA25_PPLL_POST_DIV*			*2-353*
MMReg:0x3B4	*CRTC8_IDX*	*MMReg:0x3D4*	*VGA_IO:0x3B4 VGA_IO:0x3D4: O:0x3D4*	*2-303*
MMReg:0x3B5	*CRTC8_DATA*	*MMReg:0x3D5*	*VGA_IO:0x3B5 VGA_IO:0x3D5:I O:0x3D5*	*2-303*
MMReg:0x3C2	*GENMO_WT*	*VGA_IO:0x3C2*		*2-127*
MMReg:0x3C4	*SEQ8_IDX*	*VGA_IO:0x3C4*		*2-302*
MMReg:0x3C5	*SEQ8_DATA*	*VGA_IO:0x3C5*		*2-302*
MMReg:0x3CC	*GENMO_RD*	*VGA_IO:0x3CC*		*2-128*
MMReg:0x3CE	*GRPH8_IDX*	*VGA_IO:0x3CE*		*2-312*
MMReg:0x3CF	*GRPH8_DATA*	*VGA_IO:0x3CF*		*2-312*
MMReg:0x5DFC	*SD1_MAIN_CNTL*			*2-322*
MMReg:0x5E04	*SD1_TIMING_H_TOTAL*			*2-324*
MMReg:0x5E08	*SD1_TIMING_V_F_TOTAL*			*2-325*
MMReg:0x5E0C	*SD1_TIMING_H_COUNT*			*2-325*
MMReg:0x5E10	*SD1_TIMING_V_F_COUNT*			*2-325*
MMReg:0x5E14	*SD1_TIMING_H_COUNT_INIT*			*2-325*
MMReg:0x5E18	*SD1_TIMING_V_F_COUNT_INIT*			*2-325*
MMReg:0x5E1C	*SD1_TIMING_INTERNAL_INIT*			*2-326*
MMReg:0x5E20	*SD1_TIMING_H_HSYNC*			*2-326*
MMReg:0x5E24	*SD1_TIMING_H_EQUALIZATION1*			*2-326*
MMReg:0x5E28	*SD1_TIMING_H_EQUALIZATION2*			*2-327*
MMReg:0x5E2C	*SD1_TIMING_H_SERATION1*			*2-327*
MMReg:0x5E30	*SD1_TIMING_H_SERATION2*			*2-327*
MMReg:0x5E34	*SD1_TIMING_V_EQUALIZATION1*			*2-327*
MMReg:0x5E38	*SD1_TIMING_V_EQUALIZATION2*			*2-328*
MMReg:0x5E3C	*SD1_TIMING_V_SERATION1*			*2-328*
MMReg:0x5E40	*SD1_TIMING_V_SERATION2*			*2-328*

Table 2-3 All Registers Sorted By Address

Address	Name	Secondary Address	Additional Address	Page
MMReg:0x5E44	SD1_TIMING_H_BURST			2-329
MMReg:0x5E48	SD1_TIMING_V_BURST1			2-329
MMReg:0x5E4C	SD1_TIMING_V_BURST2			2-329
MMReg:0x5E50	SD1_TIMING_H_SETUP1			2-330
MMReg:0x5E54	SD1_TIMING_H_SETUP2			2-330
MMReg:0x5E58	SD1_TIMING_V_SETUP1			2-330
MMReg:0x5E5C	SD1_TIMING_V_SETUP2			2-331
MMReg:0x5E60	SD1_TIMING_H_ADV_ACTIVE			2-331
MMReg:0x5E64	SD1_TIMING_V_ACTIVE1			2-332
MMReg:0x5E68	SD1_TIMING_V_ACTIVE2			2-332
MMReg:0x5E8C	SD1_TIMING_H_ACTIVE_FILT_WINDOW1			2-333
MMReg:0x5E90	SD1_TIMING_H_ACTIVE_FILT_WINDOW2			2-333
MMReg:0x5E94	SD1_TIMING_H_RUNIN_FILT_WINDOW			2-334
MMReg:0x5E98	SD1_Y_BREAK_POINT_SETTING			2-334
MMReg:0x5E9C	SD1_U_V_BREAK_POINT_SETTINGS			2-334
MMReg:0x5EA0	SD1_Y_AND_PASSTHRU_GAIN_SETTINGS			2-335
MMReg:0x5EA4	SD1_U_AND_V_GAIN_SETTINGS			2-335
MMReg:0x5EA8	SD1_LUMA_BLANK_SETUP_LEVELS			2-335
MMReg:0x5EAC	SD1_RGB_OR_PBPR_BLANK_LEVEL			2-336
MMReg:0x5EB0	SD1_LUMA_SYNC_TIP_LEVELS			2-336
MMReg:0x5EB4	SD1_LUMA_FILT_CNTL			2-336
MMReg:0x5EB8	SD1_LUMA_COMB_FILT_CNTL1			2-338
MMReg:0x5EBC	SD1_LUMA_COMB_FILT_CNTL2			2-338
MMReg:0x5EC0	SD1_LUMA_COMB_FILT_CNTL3			2-338
MMReg:0x5EC4	SD1_LUMA_COMB_FILT_CNTL4			2-338
MMReg:0x5EC8	SD1_VIDOUT_MUX_CNTL			2-339
MMReg:0x5ECC	SD1_FORCE_DAC_DATA			2-340
MMReg:0x5EF0	SD1_CHROMA_MOD_CNTL			2-341
MMReg:0x5EF4	SD1_COL_SC_DENOMIN			2-341
MMReg:0x5EF8	SD1_COL_SC_INC			2-342
MMReg:0x5EFC	SD1_COL_SC_INC_CORR			2-342
MMReg:0x5F00	SD1_SCM_COL_SC_DENOMIN			2-342
MMReg:0x5F04	SD1_SCM_COL_SC_INC			2-342
MMReg:0x5F08	SD1_SCM_COL_SC_INC_CORR			2-343
MMReg:0x5F0C	SD1_SCM_MOD_CNTL			2-343
MMReg:0x5F10	SD1_SCM_DB_DR_SCALE_FACTORS			2-343
MMReg:0x5F14	SD1_SCM_MIN_DTO_SWING			2-344
MMReg:0x5F18	SD1_SCM_MAX_DTO_SWING			2-344

Table 2-3 All Registers Sorted By Address

Address	Name	Secondary Address	Additional Address	Page
MMReg:0x5F1C	*SD1_CRC_CNTL*			*2-344*
MMReg:0x5F20	*SD1_VIDEO_PORT_SIG*			*2-344*
MMReg:0x5F28	*SD1_SDTV0_DEBUG*			*2-345*
MMReg:0x5F8C	*SD1_LUMA_OFFSET_LIMIT*			*2-345*
MMReg:0x5F90	*SD1_CHROMA_OFFSET*			*2-345*
MMReg:0x5F94	*SD1_UPSAMPLE_MODE*			*2-345*
MMReg:0x5F98	*SD1_CRTC_HV_START*			*2-346*
MMReg:0x5F9C	*SD1_CRTC_TV_FRAMESTART_CNTL*			*2-346*
MMReg:0x5FA0	*HD_EMBEDDED_SYNC_CNTL*			*2-346*
MMReg:0x5FA4	*HD_INCR*			*2-346*
MMReg:0x5FA8	*HD_TRILEVEL_DUR*			*2-346*
MMReg:0x5FAC	*HD_POS_SYNC_LEVEL*			*2-347*
MMReg:0x5FB0	*HD_BACKPORCH_DUR*			*2-347*
MMReg:0x5FB4	*HD_SERATION_DUR*			*2-347*
MMReg:0x5FD4	*SD1_COL_SC_PHASE_CNTL*			*2-345*
MMReg:0x7AB0	*LVTMA_CRC_CNTL*			*2-348*
MMReg:0x7AB4	*LVTMA_CRC_SIG_MASK*			*2-348*
MMReg:0x7AB8	*LVTMA_CRC_SIG_RGB*			*2-349*
MMReg:0x7ABC	*LVTMA_2ND_CRC_RESULT*			*2-349*
MMReg\:0x108	*CONFIG_APER_SIZE*			*2-112*
nbconfig:0x14	*NB_BAR1_RCRB*			*2-26*
nbconfig:0x18	*NB_BAR2_PM2*			*2-4*
nbconfig:0x1C	*NB_BAR3_PCIEXP_MMCFG*			*2-5*
nbconfig:0x2	*NB_DEVICE_ID*			*2-1*
nbconfig:0x2C	*NB_ADAPTER_ID*			*2-5*
nbconfig:0x34	*NB_CAPABILITIES_PTR*			*2-5*
nbconfig:0x4	*NB_COMMAND*			*2-1*
nbconfig:0x48	*NB_ECC_CTRL*			*2-26*
nbconfig:0x4C	*NB_PCI_CTRL*			*2-6*
nbconfig:0x6	*NB_STATUS*			*2-2*
nbconfig:0x69	*NB_SMRAM*			*2-14*
nbconfig:0x6A	*NB_EXSMRAM*			*2-15*
nbconfig:0x6C	*NB_STRAP_READ_BACK*			*2-15*
nbconfig:0x70	*NB_MC_IND_INDEX*			*2-33*
nbconfig:0x74	*NB_MC_IND_DATA*			*2-33*
nbconfig:0x7C	*NB_IOC_CFG_CNTL*			*2-34*
nbconfig:0x8	*NB_REVISION_ID*			*2-3*
nbconfig:0x80	*NB_HT_CLK_CNTL_RECEIVER_COMP_CNTL*			*2-17*
nbconfig:0x84	*NB_PCI_ARB*			*2-20*
nbconfig:0x8C	*NB_GC_STRAPS*			*2-22*

Table 2-3 All Registers Sorted By Address

Address	Name	Secondary Address	Additional Address	Page
nbconfig:0x90	NB_TOP_OF_DRAM_SLOT1			2-22
nbconfig:0x94	NB_HT_TRANS_COMP_CNTL			2-17
nbconfig:0x9C	NB_CFG_Q_F1000_800			2-25
nbconfig:0xA8	HTIU_NB_INDEX			2-26
nbconfig:0xAC	HTIU_NB_DATA			2-26
nbconfig:0xC	NB_CACHE_LINE			2-3
nbconfig:0xC4	NB_HT_LINK_COMMAND			2-18
nbconfig:0xC8	NB_HT_LINK_CONF_CNTL			2-18
nbconfig:0xCC	NB_HT_LINK_END			2-19
nbconfig:0xD0	NB_HT_LINK_FREQ_CAP_A			2-19
nbconfig:0xD4	NB_HT_LINK_FREQ_CAP_B			2-20
nbconfig:0xDC	NB_HT_MEMORY_BASE_UPPER			2-20
nbconfig:0xE	NB_HEADER			2-4
nbconfig\:0x0	NB_VENDOR_ID			2-1
nbconfig\:0x20	NB_BAR3_UPPER_PCIEXP_MMCFG			2-5
nbconfig\:0x50	NB_ADAPTER_ID_W			2-7
nbconfig\:0x54	SCRATCH_1_NBCFG			2-16
nbconfig\:0x60	NB_MISC_INDEX			2-7
nbconfig\:0x64	NB_MISC_DATA			2-7
nbconfig\:0x68	NB_FDHC			2-14
nbconfig\:0x6B	NB_PMCR			2-15
nbconfig\:0x78	SCRATCH_NBCFG			2-16
nbconfig\:0x9	NB_REGPROG_INF			2-3
nbconfig\:0x98	SCRATCH_2_NBCFG			2-17
nbconfig\:0xA	NB_SUB_CLASS			2-3
nbconfig\:0xB	NB_BASE_CODE			2-3
nbconfig\:0xD	NB_LATENCY			2-4
nbconfig\:0xE0	NB_PCIE_INDX_ADDR			2-24
nbconfig\:0xE4	NB_PCIE_INDX_DATA			2-24
nbconfig\:0xE8	NB_MC_INDEX			2-24
nbconfig\:0xEC	NB_MC_DATA			2-25
nbconfig\:0xF	NB_BIST			2-4
nbconfig\:0xF8	NB_AGP_ADDRESS_SPACE_SIZE			2-23
nbconfig\:0xFC	NB_AGP_MODE_CONTROL			2-24
NBMCIND:0x0	MC_GENERAL_PURPOSE			2-153
NBMCIND:0x100	MCCFG_FB_LOCATION			2-257
NBMCIND:0x101	MCCFG_AGP_LOCATION			2-257
NBMCIND:0x102	MCCFG_AGP_BASE			2-258
NBMCIND:0x103	MCCFG_AGP_BASE_2			2-258
NBMCIND:0x104	MC_INIT_MISC_LAT_TIMER			2-258
NBMCIND:0x105	MC_INIT_GFX_LAT_TIMER			2-259

Table 2-3 All Registers Sorted By Address

Address	Name	Secondary Address	Additional Address	Page
NBMCIND:0x106	MC_INIT_WR_LAT_TIMER			2-259
NBMCIND:0x107	MC_ARB_CNTL			2-260
NBMCIND:0x108	MC_DEBUG_CNTL			2-261
NBMCIND:0x111	MC_BIST_CNTL0			2-262
NBMCIND:0x112	MC_BIST_CNTL1			2-262
NBMCIND:0x113	MC_BIST_MISMATCH_L			2-263
NBMCIND:0x114	MC_BIST_MISMATCH_H			2-263
NBMCIND:0x115	MC_BIST_PATTERN0L			2-263
NBMCIND:0x116	MC_BIST_PATTERN0H			2-263
NBMCIND:0x117	MC_BIST_PATTERN1L			2-264
NBMCIND:0x118	MC_BIST_PATTERN1H			2-264
NBMCIND:0x119	MC_BIST_PATTERN2L			2-264
NBMCIND:0x11A	MC_BIST_PATTERN2H			2-264
NBMCIND:0x11B	MC_BIST_PATTERN3L			2-264
NBMCIND:0x11C	MC_BIST_PATTERN3H			2-264
NBMCIND:0x11D	MC_BIST_PATTERN4L			2-264
NBMCIND:0x11E	MC_BIST_PATTERN4H			2-265
NBMCIND:0x11F	MC_BIST_PATTERN5L			2-265
NBMCIND:0x120	MC_BIST_PATTERN5H			2-265
NBMCIND:0x121	MC_BIST_PATTERN6L			2-265
NBMCIND:0x122	MC_BIST_PATTERN6H			2-265
NBMCIND:0x123	MC_BIST_PATTERN7L			2-265
NBMCIND:0x124	MC_BIST_PATTERN7H			2-265
NBMCIND:0x18	MC_MISC_CNTL			2-153
NBMCIND:0x1B	NB_MEM_CH_CNTL2			2-181
NBMCIND:0x1C	NB_MEM_CH_CNTL0			2-181
NBMCIND:0x1D	NB_MEM_CH_CNTL1			2-182
NBMCIND:0x1F	NB_MC_DEBUG			2-154
NBMCIND:0x2B	GART_FEATURE_ID			2-155
NBMCIND:0x2E	GART_CACHE_CNTRL			2-157
NBMCIND:0x3A	AIC_CTRL_SCRATCH			2-160
NBMCIND:0x4E	MC_MISC_CNTL2			2-161
NBMCIND:0x4F	MC_MISC_CNTL3			2-182
NBMCIND:0x5F	MC_MISC_UMA_CNTL			2-162
NBMCIND:0x63	K8_DRAM_CS0_BASE			2-162
NBMCIND:0x64	K8_DRAM_CS1_BASE			2-163
NBMCIND:0x65	K8_DRAM_CS2_BASE			2-163
NBMCIND:0x66	K8_DRAM_CS3_BASE			2-163
NBMCIND:0x67	K8_DRAM_CS4_BASE			2-164
NBMCIND:0x68	K8_DRAM_CS5_BASE			2-164
NBMCIND:0x69	K8_DRAM_CS6_BASE			2-164

Table 2-3 All Registers Sorted By Address

Address	Name	Secondary Address	Additional Address	Page
NBMCIND:0x6A	*K8_DRAM_CS7_BASE*			*2-165*
NBMCIND:0x6B	*K8_DRAM_CS0_MASK*			*2-165*
NBMCIND:0x6C	*K8_DRAM_CS1_MASK*			*2-165*
NBMCIND:0x6D	*K8_DRAM_CS2_MASK*			*2-165*
NBMCIND:0x6E	*K8_DRAM_CS3_MASK*			*2-166*
NBMCIND:0x6F	*K8_DRAM_CS4_MASK*			*2-166*
NBMCIND:0x70	*K8_DRAM_CS5_MASK*			*2-166*
NBMCIND:0x74	*MC_MPLL_CONTROL*			*2-169*
NBMCIND:0x75	*MC_MPLL_CONTROL2*			*2-169*
NBMCIND:0x76	*MC_MPLL_CONTROL3*			*2-170*
NBMCIND:0x77	*MC_MPLL_FREQ_CONTROL*			*2-170*
NBMCIND:0x78	*MC_MPLL_SEQ_CONTROL*			*2-171*
NBMCIND:0x79	*MC_MPLL_DIV_CONTROL*			*2-171*
NBMCIND:0x7A	*MC_MCLK_CONTROL*			*2-172*
NBMCIND:0x80	*MC_UMA_WC_GRP_TMR*			*2-174*
NBMCIND:0x80	*MC_UMA_WC_GRP_TMR*			*2-182*
NBMCIND:0x81	*MC_UMA_WC_GRP_CNTL*			*2-175*
NBMCIND:0x81	*MC_UMA_WC_GRP_CNTL*			*2-183*
NBMCIND:0x82	*MC_UMA_RW_GRP_TMR*			*2-176*
NBMCIND:0x82	*MC_UMA_RW_GRP_TMR*			*2-184*
NBMCIND:0x83	*MC_UMA_RW_G3DR_GRP_CNTL*			*2-176*
NBMCIND:0x83	*MC_UMA_RW_G3DR_GRP_CNTL*			*2-185*
NBMCIND:0x84	*MC_UMA_RW_TXR_E2R_GRP_CNTL*			*2-178*
NBMCIND:0x84	*MC_UMA_RW_TXR_E2R_GRP_CNTL*			*2-187*
NBMCIND:0x85	*MC_UMA_AGP_GRP_CNTL*			*2-179*
NBMCIND:0x85	*MC_UMA_AGP_GRP_CNTL*			*2-189*
NBMCIND:0x86	*MC_UMA_DUALCH_CNTL*			*2-180*
NBMCIND:0x86	*MC_UMA_DUALCH_CNTL*			*2-190*
NBMCIND:0x90	*MC_SYSTEM_STATUS*			*2-191*
NBMCIND:0x91	*MC_INTFC_GENERAL_PURPOSE*			*2-192*
NBMCIND:0x92	*MC_INTFC_IMP_CTRL_CNTL*			*2-193*
NBMCIND:0x93	*MC_INTFC_IMP_CTRL_REF*			*2-193*
NBMCIND:0x94	*MC_LATENCY_COUNT_CNTL*			*2-194*
NBMCIND:0x95	*MC_LATENCY_COUNT_EVENT*			*2-194*
NBMCIND:0x96	*MCS_PERF_COUNT0*			*2-194*
NBMCIND:0x97	*MCS_PERF_COUNT1*			*2-194*
NBMCIND:0x98	*MCS_PERF_CNTL*			*2-195*
NBMCIND:0x99	*MC_AZ_DEFAULT_ADDR*			*2-195*
NBMCIND:0xA0	*MCA_MEMORY_INIT_MRS*			*2-195*
NBMCIND:0xA1	*MCA_MEMORY_INIT_EMRS*			*2-196*
NBMCIND:0xA2	*MCA_MEMORY_INIT_EMRS2*			*2-196*

Table 2-3 All Registers Sorted By Address

Address	Name	Secondary Address	Additional Address	Page
NBMCIND:0xA3	MCA_MEMORY_INIT_EMRS3			2-197
NBMCIND:0xA4	MCA_MEMORY_INIT_SEQUENCE_1			2-198
NBMCIND:0xA5	MCA_MEMORY_INIT_SEQUENCE_2			2-199
NBMCIND:0xA6	MCA_MEMORY_INIT_SEQUENCE_3			2-200
NBMCIND:0xA7	MCA_MEMORY_INIT_SEQUENCE_4			2-201
NBMCIND:0xA8	MCA_TIMING_PARAMETERS_1			2-202
NBMCIND:0xA9	MCA_TIMING_PARAMETERS_2			2-203
NBMCIND:0xAA	MCA_TIMING_PARAMETERS_3			2-204
NBMCIND:0xAB	MCA_TIMING_PARAMETERS_4			2-205
NBMCIND:0xAC	MCA_MEMORY_TYPE			2-206
NBMCIND:0xAD	MCA_CKE_MUX_SELECT			2-206
NBMCIND:0xAE	MCA_ODT_MUX_SELECT			2-207
NBMCIND:0xAF	MCA_SEQ_PERF_CNTL			2-208
NBMCIND:0xB0	MCA_SEQ_CONTROL			2-209
NBMCIND:0xB1	MCA_RECEIVING			2-211
NBMCIND:0xB2	MCA_IN_TIMING_DQS_3210			2-212
NBMCIND:0xB3	MCA_IN_TIMING_DQS_7654			2-214
NBMCIND:0xB4	MCA_DRIVING			2-216
NBMCIND:0xB5	MCA_OUT_TIMING			2-217
NBMCIND:0xB6	MCA_OUT_TIMING_DQ			2-219
NBMCIND:0xB7	MCA_OUT_TIMING_DQS			2-221
NBMCIND:0xB8	MCA_STRENGTH_N			2-222
NBMCIND:0xB9	MCA_STRENGTH_P			2-223
NBMCIND:0xBA	MCA_STRENGTH_STEP			2-223
NBMCIND:0xBB	MCA_STRENGTH_READ_BACK_N			2-225
NBMCIND:0xBC	MCA_STRENGTH_READ_BACK_P			2-226
NBMCIND:0xBD	MCA_PREAMP			2-226
NBMCIND:0xBE	MCA_PREAMP_N			2-229
NBMCIND:0xBF	MCA_PREAMP_P			2-230
NBMCIND:0xC0	MCA_PREAMP_STEP			2-230
NBMCIND:0xC1	MCA_PREBUF_SLEW_N			2-232
NBMCIND:0xC2	MCA_PREBUF_SLEW_P			2-233
NBMCIND:0xC3	MCA_GENERAL_PURPOSE			2-233
NBMCIND:0xC4	MCA_GENERAL_PURPOSE_2			2-234
NBMCIND:0xC5	MCA_OCD_CONTROL			2-234
NBMCIND:0xC6	MCA_DQ_DQS_READ_BACK			2-235
NBMCIND:0xC7	MCA_DQS_CLK_READ_BACK			2-235
NBMCIND:0xC8	MCA_MEMORY_INIT_MRS_PM			2-237
NBMCIND:0xC9	MCA_MEMORY_INIT_EMRS_PM			2-237
NBMCIND:0xCA	MCA_MEMORY_INIT_EMRS2_PM			2-238
NBMCIND:0xCB	MCA_MEMORY_INIT_EMRS3_PM			2-239

Table 2-3 All Registers Sorted By Address

Address	Name	Secondary Address	Additional Address	Page
NBMCIND:0xCC	*MCA_TIMING_PARAMETERS_1_PM*			*2-239*
NBMCIND:0xCD	*MCA_TIMING_PARAMETERS_2_PM*			*2-241*
NBMCIND:0xCE	*MCA_TIMING_PARAMETERS_3_PM*			*2-242*
NBMCIND:0xCF	*MCA_TIMING_PARAMETERS_4_PM*			*2-243*
NBMCIND:0xD0	*MCA_IN_TIMING_DQS_3210_PM*			*2-244*
NBMCIND:0xD1	*MCA_IN_TIMING_DQS_7654_PM*			*2-246*
NBMCIND:0xD2	*MCA_OUT_TIMING_DQ_PM*			*2-248*
NBMCIND:0xD3	*MCA_OUT_TIMING_DQS_PM*			*2-250*
NBMCIND:0xD4	*MCA_MISCELLANEOUS*			*2-251*
NBMCIND:0xD5	*MCA_MISCELLANEOUS_2*			*2-251*
NBMCIND:0xD6	*MCA_MX1X2X_DQ*			*2-252*
NBMCIND:0xD7	*MCA_MX1X2X_DQS*			*2-253*
NBMCIND:0xD8	*MCA_DLL_MASTER_0*			*2-253*
NBMCIND:0xD9	*MCA_DLL_MASTER_1*			*2-254*
NBMCIND:0xE0	*MCA_DLL_SLAVE_RD_0*			*2-254*
NBMCIND:0xE1	*MCA_DLL_SLAVE_RD_1*			*2-254*
NBMCIND:0xE8	*MCA_DLL_SLAVE_WR_0*			*2-254*
NBMCIND:0xE9	*MCA_DLL_SLAVE_WR_1*			*2-255*
NBMCIND:0xF0	*MCA_RESERVED_0*			*2-255*
NBMCIND:0xF1	*MCA_RESERVED_1*			*2-255*
NBMCIND:0xF2	*MCA_RESERVED_2*			*2-255*
NBMCIND:0xF3	*MCA_RESERVED_3*			*2-255*
NBMCIND:0xF4	*MCA_RESERVED_4*			*2-255*
NBMCIND:0xF5	*MCA_RESERVED_5*			*2-256*
NBMCIND:0xF6	*MCA_RESERVED_6*			*2-256*
NBMCIND:0xF7	*MCA_RESERVED_7*			*2-256*
NBMCIND:0xF8	*MCA_RESERVED_8*			*2-256*
NBMCIND:0xF9	*MCA_RESERVED_9*			*2-256*
NBMCIND:0xFA	*MCA_RESERVED_A*			*2-256*
NBMCIND:0xFB	*MCA_RESERVED_B*			*2-256*
NBMCIND:0xFC	*MCA_RESERVED_C*			*2-257*
NBMCIND:0xFD	*MCA_RESERVED_D*			*2-257*
NBMCIND:0xFE	*MCA_RESERVED_E*			*2-257*
NBMCIND:0xFF	*MCA_RESERVED_F*			*2-257*
NBMCIND\:0x1E	*K8_FB_LOCATION*			*2-154*
NBMCIND\:0x26	*MC_PM_CNTL*			*2-154*
NBMCIND\:0x2C	*GART_BASE*			*2-157*
NBMCIND\:0x2D	*GART_CACHE_SZBASE*			*2-157*
NBMCIND\:0x2F	*GART_CACHE_ENTRY_CNTRL*			*2-157*
NBMCIND\:0x30	*GART_ERROR_0*			*2-158*
NBMCIND\:0x31	*GART_ERROR_1*			*2-158*

Table 2-3 All Registers Sorted By Address

Address	Name	Secondary Address	Additional Address	Page
NBMCIND\:0x32	GART_ERROR_2			2-158
NBMCIND\:0x33	GART_ERROR_3			2-158
NBMCIND\:0x34	GART_ERROR_4			2-159
NBMCIND\:0x35	GART_ERROR_5			2-159
NBMCIND\:0x36	GART_ERROR_6			2-159
NBMCIND\:0x37	GART_ERROR_7			2-159
NBMCIND\:0x38	AGP_ADDRESS_SPACE_SIZE			2-160
NBMCIND\:0x39	AGP_MODE_CONTROL			2-160
NBMCIND\:0x3B	MC_GART_ERROR_ADDRESS			2-161
NBMCIND\:0x3C	MC_GART_ERROR_ADDRESS_HI			2-161
NBMCIND\:0x71	K8_DRAM_CS6_MASK			2-166
NBMCIND\:0x72	K8_DRAM_CS7_MASK			2-167
NBMCIND\:0x73	K8_DRAM_BANK_ADDR_MAPPING			2-167
NBMCIND\:0x7B	MC_UMA_HDR_LAT_INIT			2-172
NBMCIND\:0x7C	MC_UMA_GRP_CNTL			2-172
NBMCIND\:0x7D	MC_UMA_GRP_TMR			2-173
NBMCIND\:0x7E	MC_MISC_UMA_CNTL2			2-173
NBMISCIND:0x1	NB_IOC_DEBUG			2-27
NBMISCIND:0x10	DFT_CNTL2			2-28
NBMISCIND:0x16	NB_TOM_PCI			2-28
NBMISCIND:0x17	NB_MMIOBASE			2-28
NBMISCIND:0x18	NB_MMIOLIMIT			2-28
NBMISCIND:0x1F	NB_INTERRUPT_PIN			2-28
NBMISCIND:0x20	NB_PROG_DEVICE_REMAP_0			2-29
NBMISCIND:0x30	IOC_LAT_PERF_CNTR_CNTL			2-29
NBMISCIND:0x31	IOC_LAT_PERF_CNTR_OUT			2-29
NBMISCIND:0x32	PCIE_NBCFG_REG0			2-11
NBMISCIND:0x33	PCIE_NBCFG_REG3			2-12
NBMISCIND:0x34	PCIE_NBCFG_REG4			2-12
NBMISCIND:0x35	PCIE_NBCFG_REG5			2-13
NBMISCIND:0x36	PCIE_NBCFG_REG6			2-13
NBMISCIND:0x37	PCIE_NBCFG_REG7			2-13
NBMISCIND:0x38	PCIE_NBCFG_REG8			2-14
NBMISCIND:0x39	PCIE_STRAP_REG2			2-14
NBMISCIND:0x39	PCIE_STRAP_REG2			2-29
NBMISCIND:0x3A	NB_BROADCAST_BASE_LO			2-29
NBMISCIND:0x3B	NB_BROADCAST_BASE_HI			2-29
NBMISCIND:0x3C	NB_BROADCAST_CNTL			2-30
NBMISCIND:0x3D	NB_APIC_P2P_CNTL			2-30
NBMISCIND:0x3E	NB_APIC_P2P_RANGE_0			2-30
NBMISCIND:0x3F	NB_APIC_P2P_RANGE_1			2-30

Table 2-3 All Registers Sorted By Address

Address	Name	Secondary Address	Additional Address	Page
NBMISCIND:0x40	GPIO_PAD			2-31
NBMISCIND:0x41	GPIO_PAD_CNTL_PU_PD			2-31
NBMISCIND:0x42	GPIO_PAD_SCHMEM_OE			2-32
NBMISCIND:0x43	GPIO_PAD_SP_SN			2-32
NBMISCIND:0x44	DFT_VIP_IO_GPIO			2-32
NBMISCIND:0x45	DFT_VIP_IO_GPIO_OR			2-33
NBMISCIND:0x5	DFT_CNTL0			2-27
NBMISCIND:0x50	IOC_PCIE_D2_CSR_Count			2-34
NBMISCIND:0x51	IOC_PCIE_D2_CNTL			2-34
NBMISCIND:0x52	IOC_PCIE_D3_CSR_Count			2-34
NBMISCIND:0x53	IOC_PCIE_D3_CNTL			2-35
NBMISCIND:0x54	IOC_PCIE_D4_CSR_Count			2-35
NBMISCIND:0x55	IOC_PCIE_D4_CNTL			2-35
NBMISCIND:0x56	IOC_PCIE_D5_CSR_Count			2-35
NBMISCIND:0x57	IOC_PCIE_D5_CNTL			2-36
NBMISCIND:0x58	IOC_PCIE_D6_CSR_Count			2-36
NBMISCIND:0x59	IOC_PCIE_D6_CNTL			2-36
NBMISCIND:0x5A	IOC_PCIE_D7_CSR_Count			2-37
NBMISCIND:0x5B	IOC_PCIE_D7_CNTL			2-37
NBMISCIND:0x6	DFT_CNTL1			2-27
NBMISCIND:0x60	StrapsOutputMux_0			2-37
NBMISCIND:0x61	StrapsOutputMux_1			2-37
NBMISCIND:0x62	StrapsOutputMux_2			2-37
NBMISCIND:0x63	StrapsOutputMux_3			2-38
NBMISCIND:0x64	StrapsOutputMux_4			2-38
NBMISCIND:0x65	StrapsOutputMux_5			2-38
NBMISCIND:0x66	StrapsOutputMux_6			2-38
NBMISCIND:0x67	StrapsOutputMux_7			2-39
NBMISCIND:0x68	StrapsOutputMux_8			2-39
NBMISCIND:0x69	StrapsOutputMux_9			2-40
NBMISCIND:0x6A	StrapsOutputMux_A			2-40
NBMISCIND:0x6B	StrapsOutputMux_B			2-40
NBMISCIND:0x6C	StrapsOutputMux_C			2-40
NBMISCIND:0x6D	StrapsOutputMux_D			2-40
NBMISCIND:0x6E	StrapsOutputMux_E			2-41
NBMISCIND:0x6F	StrapsOutputMux_F			2-41
NBMISCIND:0x7	PCIE_PDNB_CNTL			2-25
NBMISCIND:0x70	scratch_0			2-41
NBMISCIND:0x71	scratch_1			2-41
NBMISCIND:0x72	scratch_2			2-41
NBMISCIND:0x73	scratch_3			2-41

Table 2-3 All Registers Sorted By Address

Address	Name	Secondary Address	Additional Address	Page
NBMISCIND:0x74	SCRATCH_4			2-41
NBMISCIND:0x75	SCRATCH_5			2-42
NBMISCIND:0x76	SCRATCH_6			2-42
NBMISCIND:0x77	SCRATCH_7			2-42
NBMISCIND:0x78	SCRATCH_8			2-42
NBMISCIND:0x79	SCRATCH_9			2-42
NBMISCIND:0x7A	SCRATCH_A			2-42
NBMISCIND:0x7F	DFT_SPARE			2-43
NBMISCIND:0x8	PCIE_LINK_CFG			2-9
NBMISCIND:0xB	IOC_PCIE_CNTL			2-10
NBMISCIND:0xC	IOC_P2P_CNTL			2-11
NBMISCIND:0xE	IOCIsocMapAddr_LO			2-27
NBMISCIND:0xF	IOCIsocMapAddr_HI			2-28
NBMISCIND\:0x0	NB_CNTL			2-8
NBMISCIND\:0x2	NB_SPARE1			2-8
NBMISCIND\:0x3	NB_STRAPS_READBACK_MUX			2-9
NBMISCIND\:0x4	NB_STRAPS_READBACK_DATA			2-9
NBMISCIND\:0x9	IOC_DMA_ARBITER			2-10
NBMISCIND\:0xA	IOC_PCIE_CSR_Count			2-10
pcieConfigDev[10:2]\:0x0	PCIE_VENDOR_ID			2-72
pcieConfigDev[10:2]\:0x100	PCIE_VC_ENH_CAP_HDR			2-108
pcieConfigDev[10:2]\:0x104	PCIE_PORT_VC_CAP_REG1			2-108
pcieConfigDev[10:2]\:0x108	PCIE_PORT_VC_CAP_REG2			2-108
pcieConfigDev[10:2]\:0x10C	PCIE_PORT_VC_CNTL			2-108
pcieConfigDev[10:2]\:0x10E	PCIE_PORT_VC_STATUS			2-109
pcieConfigDev[10:2]\:0x110	PCIE_VC0_RESOURCE_CAP			2-93
pcieConfigDev[10:2]\:0x114	PCIE_VC0_RESOURCE_CNTL			2-94
pcieConfigDev[10:2]\:0x11A	PCIE_VC0_RESOURCE_STATUS			2-94
pcieConfigDev[10:2]\:0x11C	PCIE_VC1_RESOURCE_CAP			2-109
pcieConfigDev[10:2]\:0x120	PCIE_VC1_RESOURCE_CNTL			2-109
pcieConfigDev[10:2]\:0x124	PCIE_VC1_RESOURCE_STATUS			2-109

Table 2-3 All Registers Sorted By Address

Address	Name	Secondary Address	Additional Address	Page
pcieConfigDev[10:2]\:0x 140	*PCIE_ENH_ADV_ERR_RPT_CAP_HDR*			*2-89*
pcieConfigDev[10:2]\:0x 144	*PCIE_UNCORR_ERR_STATUS*			*2-89*
pcieConfigDev[10:2]\:0x 148	*PCIE_UNCORR_ERR_MASK*			*2-90*
pcieConfigDev[10:2]\:0x 14C	*PCIE_UNCORR_ERR_SEVERITY*			*2-90*
pcieConfigDev[10:2]\:0x 150	*PCIE_CORR_ERR_STATUS*			*2-90*
pcieConfigDev[10:2]\:0x 154	*PCIE_CORR_ERR_MASK*			*2-91*
pcieConfigDev[10:2]\:0x 158	*PCIE_ADV_ERR_CAP_CNTL*			*2-91*
pcieConfigDev[10:2]\:0x 15C	*PCIE_HDR_LOG0*			*2-91*
pcieConfigDev[10:2]\:0x 160	*PCIE_HDR_LOG1*			*2-91*
pcieConfigDev[10:2]\:0x 164	*PCIE_HDR_LOG2*			*2-92*
pcieConfigDev[10:2]\:0x 168	*PCIE_HDR_LOG3*			*2-92*
pcieConfigDev[10:2]\:0x 16C	*PCIE_ROOT_ERR_CMD*			*2-92*
pcieConfigDev[10:2]\:0x 170	*PCIE_ROOT_ERR_STATUS*			*2-92*
pcieConfigDev[10:2]\:0x 174	*PCIE_ERR_SRC_ID*			*2-93*
pcieConfigDev[10:2]\:0x 18	*SUB_BUS_NUMBER_LATENCY*			*2-75*
pcieConfigDev[10:2]\:0x 1C	*IO_BASE_LIMIT*			*2-76*
pcieConfigDev[10:2]\:0x 1E	*SECONDARY_STATUS*			*2-76*
pcieConfigDev[10:2]\:0x 2	*PCIE_DEVICE_ID*			*2-73*
pcieConfigDev[10:2]\:0x 20	*MEM_BASE_LIMIT*			*2-77*
pcieConfigDev[10:2]\:0x 24	*PREF_BASE_LIMIT*			*2-77*
pcieConfigDev[10:2]\:0x 28	*PREF_BASE_UPPER*			*2-77*
pcieConfigDev[10:2]\:0x 2C	*PREF_LIMIT_UPPER*			*2-77*
pcieConfigDev[10:2]\:0x 30	*IO_BASE_LIMIT_HI*			*2-77*

Table 2-3 All Registers Sorted By Address

Address	Name	Secondary Address	Additional Address	Page
pcieConfigDev[10:2]\:0x34	*CAP_PTR*			*2-78*
pcieConfigDev[10:2]\:0x3C	*PCIE_INTERRUPT_LINE*			*2-78*
pcieConfigDev[10:2]\:0x3D	*PCIE_INTERRUPT_PIN*			*2-78*
pcieConfigDev[10:2]\:0x3E	*IRQ_BRIDGE_CNTL*			*2-78*
pcieConfigDev[10:2]\:0x4	*PCIE_COMMAND*			*2-73*
pcieConfigDev[10:2]\:0x50	*PMI_CAP_LIST*			*2-79*
pcieConfigDev[10:2]\:0x52	*PMI_CAP*			*2-79*
pcieConfigDev[10:2]\:0x54	*PMI_STATUS_CNTL*			*2-79*
pcieConfigDev[10:2]\:0x58	*PCIE_CAP_LIST*			*2-80*
pcieConfigDev[10:2]\:0x5A	*PCIE_CAP*			*2-80*
pcieConfigDev[10:2]\:0x5C	*DEVICE_CAP*			*2-80*
pcieConfigDev[10:2]\:0x6	*PCIE_STATUS*			*2-73*
pcieConfigDev[10:2]\:0x60	*DEVICE_CNTL*			*2-81*
pcieConfigDev[10:2]\:0x62	*DEVICE_STATUS*			*2-82*
pcieConfigDev[10:2]\:0x64	*LINK_CAP*			*2-82*
pcieConfigDev[10:2]\:0x68	*LINK_CNTL*			*2-83*
pcieConfigDev[10:2]\:0x6A	*LINK_STATUS*			*2-83*
pcieConfigDev[10:2]\:0x6C	*SLOT_CAP*			*2-84*
pcieConfigDev[10:2]\:0x70	*SLOT_CNTL*			*2-84*
pcieConfigDev[10:2]\:0x72	*SLOT_STATUS*			*2-85*
pcieConfigDev[10:2]\:0x74	*ROOT_CNTL*			*2-85*
pcieConfigDev[10:2]\:0x74	*ROOT_CNTL*			*2-107*
pcieConfigDev[10:2]\:0x76	*ROOT_CAP*			*2-107*

Table 2-3 All Registers Sorted By Address

Address	Name	Secondary Address	Additional Address	Page
pcieConfigDev[10:2]\:0x78	*ROOT_STATUS*			*2-86*
pcieConfigDev[10:2]\:0x8	*PCIE_REVISION_ID*			*2-74*
pcieConfigDev[10:2]\:0x80	*MSI_CAP_LIST*			*2-86*
pcieConfigDev[10:2]\:0x80	*MSI_CAP_LIST*			*2-107*
pcieConfigDev[10:2]\:0x82	*PCIE_MSI_MSG_CNTL*			*2-86*
pcieConfigDev[10:2]\:0x84	*PCIE_MSI_MSG_ADDR_LO*			*2-87*
pcieConfigDev[10:2]\:0x88	*PCIE_MSI_MSG_ADDR_HI*			*2-87*
pcieConfigDev[10:2]\:0x88	*PCIE_MSI_MSG_DATA*			*2-87*
pcieConfigDev[10:2]\:0x8C	*PCIE_MSI_MSG_DATA_64*			*2-87*
pcieConfigDev[10:2]\:0x9	*PCIE_REGPROG_INF*			*2-74*
pcieConfigDev[10:2]\:0x90	*CRS_TIMER*			*2-87*
pcieConfigDev[10:2]\:0x94	*IOC_CNTL*			*2-88*
pcieConfigDev[10:2]\:0xA	*PCIE_SUB_CLASS*			*2-74*
pcieConfigDev[10:2]\:0xB	*PCIE_BASE_CODE*			*2-74*
pcieConfigDev[10:2]\:0xB0	*SSID_CAP_LIST*			*2-88*
pcieConfigDev[10:2]\:0xB4	*SSID_ID*			*2-88*
pcieConfigDev[10:2]\:0xB8	*MSI_MAP*			*2-88*
pcieConfigDev[10:2]\:0xC	*PCIE_CACHE_LINE*			*2-74*
pcieConfigDev[10:2]\:0xC0	*PCIE_CFG_SCRATCH*			*2-107*
pcieConfigDev[10:2]\:0xD	*PCIE_LATENCY*			*2-75*
pcieConfigDev[10:2]\:0xE	*PCIE_HEADER*			*2-75*
pcieConfigDev[10:2]\:0xE0	*PCIE_PORT_INDEX*			*2-89*
pcieConfigDev[10:2]\:0xE4	*PCIE_PORT_DATA*			*2-89*

Table 2-3 All Registers Sorted By Address

Address	Name	Secondary Address	Additional Address	Page
pcieConfigDev[10:2]\:0x F	*PCIE_BIST*			*2-75*
PCIEIND:0x10	*PCIE_CNTL*			*2-58*
PCIEIND:0x12	*PCIE_DEBUG_CNTL*			*2-94*
PCIEIND:0x20	*PCIE_CI_CNTL*			*2-59*
PCIEIND:0x30	*PCIE_WPR_CNTL*			*2-95*
PCIEIND:0x40	*PCIE_P_CNTL*			*2-60*
PCIEIND:0x70	*PCIE_PERF_LATENCY_CNTL*			*2-95*
PCIEIND:0x71	*PCIE_PERF_LATENCY_REQ_ID*			*2-96*
PCIEIND:0x72	*PCIE_PERF_LATENCY_TAG*			*2-96*
PCIEIND:0x73	*PCIE_PERF_LATENCY_THRESHOLD*			*2-96*
PCIEIND:0x74	*PCIE_PERF_LATENCY_MAX*			*2-96*
PCIEIND:0x75	*PCIE_PERF_LATENCY_TIMER_LO*			*2-96*
PCIEIND:0x76	*PCIE_PERF_LATENCY_TIMER_HI*			*2-97*
PCIEIND:0x77	*PCIE_PERF_LATENCY_COUNTER0*			*2-97*
PCIEIND:0x78	*PCIE_PERF_LATENCY_COUNTER1*			*2-97*
PCIEIND:0xD0	*PCIE_PRBS23_BITCNT_0*			*2-97*
PCIEIND:0xD1	*PCIE_PRBS23_BITCNT_1*			*2-97*
PCIEIND:0xD2	*PCIE_PRBS23_BITCNT_2*			*2-97*
PCIEIND:0xD3	*PCIE_PRBS23_BITCNT_3*			*2-97*
PCIEIND:0xD4	*PCIE_PRBS23_BITCNT_4*			*2-98*
PCIEIND:0xD5	*PCIE_PRBS23_BITCNT_5*			*2-98*
PCIEIND:0xD6	*PCIE_PRBS23_BITCNT_6*			*2-98*
PCIEIND:0xD7	*PCIE_PRBS23_BITCNT_7*			*2-98*
PCIEIND:0xD8	*PCIE_PRBS23_BITCNT_8*			*2-98*
PCIEIND:0xD9	*PCIE_PRBS23_BITCNT_9*			*2-98*
PCIEIND:0xDA	*PCIE_PRBS23_BITCNT_10*			*2-98*
PCIEIND:0xDB	*PCIE_PRBS23_BITCNT_11*			*2-99*
PCIEIND:0xDC	*PCIE_PRBS23_BITCNT_12*			*2-99*
PCIEIND:0xDD	*PCIE_PRBS23_BITCNT_13*			*2-99*
PCIEIND:0xDE	*PCIE_PRBS23_BITCNT_14*			*2-99*
PCIEIND:0xDF	*PCIE_PRBS23_BITCNT_15*			*2-99*
PCIEIND:0xE0	*PCIE_PRBS23_ERRCNT_0*			*2-99*
PCIEIND:0xE1	*PCIE_PRBS23_ERRCNT_1*			*2-99*
PCIEIND:0xE2	*PCIE_PRBS23_ERRCNT_2*			*2-100*
PCIEIND:0xE3	*PCIE_PRBS23_ERRCNT_3*			*2-100*
PCIEIND:0xE4	*PCIE_PRBS23_ERRCNT_4*			*2-100*
PCIEIND:0xE5	*PCIE_PRBS23_ERRCNT_5*			*2-100*
PCIEIND:0xE6	*PCIE_PRBS23_ERRCNT_6*			*2-100*
PCIEIND:0xE7	*PCIE_PRBS23_ERRCNT_7*			*2-100*
PCIEIND:0xE8	*PCIE_PRBS23_ERRCNT_8*			*2-100*

Table 2-3 All Registers Sorted By Address

Address	Name	Secondary Address	Additional Address	Page
PCIEIND:0xE9	PCIE_PRBS23_ERRCNT_9			2-101
PCIEIND:0xEA	PCIE_PRBS23_ERRCNT_10			2-101
PCIEIND:0xEB	PCIE_PRBS23_ERRCNT_11			2-101
PCIEIND:0xEC	PCIE_PRBS23_ERRCNT_12			2-101
PCIEIND:0xED	PCIE_PRBS23_ERRCNT_13			2-101
PCIEIND:0xEE	PCIE_PRBS23_ERRCNT_14			2-101
PCIEIND:0xEF	PCIE_PRBS23_ERRCNT_15			2-101
PCIEIND:0xF0	PCIE_PRBS23_CLR			2-102
PCIEIND:0xF1	PCIE_PRBS23_ERRSTAT			2-102
PCIEIND:0xF2	PCIE_PRBS23_LOCKED			2-102
PCIEIND:0xF3	PCIE_PRBS23_FREERUN			2-102
PCIEIND:0xF4	PCIE_PRBS23_LOCK_CNT			2-102
PCIEIND:0xF5	PCIE_PRBS23_EN			2-102
PCIEIND:0xF6	PCIE_P90RX_PRBS_CLR			2-102
PCIEIND:0xF7	PCIE_P90_BRX_PRBS_ER			2-103
PCIEIND:0xF8	PCIE_P90TX_PRBS_EN			2-103
PCIEIND:0xF9	PCIE_B_P90_CNTL			2-103
PCIEIND\:0x0	PCIE_RESERVED			2-58
PCIEIND\:0x1	PCIE_SCRATCH			2-58
PCIEIND\:0x11	PCIE_CONFIG_CNTL			2-58
PCIEIND\:0x21	PCIE_BUS_CNTL			2-59
PCIEIND\:0x41	PCIE_P_BUF_STATUS			2-61
PCIEIND\:0x42	PCIE_P_DECODER_STATUS			2-62
PCIEIND\:0x44	PCIE_P_PLL_CNTL			2-63
PCIEIND\:0x60	PCIE_P_IMP_CNTL_STRENGTH			2-63
PCIEIND\:0x61	PCIE_P_IMP_CNTL_UPDATE			2-64
PCIEIND\:0x62	PCIE_P_STR_CNTL_UPDATE			2-64
PCIEIND\:0x63	PCIE_P_PAD_MISC_CNTL			2-64
PCIEIND\:0x64	PCIE_P_PAD_FORCE_EN			2-64
PCIEIND\:0x65	PCIE_P_PAD_FORCE_DIS			2-65
PCIEIND_P:0x10	PCIEP_PORT_CNTL			2-65
PCIEIND_P:0x20	PCIE_TX_CNTL			2-66
PCIEIND_P:0x21	PCIE_TX_REQUESTER_ID			2-66
PCIEIND_P:0x22	PCIE_TX_VENDOR_SPECIFIC			2-67
PCIEIND_P:0x22	PCIE_TX_VENDOR_SPECIFIC			2-103
PCIEIND_P:0x23	PCIE_TX_REQUEST_NUM_CNTL			2-67
PCIEIND_P:0x24	PCIE_TX_SEQ			2-67
PCIEIND_P:0x25	PCIE_TX_REPLAY			2-67
PCIEIND_P:0x26	PCIE_TX_ACK_LATENCY_LIMIT			2-67
PCIEIND_P:0x26	PCIE_TX_ACK_LATENCY_LIMIT			2-103
PCIEIND_P:0x30	PCIE_TX_CREDITS_CONSUMED_P			2-103

Table 2-3 All Registers Sorted By Address

Address	Name	Secondary Address	Additional Address	Page
PCIEIND_P:0x31	PCIE_TX_CREDITS_CONSUMED_NP			2-104
PCIEIND_P:0x32	PCIE_TX_CREDITS_CONSUMED_CPL			2-104
PCIEIND_P:0x33	PCIE_TX_CREDITS_LIMIT_P			2-104
PCIEIND_P:0x34	PCIE_TX_CREDITS_LIMIT_NP			2-104
PCIEIND_P:0x35	PCIE_TX_CREDITS_LIMIT_CPL			2-105
PCIEIND_P:0x70	PCIE_RX_CNTL			2-69
PCIEIND_P:0x72	PCIE_RX_VENDOR_SPECIFIC			2-105
PCIEIND_P:0x80	PCIE_RX_CREDITS_ALLOCATED_P			2-105
PCIEIND_P:0x81	PCIE_RX_CREDITS_ALLOCATED_NP			2-105
PCIEIND_P:0x82	PCIE_RX_CREDITS_ALLOCATED_CPL			2-105
PCIEIND_P:0x83	PCIE_RX_CREDITS_RECEIVED_P			2-106
PCIEIND_P:0x84	PCIE_RX_CREDITS_RECEIVED_NP			2-106
PCIEIND_P:0x85	PCIE_RX_CREDITS_RECEIVED_CPL			2-106
PCIEIND_P:0xA0	PCIE_LC_CNTL			2-69
PCIEIND_P:0xA1	PCIE_LC_TRAINING_CNTL			2-72
PCIEIND_P:0xA3	PCIE_LC_N_FTS_CNTL			2-72
PCIEIND_P:0xA3	PCIE_LC_N_FTS_CNTL			2-106
PCIEIND_P\:0x0	PCIEP_RESERVED			2-65
PCIEIND_P\:0x1	PCIEP_SCRATCH			2-65
PCIEIND_P\:0x50	PCIE_P_PORT_LANE_STATUS			2-68
PCIEIND_P\:0x60	PCIE_FC_P			2-68
PCIEIND_P\:0x61	PCIE_FC_NP			2-68
PCIEIND_P\:0x62	PCIE_FC_CPL			2-68
PCIEIND_P\:0x6A	PCIE_ERR_CNTL			2-68
PCIEIND_P\:0x84	PCIE_RX_LASTACK_SEQNUM			2-69
PCIEIND_P\:0xA2	PCIE_LC_LINK_WIDTH_CNTL			2-72
PCIEIND_P\:0xA5	PCIE_LC_STATE0			2-71
PCIEIND_P\:0xA6	PCIE_LC_STATE1			2-71
PCIEIND_P\:0xA7	PCIE_LC_STATE2			2-71
PCIEIND_P\:0xA8	PCIE_LC_STATE3			2-71
PCIEIND_P\:0xA9	PCIE_LC_STATE4			2-71
PCIEIND_P\:0xAA	PCIE_LC_STATE5			2-71
VGA_IO\:0x3BA	GENFC_WT	VGA_IO\:0x3DA		2-297
VGA_IO\:0x3BA	GENS1	VGA_IO\:0x3DA		2-299
VGA_IO\:0x3C0	ATTRDW			2-316
VGA_IO\:0x3C0	ATTRX			2-316
VGA_IO\:0x3C1	ATTRDR			2-316
VGA_IO\:0x3C2	GENMO_WT			2-297
VGA_IO\:0x3C2	GENS0			2-299
VGA_IO\:0x3C3	GENENB			2-127
VGA_IO\:0x3C6	DAC_MASK			2-296

Table 2-3 All Registers Sorted By Address

Address	Name	Secondary Address	Additional Address	Page
VGA_IO\:0x3C7	DAC_R_INDEX			2-296
VGA_IO\:0x3C8	DAC_W_INDEX			2-296
VGA_IO\:0x3C9	DAC_DATA			2-296
VGA_IO\:0x3CA	GENFC_RD			2-297
VGA_IO\:0x3CC	GENMO_RD			2-298
VGAATTRIND\:0x0	ATTR00			2-316
VGAATTRIND\:0x1	ATTR01			2-317
VGAATTRIND\:0x10	ATTR10			2-320
VGAATTRIND\:0x11	ATTR11			2-320
VGAATTRIND\:0x12	ATTR12			2-320
VGAATTRIND\:0x13	ATTR13			2-321
VGAATTRIND\:0x14	ATTR14			2-321
VGAATTRIND\:0x2	ATTR02			2-317
VGAATTRIND\:0x3	ATTR03			2-317
VGAATTRIND\:0x4	ATTR04			2-317
VGAATTRIND\:0x5	ATTR05			2-317
VGAATTRIND\:0x6	ATTR06			2-318
VGAATTRIND\:0x7	ATTR07			2-318
VGAATTRIND\:0x8	ATTR08			2-318
VGAATTRIND\:0x9	ATTR09			2-318
VGAATTRIND\:0xA	ATTR0A			2-318
VGAATTRIND\:0xB	ATTR0B			2-319
VGAATTRIND\:0xC	ATTR0C			2-319
VGAATTRIND\:0xD	ATTR0D			2-319
VGAATTRIND\:0xE	ATTR0E			2-319
VGAATTRIND\:0xF	ATTR0F			2-319
VGACRTIND\:0x0	CRT00			2-303
VGACRTIND\:0x1	CRT01			2-303
VGACRTIND\:0x10	CRT10			2-308
VGACRTIND\:0x11	CRT11			2-308
VGACRTIND\:0x12	CRT12			2-309
VGACRTIND\:0x13	CRT13			2-309
VGACRTIND\:0x14	CRT14			2-309
VGACRTIND\:0x15	CRT15			2-309
VGACRTIND\:0x16	CRT16			2-310
VGACRTIND\:0x17	CRT17			2-310
VGACRTIND\:0x18	CRT18			2-310
VGACRTIND\:0x1E	CRT1E			2-311
VGACRTIND\:0x1F	CRT1F			2-311
VGACRTIND\:0x2	CRT02			2-303
VGACRTIND\:0x22	CRT22			2-311

Table 2-3 All Registers Sorted By Address

Address	Name	Secondary Address	Additional Address	Page
VGACRTIND\:0x3	CRT03			2-304
VGACRTIND\:0x4	CRT04			2-304
VGACRTIND\:0x5	CRT05			2-304
VGACRTIND\:0x6	CRT06			2-305
VGACRTIND\:0x7	CRT07			2-305
VGACRTIND\:0x8	CRT08			2-306
VGACRTIND\:0x9	CRT09			2-306
VGACRTIND\:0xA	CRT0A			2-306
VGACRTIND\:0xB	CRT0B			2-307
VGACRTIND\:0xC	CRT0C			2-307
VGACRTIND\:0xD	CRT0D			2-307
VGACRTIND\:0xE	CRT0E			2-307
VGACRTIND\:0xF	CRT0F			2-308
VGAGRPHIND\:0x0	GRA00			2-312
VGAGRPHIND\:0x1	GRA01			2-312
VGAGRPHIND\:0x2	GRA02			2-313
VGAGRPHIND\:0x3	GRA03			2-313
VGAGRPHIND\:0x4	GRA04			2-313
VGAGRPHIND\:0x5	GRA05			2-314
VGAGRPHIND\:0x6	GRA06			2-314
VGAGRPHIND\:0x7	GRA07			2-315
VGAGRPHIND\:0x8	GRA08			2-315
VGASEQIND\:0x0	SEQ00			2-300
VGASEQIND\:0x1	SEQ01			2-300
VGASEQIND\:0x2	SEQ02			2-300
VGASEQIND\:0x3	SEQ03			2-301
VGASEQIND\:0x4	SEQ04			2-301

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- Open source release.