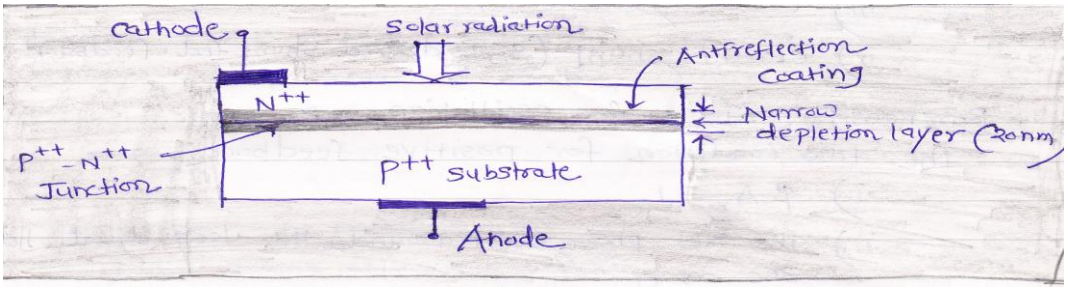
Q1) Attempt any ten of the following:- **(20 marks)**

a) Draw Labelled construction of solar cell.

Ans:- Labelled construction of 'solar cell' **(Diagram 01 mark, labeling 01 mark)**



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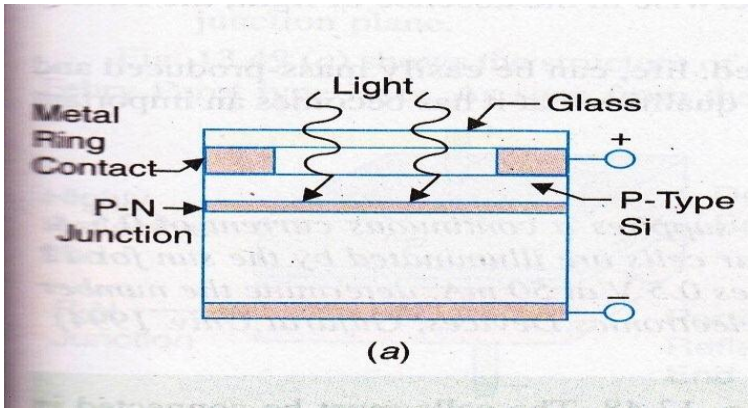

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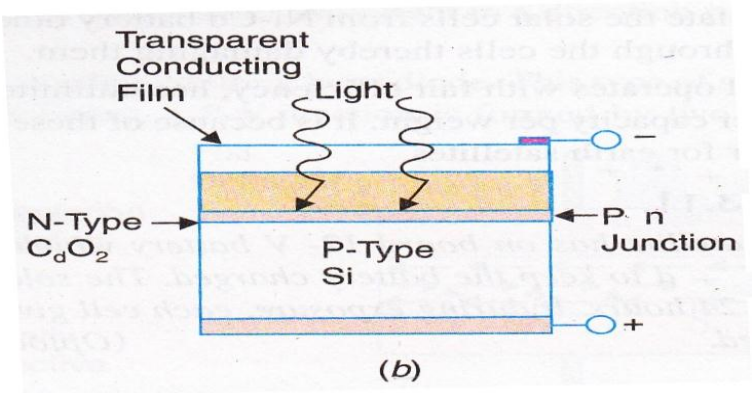


b) State any four applications of Laser diode.

Ans:- Application of 'LASER DIODE' (**Each application ½ marks (any four application)**)

i) Medical equipment used in surgery to consumer product like optical disk equipment.

ii) Laser printers.

iii) Hologram scanner

iv) Laser diodes emitting visible light are used as pointers.

v) Used in parallel processing of information & in parallel interconnections between computers

vi) To measure range or distance.

vii) As light source in fibre optic communication

viii) In the infrared spectrometers

ix) In military application

x) For flow measurement

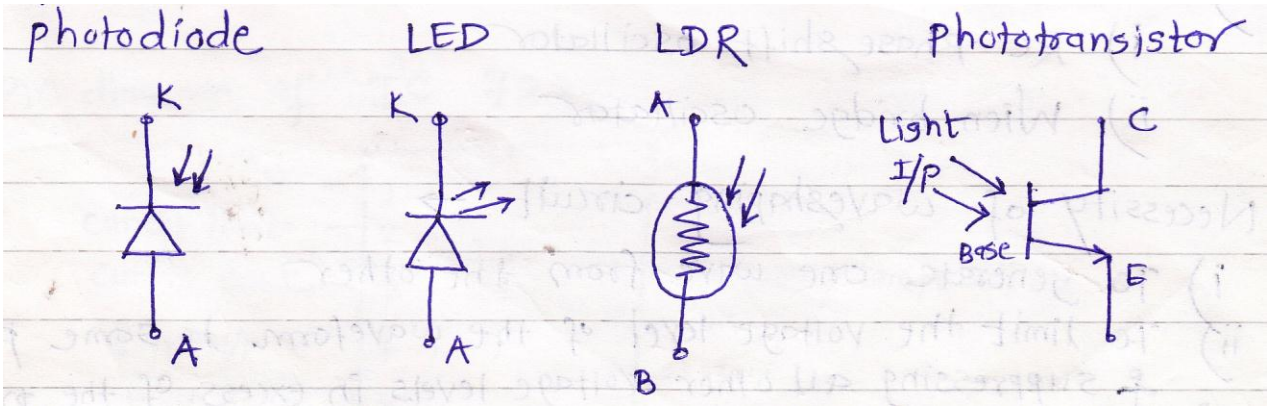
xi) As a sharp cutting tool in machine tool application

xii) In the communication

xiii) For welding

c) Draw Symbol Of Photo diode, LED, LDR, Photo transistor.

Ans:- Symbols of :- **(Each symbol ½ mark)**



d) State the types of feedback connection in negative feedback amplifier.

Ans:- Types of feedback connection in negative feedback amplifier **(½ mark each)**

i) Voltage series or (Shunt derived series fed feedback connection)

ii) Voltage shunt or (shunt derived shunt fed feedback connection)

iii) Current series or (series derived series fed feedback connection)

iv) Current shunt or (series derived shunt fed feedback connection)

e) State Bark hausen criteria for oscillation

Ans:- Bark hausen criteria for oscillation

The two condition for positive feedback

i) $\beta * A_v = 1$ **(01 mark)**

ii) The Net phase shift around the loop equal to 360^0 or 0^0 **(01 mark)**

Mathematically, the bark hausen criterion may be stated as follows

$\beta * A_v = 1$ and

$\angle \beta * A_v = 0^0$

f) State types of LC and RC Oscillator

Ans:- A) Types of LC Oscillator **(any 2, ½ mark each)**

i) Tuned collector or Armstrong oscillator

ii) Tuned Base oscillator

iii) Hartley Oscillator

iv) Colpitts Oscillator

v) Clapp Oscillator

B) Types Of RC Oscillator **(any 2, ½ mark each)**

i) RC phase shift oscillator

ii) Wien bridge oscillator

g) State the necessity of wave shaping circuit.

Ans:- Necessity of wave shaping circuit. **(1/2 mark each)**

I) To generate one wave from the other

II) To limit the voltage level of the waveform to same preset value & suppressing all other voltage levels in excess of the preset level

III) To cut-off the positive & negative portion of the input waveform

IV) To hold the waveform to a particular DC level

h) What is the necessity of regulated power supply. **(02 marks)**

Ans:- Most of the electronics circuits need a source of DC power. In some cases a simple power supply is sufficient where the line voltage is converted to Dc through HWR or FWR (but its output voltage does not remains constant).But in DC regulated power supply voltage regulator is the circuit after the filter circuit which will produce a constant voltage irrespective of change in line voltage and load voltage.

i) State the application of multivibrator.

Ans:- Application of multivibrator. **(any four applications, ½ mark each)**

i) Free running relaxation oscillator

ii) Square wave generator

iii) As a flip-flop

iv) Rectangular wave generator

v) Ramp generator

vi) It can be used to gate another circuit

vii) As delay generator

viii) In the flasher circuit

ix) As a latch

x) As the basic memory element

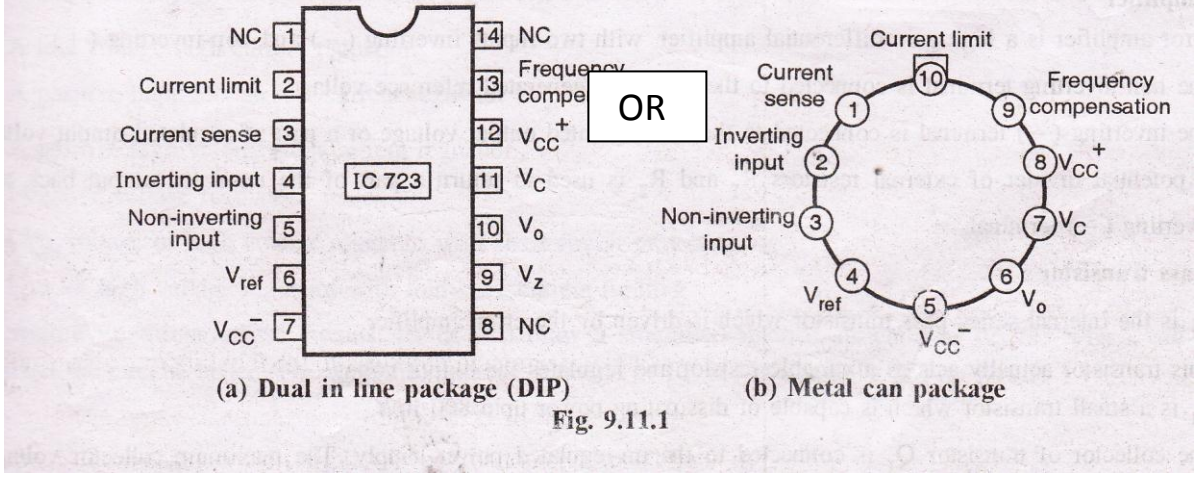
j) Define Clamper circuit **(02 mark)**

Ans:- The circuit with which the waveform can be shifted in such a way so that a particular part of it say positive or negative peak is maintained at a specified voltage level is called clamping circuit

k) Draw pin diagram of IC 723 **(02 mark)**

Ans:-

IC 723 is available in dual in line (DIP) or metal can package as shown in Fig. 9.11.1.



(a) Dual in line package (DIP) (b) Metal can package

Fig. 9.11.1

l) Define Line Regulation and Load Regulation

Ans:-

i) **Line Regulation :-** **(½ mark for definition and ½ mark for formula)**

It is the ratio of change in output voltage that will occur per unit change in the input voltage.

% line regulation = $(\Delta V_L / \Delta V_S)$* 100(unit)

Where ΔV_L = the change in output voltage in mV or µV

ΔV_S = the change in input voltage in input voltage in volts

ii) **Load Regulation :-** **(½ mark for definition and ½ mark for formula)**

It is the ratio of change in output voltage that will occur per unit change in load current.

% Load Regulation = $V_{NL} - V_{FL} / \Delta I_L$ OR $(V_{NL} - V_{FL} / V_{FL}) * 100$

WHERE

V_{NL} = NO Load output voltage

V_{FL} = Full load output voltage

ΔI_L = the change in load current

Its unit is µV/ µA

Q2) Attempt any four of the following **(16 marks)**

a) Draw Characteristic of UJT. State its application.

Ans:-

Characteristic of UJT.. **(03 mark)**

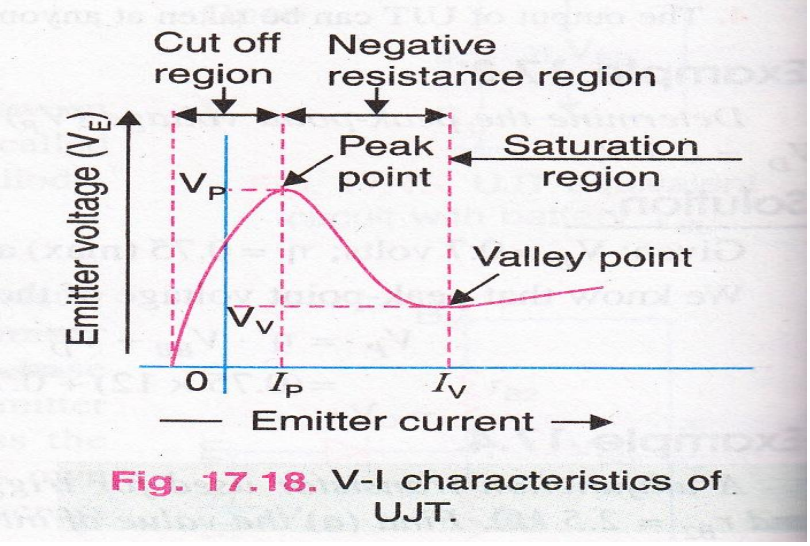


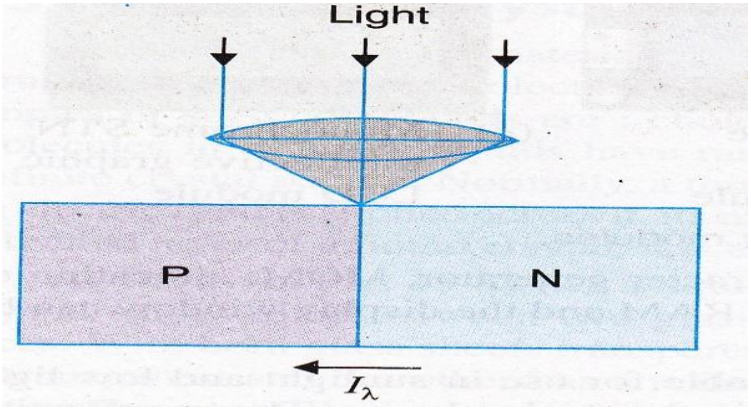
Fig. 17.18. V-I characteristics of UJT.

Application :- **(any two, ½ mark each)**

1) Trigger device for SCR's & TRIAC's
2) Non sinusoidal oscillators
3) Saw tooth generator
4) Timing Circuits
5) As a relaxation oscillator
6) In the UJT/SCR timer
7) In the automobile ignition circuit
8) In the volt. Sweep generator
9) In the precision time delay circuit

b) Draw Construction of photo diode and describe its working principle.

Ans:- Construction of photo diode :- **(Dig. 02 mark)**



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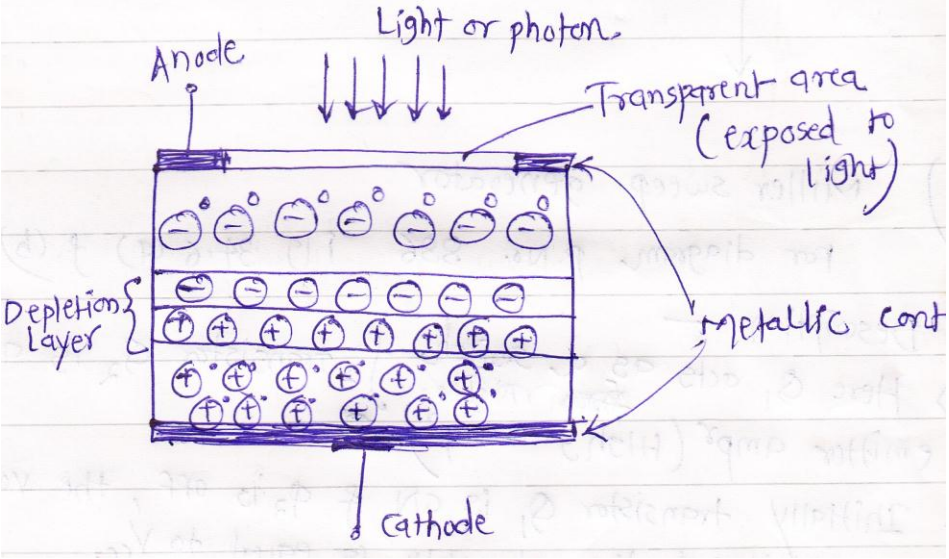


Working principle :- **(02 mark)**

It is a two terminal PN junction device which operates in a reverse bias. It has a small transparent window which allows light to strike the PN junction.

When the junction is illuminated by the light energy holes electrons pairs are generated & the minority carriers are swept across the junction increasing the level of illumination, number of charge carrier generated, thus increases the level of current flowing.

c) State the Advantages and disadvantages of negative feedback amplifier.

Ans:-

Advantages of negative feedback **(any three, 01 mark each)**

i) Increased stability

ii) Increased bandwidth

iii) Less amplitude & harmonic distortion

iv) Decrease noise

v) Less frequency distortion, phase distortion

vi) Input & Output resistance can be modified as desired

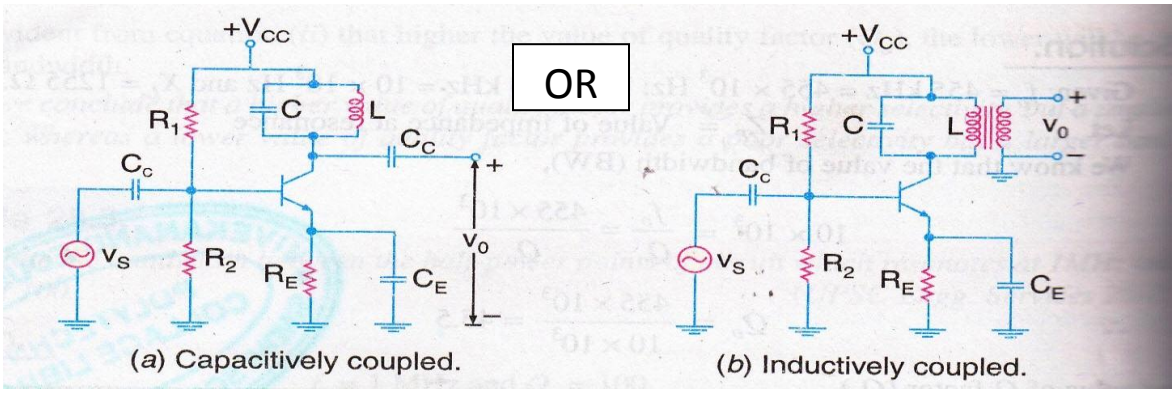
Disadvantage:- **(01 mark)**

i) It reduces the amplifier gain

d) Draw Circuit diagram of single tuned voltage amplifier with frequency response.

Ans:-

Circuit diagram of single tuned voltage amplifier circuit **(02 mark)**



Frequency response:- **(02 mark)**

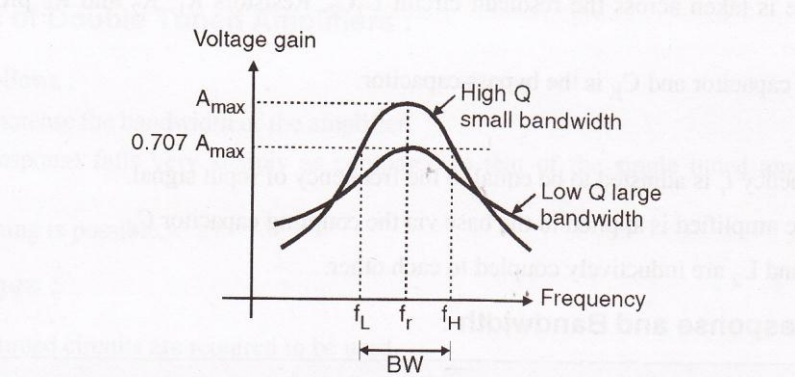


Fig. 3.5.2 : Frequency response of single tuned amplifiers

e) Identify the circuit and draw Input and Output waveform

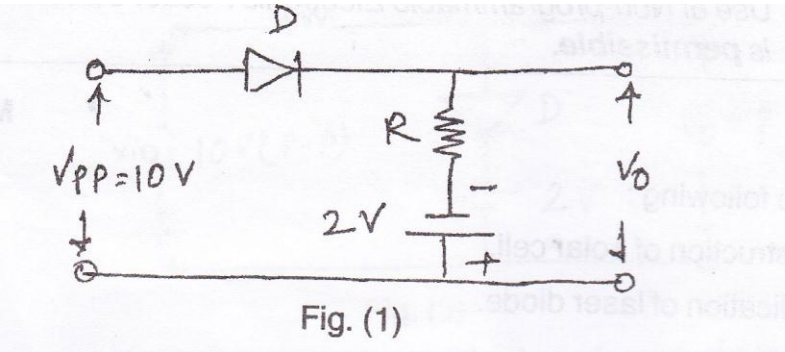
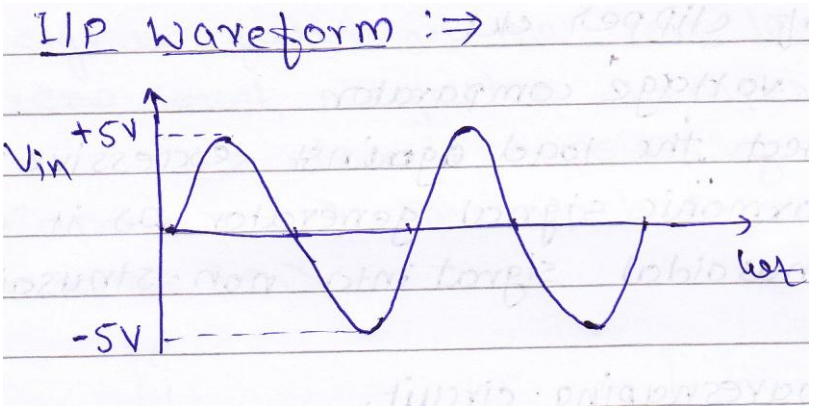


Fig. (1)

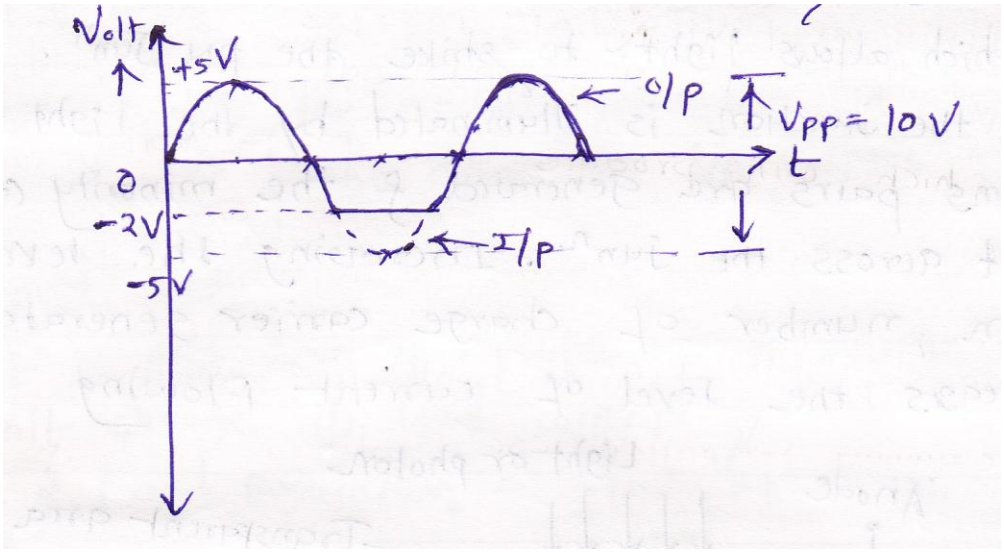
Ans:-

The circuit worked as 'Biased series negative clipper' **(01 mark)**

Input wave form:- **(01 mark)**

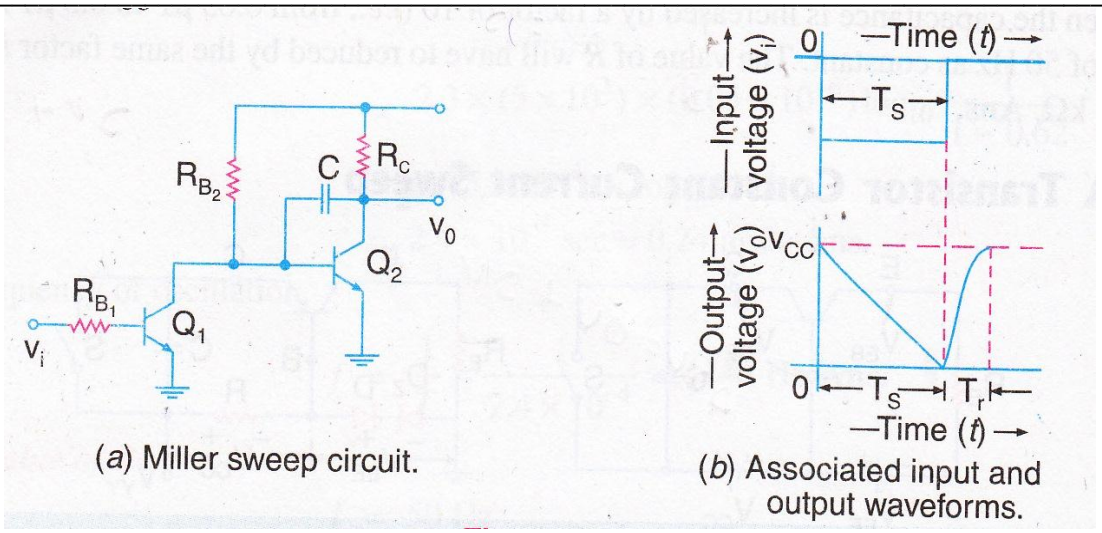


Output wave form **(02 mark)**



f) Draw and describe Miller sweep generator circuit with input and output wave form.

Ans:- Miller sweep generator:- (circuit diagram 01 mark, wave forms 01 mark, description 02 mark)



(*a*) Miller sweep circuit.

(*b*) Associated input and output waveforms.

Description:-

1) Here Q_1 acts as a switch & transistor Q_2 is a common emitter amplifier (High gain amplifier)

2) Initially transistor Q_1 is OM & Q_2 is OFF, the voltage across the capacitor & the output volt is equal to V_{CC}

3) When a input of negative pulse is applied at the base of the transistor Q_1 becomes OFF, which causes transistor Q_2 to turn ON.

   AS Q_2 is ON, the output voltage begins to decrease toward zero. Since the capacitor 'C' is coupled to the base of transistor Q_2 therefore the rate of decrease of output voltage is controlled by the rate of discharge of capacitor 'C'. The time constant of the discharge is given by the relation

   Time constant $= R_B * C$

   Since the value of time constant is very large, therefore the discharge current practically remains constant. Hence collector voltage drop down is linear.

4) When the input pulse is removed the transistor Q_1 turns ON & Q_2 is OFF. As the transistor Q_1 turns OFF, the capacitor 'C' charges quickly, through R_C to V_{CC} with the time constant equal to $R_C * C$

Q3. Attempt any four of the following: 16marks

a) Describe current series and voltage series negative feedback connection.

Ans:- Current series feedback connection:-
(diagram 1mark, explanation 1mark)

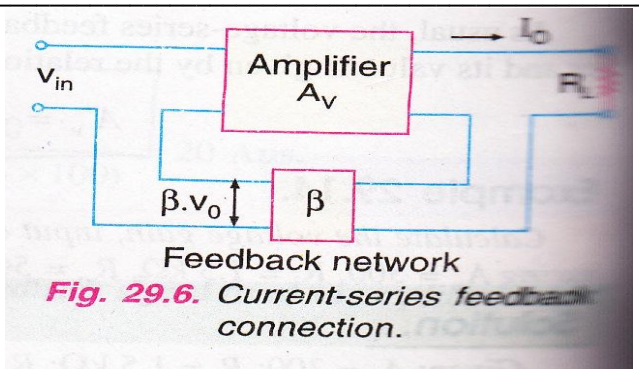


Fig. 29.6. Current-series feedback connection.

Above fig shows a block diagram of a current series feedback connection. In this connection a fraction of output current is converted into a proportional voltage by the feedback network and then applied in series with the input.

This connection increases both the input resistance and the output resistance of a feedback amplifier by a factor = $(1+ \beta A_v)$.

Input resistance is given by

$R_i' = (1+ \beta A_v) R_i$ and

Output resistance is given by

$R_o' = (1+ \beta A_v) R_o$

Where β = The feedback fraction

A_v = The voltage gain without feedback

R_i = Input resistance without feedback

R_o = Output resistance without feedback.

Voltage series feedback connection:-

(diagram 1mark, explanation 1mark)

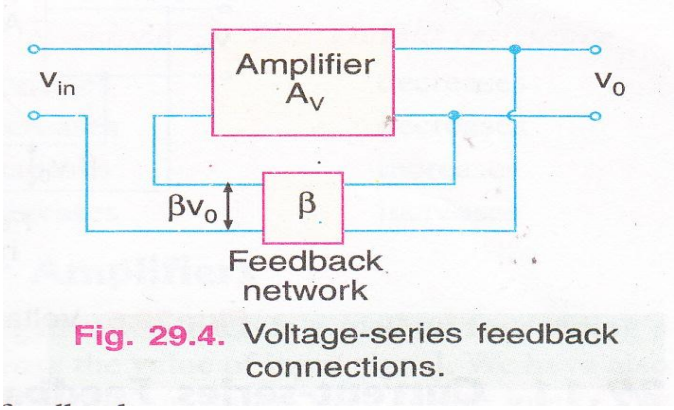


Fig. 29.4. Voltage-series feedback connections.

Above fig. shows block diagram of a voltage series feedback connection. In this connection, a fraction of the output voltage is applied in series with the input voltage through the feedback network. However, the input to the feedback network is in parallel with the output of the amplifier.

This connection increases the input resistance and decreases the output resistance of the feedback amplifier.

The input resistance is given by

$R_i' = (1+ \beta A_v) R_i$

The output resistance is given by

$R_o' = R_o / (1+ \beta A_v)$

b) State the advantages of negative feedback amplifier on the basis of voltage gain, bandwidth, input impedance, noise.

Ans:-

1) Voltage gain decreases. **(1mark)**
2) Bandwidth increases. **(1mark)**
3) Input impedance can be modified as desired. **(1mark)**
4) Noise decreases. **(1mark)**

c) Identify the following circuit shown in fig., draw input and output waveform.

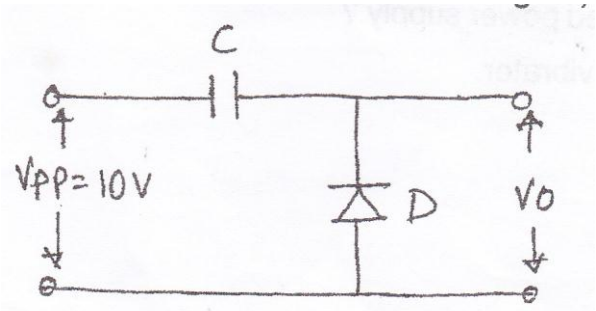
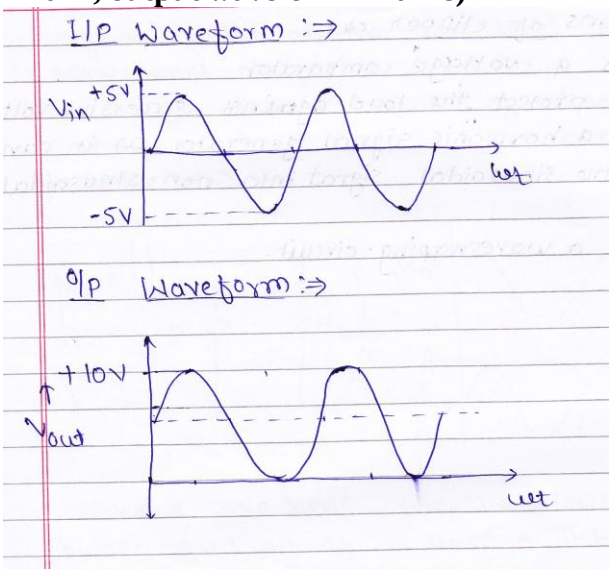


Fig. (2)

Ans:- The above circuit is positive clamper **(Identification 1 mark, Input waveform 1mark, output waveform 2marks)**



d) Describe the operation of monostable multivibrator with circuit diagram.

Ans:- (Circuit diagram 2marks, Working 2 marks)

It is also called as one shot or univibrator and used to generate a gating pulse, whose width can be controlled.

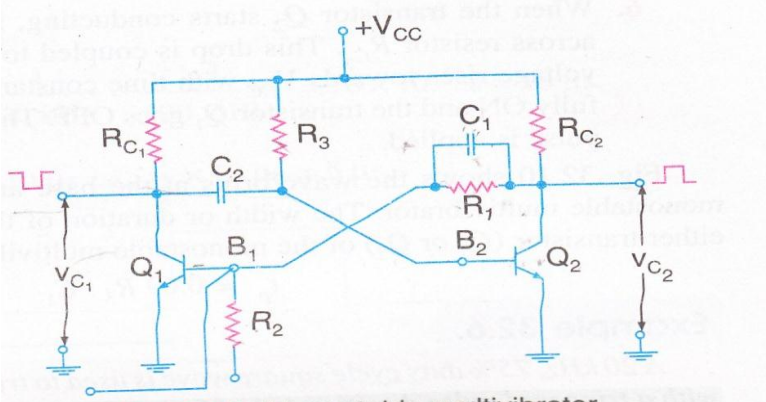


Fig. 32.9. Monostable multivibrator.

Above fig. shows the circuit diagram of a monostable multivibrator using NPN transistors. Here the output of Q_2 is coupled to the base of Q_1 through R_1 and C_1 and the output of Q_1 is coupled to the base of Q_2 through the capacitor C_2. The C_1 is known as commutating or speedup capacitor, its function is to speedup the circuit in making abrupt transition between the ON and OFF state.

The base of Q_2 is returned to V_{cc} supply through R_3, while the base of Q_1 is connected to the negative supply through resistor R_2. The advantage of this biasing is that it keeps transistor Q_1 OFF and Q_2 ON this state is known as a stable state of MMV.

The circuit operation may be explained by keeping in mind that initially the circuit is in its stable state i.e. Q_1 is OFF and Q_2 is ON.

- When a positive trigger pulse of sufficient amplitude is applied to the base of Q_1 , it overrides the revers bias and gives it a forward bias, so Q_1 starts conducting.
- As Q_1 conducts, its collector voltage falls due to voltage drop across resistor R_{c1}, which decreases the forward bias of Q_2
- Due to the reduced forward bias the collector current of Q_2 starts decreasing and its collector voltage rises exponentially towards V_{cc}.
- The rising collector voltage of Q_2 is coupled to the base of Q_1 through R_1 where it further increases its forward bias, due increased forward bias, Q_1 conducts more
- Immediately, C_2 starts charging towards V_{cc} , as C_2 charges the base voltage of Q_2 increases, as C_2 further charges, the Q_2 is pulled out from the cut off and reverse transition takes place i.e. Q_2 ON and Q_1 OFF.
- When Q_2 starts conducting its collector voltage falls due to voltage drop across R_{c2} this drop is coupled to the base of Q_1 whose collector voltage rises towards V_{cc}. finally the Q_2 turns fully ON and Q_1 goes OFF. The circuit remains in this stable state till another pulse is applied.

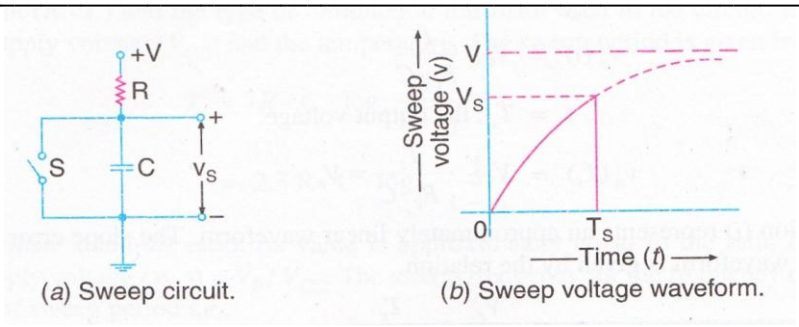
  The width of the pulse

  $T_p = 0.69\ R_3\ C_1$

e) Draw circuit diagram of exponential time base generator describe its operation.

Ans**:- (Circuit diagram 2marks, Working 1mark, waveform 1mark)**

Exponential time base generator:

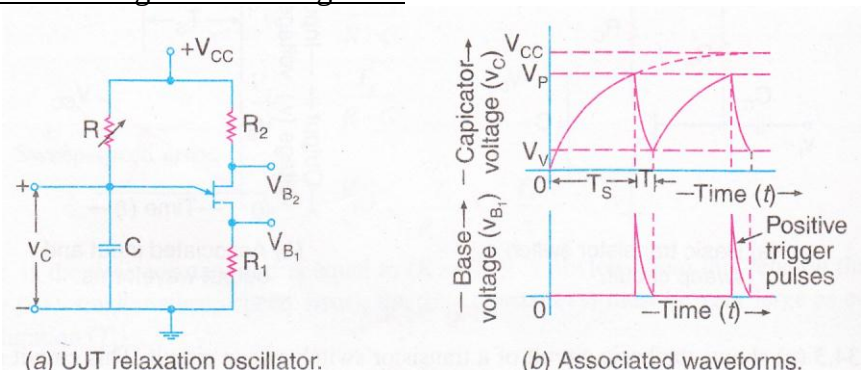


(a) Sweep circuit. (b) Sweep voltage waveform.

Above fig. shows a simplest circuit to generate an exponential time base signal. This circuit consists of a series RC circuit connected to a supply voltage V. switch is connected across the capacitor C. the output voltage is taken across the capacitor C.

OR

Exponential time base generator using UJT:



(a) UJT relaxation oscillator. (b) Associated waveforms.

When the supply voltage (V_{cc}) is switched ON, the capacitor C charges through resistor R, till the capacitor voltage reaches the voltage level $V_{p,}$ which is called peak point voltage. At this voltage, the UJT turns ON. As a result of this, the capacitor c discharges rapidly through resistor $R_{1.}$
When the capacitor voltage drops to level V_V (called valley point voltage)the UJT switches OFF, allowing the capacitor C to charge again.

Fig b. shows the collector voltage V_c and the base 1 voltage waveforms during the capacitor charging and discharging interval. It may be noted that the voltage developed at the base 1 terminal is in the form of narrow pulses commonly known as trigger pulses. The similar pulses (but with opposite polarity) are also available at the base 2 terminal of the UJT.

The sweep period (period of oscillation), depends upon the time constant (R.C) and the type of UJT used in the circuit, However it is independent of supply voltage (V_{CC}) & the temp.

It is given by

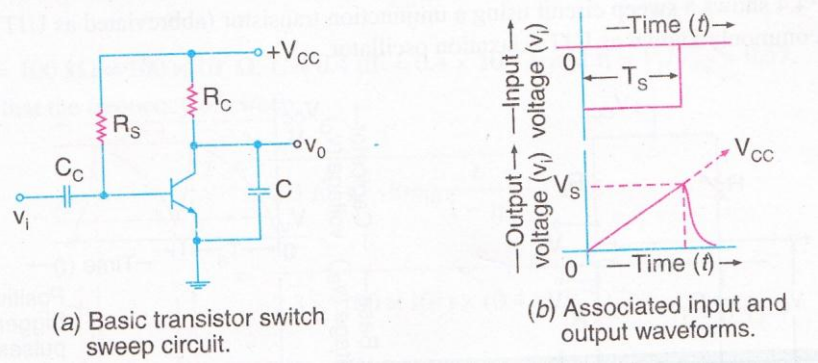
$$T = R.C. \log_e (1/1 - \eta)$$
$$= 2.3\ R.C. \log_{10}(1/1 - \eta)$$

Where η = intrinsic standoff ratio & is given by

$$\eta = V_p / V_{cc} \text{ (peak period voltage)}$$
$$F = 1/T$$
$$= 2.3\ R.C. \log_{10}(1/1 - \eta)$$

OR

Exponential time base generator using transistor switch:



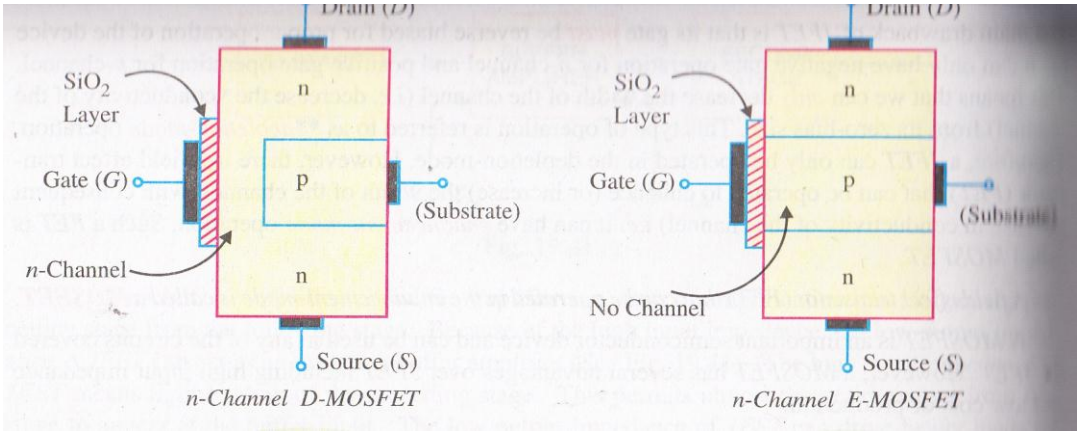
(a) Basic transistor switch sweep circuit.

(b) Associated input and output waveforms.

Above fig. shows circuit diagram of exponential time base generator using transistor switch. The circuit requires a gating waveform (V_i) as shown in above fig. it may be obtained from MMV or AMV.
Working:- Initially the transistor is bias ON and operates in saturation region. Thus when there is no input (i.e. $V_i = 0$) the output voltage is zero (actually it is $V_{CE(sat)}$).
When the gating pulse (i.e. a negative pulse) is applied, the transistor turns OFF. As a result of this, the capacitor voltage rises to a target value V_{cc} with a time constant R_c C.
It may be noted that the transistor switch is OFF only for gating time (T_s). at the end of the time T_s , the capacitor discharges and the voltage is again zero. It is possible to generate a negative going sweep using transistor switch but in that case, we have to use a PNP transistor.

f) Draw construction of N-channel depletion type and enhancement type MOSFET.

Ans:-<u>N-channel D- type MOSFET</u>.(2marks) <u>N-channel E- type MOSFET</u>. (2marks)



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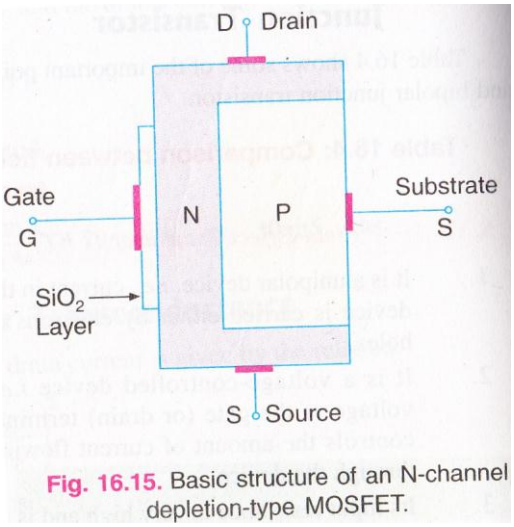
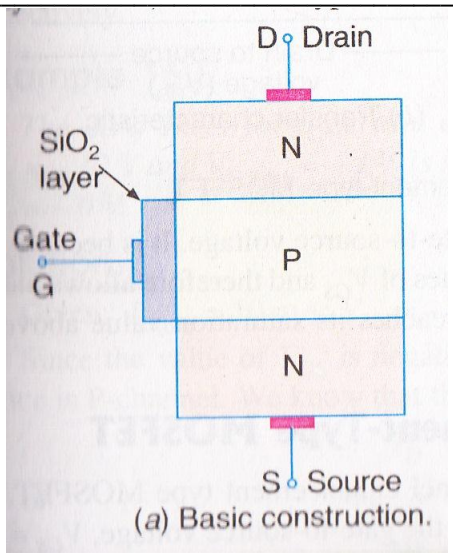


Fig. 16.15. Basic structure of an N-channel depletion-type MOSFET.



(a) Basic construction.

Que.4) Attempt any two of the following: (16 marks)

a) Draw neat circuit diagram of Hartley Oscillator describe its working. Also give the formula for frequency of oscillation.

Ans:- (Circuit diagram 3marks, Working 3marks, formula 2marks)

circuit diagram:-

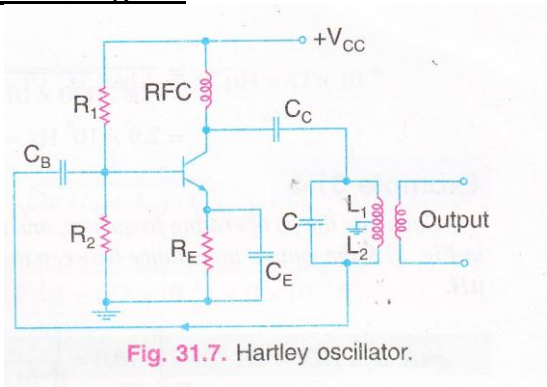


Fig. 31.7. Hartley oscillator.

OR

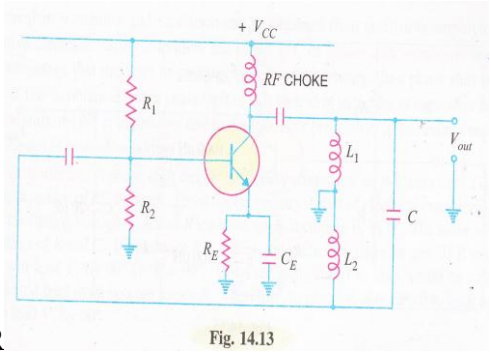


Fig. 14.13

Above fig. shows circuit diagram of Hartley Oscillator. It consists of two coils L_1 and L_2. The coil L_1 is inductively coupled to coil L_2 and the combination works as an autotransformer. Which introduces a phase shift of 180^0, the phase reversal between input and output voltage occurs because they are taken from the opposite ends of the coil (L_1 and L_2) with respect to tap, which is grounded.

Since the transistor also introduces a phase shift of 180^0, therefore the total phase shift is 360^0 and hence the feedback is positive.

The feedback fraction is given by $\beta = L_2 / L_1$.

For oscillations voltage gain must be greater than $1/\beta$ which is equal to L_1 / L_2 .

The capacitor C_c is coupling capacitor, it permits only the AC currents to pass to the tank circuit. R_1, R_2 and R_E are used to provide DC bias and stabilization. C_E is the emitter bypass capacitor.

When the circuit is energized by switching on the supply, the collector current flows. The oscillations are produce because of positive feedback from the tank circuit.

The frequency of oscillations is given by

$$f_0 = 1/2\pi\sqrt{L_{TC}}$$

where, $L_T = L_1 + L_2 + 2M$

$L_T = L_1 + L_2$ (if mutual inductance is neglected)

$$f_0 = 1/2\pi\sqrt{(L_1 + L_2)C}$$

b) Draw circuit diagram of transistorized series voltage regulation, describe its operation.
Ans:- (Circuit diagram 4marks, Working 4marks)
circuit diagram:-

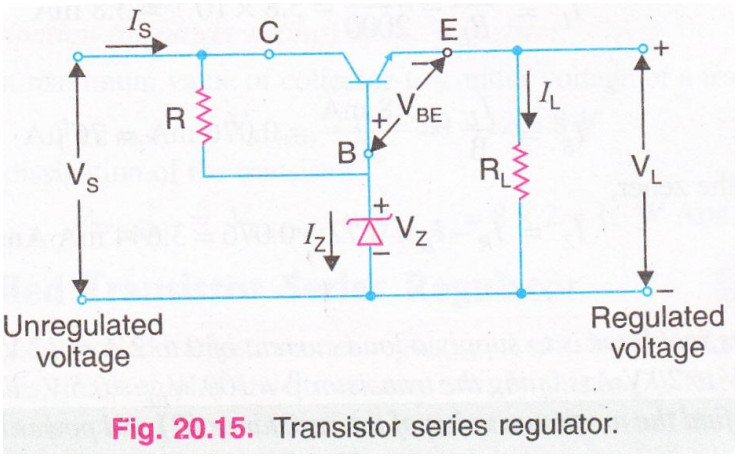


Fig. 20.15. Transistor series regulator.

Above fig. shows a circuit of a transistor series regulator. Since the transistor is connected in series with the load, therefore the circuit is known as a series regulator.
Operation:-

- The unregulated DC supply is fed to the input terminal as shown in above fig.
- The output voltage is given by $V_L = V_Z - V_{BE}$
- V_Z being a zener voltage is assumed to be a constant therefore if the output voltage varies, then there will be a change in V_{BE} .
- If the output voltage increases due to some region then V_{BE} decreases and due to this base current decreases. Therefore collector current decreases. This will increase the collector to emitter voltage (V_{CE}) across the transistor and V_L will be regulated. this is because $V_L = V_s - V_{CE}$.
- If the output voltage decreases then exactly opposite action will takes place and the output voltage is regulated.
- The circuit action may be summarized in the form of the following equation.
  $V_L\uparrow \rightarrow V_{BE}\downarrow \rightarrow I_B\downarrow \rightarrow I_C\downarrow \rightarrow V_{CE}\uparrow \rightarrow V_L\downarrow$

c) Draw circuit diagram of bistable multivibrator and describe its working with waveforms.
Ans:- (Circuit diagram 3marks, Working 3marks, Waveforms 2marks)

It is also called flipflop, trigger circuit or binary. It has two stable state, indefinitely, as long as the power is supplied.
It changes to other state only when it receives a trigger from outside.

Circuit diagram:-

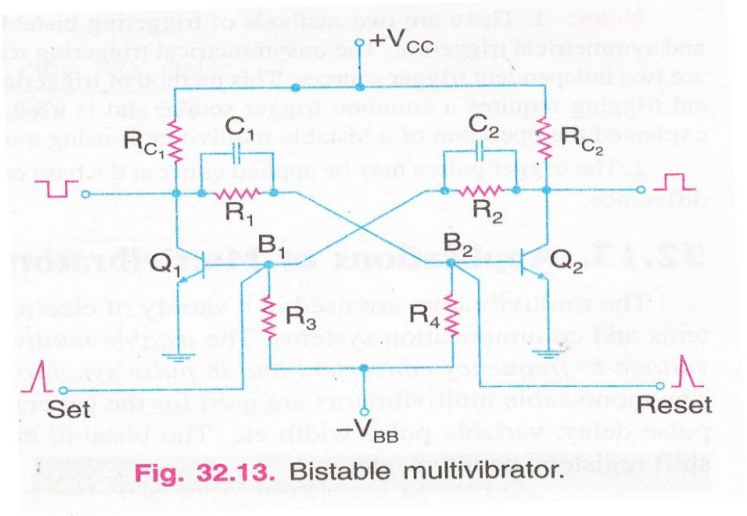


Fig. 32.13. Bistable multivibrator.

Above fig. shows the circuit of bistable multivibrator using two NPN transistors. Here the output of Q_2 is coupled to the input of Q_1 through R_1 and output of Q_1 is coupled to input of Q_2 through R_2 .

The capacitor C_1 and C_2 are called speedup capacitor. Their function is to increase the speed of the circuit in making abrupt transition from one stable state to another stable state.

The R_3 and R_4 are connected to a common source $-V_{BB}$.

The output of bistable multivibrator is available at the collector terminal of both the transistors Q_1 and Q_2 which is complementary to each other

Fig. shows waveforms at the collector of Q_1 and Q_2 .

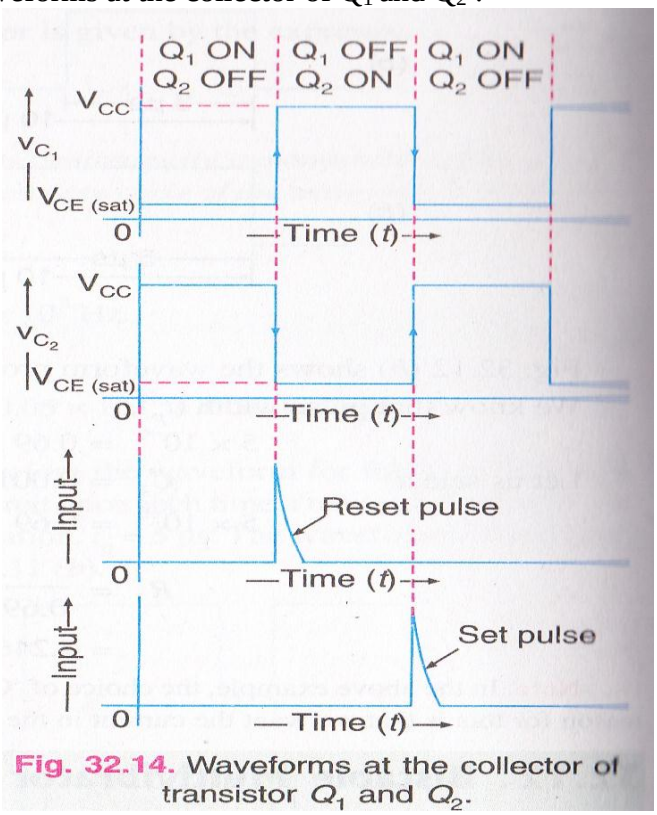


Fig. 32.14. Waveforms at the collector of transistor Q_1 and Q_2.

- When V_{CC} supply is switched ON, one of the transistor will start conducting more than the other. Then because of the feedback action. This transistor will be driven into saturation and the other to cut off.
- Let us assume that Q_1 is in saturation (i.e. ON) and Q_2 is cut off (i.e. OFF). It is stable state of the circuit and will remain in this state till a trigger pulse is applied from outside.

- A negative pulse is applied to set input will turn OFF the Q_1 and Q_2 to ON. A similar action can also be achieved by applying a +ve pulse at reset input.
- Suppose a +ve pulse is applied at the reset input it will caused the Q_2 to conduct as the collector voltage of Q_2 falls it cuts off the Q_1 thus the circuit switches to other stable state i.e. a where Q_1 is OFF and Q_2 is ON.

Now if a positive pulse is applied at the set input it will switch the circuit back to its original stable state i.e. Q_1 is ON Q_2 is OFF.

Q5) Attempt any four of the following (16 marks)

a) Compare LC and RC oscillator on the basis of Component Used, Feedback element, Frequency range, Frequency formula

Ans:- Comparison between LC and RC oscillator **(01mark each)**

Characteristics	LC oscillator	RC oscillator
Component Used	Inductor, Capacitor	Resistor, Capacitor
Feedback element	LC tank circuit	RC phase shift circuit
Frequency range	High usually from 1MHz-500MHz	Low usually in audio frequency range 20Hz-20KHz
Frequency formula	$1/2\prod\sqrt{LC}$	$1/2\prod RC\sqrt{6}$

b) Draw Circuit diagram of RC Integrator. Draw output waveform with Square input

Ans:- Circuit diagram of RC Integrator **(02 marks)**

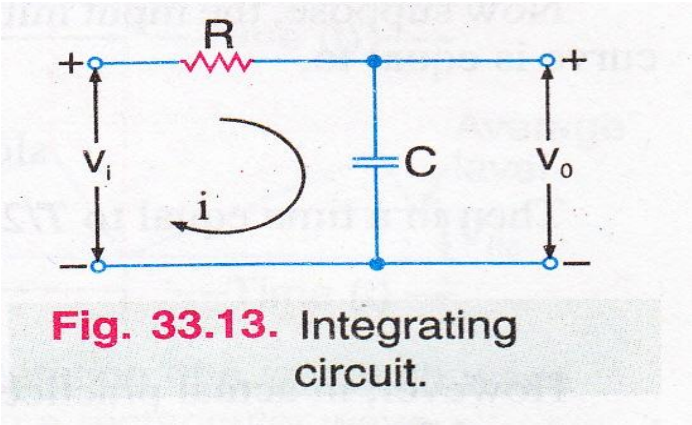


Fig. 33.13. Integrating circuit.

Output waveform with square input **(02 marks)**

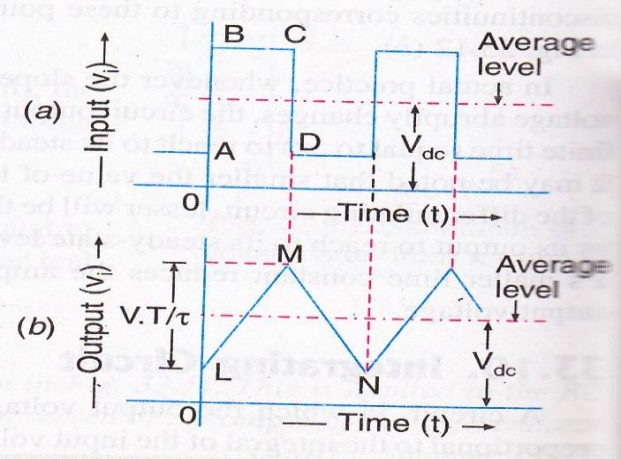
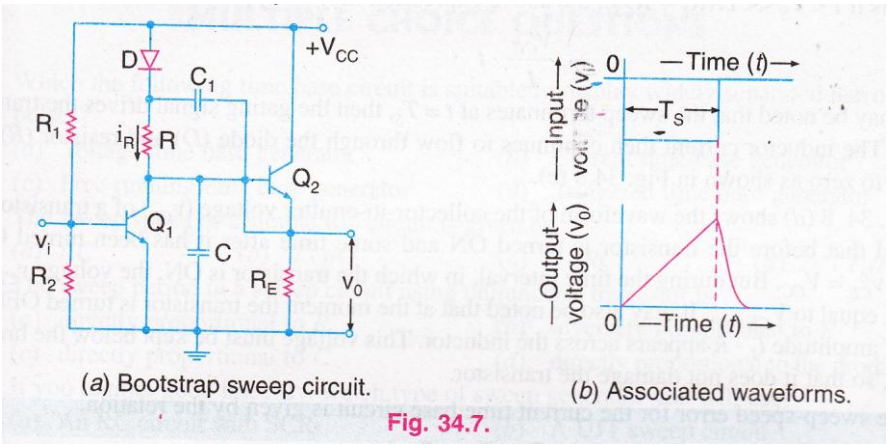


Fig. 33.14. Generation of a triangle wave from a square wave.

c) Draw Circuit diagram of bootstrap sweep generator and describe its working

Ans:- Circuit diagram of bootstrap sweep generator **(02 marks)**



(a) Bootstrap sweep circuit. (b) Associated waveforms.

Fig. 34.7.

Working:- **(02 marks)**

Initially let Q_1 be 'on' and Q_2 be 'off'

Capacitor C_1 get charged to Vcc through diode D

Output voltage = 0 at this instance

Now, when a negative pulse is applied to base of Q_1, it turns 'off' and Q_2 turns 'on'

For Q_2, $V_B = V_E = V_O$

Therefore Capacitor C_1 starts charging capacitor through RC

Therefore voltage at base of Q_2 (= voltage across capacitor and output voltage increases

Value of C_1 >> C, voltage across C_1 practically remains constant.

Therefore voltage drop across R_C remains constant .

Capacitor C charges with constant current

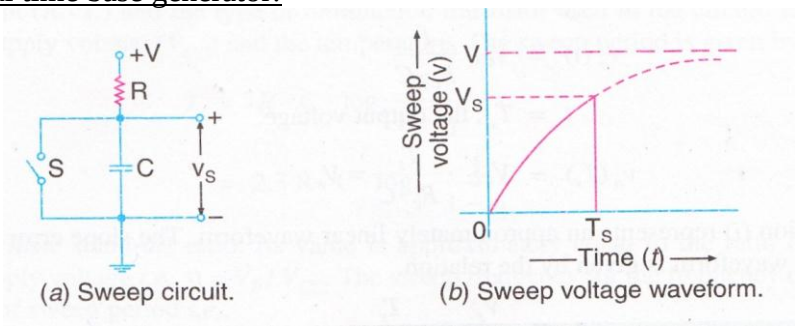
Voltage across C increases linearly with time.

When negative voltage pulse applied to base of transistor is removed, 'C' discharge rapidly through Q_1 and output becomes zero.Capacitor C_1 again get changed through diode D.

d) Draw Circuit Diagram of Exponential sweep generator and describe its working

Ans:- (Circuit diagram 2marks, Working 1mark, waveform 1mark)

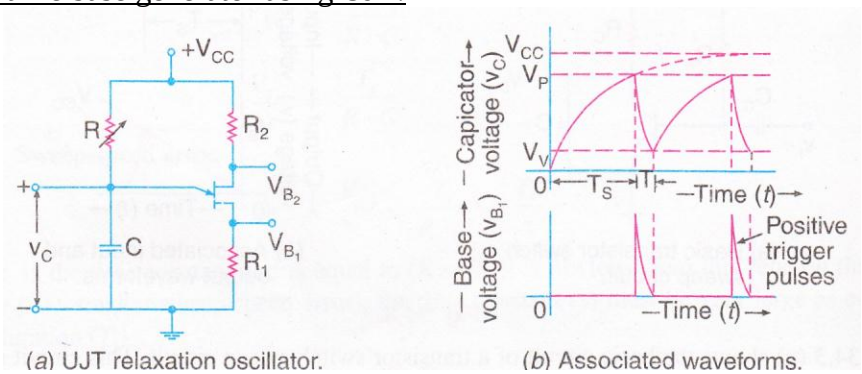
Exponential time base generator:



Above fig. shows a simplest circuit to generate an exponential time base signal. This circuit consists of a series RC circuit connected to a supply voltage V. switch is connected across the capacitor C. the output voltage is taken across the capacitor C.

OR

Exponential time base generator using UJT:



When the supply voltage (V_{cc}) is switched ON, the capacitor C charges through resistor R, till the capacitor voltage reaches the voltage level V_p, which is called peak point voltage. At this voltage, the UJT turns ON. As a result of this, the capacitor c discharges rapidly through resistor R_1.

When the capacitor voltage drops to level V_V (called valley point voltage)the UJT switches OFF, allowing the capacitor C to charge again.

Fig b. shows the collector voltage V_c and the base 1 voltage waveforms during the capacitor charging and discharging interval. It may be noted that the voltage developed at the base 1 terminal is in the form of narrow pulses commonly known as trigger pulses. The similar pulses (but with opposite polarity) are also available at the base 2 terminal of the UJT.

The sweep period (period of oscillation), depends upon the time constant (R.C) and the type of UJT used in the circuit, However it is independent of supply voltage (V_{CC}) & the temp.

It is given by

$$T = R.C.\ \log_e (1/1 - \eta)$$
$$= 2.3\ R.C.\ \log_{10}(1/1 - \eta)$$

Where η = intrinsic standoff ratio & is given by

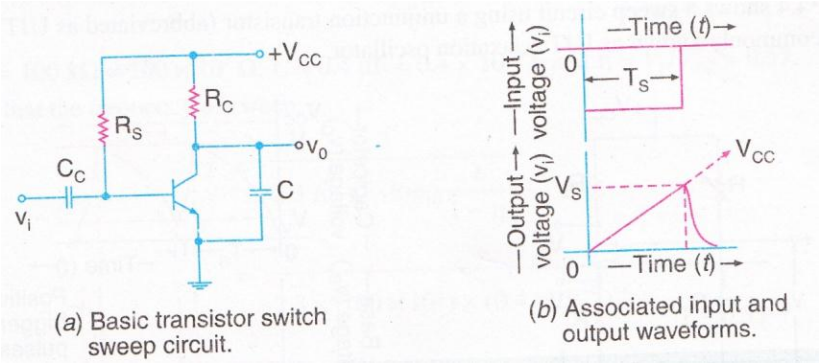
$\eta = V_p / V_{cc}$ (peak period voltage)

$F = 1/T$

$= 2.3\ R.C.\ \log_{10}(1/1 - \eta)$

OR

Exponential time base generator using transistor switch:



Above fig. shows circuit diagram of exponential time base generator using transistor switch. The circuit requires a gating waveform (V_i) as shown in above fig. it may be obtained from MMV or AMV.

Working:- Initially the transistor is bias ON and operates in saturation region. Thus when there is no input (i.e. $V_i = 0$) the output voltage is zero (actually it is $V_{CE(sat)}$).
When the gating pulse (i.e. a negative pulse) is applied, the transistor turns OFF. As a result of this, the capacitor voltage rises to a target value V_{cc} with a time constant R_c C.
It may be noted that the transistor switch is OFF only for gating time (T_s). at the end of the time T_s , the capacitor discharges and the voltage is again zero. It is possible to generate a negative going sweep using transistor switch but in that case, we have to use a PNP transistor.

e) Draw Circuit diagram of RC phase shift oscillator and describe its working

Ans:- Circuit diagram of RC phase shift oscillator **(02 marks)**

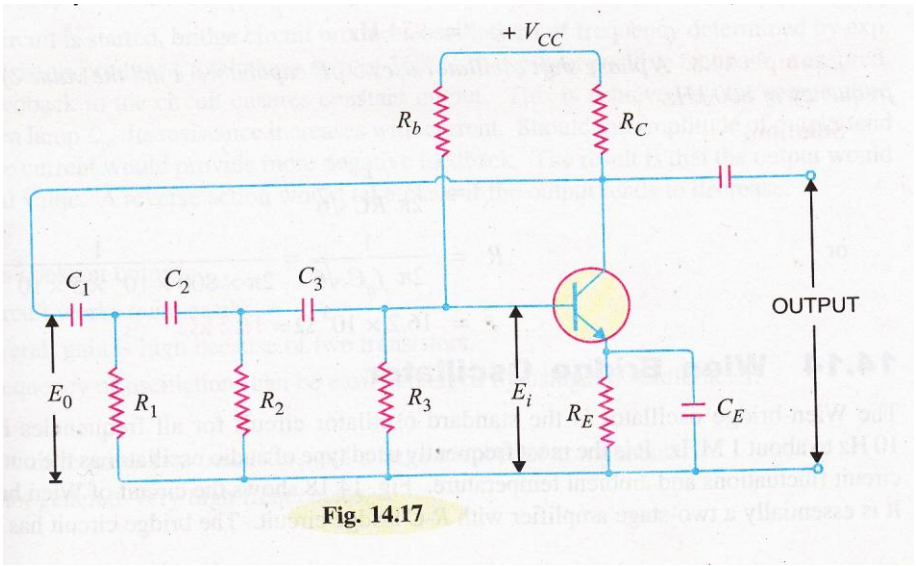


Fig. 14.17

Working:- **(02 marks)**

It consist of a conventional single transistor amplifier and a RC phase shift network.

The phase shift network consist of three sections R_1C_1, R_2C_2 and R_3C_3.

At some particular frequency fo, the phase shift in each RC section is 60^0. SO the total phase shift produced by the RC network is 180^0.

The frequency of oscillations is given by

$$fo = 1/2\prod RC\sqrt{6}$$

where $R_1 = R_2 = R_3 = R$ and

$$C_1 = C_2 = C_3 = C$$

When the circuit is switched on, it produces oscillation of frequency fo

The output Eo of amplifier is fed back to RC phase shift network. This network produces a phase shift of 180^0 and voltage Ei appears at its output which is applied to transistor amplifier

Further phase shift of $180^0$is produced by transistor amplifier.

Therefore entire loop produces a phase shift of 360^0. Therefore feedback phase shift is correct.

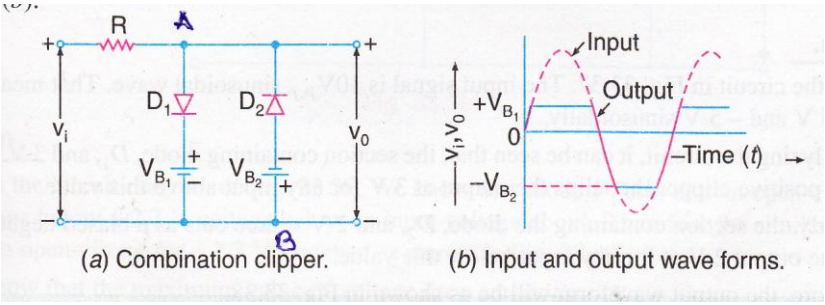
The feedback fraction

$$M = Ei / Eo$$

f) Draw circuit diagram of combinational clipper, describe its working with input and output waveform

Ans:-

Circuit diagram of combinational clipper **(01 marks)** **N**ature of input and output waveform **(01 marks)**



Working :- **(02 marks)**

This is a combination of positive and negative clipper

During positive half cycle of the input voltage V_1, as long as Vin < V_A, the diode D_1 will not conduct.

When $Vin \geq V_A$, the diode D_1 will conduct and output voltage $V_0 = V_A = 0.7 + V_{Bias}$ D_2 is reverse biased during this cycle.

During negative half cycle of the input voltage V_1, as long as $V_{in} < V_B$, diode D_2 will be forward biased and will conduct.

Output voltage $V_B = -0.7 - V_{Bias}$

D_1 is reverse biased during entire negative half cycle.

Q6) Attempt any four of the following (16 marks)

a) A tuned circuit has resonance freq. of 2MHz what will the value of Q factor if bandwidth is 10MHz

Ans:- Given:-

Freq. = 2MHz = $2*10^6$Hz

Bandwidth (B.W) = 10MHz = $10*10^6$Hz

Q = Freq./B.W **(01 marks)**

Q = $2*10^6 / 10*10^6$

= 0.2 **(03 marks)**

b) Draw input and output waveform of following circuit

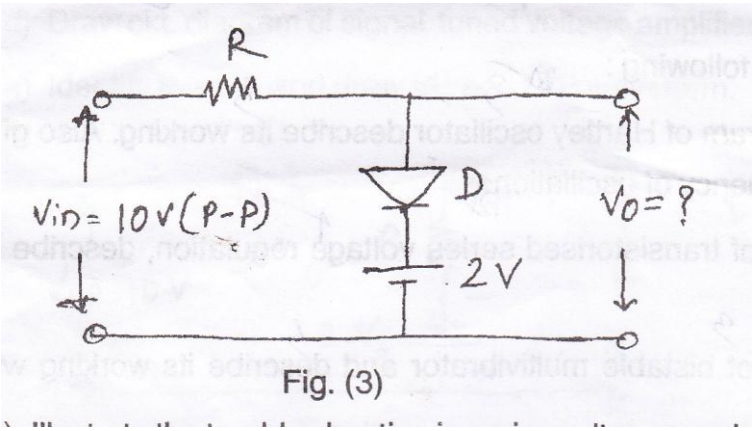
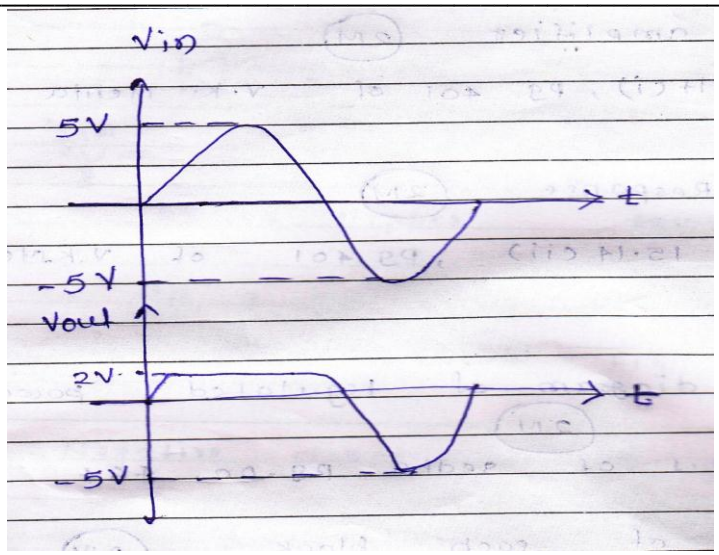


Fig. (3)

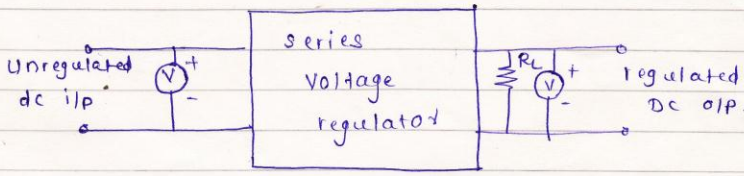
Ans:- Given Circuit is biased positive parallel clipper **(01 mark)**

Input & Output waveforms (**03 mark**)



Q.6. C

- Testing set up for troubleshooting of series voltage regulator is as shown below



- Series voltage regulator circuit consists of series resistor (R_S), Base biasing resistor(R_B), series pass transistor (S), zener diode (Z) and a load resistor R_L.

- check i/p and o/p voltages by using a dc voltmeter. If o/p is below the normal dc voltage level then carry out ohmic test for all the component in ckt.

- For this, switch off i/p supply and check i) transistor : Forward and reverse resistances across BE, BC and CE junction are to be checked,
  ii) zener diode : check forward & reverse resistance
  iii) Resistors : check values.

- Replace the faulty components.

d) Describe with a neat circuit diagram and wave form of Positive clipper circuits and Negative clipper circuit.

Ans:-

Positive clipper circuits (½ marks) Input & output waveform (½ marks)

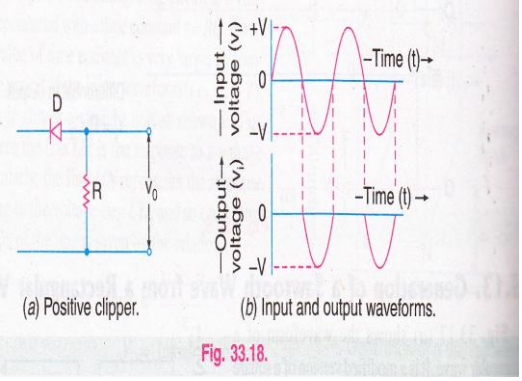


Fig. 33.18.

Description :- **01 mark**)

During positive half cycle diode D is reverse biased hence $V_0 = 0$.

During negative half cycle diode D is forward biased hence $V_0 = - V_{in}$

OR

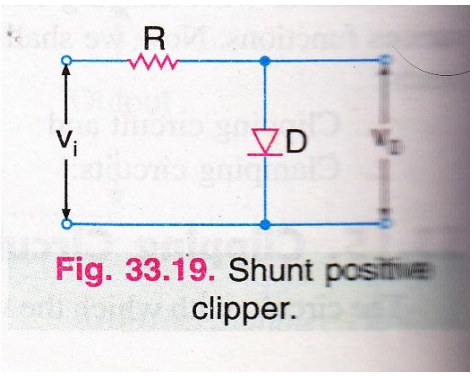


Fig. 33.19. Shunt positive clipper.

Description :- **01 mark**)

During positive half cycle diode D is forward biased hence $V_0 = 0$.

During negative half cycle diode D is reverse biased hence $V_0 = - V_{in}$

Negative clipper circuit **(½ marks)** Input & output waveform **(½ marks)**

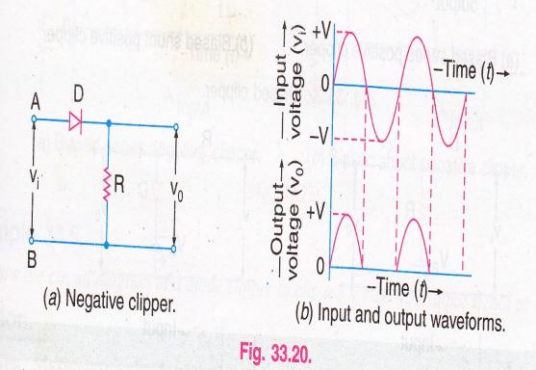


Fig. 33.20.

Description :- (**01 mark**)

During positive half cycle diode D is forward biased hence $V_0 = + V_{in}$.

During negative half cycle diode D is reverse biased hence $V_0 = 0$

OR

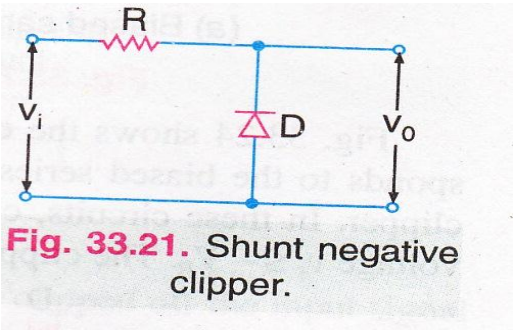


Fig. 33.21. Shunt negative clipper.

Description :- (**01 mark**)

During positive half cycle diode D is reverse biased hence $V_0 = + V_{in}$.

During negative half cycle diode D is forward biased hence $V_0 = 0$

e) Draw Circuit diagram of double tuned voltage amplifier with frequency response.

Ans:-

Circuit diagram **(02 marks)** Freq. response **(02 marks)**

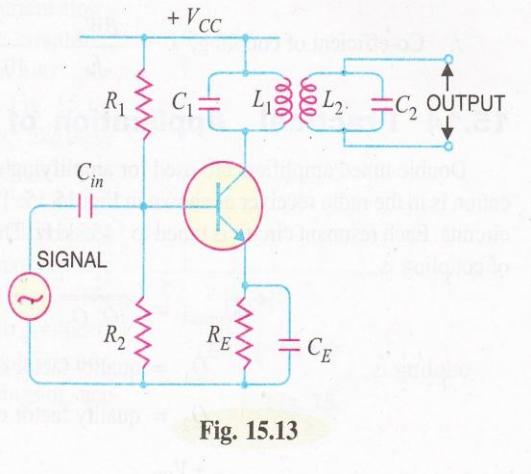
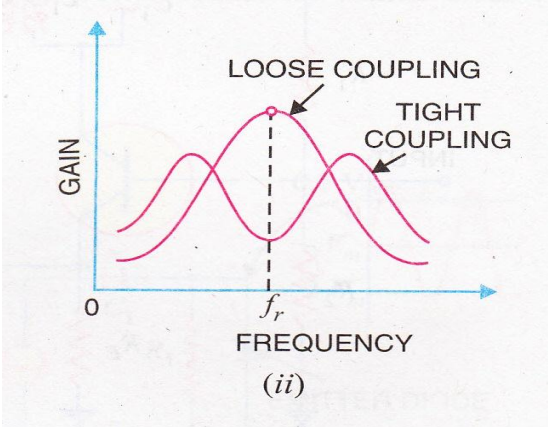


Fig. 15.13



f) Draw block diagram of regulated power supply describe the function of each block**s**

Ans:- Block diagram of regulated power supply **(02 marks)**

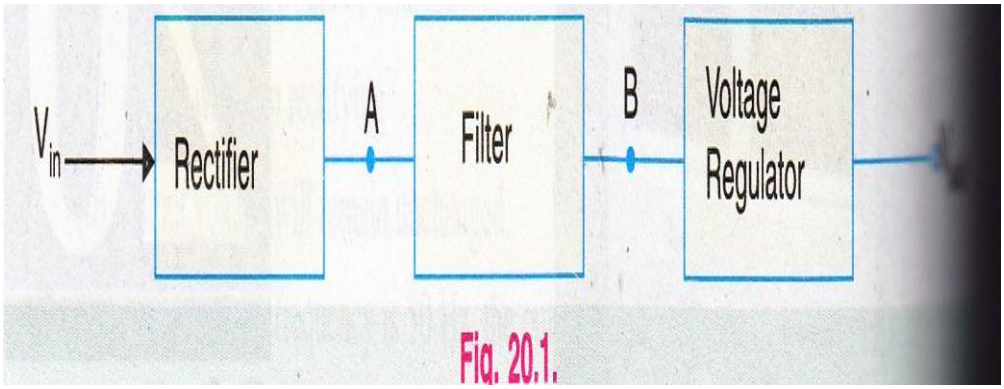
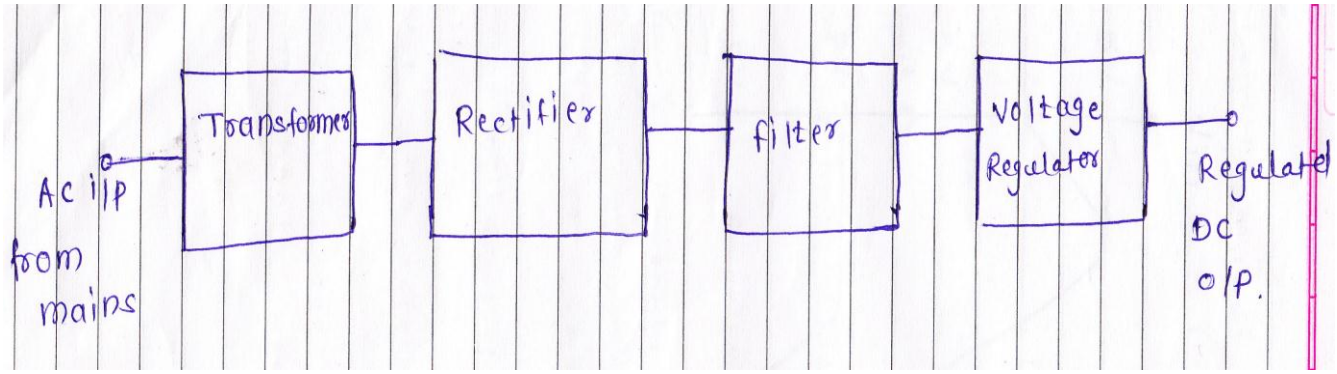


Fig. 20.1.

OR



Function of each block **(02 marks)**

Transformer :- Its steps down AC input from mains

Rectifier:- It converts AC mains voltage into pulsating DC voltage. It is then applied to filter circuits.

Filter :- It reduces the pulsation in the rectifier dc output voltage.

Voltage regulator :- It Carries out two functions firstly, it reduces variations in the filtered output voltages. Secondly, it keeps the output voltage nearly constant even though the load changes or input ac voltage changes.