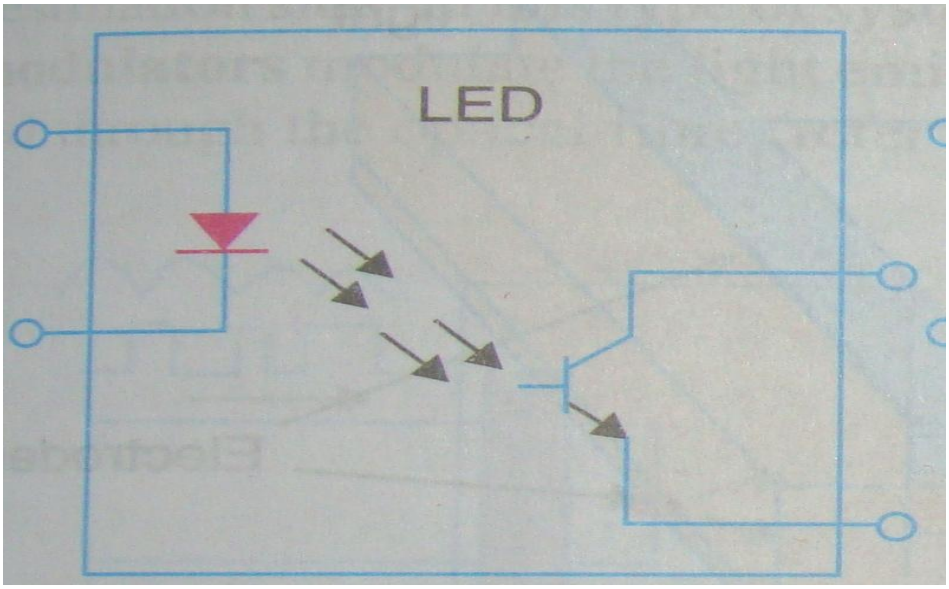

Q. 1. A) Attempt any SIX of the following. (2 x 6 = 12)

i) Draw the symbol of opto-coupler and gives its 2 application.

Ans. :- **{Symbol 01mark, applications (any two)-1 mark}**

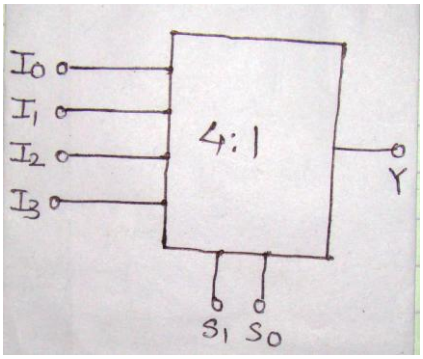


Application: i) Punch card reader, a part counter,

ii) Used to couple the two providing high level of Isolation.

ii) Draw 4: 1 multiplexer.

Ans.:- **(logic diagram -2 marks)**



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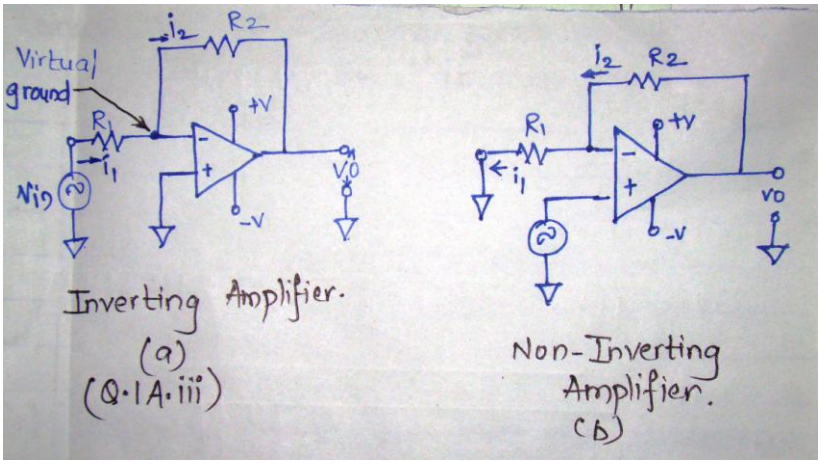
iii) Define inverting and non – inverting op- amp.

Ans.:- **(definition & diagram or one of it of each type – 1 mark)**



Inverting amplifier: When the input is connected to the inverting terminal of op-amp then it is termed as Inverting amplifier.

Non- Inverting amplifier: When the input is connected to the non-inverting terminal of op-amp then it is termed as non-Inverting amplifier

iv) Define β dc and γ dc with its expression.

Ans.:- **(each definition 1 mark)**

β dc:- It is called as common emitter DC current gain. **β dc** is defined as the ratio of change in (Δ Ic) to to base current (ΔIβ)

$\beta = Ic / I_B$

γ dc:- is called as common collector current gain.

γ dc = IE / Ic x Ic / IB = (1 / α) x β. = 1 + β

v) Convert $(58)_{10}$ to hexadecimal.

Ans. :- **(for the steps 1 mark and answer -1 mark)**

Convert (58) to hexadecimal (procedure – 1mark, Ans.- 1mark)

(58) 10 = ( ) H.

Decimal no		Base		Quotient	Remainder
58	÷	16	=	3	10
			=	3AH.	

vi) State the application of PN junction diode (any 2).

Ans.:- **(each application – 1 mark)**

i) It is used as power diode in rectifiers of power supply.

ii) As signal diode in communication ckt.

iii) As varactor diode in radio and TV receivers.

iv) As a switch in logic ckt used in computer

vii) Define level trigger and edge trigger.

Ans.:- **(for each definition 1 mark)**

Edge trigger:- the data transfer from i/p to o/p of flip-flop at the +ve or –ve edge of clock pulse is called edge trigger.

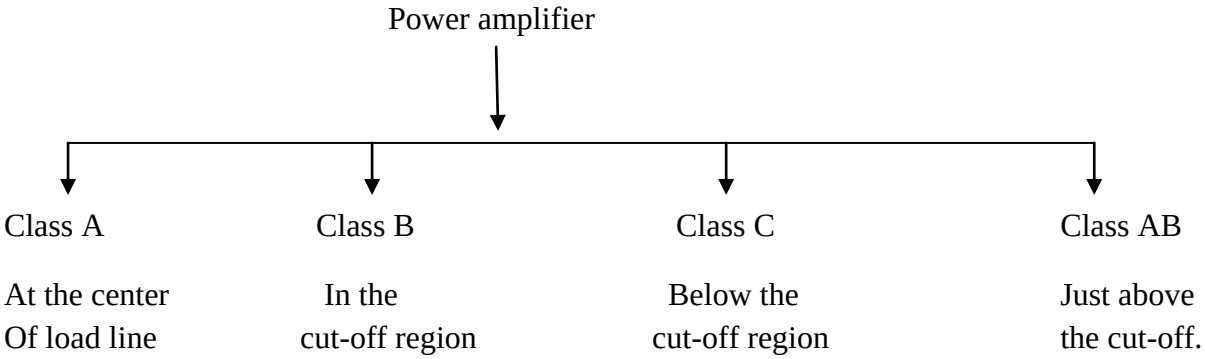
Level trigger:- the o/p responds to i/p as long as the clock is present is called level trigger.

viii) Give the classification of power amplifier on the basis of operating point.

Ans.:- **(01 marks for classification, ½ mark each for operating point)**

Class A :- Operating point is exactly at the center hence o/p of waveform is exactly same as i/p amplification is good efficiency – 25 – 50 %.

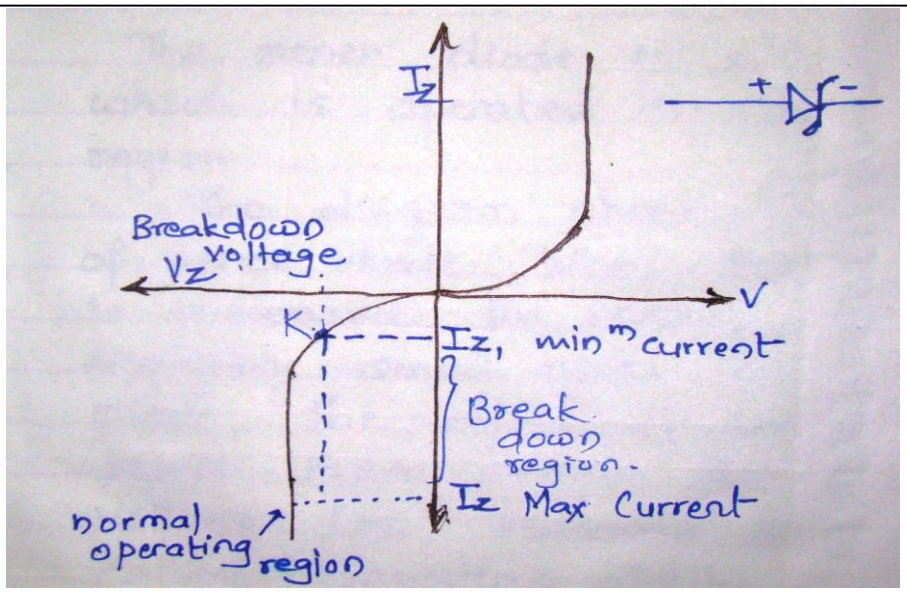
Class B:- Operating point is at collector cut-off voltage efficiency – 18 %.



Q. 1. B) Answer any TWO of the following. (2x4 = 8 marks)

i) Explain the working principle of zener diode with respect to its characteristics.

Ans.:- (Diagram of graphical of chara. – 2 marks, expl. – 2 marks)



The zener diode is silicon PN junction diode which is operated in reverse breakdown region.

The diagram shows the characteristics of zener diode. When the reverse voltage is increased, the reverse current remains negligibly small up to 'knee point '. At this point the effect of breakdown process begins from bottom the knee, the breakdown voltage (Vz) remains constant. this is called regulating ability.

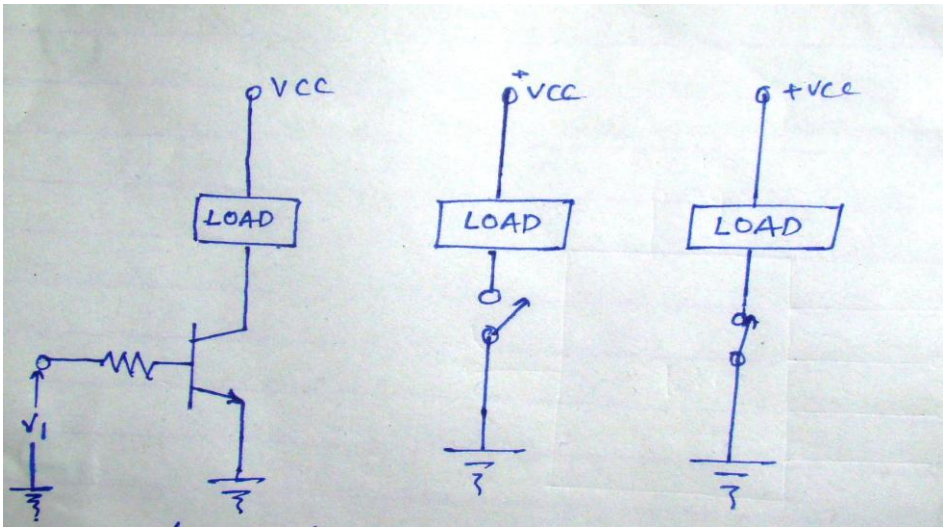
ii) Compare H. W. R. C. F. W. R. and Bridge rectifiers**. (any 4 points)**

Ans.:- **(each point for 01 mark)**

Points	**H.W.R.**	**C.F.W.R.**	**BRIDGE RECTIFIER**
No of diodes	1	2	4
PN of diode	Vm	2Vm	Vm
DC o/p voltage	0.318 Vm	0.636 Vm	0.636 Vm
Ripple factor	1.21	0.482	0.482
Ripple frequency	2 fin	2fin	2fin
Transformer utilization factor	0.287	0.693	0.812

iii) Draw and explain transistor as a switch circuit.

Ans.:- **(diagram – 2 marks, explanation. – 2 marks)**



When using BJT as a switch, two level of control signal are employed. In this process transistor operated in two region i) saturation, and ii) cut – off. As shown as fig. Vi , the control signal is applied to BE junction.

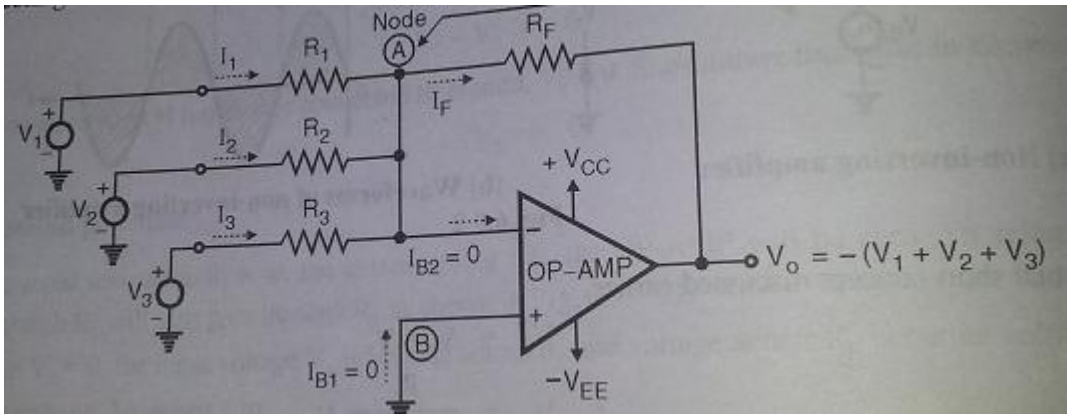
When Vi = 0 the BE junction is reversed biased and hence transistor acts as open switch.

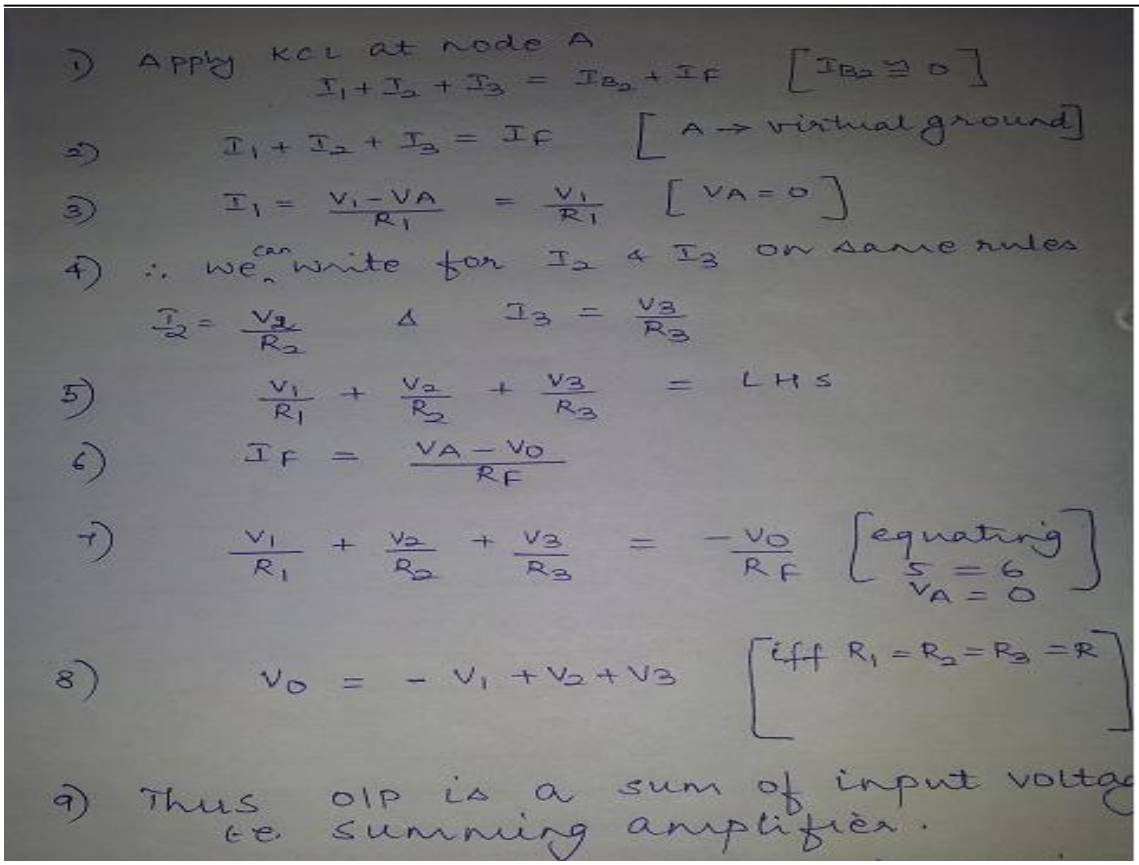
When Vi = 1 the BE junction gives forward biased. The transistor goes in to saturation region, and its acts as a closed switch.

Q2) Attempt any four **(16 M)**

i) Draw neat circuit diagram of op-amp as summing amplifier and derive the expression for 3 inputs applied

Ans: - **(2 M for diagram, 2 M for derivation)**

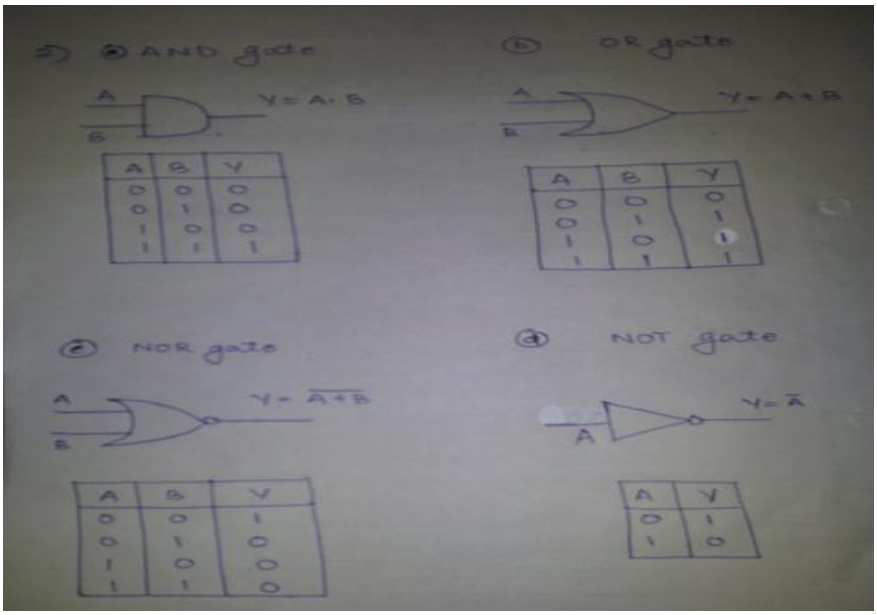




ii) Draw the symbol of following gates with their truth table:

a) AND gate b) OR gate iii)NOR gate iv) NOT gate

Ans:- **(1 M for each gate symbol & TT)**



iii) With the help of circuit diagram explain monostable multivibrator using IC 555 timer

Monostable M/V using 555 timer IC

Ans:- **(2 M for ckt, 2 M for expln)**

i) It is known as monostable since it has only one stable state.

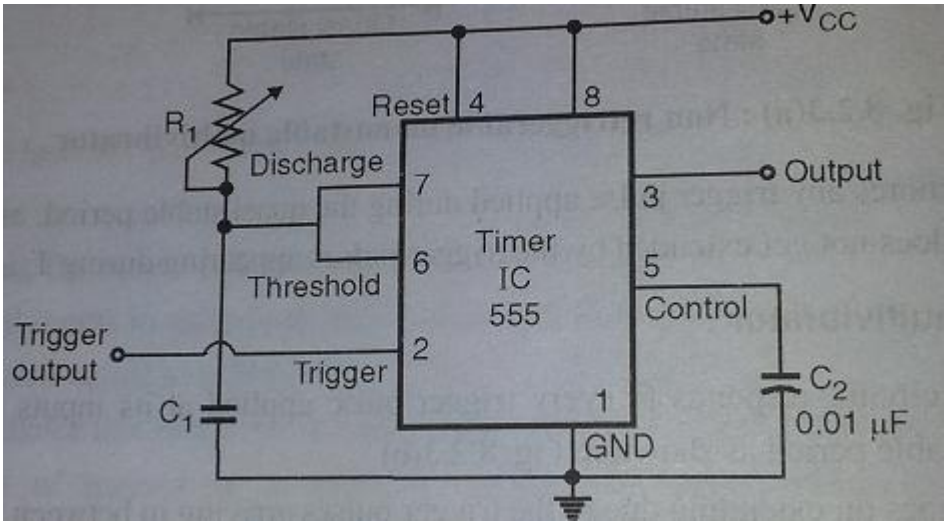
ii) Initially is in its stable state ie say 0V

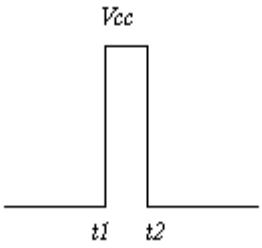
iii) A –ve trigger pulse is applied, i/p voltage goes below 1/3 Vcc.

iv) C1 starts charging, o/p is high.

v) When Voltage at C1 is 2/3 Vcc, S-R FF resets and C1 starts discharging

vi) O/p goes low.





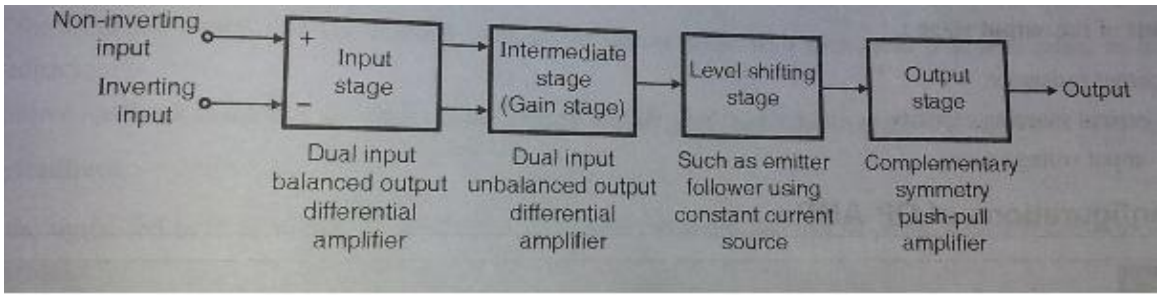
Monostable o/p

T_{ON} time = 1.1 RC

Where in our ckt R=R1, C=C1

iv) Draw and explain block diagram of op-amp. Give its two specifications

Ans:- Op amp **(BD for 2 M, expln for 1M, 1M for specs)**



1) Op amp is basically a differential amplifier ie it amplifies voltage which is differentially present at its input terminals.
2) Input stage is a dual input, balanced output differential amplifier.
3) The input stage provides high input impedance.
4) The second stage provides an additional gain to the amplifier.
5) The third stage is a level shifter stage to bring any level shift to zero volts w.r to gnd.
6) The last stage is a power amplifier and provides low resistance.
7) Specs : High input resistance, low o/p resistance, high CMRR, high gain, high bandwidth, high slew rate.

v) Differentiate regulated and unregulated power supply and define line regulation and load regulation

Ans:- **(2M for 2 pts comparison, 1 M for each def)**

Parameter	**Regulated Power supply**	**Unregulated Power supply**
O/p Voltage	Remains constant	Fluctuating, does not remain constant
Ripple content	Less	high
o/p voltage change	Does not change with temp, input voltage, and load	Changes with all the parameters

a) **Load regulation :** The load regulation is defined as the change in output voltage when the load current is changed from zero(no load) to max(full load) value.
L.R. = $(V_{NL} - V_{FL})$ / V_{NL} * 100

b) **Line regulation :** The line/source regulation is defined as the change in regulated load voltage due to change in line voltage in a specified range of 230V , 10% tolerance at a constant load current.
S.R = $(V_{LH} - V_{FL})$ (Load voltage with high line and low line voltage)

% SR = S.R/ Vnom * 100 (Vnom is nominal load voltage)

vi) Draw the circuit diagram of RC phase shift oscillator and write the expression for frequency.

Ans: - **(2M for diag , 2M for theory)**

RC phase shift oscillator

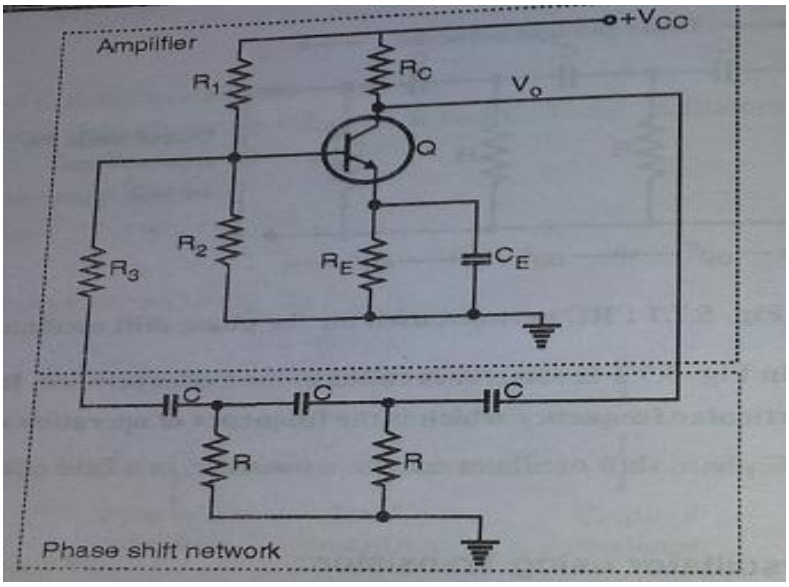
1) It consists of a CE amplifier and 3 RC phase shift network.

2) The amplifier provides 180^0 phase shift and remaining 180^0 is provided by the RC network, each provides 60^0 phase shift.

3) Total phase shift for a oscillator is 360^0.

4) $F = 1 / 2\pi RC$

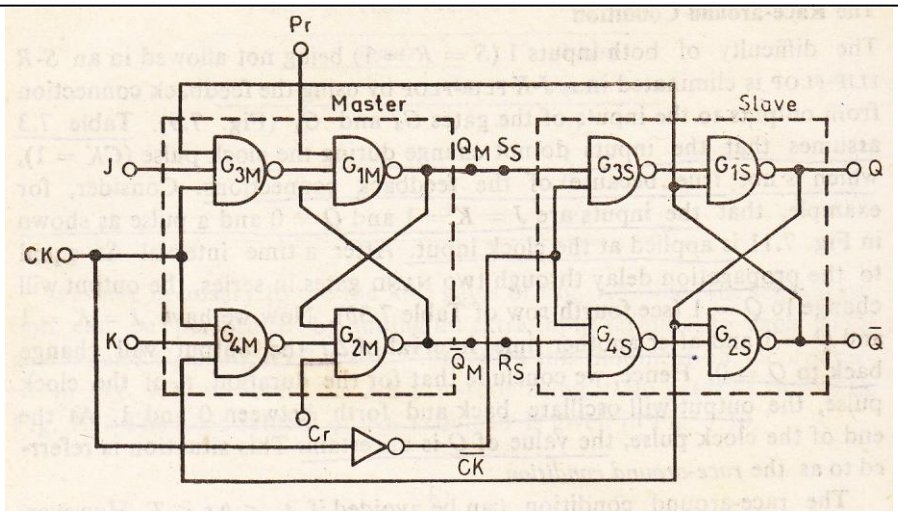
5) RC phase shift oscillator is widely used in audio frequency range , few Hz to several Hz around 200 KHz.



Q3) **. Attempt any two** **(2X8= 16)**

i) Draw master slave JK flip-flop and explain in detail.

Ans: **(Diagram 02 marks, explaination 02 marks)**



Data Inputs J_n	Data Inputs K_n	Outputs Q_n	Outputs $\bar{Q}_n$	Inputs to S–RFF S_n	Inputs to S–RFF R_n	Output Q_{n+1}
0	0	0	1	0	0	0
0	0	1	0	0	0	1 $= Q_n$
1	0	0	1	1	0	1
1	0	1	0	0	0	1 $= 1$
0	1	0	1	0	0	0
0	1	1	0	0	1	0 $= 0$
1	1	0	1	1	0	1
1	1	1	0	0	1	0 $= \bar{Q}_n$

Table.1a

Inputs J_n	Inputs K_n	Output Q_{n+1}
0	0	Q_n
1	0	1
0	1	0
1	1	$\bar{Q}_n$

Table 1.b

Explanation:-

A master-slave J-K flip-flop is a cascade of two S-R flip-flops with feedback from outputs of the second to the inputs of the first . positive clock pulses are applied to the first flip-flop and the clock pulses are inverted before these are applied to the second flip flop.

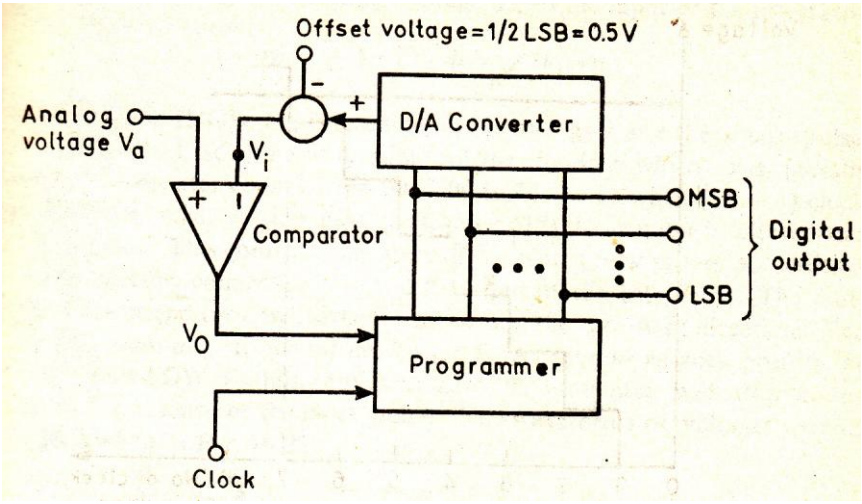
When CK=1,the first flip-flop is enabled and the outputs Q_M and $\overline{Q_M}$ respond to the inputs J and K(table 1a) . At this time, the second flip-flop is inhibited because its clock

is low. When clock goes LOW the first flip-flop is inhibited and second flip-flop is enabled because now its clock is HIGH. Therefore the output Q and **Q follow** the outputs Q_M and **Q_M respectively (table 1b) .As** second flip –flop follows the first one, it is referred to as the slave and the first one as the master.

ii) Explain successive approximation type of ADC with suitable diagram. Give its two advantages.

Ans: (**Diagram 02 marks, explaination 01 mark, application 01 mark)**

(Note: Small relevant explaination is expected.)



It consist of comparator which serves the function of the scale, the output ,used for setting the programmer. This output is converted into equivalent analog voltage from which the offset voltage is subtracted it is then applied to the inverting input of comparator. The output of comparator change only when clock pulse is present.

Advantages:

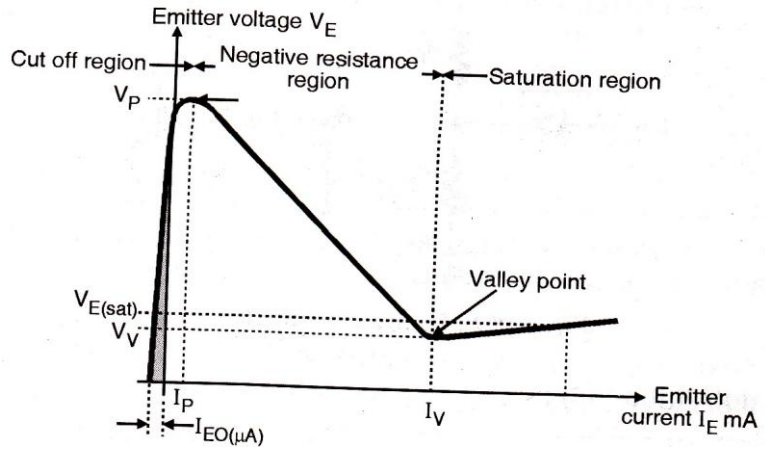
a) Conversion time is very short.

b) Conversion time is constant and independent of the amplitude of analog signal V_A

iii) Draw and explain UJT characteristics circuit diagram and also define V_p, I_p ,V_{valley}, I_{valley}

Ans: (**Diagram 2marks, explaination 02marks)**

(Note: in characteristics show the mention points also gives its definitions in explaination).



The characteristics are shown in diagram.

For emitter potentials less than V_P (peak point potential) the UJT is in the OFF state magnitude of IE is very less (equal to I_{EO}).
the current I_{EO} corresponds to reverse leakage current I_{CO} of the bipolar transistor. This region is known as the cut-off region.

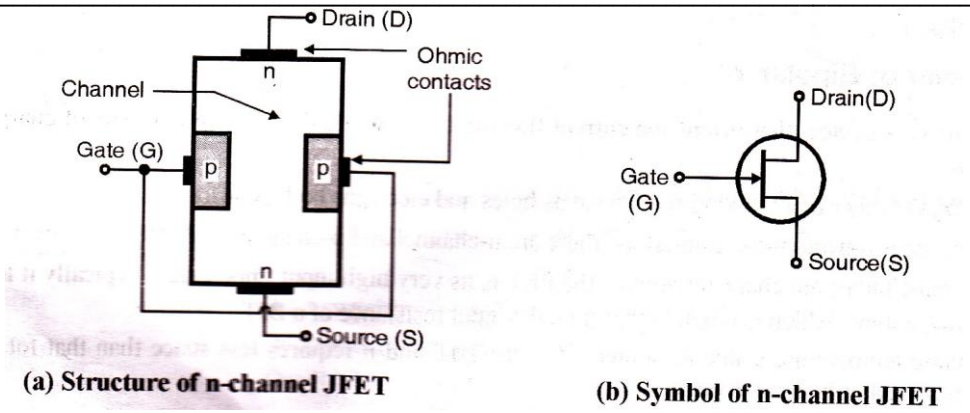
As emitter potential increases and reaches $V_P = (\eta V_{BB} + VD)$ the UJT starts conduction. Then with increase in emitter current IE the emitter voltage decreases. The voltage is reduced because of reduction in RB1with the increase in the value of IE. This region is called negative resistance region.

With the further decreased in voltage the valley point will be reached and device goes in saturation region. Voltage had current at valley point is called V_{VALLEY}, I_{VALLEY} respectively.

Q4) Answer any four **(4 * 4 = 16)**

i) Explain construction and working of n-channel JFET with diagram

Ans: (**Diagram 2marks, working -2marks)**



(a) Structure of n-channel JFET **(b) Symbol of n-channel JFET**

A semiconductor bar of n-type material is taken and ohmic contacts are made to the ends of the bar. These terminals named drain and source.

On the both sides of n-type bar heavily doped (p+) regions have been formed by alloying or by diffusion to create a p-n junction. Both these p+ regions are connected together and via ohmic contact the gate terminal is brought out.

The supply voltage is connected between the drain and source terminals of JFET hence current is caused to flow along the length of the n-type bar. This current is due to majority carriers which are electrons.

ii) Draw the block diagram and explain working of welding control circuit.

Ans: (**Diagram:2 marks explaination 2 marks.)**

(Note: any one type of welding control system explaination is expected).

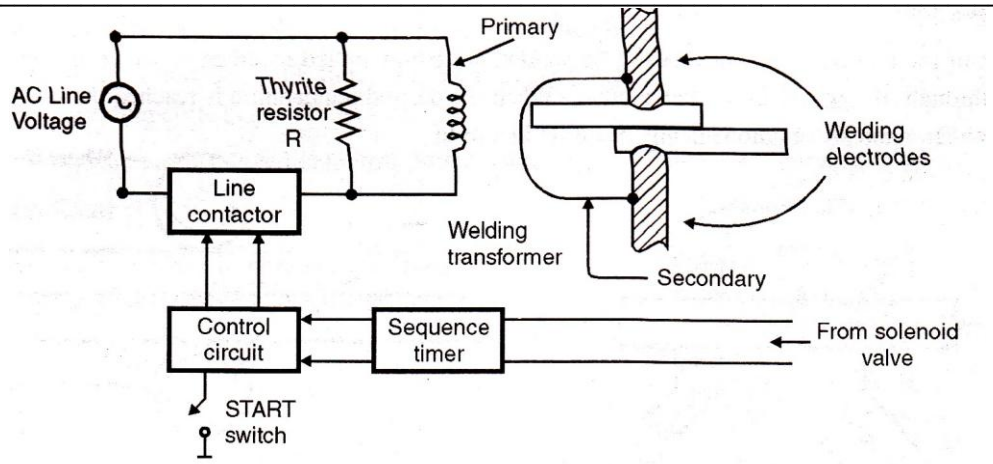
There are three types of welding systems.

1. Forge welding system

2. Fusion welding system

3. Resistance welding system

Basic circuit of resistance circuit welding



Resistance welding: -

Resistance welding is a process in which two or more metal pieces are welded by passing a short duration high value ac or dc current through the area of contact between the metal pieces.

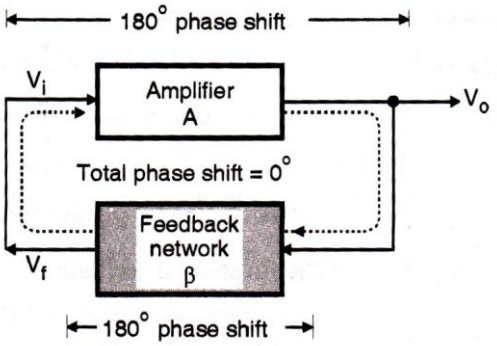
- The "line contactor" is basically a controlled switch which connects the ac mains voltage across the primary winding of the "welding transformer" only during the welding interval.
- The "welding transformer" is a step down transformer which supplies current which is "welding current" in the range of several hundred to several hundred to several thousands of amperes.
- "Thyrite resister" it is a connected across the primary winding transformer in order to protect its insulation against high voltage spikes.
- The control circuit decides the instants at which the line contactor is turned on and off i.e. the welding time.
- The line contactor may use a "controlled switch" like ignitron tubes or thyristors in order to control the magnitude of the welding current.

iii) State the need of an oscillator. Explain barkhauson's criteria with respect to block diagram of oscillator

Ans: (Need of oscillator- 1 mark, Block Diagram -1marks, working -1mark barkhauson's criteria -1marks)

1. Many electronic circuits require frequency signal varying from few hertz to several Mhz.. This is achieved by oscillator easily at low voltage signal. As oscillator is an electronic circuit which generate continuous sinusoidal and non-sinusoidal signal without any input.

2. Block diagram



3. An oscillator consist of an amplifier and a phase shifting network. The amplifier receives the output of phase shifting network. The amplifier amplifies it phase shift it through 180°and applies it to the input of phase shifting network. The phase shift network shifts the amplifier output through another 180° and attenuates it before applying it back to the amplifier input. Due to this total phase shift of 360° ,the feedback becomes positive which gives rise to oscillation.

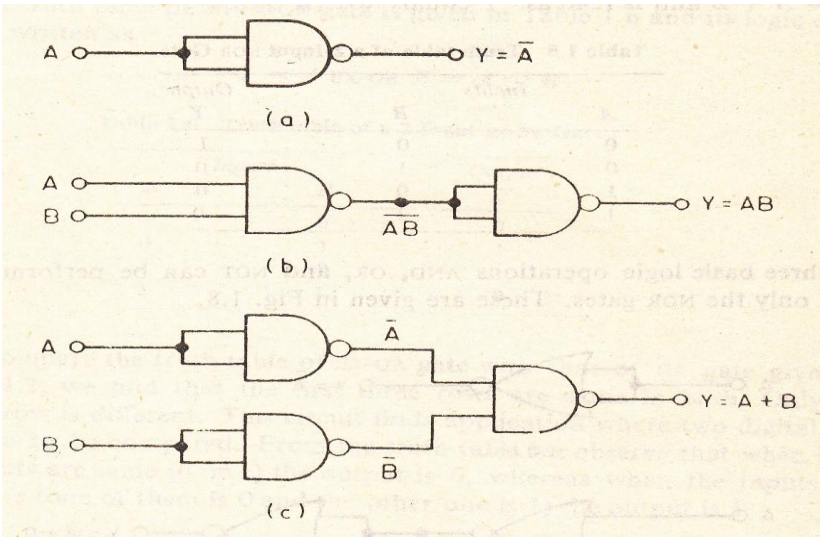
4. Barkhauson's criteria ; a)total phase shift should be 360° or 0°,b) loop gain greater than and equal to unity

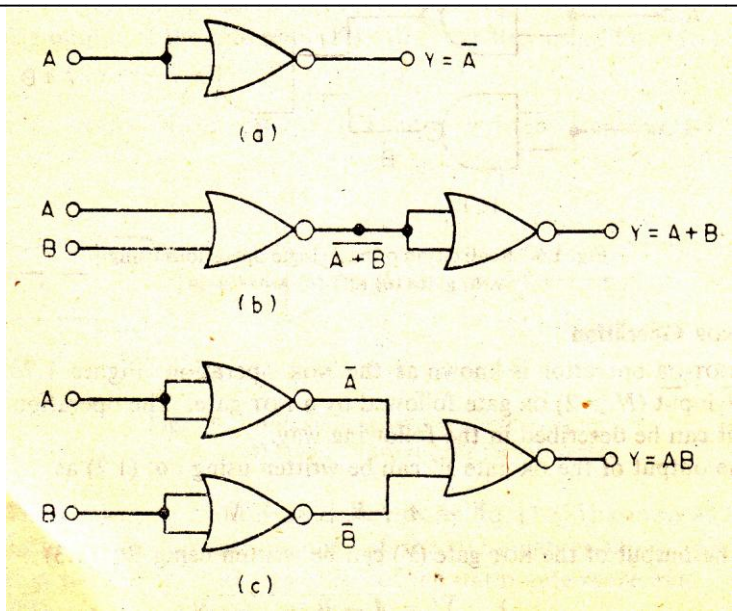
$$|A\beta| >= 1$$

iv) Why NAND and NOR gates are called as universal gates? Justify.

Ans: Any Boolean expression can be realized by using AND, OR, NOT logic. From NAND and NOR gates any logical expression related to AND, OR, NOT logic can be realized instead of using these gates as shown in diagram below.

Diagram



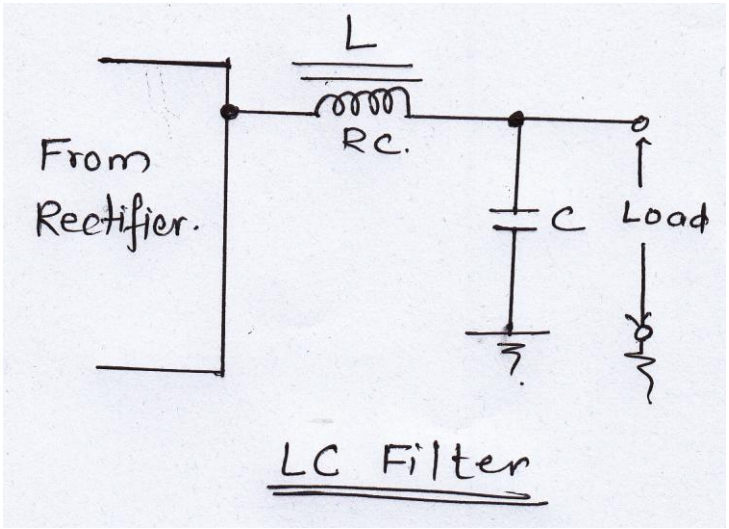


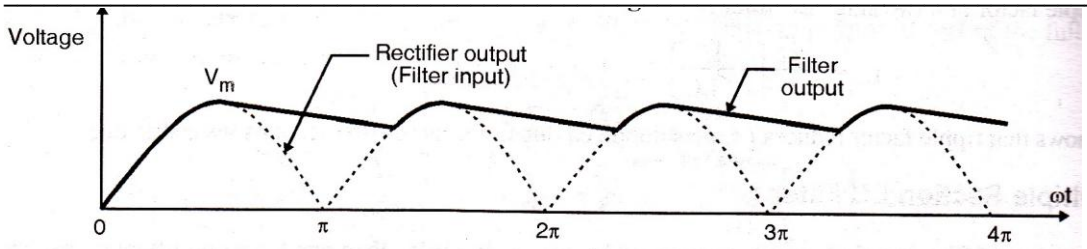
v) Enlist the types of filter and explain LC filter with the waveform.

Ans: (types -1mark, Diagram -1 mark,waveform-1mark,explaination 1 mark.)

Types of filters.:

a. Capacitor input filter
b. inductor filter
c. L-C filter
d. R-C filter
e. Π filter

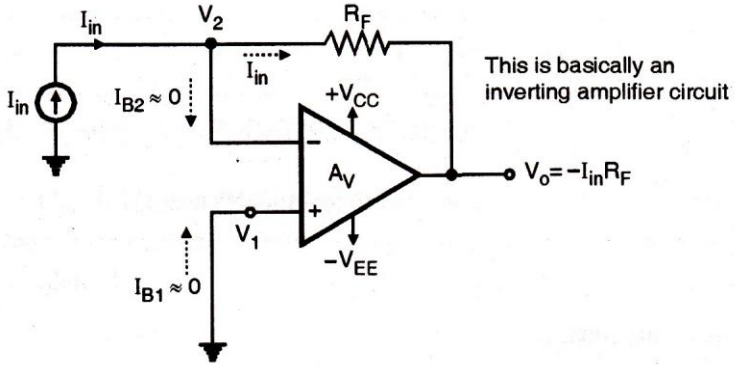




(b) Input output voltage waveforms

L-C filter: this is also term as tank filter. It is combination of two filters. Where inductor filter is preferred for low values of Rand capacitor input filter for high value of load resistance. The L-C filter can give low ripple factor irrespective of the load. This is because series inductor offers a high reactance to that harmonics component in the output and parallel capacitor provides a low reactance by pass path for them. This reduce ripple to minimum.

vi) Explain current to voltage converter with circuit diagram.
Ans : diaram- 2 mark,explaination-2 mark



The current to voltage convertor is as shown in diagram. This circuit is special case of inverting amplifier. The gain of inverting amplifier is given by

A_{VF} = (-Rf/R1) X Vin

But V1=V2 and V1= 0 as the non-inverting terminal is connected to ground v2=0

So whole output appear across R1.

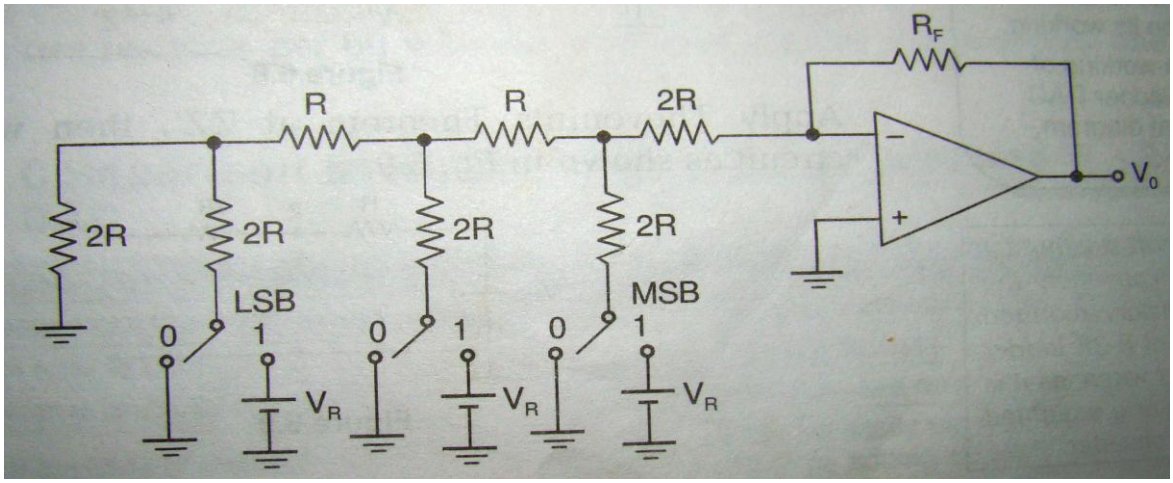
And we get Vo=-R_f I_{in}

Q. 5. Answer any FOUR. (4 x 4 = 16 marks)

i) Explain DAC with respect to R – 2R ladder network method.

Ans.:- R- 2R ladder DAC:- (diagram – 2 marks, equation -2 marks)

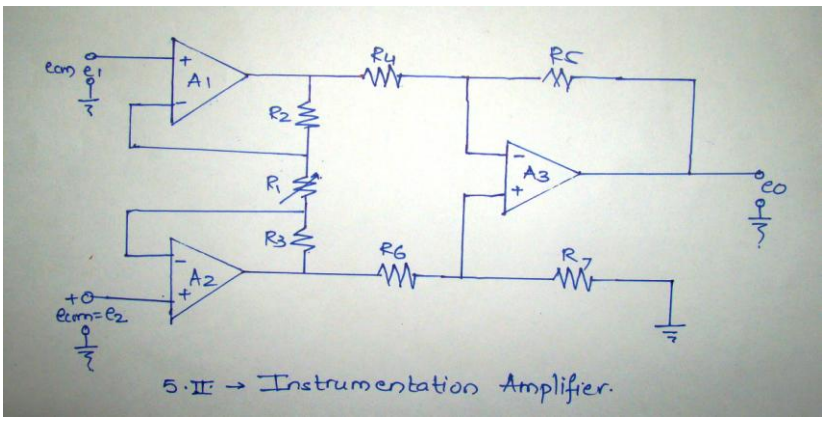
This network overcomes the problems of weighted resister network. It is also a resistive network to produce binary weighted current but uses only two value of resistor as R and 2R. it uses a ladder network containing series and parallel combination of two resistors of values R and 2R. the i/p to the resistor network are applied through digitally controlled switches. A switch is in position 0 or 1 corresponding to the digital i/p for that bit position 0 or 1 respectively.



$$V_o = -\left(\frac{R_F}{3R}\cdot\frac{V_R}{2^3}b_0 + \frac{R_F}{3R}\cdot\frac{V_R}{2^2}b_1 + \frac{R_F}{3R}\cdot\frac{V_R}{2^1}b_2\right)$$

ii) With the help of block diagram, explain instrumentation amplifier. Give its 2 application.

Ans.:- **(Block diagram – 1 ½ , expl. – 1 ½ , any 2 application- 1 mark)**



The bridge circuit is DC excited as shown in fig.

For balance bridge

Vb = Va

Rc / RB = RT / RA.

Resistor RA = RB = RC

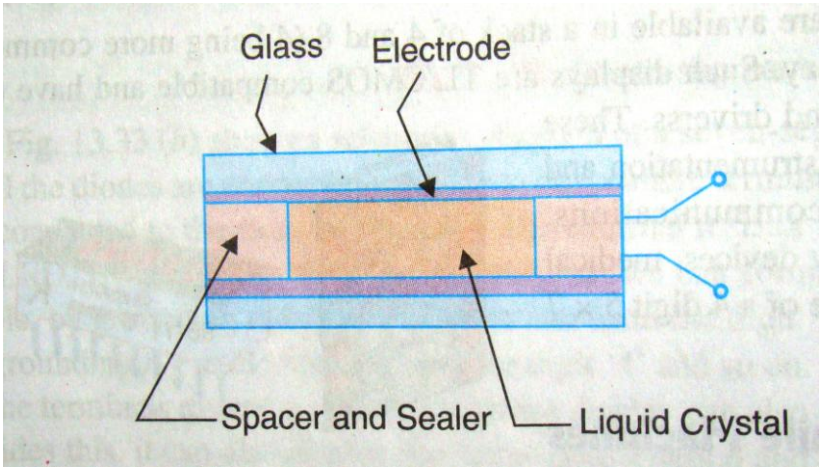
The bridge is balanced initially at a desired ref. condition as a physical quantity to be measured changes the resistance of transducer also changes which cause to unbalance. The o/p voltage of bridge is a function of change in resistance of the transducer.

The o/p voltage Vab of the bridge is then applied to the differential instrumentation amplifier composed of three op-amps. The voltage follower preceding the basic differential amplifier help to eliminate loading of bridge ckt.

The i/p amplifier A1 and A2 acts as i/p buffers with unity gain for common anode signals ecm and with a gain of (1+2R2/R1) for differential signals. CMRR is achieved by following stage because of differential amplifier. Optimum CMRR can be obtained by adjusting R6 / R7 ensure R5 / R4 = R7 / R6.

iii) Explain the working principle of LCD display with diagram.

Ans.:- **(diagram – 2marks, expl. – 2 marks)**



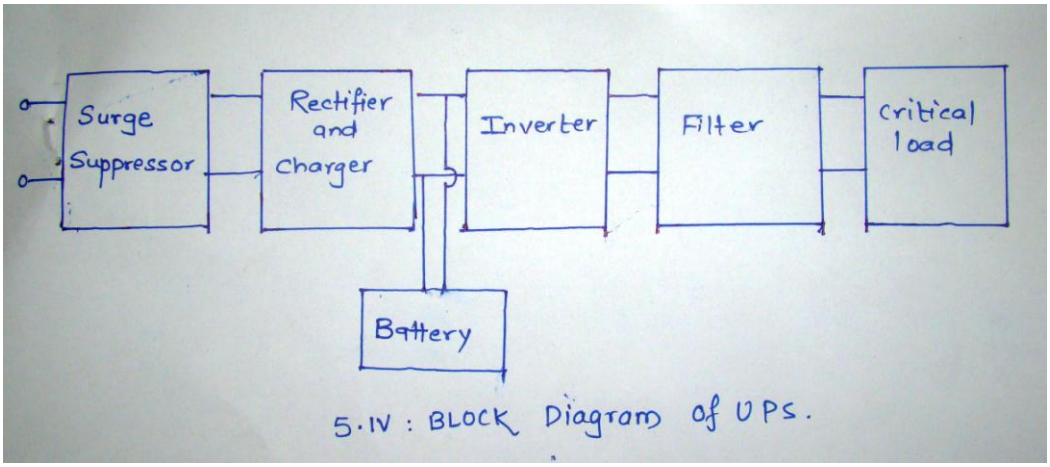
- A liquid crystal cell consists of a thin layer of a liquid crystal.
- This layer is sandwiched between two glass sheets with transparent electrodes deposited in their inside faces.
- When one glass is transparent other glass sheets has reflecting coating. This means one glass cell is transitive type and other cell is reflection type.
- The illumination of LCD is depends upon external source.
- There are two types of displays

a) Field effect display:- where when it is energized the energized area absorbs light incident on it and gives localized black display.

b) Dynamic scattering display:- when it is energized the modules of energized area of the display becomes turbulent and scattered light in all directions. The activated area take on frosted glass appearance resulting in silver display and unenergized areas remains translucent.

iv) Draw the block diagram of UPS and define online and off line UPS.

Ans.:- (2 marks – diagram, 1 mark – each definition)

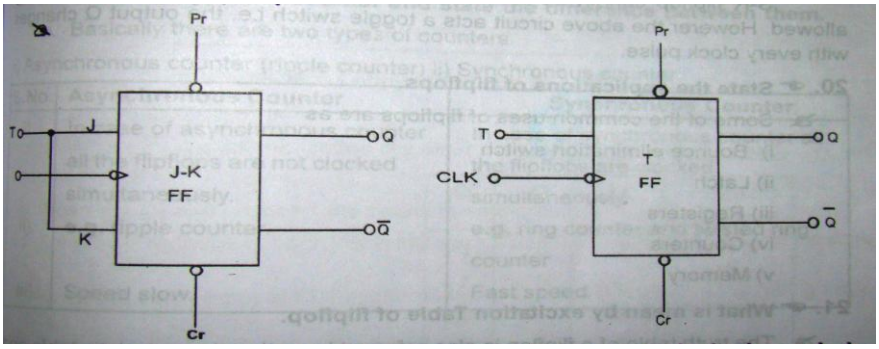


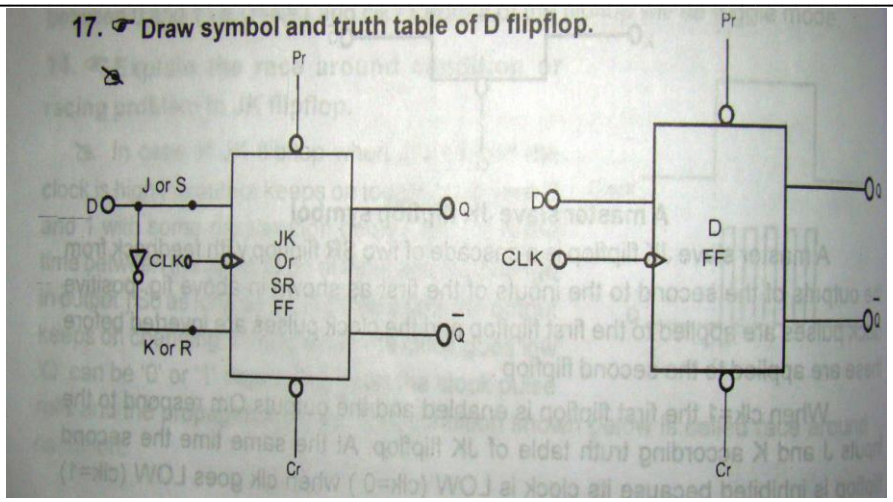
Online UPS :- the load is always connected to the inverter through UPS static switch which is normally ON switch. It turns OFF when UPS system fails. Thus then it has to be by pass and mains should directly be connected to load. In this case mains static off switch used to bypass UPS.

OFF line UPS:- in off line UPS Mains static switch is used which normally ON. It connects AC main directly to the load when the mains is ON.

v) Show that how JK flip-flop is converted into D flip-flop and T flip-flop.

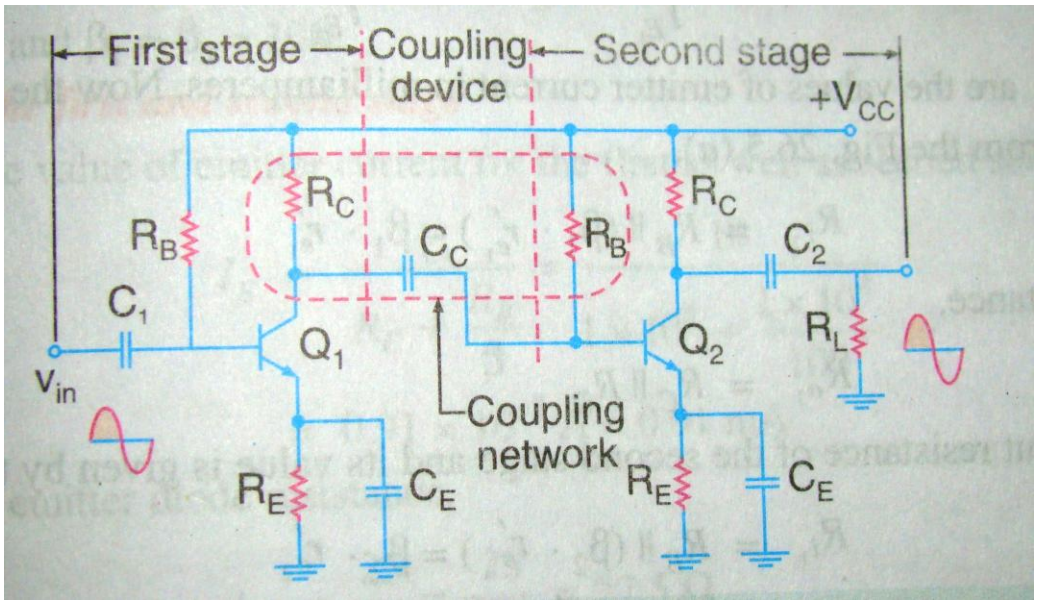
Ans.:- **(** D –flip- flop conversion – 2 marks, conversion to T flip flop – 2 marks)





vi) Draw the ckt diagram of two stage RC coupled amplifier. If A1 and A2 are the amplification factors of amplifier 1 and 2. What will be the amplification factor of 2 stage RC coupled amp?.

Ans.:- diagram 3 marks and amplification factpr -1 mark



Amplification factor = $A_1 + A_2$, $A_1 - A_2$ in terms of dB (any 1 written is right.)

Q 6) Attempt any two **(2 * 8 = 16 M)**

i)

a) Compare conductor, semiconductor, insulator (any four)

Ans:- (any four points 4 marks)

Parameter	**Conductor**	**Semiconductor**	**Insulator**
Free electrons	More	Due to doping	No free e-
Flow of current	High	In between conductor & insulator	Does not allow
Forbidden energy band	Overlapping or 0 eV	Approx 1 eV	High , > 5 eV
Temp coeff of resist	+ve	-ve	-ve
examples	Al, Cu	Si, Ge	Paper, Glass

b) Define intrinsic semiconductor and extrinsic semiconductor with 2 examples of each

Ans:- (1 marks for each definition and 1 mark each for example)

I**ntrinsic Semiconductor (or pure)** : Intrinsic semiconductors are the semiconductors in their purest form.

Example : Silicon, Germanium

Extrinsic Semiconductor: Intrinsic semiconductors when doped are extrinsic semiconductors. This is done to improve its conductivity.

They are of two types: n type and p type. (2 M)

ii) Compare CB, CE, CC configuration

Ans:- (8 marks for 8 points)

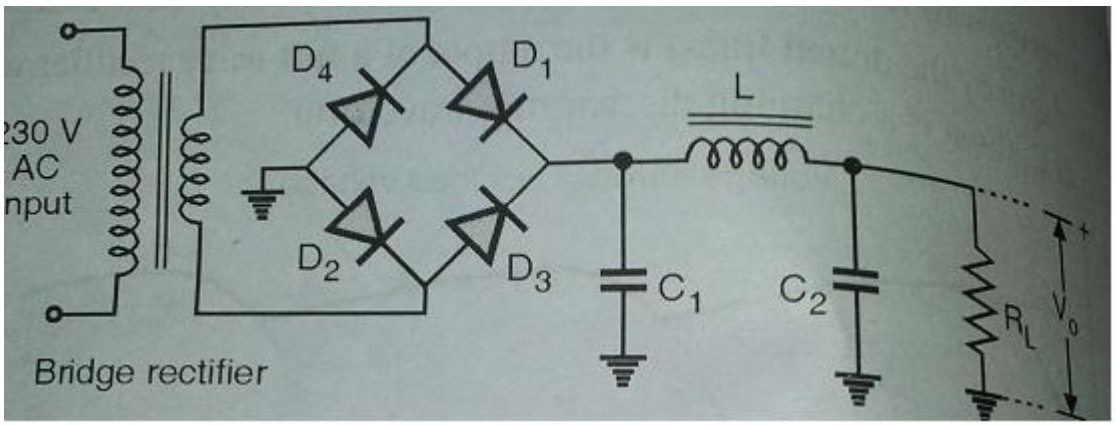
Parameter	**CB**	**CE**	**CC**
i/p current	I_E	I_B	I_B
o/p terminal	Collector	Collector	Emitter
Current gain	$\alpha \sim 1$ (less than 1)	$\beta \sim 50 - 1000$ (High)	$\gamma = \beta + 1$ (V high)
Voltage gain	High	high	Less than 1
I/p resist	low	medium	V high
o/p resist	High	medium	low

Phase shift between i/p and o/p	0 deg	180 deg	0 deg
application	Low noise pre amp	Audio amp	Buffer amp

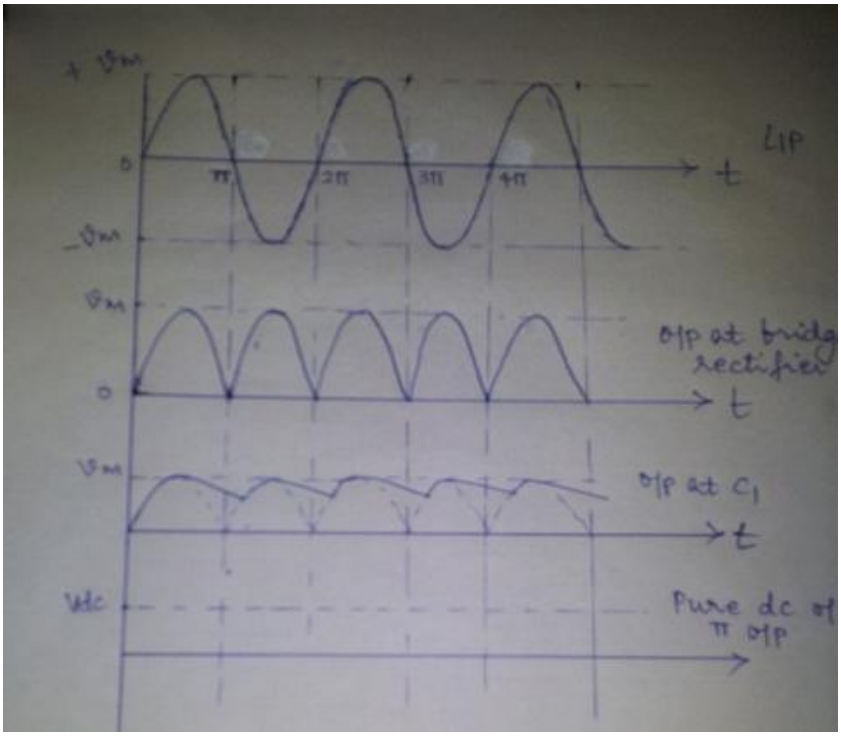
iii) With circuit diagram explain bridge full wave rectifier with 'π ' filter. Draw its waveform

Ans: - **(3M for diagram, 3 M for waveform, 2 M for explanation)**

Bridge rectifier with π filter



Waveform :-



Explanation:-

i) A full wave bridge rectifier has 4 diodes to form a bridge.

ii) It offers full wave rectification.
iii) D_1 & D_2 conduct for the +ve half cycle and D3 & D4 conduct for the –ve half cycle.
iv) π filter is formed by C_1, L, C_2, they form a pi shape.
v) C_1 acts as a C filter and L & C_2 form a LC filter.
vi) Due to the three filtering elements, the ripple content is reduced and we get a pure dc voltage.