Important Instructions to examiners:

1) The answers should be examined by key words and not as word-to-word as given in the model answer scheme.
2) The model answer and the answer written by candidate may vary but the examiner may try to assess the understanding level of the candidate.
3) The language errors such as grammatical, spelling errors should not be given more Importance (Not applicable for subject English and Communication Skills).
4) While assessing figures, examiner may give credit for principal components indicated in the figure. The figures drawn by candidate and model answer may vary. The examiner may give credit for any equivalent figure drawn.
5) Credits may be given step wise for numerical problems. In some cases, the assumed constant values may vary and there may be some difference in the candidate's answers and model answer.
6) In case of some questions credit may be given by judgement on part of examiner of relevant answer based on candidate's understanding.
7) For programming language papers, credit may be given to any other program based on equivalent concept.

Q1. a) Attempt any six of the following. **12M**

i) Define collector efficiency of power amplifier. **2M**

Ans: Collector efficiency of power amplifier :- **(η_c)**

It is the ratio of a.c. power delivered to the load, to the power supplied by the d.c. source to the transistor.

$$\eta_c = \frac{\text{A.C power delivered to the load}}{\text{Power supplied by the d.c. source to the transistor.}}$$

ii) State effect of positive feedback on gain of amplifier.

Ans: Due to the positive feedback the gain of amplifier is increased **2M**

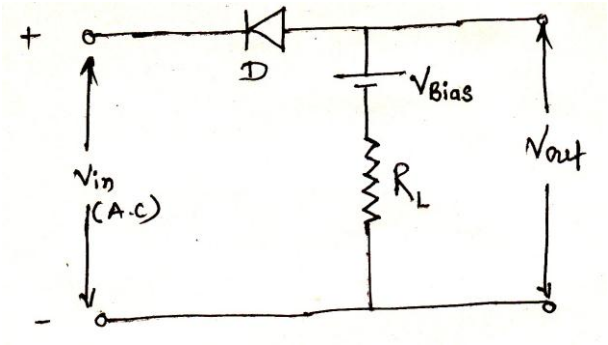
$$A_{vf} = \frac{A}{1-\beta A}$$

A_{vf} Is gain with positive feedback increased by the factor $(1 - \beta A)$.

iii) Draw neat circuit diagram of Biased positive clipper.

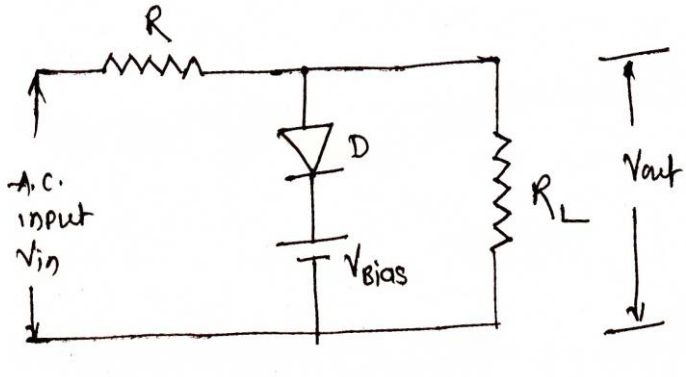
Ans: *[Note: either biased series or parallel positive clipper cab be considered.]*

Series biased positive clipper **2M**



OR

Parallel biased positive clipper **2M**



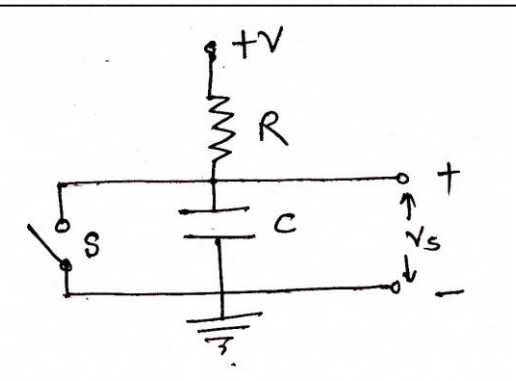
iv) Define turn on time.

Ans: Turn on time: It is the summation of rise time (t_r) and delay time (t_d) **2M**

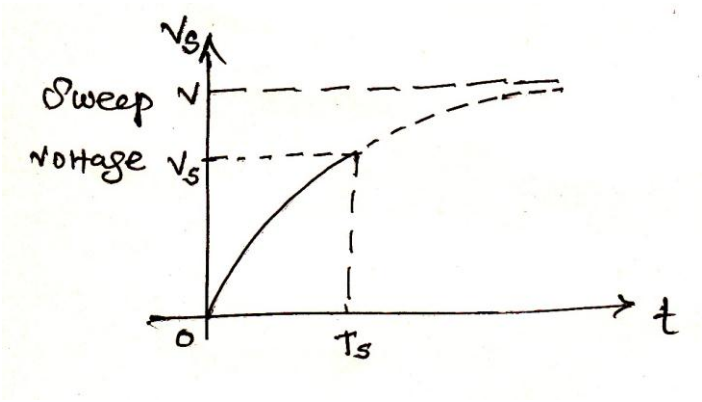
$T_{on} = t_r + t_d$

v) Draw neat waveform and circuit of exponential sweep generator.

Ans: circuit of exponential sweep generator: - **1M**



Waveform: **1M**



vi) In case of biased clipper neither negative half cycle nor any part of ac is obtained on CRO, state tentative fault in the circuit.

Ans*: [Note: either Biased parallel or Biased series clipper can be consider]* **2M**

In Biased parallel clipper –

may be due to internal short (fault) of diode neither negative half cycle nor any part of ac is obtained on CRO.

OR

In Biased series clipper –

May be due to internal open (fault) of diode neither negative half cycle nor any part of ac is obtained on CRO.

vii) State application of negative resistance generator.

Ans: application of negative resistance generator:

[Note: any four applications are expected ½ mark each]

a) Sweep generator (UJT relaxation oscillator)

b) Trigger device for SCR_s and Triacs.

c) Phase control.

d) Timing circuits.

e) Non sinusoidal oscillator.

f) T.V.

g) CRO

viii) What is multivibrator ? State defferent types of multivibrator.

Ans: multivibrator: **1M**

A multivibrator is an electronic circuit used to implement a variety of simple two state systems such as oscillators, time sweep and flip flop.

OR

A relaxation oscillator using two transistors with the output of each coupled to the input of the other through resistance – capacitance element or other elements to obtain in phase feedback voltage.

[Note: from above any one can be consider.]

Different types of multivibrator: **1M**

1. Astable multivibrator
2. Monostable multivibrator
3. Bistablr multivibrator.

ix) Write expression for frequency of oscillation of Colpitt's oscillator.

Ans: frequency of oscillation of Colpitt's oscillator: **2M**

$$f = \frac{1}{2\pi\sqrt{LC_T}}$$

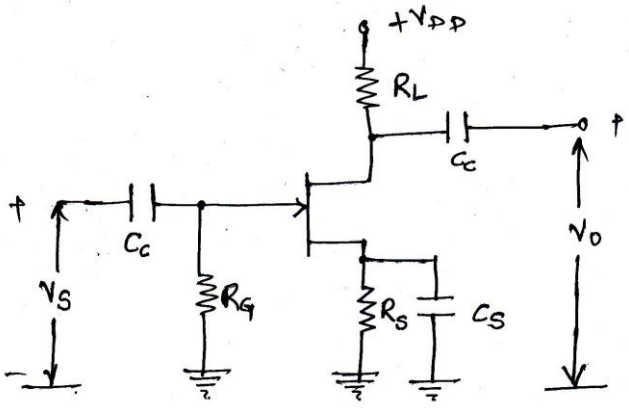
Where $C_T = \frac{C1 . C_2}{C_1 + C_2}$

b) Attempt any two of the following. **8M**

i) Draw and explain self-bias FET amplifier.

Ans: Self-bias FET amplifier:

Circuit: - **1 ½ M**



Circuit analysis:- **1M**

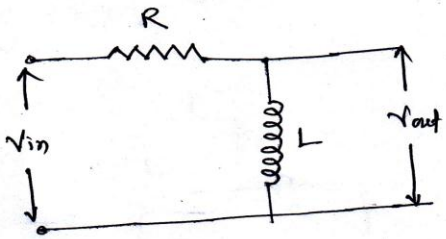
- R_G keeps gate voltage at 0V and its large value prevent loading of ac signal source.
- Biased voltage is created by drop across R_s.
- Bypass capacitor C_s keeps the source of the JFET efficiency at ac ground.

Circuit operation: - **1 1/2M**

- When a small ac signal is applies to the gate, it produced variation in the gate to source voltage. This produces variation in the drain current.
- For positive half cycle input, reverse biasing across gate and source decreases; therefore drain current increases for negative half cycle input, reveres biasing across gate and source increases, therefore drain current decreases.
- Thus smaller change in gate voltage produces large change in the drain current, this produces large output across the load. Hence FET acts as an amplifier.

ii) Draw RL differentiator circuit. Write expression for output voltage. State condition for good differentiation.

Ans:



2M

Expression for output : **1M**

$V_{out} \propto \frac{d}{dt}(V_{in})$

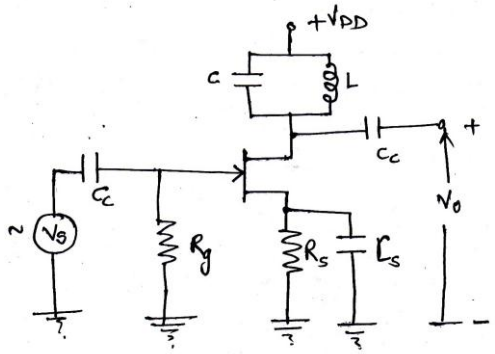
Condition for good differentiation : **1M**

i) $X_L << R$

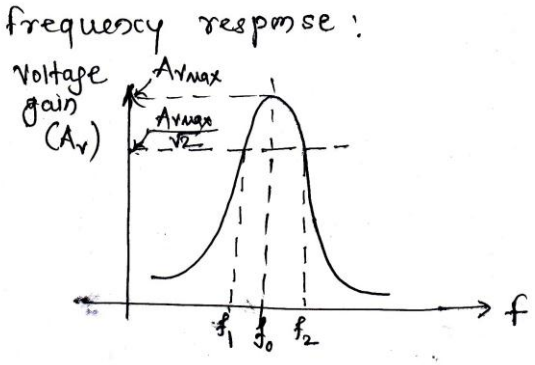
ii) T i.e. $\frac{L}{R} << T$

iii) Draw neat circuit diagram of single tuned amplifier using FET. Draw frequency response.

Ans: circuit diagram of single tuned amplifier using FET **2M**



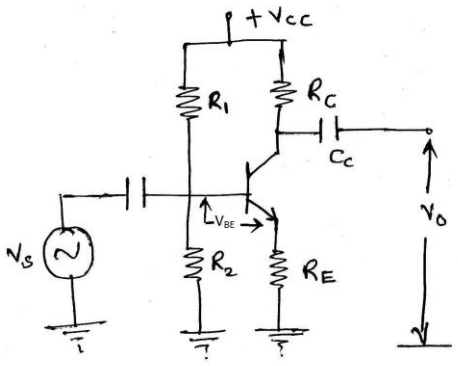
Frequency reponse: **2M**



Q2. Attempt any two of the following. **16M**

a) Draw circuit of current series feedback. State its effects on input and output resistance. Describe its operation.

Ans: **3M**



Effect of current series negative feedback: **2M**

Due to current series negative feedback input resistance is increased and output resistance is also increased.

Mathematically it can be written as

$$R_{if} = R_i(1 + AB)$$ AND

$$R_{of} = R_o(1 + AB)$$

Operation: **3M**

Negative current series feedback improves the high frequency response of amplifier. It processes the input impedance as well as output impedance of amplifier.

By removing C_E i.e. bypass capacitor across emitter resistance in C_E amplifier it becomes a current series negative feedback amplifier.

When the signal is applied at the input, resulting ac emitter current produces voltage drop across R_E. This voltage drop opposes the signal as it is in opposite direction to the signal. The voltage feedback is proportional to the current i_e.

Therefore circuit provides negative current feedback.

Apply KVL in input loop

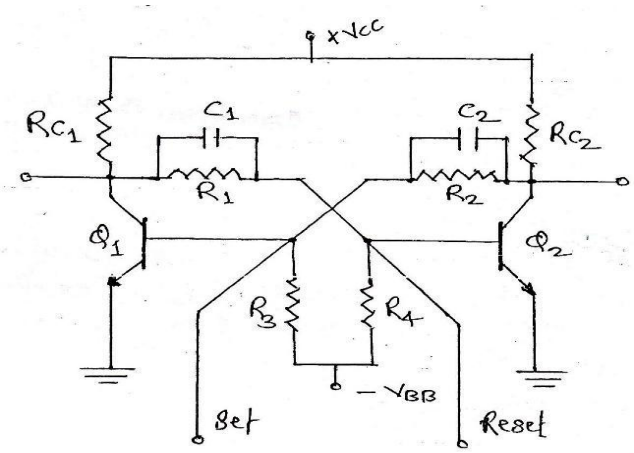
$V_S - V_{BE} - i_eR_E = 0$

$V_{BE} = V_S - i_eR_E$

Thus V_{BE} is the input which is source voltage minus drop across R_E which is due to output current hence current series negative feedback.

b) Draw circuit diagram of bistable multivibrator and describe it working. Draw input and output waveforms.

Ans: It is also called flip flop. The bistable multivibrator is used for counting and storing of binary information in computer circuit. **3M**



The bistable multivibrator has two stable states and can stay in any one of these two states as long as the power is supplied it changes to other state only when it receives a trigger from outside.

Figure shows the circuit of bistable multivibrator using two NPN transistors Q_1 and Q_2. Here output of transistor Q_1 is coupled to the input of transistor Q_2 through resistor R_1.

Similarly the output of a transistor Q_2 is coupled to the base of transistor Q_1 through R_2.

The capacitor C_1 and C_2 known as speed up capacitor. The base resistors of both the transistors are connected to a common source - V_{BB}

The output of a bistable multivibrator is available at the collector terminal of the transistor Q_1 and Q_2. However the two outputs are the complements of each other.

Operation: - **3M**

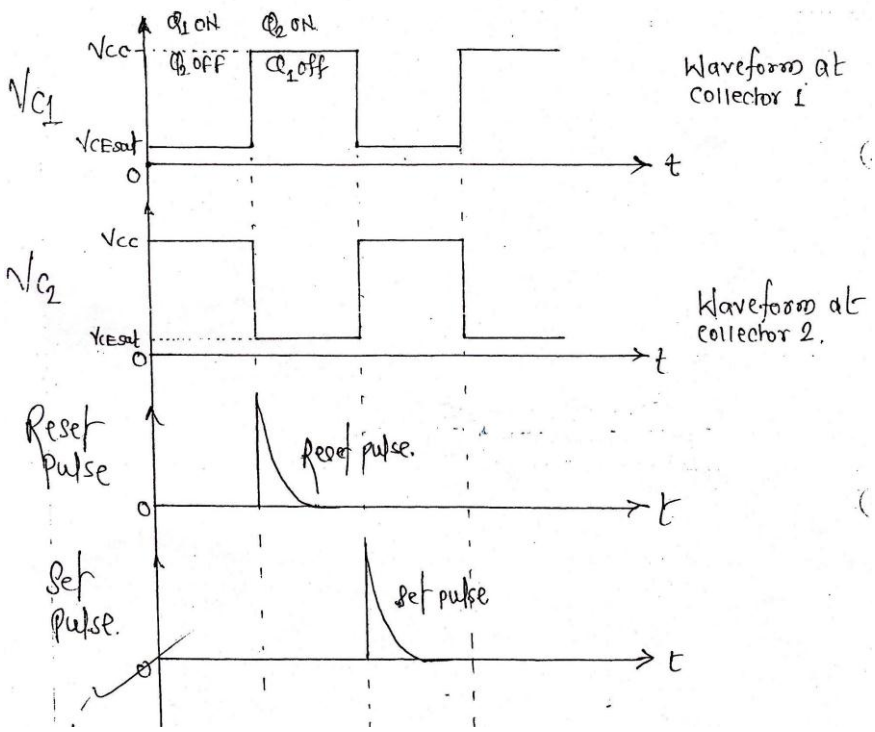
When the V_{CC} supply is switched 'ON', one of the transistor will conducting more than the other. Then because of feedback action one transistor will be driven into saturation and other into cutoff.

Let us assume, the transistor Q_1 is in saturation ('ON') and Q_2 is cutoff ('off'). It is a stable state of the circuit and will remain in this state, till a trigger pulse is applied. A negative pulse is applied to the set input will turn off the transistor Q_1 and Q_2 to ON. A similar action can also be achieved by applying a positive pulse at reset input.

Suppose a positive pulse is applied at the reset input. It will cause the transistor Q_2 to conduct. As the collector voltage of Q_2 falls, it cut off the transistor Q_1. Thus the circuit switches to other stable state i.e. a state where Q_1 is off and Q_2 is ON.

Now if a positive pulse is applies at the set input, it will switch the circuit back to its original stable i.e. Q_1 ON and Q_2 OFF.

Waveforms: **2M**

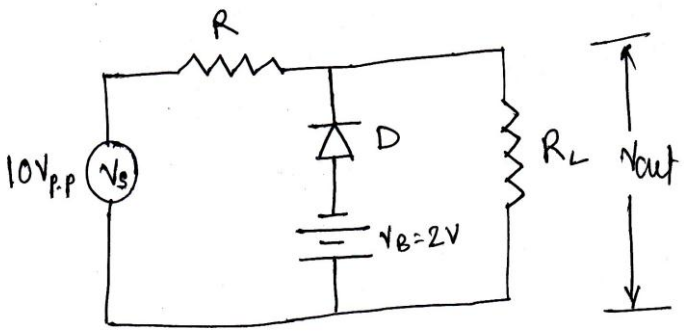


c) Draw circuit diagram and waveform of

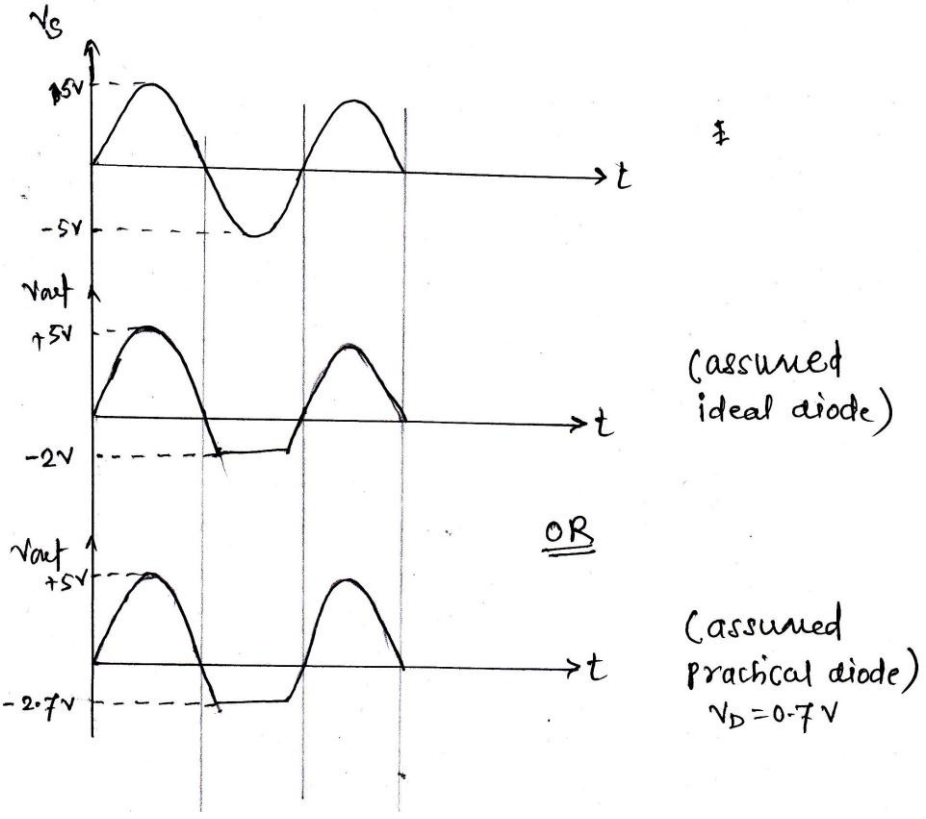
i) Biased shunt negative clipper with input voltage $10V_{p-p}$ V_B = 02V

ii) Biased series positive clipper with input voltage $10V_{p-p}$, V_B = 02V

Ans: Circuit of Biased shunt negative clipper **2M**

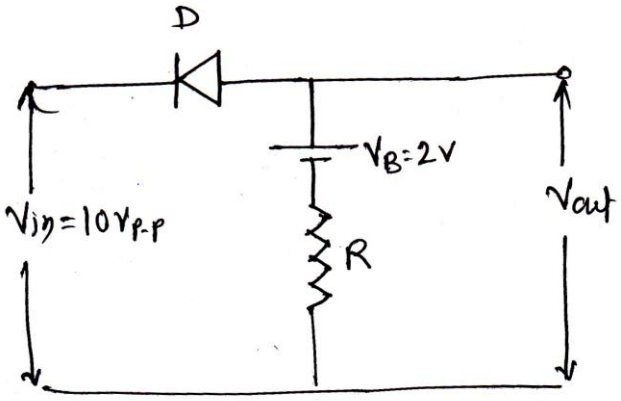


2M

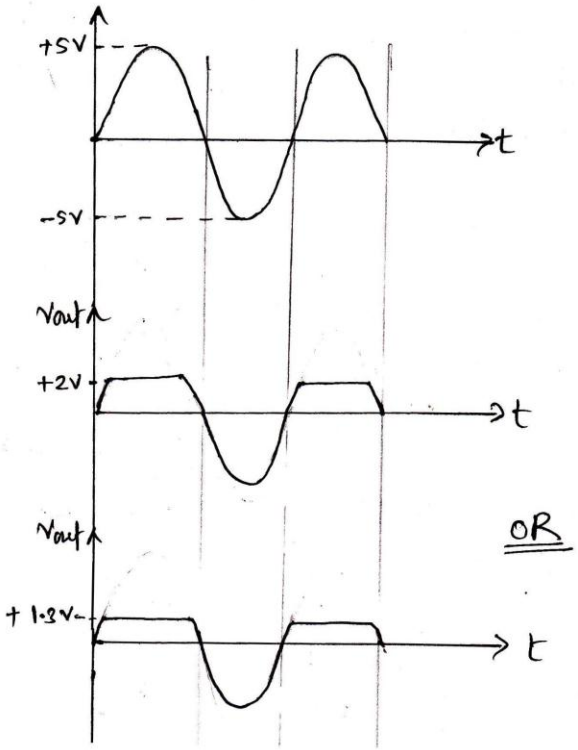


[Note: for output waveform any one case i.e. ideal diode or practical diode can be consider]

Circuit of Biased series positive clipper **2M**



2M



OR

(assumed ideal diode)

(assumed practical diode)
V_D=0.7V

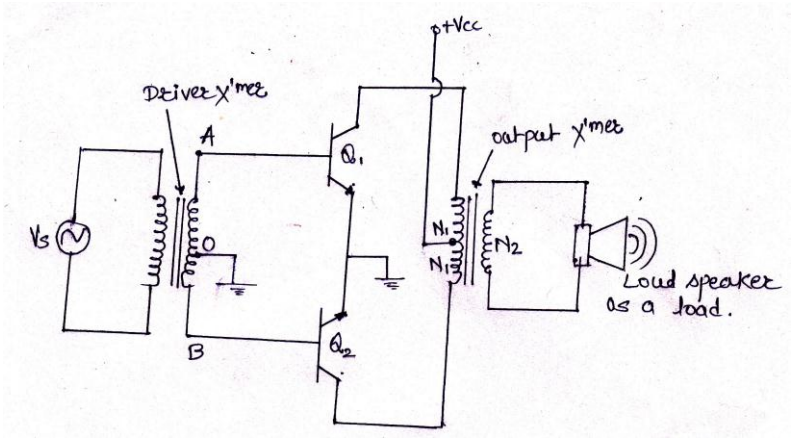
[Note: for output waveform any one case i.e. ideal diode or practical diode can be consider]

Q3. Attempt any two of the following:

a) Describe operation of class B-push power amplifier.

Ans: **4 M**

Class B-push power amplifier



Operation:

Fig. shows transformer coupled class-b push pull amplifies **4 M**

- If we use both the transistors of same type i.e. both are either p-n-p or n-p-n.
- Push pull amplifier shown fig a use n-p-n transistor
- The circuits consist of two centre tapped transformer
- The transformer on the I/P side is known as driver transformer & the other on the load side is known as O/P transformer.
- The I/P signal 'Vs' is applied to the primary winding of the i/p transformer.
- The operation of the circuit can be divided into two parts:

  1) Operation in the positive half cycle of i/p:
- In the positive half cycle of i/p, secondary voltage of the driver transformer, 'A' is positive & 'B' is negative.
- Base- Emitter junction of transistor Q1 is forward bias & Base- Emitter junction of Q_2 is Reverse Bias. i.e. Q_1 conducts & Q_2 turn off
- Thus base current for Q1 i.e Ib, will flow & Ib2 =o
- Hence the collector current I.e. IG will flow & IC2=0
- A positive sinusoidal voltage will appear across the load as shown fig
- The amplitude of the secondary load voltage is dependent on the primary to secondary turns ratio of o/p transformer

2) Operation in the negative half cycle of i/p:-

- In the negative half cycle of i/p 'A' is negative & 'B" is positive
- Base- Emitter junction of transistor Q_1 is Reverse Bias. & Base- Emitter junction of transistor Q_2 is forward bias
- The base current $Ib_1 = 0$ & Ib_2 will flow through transistor Q_2
- Thus in this half cycle Q_1 is OFF & Q_2 is ON
- Hence the collector current i.e.IC_2 flows through primary winding of o/p transformer & $IC_1 = 0$
- Hence a negative sinusoidal voltage will appear across the load.
- The amplitude of this secondary induced voltage is dependent on the turns ratio of the o/p transformer.
- The turns ration of each half of primary to secondary of the o/p transformer is $N_1:N_2$
- Thus at a time only one transistor will conduct.

b) Draw neat constructional sketch of N-channel depletion type MOSFET and explain its working principle

Ans: Fig (a) shows Construction of n-channel depletion type MOSFET **2M**

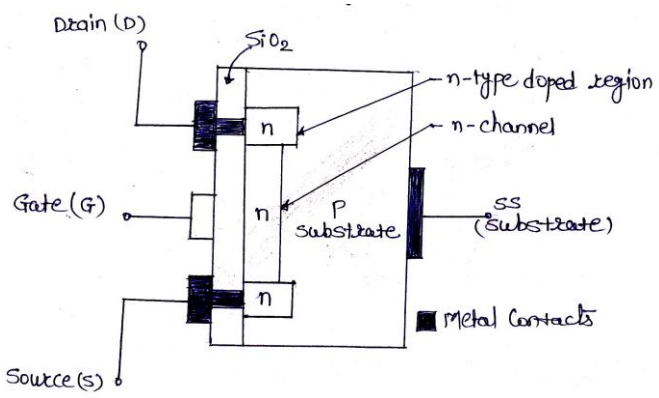


Diagram **3M**

[Note: 1½ + 1½ each diagram]

Fig (b) n- channel depletion type MOSFET with $V_{GS=0}$

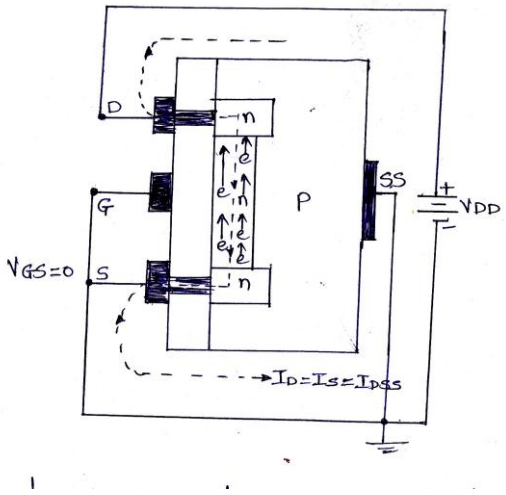
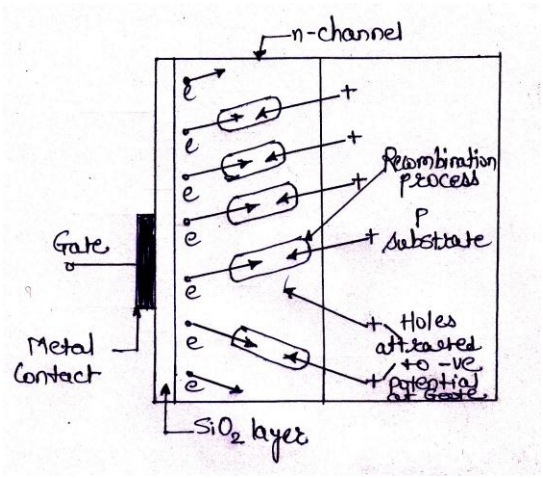


Fig (c) Effect of negative V_{GS}



Working **3 M**

- A P-type semiconductor material i.e. 'Si' is used as a substrate.
- Usually the substrate is internally connected to the source terminal.
- The drain & source terminals are connected to the n-type regions through the metallic contacts.
- These n-type regions are linked with each other by a n-channel as shown in fig (a)
- Fig. (b) shows n-channel D-MOSFET with $V_{GS = OV}$
- Gate, source & substrate terminals are connected to the ground point
- Thus $V_{GS = OV}$

- A positive voltage VDD is applied between drain & source terminals
- Due to the positive voltage is applied to the drain terminal, free electrons from the channel are attracted to the drain & the ID starts flowing
- Fig (c) shows effect of –ve V_{GS}
- If the gate voltage is made –ve, the gate will tend to repel the free electrons toward p-type substrate and attract holes from the substrate
- These electron and hole will recombine inside the channel as show in fig (c) this will reduce the no. of free electrons
- Therefore the In will decrease with increase in V_{GS}
- Depending on the magnitude of –ve bias V_{GS} a level of recombination between electrons & hole will occur
- This will reduce no of free electrons
- If gate voltage is +ve with respect to source the + V_{GS} will draw additional free electron from p-type due to reverse leakage current.
- Thus In will increase as we increase the positive V_{GS}
- Level of fee electron has been 'enhanced' due to +ve gate voltage
- Therefore the region is known enhancement region of operation & the region between cut off & saturation is known depletion region.

c) i) State testing procedure for transistorized sweep circuits.
ii) Draw neat diagram of biased combination clipper with waveforms.

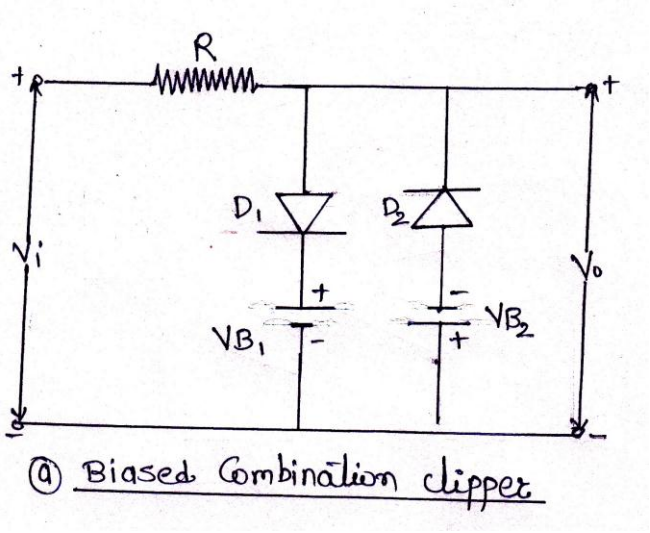
Ans: i)Testing procedure for transistorized sweep circuits are as follows:- **4M**

1. Check the dc supply voltage
2. Check the dc biasing of the transistor
3. If dc voltage are abnormal, the check the transistor as well as the resistors involved in the biasing circuits
4. If dc voltage are OK then observe the o/p waveform on CRO & measure the following characteristic of the sweep waveform:
   a) Linearity
   b) Peak magnitude of sweep.
   c) Frequency
   d) Frequency stability

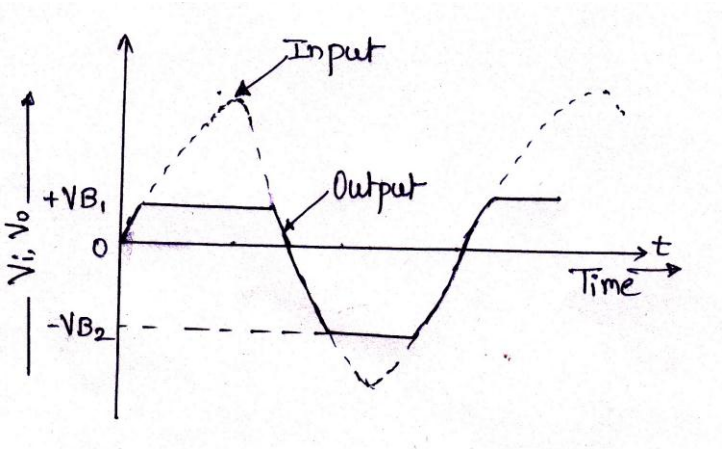
e) Distortion

5. if no –linear o/p sweep is observe, then check the components in the constant current source
6. If frequency is incorrect then check the value of charging current and sweep capacitors
7. If the waveform is distorted, then the check the charging current
8. If the frequency is not stable then check & change the transistor.

Ans : ii) Diagram of biased combination clipper with waveforms: **2 M**



2 M

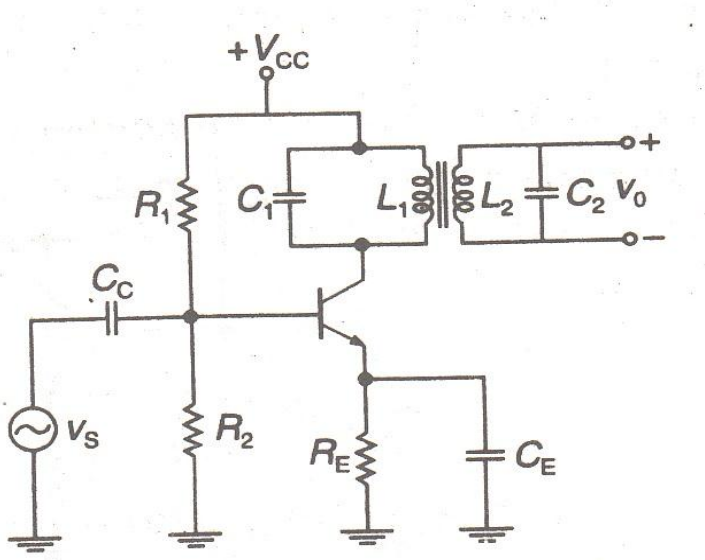


B Input & output waveforms

Q4. Attempt any two of the following: **16M**

a) Draw double tuned amplifier and describe it's working. Draw frequency response of the amplifier.

Ans: Diagram of Double tuned voltage amplifier: **3M**



Explanation: **3M**

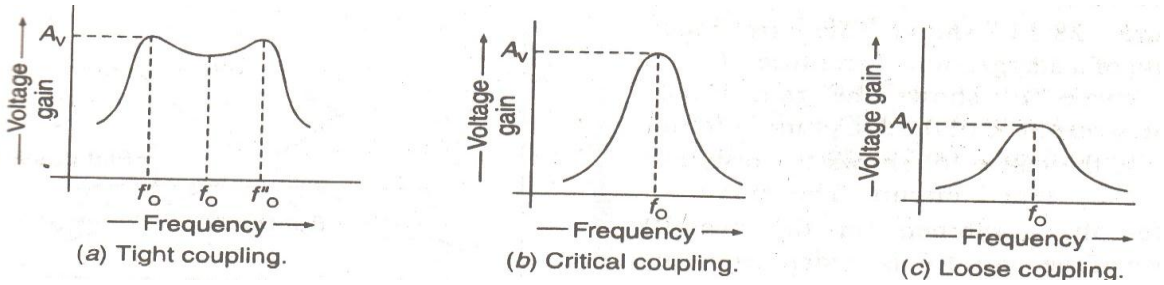
Above fig. shows the circuit of a double tuned voltage amplifier. It consists of transistor amplifier with two tuned circuits. One of the tuned circuits (i.e. L_1 C_1) is shown as the collector load and other (i.e. L_2 C_2) as the output. The resistor R_1, R_2 and R_E are used to provide d.c. currents and voltages for the transistor operation.

The signal to be amplified is applied at the input terminal through the coupling capacitor (Cc). the resonant frequency of the tuned circuit L_1 C_1 is made equal to that of the signal (by adjusting L_1 or C_1).

Under these conditions, the tuned circuit offers a very high impedance to the input signal as a result of this, a large output appears across the tuned circuit L_1 C_1. The output from this tuned circuit is inductively coupled to the L_2C_2 tuned circuit.

The double tuned voltage amplifiers are extensively used in intermediate frequency (IF) amplifiers in radio and television receivers.

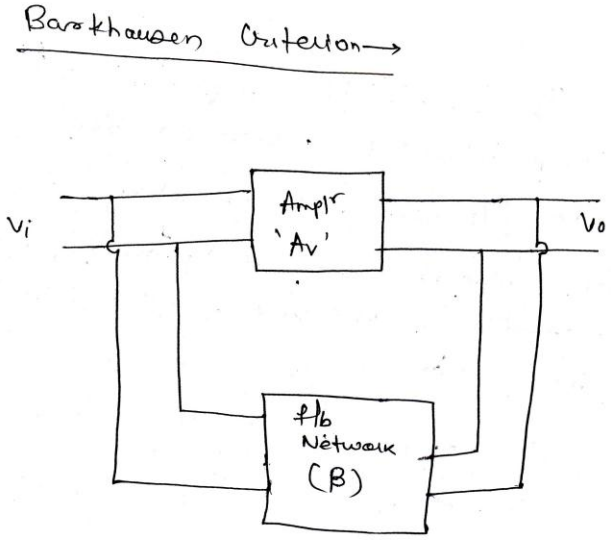
Frequency response of Double-tuned voltage amplifiers: **2M**



The frequency response of double tuned voltage amplifier depends upon its degree of coupling i.e. coefficient of coupling between the two tuned circuit fig a, fig b, fig c shows the frequency response of tuned circuit with different degrees of coupling like tight coupling , critical coupling and loose coupling. The tuned circuit of double tuned voltage amplifier is tightly coupled to each other and its frequency response is shown in fig a. which provides a high selectivity, high gain and relatively large bandwidth.

b) State Barkhausen criterion for oscillation. Draw and describe working principle of RC phase shift oscillator.

Ans: Block diagram:



Statement of Barkhausen criterion: **2M**

Above block diagram shows the basic block diagram of oscillator.

The Barkhausen criterion for sustained oscillation states that,

i) $\beta . Av = 1$

ii) $\angle\beta . Av = 0^0$ or 360^0

i.e. $\beta . Av = 1\angle 0^0$ or 360^0 .

OR

i) This means that; the loop gain i.e. $|AB| = 1$

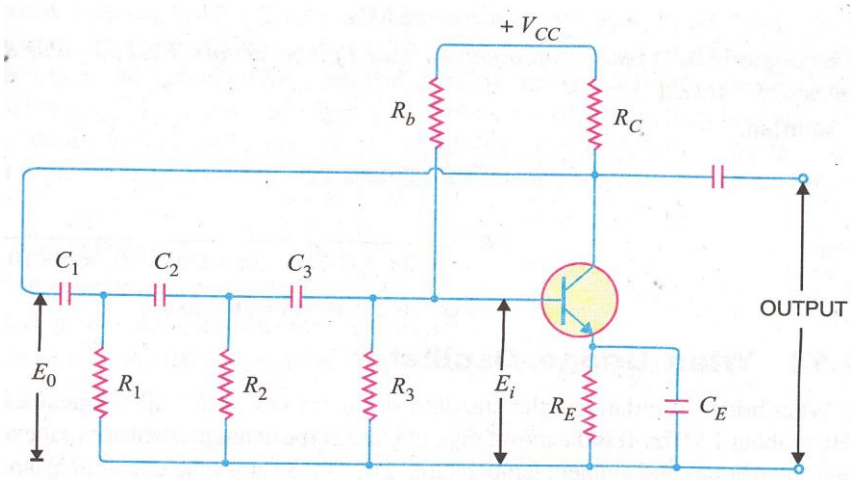
Where, Av = gain of the amplifier

β = feedback factor.

ii) The net phase shift around the loop should be zero or 360^0 i.e. feedback should be positive.

If a circuit doesn't satisfy any one of these conditions, sustained oscillations will not be produced.

Diagram of RC phase shift: **3M**



Explaination: **3M**

The above fig shows RC phase shift oscillator, it consists of single stage CE amplifier and RC phase shift network. The RC phase shift network consists of three sections R_1C_1, R_2C_2, R_3C_3. at some particular frequency, the phase shift in each RC section is 60^0 so that the total phase shift produce by RC network is 180^0.

Circuit Operation:

When the circuit is switch ON, it produces oscillations of frequency $f = 1/2\pi RC\sqrt{6}$ (if $R_1=R_2=R_3=R$ and $C_1=C_2=C_3=C$) the output E_0 of the amplifier is feedback to RC network which produces 180^0 phase shift and voltage E_i appears at its output which is applied to the transistor amplifier. The feedback fraction $\beta = E_i / E_0$.

A phase shift of 180 is produce by CE amplifier and remaining 180 are produce by RC network. As a result phase shift around the entire loop 360 (i.e. positive feedback)

The frequency of oscillation is given by,

$f = 1/2\pi RC\sqrt{6}$

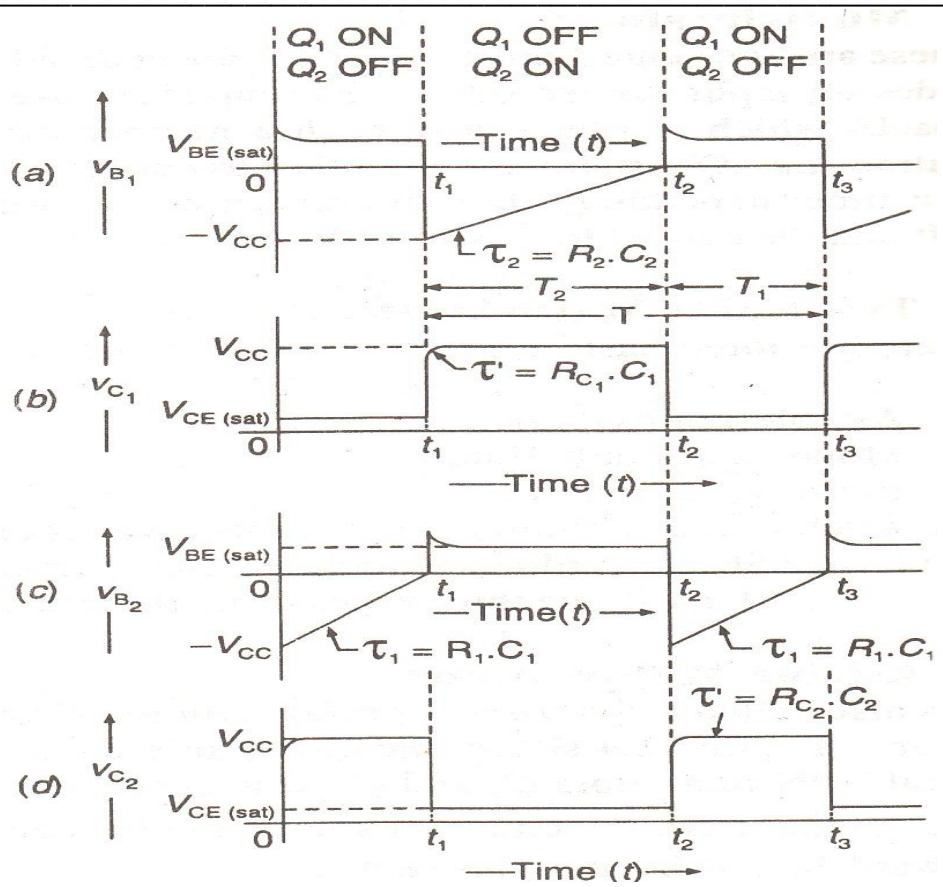
if $R_1=R_2=R_3=R$

$C_1=C_2=C_3=C$

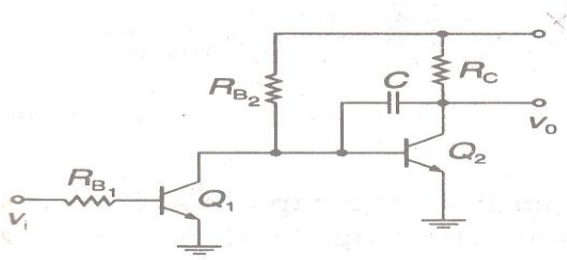
c) i) Draw neat waveforms of base and collector of astable multivibrator.

ii) Draw neat circuit diagram of miller sweep generator.

Ans: i) Wave forms of base and collector of generator **(1 waveform each 1mark)** **4M**



ii) Circuit diagram of miller sweep generator: **4M**



Q.5 Attempt any two of the following: **16M**

a) State advantages of push-pull amplifier over single ended power amplifier. State necessity of heat sink.

Ans: Advantages of push-pull amplifier over single ended power amplifier: **4M**

1. The circuit efficiency of a class- B push- pull amplifier is much higher than that of single ended amplifier.
2. The use of push-pull system eliminates even order harmonics in AC o/p signal
3. Output power per transistor is more as compared to single ended power amplifier.
4. There is no. DC component in the output signal. Therefore there is no possibility of transformer core saturation.

Necessity of heat sink: **4M**

The reverse saturation current in semiconductor device (transistor) charges with temperature, approximately doubles for every 10^0 C rise in temperature. This increase in collector current produces an increase in power dissipation at the collector base junction. This in turn, further increases the temperature of the collector base junction. Collector current Ic to further increase. This process may become cumulative and it is possible that the rating of transistor is exceeded.

If it happens, the device gets burn out. This process is known as thermal runaway of the transistor.

And a thermal runaway is avoided by using heat sink with the transistor.

A heat sink is metallic heat conductive device placed in close contact with a transistor to increase the power dissipation capability of the transistor.

Heat sink increase the surface area from which the heat is removed from the sink to the atmosphere by convection and radiation

b) Name different types of oscillator. Draw and explain working of Hartley oscillator.

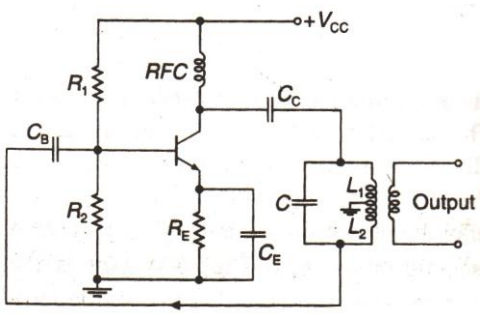
Ans: [*Note: Any four = 2 marks]*

Types of oscillators: **2M**

1. Hartley oscillator

2. Colpitts oscillator
3. Clapp oscillator
4. RC phase shift oscillator
5. Wein bridge oscillator
6. Crystal oscillator

Circuit diagram: **3M**



Explaination: **3M**

The above fig. shows hartley oscillator, it consists of two coils L_1, L_2 and C.

A coil called radio frequency choke (RFC) is connected between collector and Vcc supply it acts as a load for the collector and also permits easy flow of DC current but blocks AC current.

The resistance R1, R2 and R_E are used to provide DC bias to the transistor.

The coil L_1 is inductively coupled to coil L_2 and the combination work as auto transformer. The feedback between the output and input circuit is given through auto transformer which produces the phase shift of 180^0. Since the transducer also introduces phase shift of 180^0 therefore the total phase shift is 360^0 and hence the feedback is positive. The feedback fraction is given by $\beta = L_2/L1$. For oscillations to start, the voltage gain must be greater than $1/\beta$. When the circuit is energized the switching on the supply the collector current flows. The oscillations are produced because of positive feedback from the tank circuit.

The frequency of oscillation is given by,

$f_0 = 1/2\pi\sqrt{LC}$.

Where, L = L1 + L2 + 2M

= L1 + L2 ---------- if M- mutual inductance is neglected

c) What is clamper circuit? Draw positive and negative clamper with waveform. State its application.

Ans: ***[Note: definition 1 mark, application 1 mark and 6 marks for positive and negative clamper with waveform]***

Clamper circuit:

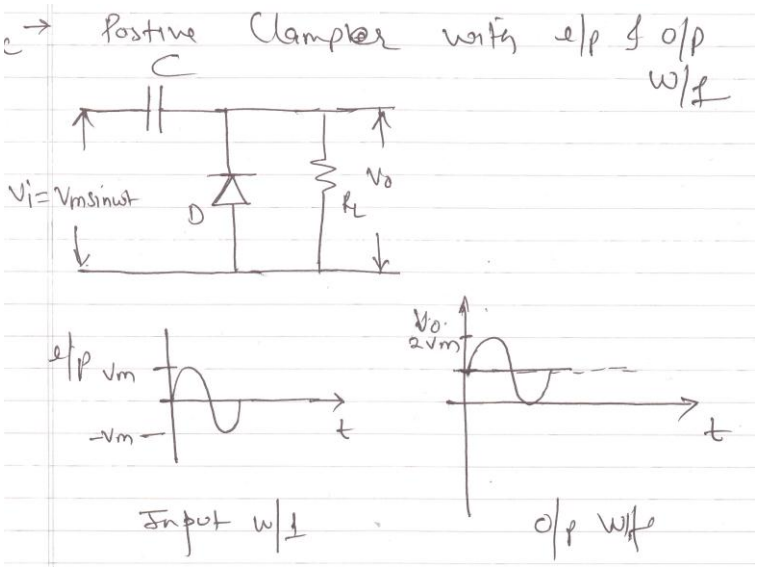
The circuit, with which the waveform can be shifted in such a way that a particular part of it (positive or negative) is maintained at a specified voltage level is called as clamper circuit.

A clamping circuit introduces (or restores) a DC level to an AC signal.

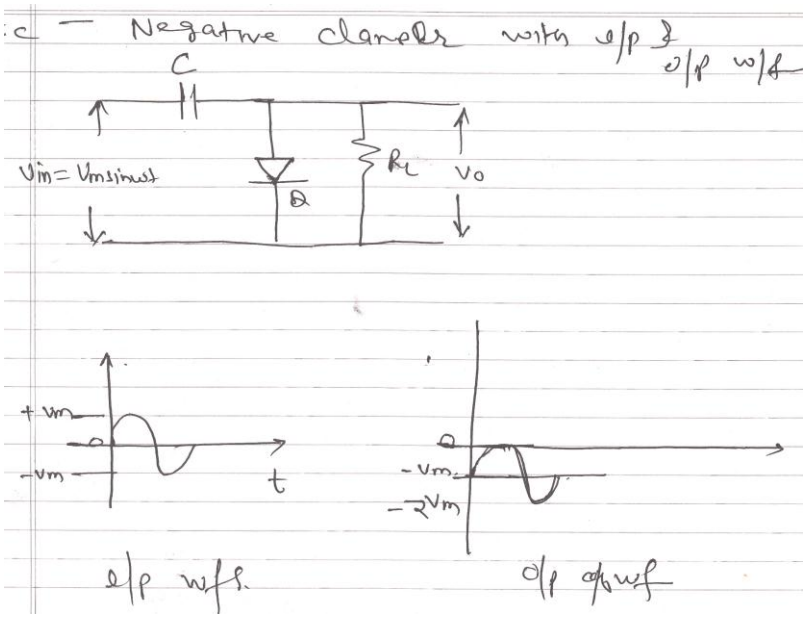
Applications:

- Used in TV receivers.
- Used in voltage multipliers.

Positive clamper with input and output waveform:



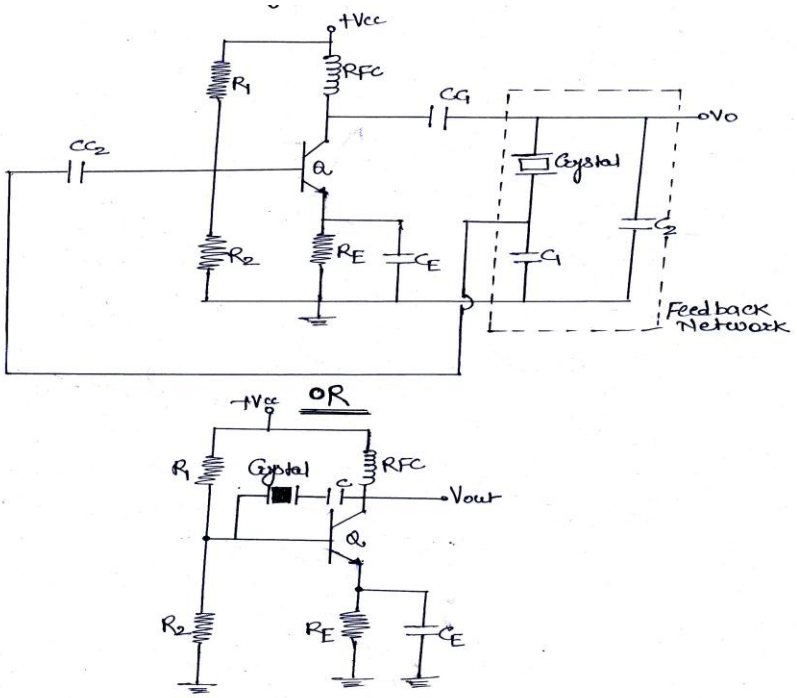
Negative clamper with input and output waveform:



Q6. Attempt any four of the following: **16M**

a) Draw neat circuit of crystal oscillator. State its two advantages.

Ans: Circuit diagram of crystal oscillator: **2 M**

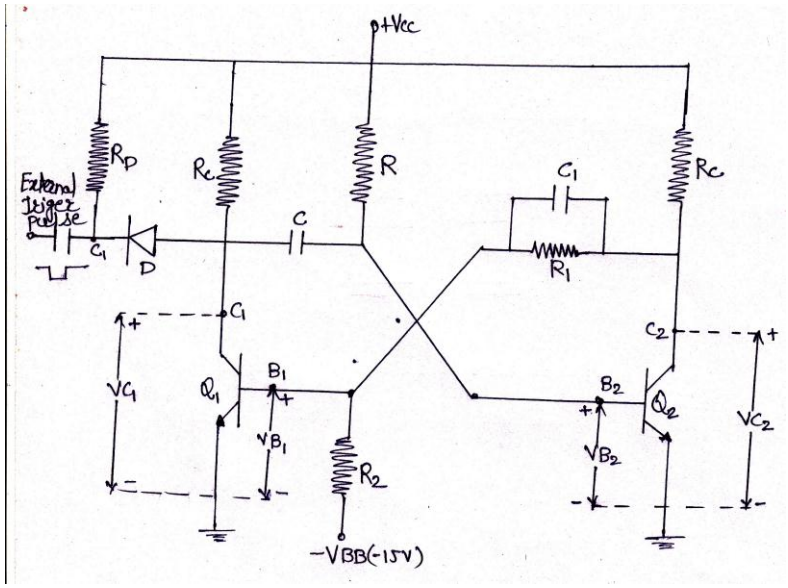


Following are some of the advantages of crystal oscillator: (any two) **2 M**

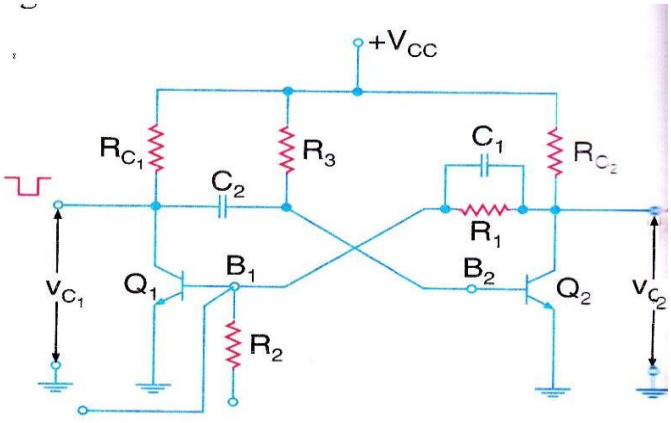
1. High frequency stability.
2. Q is very high.
3. Very low frequency drift due to change in temperature and other parameters.
4. It is possible to obtain very high, precise and stable frequency of oscillations.
5. It is possible to obtain frequencies, higher than the fundamental frequency by operating the crystal.

b) Draw neat circuit diagram of monostable multivibrator. **4M**

Ans:



OR



c) Describe operation of transistor as a switch. **4 M**

Ans: This switch operates between two states namely saturation region and cut-off region.

1) Transistor in the saturation region: (closed switch)

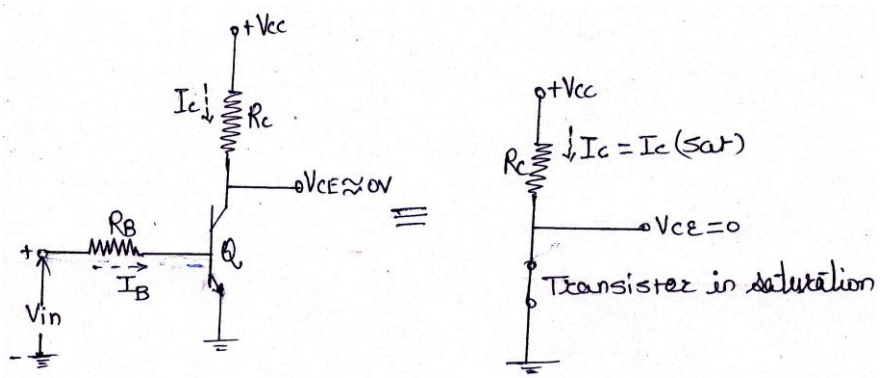


Fig ⓐ Transistor in saturation region

- In the saturation region both the junctions of transistor i.e. Emitter-Base junction and collector-Base junction are forward bias.
- The voltage drop across the transistor (V_{CE}) is very small of the order of 0.2V to 1V and Ic is very large.
- When Vin is positive, large Ib flows and transistor saturates.
- In saturation region transistor acts as a closed switch as shown in fig a.

2) Transistor in cut-off region : (open switch)

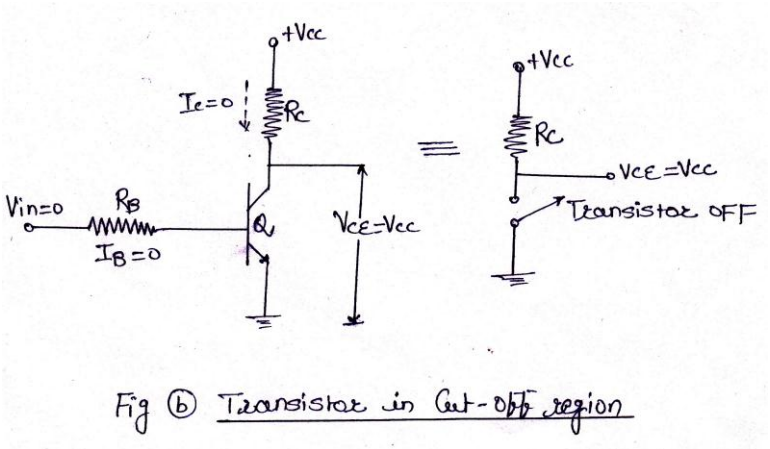


Fig ⓑ Transistor in Cut-off region

- In the cut-off region both the junction i.e. Emitter-Base and collector –Base of transistor are reverse bias and a very small reverse current flows through the transistor.
- The voltage drop across the transistor (V_{CE}) is high.

- Thus in the cut-off region the transistor acts as a open switch as shown in fig b.
- When Vin = 0, the $I_B = 0$, hence Ic = 0 and the transistor operates in the cut-off region.
- The output is given by,

$$V_{CE} = Vcc - Ic\ Rc$$

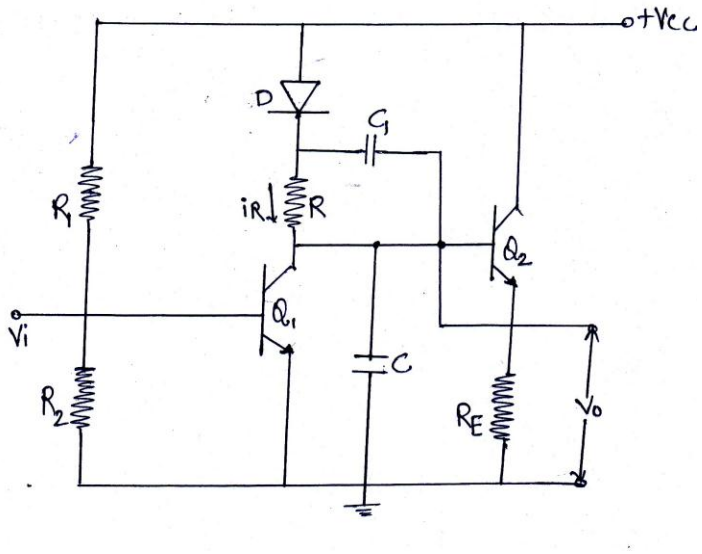
$$\therefore\ Ic\ Rc = 0$$

$$= Vcc - 0$$

$$V_{CE} = Vcc$$

d) Draw neat circuit diagram of Bootstrap sweep generator. **4 M**

Ans: Circuit diagram of Bootstrap sweep generator:



e) Write expression for time period of UJT relaxation oscillator. Draw wave forms at different terminals.

Ans: The expression for time period of UJT relaxation oscillator is given by: **2M**

$$T = R.C.\ \log_e 1/(1-\eta)$$

OR

$$T = 2.3RC\ log_{10}\frac{1}{(1-\eta)}$$

The frequency of relaxation oscillator is given by,

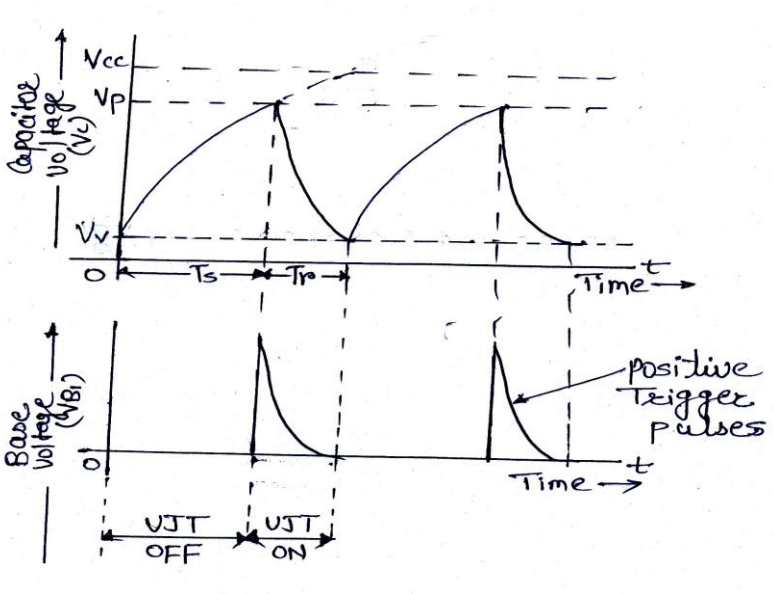
$$f = 1/T$$

$\therefore f = 1/ [R.C. \log_e [1/(1-\eta)]$

OR

$$f = \frac{1}{2.3\, RC \log_{10} \frac{1}{(1-\eta)}}$$

Wave forms of UJT relaxation oscillator at different terminals: **2 M**

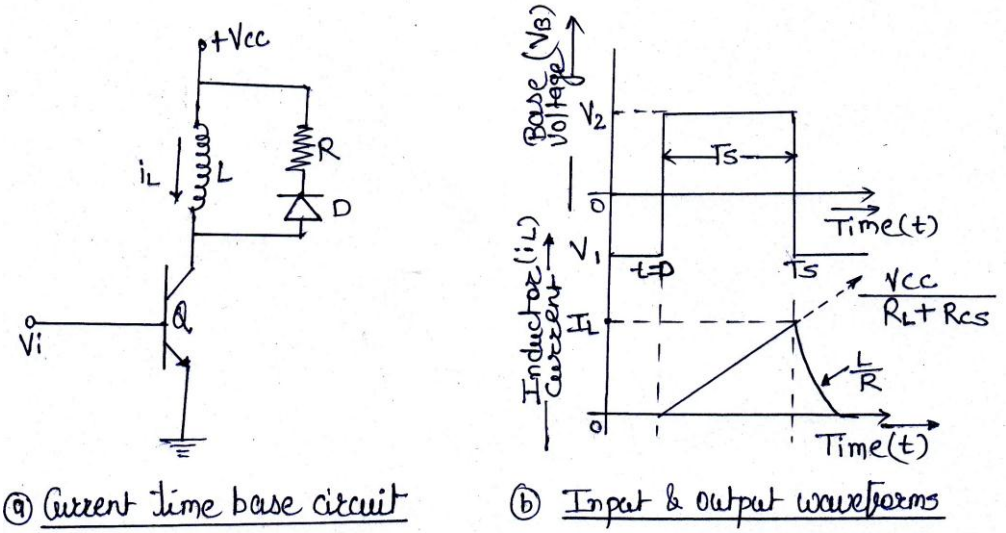


f) Why linearity correction is necessary in current time base generator? Describe any one method

Ans: Reason: **1M**

Due to non linearity tracing will be distorted or unexpected. Therefore linearity correction is necessary in current time base generator for proper tracing.

(1 marks for each diagram) **2 M**



(a) Current time base circuit (b) Input & output waveforms

Explanation **1 M**

When the transistor is ON the current through an inductor increases linearly with time. The diode D does not conduct during this sweep time. When transistor is OFF then inductor discharging through the freewheeling diode & the series resistor. 'R'. The nature of the current flowing through the transistor when it turn ON & turn OFF as shown in above fig.