MAHARASHTRA STATE BOARD OF TECHNICAL EDUCATION
(Autonomous)
(ISO/IEC - 27001 - 2005 Certified)

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SUMMER – 14 EXAMINATION

Model Answer

Subject Code: **12188**

Important Instructions to examiners:

1) The answers should be examined by key words and not as word-to-word as given in the model answer scheme.

2) The model answer and the answer written by candidate may vary but the examiner may try to assess the understanding level of the candidate.

3) The language errors such as grammatical, spelling errors should not be given more Importance (Not applicable for subject English and Communication Skills).

4) While assessing figures, examiner may give credit for principal components indicated in the figure. The figures drawn by candidate and model answer may vary. The examiner may give credit for any equivalent figure drawn.

5) Credits may be given step wise for numerical problems. In some cases, the assumed constant values may vary and there may be some difference in the candidate's answers and model answer.

6) In case of some questions credit may be given by judgement on part of examiner of relevant answer based on candidate's understanding.

7) For programming language papers, credit may be given to any other program based on equivalent concept.

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Q-1 (a) Attempt ANY THREE of the following.   (12 Marks)

i.   State advantages and disadvantages of digital communication system.

Ans. **Advantages of digital communication   (Any 2 points -2 marks)**
- Noise Immunity is good.

- Digital signals are better suited than analog signals for procession and combining using technique called multiplexing.

- Digital transmission systems are more resistant to analog systems to additive noise because they use signal regeneration rather than signal amplification.

- Digital signals are simpler to measure and evaluate than analog signals.

- In digital systems transmission errors can be corrected and detected more accurately.

- Using data encryption only permuted receivers can be allowed to detect the transmission data.

- Wide dynamic range.

- Because of the advances of IC technologies and high speed computers, digital communication systems are simpler and cheaper.

- Digital communication is adaptive to other advance branches of data processing such as digital.

Disadvantages of Digital Communication   (Any 2 points- 2 marks)
- The transmission of digitally encoded analog signals requires significantly more bandwidth.

- Digital transmission requires precise time synchronization between the clocks in the transmitter and receiver.

- Digital transmission systems are incompatible with older analog transmission systems.

ii.   State sampling theorem. What are the types of sampling?

Ans: **(Statement-2 Marks, Types - 2Marks)**

Sampling theorem states that, the sampling frequency (Fs) i.e. number of sample per second should be greater than or equal to twice the maximum frequency component (Fm) of the input signal, in order to recover the signal without any distortion at the receiver.

$$Fs \geq 2fm$$

(OR)

Sampling theorem states that a band limited signal of finite energy having the highest frequency component f_m Hz can be represented and removed completely from a set of samples taken at a rate of Fs sampling per seconds provides that $Fs \geq 2Fm$

Types of sampling: (2 Marks)
1. Ideal
2. Practical   a) Natural sampling
                   b) Flat top sampling.

iii. Draw waveforms for 10101100 in ASK and FSK modulation.

Ans: **(ASK-2Marks,   FSK-2 Marks)**
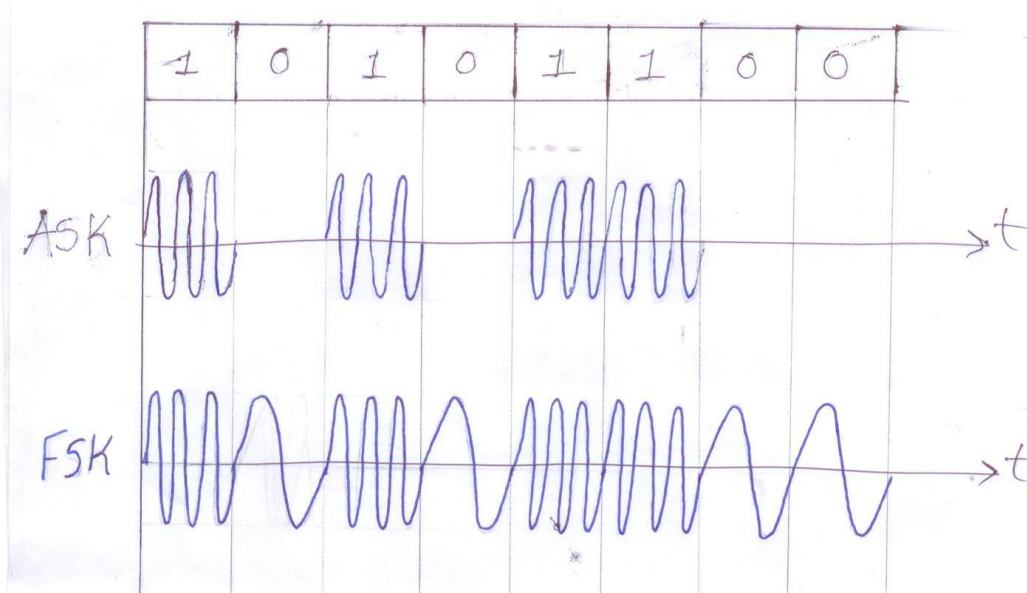
iv.   Compare pulse modulation with continuous wave modulation.

Ans: **(Any four points-4Marks)**

Sr. No	Pulse modulation	Continuous wave modulation
1	The carrier is train of pulses.	The carrier is sine wave
2	The modulation can be done by varying width, position and amplitude of pulse.	The modulation can be done by varying the amplitude, phase and frequency of the sine wave.
3	More bandwidth required	Less bandwidth required.
4	Applications in Satellite communication, communication between spaceships and earth stations.	Applications in broadcasting radio and TV.
5	The noise immunity for PAM is least but rest all modulation techniques work well.	The noise immunity is low for AM. While PM and FM work well.
6	Digital modulation is possible.	Digital Modulation is not possible.
7	Simpler and less costly.	Costly and complicated.

Q-1 (b)   Attempt ANY ONE of the following.   (06 Marks)

i. Describe the noise present in Delta modulation with waveforms. How to reduce them?

Ans: **(Description-2Marks, Waveforms-2Marks, Remedy-2Marks)**

Noises present in delta modulation are,
- Slope overload and
- Granular noise

- **Slope-overhead distortion**:
If the slope of the signal x(t) is much higher than that of the approximate signal x'(t) over will not follow x(t) at all as shown in figure. The difference between x(t) and x'(t) is called the slope-overload distortion or the slope overload error. Thus, slope-overload error occurs when the slope

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of x(t) is much higher than x'(t). The slope overload error can be reduced by increasing the step size δ or by increasing the sampling frequency. However with the bit rate and bandwidth requirement will increase.
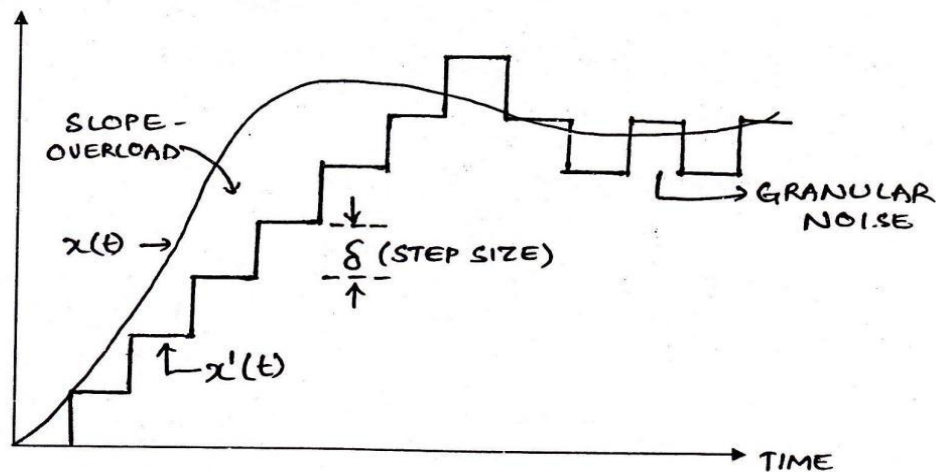
Waveform showing Slope-Overload error and Granular noise in DM

- **Granular noise:**

When the input signal x(t) is relatively constant in amplitude, the approximated signal x'(t) will hunt above and below x(t) . This leads to a noise called granular noise. It increases with in step size δ. To reduce granular slope-overload distortion.

Remedy: If the step size δ is variable then slope overload distortion and granular noise both can be controlled. This is in Adaptive Delta Modulation.

**ii. Describe the working of DSSS transmitter & receiver with the help of block diagram. Draw the waveforms.**

Ans: **(Description-2Marks, Waveforms-2Marks, Diagram of Tx & Rx-2Marks)**

Direct Sequence Spread Spectrum Coherent PSK Transmitter

The averaging system reduces the interference by averaging at over a long period the DSSS system is a averaging system. This technique can be used in practice for transmission of signal over a band pass channel (E.g. satellite channel). For such application the coherent binary phase shift (BPSK) is used in the transmitter and receiver.


Direct sequence spread spectrum coherent PSK transmitter
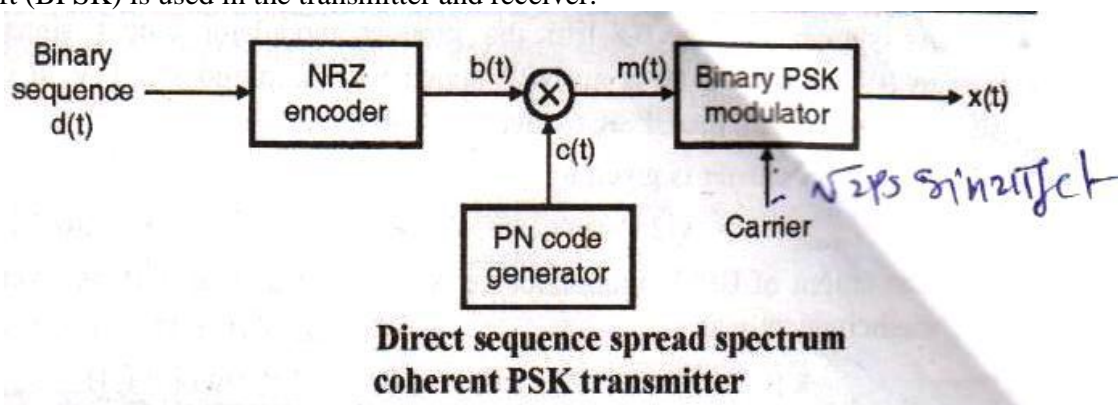
(OR)

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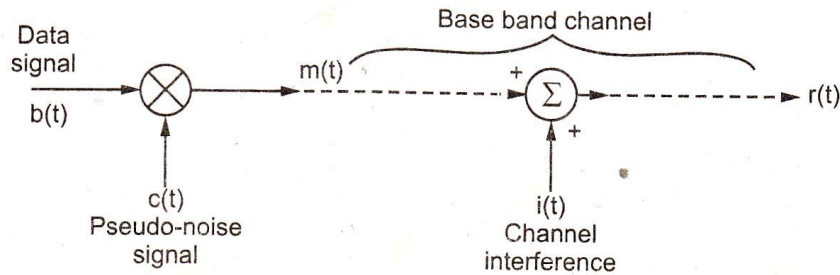
**Direct sequence spread spectrum system transmitter (baseband transmission) or encoder**

The binary sequence d(t) is given to the NRZ encoder. The d(t) is converted NRZ signal b(t).The NRZ signal b(t) is used to modulate the PN sequence C(t) generated by the PN code generator. The multiplier multiply the signal b(t) * c(t) = m(t). The m(t) signal is given to binary PSK modulator. The modulated signal at the output of product modulator or multiplier i.e. m(t) is used modulate the carrier for BPSK modulation. The transmitted signal X(t) is thus direct sequence SSBPSK .

DSSS Receiver Block Diagram
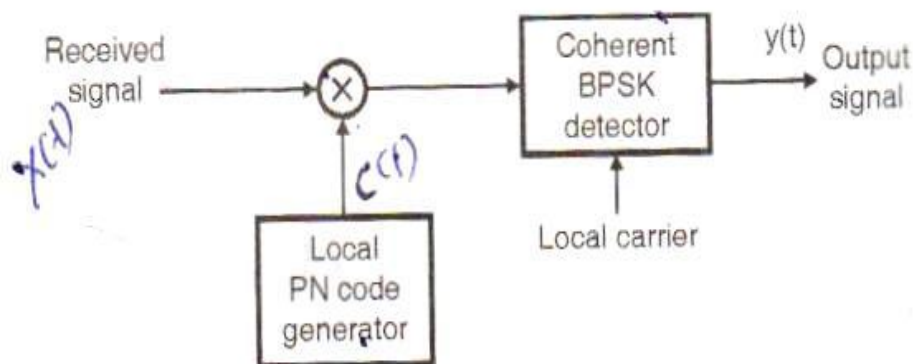
The DS-BPSK receiver

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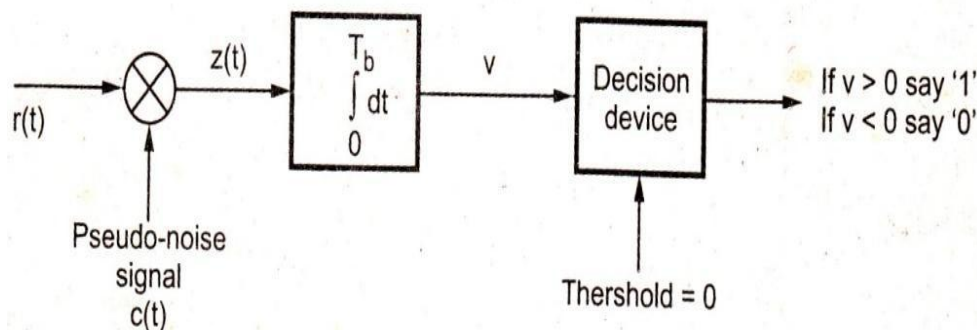
The receiver signal X(t) and the locally generated replica of the PN sequence generator are applied to a multiplier this is 1ST stage of multiplication. The multiplier performs the de-spreading operation output of multiplier is then applied to a coherent BPSK detector with local carrier applied to it.

At the output of coherent BPSK detector we get back the original signal d(t) data signal.

Waveform :-

Waveforms of DS-BPSK transmitter
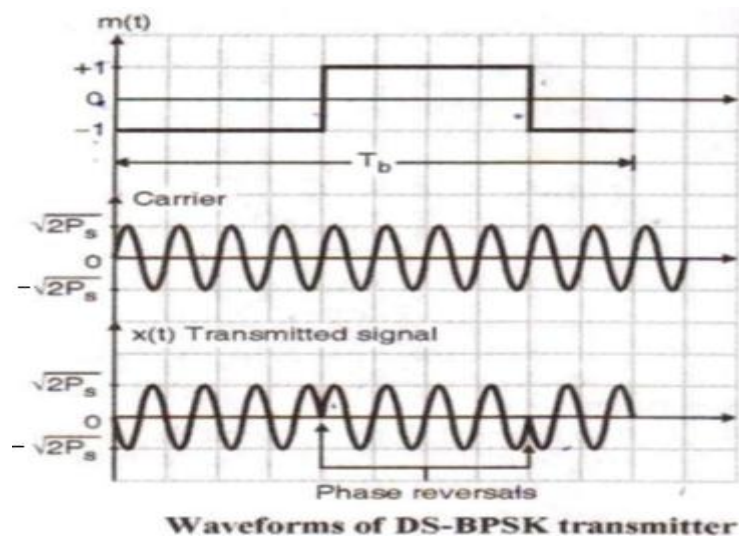
Q-2 Attempt ANY FOUR of the following.   **(16 Marks)**

 a) Define:

          i) Bit rate   **ii) Baud rate**

Also give baud rate of Manchester and RZ line codes.
Ans:-
Bit rate   **(1 Mark)**
It is the number of bits transmitted or sent in one second .Its unit is bits per second. If bit duration is "Tb" then bit rate will be 1/Tb
Baud rate   **(1 Mark)**
Baud is the unit of signaling speed or modulation rate or the rate of symbol transmission. It indicates the rate at which a signal level changes over a given period of time.
Baud rate of Manchester- 2 times Bit Rate
Baud rate of RZ line codes - 2

 b) Draw block diagram of M-ary FSK transmitter and receiver and explain its working.
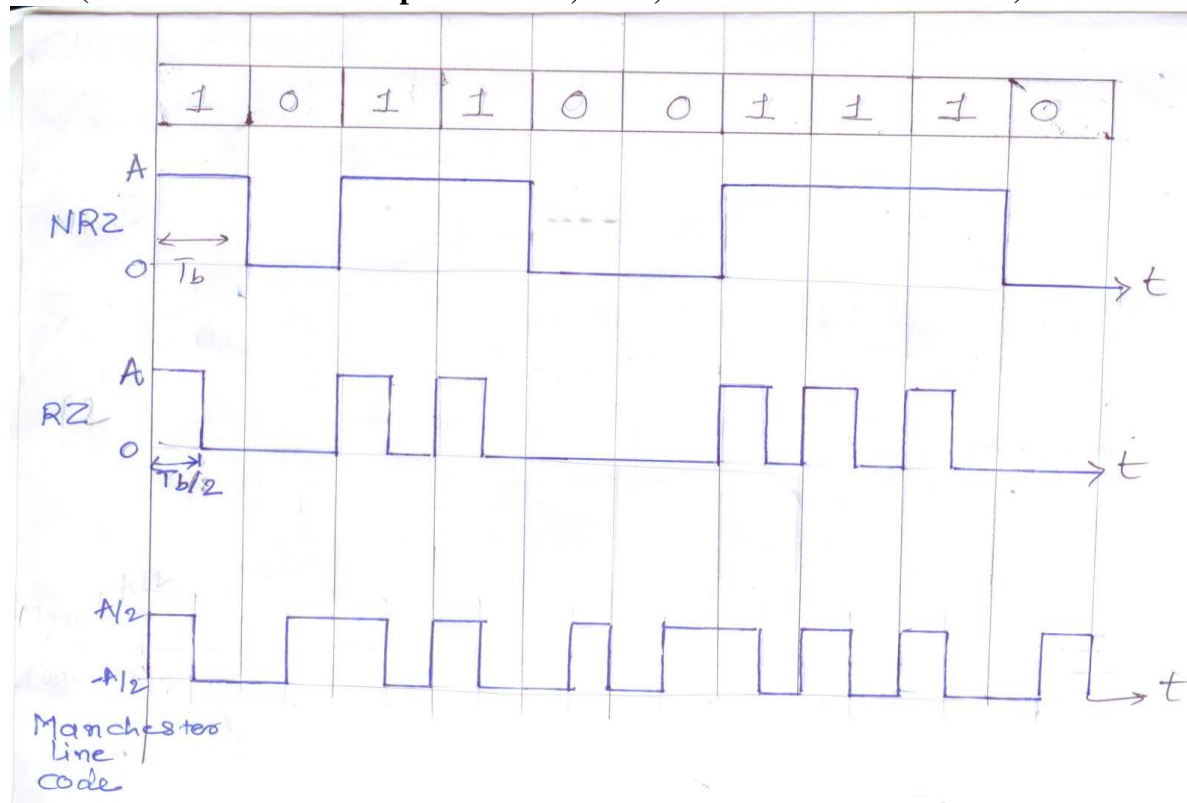Ans:- (**Explanation-2 marks, Block diagram-2 marks each**)
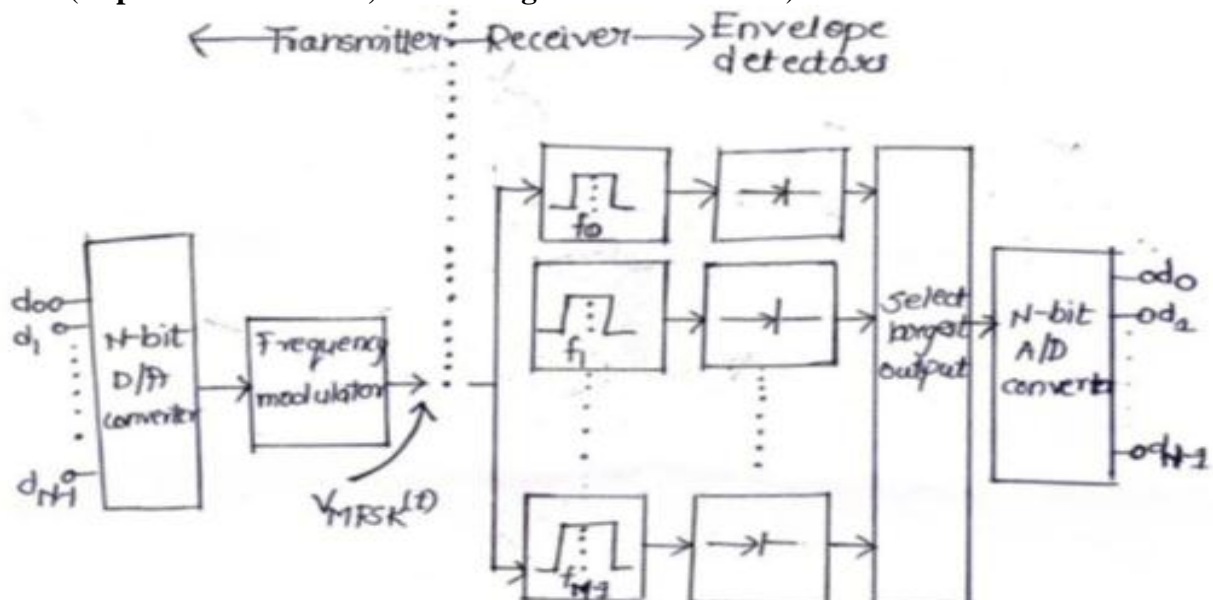
Block diagram of M-ary FSK transmitter and receiver

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M-ary FSK transmitter and receiver Explanation

- An M-ary FSK system is the logical extension of a binary FSK system. In an M-ary FSK system the symbols are not one bit long like BFSK but each symbol is N bit long with a symbol duration of $T_s= NT_b$, the block diagram of an N bit M-ary FSK system is as shown in figure.

- At the transmitter an N bit symbol is presented after a period of T_s to an N bit D/A converter. The output of D/A converter is applied to the frequency modulator. The frequency modulator generates a carrier waveform whose frequency is determined by the analog modulating signal at the output of D/A converter.

- The transmitted signal, for the duration of the symbol interval has the frequency $f_0, f_1 \ldots \ldots f_{M-1}$ where $M=2^N$. for example , if N=2 then M=4. Then there will be four different frequencies corresponding to the four different possible messages i.e. 00,01,10 and 11.

- The M-ary FSK signal is demodulated using Envelope detector as shown in figure. At the receiver the incoming signal is applied to M paralleled band pass filter each followed by an envelope detector.

- This band pass filter has center frequency $f_0, f_1 \ldots \ldots f_{M-1}$. Therefore this filter will pass only the signals of their center frequencies. Remember that at any given instant of time only one frequency is being received.

- The output of band pass filter is then applied to envelope detectors. They produce DC voltage proportional to their AC input voltage. Output of the entire envelope detectors are applied to a device which determines which of the detector is the largest of all at the given time. The output of the device is applied to an N bit A/D converter which reproduces the originally transmitted N bit message.
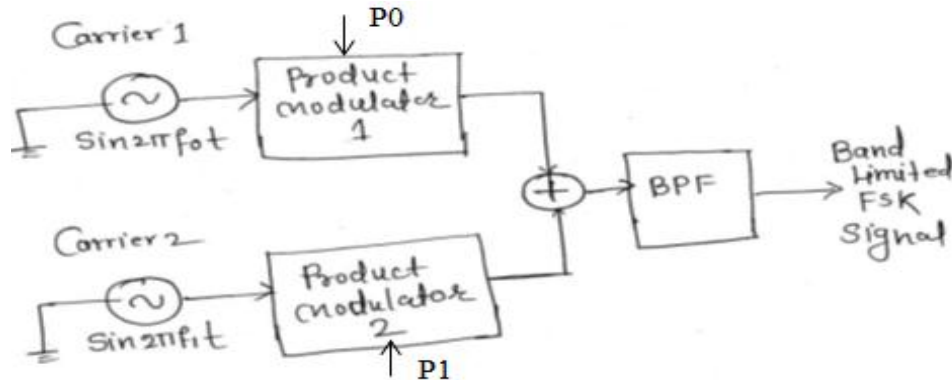
c) **Draw NRZ, RZ and Manchester line code waveforms for given data 1011001110.**

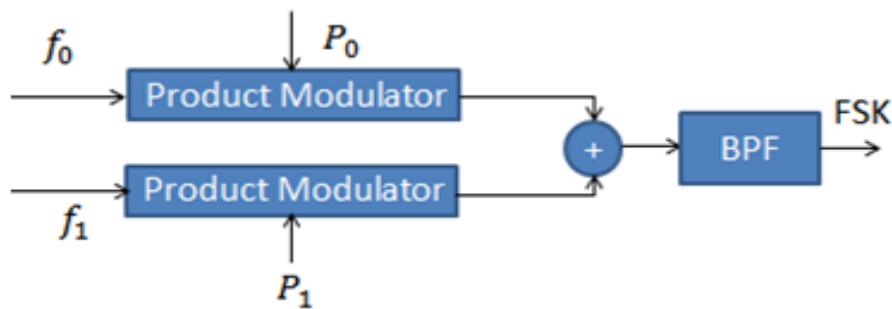Ans: **(1 Marks each for data presentation, NRZ,RZ and Manchester code.)**

d) **Draw block diagram of FSK modulator. Explain its working with the help of waveforms.**

Ans: **(Diagram-1Mark, Explanation-2Marks, Waveform-1Mark)**

(OR)

**FSK modulator**

Explanation

In frequency shift keying (FSK) the frequency of sinusoidal carrier is shifted two discrete values.

One of these frequency f_1 represents a binary 1 and other values f_0 represents a binary 0. In FSK there is no change on amplitude of the carrier.

It consist of two oscillator which produces sin ware at frequency f_1 and f_0 the oscillator output are applied to the input of two products modulators.

When a binary 0 is transmitted $P_0 = 1$ and When a binary 1 is transmitted $P_1 = 0$. Bandwidth of FSK is $4f_b$.

Waveform

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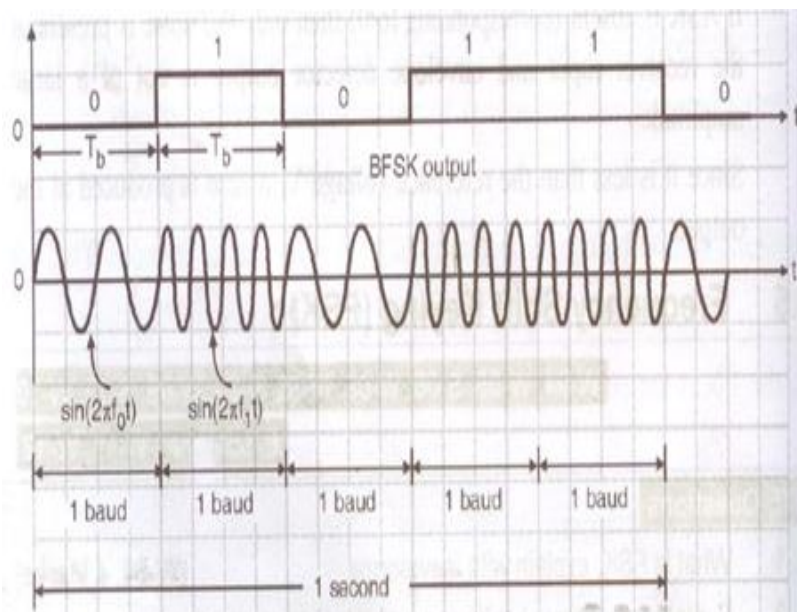
e) Explain DPCM with the help of block diagram.

Ans: **(Diagram- 2Mark   Explanation-2Marks)**

The block diagram of DPCM transmitter and receiver is as shown in figure. Unlike PCM in DPCM scheme, digital equivalent of each quantize sample is not transmitted by the transmitter. Instead the digital equivalent of the difference between the present sample value and the previous sample value is transmitted.

Differential Pulse Code Modulation transmitter:

DPCM transmitter
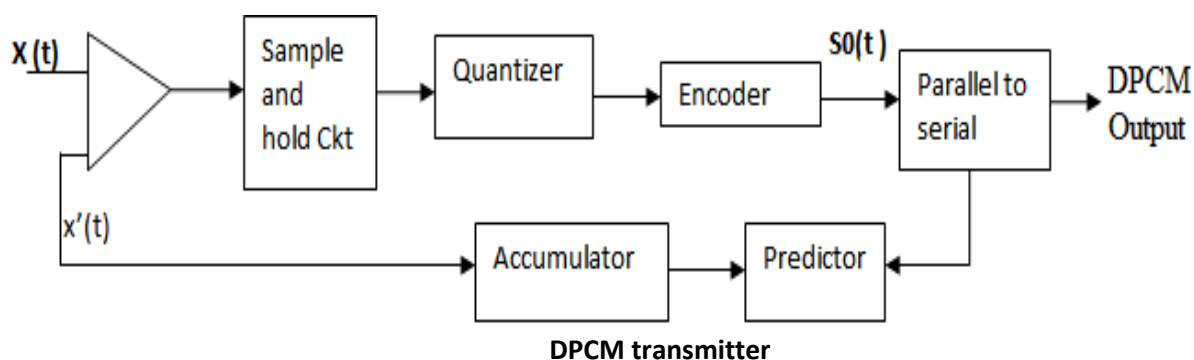
As shown in fig, x (t) is the analog input signal and x'(t) is the appoximated signal. At each sampling instant the difference amplifier compares x(t) and x'(t) and the sample and hold ckt will hold the result of this subtraction.

The difference signal at the output of sample and hold ckt is quantize by the quantizer. The quantizer output S0(t) is then transmitted as it is encoded in a stream of bits. The quantizer output is also used to produce the approximated signal x'(t) by passing the quantizer output throught the predictor and accumulator.

f) Compare TDM with FDM. (four points)

Ans:- **(Any four points - 1 Mark each)**

Sr. No	TDM	FDM
1	TDM divides and allocates certain time periods to each channel.	FDM divides the channel into the two or more frequency ranges that do not overlapped
2	TDM is preferred for digital signals	FDM is usually preferred for the analog signal
3	In TDM, each signal uses all of bandwidth for some time	In FDM, each signal uses the small portion of the bandwidth all of the time
4	TDM circuit is not complex	FDM requires the complex circuitry.
5	In TDM the problem of crosstalk is not sever.	FDM suffers from the problem of crosstalk due to imperfect band pass filter
6	Due to fading only a few TDM channel will be affected	Due to wide band fading in the transmission medium, all the FDM channel will be affected
7	Synchronization is required.	Synchronization is not required.
8	Due to slow narrow band fading all the TDM channel may gets wiped out.	Due to slow narrow band fading taking place in the transmission channel only a single channel may be affected in FDM.

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3) Attempt ANY FOUR of the following **(16 Marks)**

a) State Shannon-Hartley theorem on Channel Capacity. State the significance of each term in it.

Ans: (Theorem-2 Marks, Significance-2 Marks)

The relationship between the capacity, bandwidth and noise of a channel is termed as Shannon – Hartley's Theorem.

It states that, For a White Gaussian Channel the channel capacity can be expressed as

$$C = B \log_2\left(1 + \frac{S}{N}\right) \text{ bits/second}$$

Where C = channel capacity

B = channel bandwidth
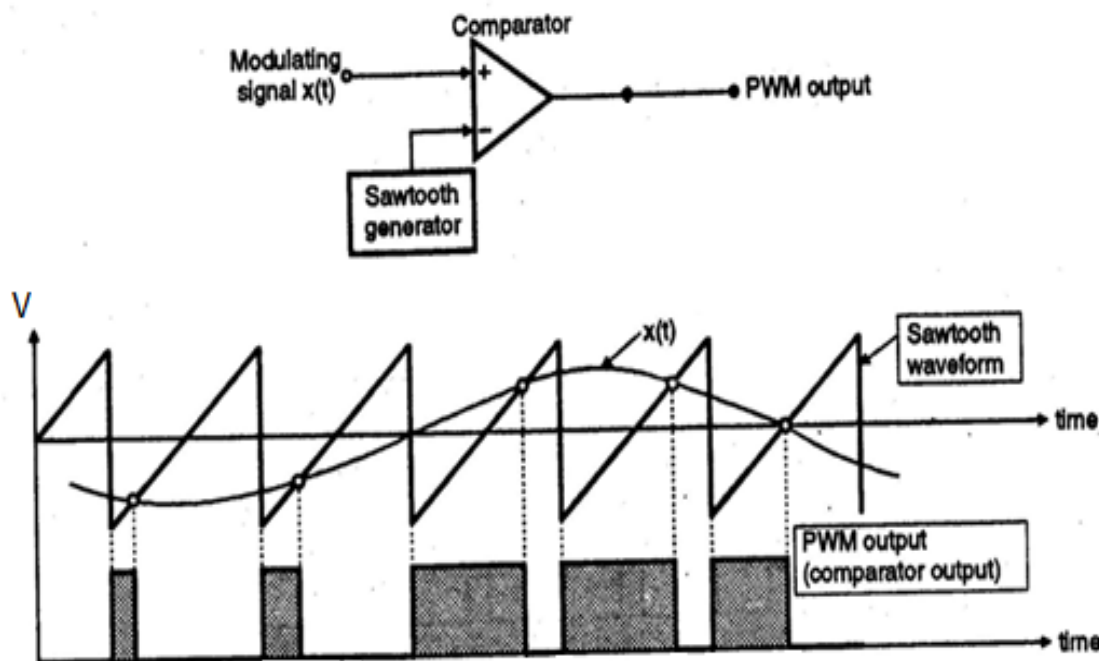
S = signal power

N = Noise within the channel Bandwidth

$\frac{S}{N}$ = Signal to Noise Ratio

b) Describe the Generation of PWM signal with the help of block diagram and waveforms?

Ans :

Diagram **(2 Marks)**

block diagram and waveform of PWM Generation

Explanation **(2 Marks)**

- A saw tooth generates a saw tooth signal frequency fs, therefore the saw tooth signal in this case is a sampling signal. It is applied to the inverting terminal of the same comparator.
- The modulating signal x(t) is applied to the non-inverting terminal of the same comparator.

- The comparator output will remain high as long as the instantaneous amplitude of x(t) is higher than that of the ramp signal.
- This gives rise to a PWM signal at the comparator output as shown in waveform above.
- The leading edges of PWM signal are always generated at fixed time instants. However the occurrence of its trailing edges will be dependent on the instantaneous amplitude of x (t).
- In other words, the leading edge of the PWM signal coincides with the trailing edge of the Sawtooth sampling signal while the trailing edge of PWM signal depends on the amplitude of the modulating signal.
- Therefore this PWM signal is said to be trail edge modulated PWM.

c) Draw the block diagram of DPSK Transmitter and explain.

Ans :

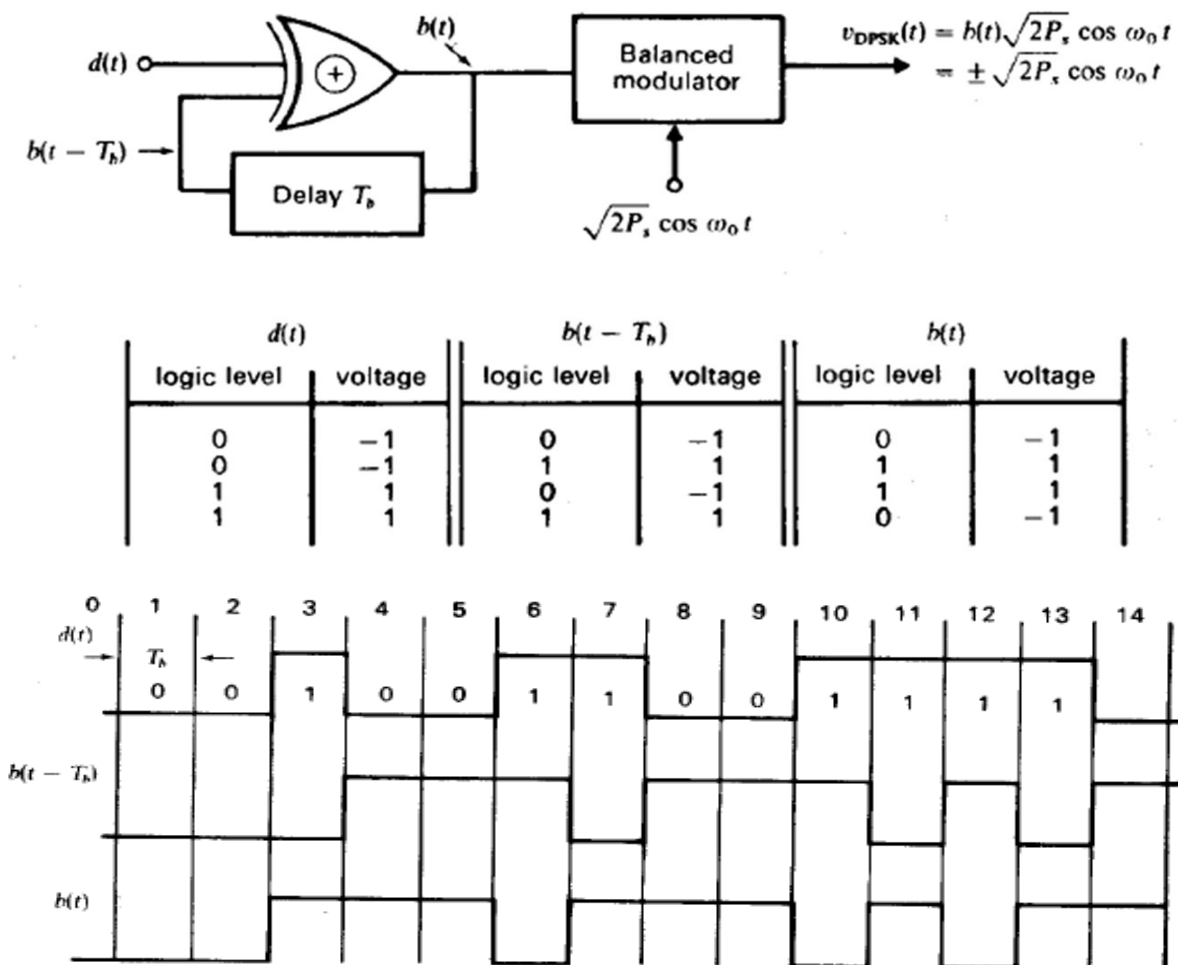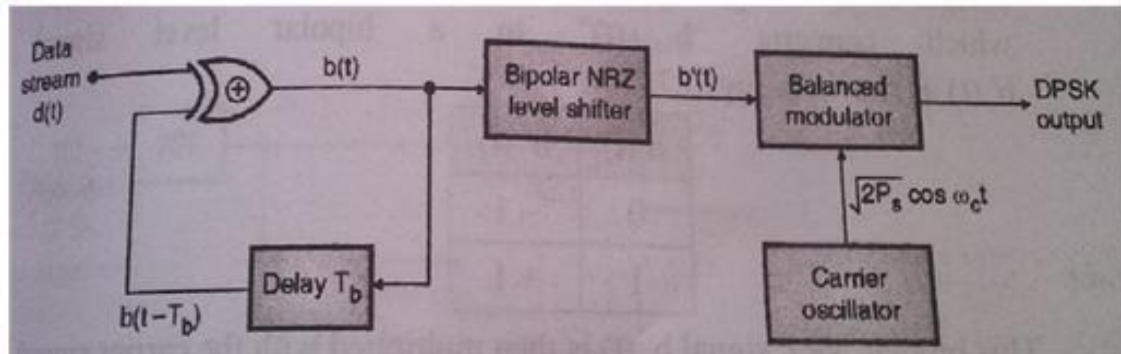<u>Diagram</u>   **(2 Marks)**

Figure 6.3-2 Logic waveforms to illustrate the response $b(t)$ to an input $d(t)$.

Block diagram and waveform of DPSK Transmitter

(OR)

Diagram   **(2 Marks)**

block diagram of DPSK Transmitter

Explanation   **(2 Marks)**

- d (t) represents the data stream which is to be transmitted it is to one input of an EX-OR logic gate.
- The EX-OR gate output "b (t)" is delayed by one bit period the applied to the other input of EX-OR gate. The delayed represented by "b (t-Tb)".
- Depending on the values of "d (t)" and "b (t-Tb)" the EX-OR produces the output sequence "b(t)".the waveform for the generator .the waveform drawn by arbitrarily assuming that in the first interval b (0)=0.
- Output of EX-OR gate is the applied to a bipolar NRZ level which converts "b(t)" to a bipolar level "b(t)as shown
- This bipolar NRZ signal b"(t) is then multiplied with the current to produce the DPSK signal. The DPSK output spilt mathematically expressed as:
- So when b (t) =1, b"(t) =1,

  Hence, $V_{DPSK}(t)=\sqrt{2P_s}\ cos\omega t$. That Means no phase Shift has been introduced.
- But when b(t) = 0,b" (t) = -1

  Hence, $V_{DPSK}(t)= - \sqrt{2P_s}\ cos\omega t$

  Thus 180 Phase shift is introduced to represent b (t) =0

d) Draw the block diagram of PN Sequence Generator using 4 'D' flip-flops.
Ans:
Diagram   **(4 Marks)**
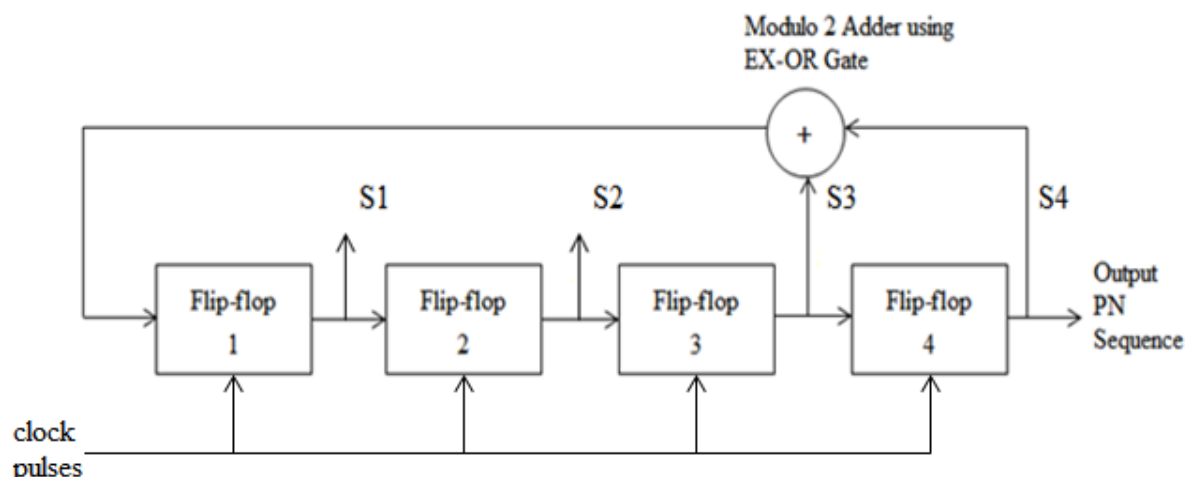
block diagram of PN Sequence Generator

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e) Compare DSSS with FHSS (Four points)

Ans: (Any Four points) **(4 Marks)**

Sr. No	Parameters	DSSS	FHSS
1	Definition	PN sequence of large bandwidth is multiplied with the narrow band data signal.	Data bits are transmitted in different frequency slots which are changed by PN sequence.
2	Chip Rate	It is fixed $R_c = \frac{1}{T_c}$	$R_c = \max(R_h, R_s)$
3	Modulation Technique	BPSK	M-ary FSK
4	Processing Gain	$PG = \frac{T_b}{T_c} = N$	$PG = 2^t$
5	Acquisition Time	Long	Short
6	Effect of Distance	This system is distance relative.	Effect of distance is less.

**4. a) Attempt ANY THREE of the following** **(12 Marks)**

i) Explain 'Companding' in PCM with help of suitable diagram.
Ans : (Diagram – 1 Mark, Explanation – 3 Marks)
- Companding is non-uniform quantization. It is required to be implemented to improve the signal to quantization noise ratio of weak signals.
- The quantization noise is given by,

$$N_q = \frac{s^2}{12}$$

- This shows that in the uniform quantization once the step size is fixed, the quantization noise power remains constant.
- But the signal power is not constant. It is proportional to the square of signal amplitude. Hence the signal power will be small for weak signals, but quantization noise power is constant.
- Therefore, the signal to quantization noise ratio for the weak signals is very poor. This will affect the quality of signal. The remedy is to use Companding.
- Companding is a term derived from two words, compression and expansion. Compression = Compression + Expanding
- The process of Companding is shown in the bock diagram below
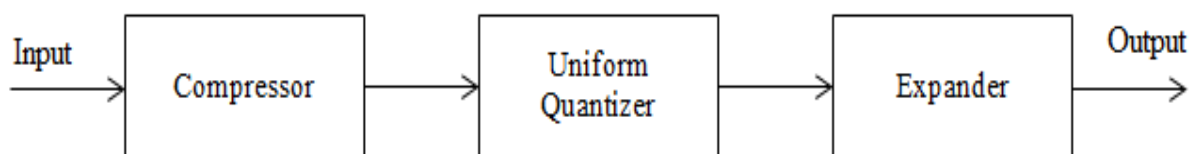
Block diagram of Companding
- Practically it is difficult to implement the non-uniform quantization because it is not known in advance about the changes in the signal level.
- Therefore, the weak signals are amplified and strong signals are attenuated before applying them to a uniform quantizer.

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- This process is called 'Compression' and the block that provides it is called as 'Compressor'.
- At the receiver exactly opposite process is followed which is 'Expansion'. The circuit used for providing expansion is called 'Expander'.
- In short, the compression of signal at the transmitter and expansion at the receiver is combined to be called as 'Companding'.
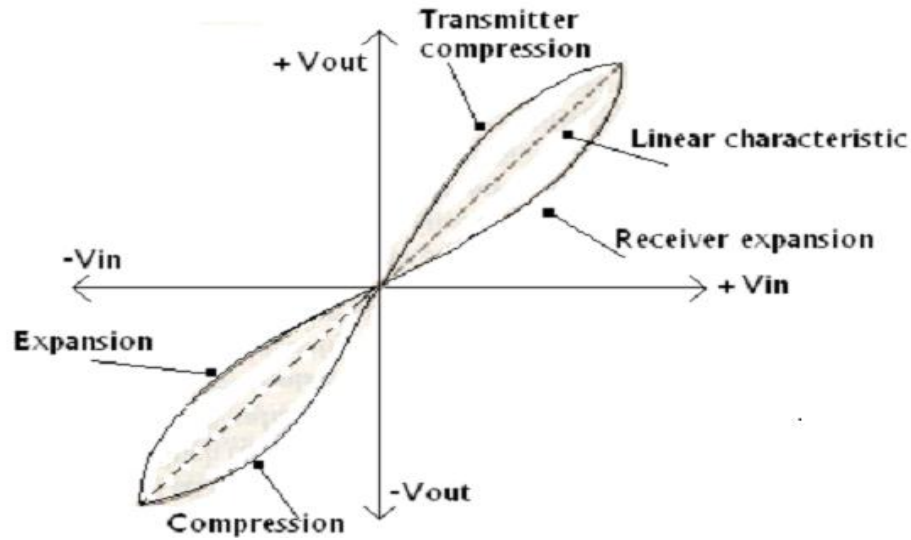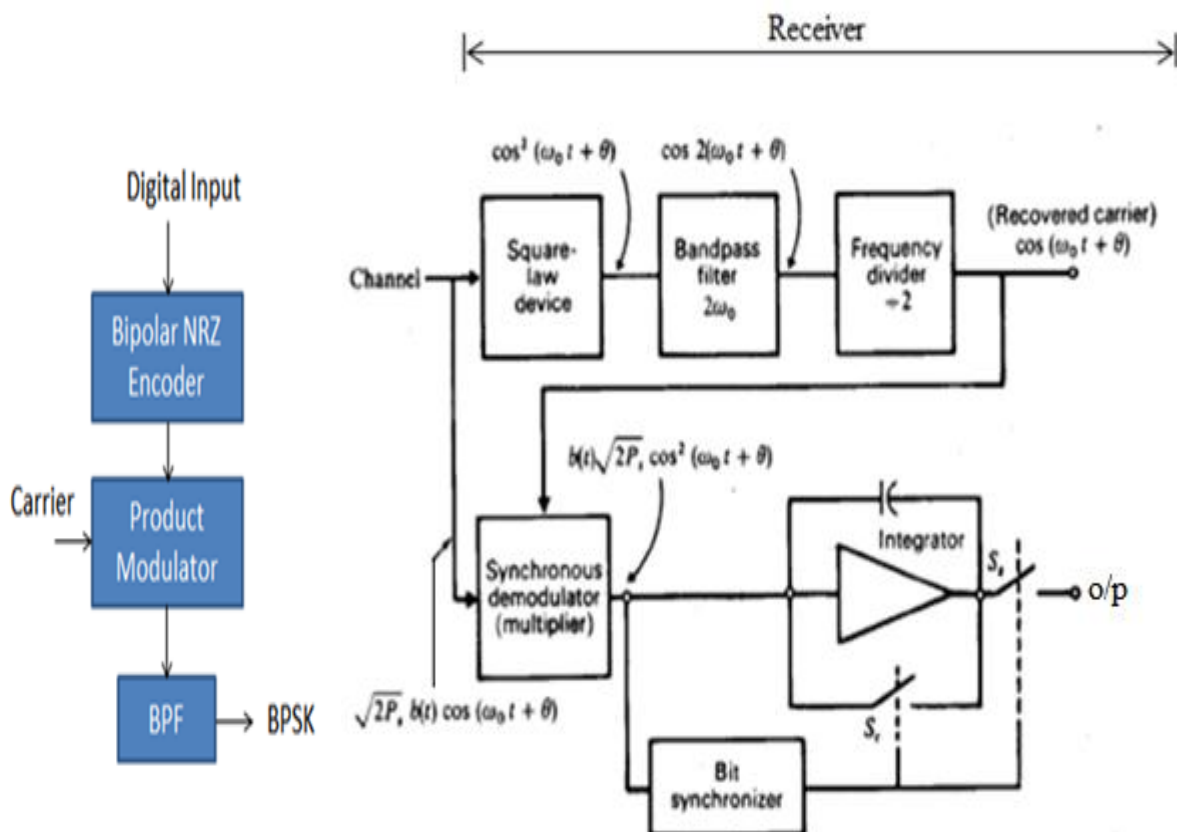

Companding Curve for PCM

ii) Draw the block diagram of BPSK transmitter and receiver. Explain its working.

Ans : Transmitter & Receiver Diagram   **(2 Mark)**

block diagram of BPSK Transmitter & Receiver

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BPSK Transmitter Explanation   **(1 Mark)**

- The digital information from the source may be a unipolar NRZ data which varies between values 1 and 0. But if digital data is unipolar then during 0 data output will be zero due to use of multipliers at transmitter. So to avoid this problem the unipolar data is first converted into bipolar data whose value varies between +1 and -1.
- The transmitter of BPSK signal is shown in the above figure.
- The digital signal from the information source is a unipolar NRZ signal which is first converted into bipolar signal. This signal acts as the modulating signal. The BPSK modulator is nothing but a multiplier followed by a band pass filter as shown in above figure.
- Due to multiplication, the BPSK output will be present with 0^0 phase shift when a binary '1' is to be transmitted and when the digital input is '0' then we get BPSK output with 180^0 phase shift as shown in the waveform above.
- From the waveform analysis we can conclude that when a binary '1' is to be sent the carrier is transmitted with 0^0 phase shift and when binary '0' is to be sent then the carrier is transmitted with 180^0 phase shift.
- The transmitted BPSK signal is s (t) = b (t) $\sqrt{2Ps}\cos\omega_0 t$.
- The phase of this signal changes depending on the time delay from transmitter to receiver. This phase change is generally fixed in the transmitted signal. Let the phase shift be Θ.
- Therefore the signal at the input of receiver is s (t) = b (t) $\sqrt{2Ps}\cos\omega_0 t + \Theta$.

BPSK Receiver Explanation   **(1 Mark)**

In the Receiver, we get noise mixed BPSK signal with a phase shift of Θ. This signal is given to both square law device and a synchronous demodulator.
- The square law device performs the squaring operation of the BPSK signal and raises its power two times.
- The output of square law device is given to the band pass filter which is designed with a cut off frequency $2\omega_0$.
- The band pass filter will filter out only the $2\omega_0$ frequency components of the BPSK signal and suppresses the other frequency components of the signal.
- The output of band pass filter is given to the frequency divider. This is used for bringing the frequency components of the signal from $2\omega_0$ to ω_0. So the output of frequency divider is nothing but the recovered carrier signal.
- The main purpose of using these square law device, band pass filter and the frequency divider is to recover the carrier signal in proper form so that it will be easy for the receiver to demodulate the original modulating signal from BPSK signal.
- The synchronous demodulator is nothing but a multiplier which multiplies both the recovered carrier signal and the BPSK signal received.
- The output of synchronous demodulator is given to bit synchronizer and the integrator.
- The integrator integrates the received signal and accordingly the capacitor in the circuit starts charging. One bit period T_b contains integral number of cycles of carrier. This means the phase change occurs in the carrier only at zero crossing.

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- The bit synchronizer takes care of starting and ending times of a bit.
- At the end of bit duration(T_b) , the bit synchronizer closes switches and the capacitor discharges through these switches and we get recovered original modulating signal at the output.

iii) **Find the entropy and data rate for signals having probabilities$\frac{1}{2}, \frac{1}{4}, \frac{1}{8}, \frac{1}{8}$.**

Note: given question is incomplete. So data rate cannot be found.

So the mark distribution is only for entropy.

Given: $p_1 = \frac{1}{2} = 0.5$, $p_2 = \frac{1}{4} = 0.25$, $p_3 = \frac{1}{8} = 0.125$, $p_4 = \frac{1}{8} = 0.125$

To find: 1. Entropy (H)

       2. Data Rate (R)

Formulae: **(2 Marks)**

> $H = \sum_{k=1}^{M} p_k \log_2 \frac{1}{p_k}$

Solution: **(2 Marks)**

> $H = \sum_{k=1}^{M} p_k \log_2 \frac{1}{p_k}$

$$= p_1 \log_2 \frac{1}{p_1} + p_2 \log_2 \frac{1}{p_2} + p_3 \log_2 \frac{1}{p_3} + p_4 \log_2 \frac{1}{p_4}$$

$$= 0.5 \log_2 \frac{1}{0.5} + 0.25 \log_2 \frac{1}{0.25} + 0.125 \log_2 \frac{1}{0.125} + 0.125 \log_2 \frac{1}{0.125}$$

$$= 0.5 + 0.5 + 0.375 + 0.375$$

$$= 1.75 \frac{\text{bits}}{\text{message}}.$$

iv) State the bandwidth required for BPSK, QPSK, FSK, and DPSK.

Ans. **(Four Points)**   **(4 Marks)**

Sr. No	Modulation Technique	Bandwidth Required
1	BPSK	BW = 2 f_b
2	QPSK	BW = f_b
3	FSK	BW = 4 f_b OR BW = $\lvert f_1 - f_0 \rvert + f_b$
4	DPSK	BW = f_b

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4. b) Attempt ANY ONE of the following **(6 Marks)**

i) Draw the block diagram of PCM Transmitter and Receiver and explain its working.

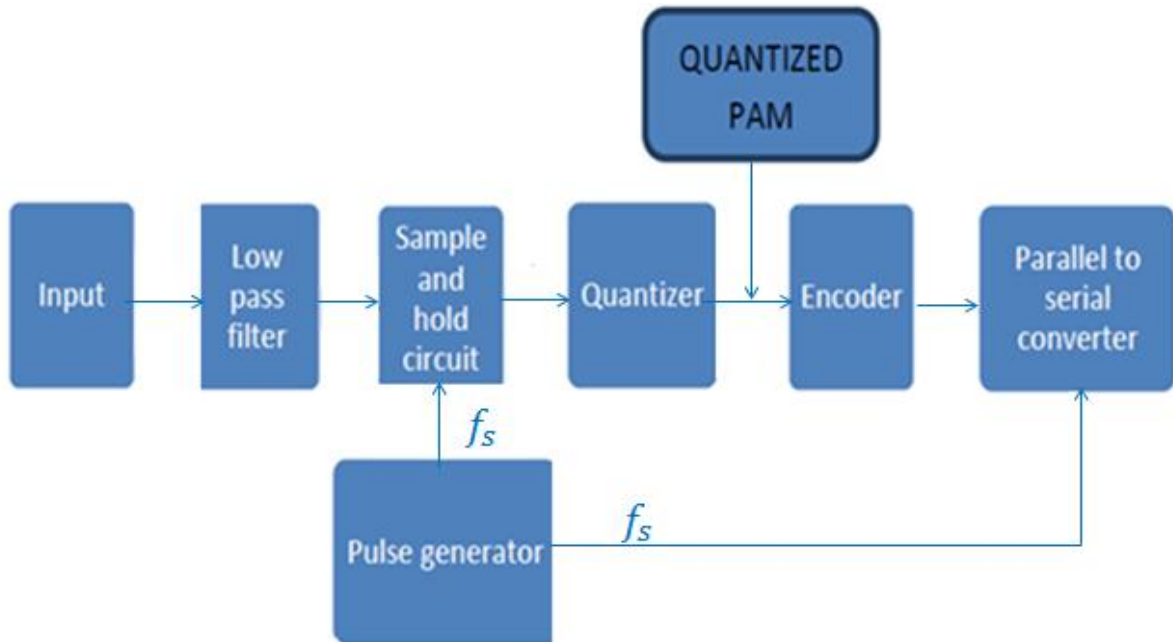Ans. <u>PCM Transmitter Diagram</u> **(2 Mark)**

Fig. block diagram of PCM Transmitter

<u>PCM Transmitter Explanation</u> **(1 Mark)**

- The analog signal x (t) is passes through band limiting / low pass filter, which has a cut-off frequency fc=W Hz. This will ensure x (t) will not have any frequency component higher than "W". In other words, suppresses high frequency components and passes only low frequency signal to avoid 'aliasing error'.
- The band limited analog signal is then applied to sample and circuit where this circuit acts as modulator and both modulating input signal and sampling signal with adequately high sampling rate are inputs to this circuit. Output sample and hold block is a flat topped PAM signal.
- These samples are subjected to operation "quantization" in the "quantizer". The quantizer is used to reduce effect of noise. Quantization is a process of approximation of the value of respective sample in to a finite number that will reduce data bits. The combined effect of sample and quantization produces is 'Quantized PAM' at the quantizer output.
- The Quantized PAM output is analog in nature. So to transmit it through digital communication system the quantized PAM pulses are applied to an encoder which is basically A to D convertor. Each quantized level is converted into N bit digital word by A to D converter.
- The communication system is normally connected to each other using a single cable i.e. serial communication. But the output of ADC is parallel which cannot be transmitted through serial communicating links. So this block will convert the parallel data into serial stream of data bits.
- A pulse generator produces train of rectangular pulses of duration "t" seconds. This signals acts as sampling signals for the sample and hold block. The same signal acts as "clock" signals for parallel to converter .the frequency "f" is adjusted to satisfy the criteria.

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PCM Receiver Diagram   (2 Mark)

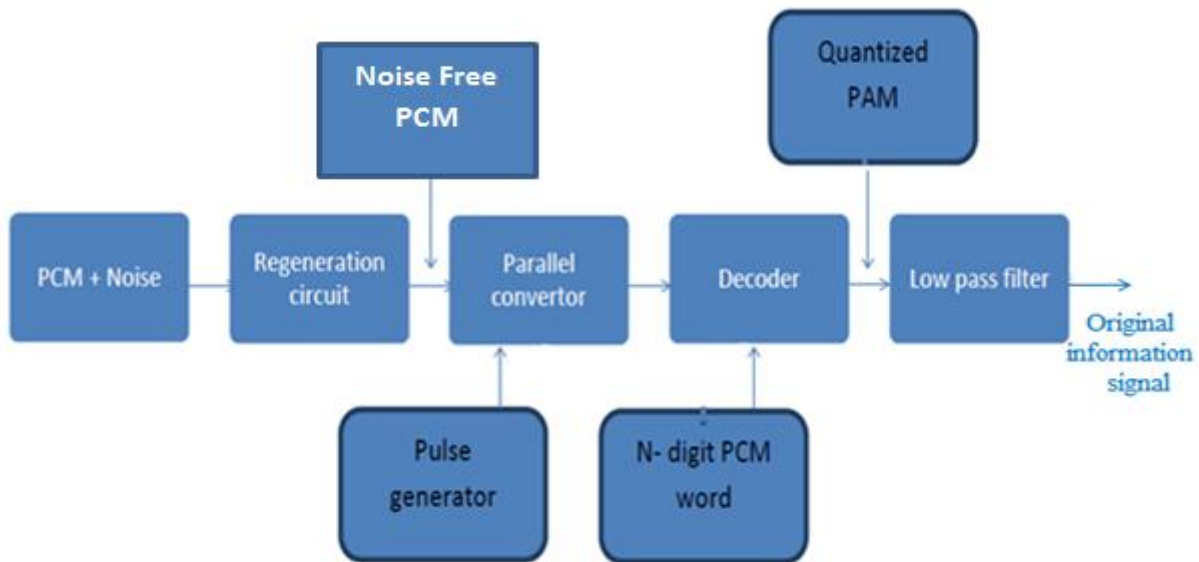Fig. block diagram of PCM Receiver

PCM Receiver Explanation   (1 Mark)
- A PCM signal contaminated with noise is available at the receive input.
- The regeneration circuit at the receiver will separate PCM pulses from noise and will reconstruct original PCM signal.
- The pulse generator has to operate in synchronization with that transmitter .Thus at the regeneration circuit output we get "clear" PCM signal.
- The reconstruction of PCM signal is possibly due to digital of PCM signal.
- Output of this block is then applied to a decoder. The decoder is D to A convertor which performs opposite operation of an encoder
- The decoder output is sequence of quantized PAM signal is thus obtained, at the output of decoder.
- This quantized PAM signal is passed through a low pass filter recovers the analog signal x (t).

ii) Draw the block diagram of TDM and explain its working.

Ans. Diagram   (2 Marks)

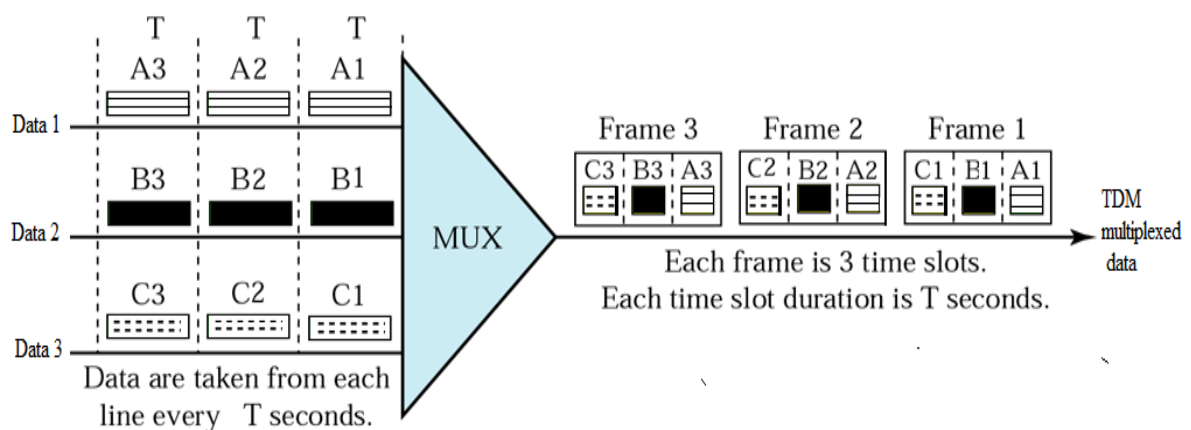Fig. block diagram of TDM

Explanation   **(4 Marks)**

- Process of combining digital signals from several sources whereby each connection occupies a portion of time in the link is called Time Division Multiplexing (TDM).
- Links are sectioned by time rather than frequency.
- Data flow of each connection is divided into units.
- In TDM data units from each input connection is collected in to a frame i.e link combines one unit of each connection to make a frame.
- If we have "n" connection a frame is divided in to "n" time slots and one slot is allowed for each unit. i.e n input connections → n time slots.
- One for each input line, if the duration of input is T, the duration of each slot is T/n and the duration of each frame is T.
- Data rate of link must be n times the duration of a time slot to guarantee flow of data.
- Time slots are grouped into frames; one complete cycle of time slots; each slot dedicated to one device.
- A simple TDM process for three different data transmission is shown above.
- Here, all three data are divided into equal timeslots also called as units.
- And each data unit from all three data are combined / multiplexed together to form TDM frames comprising of small units of all three data which is further transmitted.

Q-5 Attempt ANY FOUR of the following.   **(16 Marks)**

a) Explain with example, how parity helps in detecting any numbers of errors in data.

Ans:- **(Figure-2marks, explanation-2marks)**
The parity checking at the receiver can detect the presence of an error if the parity of the received signal is different from the expected parity. That means if it is known that the parity of the transmitted signal is always going to be "even" and if the received signal has an odd parity then the receiver can conclude that the received signal is not correct. This is as shown in figure.

	P	Message bits	Parity	Receiver's decision
Transmitted code:	0	1 0 0 1 0 1 1 0	Even	Correct word
Received code with one error	0	0 0 0 1 0 1 1 0	Odd	Incorrect word
Received code with three error	0	0 1 0 0 0 1 1 0	Odd	Incorrect word

When a single error or an odd number of errors occur during transmission, the parity of the code word changes. Parity of the received code word is checked at the receiver and change in parity indicates that error is present in the received word. If the presence of error is detected then the receiver will ignore the received byte and request for the retransmission of the same byte to the transmitter.

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b) Explain "Hamming code" with one example.

Ans: **(Definition-1marks, Example-3marks)**
Hamming codes are basically linear block codes. it is an error correcting code. The parity bits are inserted in between the data bits as shown below.

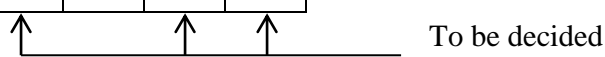| D7	D6	D5	P4	D3	P2	P1	
7bit	6bit	5bit	4bit	3bit	2bit	1bit	7-bit hamming code

Where D-data bits and P- parity bits

- The hamming coded data is then transmitter.

- At the receiver it is coded to get the data back.

- The bits (1, 3, 5, 7),(2,3, 6, 7) and (4, 5, 6,7) are checked for even parity(or odd parity), if all the 4-bit groups mentioned above possess the even parity (or odd parity) then the received code word is correct but if the parity is not matching then error exist. Such error can be located by forming a three bit number out of three parity checks.

- This process can be well explained by following example,

- For Example, suppose a bit word 1 0 1 1 has to be transmitted then the Hamming Code generated before transmission is as follows

  ➢ Step 1: the code word format
    The seven bit Hamming code format is shown below. Given bit word is 1 0 1 1

D7	D6	D5	P4	D3	P2	P1
1	0	1		1		

    To be decided

  ➢ Step 2: Decide P1
    P1 sets the parity of bits P1, D3, D5, and D7. As D7 D5 D3 = 1 1 1 we have to set P1 = 1 in order to have the even parity.

D7	D6	D5	P4	D3	P2	P1
1	0	1		1		1

    Set P1 = 1 to have the even parity of P1, D3, D5, and D7.

  ➢ Step 3: Decide P2
    P2 sets the parity of bits P2, D3, D6, and D7. As D7 D6 D3 = 1 0 1 we have to set P1 = 0 in order to have the even parity.

D7	D6	D5	P4	D3	P2	P1
1	0	1		1	0	1

    Set P2 = 0 to have the even parity of P2, D3, D6, and D7.

  ➢ Step 4: Decide P4
    P4 sets the parity of bits P4, D5, D6, and D7. As D7 D6 D5 = 1 0 1 we have to set P4 = 0 in order to have the even parity.

D7	D6	D5	P4	D3	P2	P1
1	0	1	0	1	0	1

Set P4 = 0 to have the even parity of P4, D5, D6, and D7.

➢ Hence the final Hamming code generated for transmitting given data 1 0 1 1 is

D7	D6	D5	P4	D3	P2	P1
1	0	1	0	1	0	1

(OR)

• For example: Suppose a 7-bit hamming code is received as 1110101 and parity used is assumed to be even .hence we can detect and correct the code as

➢ **Step1:** Received 7bit hamming code is applied to hamming code format as

D7	D6	D5	P4	D3	P2	P1
1	1	1	0	1	1	1

➢ **Step2:** Check bits for P4 bit

    i.e.   P4   D5 D6 D7

    | 0 | 1 | 1 | 1 | = odd parity hence error

So, P4=1

➢ **Step 3:** check bits for P2bit

    i.e.   P2   D3   D6 D7

    | 0 | 1 | 1 | 1 | = odd parity hence error

So, P2=1

➢ **Step 4:** check bits for P1 bit

    i.e. P1   D3   D5   D7

    | 1 | 1 | 1 | 1 | = even parity hence no error

So, P1=0

Hence the error word is

E =	P4	P2	P1
	1	1	0

➢ **Step 5:** decimal equivalent of 110 is 6 hence 6th bit is incorrect so invert it and the correct code word will be,

D7	D6	D5	P4	D3	P2	P1
1	0	1	0	1	0	1

➢ Hence by using this method we can detect as well as correct the error in the transmitted coed word. But it can locate a single bit error and fails in detecting the burst error.

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c) Describe the concept of CDMA with diagram.

Ans. **(Explanation – 2 Marks, Diagram - 2 Marks)**

Ans:-

- In CDMA more than one user is allowed to share a channel or sub channel with the help of DSSS signals.
- In CDMA each user is given a unique code sequence. This sequence allows the user to spread the information signal across the assigned frequency. At the receiver the signal received from various users are separated by checking the cross correlation of the received signal with each possible user sequence.
- In CDMA as the bandwidth as well as time of the channel is being shared by users. In CDMA the users access the channel in a random manner. Hence the signals transmitted by multiple users will overlap both in time and in frequency. CDMA does not need any synchronization.

Diagram:-

Structure of CDMA
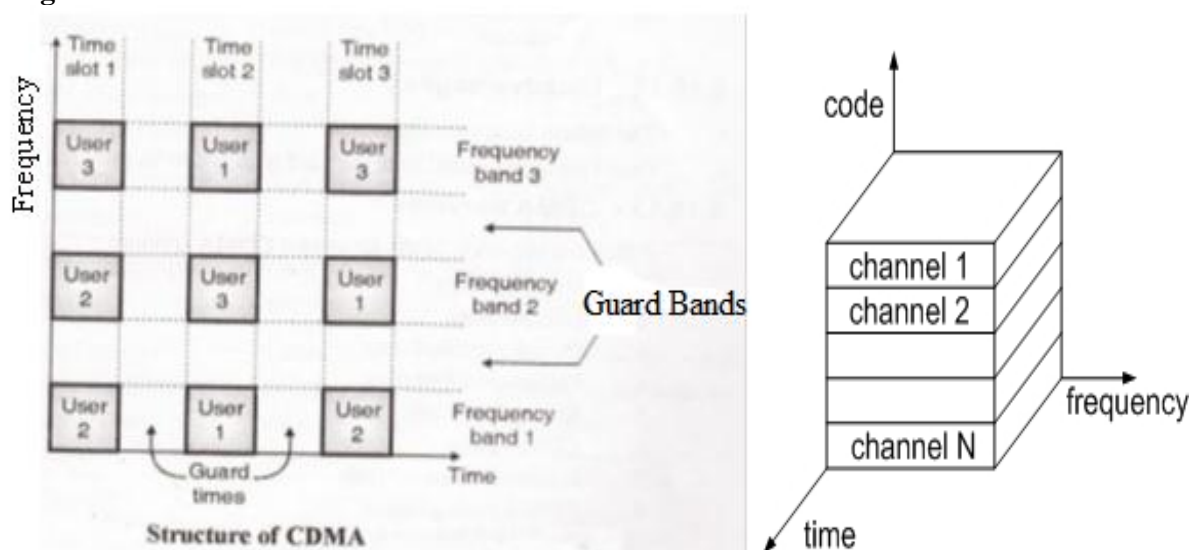
d) Explain Fast frequency hopping with suitable diagram.

Ans. **(Explanation-2marks, Diagram-2marks)**

- The fast frequency hopping is used for defeating a smart jammer who tries to interfere the transmission. Before the jammer could understand the frequency band which is being used by the transmitter, the transmitted signal is hopped to a new carrier frequency. The data sequence used for the fast hopping is same as the one used for the slow hopping. The number of bits per MFSK symbol K=2.
- Therefore the number of MFSK tones=2^k=4.The length of PN segment per hop i.e. n=3.
- Therefore the total number of frequency hops=2^3=8.The PN sequence decides the hopping frequency. Two successive input binary bits 0 1 form the first symbol. During this symbol duration the PN sequence has two distinct values viz. 001 & 110.Therefore one symbol duration corresponds to two frequency hops.
- The frequency of the MFSK modulator for symbol 01 is f2 and the output of the synthesizer corresponding to 001 & 110 outputs of the PN sequence generator are say FH1 & FH6.Therefore the transmitted frequencies are (FH1+f2) and (HF6+f2).
- **The operation for the first symbol 01 is summarized below**

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Symbol:01	
Frequency of MFSK modulator = f2	
Output of PN code generator	Frequency of synthesizer (hop)
001	FH1
110	FH6
Transmitted frequencies: (f2+FH1) and (f2+FH6)	

Diagram:
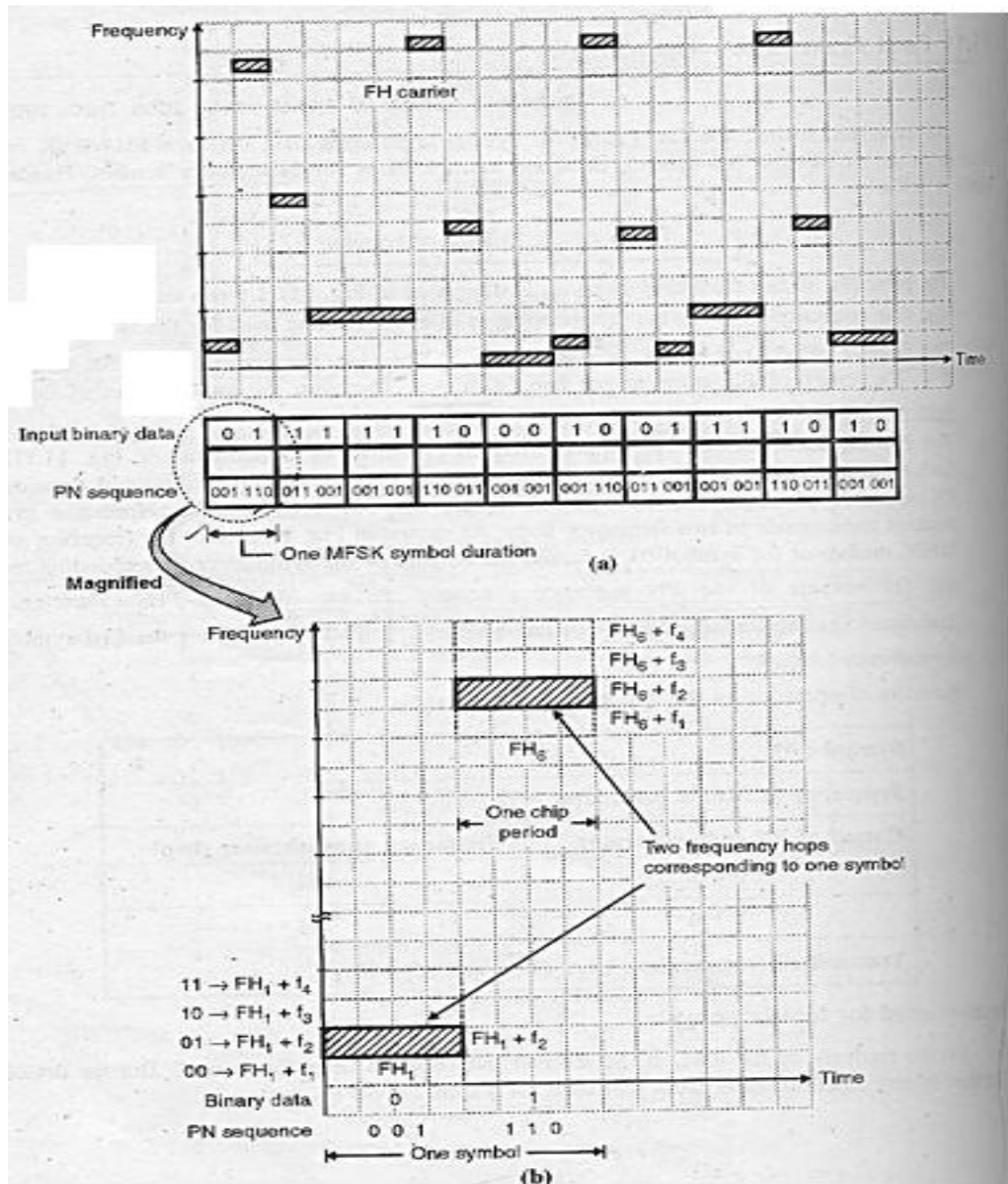
(OR)

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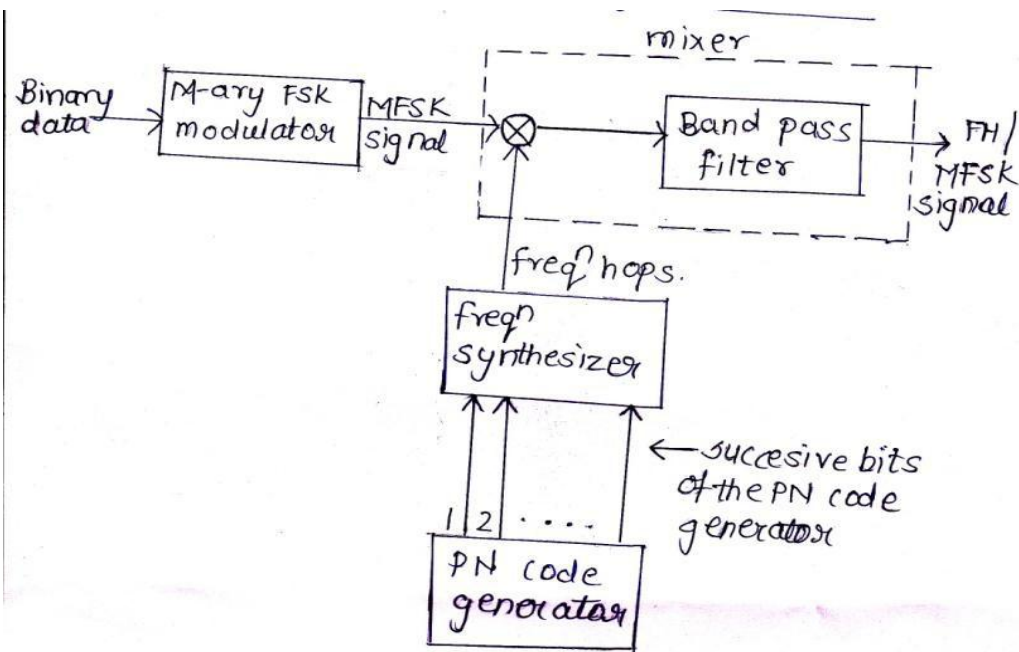
e) State the types of errors present in the digital communication system. State the causes of error.

Ans:- <u>Types of errors</u>   **(2 Marks)**

   The errors introduced in the data bits during their transmission can be categorized as,
   1. Content errors
   2. Flow integrity errors

   Depending on the number of bits in the error, the errors can be classified into two types as:
   1. Single bit error
   2. Burst error

Causes of errors: **(any 2 points- 2 Marks)**

Due to addition of noise in transmission & reception of data.
   1. If data block is lost in the network as it has been delivered to wrong destination.
   2. If two or more bits from data unit such as a byte change from 1 to 0 or 0 to 1.

f) Draw block diagram of FDM transmitter and FDM receiver. Describe its working.

Ans:- **(Block diagram of transmitter and Receiver 2 Marks; Explanation of Both -2Marks)**

Frequency Division Multiplexing (FDM) is based on the idea that number of signals can share the bandwidth of a common communication channel. The multiple signals to be transmitted over this channel are each used to modulate a separate carrier. Each carrier is on a different frequency. The modulated carrier are then added together to form a single complex signal that is transmitted over the single channel. The spectrum of the FDM signal is as shown below.

<u>Block diagram of multiplexer of FDM: Transmitter</u>
Fig below shows a general block diagram of FDM system. Each signal to be transmitted is fed to modulator circuit. The carrier for each modulation fc is on a different frequency. The carrier frequencies are equally spaced from one another over a specific frequency range. Each input signals given portion of the bandwidth. Another standard modulation like AM, SSB, FM or PM can be done.

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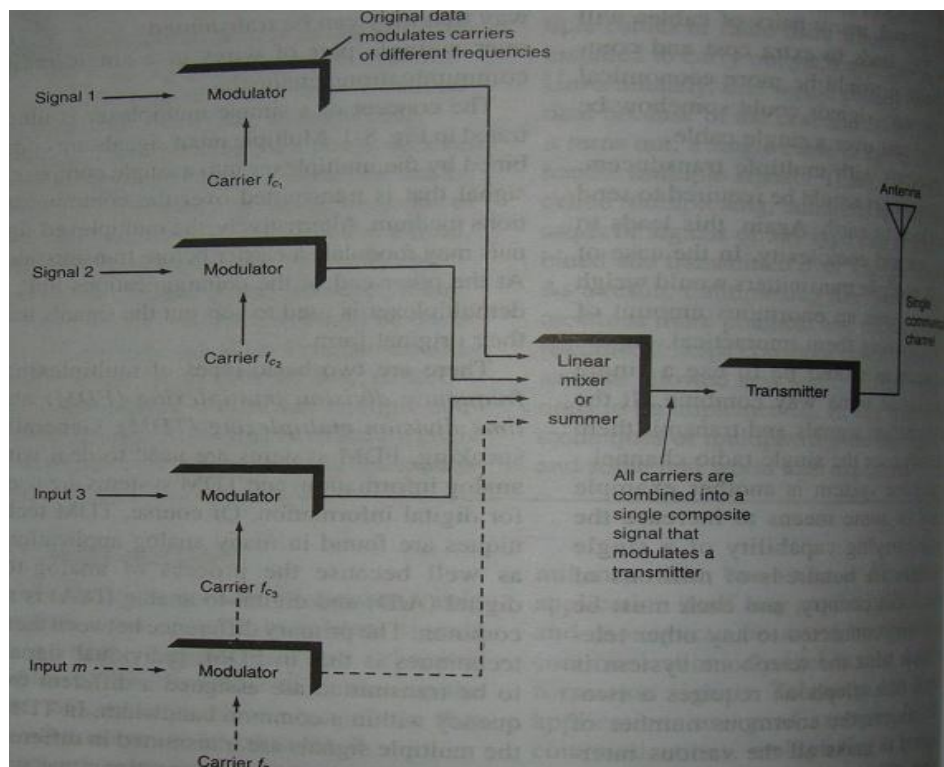
The modulator output having side band information are added together in a linear mixer in which all the signals are simply added together algebraically. The resulting output signal is composite of all carriers containing their modulation. This signals transmitted over single communication channel.

Block diagram of de multiplexer of FDM: Receiver
The receiving portion of FDM is as shown below. A receiver picks up the signal and demodulates it. This is sent to a group of band pass filter. Each centered on one of the carrier frequencies. Each filter passes only its channel and rejects all other.

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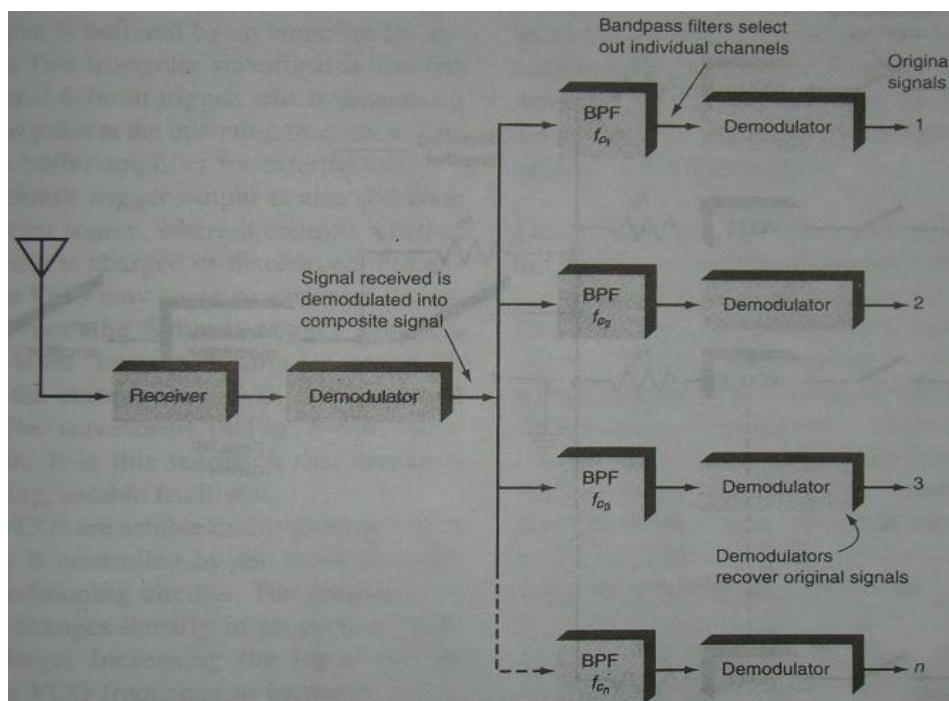
A channel demodulator then recovers each original input signal. The example of FDM system is Telemetry, telephone and FM stereo.

Q-6 Attempt ANY FOUR of the following. (16 Marks)

a) Calculate the capacity of a Gaussian channel having bandwidth of 100MHz & S/N =20dB.

Ans:- (Formula 2 Marks, Correct answer 2 Marks)

According to Shannon Hartley theorem

$$C=B\log_2(1+S/N)$$

Substituting the values we get,

$$C=100\times10^6\log_2(1+20dB)$$

$$C=100\times10^6\log_2(1+100) \qquad\qquad ;20dB=100$$

$$C=100\times10^6\log_2(101)$$

$$\mathbf{C=2.004\times10^8 bits/second}$$

b) Explain slow frequency hopping with the help of suitable diagram.

Ans:- (Explanation-2marks, Diagram-2marks)

Slow frequency hopping- In slow frequency hopping the symbol rate Rs of the MFSK signal is an integer multiple of the hop rate Rn that means several symbols are transmitted corresponding to each frequency hop.

Block Diagram of transmitter:-
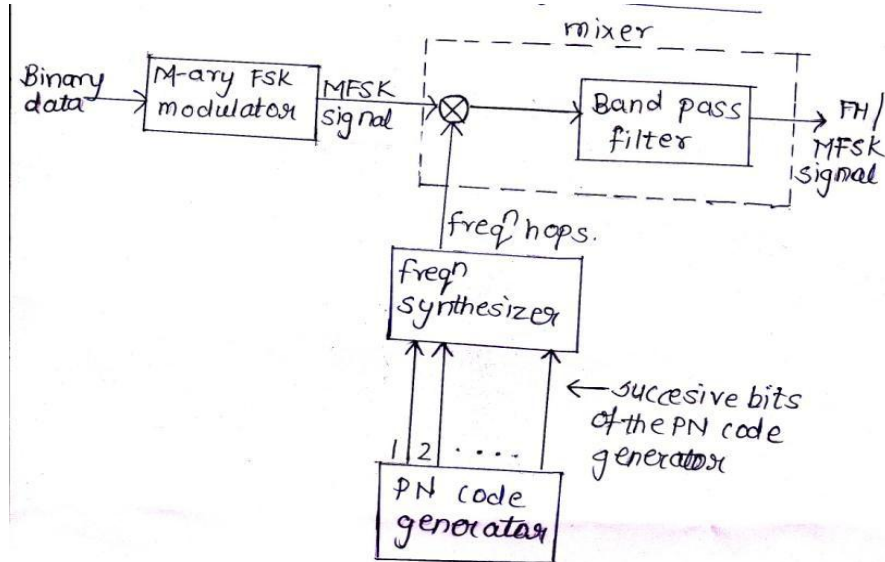
- The binary data sequence b (t) is applied to the M - ary FSK modulator the o/p of which goes to the i/p of mixer.
- The other i/p to the mixer block is obtained from a digital frequency synthesizer. The mixer is consisting of multiplier followed by a band pass filter. At the multiplier o/p, we get two frequencies their sum and their difference frequency components.
- The band pass filter is designed to select only the sum frequency component and rejecting all other components only sum components of frequency is transmitted. Each frequency hop is mixed with MFSK signal to produce the transmitted signal. Frequency hops at the o/p of synthesizer are controlled by successive bits at the o/p of PN code generator. The o/p bit of code generator change randomly.

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- Frequency hops produced will vary in a random manner. The total BW of the transmitted FH/MFSK signal is equal to the sum of all the frequency hops. BW of transmitted signal is very large in GHz.
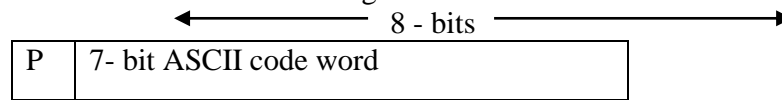
c) Explain ASCII code with example.

Ans:- **(Explanation-3marks, Example-1mark)**

ASCII (American standard code for information interchange):-

- It is designed by American National Standards Institute.
- It is a 7 bit code with $2^7 = 128$ possible combination and all of them have defined meaning.
- The ASCII code set consists of 94 printable character. SPACE & DELETE characters & 32 control symbol.
- The control symbol are code reserved for special function, e.g. CR(carriage return) & LF(line feed) are the symbol used for basic operation of printers & displays.
- Symbol ACK(acknowledgement) or NAK(negative acknowledgement) are used for error control.
- Symbol STX(start to text) and ETX (end to text) are used for grouping of data character.
- ASCII is a 7 bit code but the eight bit is often used.
- This bit is called as parity bit.
- Parity bit is used to detect the error introduced during transmission.
- Parity bit is generally added in the most significant bit(MSB)

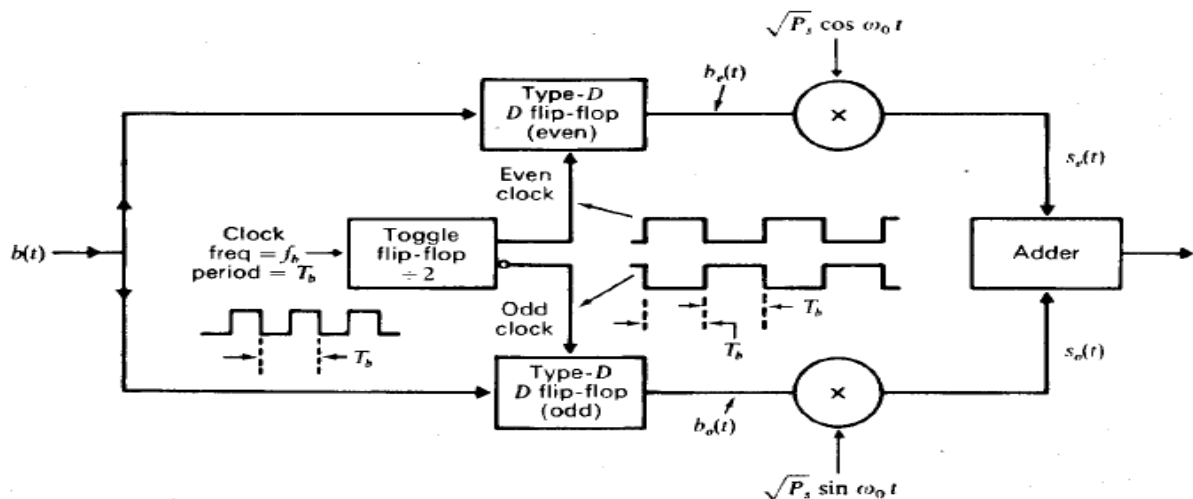The eight bit ASCII code word format is shown in figure.

$$\overleftarrow{\hspace{3cm}} 8 \text{ - bits} \overrightarrow{\hspace{3cm}}$$

P	7- bit ASCII code word

MSB parity bit
ASCII code word for character 'K'
Example- Character "K" is (4B) therefore its code is 1001011.

d) Draw & explain QPSK modulator.

Ans:- **(Diagram-2 Marks, Explanation-2 Marks)**

QPSK Modulator Block Diagram

Explanation

- The mechanism by which a bit stream b(t) generates a QPSK signal for transmission is shown above.
- The toggle flip flop is driven by clock pulses whose time period is bit time T_b. the toggle flip flop generates odd and even clock pulses.

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- These clock pulses have time period $2T_b$ and the active edges of both the pulses are separated by bit time T_b.
- The data stream b (t) is applied as the data input to both the D flip flops which are driven by odd and even clock pulses respectively.
- The D flip flops register alternate bits in the stream b(t) and hold each such register bits for the two bit intervals i.e $2T_b$.
- The output of D flip flops are $b_e(t)$ & $b_o(t)$ which are nothing but even data stream and odd data stream respectively.
- These odd and even data streams $b_e(t)$ & $b_o(t)$ are superimposed on a carrier $\sqrt{2Ps}\cos\omega_0 t$ and $\sqrt{2Ps}\sin\omega_0 t$ respectively to generate the modulated output signal $s_e(t)$ & $s_o(t)$.
- These signals are then added together to get the final modulated QPSK signal

$$V_{QPSK}(t) = \sqrt{2Ps}\cos\omega_0 t + \sqrt{2Ps}\sin\omega_0 t$$

(OR)
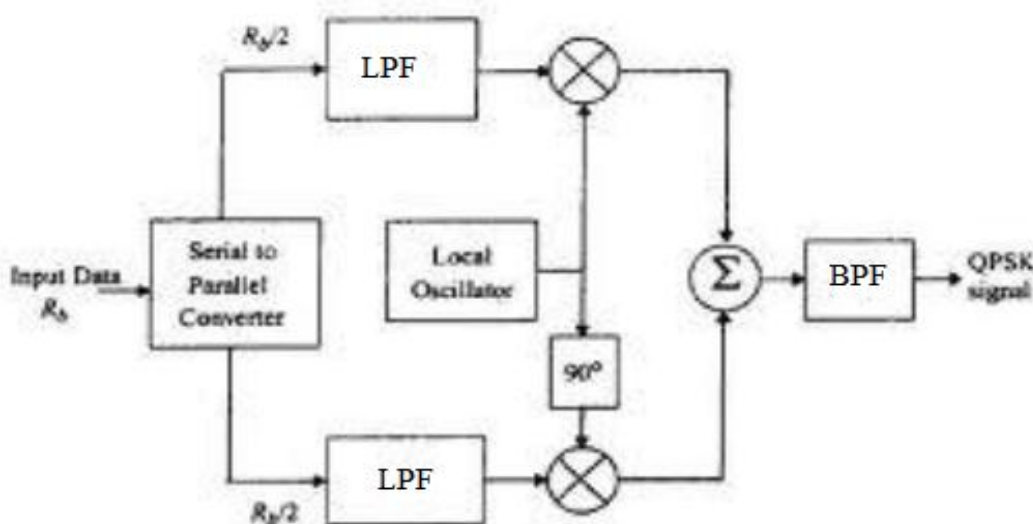
QPSK Modulator Block Diagram

Explanation
First unipolar binary messages are converted into bipolar NRZ sequence. Next, the bit stream is split into in-phase (even) and quadrature (odd) bit streams each with a bit rate .
Two orthogonal carriers separately modulate two binary sequences. They are summed to produce a QPSK signal.
Finally, the band pass filter at the output prevents the spillover of signal energy into adjacent channels and also removes the out-of-band spurious signals generated during the modulation process.
In most wireless and other RF implementations, pulse shaping is done at the baseband to provide proper RF filtering at the output.

e) What is intersymbol interference? Explain with suitable diagram. How to reduce it.
Ans:- **(Definition-1mark, explanation-1mark, diagram-1mark, Remedy-1mark)**
In a communication system when the data is being transmitted in the form of pulses (bits), the output produced at the receiver due to the other bits or symbols interferes with the output produced by the desired bit. This is called intersymbol interference (ISI).The intersymbol interference will introduce error in the detected signal. The ISI arises due to the imperfection in the overall frequency response of the system.

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When a short pulse of duration Tb seconds is transmitted through a band limited system, then the frequency components contain in the input pulse are differentially attenuated and more importantly differentially delayed by the system. Due to this the pulse appearing at the output of the system will be dispersed over an interval which is longer than Tb seconds. Due to this dispersion, the symbols each of duration Tb will interfere the each other when transmitted over the communication channel. This will result in intersymbol interference. The transmitted pulse of duration Tb seconds & the dispersed pulse of duration more than Tb seconds are shown in figure.
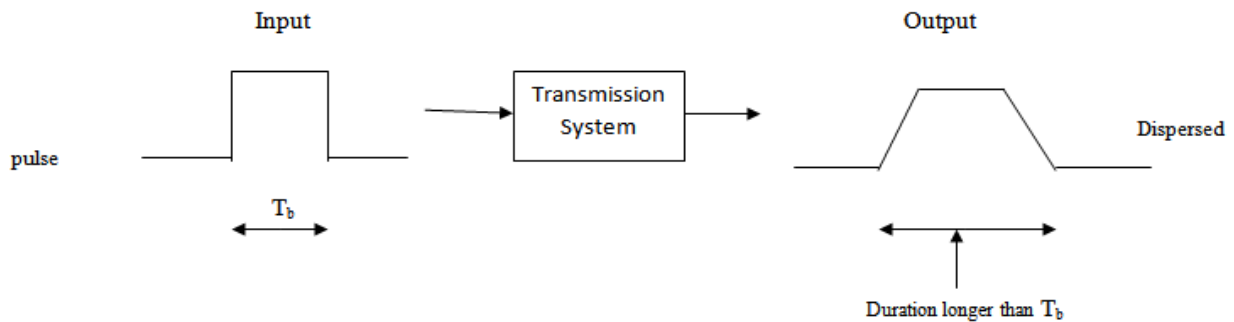
Remedy to reduce the ISI:
It has been proved that the function which produces a zero intersymbol interference is a sine function. Thus instead of a rectangular pulse if we transmit a sine pulse then the ISI can be reduce to zero.

This is known as Nyquist pulse shaping. The sine pulse transmitted to have a zero ISI is shown in figure below-
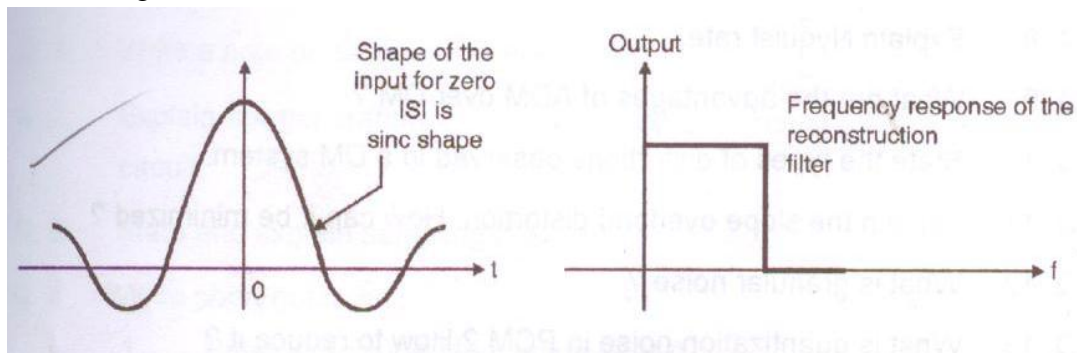
We know that Fourier transform of a sine pulse is a rectangular function. Hence to preserve all the frequency components, the frequency response of the filter must be exactly flat in the pass band & zero in the attenuation band as shown in figure below-
This type of filter is practically not present. Hence practically the frequency response of the filter is modified as shown in following figure with different roll of factor "α" to obtain the achievable filter response curves.