MAHARASHTRA STATE BOARD OF TECHNICAL EDUCATION
(Autonomous)
(ISO/IEC – 27001 – 2005 Certified)

WINTER – 12 EXAMINATION
Model Answer

Subject Code: **12187**

Q1. a)	**Attempt any THREE of the following:**	**12 Marks**
Ans. i		4 Marks for Any 4 points (01 mark for each point)

Sr. No.	**Microprocessor**	**Microcontroller**
1.	Microprocessor does not have inbuilt RAM/ROM	Microcontroller Has inbuilt/on chip RAM and ROM
2.	Does not have inbuilt timer and serial ports	Inbuilt Timer and serial ports available
3.	Program and data are stored in same memory	Separate memory to store data and program
4.	Less multifunction pins on the IC	Many multi-function pins on the IC.
5.	Many instructions to read/write data from/ to External memory	Few instructions to read/write data from/to External memory.

Ans. ii

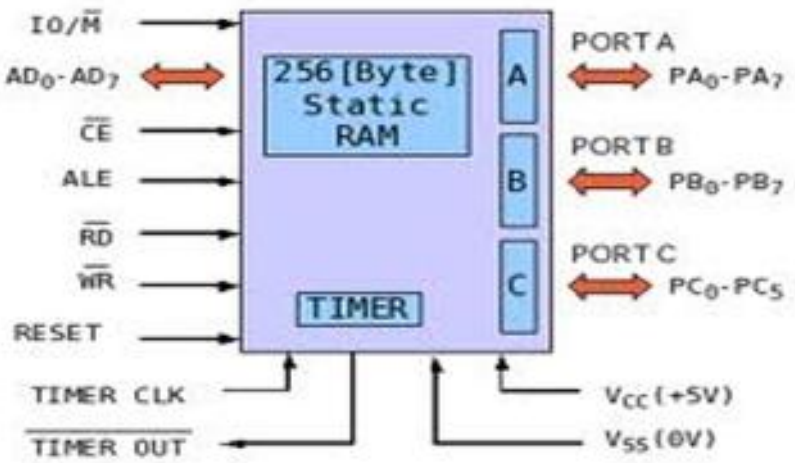
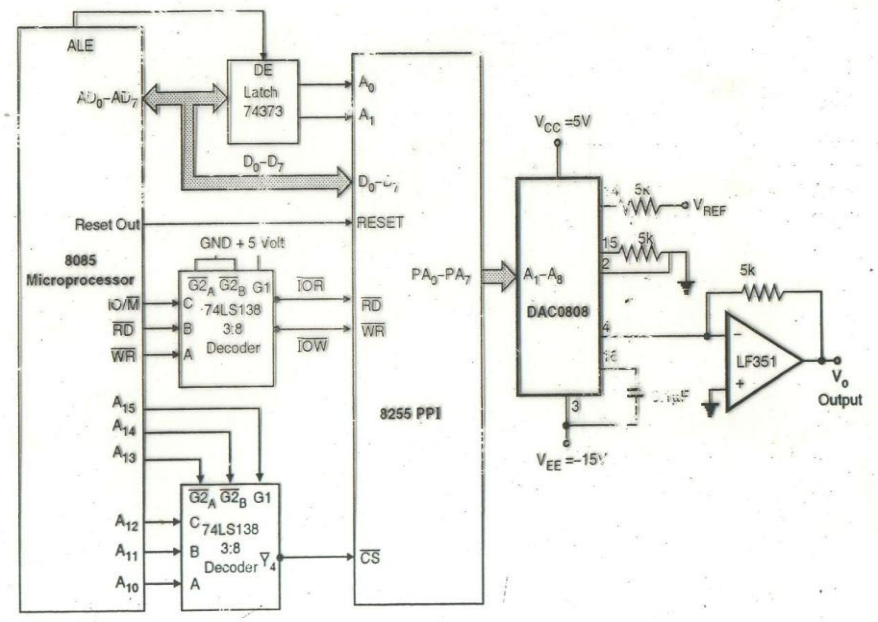


Fig: Block diagram of 8155

4 marks for Neat and labeled diagram

Ans. iii	**ALP:**
	
	Sample program:
	MOV A,#50H ;Load the first no. in Accumulator
	ADD A,#60 ;Add the second no. with Accumulator
	DAA ;Adjust result to BCD
	MOV 41H, A ;Store the result in memory location 41H
	END
		04 marks for relevant logic/ALP

Ans. iv	➔ $PSEN$ Program store enable is the output control signal activated every 6 oscillator periods, while fetching the external program memory. It is the read strobe to external program memory. During the internal program execution it remains high. ➔ EA External excess pin when held high, executes instruction from the internal program memory till address 0FFF H; beyond this address, the instructions are fetched from external program memory. If this pin is low, all the instructions are fetched from the external memory. During normal operation, this pin should not be floated. ➔ $XTAL_1$ is the input to the inverting amplifier that forms part of the oscillator circle. In case of external clock the pin must be connected to ground. ➔ $XTAL_2$ is the output of inverting amplifier that forms a part of the oscillator and input to the internal clock generated. In case of external clock it must be connected to ground.	01 mark for each pin
b)	**Attempt any <u>ONE</u> of the following:**	**6 Marks**
Ans. i	.  Fig: Interfacing Diagram of DAC with 8085	03 Marks for Diagram

DAC0800/0808 is an 8 bit high speed D to A converter. Figure shows interfacing of DAC 0808/08 09 with 8085 microprocessor. Port A of 8255 is used as output Port. It is connected to A1 to A8 pins of DAC.

When OUT PORT A instruction is executed digital data from accumulator is transferred to DAC.DAC converts these digital data into analog and controls further analog circuit.

Control word of 8255
1 x xxx 0 0 x =80 H
Port A=81 H
Port B=82 H
Port C=83 H

Label	Opcode	Operand	Description
	MVI OUT	A, 80h CWR	Initialize ports 8255
START: UP:	MVI OUT CALL INR OUT CPI JNZ	A,00h Port A Delay A PORT A FF H UP	Generate positive Ramp
LOOP;	DCR OUT CALL CPI JNZ JMP	A PORT A DELAY 00 H LOOP START	Generate negative Ramp

Any Delay program should be mentioned**.**

03 Marks for Program

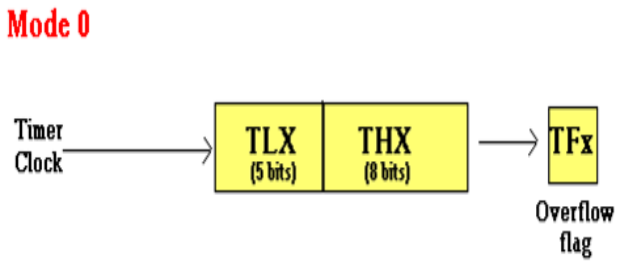
Ans. ii

To operate the timer/counter the bit TR1/TR0 in TCON register must be set and gate bit in TMOD register must be reset or INT1/INT0 i/p pin should be 1

Operating modes of Timer: The timer may operate in any of the four modes that are determined byM1 and M0 bit in TMOD register.

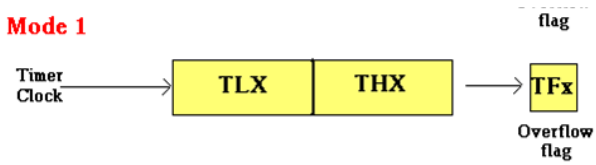
1½ Marks for each mode

Mode 0:



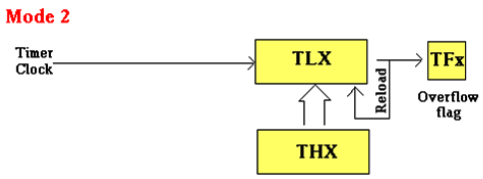
In mode0 the register THX is used as 8 bit counter and TLX is used as 5 bit counter. The pulse i/p is divided by $(32)_{10}$so that TH counts. Hence original oscillator frequency is divided by $(384)_{10}$.The timer flag is set when THX rolls over from FF to 00H.

Mode 1:



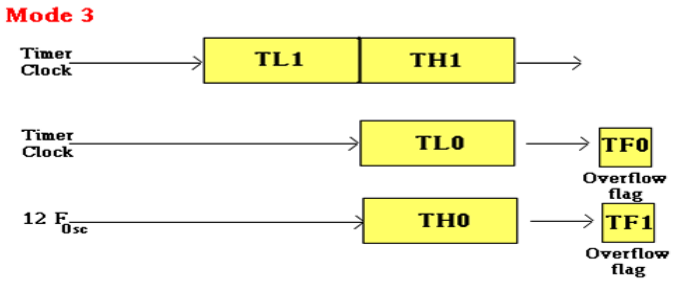
It is similar to Mode 0 except TLX is configured as a full 8-bit counter. Hence pulse input is divided by 256_{10} so that TH counts the timer flag is set when THX rolls over from FF to 00H.

Mode 2

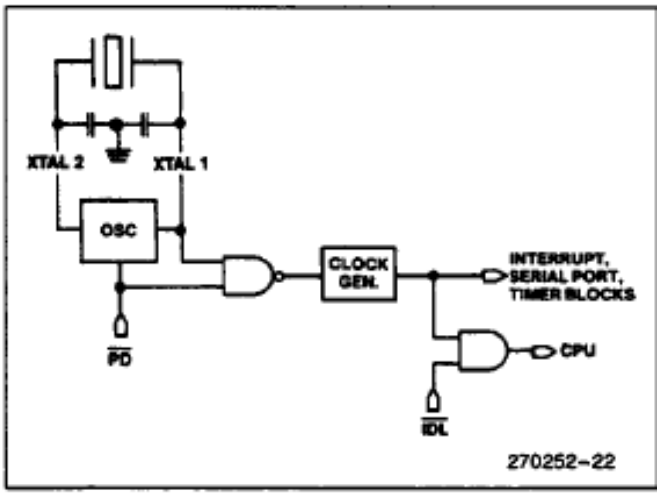


In this mode only TLX is used as 8-bit counter. THX is used to hold the value which is loaded in TLX initially. Everytime TLX overflows from FFH to 00H the timer flag is set and the value from THX is automatically reloaded in TLX register.

Mode 3



In this mode, timer 0 becomes two completed separate 8-bit timers. TL0 is controlled by gate arrangement of timer 0 and sets timer 0 flag when it overflows. TH0 receives the timer clock under the control of TR1 bit and sets TF1 flag when it overflows. Timer 1 may be used in mode 0, 1 and 2 with one important exception that no interrupt will be generated by the timer when the timer 0 is using TF1 overflow flag.

Q2.	**Attempt any <u>FOUR</u> of the following:**	**16 Marks**
Ans. a.	**i. MOV A, @RI** ➔ Copy contents of memory location whose address is specified either in R0 or R1 ➔ Addressing mode: indirect ➔ E.g. MOV A, @R1 Move the contents of memory location stored in R 1 to the ACC. **ii. MOVX A, @DPTR** ➔ Move the contents of the memory location stored in DPTR in to the acc. ➔ Addressing mode indirect **iii. SWAP A** ➔ Interchanges the low and high order nibbles of the accumulator ➔ Addressing mode: register specific. **iv. DA A** ➔ The DAA instruction operates on the result of addition of two packed BCD numbers and gives the final result in decimal system. ➔ Addressing mode: register specific.	01 mark for each instruction
Ans. b.	 Fig: Power saving mode of 8051 microcontroller ➔ Format of PCON: (MSB) (LSB) SMOD | - | - | - | GF1 | GF0 | PD | IDL	01 mark for diagram 03 mark for Explanation

SMOD	Double Baud rates bit. When set to 1 and Timer 1 is used to generate baud rate, and the serial port is used in modes 1, 2, or 3.
PD	Power Down bit. Setting this bit activates power down operation
IDL	Idle mode bit. Setting this bit activates idle mode operation

IDLE MODE
In the Idle mode, the internal clock signal is gated off to the CPU, but not to the Interrupt, Timer, and Serial Port functions.

The CPU status is preserved in its entirety,the Stack Pointer, Program Counter, Program Status Word, Accumulator, and all other registers maintain their data during Idle. The port pins hold the logical state they had at the time idle mode was activated. ALE and PSEN hold at logic high levels.

There are two ways to terminate the Idle mode.

i) Activation of any enabled interrupt will cause PCON.O to be cleared and idle mode is terminated.

ii) Hard ware reset: that is signal at RST pin clears IDEAL bit IN PCON register directly. At this time, CPU resumes the program execution from where it left off.

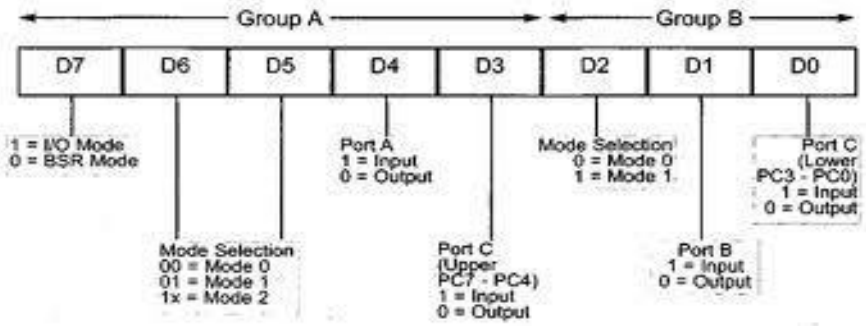
POWER DOWN MODE
An instruction that sets PCON.1 causes that to be the last instruction executed before going into the Power Down mode. In the Power Down mode, the on-chip oscillator is stopped. With the clock frozen, all functions are stopped, but the on-chip RAM and Special Function Register are maintained held. The port pins output the values held by their respective SFRS. ALE and PSEN are held low.

Termination from power down mode: an exit from this mode is hardware reset.
Reset defines all SFRs but doesn't change on chip RAM.

Ans c.

(Control word for port A as i/p and port B & C as o/p --02 marks)

02 Marks for Control word format and explanation



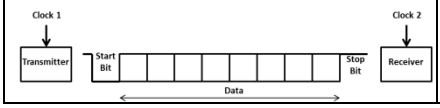
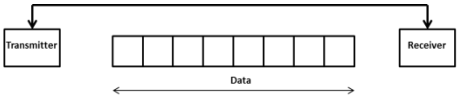
PortA as i/p
Port B & C as o/p

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	0	0	0	0

=90 H

02 Marks for control word

Ans. d.

Asynchronous data transfer	**Synchronous data transfer**
Used to transfer one character at a time	Used to transfer group of character at a time
Data transmission rate<= 20kbps	Data transfer rate>=20kpbs
Transmission begins with start bit followed by data and then stop bit	First synchronous character is transmitted and then data is transmitted
Different clock sources are required for transmitter and receiver	Same clock sources are required or transmitter and receiver
	

01 mark for Any four points

Ans e.

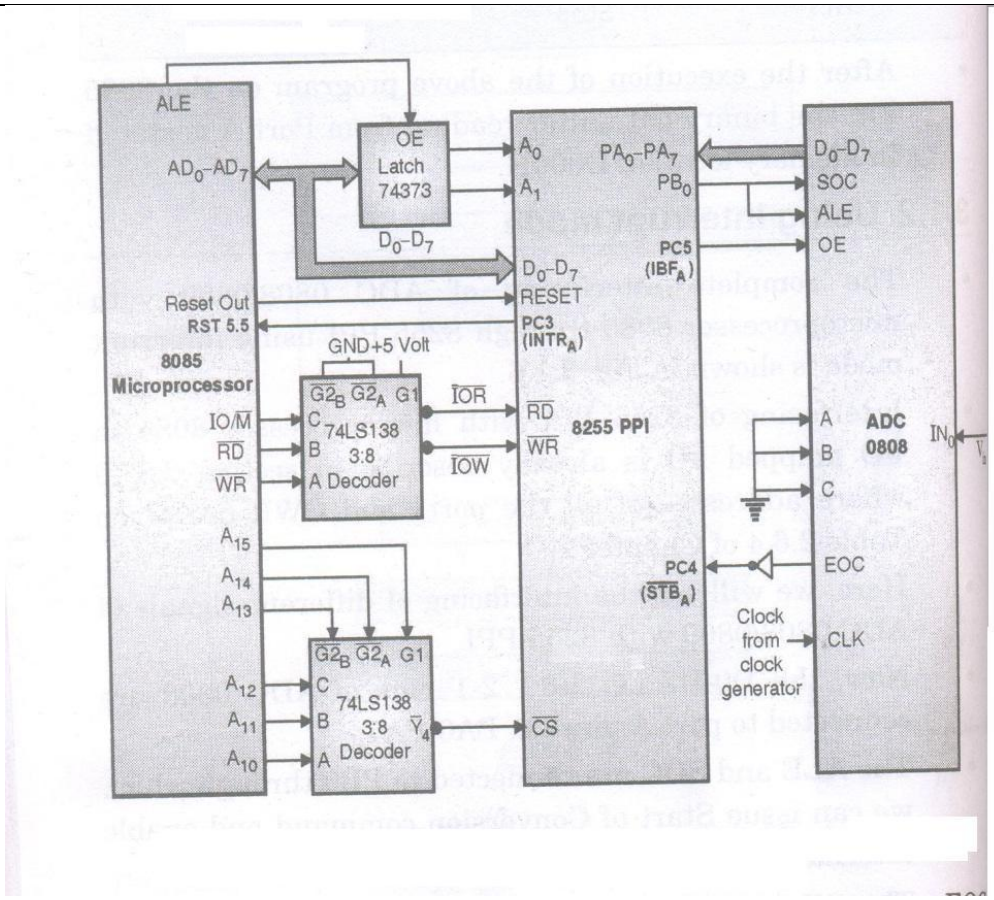
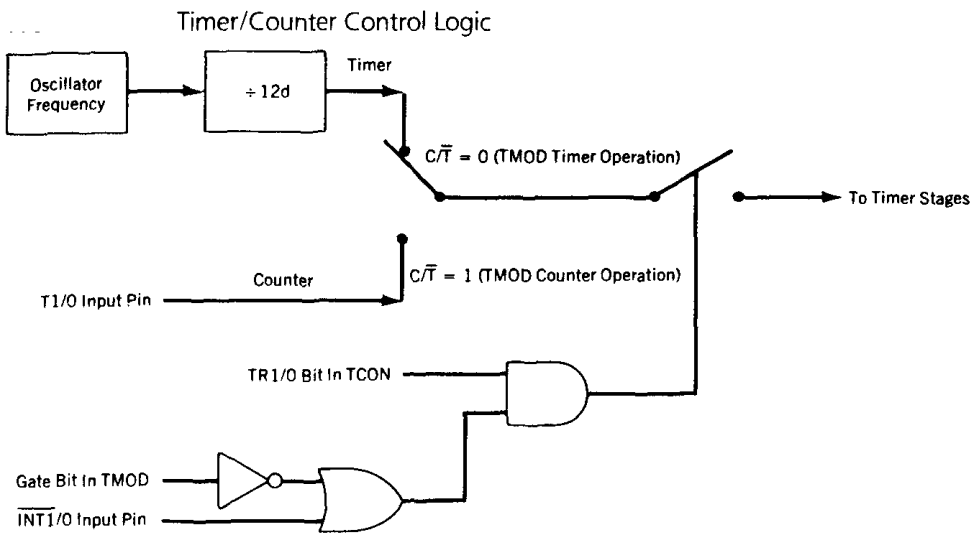


Fig: Interfacing Diagram of A-D Converter with 8085

04 marks for Correct interfacing diagram

Ans. f.	8051 has two 16-bit programmable UP timers/counters. They can be configured to operate either as timers or as event counters. The names of the two counters are T0 and T1 respectively. The timer/ content is available in four 8-bit special function registers, viz. TL0,TH0, TL1 and TH1 respectively. In the "timer" function mode, the counter is incremented in every machine cycle. Thus, one can think of it as counting machine cycles. Hence the clock rate is 1/12th of the oscillator frequency. In the "counter" function mode, the register is incremented in response to a 1 to 0 transition at its corresponding external input pin (T0 or T1). It requires 2 machine cycles to detect a high to low transition. Hence maximum count rate is 1/24th of oscillator frequency. The operation of the timers/counters is controlled by two special function registers, TMOD and TCON respectively.  	04 marks for Description

3.	**Attempt any <u>FOUR</u> of the following:**	**16 Marks**
Ans. a.	**List Any four Addressing modes ---2 Marks.** **One example of each---- 2 Marks.** There are a number of addressing modes available to the 8051 instruction set, as follows: There are a number of addressing modes available to the 8051 instruction set, as follows: 1. Immediate Addressing mode 2. Register Addressing mode 3. Direct Addressing mode 4. Register Indirect addressing mode 5. Relative Addressing mode 6. Absolute addressing mode 7. Long Addressing mode 8. Indexed Addressing mode **1) Immediate Addressing mode:** Immediate addressing simply means that the operand (which immediately follows the Instruction op. code) is the data value to be used. For example the instruction: **MOV A, #25H ; Load 25H into A** Moves the value 25H into the accumulator The # symbol tells the assembler that the immediate addressing mode is to be used. **2) Register Addressing Mode:** One of the eight general-registers, R0 to R7, can be specified as the instruction Operand. The assembly language documentation refers to a register generically as Rn. An example instruction using register addressing is : **ADD A, R5 ; Add the contents of register R5 to contents of A (accumulator)** Here the contents of R5 are added to the accumulator. One advantage of register addressing is that the instructions tend to be short, single byte instructions. **3) Direct Addressing Mode:** Direct addressing means that the data value is obtained directly from the memory location specified in the operand. For example consider the instruction: **MOV R0, 40H ; Save contents of RAM location 40H in R0.** The instruction reads the data from Internal RAM address 40H and stores this in the R0. Direct addressing can be used to access Internal RAM , including the SFR registers. **4) Register Indirect Addressing Mode:** Indirect addressing provides a powerful addressing capability, which needs to be appreciated.	

An example instruction, which uses indirect addressing, is as follows:
MOV A, @R0 ; move contents of RAM location whose
; address is held by R0 into A
Note the @ symbol indicated that the indirect addressing mode is used. If the data is inside the CPU, only registers R0 & R1 are used for this purpose.

5) Relative Addressing Mode:
This is a special addressing mode used with certain jump instructions. The relative address, often referred to as an offset, is an 8-bit signed number, which is automatically added to the PC to make the address of the next instruction. The 8-bitsigned offset value gives an address range of + 127 to –128 locations.

Consider the following example:
SJMP LABEL_X
An advantage of relative addressing is that the program code is easy to relocate in memory in that the addressing is relative to the position in memory.

6) Absolute addressing Mode:
Absolute addressing within the 8051 is used only by the AJMP (Absolute Jump) and
ACALL (Absolute Call) instructions.

7) Long Addressing Mode:
The long addressing mode within the 8051 is used with the instructions LJMP and
LCALL. The address specifies a full 16 bit destination address so that a jump or a call
can be made to a location within a 64KByte code memory space (216 = 64K).

An example instruction is:
LJMP 5000h ; full 16 bit address is specified in operand

8) Indexed Addressing Mode:
With indexed addressing a separate register, either the program counter, PC, or the data pointer DTPR, is used as a base address and the accumulator is used as an offset address. The effective address is formed by adding the value from the base address to the value from the offset address. Indexed addressing in the 8051 is used with the JMP or MOVC instructions. Look up tables are easy to implement with the help of index addressing.

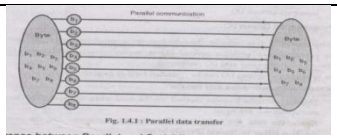
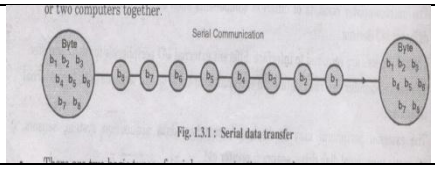
Consider the example instruction:
MOVC A, @A+DPTR

MOVC is a move instruction, which moves data from the external code memory space. The address operand in this example is formed by adding the content of the DPTR register to the accumulator value. Here the DPTR value is referred to as the base address and the accumulator value us referred to as the index address.

Ans. b.	Assume 10 bytes are stored in the internal memory from address 40H. And starting address of the destination block is 50H.
	
	Program:
	; Write a program to transfer a block of data in internal RAM.
	
	ORG 0000H ;Program from 0000H
	CLR PSW.3 ; select bank 0
	CLR PSW.4 ;
	MOV R3, #0AH ; Initialize Byte counter
	MOV R0, #40H ; Initialize memory pointer
	; for source array
	MOV R1, #50H ; Initialize memory pointer
	; for destination array
	; therefore R0 ---> Source
	;pointer
	; R1 ---> destination pointer
	UP: MOV A, @R0 ; Read number from source
	;array
	MOV @R1, A ; Write number to destination
	;array
	INC R0 ;Increment source memory
	;pointer by 1
	INC R1 ; Increment destination
	;memory pointer by 1
	
	DJNZ R3, UP ;Decrement byte counter by 1
	; Is it zero? No, jump to UP
	HERE: SJMP HERE
	END ; Stop
		4 marks for Program

Ans c.	**TCON: TIMER/COUNTER CONTROL REGISTER. BIT ADDRESSABLE.** TF1 | TR1 | TF0 | TR0 | IE1 | IT1 | IE0 | IT0 TF1 TCON. 7 Timer 1 overflow flag. Set by hardware when the Timer/Counter 1 overflows. Cleared by hardware as processor vectors to the interrupt service routine. TR1 TCON. 6 Timer 1 run control bit. Set/cleared by software to turn Timer/Counter 1 ON/OFF. TF0 TCON. 5 Timer 0 overflow flag. Set by hardware when the Timer/Counter 0 overflows. Cleared by hardware as processor vectors to the service routine. TR0 TCON. 4 Timer 0 run control bit. Set/cleared by software to turn Timer/Counter 0 ON/OFF. IE1 TCON. 3 External Interrupt 1 edge flag. Set by hardware when External Interrupt edge is detected. Cleared by hardware when interrupt is processed. IT1 TCON. 2 Interrupt 1 type control bit. Set/cleared by software to specify falling edge/low level triggered External Interrupt. IE0 TCON. 1 External Interrupt 0 edge flag. Set by hardware when External Interrupt edge detected. Cleared by hardware when interrupt is processed. IT0 TCON. 0 Interrupt 0 type control bit. Set/cleared by software to specify falling edge/low level triggered External Interrupt.	2 Marks for Format of timer control (TCON) register 2 Marks for Function of every bit

Ans. d.

Sr. No.	Parallel Data Transfer	Serial Data Transfer
1	All 8 bits data can be transferred at a time.	Only 1 bit data can be transferred at a time.
2	Total 9 lines are required between receiver and transmitter.	Only 2 lines are required between transmitter and receiver.
3	Data transfer rate is fast.	Data transfer rate is slow.
4	Used only if data transfer is required within small distance.	Used only if data transfer is required over a large distance.
5	Installation cost is more.	Installation cost is less.
6		

04 Marks
For Any four points

Ans. e.

P3 Bit	Function	Pin
P3.0	RxD – Serial Input Data Pin	10
P3.1	TxD –Serial Output Data Pin	11
P3.2	$\overline{\text{INT0}}$ – External Hardware interrupt pin 0	12
P3.3	$\overline{\text{INT1}}$ – External Hardware interrupt pin 1	13
P3.4	T0 – External Interrupt to Timer 0	14
P3.5	T1 – External Interrupt to Timer 1	15
P3.6	$\overline{\text{WR}}$ -- Write signal for data	16
P3.7	$\overline{\text{RD}}$ – Read signal for data	17

04 Marks

Ans f.

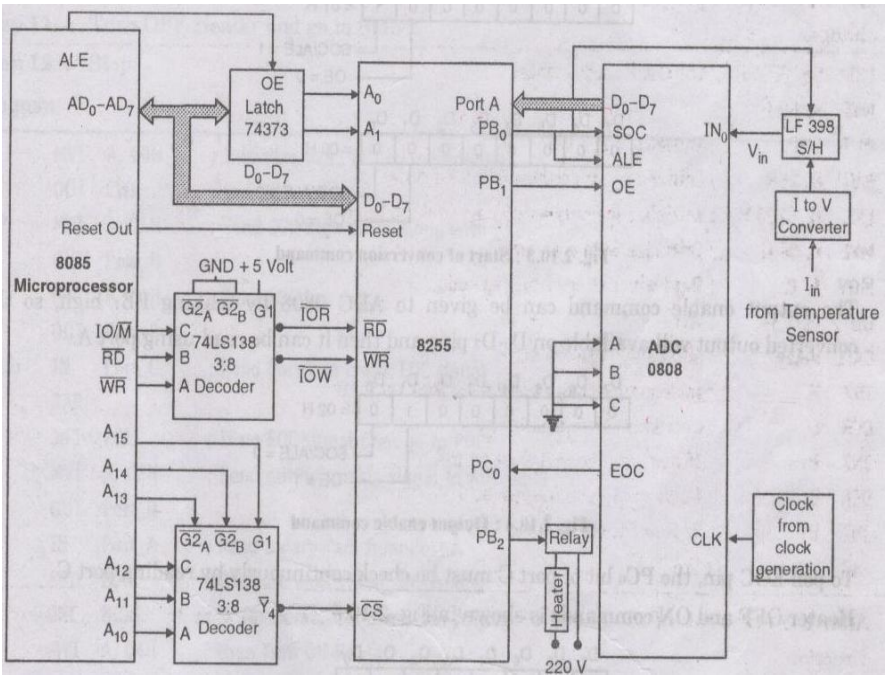
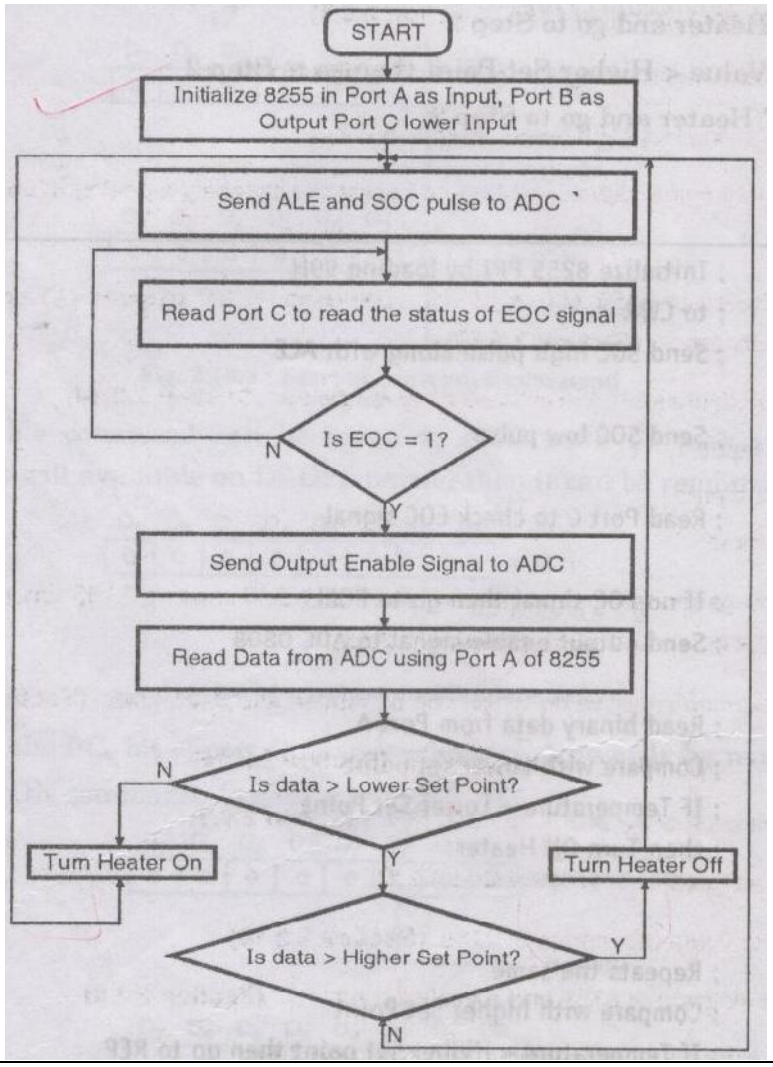


Fig: Microprocessor based temperature control

1 Marks for Interfacing Diagram

Flow chart:



3 Marks for Program OR Flow chart with explanation

The temperature is one form of energy which must be converted into voltage form and then to its equivalent digital form, so that the microprocessor can understand and take the action on the desired temperature.

Hence, we can use temperature sensor to sense the temperature. Here, we will See how to control room temperature between 25^oC i.e. lower set point and 30^0C i.e. higher set point.

Assume sensor is giving output 1 volt for 0^0C and 5 volt for 50^0C. Afte feeding this voltages to ADC, suppose ADC is giving 00H for 0^0C and FF H for 50^oC.

Then we can find out the voltages for 25^oC and 30^oC as given below, So,
$50^oC \longrightarrow$ 5 Volt then for $25^oC \longrightarrow$? And $30^0C \longrightarrow$?

Voltage for 25^oC (Lower Set Point) = (25X 5) /50 = 2.5 Volt

Voltage for 30^oC (Higher set Point) = (30X 5) /50= 3 Volt , then

5V $\longrightarrow$ FFH $\longrightarrow$? 255 then for 2.5 V $\longrightarrow$? And 3V $\longrightarrow$

Binary (hex) value for 25^oC (Lower set point)=
$(2.5 \text{ X } 255)/5 = (128)_{10} = 80H$

Binary (hex) value for 30^oC (Higher set point)=
$(3 \text{ X } 255)/5 = (153)_{10} = 99H$

Now, when temperature is lower than 25^0C (80H in binary), then heate should be ON and When temperature is greater than 30^0C (99H in binary) , then heater should be OFF.

The heater can be controlled through relay. The complete interfacing o 8085, 8255 and ADC with temperature sensor is shown in Fig. 3.4.1
The port A of 8255 is used to read data from ADC; Port B is used to control ADC and heater.

Port C is used for handshaking as shown in fig
In additional to control ADC, 8255 Port B can be used control heater to turn ON/OFF hence PB_2 is used to control relay which makes heater O or OFF.

Sample and hold must be used to ensure correct temperature reading, means this circuit samples the instantaneous value from sensor and maintains it at constant level.

In this application LF 398 S/H is used and is controlled by PB_0.
The falling edge of the pulse on PB_0 starts conversion and sample pulse can be used by S/H circuit to hold the output from I to V converter.

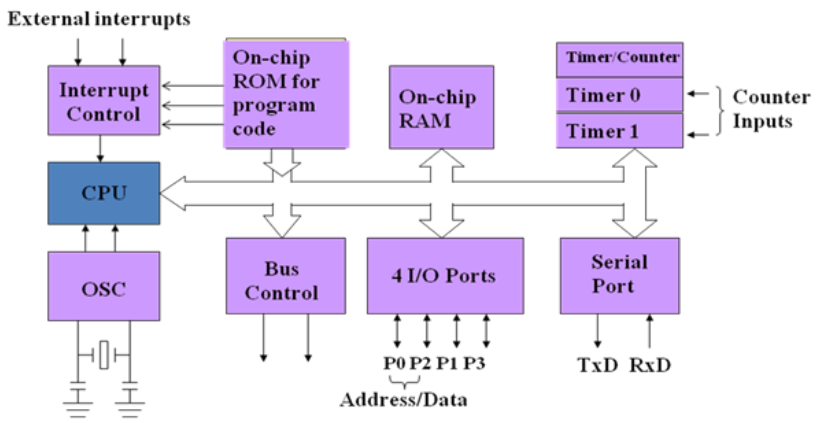
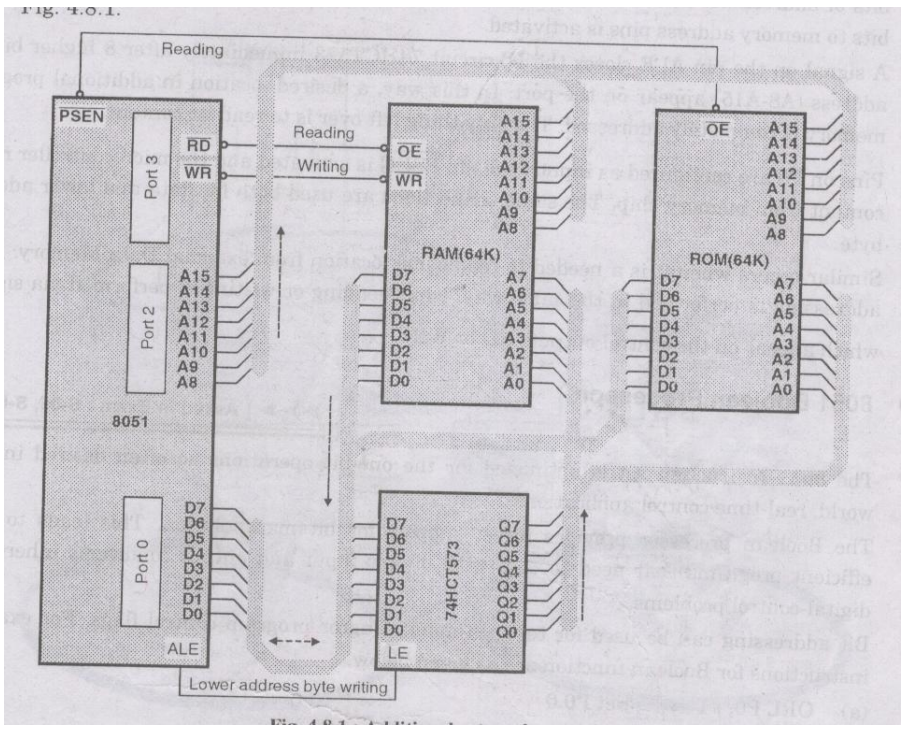
Program:

```
        MVI   A, 99H    ; Initialize 8255 PPI by loading 99H
        OUT  CWR        ; to CWR
REP:    MVI A, 01H      ; Send SOC high pulse along with ALE
        OUT PORT_B
        MVI A,00H       ; Send SOC low pulse
OUT     PORT_B
POLL:   IN PORT_C       ; Read Port C to check EOC signal
        RAR
        JNC POLL        ; If no EOC signal then go to poll
        MVI A,02H       ; Send output enable signal to ADC 0808
        OUT PORT _B     ;


        IN PORT_A       ; Read binary data from port A
        CPI 80H         ; compare with lower set point
        JNC NEXT        ; if temperature < lower set point
        MVI A,04H       ; then turn  on heater
        OUT PORT_B
        CALL Delay
        JMP REP         ; Repeats the same
NEXT:   CPI 99H         ; compare with higher set point
        JC REP          ; if the temperature < higher set point then
                        ;go to REP
        MVI A, 00H      ; Turn OFF heater
        OUT PORT_B
        CALL DELAY
        JMP REP         ; continue the process for automatic
                        temperature control
```

Delay sub routine using 8 bit counter for all application

```
PUSH  PSW
MVI  C,FF H
UP: DCR C
JNZ UP
POP PSW
RET
```

Q 4. a	**Attempt any THREE of the following:**	**12 Marks**
Ans. i.	 Fig: Block diagram of microcontroller 8051	4 marks for labeled diagram
Ans. ii	In case memory (RAM or ROM) built in the microcontroller is not sufficient, it is possible to add two external memory chips with capacity of 64Kb each. P2 and P3 I/O ports are used for their addressing and data transmission as shown in fig.  Fig: Additional external memories From the user's point of view, everything works quite simply when properly connected because most operations are performed by the microcontroller itself.	

	The 8051 microcontroller has two pins for data read $\overline{RD}$(P3.7) and $\overline{PSEN}$. The first one is used for reading data from external data memory (RAM), while the other is used for reading data from external program memory (ROM). Both pins are active low. A typical example of memory expansion by adding RAM and ROM chips (Hardward architecture), is shown in figure above. Even though additional memory is rarely used with the latest versions of the microcontrollers, we will describe in short what happens when memory chips are connected according to the previous schematic. The whole process described below is performed automatically. When the program during execution encounters an instruction which resides in external memory (ROM), the microcontroller will activate its control output ALE and set the first 8 bits of address (A0-A7) on P0. IC circuit 74HCT573 passes the first 8 bits to memory address pins. A signal on the ALE pin latches the IC circuit 74HCT573 and immediately afterwards 8 higher bits of address (A8-A15) appear on the port. In this way, a desired location of additional program memory is addressed. It is left over to read its content. Port P0 pins are configured as inputs, the PSEN pin is activated and the microcontroller reads from memory chip. Similar occurs when it is necessary to read location from external RAM. Addressing is performed in the same way, while read and write are performed via signals appearing on the control outputs $\overline{RD}$ or $\overline{WR}$.	
Ans. iii.	**Program:** CLR PSW.3 ; Select Bank 0 CLR PSW.3 MOV R1, 0AH ; Initialize byte counter MOV DPTR, # 3000H ; Initialize memory pointer DEC R1 ; Decrement byte counter by 1 MOV X A, @DPTR ; Load number in accumulator MOV 40 H,A ; Store number in memory ; location UP : INC DPTR ; Increment memory pointer by 1 MOVXA, @DTPR ; Read next number	4 Marks for program

```
        CJNE A, 40 H, DN        ; if number≠ next
                                  number, then go to NEXT
DN :    JC NEXT                 ; If next number > number then
                                ; go to NEXT
        MOV 40H, A              ; Else replace NEXT  number
                                ;with   number
NEXT : DJNZ R1, UP              ; Decrement byte counter by 1, if
                                ; byte counter≠ 0 then go to UP
        INC DPTR                ; Increment memory pointer by 1
        MOV A, 40H
        MOVX@ DPTR, A           ; Store result t external
                                ; memory location
LOOP : AJMP LOOP                ; Stop
```

Ans. iv

Reset – power-up reset

- **Two interrupts are set aside for the timers: one for timer 0 and one for timer 1**
- **Two interrupts are set aside for hardware external interrupts**
  P3.2 and P3.3 are for the external hardware interrupts INT0 (or EX1), and INT1 (or EX2)
- **Serial communication has a single interrupt that belongs to both receive and Transfer**

2 Marks for Types of interrupts

Interrupt vector table

Interrupt	ROM Location (hex)	Pin
Reset	0000	9
External HW (INT0)	0003	P3.2 (12)
Timer 0 (TF0)	000B	
External HW (INT1)	0013	P3.3 (13)
Timer 1 (TF1)	001B	
Serial COM (RI and TI)	0023	

<u>Format of IE special function register :</u>

IE: INTERRUPT ENABLE REGISTER. BIT ADDRESSABLE.

If the bit is 0, the corresponding interrupt is disabled. If the bit is 1, the corresponding interrupt is enabled.

EA	—	ET2	ES	ET1	EX1	ET0	EX0

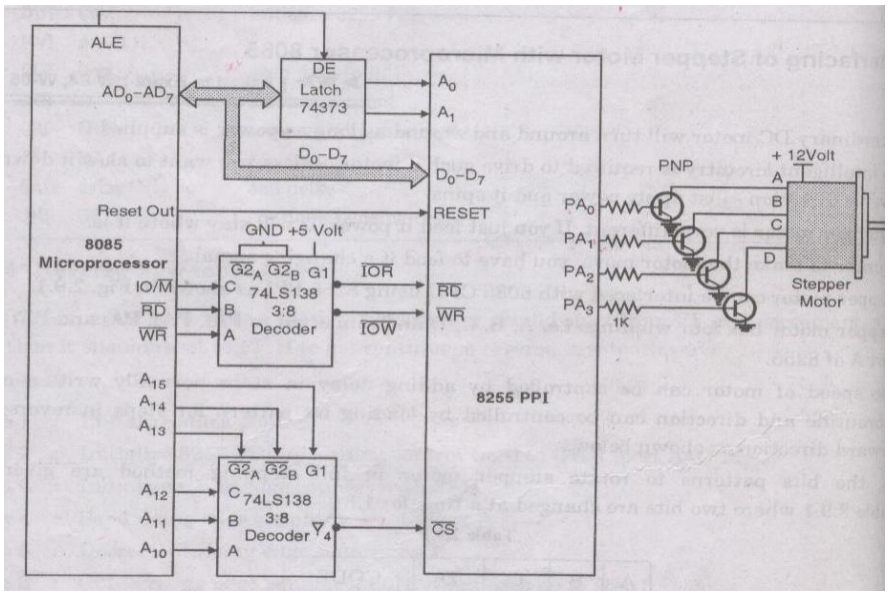
EA	IE.7	Disables all interrupts. If EA = 0, no interrupt will be acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
—	IE.6	Not implemented, reserved for future use.*
ET2	IE.5	Enable or disable the Timer 2 overflow or capture interrupt (8052 only).
ES	IE.4	Enable or disable the serial port interrupt.
ET1	IE.3	Enable or disable the Timer 1 overflow interrupt.
EX1	IE.2	Enable or disable External Interrupt 1.
ET0	IE.1	Enable or disable the Timer 0 overflow interrupt.
EX0	IE.0	Enable or disable External Interrupt 0.

*User software should not write 1s to reserved bits. These bits may be used in future MCS-51 products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1.

2 Marks for format

b.	**Attempt any <u>ONE</u> of the following**	**6 Marks**

Ans i.

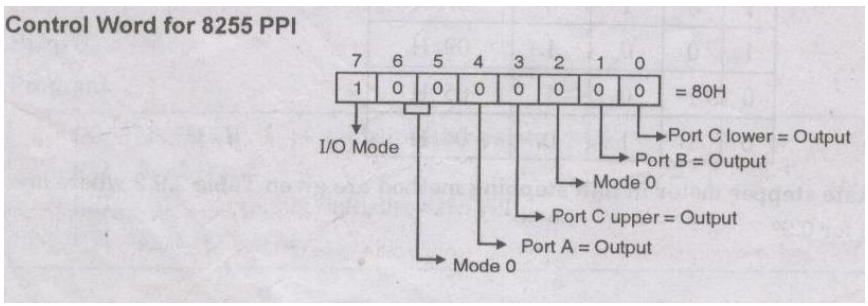


3 Marks for Interfacing diagram

Fig : Interfacing Stepper motor to IC 8085 using 8255

Stepper motor has four windings i.e. A, B, C,D and connected to PA0, PA1, PA2, PA3 of a port of 8255.
The bits pattern to rotate stepper motor in 1.8 degree ie. in full stepping method is as follows:

A	**B**	**C**	**D**	**CODE**
1	0	1	0	0AH
1	0	0	1	09H
0	1	0	1	05H
0	1	1	0	06H

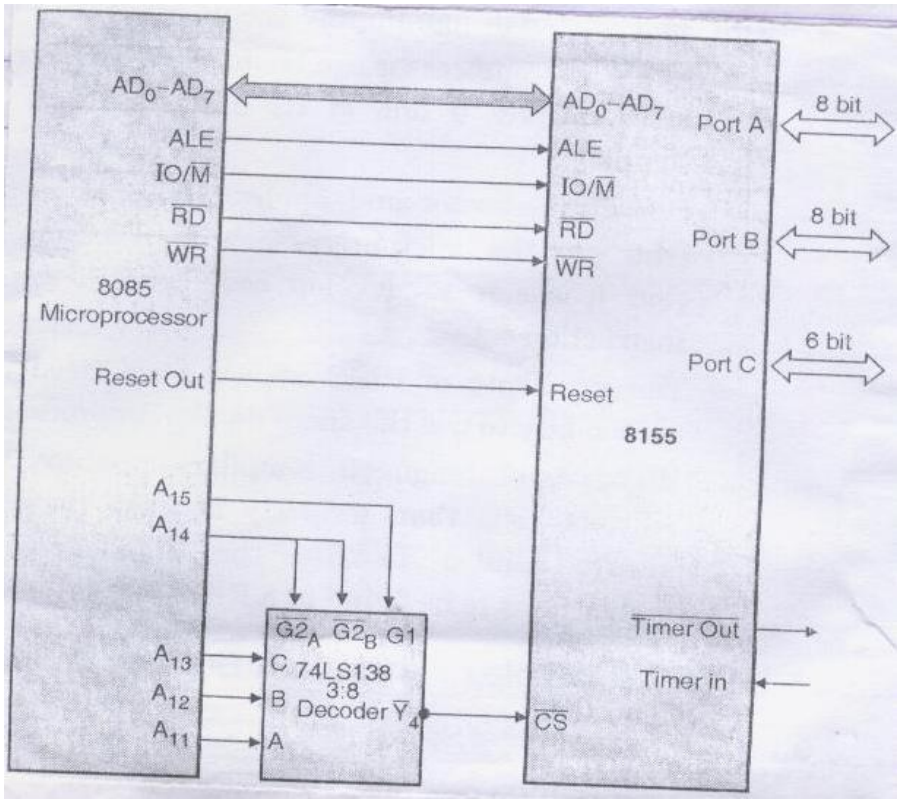


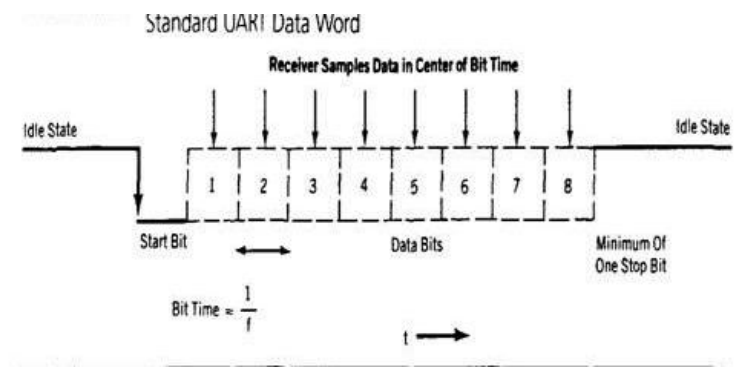
Program:

03 Marks for Program

```
LXI SP, FFE0 H      ; Initialize stack pointer
MVI A, 80H
OUT CWR             ; Initalize 8255 PPI
UP : LXI H, C200 H; Initalize memory pointer for look up table
MVI C, 04 H         ;Initalize byte counter
UP 1: mov A,M       ; Read bits pattern i.e step code
OUT PORT_A          ; write to port A
CALL DELAY          ; add delay between steps
INX H               ; increment memory pointer for look up table
DCR C               ; DECREMENT BYTE COUNTER BY 1
```

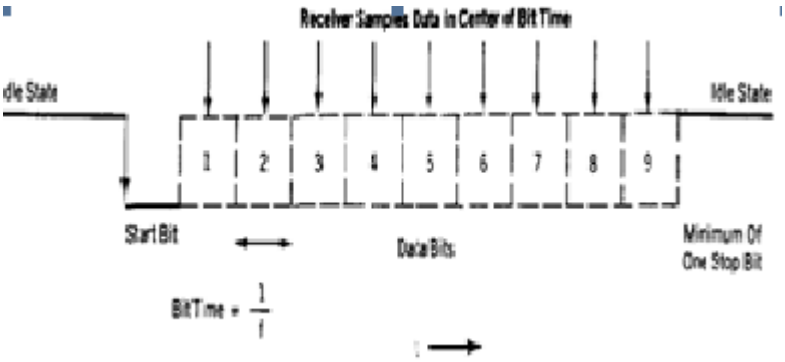
	JNZ UP1 ; if byte counter ≠ 0 then go to UP1 JMP UP ; Continous rotation	
Ans ii.	**<u>Assembly language programming tools:</u>** **1) Editor** **2) Assembler** **3) Linker** **4) Object-Hex converter** **1) Editor:** • An editor is a program which helps you to construct your assembly language program in right format so that the assembler will translate it correctly to machine language. • So, you can type your program using editor. • This form of your program is called as source program and extension of program must be .asm or .src depending on which assembler is used. • The DOS based editor such as EDIT , Wordstar, and Norton Editor etc. can be used to type your program. **2) Assembler:** • An assembler is programs that translate assembly language program to the correct binary code for each instruction i.e. machine code and generate the file called as Object file with extension .obj and list file with extension .lst extension. • Some examples of assembler are ASEM-51, Keil's A51, AX 51 and C51, Intel PL/M-51 etc. **3) Linker:** • A linker is a program, which combines, if requested , more than one separately assembled object files into one executable program, such as two or more programs and also generate .abs file and initializes it with special instructions to facilitate its subsequent loading the execution. • Some examples of linker are ASEM-51 BL51, Keil u Vision Debugger, LX 51 Enhanced Linker etc. **4) Object-Hex converter:** • The Object – HEX converter creates Intel HEX files from	2 Marks for Listing Assembly language programming tools 4 Marks for Explanation

	absolute object modules i.e. .abs file. • Intel HEX files are ASCII files that contain a hexadecimal representation of your program. • They may be easily loaded into a device programmer for writing EPROMS or other memory devices. Example of object to HEX converter is Keil's OH51.	
Q5	**Attempt any <u>FOUR</u> of the following**	16 Marks
Ans a.	 Fig: Interfacing of IC 8085 with IC 8155 The complete interfacing diagram of IC 8085 with IC 8155 is as shown above. (1) The 8155 has inbuilt de-multiplexing circuitry to de-multiplexed address/data bus, i.e., ADO-AD7 using ALE signal. (2) Hence, external circuitry for de-multiplexing of AD bus is not required; the ADO-AD7 lines of 8085 can be directly connected to AD0-AD7 lines of 8155. (3) The control signals RD, WR & IO/M of 8085can also be connected directly to the corresponding pins of 8155, so no need to generated control signal like IOW, IOR, MEMR & MEMW using decoder. (4) The RESET OUT of 8085 can be connected directly to RESET pin of 8155. (5) The 8155 requires a CS signal to select chip during I/O or	2 marks for Interfacing diagram 2 marks for Explanation

	memory related operations. (6) Hence, it can be generated using address line A11-A15 & 3:8 decoder.	
Ans b.	8051 has 4 modes of data transmission. The modes are selected by setting bits SM0 and SM1 in SCON register. Baud rates are fixed for Modes0 and variable for Mode 1,2 and 3. Setting bits SMO and SM1 in SCON to b configures SBUF to receive or transmit eight data bits using pin RXD for both functions. Pin TXD is connected to internal shift frequency pulse source to supply shift pulses to external circuits. The shift frequency or baud rate is fixed at / Of the oscillator frequency, the same rate used by the timers when in the timer mode. The TXD shift clock is a square wave that is low for machine cycle state S3-S4- S5 and high for S6-S1- S2 When transmitting data is shifted out of RDX the data changes on the falling edge of S6P , or one clock pulse after the rising edge of the output TXD shift clock. The user must design the circuit that receives this data to receive the data reliably based on this timings. **<u>Serial data mode 0</u>** 1. It is also called as shift register mode. 2. Baud rate is 1/12th of oscillator frequency i.e. the same rate used by the times 3. TXD shift clock is square wave, low for machine cycles S3-S4-S5 and high for S6-S1-S2. 4. Data is transmitted out of SBUF on falling edge of S6P2 out of RXD. 5. Data is received into SBUF through RXD pin during S5P2. This mode is used for high speed serial data communication  Transmitted data is send as a start bit, eight data bits (at least LSB first) and then stop bit. Interrupt flag T1 is set once all ten bits have been sent. Each bit interval is the inverse of the baud rate frequency, and each bits is maintained high or low over that interval. Received data is obtained in the same order. Reception is triggered by the falling edge of the start bit and continues if the stop bit is true (0 level) halfway through the start bit	4 marks for Explanation of four operating modes

interval. This is an anti noise measure; if the reception circuit is triggered by noise on the transmission line, the check for a low after half a bit interval should limit false data reception. Data bits are shifted into the receiver at the programmed baud rates and the data word will be loaded to SBUF if the following conditions are true: RI must be 0 and mode bit SM2 is 0 or the stop bit is 1 (the normal state of stop bits). RI set to 0 implies that the program has read the previous data byte and is ready to receive the next; a normal stop bit will then complete the transfer of data to SBUF regardless of the state of SM2. SM2 set to 0 enables the reception of a byte with any stop bit state, a condition that is of limited use in this mode, but very useful in modes 2 and 3 . SM2 set to 1 forces reception of only "good' stops bits, an anti noise safeguard . Of the original ten bits, the start bit is discarded the eight data bits go the stop bit is saved in bit RB8 of SCON . RI is to set1, indicationg a new data byte has been received.
If RI is found to be set at the end of the reception, indicating that the previously received data byte has not been read by the program, or if the other conditions listed are not true, the new data will not be loaded and will be lost.

<u>Serial Data Mode 2: Multimode Mode:-</u>
Mode 2 is similar to mode 1 except 11 bits are transmitted : a start bit, nine data bits, and a stop bit, as shown. The ninth data bit is copied from bit TB8 in SCON during transmits and stored in bit RB8 of SCON when data is received . Both the start and stop bits are discarded.



The conditions for settings R1 for mode mode2 are similar to mode 1: R1 must be 0 before the last bit is received, and SM2 must be 0 or the ninth data bit must be at 1. Setting R1 based on the state of SM2 in the receiving 8051 and the state of the bit 9 in the transmitted message makes multiprocessing possible by enabling some recievers to the interrupted by certain message,while other recievers ignore those messages. Only those 8051 that have SM2 set to 0 will be interrupted by received data that has the ninth data bit set to 0; those with SM2 set to 1 will not be interrupted by messages with data bit 9 at 0. All recievers will be interrupted by data words that have the ninth data bit set to 1; the state of SM2 will not block reception of such messages.

	<u>Serial Data mode 3</u> Mode 3 is identical to mode 2 except that the baud rate is setermined exactly as in the mode 1; using timer 1 to generate communication frequencies.	
Ans c.	**TMOD: TIMER/COUNTER MODE CONTROL REGISTER. NOT BIT ADDRESSABLE.** GATE | C/$\overline{T}$ | M1 | M0 | GATE | C/$\overline{T}$ | M1 | M0 TIMER 1 — TIMER 0 GATE When TRx (in TCON) is set and GATE = 1, TIMER/COUNTERx will run only while INTx pin is high (hardware control). When GATE = 0, TIMER/COUNTERx will run only while TRx = 1 (software control). C/$\overline{T}$ Timer or Counter selector. Cleared for Timer operation (input from internal system clock). Set for Counter operation (input from Tx input pin). M1 Mode selector bit. (NOTE 1) M0 Mode selector bit. (NOTE 1) **NOTE 1:** M1 M0 Operating Mode 0 0 0 13-bit Timer (MCS-48 compatible) 0 1 1 16-bit Timer/Counter 1 0 2 8-bit Auto-Reload Timer/Counter 1 1 3 (Timer 0) TL0 is an 8-bit Timer/Counter controlled by the standard Timer 0 control bits, TH0 is an 8-bit Timer and is controlled by Timer 1 control bits. 1 1 3 (Timer 1) Timer/Counter 1 stopped.	2 Marks for Format 2 marks for function of each bit.
Ans d.	**DPTR:-** The DPTR register is made up of two registers named as DPH & DPL which are used to access any memory address that may be internal & external code access & external data access. The DPTR is under the program control & can also be specified as 16-bit pointer as DPTR or by individual 8- bits as DPH & DPL. DPTR does have a single address but the DPH is assigned the address as 82 H. **PC:-** The program counter (PC) IS A 16-bit register. It is used to hold address of a byte in memory. Program instruction bytes are fetched from locations in memory that are addressed by PC. Program ROM may be on chip at addresses OOOOH to OFFF H. external to the chip for addresses that exceeds OFFF h or totally external for all addresses from 0000H to external for all addresses from OOOOH to FFFF H. The PC is incremented automatically after every instruction byte is fetched. The PC is the only register that does not have any address. **Stack Pointer:-** The 8-bit stack pointer (SP) register is used to hold an internal RAM address that is called the top of stack. The address held in the SP register is the location in internal RAM where the last byte of data was stored by a stack operation. **PSW register:-** The program status word is used to store a number of important bits that are set & cleared by 8051 instructions. The	1 Mark for function of each

	PSW SFR contains the carry flag. The auxiliary carry flag, the overflow flag, & the parity flag. Two register bank select bits, & user-definable status flag. Additionally, the PSW register contains the register bank select flags which are used to select which of the "R" register banks are currently selected.	
Ans e.	DB:- (Data Byte) Syntax: Label: DB BYTE Where byte is an 8-bit number represented in either binary, Hex, decimal or ASCII form. There should be at least one space between label & DB. The colon (:) must present after label. This directive can be used at the beginning of program. The label will be used in program instead of actual byte. There should be at least one space between DB & a byte. ORG:- Origin It is used to indicate the beginning of address. Syntax: ORG Address The address can be given in either hex or decimal there should be a space of at least one character between ORG & address fields. Some assemblers use ORG should not begin in label field. EQU: Equate It is used to define constant without occupying a memory location. Syntax: Name EQU Constant By means of this directive, a numeric value is replaced by a symbol. For e.g. MAXIMUM EQU 99 After this directive every appearance of the label "MAXIMUM" in the program, the assembler will interpret as number 99 (MAXIMUM=99). DATA: Syntax:- Name Data Data Address By means of this directive an address with internal RAM is designated as a symbol (address must be in the range of 0-255). In other words, any selected register may change its name or be assigned a new one. For e.g. TEMP 12 DATA 32:- register at address 32 is named as "TEMP 12".	1 Mark for function of each directive

Ans f.	Four instruction related with external memory:- 1) MOVX A @ DPTR 2) MOVX @ DPTR, A 3) MOVX @ R0, A 4) MOVX A, @ R0.	01 mark for each instruction.
Q. 6	**Attempt any <u>FOUR</u> of the following**	**16 Marks**
Ans a.	**Crystal frequency= 12 MHz** I/P clock = $\frac{12 \times 10^6}{12}$ = 1000000 Tin = 1µ sec For 1 khz square wave F_{out} = 1 KHz T_{out} = 1/ 1X 10^3 T_{out} = 1000µ sec Consider half of it = T_{out} = 500µ sec N = T_{out} / Tin = 500/1 = 500 65536-500= $(65036)_{10}$ = $(FEOC)_{16}$ **Program:-** MOV TMOD, # 01H ; Set timer 0 in Mode 1, i.e., 16 bit; ; timer L_2 : MOV TLO, # OCH ; Load TL register with LSB of count MOV THO,# FEH ; load TH register with MSB of count SETB TRO ; start timer 0 L_1 JNB TFO, POLL L_1 ; poll till timer roll over CLR TRO ; stop timer 0 CPL P1.5 ; complement port 1.5 line to get ; high or low CLR TFO ; clear timer flag 0 SJMP L_2 ; re-load timer with count as ; mode 1 is not auto-re-load	01 mark for calculation of count 03 Marks for program
Ans b	• The 8051 instruction set is optimized for the one bit operations so often desired in real world, real time control applications. • The Boolean processor provides direct support for bit manipulation. This leads to more efficient programs that needs to deal with binary input and output conditions inherent in digital control problems. • Bit addressing can be used to test pin monitoring or program control flags. For examples, instructions for Boolean function are as given below. (a) ORL P0, # 1 ; Set P0.0 (b) XRL P0, # 1 ; Toggle P0.0	04 Marks for explanation

Ans c

Program for sum of series (10 numbers)

```
        CLR PSW.3        ; Select register Bank 0
        CLR PSW.4        ;
        MOV Ro, #OAH     ; Initialize byte counter
        MOV R1,#40H      ; Initialize memory pointer
        MOV A, # 00H     ; Clear Accumulator
UP:     ADD A @R1        ; Add accumulator with number
                           from array
        INC R1           ; Increment memory pointer
        DJNZ R0, UP      ; Decrement byte counter,
                         ; if byte counter ≠ 0
                         ; Then go to UP
        MOV@ R1,A        ; Store result in internal memory
LOOP:   AJMP Loop        ; stop
```

04 Marks for program

Ans d

Sr. No	RISC(Reduced Instruction Set Computer)	CISC(Complex Instruction Set Computer)
1	Emphasis on software	Emphasis on hardware
2	Single clock reduced instruction only	Includes multi clock complex instruction
3	Register to Register: ‘’Load” and “Store” are independent instructions	Memory to memory:” Load and “Store” incorporated in instructions.
4	Low cycles per second, large code sizes	Small code sizes, high cycles per second
5	Spends more transistors on memory registers	Transistors used for strong complex instructions.

04 marks for any four points

Ans e

Handshake mode of data transfer

(1) In this mode, the data transfer takes place between microprocessor based system with 8155 and peripheral using control signals called handshake signals.
(2) The port A and port B can be configured in handshake mode as an input or output port where each port uses port C bits as handshake signals.
(3) In ALT3 only port A can be configured in handshake input or output mode in which port A uses PC0, PC1 and PC2 for handshake signals.
(4) In ALT4, both ports A and port B can be configured in handshake input or output modes in which port A uses PC0, PC1, PC2 and port B uses PC3, PC4, PC5 for handshaking signals.

04 Marks for explanation

Ans. f	The stack refers to an area of internal RAM that is used in conjunction with certain op codes to store and retrieve data quickly. The 8 bit stack pointer (SP) register holds an internal RAM address that is called top of stack. The address held in the SP register is the location in internal RAM where the last byte of data was stored by a stack operation. If you push a value on to the stack, the value will be written to address of SP+1 .that is to say if SP holds the value of 07H, a push instruction will push the value on to the stack at address 08H. This SFR is modified by all instructions which modify the stack, such as PUSH, POP, CALL, RET, RETI and whenever interrupts are provoked by the microcontroller. A value of stack pointer ensures that the stack pointer will point to valid Ram and permits stack availability. By starting each subprogram, the value in the stack pointer is incremented by 1. In the same manner, by ending subprogram, this value is decremented by 1.	01Mark for Definition of stack 3 mark for Operation of stack