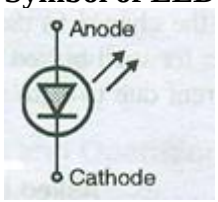
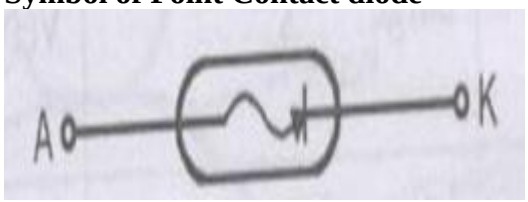
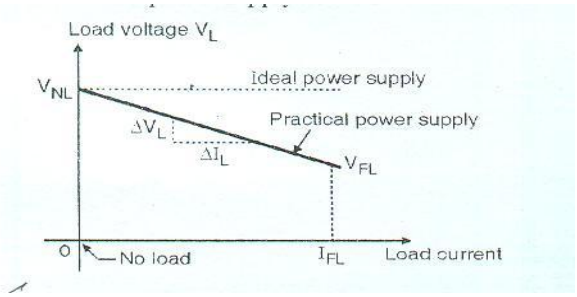
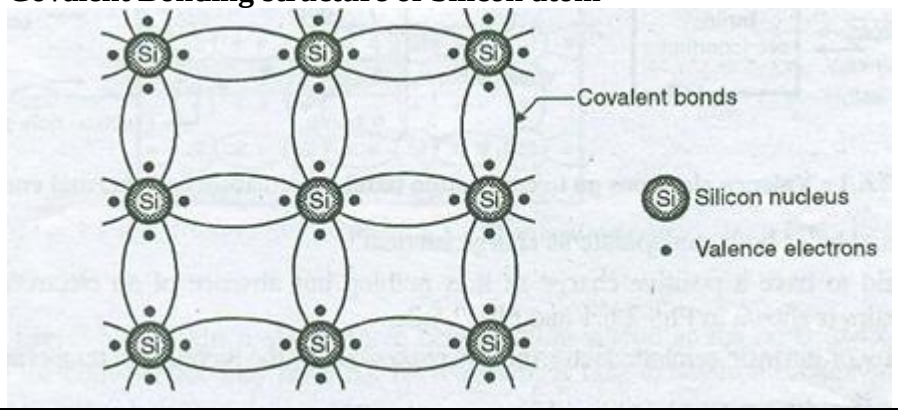
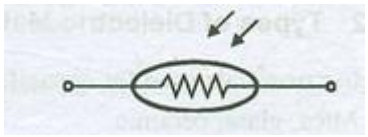
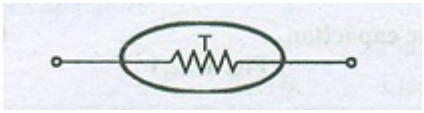
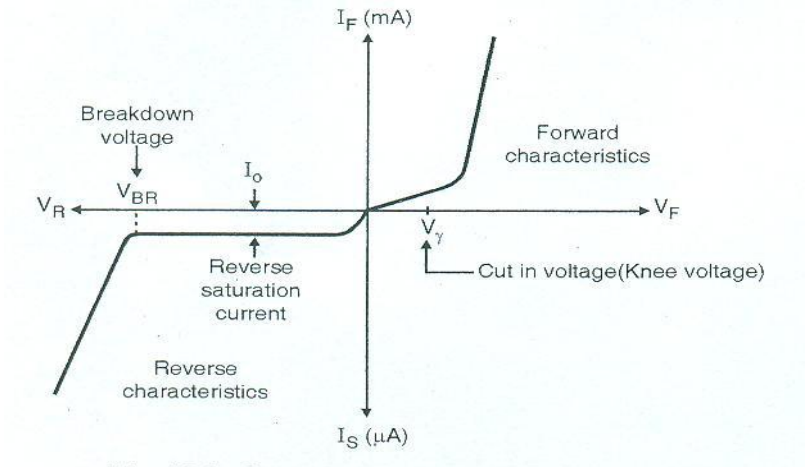
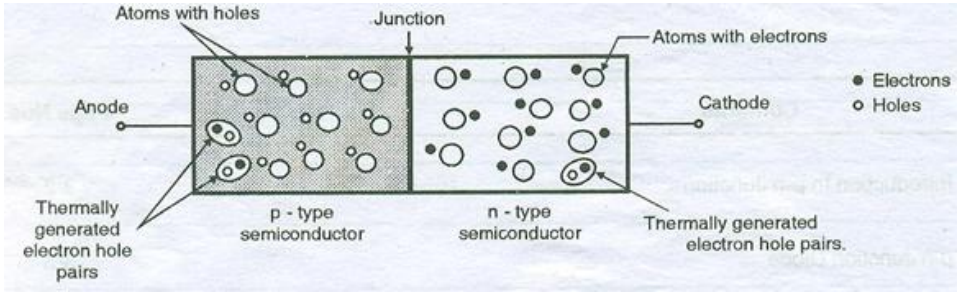
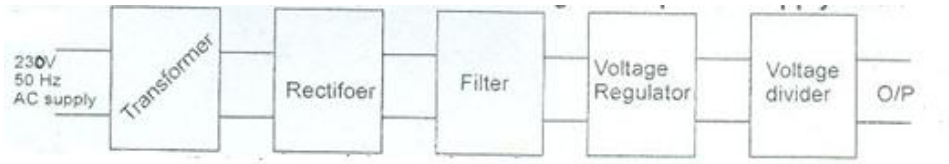
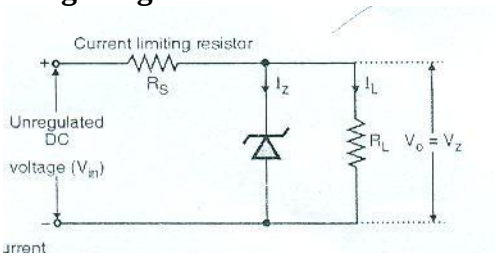
Q1 .	**Attempt any Ten**	**20 Marks**
Ans a	**Symbol** 	1
	Unit of Inductance Henry(H)	1
Ans b	**Doping** The process of adding impurities to the Intrinsic semiconductor is called Doping.	1
	Need To increase conductivity of intrinsic semiconductor.	1
Ans c	**Symbol of LED** 	1
	Applications of LED 1. In the optocouplers 2. In the infrared remote controls 3. As indicators in various electronic circuits	
	Symbol of Point Contact diode 	1
	Applications of Point Contact diode 1. AM detector in radio receiver 2. Video detector in T.V 3. Microwave frequency Mixer 4. Pulse Circuits	
Ans d	**Filter:** Filter are the electronic circuit used with rectifiers to get pure DC voltage. The rectifiers give pulsating dc voltage. Filters are connected at the output of rectifier to get pure ripple free dc voltage.	1
	Types of filter: 1.Shunt Capacitor filter 2.Series Inductor filter 3.LC / choke input filter 4. CLC or πfilter	1

Ans e	**Load Regulation** - It is defined as the change in output voltage when the load current is changed from zero (no load) to maximum (full load) value. It is calculated as % Load Regulation = $\frac{V_{NL} - V_{FL}}{V_{FL}} \times 100$ | Vin Constant Where V_{NL} = No load voltage ($I_L = 0$) V_{FL} = Full load voltage ($I_L = I_L$ Max) Diagram of load regulation  **Line Regulation** : It is defined as the change in regulated load voltage for a specified range of line voltage with load R_L constant (I_L constant) Line Regulation = $V_{HL} - V_{LL}$ V_{HL} = Load voltage with high line voltage V_{LL} = Load voltage with low line voltage	1 1
Ans f	**α** - It is defined as the ratio of collector current Ic to the emitter current I_E $\alpha_{dc} = \frac{Ic}{I_E}$ or $\alpha_{ac} = \frac{\Delta I_C}{\Delta I_E}$ **β** – It is defined as the ratio of collector current I_C to the Base Current I_B $\beta_{dc} = \frac{Ic}{I_B}$ or $\beta_{ac} = \frac{\Delta I_C}{\Delta I_B}$	1 1
Ans g	**Types of Coupling** 1. RC Coupling 2. Transformer Coupling 3. Direct Coupling	2
Ans h	**Applications of JFET (any one)** 1. Used as amplifier 2. Used as switch 3. Used as a voltage variable resistor(VVR) 4. Used in digital circuits **Applications of MOSFET (any one)** 1. Used as Amplifier 2. It can be used as switch	1 1

Ans i	**Advantages of IC (any two)** 1. Small size and weight 2. Low cost 3. High Reliability 4. Low power consumption 5. High operating speed **Disadvantages of IC (any two)** 1. Power dissipation is limited 2. Not possible to fabricate capacitor of values higher than 30 pF 3. Not possible to fabricate resistor of values higher than 100KΩ 4. Not possible to directly fabricate Inductor 5. Initial cost to be incurred is high	1 1
Ans j	**Covalent Bonding structure of Silicon atom**  	2
Ans k	**Forbidden Energy Gap(** E_G**) :** It is the energy gap that separates the conduction and valence band in the energy band diagram. No electrons can exist in the forbidden energy gap. **For** E_G Wood > 5eV E_G Copper = 0eV	1 1
Ans l	**Ripple Factor :** it is defined as the ratio of RMS value of the AC component of output to the DC or average value of the output . $r = [V^2_{L\ rms} - V^2_{Ldc}]^{1/2} / V_{Ldc}$ **PIV :** Peak Inverse Voltage It is the maximum reverse voltage that a diode can withstand in the reverse direction without breaking down.	1 1
Ans m	**Different types of Capacitor** **Fixed Capacitor** 1. Paper 2. Mica 3. Ceramic 4. Glass 5. Plastic Film 6. Electrolytic **Variable Capacitor** 1. Tuning (Ganged) Capacitor **2.** Trimming Capacitor	 1 1
Ans n	**Intrinsic Semiconductor -** Intrinsic means 'pure', so intrinsic semiconductors are the semiconductors in the purest form. **Extrinsic Semiconductor -** Extrinsic means 'Impure' . These are obtained by adding impurities to the Intrinsic semiconductor.	1 1

Q2	Attempt ANY FOUR	16
Ans a	**Symbol of LDR**  **Applications (any two)** 1.Camera light meters 2.Security Alarms 3.Smoke detectors 4.Light sensitive relays **Symbol of Thermistor**  **Applications (any two)** 1.Used in Bio-medical Instrumentation 2.Automatic temperature controller 3.Temperature sensor 4. Biasing and compensating circuits of transistor	**1** 1 1 1
Ans b	**Difference between Intrinsic & Extrinsic semiconductor(any 4 points)** **Sr.No. | Intrinsic Semiconductor | Extrinsic semiconductor** 1. | Pure form | Impure form 2. | Number of holes is equal to the no. of electrons | In N type number of electrons is more and in P type number of holes is more 3. | Electrons and holes are thermally generated | Electrons and holes are generated due to doping 4. | Total current flow is due to holes and electrons | Total current flow is due to majority carriers holes in P-Type and electrons in N -type 5. | Conductivity is poor | Conductivity is high 6. | Fermi level is at the center of forbidden energy gap | Fermi level is either near the conduction band or valence band	4
Ans : c	**V-I Characteristics of Diode**  **Knee Voltage**: The voltage at which the forward current of diode starts increasing rapidly is known as Knee voltage. **Reverse Breakdown voltage**: If the reverse bias voltage is increased, to a large value then reverse saturation current through PN junction increases abruptly. The voltage at which this action occurs is known as reverse breakdown voltage	2 1 1

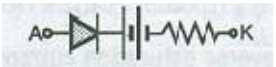
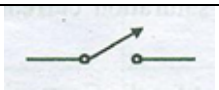
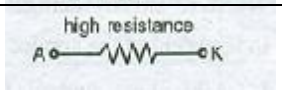
Ans : d	**Construction of Zener Diode**  **Operation in Reverse Bias** 1. Reverse bias means connecting the anode of diode to the negative terminal of the battery & cathode of the diode to the positive terminal of the battery. 2. As we increase the reverse voltage, initially a small reverse saturation current will flow due to minority carriers. 3. At certain value of reverse voltage, the reverse current will increase suddenly and sharply, this voltage is break down voltage. 4. This break down voltage is called zener break down voltage.	2 2
Ans e	**Block Diagram of Regulated Power Supply**  There are four basic blocks of a d.c. regulated power supply. They are 1) Step down transformer 2) Rectifier 3) Filter 4) Voltage Regulator 5)Voltage divider **Functions** of each block are as follows : **Step down transformer** : Reduces 230 volts 50Hz ac voltage to required ac voltage level. **Rectifier** : Rectifier converts ac voltage to dc voltage. Typically bridge full wave rectifier is widely used. **Filter** : Filter is a circuit used to remove fluctuations (ripple or ac) present in dc output. **Voltage Regulator** : Voltage regulator is a circuit which provides constant dc output voltage irrespective of changes in load current or changes in input voltage. **Voltage divider** is a passive circuit used for providing different dc voltages required by different electronic circuits	2 2

Ans f	**Zener Diode as Voltage Regulator**  - A Voltage Regulator circuit provides constant O/P voltage inspite of changes in its i/p voltage or load current. - The Series Resistance Rs is connected to limit the total current drawn from the unregulated power supply. - Zener diode is a shunt type voltage regulator because the zener diode is connected in parallel with the load resistance and is connected in reverse biased condition. - If Vin is higher than Vz and if the Iz is between Izmin & Izmax then the voltage across zener will remain constant equal to Vz irrespective of any changes in Vin & IL. As output voltage is constant and equal to Vz, a regulated o/p voltage is obtained. - **When Vin varies** Assume R_L constant, Vin is varying So, I_L is also constant as $I_L = V_Z/R_L$ But Vin changes & supply current also changes $I = \frac{Vin - Vz}{R_S}$ Also $I = Iz + I_L$ If Vin is increased, then current I will increase. But as Vz is constant & R_L is also constant, the I_L will remain constant. - The increase in current I will increase Iz but Iz is less than Iz (max). - Thus the output voltage will remain constant. **When I_L varies** Assume Vin constant, R_L is variable. If R_L increases, I_L will decrease. But I is constant. $I = \frac{Vin - Vz}{Rs}$ Also $I = Iz + I_L$ Therefore with decrease in I_C, Iz will increase. This can be continued without damaging the Zener diode as long as I_Z is less than I_Z max., the O/P voltage will remain constant.	2 2
Q3	**Attempt ANY FOUR**	**16**
Ans a	Acceptor Doped Material is termed as Trivalent Impurity. Donor Doped Material is termed as Pentavalent Impurity. Trivalent Impurity : Boron, Aluminium , Gallium (any one) Pentavalent Impurity : Phosphorous , Arsenic ,Antimony (any one)	1 1 1 1

Ans b

Difference between P-N Junction diode and Practical P-N Junction diode (any four)

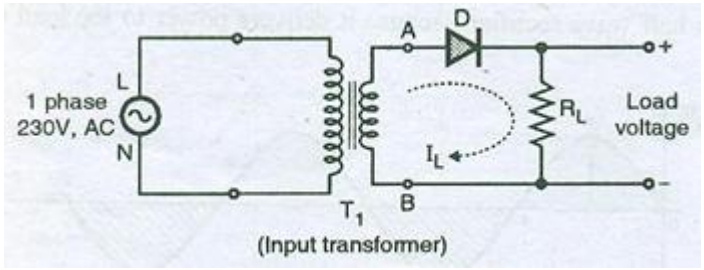
4

Sr. No	Parameter	Ideal Diode	Practical Diode
1	Forward Resistance	0Ω	FewΩ
2	Reverse Resistance	Infinity	Few hundred KΩ
3	Cut In Voltage	0V	0.6V for Silicon diode 0.3V for Germanium diode
4	Reverse saturation Current	0	Few nA For silicon diode Few mA for Germanium diode
5	Equivalent circuit in Forward bias		
6	Equivalent circuit in Reverse bias		

Ans c

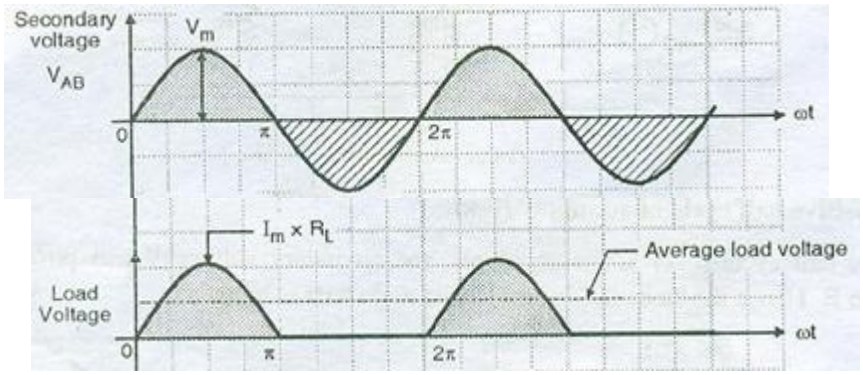
Half Wave Rectifier

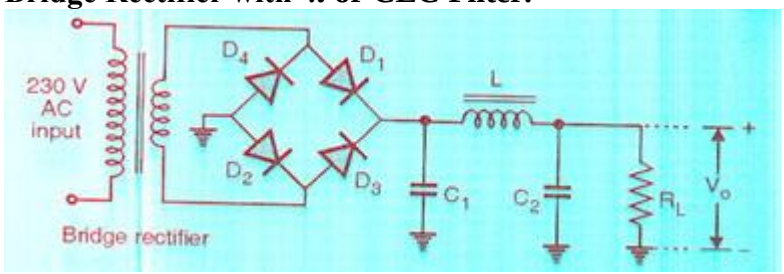
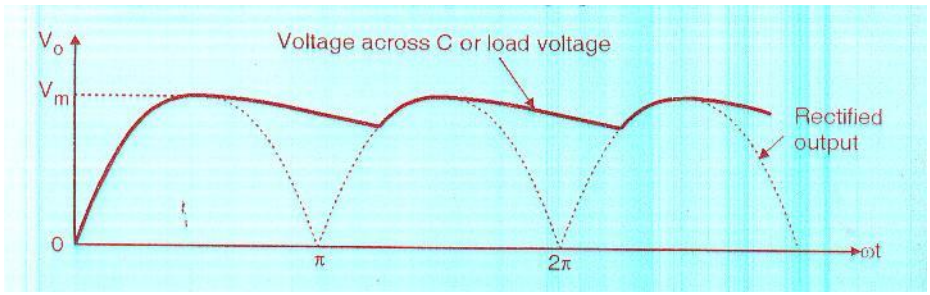
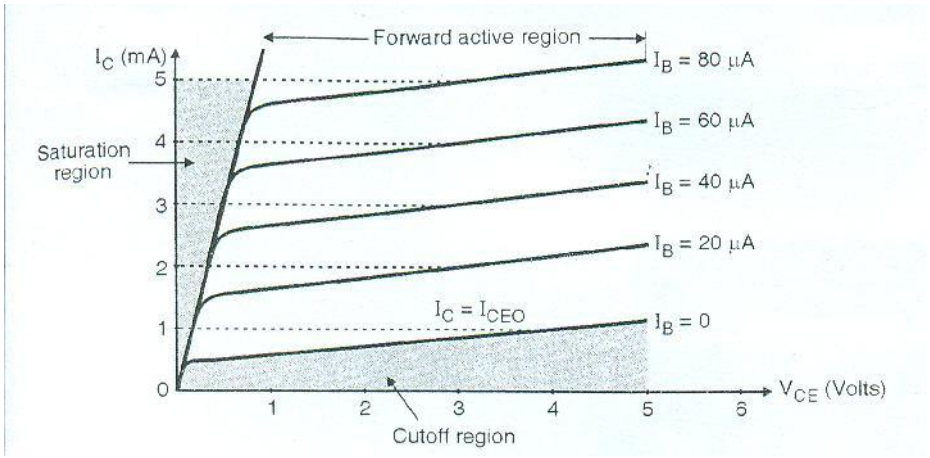
2

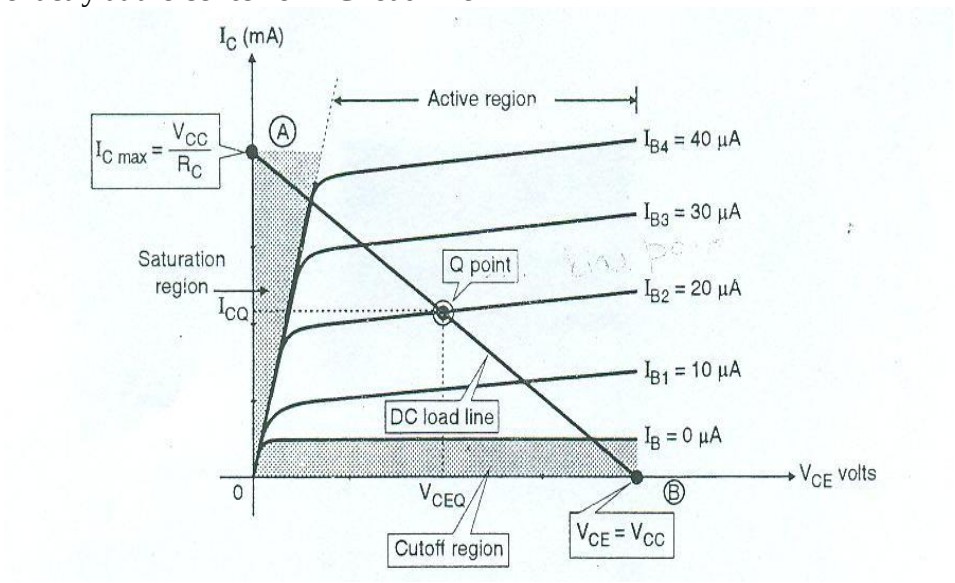
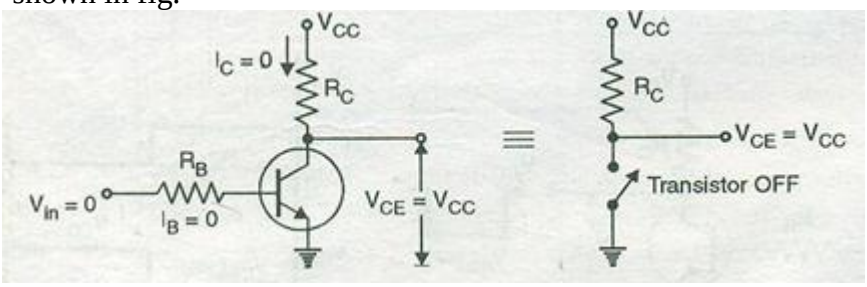


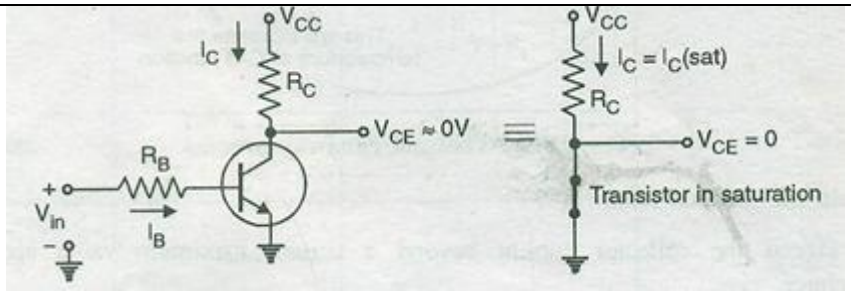
Input and Output Waveforms

2



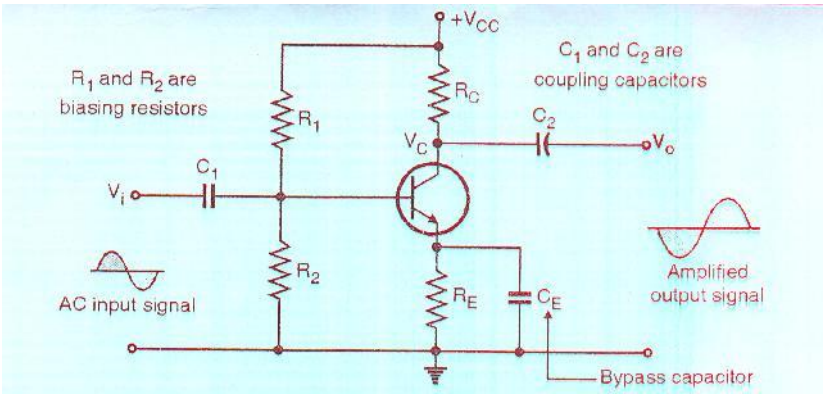
Ans d	**Bridge Rectifier with π or CLC Filter.**  **Waveforms for filter circuit.**  In bridge rectifier diodes D_1 & D_2 conduct in positive half cycle of ac input. During negative half cycle diodes D_3 & D_4 conduct. Rectified o/p of a bridge rectifier is shown in dashed wave forms. π Filter consists of two capacitors C_1 & C_2 and one inductor L. Capacitor filter bypasses unwanted ac through it and blocks dc through it as it is connected in parallel with the load R_L Inductor filter passes dc through it and blocks ac through it, as it is connected in series with the load R_L. π Type filter can be considered as combination of shunt capacitor filter and LC filter. Due to the use of three filtering elements (C_1, L & C_2) the ripple factor of π type filter is very low as compared to the other filters. **OR** **Note** : CLC filter can also be used with Full Wave center tap rectifier or Half Wave Rectifier	2 2
Ans e	**CE Output characteristics of BJT** 	2 Dia 2 label

Ans : f	If the transistor is being used for amplification purpose, then Q point is exactly at the **center** of DC load line  **Operating Point** ➢ It is the point on the load line which represents the dc current through a transistor (I_{CQ}) and the voltage across it (V_{CEQ}) when no ac signal is applied. ➢ The dc load line is a set of infinite number of such operating points and the user or designer can choose any point on the dc load as the operating point. ➢ The position of operating point on the load line is dependent on the application of the transistor. ➢ The factors affecting the stability of Q-point are : 1. Changes in temperature 2. Changes in the value of β_{dc} .	2 2
Q4 .	**Attempt any FOUR**	**16**
Ans : a	**Transistor as a switch** **Transistor in cut off region (Open Switch)** - In the cut-off region both the junctions of a transistor are reverse biased and a very small reverse current flows through transistor. - The voltage drop across the transistor (V_{CE}) is high. Thus in the cut off region the transistor is equivalent to an open switch as shown in fig.  **Transistor in the saturation region (close switch)** - When Vin is positive, a large base current flows and the transistor saturates. - In the saturation region both the junctions of a transistor are forward biased. The voltage drop across the transistor (V_{CE}) is very small of the order of 0.2V to IV depending on the type of transistor and the collector current is very large. - In saturation the transistor is equivalent to a closed switch as shown in fig. (contd. Page 10)	2 2



Ans : b

. **SINGLE STAGE CE AMPLIFIER** 2



i) **Biasing Circuit** : The resistances R_1, R_2& R_E, & R_C + V_{CC}& transistor form the dc biasing & stabilization ckts. The biasing ckt must establish a proper Q point otherwise a part of the negative half cycle of the signal may be cut off in the o/p.

ii) **Input Capacitor** : (Cin) An electrolytic capacitor C_{in} = 10µf is used to couple the sign to the base of transistor. If it is not used, then signal source resistance will come across R_2& thus change the bias. The capacitor C_{in} allows only a.c. signal to flow but isolates the signal source from R_2.

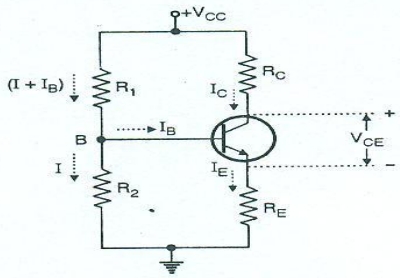
iii) **Emitter Bypass Capacitor C_E** : An emitter bypass capacitor $C_E \cong$ 100µF is used in parallel with R_E to provide a low reactance path to the amplified ac signal. If it is not used then amplified ac signal flowing through R_E will cause a vg drop across it, thereby reducing the o/p vg.

iv) **Coupling Capacitor C_C** : The C_C coupling capacitor$\cong$ 10µf couples one stage amplification to next stage. If it is not used, the bias conditions of the next stage will be drastically changed due to the shunting effect of R_C. This is because R_C will come in parallel with the upper resistance R_1 of the biasing n/w of the next stage. Therefore, the coupling capacitor C_C isolates the d.c. of one stage from the next stage, but allows the passage of a.c. signal

2

Ans : c

Voltage Divider Bias 2



(Contd. Pg. 11)

Now applying the Thevenin's theorem, we get the voltage, 2

$V_{TH} = \left(\frac{R2}{R_1 + R_2}\right). V_{CC}$

And the equivalent resistance.

$R_{TH} = R_1 \text{ll } R_2 = \frac{R_1 . R_2}{R_1 + R_2}$

Applying KVL to the base emitter loop of this circuit,

$V_{TH} = I_B R_{TH} + V_{BE} + I_E R_E$

$V_{BE} = V_{TH} - I_B R_{TH} - I_E R_E$

Applying KVL to the output section, we get

$V_{CC} = I_C R_C + V_{CE} + I_E R_E$

$V_{CE} = V_{CC} - I_C (R_C + R_E)$

Ans : d

Compare BJT and FET (any four points) 4

Sr. No.	BJT	FET
1.	BJT is a Bipolar device	FET is a unipolar device
2.	Input impedance is low (In k Ω)	Input impedance is high (In MΩ)
3.	AC voltage gain of BJT amplifier is high (100-300)	AC voltage gain of FET amplifier is low (less than 50)
5	Transfer characteristics is linear.	Transfer character of FET is non linear.
6	Thermal runaway can damage the BJT.	Thermal runaway does not take place.
7.	Noise generated by BJT is high	Noise generated by FET is low
8.	BJT is current controlled device.	FET is a voltage controlled device.
9	BJT is more sensitive	FET is less sensitive.
10	Size of BJT is bigger than FET	Size of FET is smaller than BJT.

Ans : e

Dynamic drain Resistance (r_d): 1

It is defined as the ratio of change in drain to source voltage to the corresponding change in the drain current, at a constant value of gate to source voltage.

$r_d = [\Delta V_{DS} / \Delta_{ID}]_{\text{constant VGS}}$

Transconductance (g_m) or Mutual Conductance: 1

The transconductance g_m is defined as the ratio of change in drain current to the corresponding change in gate to source voltage at a constant value of drain to source voltage.

$g_m = [\Delta_{ID} / \Delta V_{GS}]_{\text{constant VDS}}$

Amplification factor (μ): 1

Amplification factor μ is defined as the ratio of change in the drain to source voltage, to change in the gate to source voltage, at a constant value of I_D.

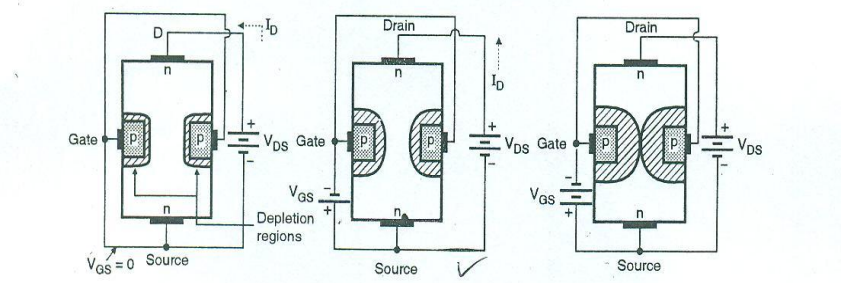
$$\mu = [\Delta V_{DS} / \Delta V_{GS}]^{I}_{D \text{ constant}}$$

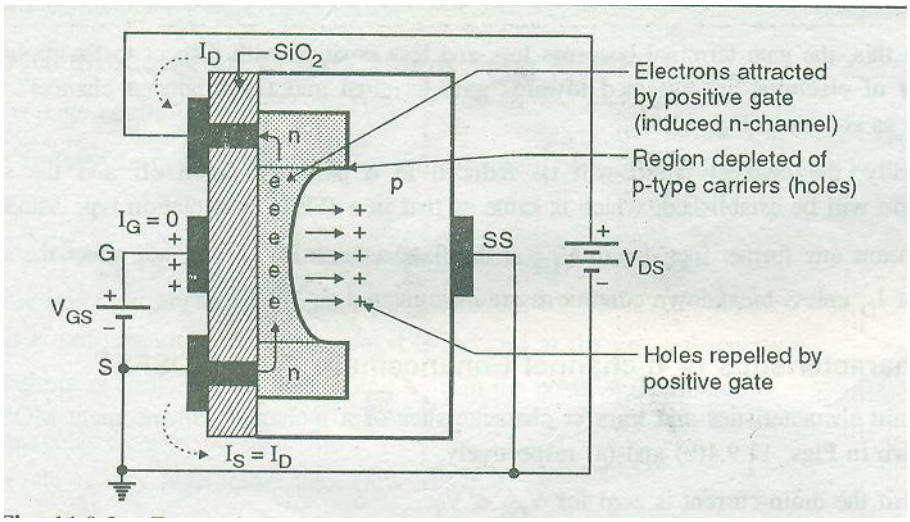
Relation between the parameters: 1

$\mu = [\Delta V_{DS} / \Delta_{ID}] * [\Delta_{ID} / \Delta V_{GS}]$

$\mu = r_d \text{ X } g_m$

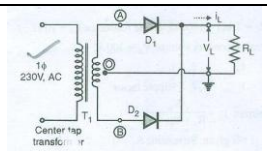
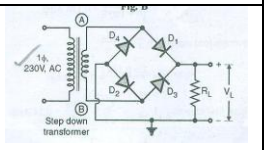
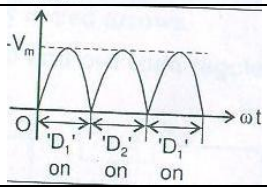
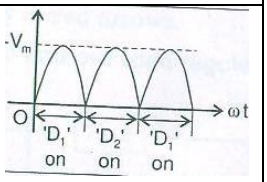
The amplification factor is equal to the product of drain resistance and transconductance.

Ans : f	 (a) Operation with no bias voltage (b) Operation with a small negative gate source bias (c) Operation with a large negative gate source bias Operation of n channel JFET : i) Operation of n-channel JFET with $V_{GS} = 0$ ➢ Due to the supply voltage V_{DS}, current starts flowing through the channel. ➢ The n-type material has a finite resistance. Therefore the drain current flow, causes a voltage drop along the channel. ➢ This voltage drop will reverse bias the gate to source p-n junction. ➢ The depletion region of the reverse biased p-n junction penetrates more into the n-type bar because it is lightly doped as compared to the heavily doped p-type gate. ➢ The penetration of the depletion region into n-type bar depends on the reverse bias voltage. Due to the depletion regions the width of the channel available for conduction is reduced. ii) Operation of a n-channel JFET for small negative V_{GS} :- ➢ Due to the reverse voltage applied across the gate source junction, the penetration of the depletion region into n-type material increases further. ➢ This will reduce the channel width further. Due to reduced channel width less number of electrons can pass through to drain from source. Therefore, drain current I_D reduces with increase in $– V_{GS}$. iii) Operation of n-channel JFET for large value of negative V_{GS} : ➢ As the negative voltage V_{GS} is further increased, the depletion region spread more inside the n-type bar. ➢ At a certain value of negative V_{GS}, the depletion regions touch each other. ➢ The channel width is therefore zero and therefore the drain current $I_D = 0$. Thus with increase in the negative gate to source voltage, the channel becomes more and more narrow and drain current I_D reduces.	2 2
Q5.	**Attempt any FOUR**	**16**
Ans : a	**Classification of ICs on the basis of** **i) Packaging** 1) Single-in-line package (SIP) 2) Dual-in-line package (DIP) 3) Flat package 4) Top hat (TO) Package. ii) **Signals processed** : 1) Analog IC (Linear IC) 2) Digital IC (Non-linear IC)	2 2

Ans : b	**Enhancement MOSFET**  The operation can be explained with two different operating conditions : i) **Operation with V_{GS} = 0 Volt** : ➢ If V_{GS} = 0V and a positive voltage is applied between its drain and source, then due to the absence of the n-type channel, a zero drain current will result. ii) **Operation when V_{GS} is positive** : ➢ The positive potential at the gate terminal will repel the holes present in the P-type substrate. ➢ This results in creation of a depletion region near the SiO_2 insulating layer. But the minority carriers i.e. the electrons in the P-type substrate will be attracted towards the gate terminal and gather near the surface of SiO_2. ➢ As we increase the positive V_{GS}, the number of electrons gathering near the SiO_2 layer will increase. ➢ The electron concentration near SiO_2 layer increases to such an extent that it creates an induced n-channel which connects the n-type doped regions. ➢ The drain current then starts flowing through this induced channel. The value of V_{GS} at which this conduction begins is called as the 'threshold voltage' and is indicated by V_T or $V_{GS\ (TH)}$	2 2
Ans : c	The relation between α and β 1) $\alpha = I_C/I_E$ (But $I_E = I_B + I_c$) $\alpha = I_C/I_B + I_C$ Divide by I_B both Numerator& Denominator $\alpha = (I_C/I_B)/(I_B/I_B + I_C/I_B)$ as $\beta = I_C/I_B$ $\alpha = \beta/1+\beta$ OR $\beta = I_C/I_B$ (But $I_E = I_B + I_c$)therefore $I_B = I_E - I_C$ $\beta = I_C/I_E - I_C$ Divide by I_E to both Numerator& Denominator $\beta = (I_C/I_E) / (I_E/I_E - I_C/I_E)$ as $\alpha = I_C/I_E$ $\beta = \alpha/1-\alpha$	4

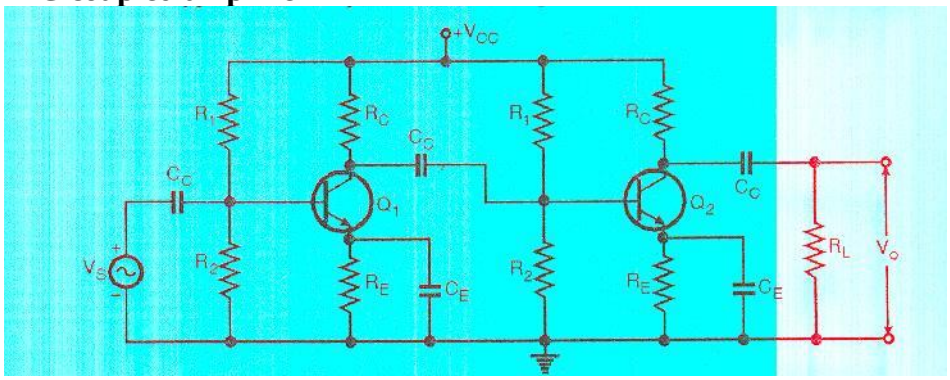
Ans : d

Compare Centre tapped rectifier and Bridge rectifier (any four) — 4

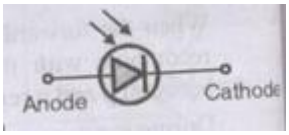
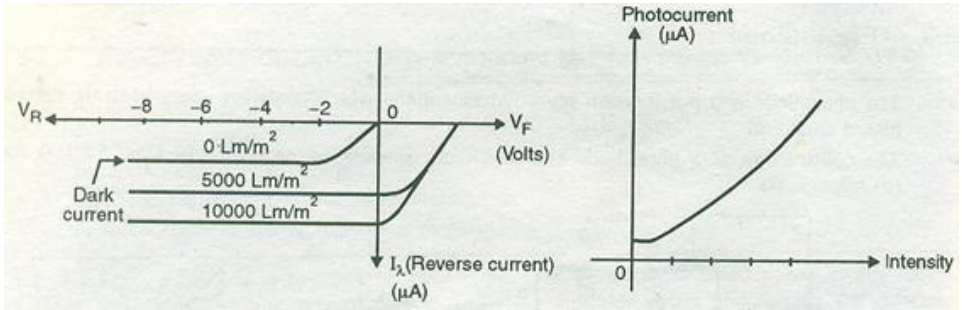
Sr. No	Parameter	Centre tapped rectifier	Bridge rectifier
1	Circuit diagram		
2	Wave forms		
3	DC or average load current I_{Ldc}	$2I_m/\pi$	$2I_m/\pi$
4.	Maximum average load voltage	$2V_m/\pi$	$2V_m/\pi$
5.	RMS load Current I_{Lrms}	$I_m/\sqrt{2}$	$I_m/\sqrt{2}$
	RMS load voltage V_{Lrms}	$V_m/\sqrt{2}$	$V_m/\sqrt{2}$
5.	DC load power P_{dc}	$4I^2_m R_L/\pi^2$	$4I^2_m R_L/\pi^2$
6.	Maximum rectification efficiency	81.2%	81.2%
7.	TUF	69.3%	81.2%
8.	Ripple factor	48%	48%
9.	Ripple frequency	100Hz	100Hz
10.	Number of diodes used	Two	Four
11.	Centre tap transformer	Very much required	Not required
12.	Transformer core Saturation	Not Possible	Not Possible
13.	PIV	$2V_m$	V_m
14.	Expression for the peak load current	$I_m=V_m/(R_s+R_f+R_L)$	$I_m=V_m/(R_s+2R_f+R_L)$

Ans : e

R-C coupled amplifier — 2



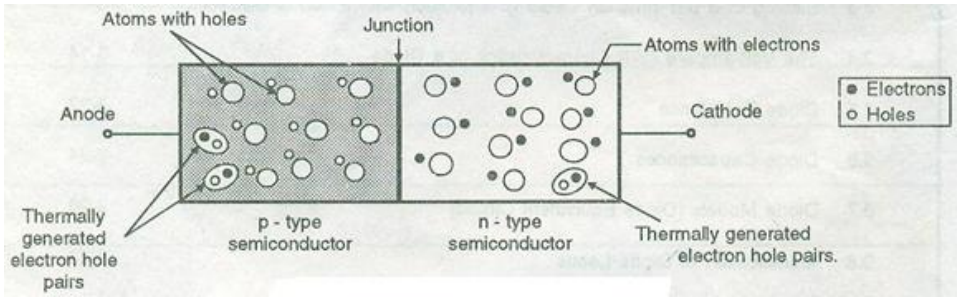
(contd. Pg. 15)

	Need of Cascading : i. The meaning of the word cascading is to connect a number of amplifier stages to each other with the output of the previous stage connected to the input of the next stage. ii. Thus a multistage amplifier is obtained by cascading a number of amplifiers. iii. The most important parameters of an amplifier are its input impedance, voltage gain, Bandwidth, and output resistance. iv. It is generally not possible for a single stage amplifier to fulfil all the requirements. Hence we have to use a multistage amplifier. v. If more than one amplifier stages are cascaded then the input stage takes care of the input impedance while the output stage takes care of the output impedance matching requirements and the middle stages will fulfil the high voltage gain requirements. Thus the cascading of amplifiers is to be done when. i. The amplification provided by a single stage amplifier is not sufficiently large ii. The input and output impedance are not of correct value.	2
Ans : f	**Photo diode:** Symbol:  Characteristics:  Applications: 1) In object counting system. 2) In the cameras for sensing the light intensity. 3) In the fiber optic receiver. 4) In light intensity meters.	1 1 2

Q6.	**Attempt any Four**	16

Ans : a

P-N Junction with no bias:



2

- P-type semiconductor and N-type semiconductor are joined together with the help of a special fabrication technique to form a p-n junction.
- Terminals are brought out for the external connection with P and N-type semiconductors. The P-side is called as anode and the N-side is called as Cathode.
- The N-side consists of a large number of electrons and few thermally generated holes whereas the P-side consists of a large number of holes and a few thermally generated electrons.
- Thus the electrons are majority carriers and holes are minority carriers in the N-region whereas their roles are exactly opposite in the P-region.
- The P-N junction forms the basic semiconductor device called diode.

Barrier Potential :

- Due to the presence of immobile positive and negative ions on opposite sides of the junction, an electric field is created across the junction. This electric field is known as the barrier potential.

1

Depletion Region :

- The region on both sides of junction contains only immobile ions and no free charge carriers such as electrons or holes. In other words this region is depleted of the free charge carriers. Therefore, this region is called as the depletion region.

1

Ans : b

Comparison between CE, CB and CC (any four)

4

Sr. No.	Parameters	CE	CB	CC
1	Common terminal between input and output	Emitter	Base	Collector
2	Input Current	I_B	I_E	I_B
3	Output Current	I_C	I_C	I_E
4	Current gain	β dc = I_C/I_B	α dc = I_C/I_E	$\gamma = I_E/I_B$
5	Input Voltage	V_{BE}	V_{EB}	V_{BC}
6	Output Voltage	V_{CE}	V_{CB}	V_{EC}
7	Voltage gain	Medium	Medium	Less than 1
8	Applications	Audio Amplifiers	As preamplifier	For impedance matching.

Ans : c

i) **Rectifier efficiency**: 1

Rectifier efficiency is defined as the ratio of DC output power to AC output power

η = DC output power / AC output power = P_{Ldc}/ P_{ac}

ii) **Current gain:**

Current gain is defined as the ratio of output current to the input current. 1

Current gain, $A_I = I_o / I_i$

iii) Voltage gain:

Voltage gain is defined as the ratio of output voltage to the input voltage. 1

Voltage gain, $A_V = V_o / V_i$

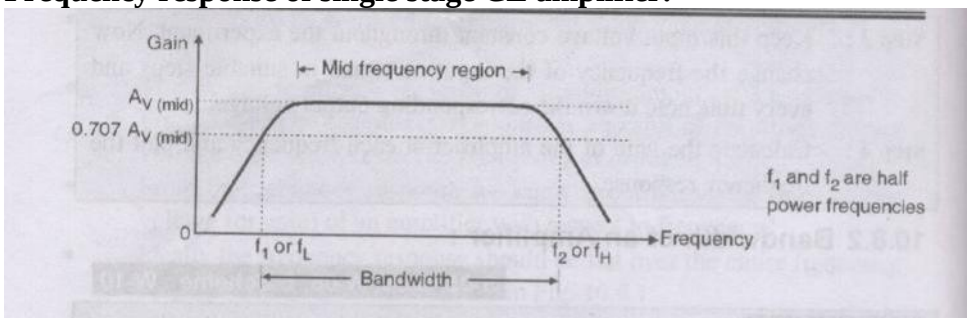
iv) Power gain:

Power Gain defined as the ratio of output power Po and input power $P_{in.}$ 1

Power gain, $A_P = P_o / P_{in} =$ Voltage gain *current gain =Vo/Vi*Io/Ii

Ans : d

Frequency response of single stage CE amplifier: 2



Gain: 1

The gain of an amplifier is defined as the ratio of output quantity to the input quantity.

Bandwidth: 1

To fix the frequency range in which the amplifier gain is relatively large a cut-off level of 0.707 Av mid or 0.707 Vo mid is chosen. The corresponding frequencies f1 and f2 are known as half power frequencies.

The bandwidth of the amplifier is defined as the difference between the half power frequencies. BW = f_2-f_1Hz

Ans : e

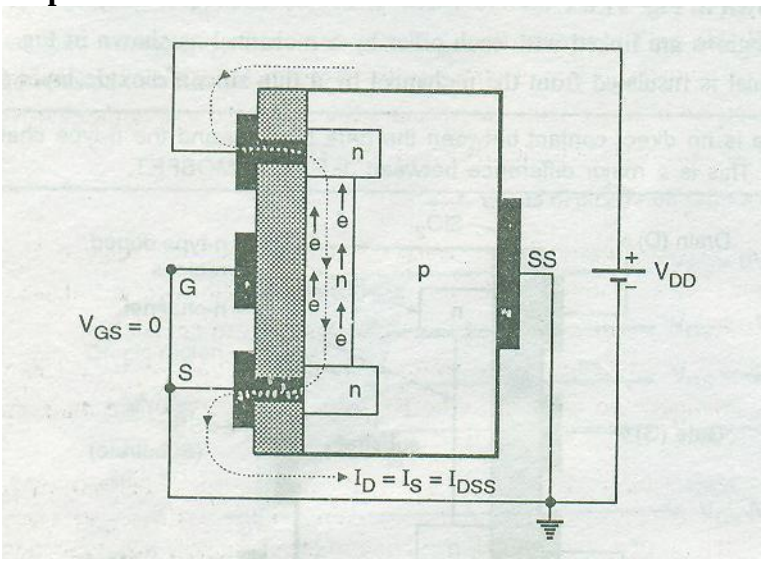
Difference between Linear IC and Non-linear IC (Any four) 4

Sr. No.	Linear IC	Non-linear IC
1	They are designed to handle and process analog signals.	They are designed to handle and process digital signals.
2	Output voltage vary according to input voltage.	Output voltage is either high or low.
3	It is a analog IC	It is a digital IC
4	It takes any inputs and produce output of any level.	It expects high/low, true/false inputs and outputs.
5	Examples are op-amp, voltage comparator, voltage regulator, power amplifiers, voltage amplifiers, etc.	Examples are logic circuits, flip-flops, counters, ADC, DAC, RAM, ROM, etc.
6	Applications are in audio amplifiers, aircrafts Radar, TV, etc.	Applications are in microprocessors, computers, digital clocks, etc.

Ans : f

Depletion MOSFET

2



i) Operation with V_{GS} = 0V :

2

- It shows that the gate, source and substrate terminals are connected together to the ground point. Thus V_{GS} = 0V. A positive voltage V_{DD} is applied between drain and source.
- Due to the positive voltage applied to the drain terminal, free electrons from the channel are attracted to the drain and the drain current starts flowing.

ii) Operation with negative V_{GS} :

- Due to negative voltage applied between gate and cathode terminals, the gate will tend to repel the free electrons towards the P-type substrate and attract the holes from the substrate.
- These electrons and holes will recombine inside the channel. This will reduce the number of free electrons available for conduction.
- Therefore the drain current will decrease with increase in negative value of V_{GS}. Thus as V_{GS} increase, I_D decreases for a constant value of V_{DS}.
- Depending on the magnitude of negative bias V_{GS}, a level of recombination between electrons and holes will occur.
- This will reduce the number of free electrons in the n-channel available for conduction.
- The higher the negative bias, the more the recombination and the less is the drain current.

iii) **Effect of positive gate to source voltage** :

- The drain current will increase as the positive voltage V_{GS} increases.
- Thus the level of free electrons has been enhanced due to the application of positive gate voltage. Therefore, the region of operation corresponding to the positive gate current is called as enhancement region of operation and the region between cut off and saturation is referred to as depletion region.

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