Important Instructions to examiners:

1) The answers should be examined by key words and not as word-to-word as given in the model answer scheme.

2) The model answer and the answer written by candidate may vary but the examiner may try to assess the understanding level of the candidate.

3) The language errors such as grammatical, spelling errors should not be given more Importance (Not applicable for subject English and Communication Skills).

4) While assessing figures, examiner may give credit for principal components indicated in the figure. The figures drawn by candidate and model answer may vary. The examiner may give credit for any equivalent figure drawn.

5) Credits may be given step wise for numerical problems. In some cases, the assumed constant values may vary and there may be some difference in the candidate's answers and model answer.

6) In case of some questions credit may be given by judgement on part of examiner of relevant answer based on candidate's understanding.

7) For programming language papers, credit may be given to any other program based on equivalent concept.

Q1. a) Attempt any six of the following : **12 M**

i) Define slew rate and input offset voltage.

Ans:- **Slew Rate:-** **01 M**

It is defined as the maximum rate of change of output voltage per unit time.

$$SR = \frac{dV_0}{dt}\Big|_{\max} \quad \frac{V}{\mu s}$$

Input offset voltage :- **01 M**

It is voltage that must be applied between the two input terminals of op – amp to nullify the output.

ii) Write the meaning of following IC number :- µA 741 TC

Ans:- **(01 M for µA741, 01 M for TC)**

IC number :- µA 741 TC

µA741	T	C
↑	↑	↑
Fairchild Manufacturer	Package type (mini DIP)	Commercial temperature range (0^0 to 70^0 C)

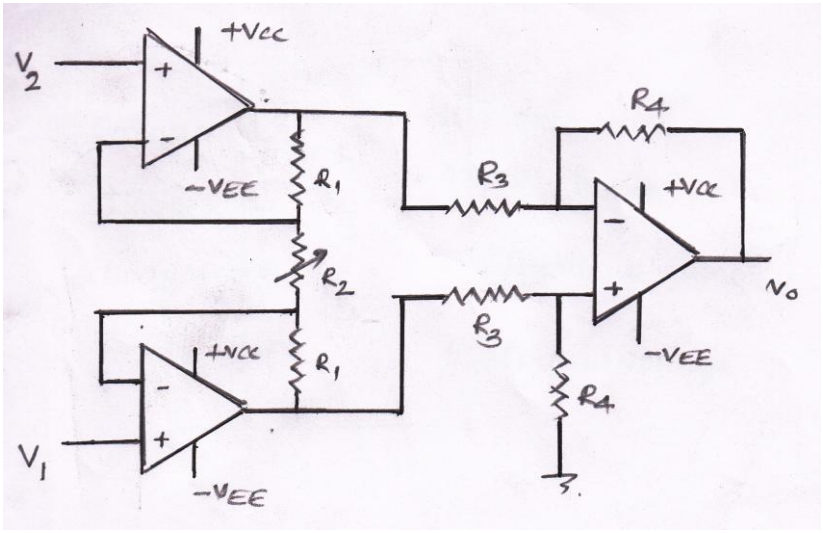
iii) List any four characteristics of op - amp with their ideal and practical values.

Ans**:-** **(Any four points, ½ M for each point)**

Characteristic	Ideal values	Practical value
Input impedance	$R_i = \infty$	2MΩ
Output impedance	$R_o = 0$	75MΩ
Voltage gain	∞	$2 * 10^5$
Bandwidth	∞	1MHz
CMRR	∞	90dB
Slew rate	∞	0.5V/µs
SVRR	0	150µV/V

iv) Draw only circuit of instrumentation amplifier using 3 op – amp and write its output equation.

Ans:- **Diagram :-** **01 M**



Output Equation:- **01 M**

$$V_0 = \frac{R_4}{R_3}\left(1+\frac{2R_1}{R_2}\right)(V_1 - V_2)$$

v) List advantages of active filters.

Ans:- **Advantages of active filters are** :- **(½ * 4 = 02 M)**

a) High value of pass band gain can be obtained.

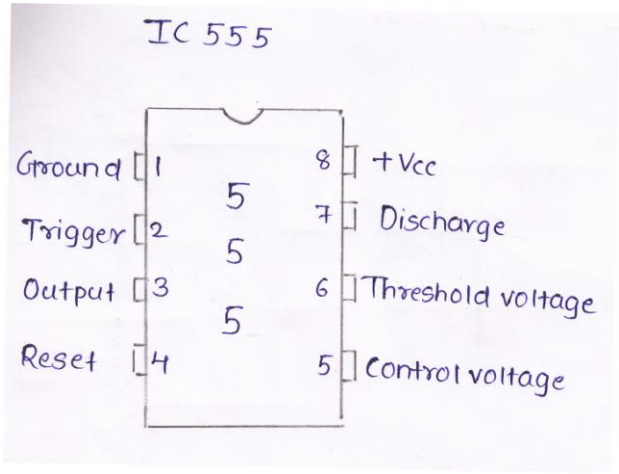
b) It is very easy to select cutoff frequency.

c) They will not produce loading effect because the output impedance is less.

d) They are not using inductor so designing of active filter is simple, cost is less and it occupy less space.

vi) Draw pin configuration of IC 555 and write the function of pin no 6.

Ans:- **Pin configuration of IC 555:-** **01 M**

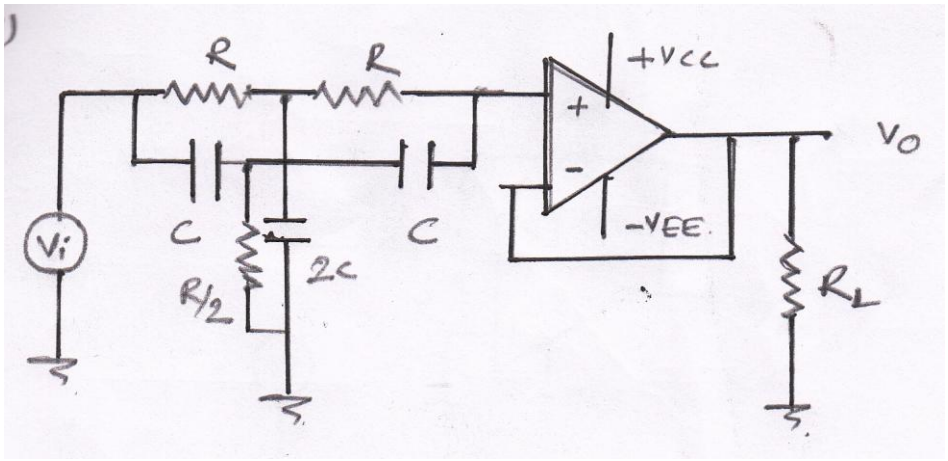


Function of pin no 6. Of IC 555:- **01 M**

When positive going pulse is applied at this pin, but it is more positive then reference voltage (2/3 V_{CC}) of upper comparator then output of timer goes low.

vii) Draw only circuit of notch filter and write formula for notch frequency F_N.

Ans **Circuit diagram:-** **01 M**



Formula :- **01 M**

$$F_N = \frac{1}{2\Pi RC}$$

viii) What is the need of signal conditioning and signal processing.

Ans:- **Need of signal conditioning :-** **01 M**

It means manipulating analog signal in such a way that it meets requirements of next stage for further processing**.**

Need of signal processing:- **01 M**

It deals with operation on signals or measurements of time varying physical quantities.

Q1. b) Attempt any two of the following: **08 M**

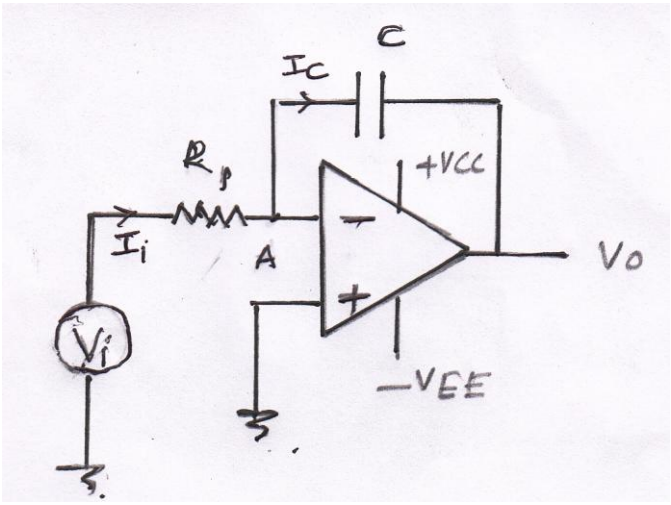
i) Why open loop configuration of op – amp is not used for linear application.

Ans:- **04 M**

- Open loop voltage gain op – amp is not constant voltage gain, it varies with temperature, power supply, mass production techniques. This makes op – amp unsuitable for linear application, as in most linear application output is proportional to the input.
- Bandwidth of most open loop op – amp is zero in ac application.

ii) In basic Integrator circuit, derive the formula for output voltage. Also write the drawbacks of basic integrator.

Ans:- **Circuit Diagram : -** **01 M**



Derivation :- **02 M**

Apply KCL at A,

$I_i = I_C + I_{B2}$ since I_{B2} is similar to or equal to zero

$I_1 = I_C$

Now, according to ohm's law,

$$\frac{V_i - V_A}{R_1} = C * \frac{d_{vi}}{d_t}$$

Therefore $$\frac{V_i - V_A}{R_1} = C * \frac{d}{d_t}(V_A - V_0)$$

$$\frac{V_i}{R_1} = C * \frac{d}{d_t}(-V_0)$$ since $V_A = 0$

Now, taking integration on both sides,

$$\int \frac{V_i}{R_1} = -c \int \frac{d}{dt} V_0$$

Therefore,

$$\int V_i * dt = -Ri * c \int dV_0$$

Therefore,

$$V_0 = -\frac{1}{R_1 * C} \int V_i * dt$$

Drawbacks :- **01 M**

a) It can operate as integrator over a short frequency range.

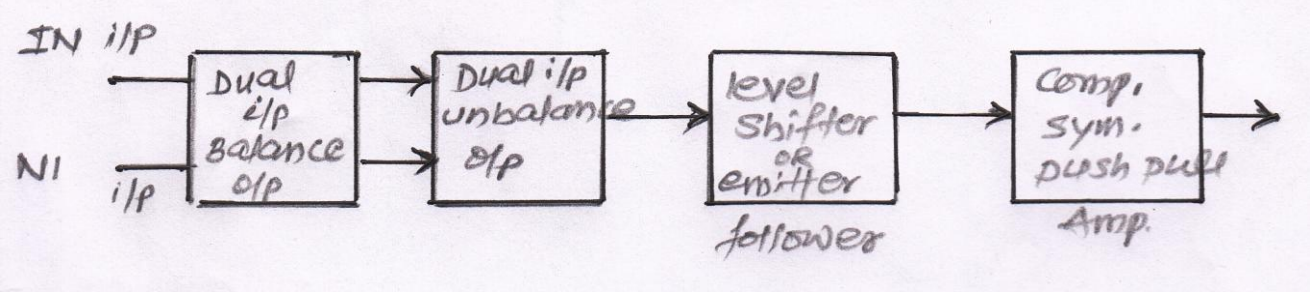
b) Outside this frequency range, the output is distorted.

c) Op – amp parameters offset the output.

d) Gain reduces with increase in frequency.

iii) Explain block diagram of op- amp.

Ans:- **Block diagram :-** **02 M**



Explanation :- **02 M**

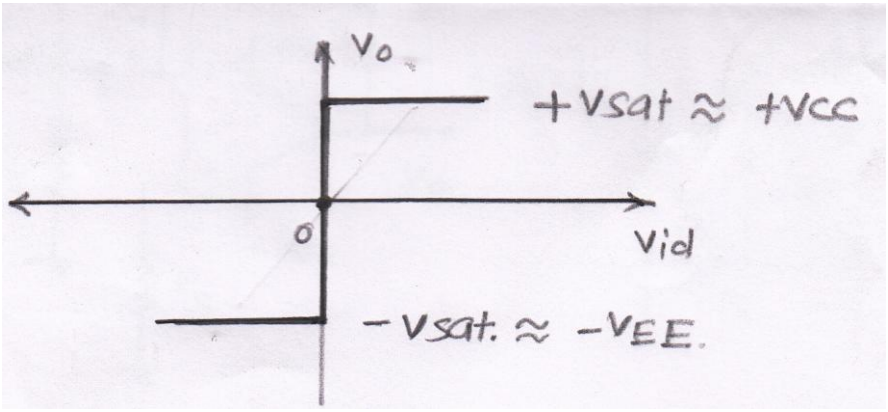
Block diagram of op – amp, V_1 and V_2 are the two inputs voltage applied to the first stage. The first stage is a dual input balanced output differential amplifier. It provides necessary voltage gain and input resistance. Output of first stage is given to the input of second stage which is dual input unbalanced output differential amplifier and it is used for additional gain it also isolate the level shifting circuit from one stage. The third stage is level shifting stage. This circuit shift the DC level at the output of second stage to zero volt.

Output of third stage is given to the push pull amplifier. It is used to provide necessary power gain and output swing and also provides low resistance.

Q2) Attempt any four of the following:- **16 M**

a) Draw and explain ideal voltage transfer curve of op – amp.

Ans:- **Ideal voltage transfer curve :-** **02 M**



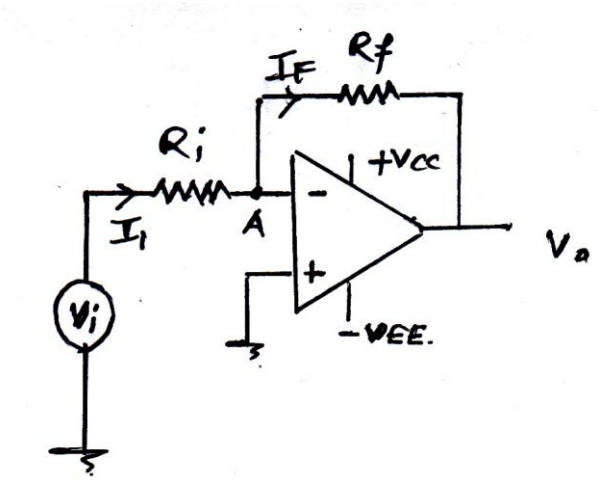
Explanation :- **02 M**

In basic op – amp operation, the offset voltage is assumed to be zero where the output voltage is plotted against input difference voltage (V_{id}) keeping gain constant. However, that the output voltage cannot exceed the

positive and negative saturation voltage. These saturation voltage are specified by an output voltage swing rating of the op – amp for given value of supply voltage that means output voltage is directly proportional to the input difference voltage only until it which is the saturation voltage and that there after output voltage remains constant. Hence, these curve is called an ideal voltage transfer curve.

b) Derive the expression for gain in inverting amplifier with feedback.

Ans:- **Circuit diagram :-** **02 M**



Derivation :- **02 M**

Apply KCL at point A,

$I_1 = I_{B2} + I_F$ ……(1)

But, $I_{B2} = 0$ ……due to virtual grounding

So, $I_1 = I_f$ ……(2)

Now, as ohm's law

$$I = \frac{V}{R}$$

$$I_1 = \frac{V_i - V_A}{R_i} \quad and \quad I_f = \frac{V_A - V_0}{R_f}$$

$$so, \quad \frac{V_i - V_A}{R_i} = \frac{V_A - V_0}{R_f}$$

$V_A = 0$ ……..virtual grounding

$$therefore, \quad \frac{V_i}{R_i} = \frac{-V_0}{R_f}$$

$$therefore, \quad V_0 = -\frac{R_f}{R_i} * V_i$$

c) Design the circuit to get the output voltage $V_0 = 3V_1 + 2V_2$, where V_1 and V_2 are input voltages.

Ans:-

[***Note :- The value of R_1, R_2 may be different it depends on assume value of Rf]***

Compare with $Vcc \approx V_{EE} \approx \pm 12V$ or $\pm 15V$

$$-\left[\frac{R_f}{R_1}(V_1) + \frac{R_f}{R_2}(-V_2)\right]$$

Assume Rf = 6KΩ

We have

$$therefore, \quad \frac{R_f}{R_1} = 3 \ \& \ \frac{R_f}{R_2} = 2$$

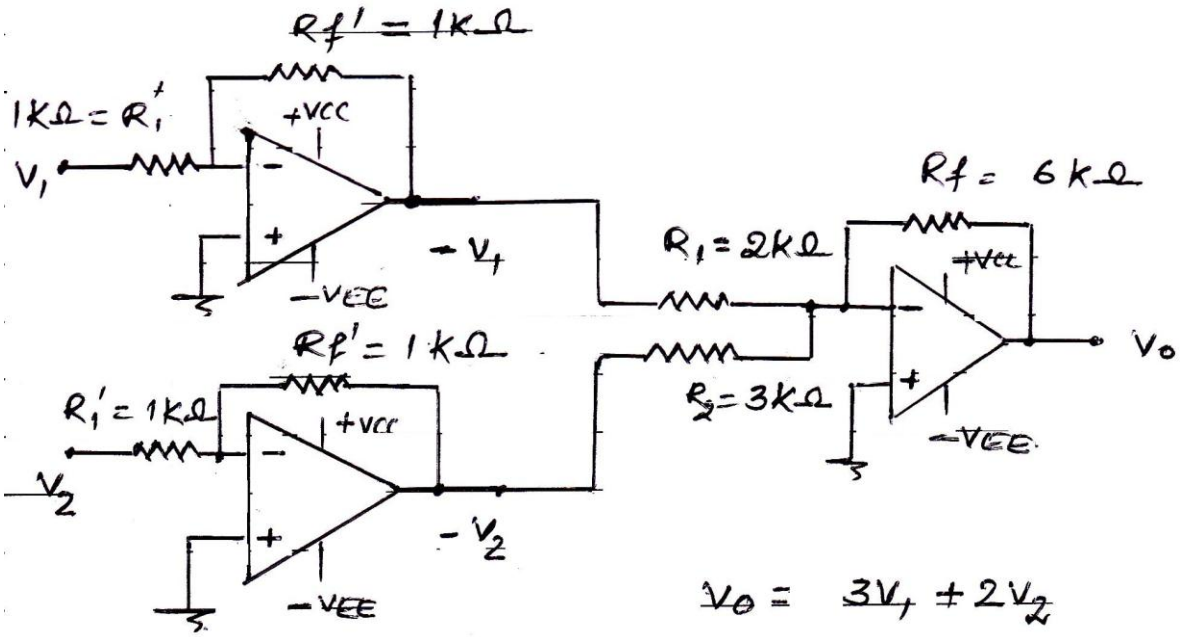
Therefore,

$R_1 = 2K\Omega$

$R_2 = 3K\Omega$

02 M

Circuit diagram :- **02 M**



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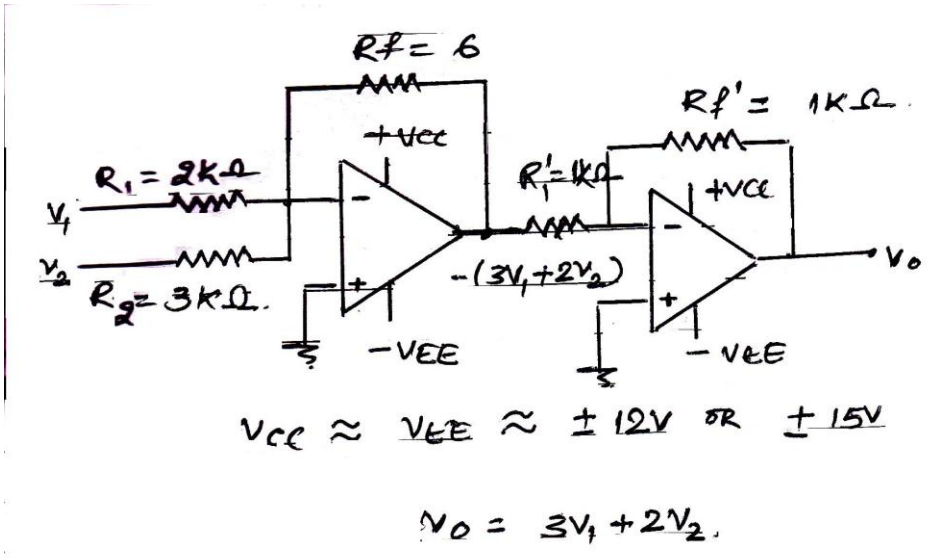
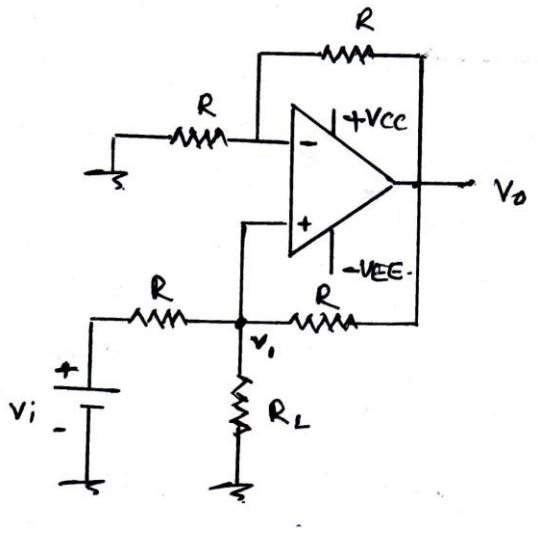


d) Explain voltage to current convertor with grounded load.

Ans:- **Diagram:-** **02 M**



Explanation :- **02 M**

$$V_0 = (1 + \frac{R}{R}) V_1 \quad \text{.....(1)}$$

$$V_0 = (1 + 1) V_1$$

Therefore $V_0 = 2V_1$.....(2)

Apply KCL at node V_1,

$$I_1 + I_2 = I_{B2} + I_L \quad \text{.....} I_{B2} \approx 0$$

$$I_1 + I_2 = I_L$$

$$\frac{V_i - V_1}{R} + \frac{V_0 - V_1}{R} = I_L$$

$$\frac{V_i - V_1 + V_0 - V_1}{R} = I_L$$

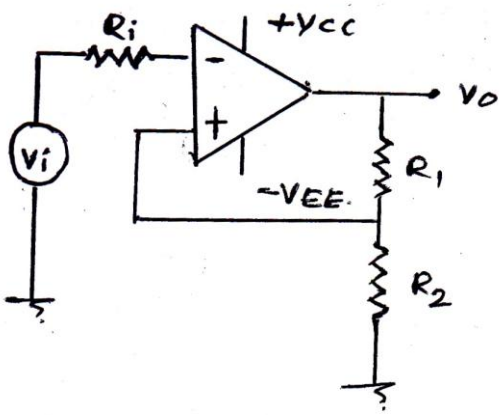
$$\frac{V_i + V_0 - 2V_1}{R} = I_L \quad \text{.....since } V_0 = 2V_1$$

$$\frac{V_i + 2V_1 - 2V_1}{R} = I_L$$

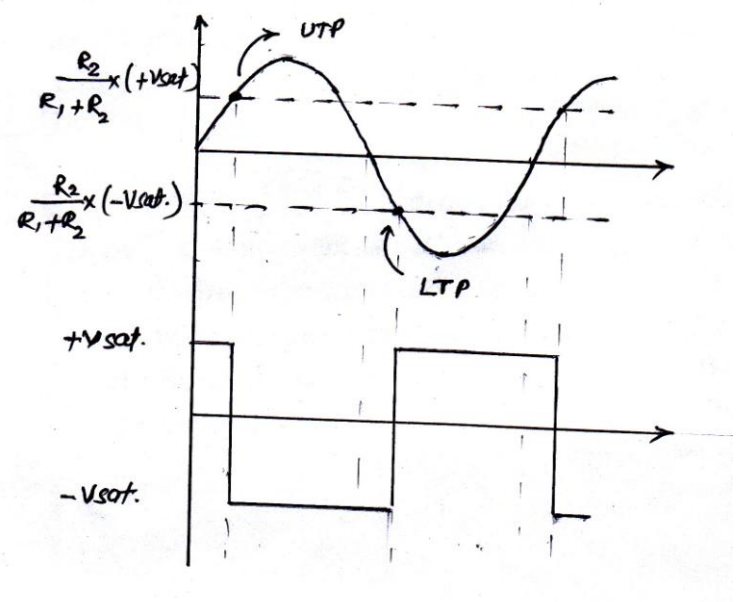
$$I_L = \frac{V_i}{R}$$

e) Explain Schmitt trigger using op –amp with neat circuit and waveforms

Ans:- **Diagram :-** **01 M**



Waveform:- **01 M**



Explanation :- **02 M**

A Schmitt trigger converts on irregular shape waveform into a square wave. It is used positive feedback. It is a special type of comparator in which the output changes from one saturation level to depending on differential input voltage.

- Before applying any input the output is assume to be small and positive. This is the output offset voltage. The differential voltage is positive, hence the output is driven into +Vsat. At this instant, the potential at point B is

$$V_B = \frac{R_2}{R_1 + R_2} * (+Vsat)$$

- This is called upper trigger point (V_{UTP}). When the input becomes more positive than UTP, the differential input is negative. Therefore output is driven in –Vsat. At this instant, the potential at point B is,

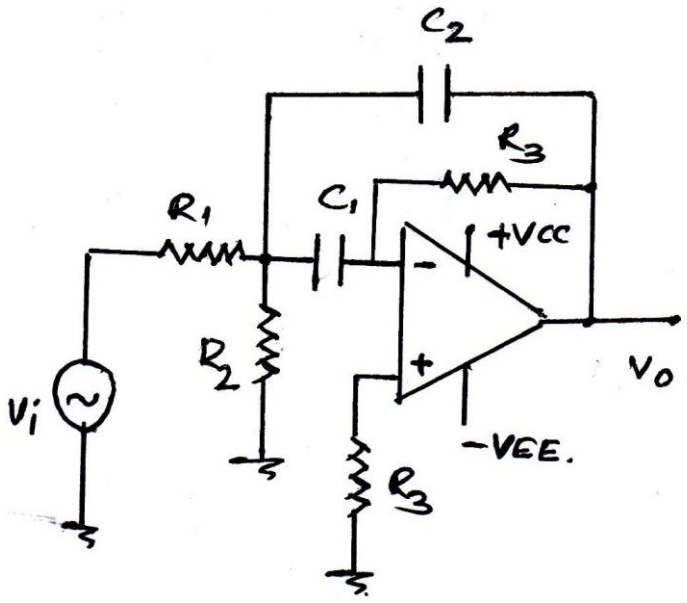
$$V_B = \frac{R_2}{R_1 + R_2} * (-Vsat)$$

This is called lower trigger point (V_{LTP}). The output remains at –Vsat until input voltage becomes more –ve than LTP.

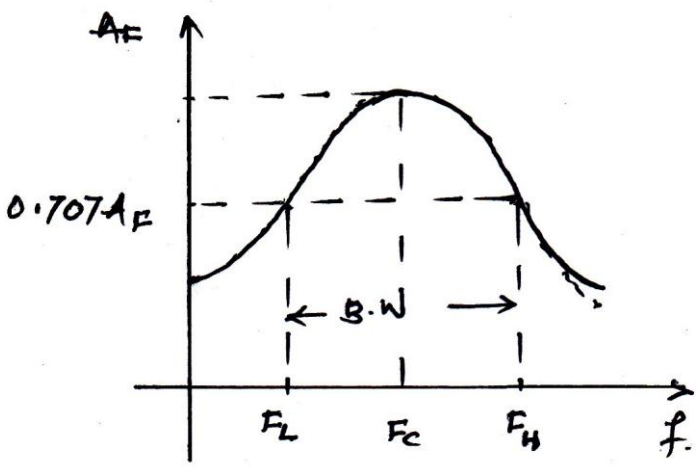
- When input crosses and becomes more negative than LTP, the differential input voltage is positive and the output becomes +Vsat.

f) Explain narrow band pass filter with neat circuit and frequency response.

Ans:- **Circuit Diagram:-** **02 M**



Frequency response :- **01 M**



Explanation :- **01 M**

This filter uses only one op – amp in inverting mode with multiple feedback. It can be designed for specific values of center frequency f_C & Q.

To simply design calculation, choose $C_1 = C_2 = C$

$$R_1 = \frac{Q}{2\Pi f_C C * AF}$$

$$R_2 = \frac{Q}{2\Pi f_C C(2Q^2 - AF)}$$

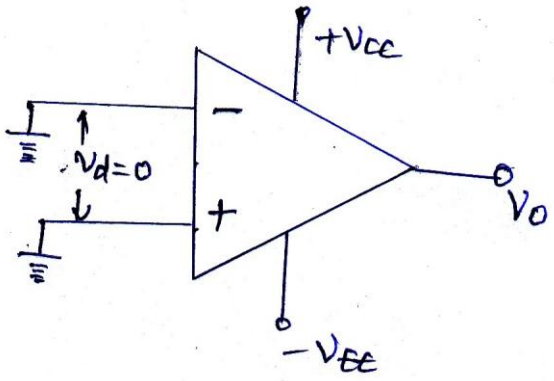
$$R_3 = \frac{Q}{\Pi f_C * C}$$

$$Gain\ AF = \frac{R_2}{2R_1}$$

Q.3 Attempt any four of the following: **16M**

a) Explain virtual ground concept.

Ans: Diagram: **1M**



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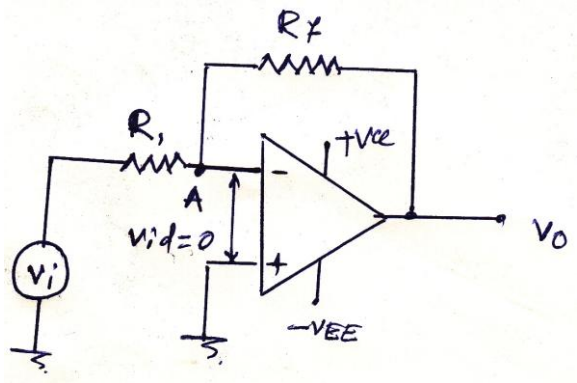


Virtual Ground Concept: **3M**

The voltage $V_I = 0$, implies that terminal A has same potential at terminal 2(non - inverting) since non inverting is grounded hence terminal A is also virtually grounded thus we can say that there is virtual ground at negative terminal (at A). The term virtual is used to implies that since feedback serves to keep the voltage V_i at zero, no actual current flows from negative to positive terminal i.e. inverting and non - inverting. Thus virtual ground point has a zero Voltage at A and draws no current. Due to zero potential at A this concept is called Virtual ground concept.

b) Define; roll off rate, order of filter, Band width and cut off frequency.

Ans: Roll off rate: **1M**

The rate at which gain falls off rapidly in stop band is Roll off rate.

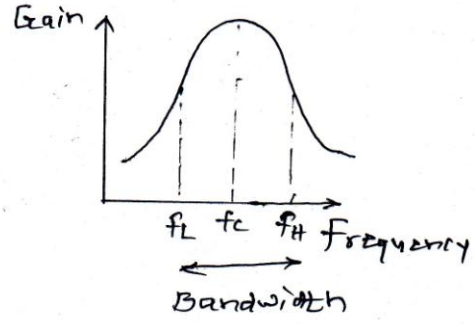
Order of filter: **1M**

Transfer function of filter is given by,

T(s) = N(s) / D(s)

The degree of D(s) determines order off filter.

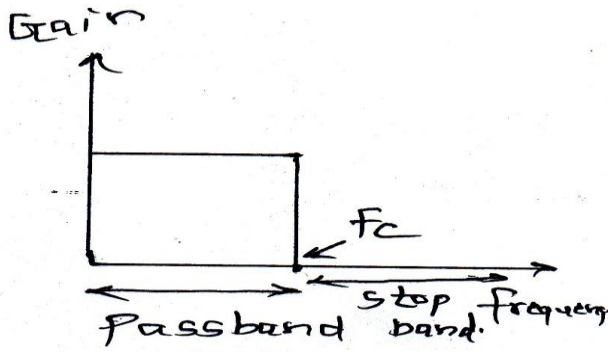
Bandwidth: **1M**



The difference between higher cutoff frequency (f_H) and lower cutoff frequency (f_L) is bandwidth.

$BW = f_H - f_L$

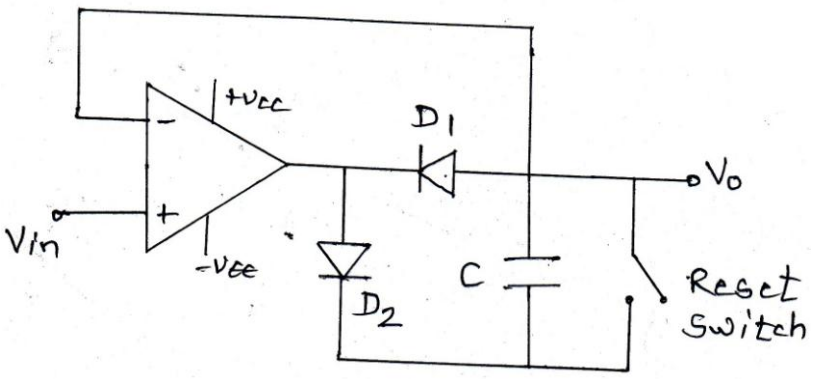
Cut off frequency (f_C) : 1M



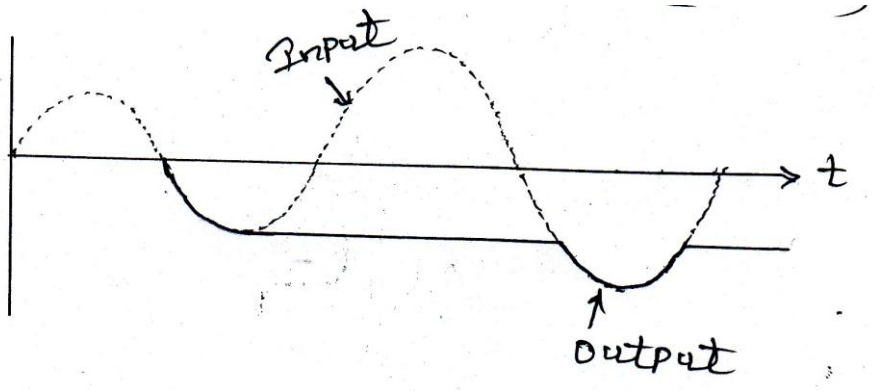
Boundary between pass band and stop band of filter is cut off frequency

c) Explain active negative peak detector with neat circuit and waveforms.

Ans: Circuit diagram of active negative peak detector: 1 ½M



Waveform: 1M



Explanation: 1 ½M

In the positive half cycle, diode D_1 will be reverse biased and diode D_2 will be forward biased.

In the negative half cycle, diode D_1 will be forward biased and diode D_2 will be reversed biased so capacitor charges to negative peak of input voltage. OP-AMP acts as voltage follower.

In the next positive half cycle, diode D_1 reverse biased and D_2 forward biased and voltage across capacitor 'C' is retained. Capacitor maintains constant negative voltage equal to negative peak of input voltage.

d) Identify the following Fig. No. 1 and write equation of O/P at each stages.

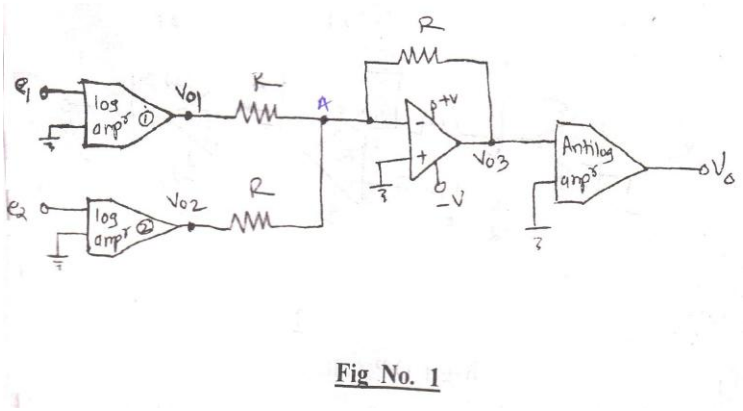


Fig No. 1

Ans:

$V_{o1} = -K_1 \log_e e_1 K_2$ } (01 Mark)

$V_{o2} = -K_1 \log_e e_2 K_2$ }

To find V_{o3} we have to use Superposition Theorem.

$$V_{o3} = -\frac{R}{R} V_{o1} + \left(-\frac{R}{R} V_{o2}\right)$$

$$= -[V_{o1} + V_{o2}]$$

$$= -[-K_1 \log_e e_1 K_2 + (-K_1 \log_e e_2 K_2)]$$

$$= [K_1 \log_e e_1 K_2 + K_1 \log_e e_2 K_2]$$

$V_{o3} = K_1 \log_e (K_2^2 e_1 e_2)$ (01 Mark)

$V_o = \text{Antilog}(V_{o3})$

$V_o = \frac{1}{K_1 K_2} e^{(K_1 \log_e (K_2^2 e_1 e_2))}$

$V_o = \frac{1}{K_1 K_2} K_1 K_2^2 e_1 e_2$

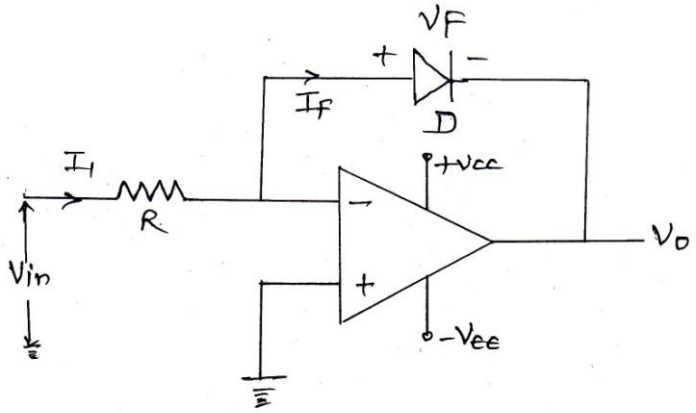
$V_o = K_2 e_1 e_2$ (01 Mark)

Given circuit is Multiplier (01 Mark)

K_1 & K_2 are scaling factors

e) Explain logarithmic amplifier.

Ans: Diagram: **1M**



Explanation: **3M**

$V_O = -V_F$

$I_1 = I_F = V_{in}/R$

Voltage across Diode (V_F)

$V_F = \eta\ V_T\ (\log_e I_F - \log_e I_O)$

Where V_F = Diode forward voltage

I_F = Diode forward current

I_O = saturation current of diode

V_T = thermal voltage

η = 2 for silicon diodes.

From (1) and (2)

$\therefore\ V_O = -\eta\ V_T\ (\log_e I_F - \log_e I_O)$

$V_O = -\eta\ V_T\ [\log_e (V_{in}/R) - \log_e I_O]$

$V_O = -\eta\ V_T\ [\log_e (V_{in}/I_O * R)]$

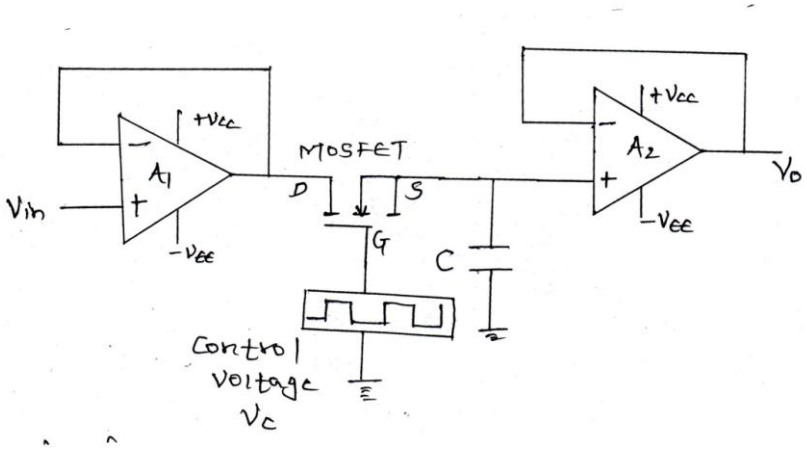
$V_O = -\eta\ V_T \log_e (V_{in}/V_{ref})$

$V_O \propto$ logarithm of input voltage

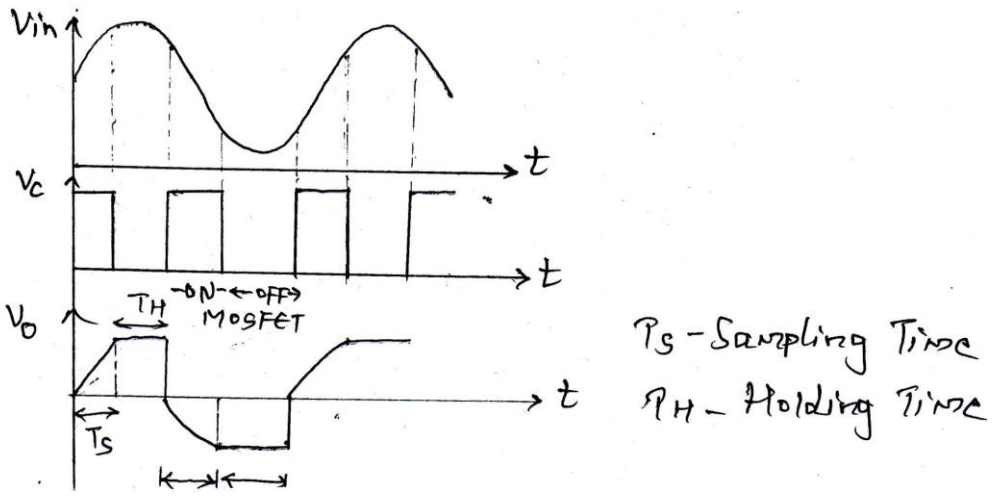
i.e. $V_O \propto \log_e V_{in}$

f) Explain sample and hold circuit with neat diagram and waveforms.

Ans: Diagram: **1 ½M**



Waveforms: **1M**



Explanation: **1 ½M**

Sample and hold circuit is shown in figure.

Sample and hold circuit samples an input signal and holds on its last sampled value until input is sampled again.

MOSFET works as a switch which is controlled by control voltage Vc. The capacitor stores charge. Input voltage Vin is applied to MOSFET. The control voltage Vc is applied to gate of the MOSFET.

When Vc is positive, MOSFET turns ON and capacitor charges to instantaneous value of input Vin. Thus Vin appears across capacitor 'C' then at output through voltage follower A_2.

When Vc is zero, MOSFET is off, but capacitor cannot discharge due to high input impedance of voltage follower A_2. Capacitor holds voltage across it.

Time during which Vc = Vin is sampling time Ts.

Time during which voltage across capacitor is constant is holding time (T_H)

Q.4 Attempt any four of the following: **16M**

a) Calculate the output voltage for open-loop non-inverting amplifier if Vin = 10mV dc. Also draw i/p and o/p waveforms.

Ans: Solution: **2M**

For open loop Non-inverting amplifier,

$V_O = A\ Vin$ -------- $A = 2 \times 10^5$

$V_O = 2X10^5 \times 10 \times 10^{-3}$

$= 20X10^2$

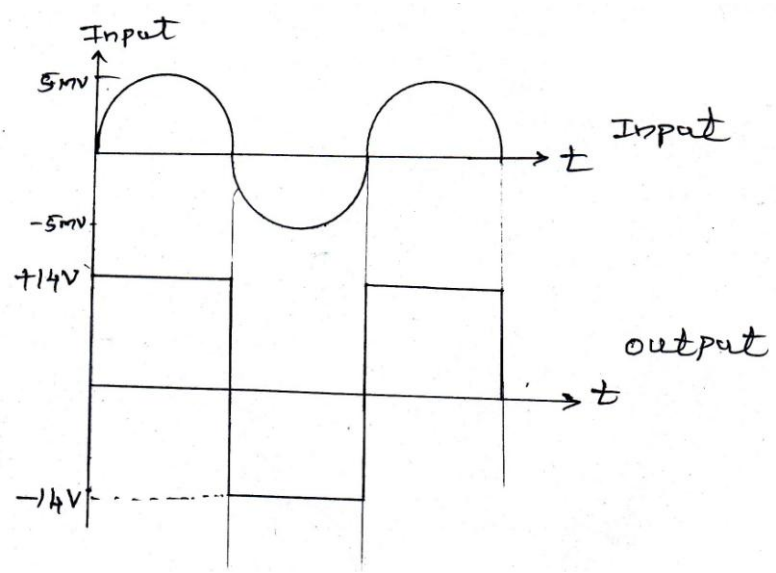
$= 2kV$

But maximum output of OP-AMP will never exceed ± Vsat i.e. ± 14V

$\therefore V_O = Vsat$

$= \pm 14V$ or 28 Vpp

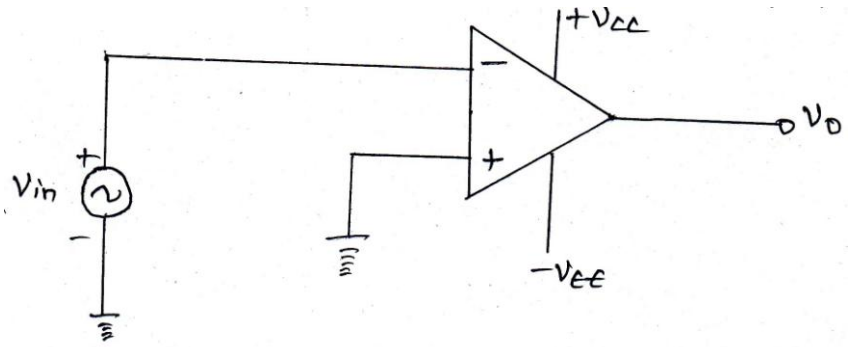
Waveforms: **2M**



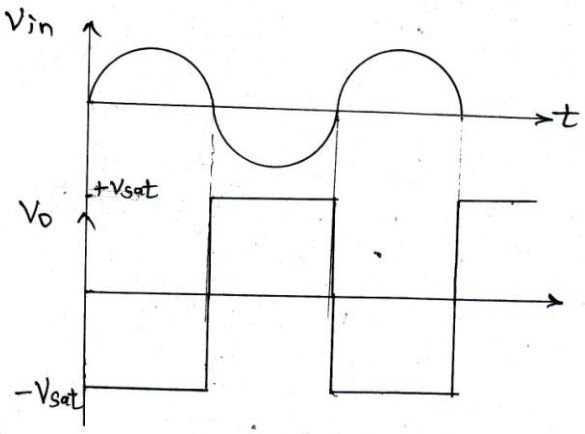
{(Note :- ± Vsat can be ± 12V to ± 14V) credit should be given if students consider Vsat in this range}

b) Draw inverting ZCD and explain.

Ans: Diagram: **1M**



Waveform: **1M**

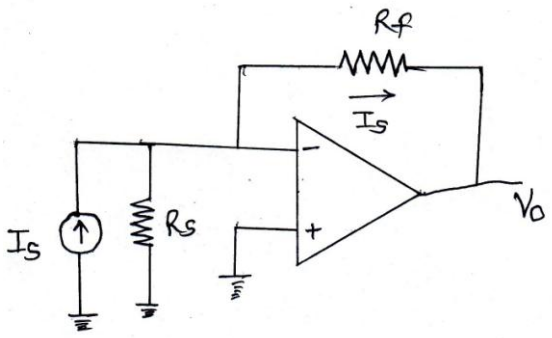


Explanation: **2M**

When input signal passes zero in positive direction, output V_O is driven into negative saturation. Similarly when Vin passes zero in negative direction, output V_O switches into positive saturation.

c) Explain current to voltage converter. Write its application.

Ans: Diagram: **2M**



Explanation: **1M**

Since inverting terminal is at virtual ground, no current flows through R_S and current I_S flows through feedback resistor R_F.

$\therefore$ output voltage $V_O = -I_S R_F$

Input current is converted into output voltage. Therefore output voltage is proportional to input current.

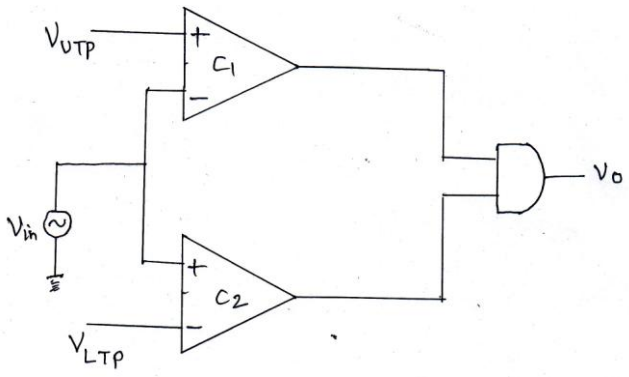
Applications: **1M**

1) Light intensity meter

2) Digital to Analog converter (DAC)

d) Explain window detector with neat circuit.

Ans: Diagram: **2M**



Explanation: **2M**

Window detector uses two comparators C_1 and C_2. Reference voltage of comparator C_1 is V_{UTP} and reference voltage of comparator C_2 is V_{LTP}.

Assume $V_{LTP} < V_{UTP}$

Case i) When Vin < V_{LTP}:

Output of comparator C_2 is low and also Vin< V_{UTP} so output of C_1 is high and output of AND gate is low.

Case ii) When Vin> V_{UTP}:

Output of comparator C_1 is low and output of comparator C_2 high. So output of AND gate is low.

Case iii) When V_{LTP} < Vin < V_{UTP}:

Output of both comparators C_1 and C_2 is high and output of AND gate is also high.

This circuit can detect voltage between two different voltage levels.

e) Calculate the O/P voltage of following circuit if R1 = 1KΩ and Rf = 1.8 KΩ. (Refer fig. No. 2)

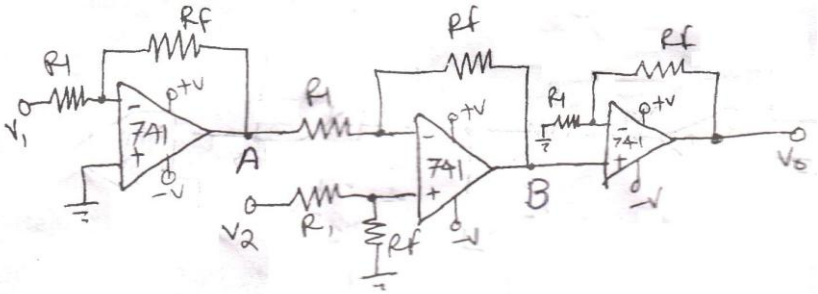


Fig No. 2

Ans:

$$V_A = -\frac{R_f}{R_1} V_1 = -\frac{1.8}{1} V_1 = -1.8 V_1$$ —— (01 Mark)

$$V_B = (V_2 - V_A)\frac{R_f}{R_1}$$

$$= [V_2 - (-1.8 V_1)]\frac{R_f}{R_1}$$

$$V_B = 1.8(V_2 + 1.8 V_1) \quad \text{—— (1)} \quad \text{—— (01 Mark)}$$

$$V_o = \left(1 + \frac{R_f}{R_1}\right) V_B \quad \text{—— (2)} \quad \text{—— (01 Mark)}$$

Put equation (1) in equation (2)

$$V_o = \left(1 + \frac{R_f}{R_1}\right) 1.8(V_2 + 1.8 V_1)$$

$$V_o = (1 + 1.8)\, 1.8(V_2 + 1.8 V_1)$$

$$V_o = 5.04(V_2 + 1.8 V_1)$$ —— (01 Mark)

f) Design the circuit to get O/P voltage $V_O = 5V_i$ and draw design circuit.

Ans: Design: **2M**

$V_O = 5V_i$

Given equation shows that gain is positive, therefore it is non inverting configuration.

Gain of Non-Inverting configuration = $1+ R_f/R_1$

i.e. $1+ R_f/R_1 = 5$

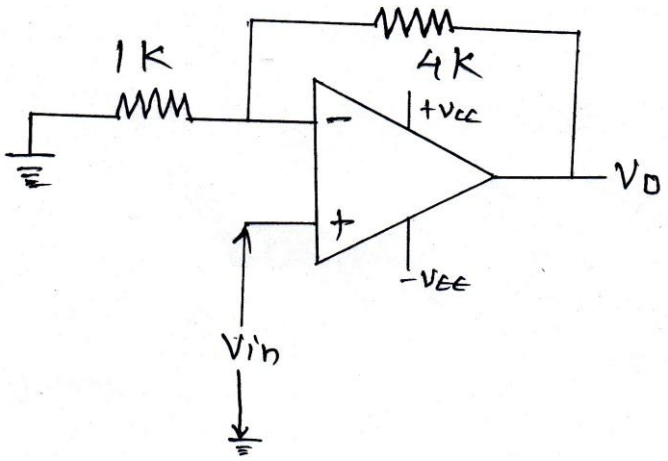
$R_f/R_1 = 4$

$R_f = 4R_1$

Assume $R_1 = 1K$

$\therefore R_f = 4K$

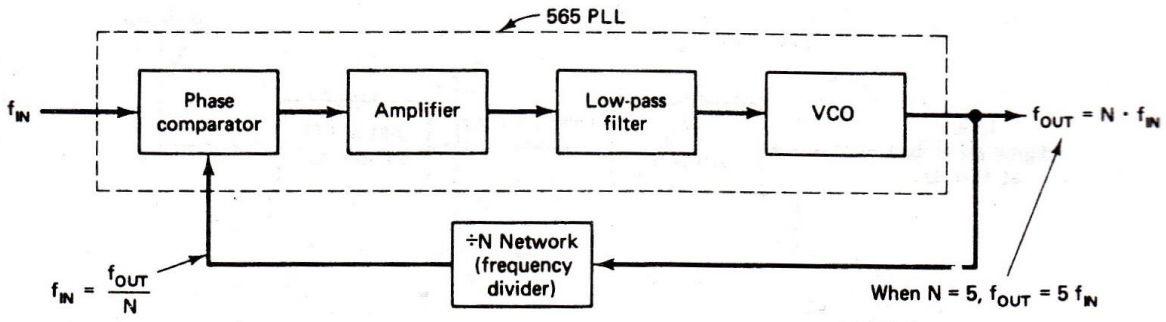
Designed circuit is shown below, **2M**



Q.5 Attempt any Four of the following: **16M**

a) Draw and explain frequency multiplier using PLL**.**

Ans: Diagram: **2M**



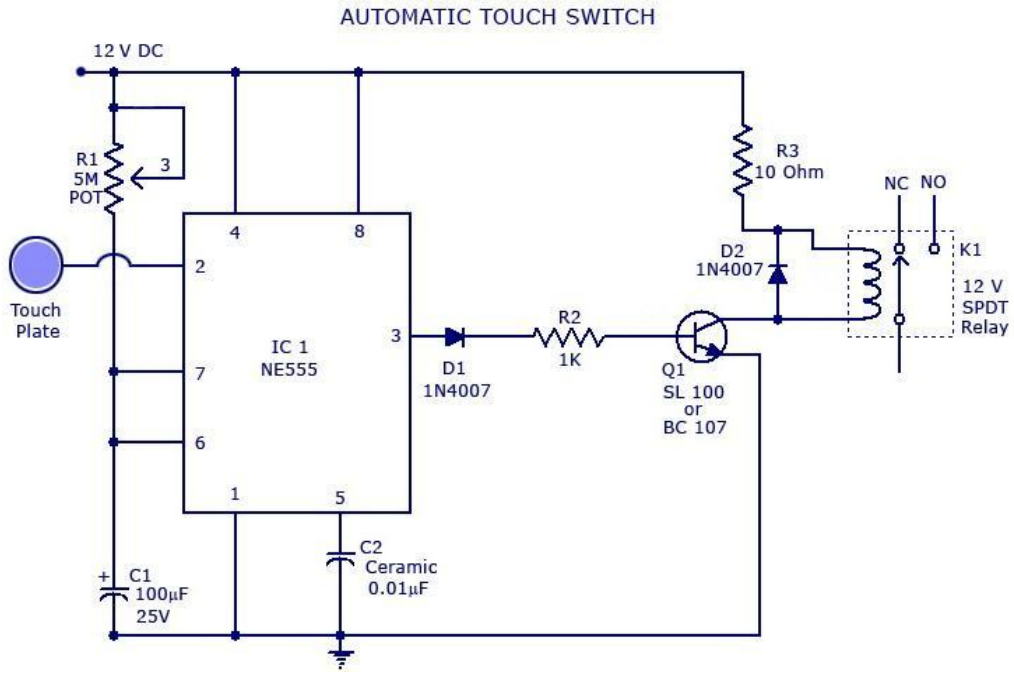
Explanation: **2M**

- A divide by N network frequency divider is connected externally between the VCO output and the phase comparator input.
- Since the output of the divider network is locked to the input frequency f_{IN} the VCO is actually running at a multiple of the input frequency. Which is N times f_s

  $F_{OUT} = N. F_{IN}$
- The multiplying factor can be obtained by the proper selection of the scaling factor N of the frequency divider.

b) Draw and explain touch plate using IC 555.

Ans: Diagram: **2M**



Explanation: **2M**

- Touch plate (push to ON) is used to turn on the timer and active the relay.
- As soon as touch plate is switched ON (pushed) a trigger pulse is produced because of the induced voltage of the human body and the output of 555 timer goes high for a time determined by R_1 and C_1.
- The output remains high for a period of $T_{ON} = 1.1 R_1C_1$. The high output of IC 555, activates the transistor Q_1 which in turn energize the relay coil and closes the N.O. (Normally Open) contact of the relay.
- The relay contact can be used to drive the load like motor, light.

c) Identify the given Fig No. 3. How to convert it into VCO? Draw modified circuit and write on what factors the O/P frequency of oscillations depends on.

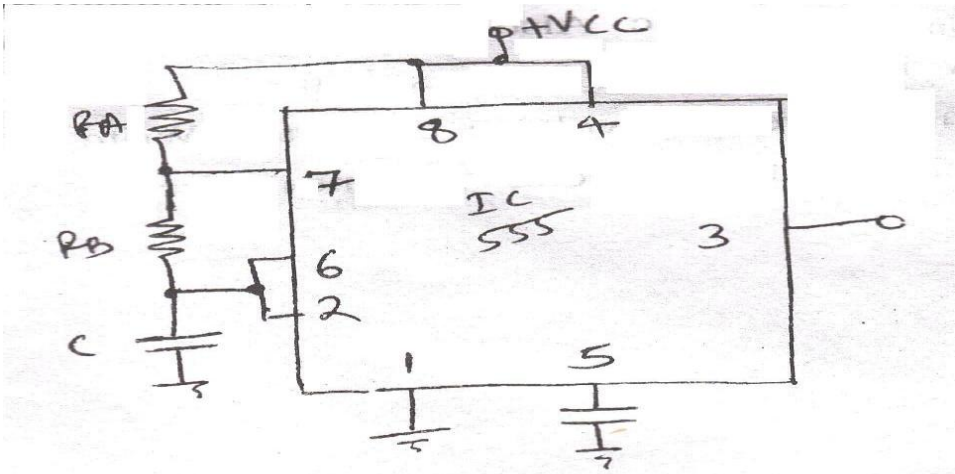
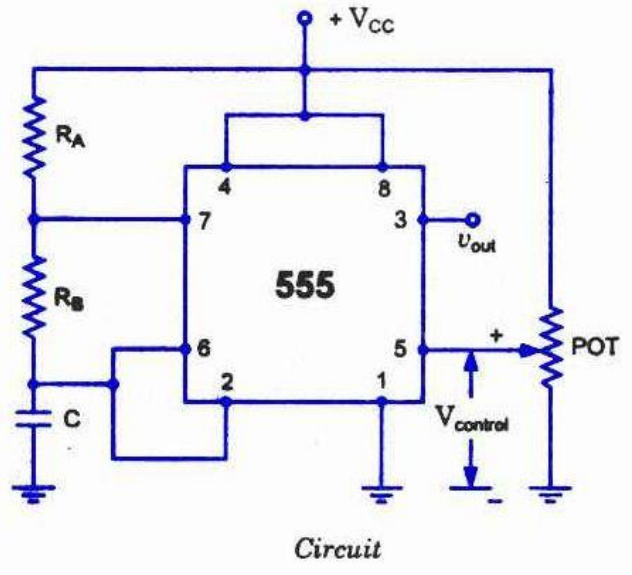


Fig No. 3

Ans: Diagram: **1M**



Circuit

Explanation:

- Fig. is Astable multivibrator using IC 555. **1M**
- It can be converted into a VCO by connecting pin no. 5 to an adjusting control voltage. **1M**

- The output frequency of the astable multivibrator is a function of the control voltage applied at pin no. 5. Hence the circuit works as VCO. **1M**

d) Design astable Multivibrator using IC55 to get O/P waveform as shown in fig. No. 4. Draw designed circuit.

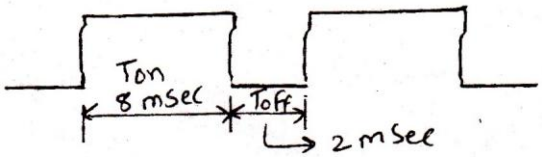
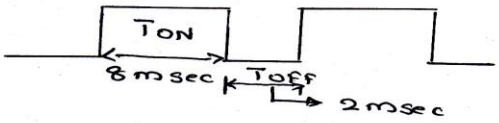


Fig No. 4

Ans: Solution: **3M**



$T_{ON} = 8\ msec$

$T_{OFF} = 2\ msec$

$T_{ON} = 0.69 (R_A + R_B) C$

$T_{OFF} = 0.69\ R_B C$

Step 1 : To Calculate R_A and R_B (03M)

$T_{ON} = 0.69 (R_A + R_B) C$ Assume $C = 0.1 \mu F$

$T_{ON} = 8\ msec = 8 \times 10^{-3}$

$$R_A + R_B = \frac{T_{ON}}{0.69 \times C} = \frac{8 \times 10^{-3}}{0.69 \times 0.1 \times 10^{-6}}$$

$$= \frac{8 \times 10^{3}}{0.069} = 115.9\ K\Omega$$

$T_{OFF} = 0.69\ R_B C$

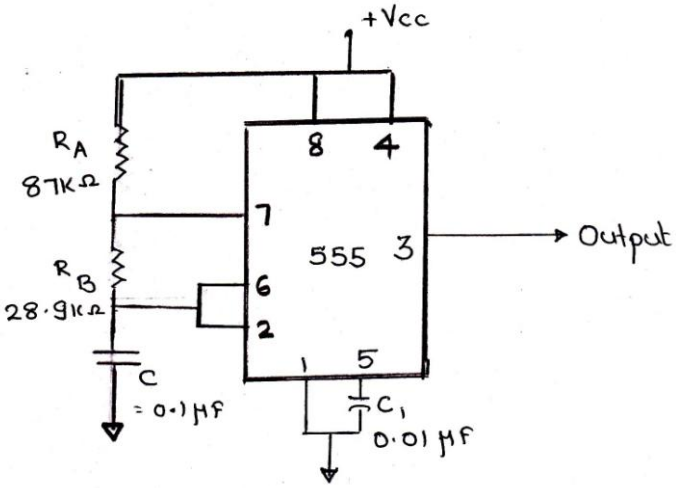
$$R_B = \frac{T_{OFF}}{0.69 \times C} = \frac{2 \times 10^{-3}}{0.69 \times 0.1 \times 10^{-6}}$$

$$= \frac{2 \times 10^{3}}{0.069} = 28.9\ K\Omega$$

$R_A + 28.9 = 115.9$

$R_A = 115.9 - 28.9 = 87\ K\Omega$

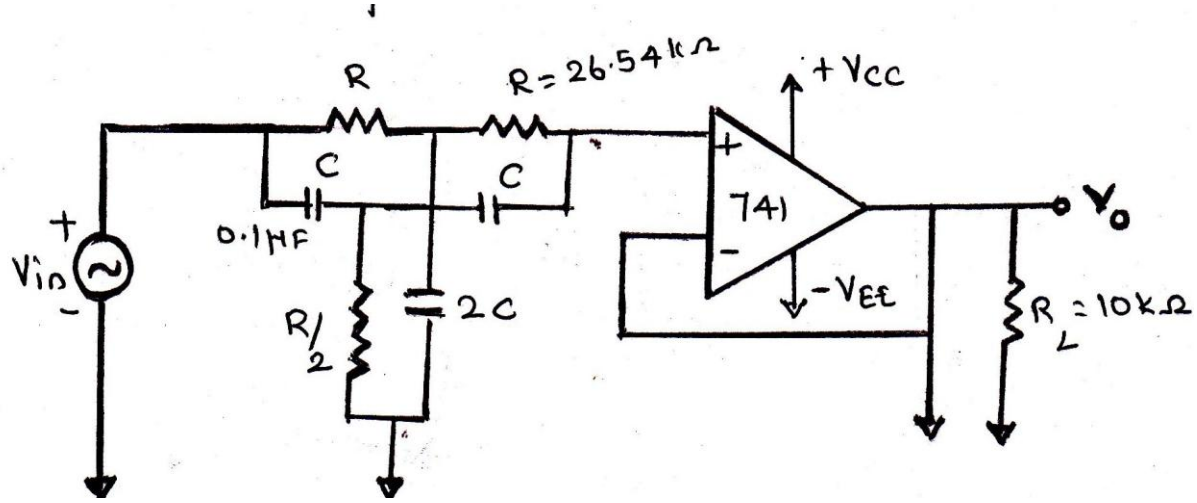
Circuit diagram: **1M**



{Note :- The values of R_A & R_B can be varied as per value of capacitor}

e) Design notch filter for notch frequency of 60Hz. Draw designed circuit with frequency response.

Ans: Circuit diagram: **2M**



Solution: **1M**

Solution

Given $f_N = 60Hz$

$$f_N = \frac{1}{2\pi RC} \quad \text{Let } C = 0.1\mu f$$

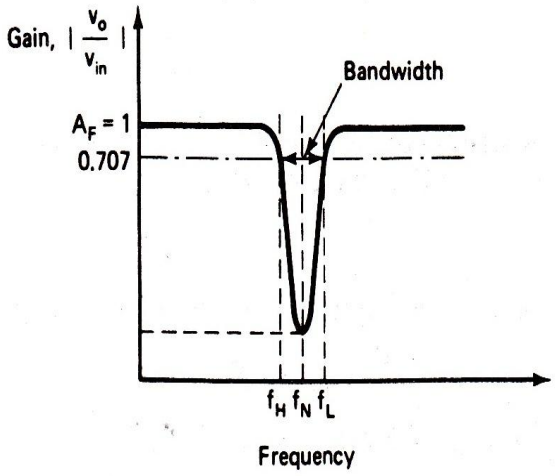
$$R = \frac{1}{2\pi f_N C} = \frac{1}{2\pi \times 60 \times 0.1 \times 10^{-6}}$$

$$= 26.54k\Omega$$

For $R/_2$: Parallel two $26.54k\Omega$ resistors

For 2C component, parallel two $0.1\mu f$ capacitors.

Frequency response: **1M**

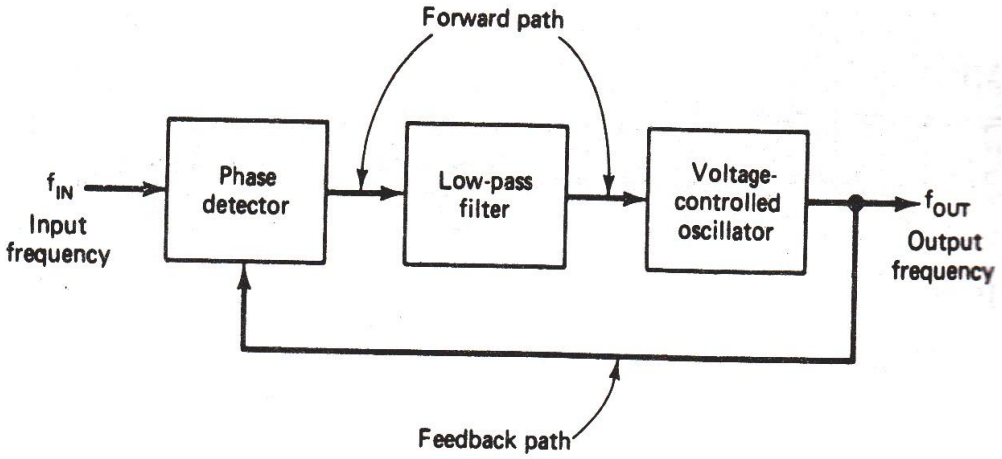


{Note:- Value of R can vary according to value of C}

Q.6 Attempt any four of the following: **16M**

a) Explain block diagram of PLL.

Ans: Block diagram: **2M**



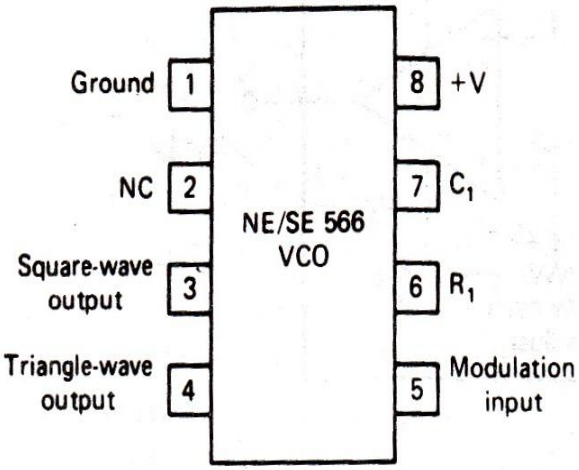
Explanation: **2M**

- The phase locked loop consists of,
  1. Phase detector
  2. Low pass filter
  3. Voltage controlled oscillator
- The phase detector or comparator compares the input frequency F_{IN} with the feedback frequency F_{OUT}.
- The output of the phase detector is proportional to the phase difference between F_{IN} and F_{OUT}. The output voltage of a phase detector is a dc. voltage which is known as error voltage.
- The O/P of the phase detector is applied to the low-pass filter which removes the high frequency noise and produces a dc. level.
- This dc. level is the input to the voltage controlled oscillator (VCO).
- The O/P frequency of the VCO is directly proportional to the input dc. level. The VCO frequency is compared with the input frequencies and adjusted until it is equal to the input frequency.
- The phase locked loop goes through three states,
  1. Free running
  2. Capture
  3. Phase lock
- Before the input is applied the phase-locked loop is in the free running state.

- Once the input frequency is applied the VCO frequency starts to change and the PLL is said to be in capture mode.
- When phase locked, the loop tracks any change in input frequency through its repetitive action.

b) Draw pin diagram and explain pin function of IC 566 [VCO].

Ans: Pin diagram: **2M**



Pin function: **2M**

Pin No. 01 : - Ground

Pin No. 02 : - No connection

Pin No. 03 : - Square wave output

Pin No. 04 : - Triangular wave output

Pin No. 05 : - Modulation input

Pin No. 06 : - R_1

Pin No. 07 : - C_1

Pin No. 08 : - +Vcc (10V – 26V) Ideally 12V is applied.

R_1, C_1 : - External resistor and capacitor which decides the frequency of oscillation of VCO.

Modulating input: - Control voltage.

c) Design monostable multivibrator to get pulse width of 10m sec**.**

Ans: Solution: **2M**

Given, pulse width = 10msec

$T = 1.1R_AC$

Assume $C = 0.1\mu f = 0.1 * 10^{-6} f$

$10X10^{-3} = 1.1 * R_A * 0.1 * 10^{-6}$

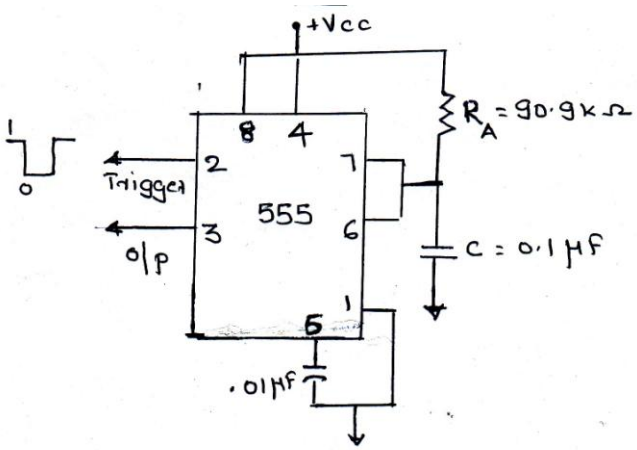
$R_A = 10 * 10^{-3} / 1.1 * 0.1 * 10^{-6}$

$= 10 * 10^3 / 11$

$R_A = 90.9\ k\Omega$

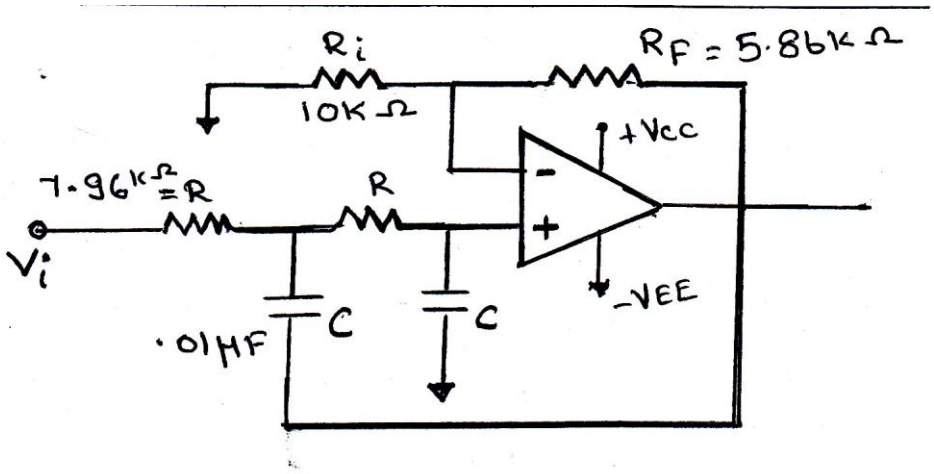
[Note: capacitor value can be assumed 0.01μf or other value find R_A according to that]

Diagram: **2M**



d) Design 2nd order low pass filter with cutoff frequency = 2KHz. Draw designed circuit and frequency response.

Ans: Second order low pass filter: - **1M**



Solution:

Given, f_H = 2KHz let C = 0.01μf

Step 1 : to calculate R **1M**

$f_H = 1 / 2\pi RC$

$R = 1 / 2\pi f_H C$

$$R = \frac{1}{2\Pi * 2 * 10^3 * 0.01 * 10^{-6}}$$

R = 7.96 kΩ

Step 2: to calculate R_f and R_i **1M**

Pass band gain = 1.586

$1.586 = 1 + R_f / R_i$

$R_f / R_i = 1.586 - 1$

$= 0.586$

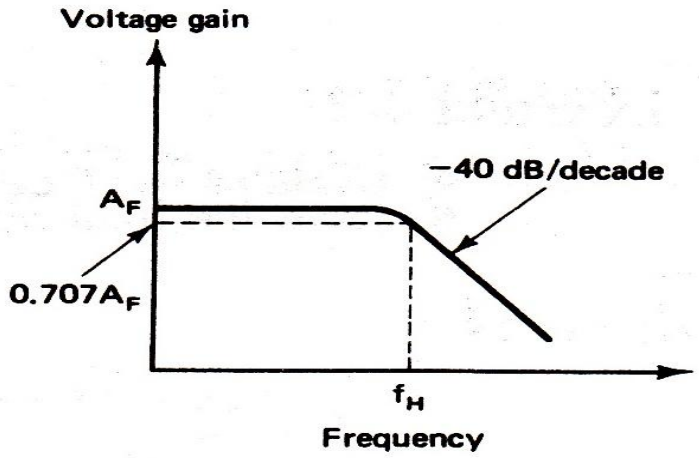
Let R_i = 10kΩ

$R_f = 0.586 * 10$

$= 5.86k\Omega$

[Note: C and R_i can take other values, $C \leq 1\mu_f$, $R_i \leq 100k\Omega$. calculate R and R_F according to that.]

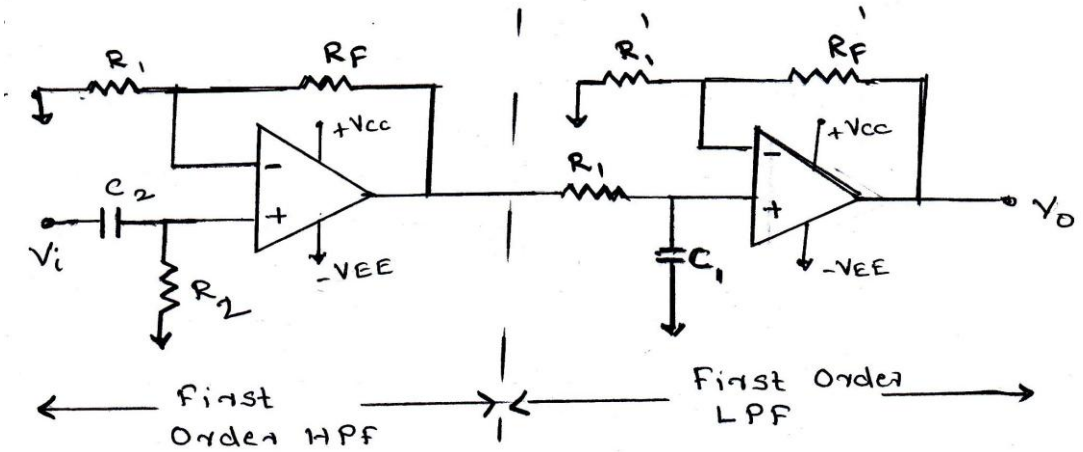
Frequency Response: **1M**



e) Design wide band pass filter with lower cut-off frequency = 400Hz and higher cutoff frequency of 1 KHz and Pass band gain = 4.

Ans: ***[Note: 2 marks for diagram, 1 mark for design of LPF, 1 marks for design of HPF]***

Diagram:



Solution:

Solution:

Step 1: Design of Low Pass Filter.

$f_H = 1\ kHz$

Let $C_1 = 0.01\ \mu F$ [Capacitor can take any value $\leq 1\ \mu F$)

$f_H = \frac{1}{2\pi R_1 C_1}$ $\quad R_1 = \frac{1}{2\pi f_H C_1}$

$= \frac{1}{2\pi \times 1\times10^{3} \times 0.01\times10^{-6}}$

$= 15.9\ k\Omega$

Since the pass band gain is 4

Gain of LPF = 02

Gain of HPF = 02

Gain $= 1 + \frac{R_F'}{R_1'} = 2$

$\frac{R_F'}{R_1'} = 2 - 1 = 1$ $\quad R_F' = R_1' = 10\ k\Omega$ (Assume)

Components of Low Pass Filter are

$R_1 = 15.9k\Omega$	$R_F' = 10k\Omega$
$C_1 = 0.01\mu F$	$R_1' = 10k\Omega$

Step 2 Design of High Pass Filter

$f_L = 400Hz$

$f_L = \frac{1}{2\pi R_2 C_2}$ Let $C_2 = 0.05\mu F$

(C_2 can assume $0.01\mu F$ also)

$R_2 = \frac{1}{2\pi f_L C_2}$

$= \frac{1}{2\pi \times 400 \times 0.05 \times 10^{-6}}$

$= 7.96k\Omega$

$C_2 = 0.01\mu F$

$R_2 = \frac{1}{2\pi f_L \times 0.01}$

$= \frac{1}{2\pi \times 400 \times .01 \times 10^{-6}}$

$= 39.8k\Omega$

Pass Band Gain = 2

$1 + \frac{R_F}{R_1} = 2$

$\frac{R_F}{R_1} = 2 - 1 = 1$ $R_F = R_1 = 10k\Omega$

Components of HPF

$C_2 = 0.05\mu F$	$R_F = 10k\Omega$
$R_2 = 7.96k\Omega$	$R_1 = 10k\Omega$

If $C_2 = 0.01\mu F$ $R_2 = 39.8k\Omega$ $R_F = R_1 = 10k\Omega$