Q 1) Attempt any TEN of the following. (20 marks)

a) Any 2 difference **(1 mark for each difference)**

Sr.No	Analog Signal	Digital Signal
1	Analog signal has continuous values	Digital Signals have discrete values
2	More affected by noise	Less affected by noise
3	Sine Wave is an example	Square wave is an example
4	Cannot be controlled by computer	Can be controlled by computer

b) Fan in: is the maximum no of inputs a gate can handle. **(01m)**

Figure of merit: is the product of propagation delay time and power dissipation in logic families. **(01m)**

c) i) (372)8 = (11 111 010) **(01m)**

ii) (546) 8 = (101 100 110) **(01m)**

d)

i) 101110 **(01m)**

is complement = 101110

= 010001

+ 1

010010

ii) 101010 **(01m)**

is complement = 010101

+ 1 1

.010110

e) $(39)_{10}$ = (00111001) BCD **(01m)**

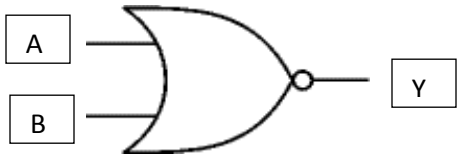
$(47)_{10}$ = (0100 0111) BCD **(01m)**

f) 101011 **(02m)**

\+ 110010

1011110

g) NOR gate symbol **(01m)**



Truth table **(01m)**

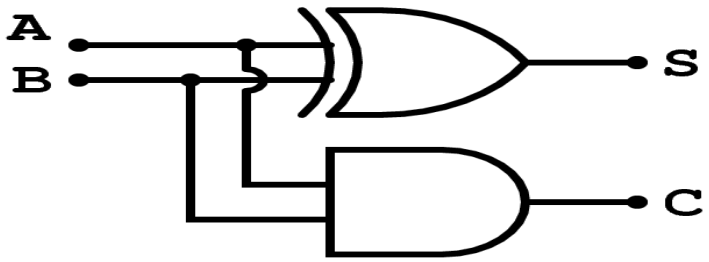
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

h) Flip flop is bistable device used to store one bit value either 0 or 1. Hence called a basic memory cell.

i) Truth table **(01m)**

A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Logic Diagram **(01m)**



j)

Based on fabrication technology memories are classified as

i) Bipolar (e. g. SRAM, ROM, PROM.)
ii) Unipolar (MOS) (e. g. RAM, EPROM, EAPROM)

k) (01 m for each point)

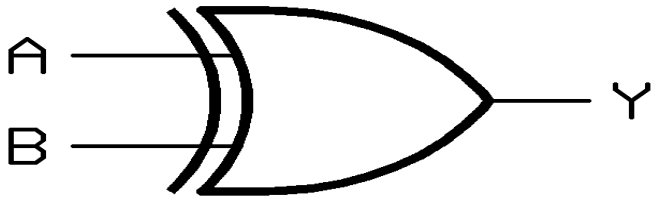
1) Counters are used to count no of clock pulse to count no of times the event occurring.

2) Used in digital multimeter

l) De Morgan's first theorem states that complement of sum of variable is equal to product of individual variables. E. g. $\overline{A+B} = \overline{A}\ \overline{B}$

Q. 2. Attempt any FOUR of the following. (16 marks)

a) Symbol **(01m)**



Logic expression $Y = A \oplus B$ **(01m)**

Truth table **(02m)**

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

b)

i) $(0111)_2 - (1011)_2$ **(02m)**

A – B, find 2's complement of B

Is complement = 0100

Add 1 1

0101

Add A 0111

\+ 0101

1100

If there is no carry answer is – ve and is in 2's complement form.

Answer is - 0100.

ii) 1010 – 1000 **(02m)**

Find 2's complement of 1000

0111

\+ 1

1000

Add 1010,

1000

+ 1010

---

1 0010.
Discard the carry, the remaining its gives the +ve answer
Answer is + 0010.

c)

i) 1024 **(01m)**

Octal

8	1024
8	128 -- 0
8	16 -- 0
8	2 -- 0
	0 -- 2

1024 = $(2000)_8$

Hexadecimal **(01 m)**

16	1024
16	64 -- 0
16	4 -- 0
	0 -- 4

1024 = $(400)_{16}$

ii) 98

Octal **(01 m)**

8	98
8	12 -- 2
8	1 -- 4
	0 -- 1

$98 = (142)_8$

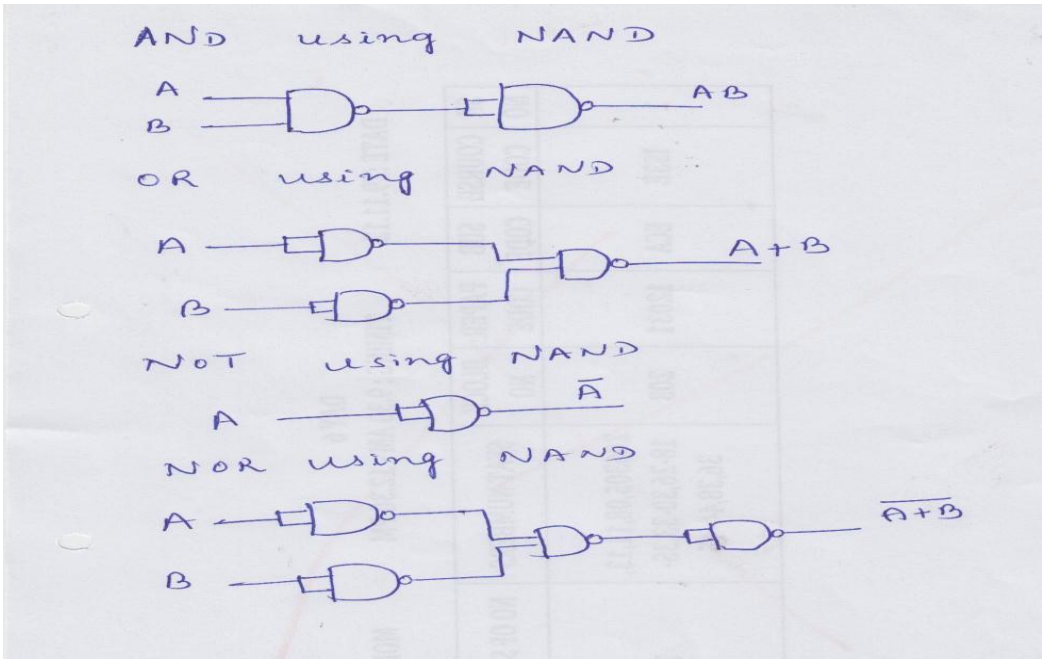
Hexadecimal **(01 m)**

98 =

16	98
16	6 -- 2
	0 -- 6

$(62)_{16}$

d) (01m for each diagram)



e) (04 m)

$\bar{y}\,\bar{z} + \bar{w}\,\bar{x}\,\bar{z} + \bar{w}\,x\,y\,\bar{z} + w\,y\,\bar{z}$

$\bar{y}\,\bar{z} + \bar{w}\,z\,(\bar{x} + x\,y) + w\,y\,\bar{z}$

$\bar{y}\,\bar{z} + \bar{w}\,z\,(\bar{x} + y) + w\,y\,\bar{z}$

$\bar{y}\,\bar{z} + \bar{w}\,z\,\bar{x} + \bar{w}\,z\,y + w\,y\,\bar{z}$

$\bar{y}\,\bar{z} + \bar{w}\,\bar{x}\,\bar{z} + y\,\bar{z}\,(\bar{w} + \bar{w})$ . . $\bar{w} + w = 1$

$= \bar{y}\,\bar{z} + w\,\bar{x}\,\bar{z} + y\,\bar{z}$

$\bar{Z}\,(\bar{y} + y) + \bar{w}\,\bar{x}\,\bar{z}$ . . $\bar{y} + y = 1$

$= \bar{z} + \bar{w}\,\bar{x}\,\bar{z}$

$= \bar{z}\,(1 + \bar{w}\,\bar{x})$ . . $1 + \bar{w}\,\bar{x} = 1$

$= \overline{z}\ 1$

$= \overline{z}$

f)

$(7)_{10} + (4)_{10}$

0111

\+ 0100

1011

\+ 0110 (Since invalid BCD add 6 = 0110)

---

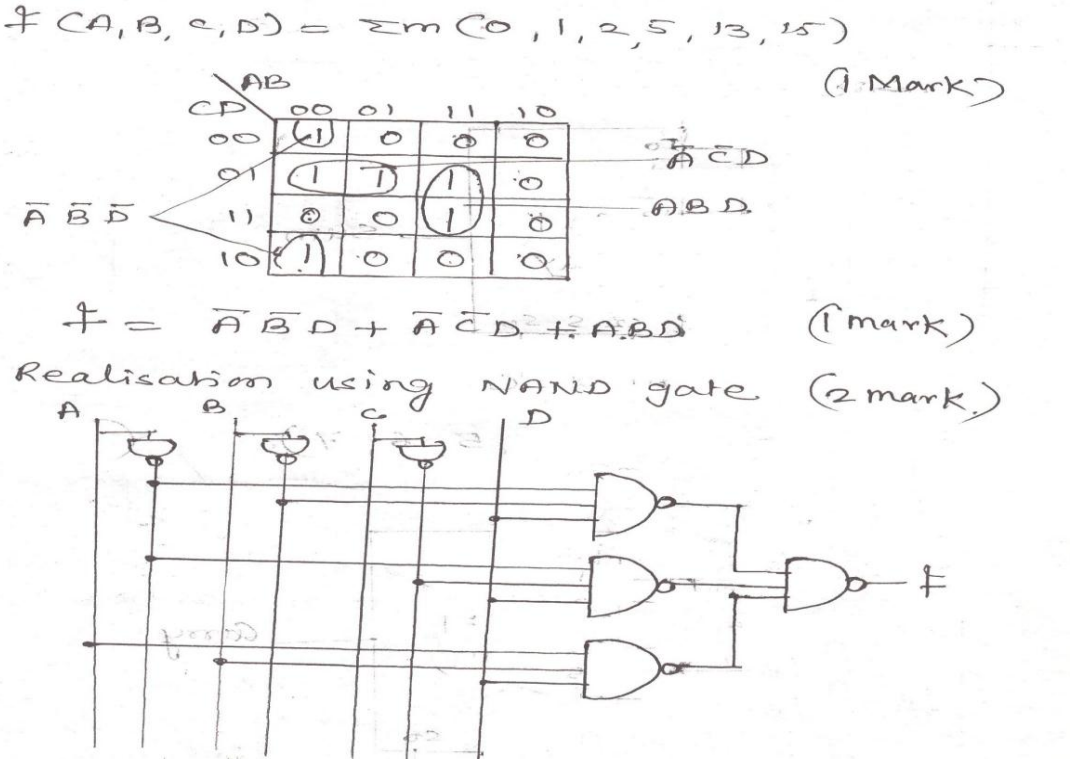
1 0001

Answer in 1 0001 = 1 1.

Q3. Attempt any four of the following **(16 marks)**

a)

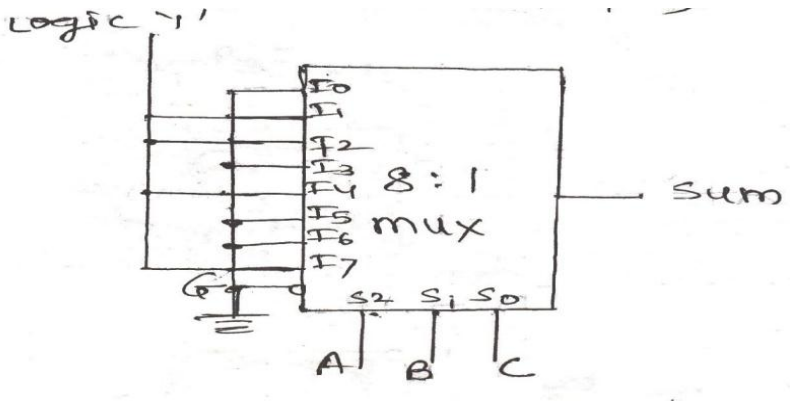
NAND – NAND realization



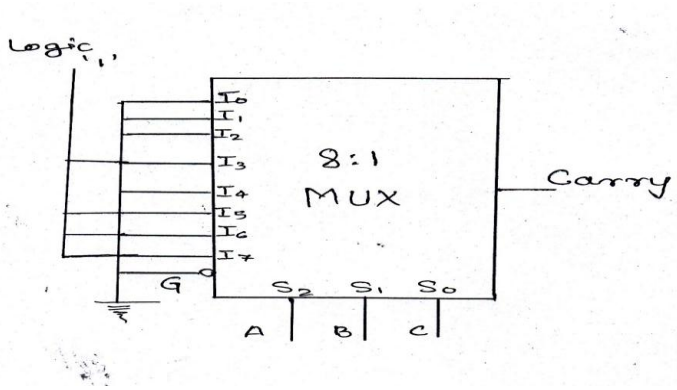
b) Truth table of full adder **(01 mark)**

A	B	C	Sum	Carry~
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Multiplexer required is 8:1 multiplexer
Equation for sum = ∑m (1, 2, 4, 7)
Carry = ∑m (3, 5, 6, 7)
Sum = ∑m (1, 2, 4, 7) **(1 ½ marks)**



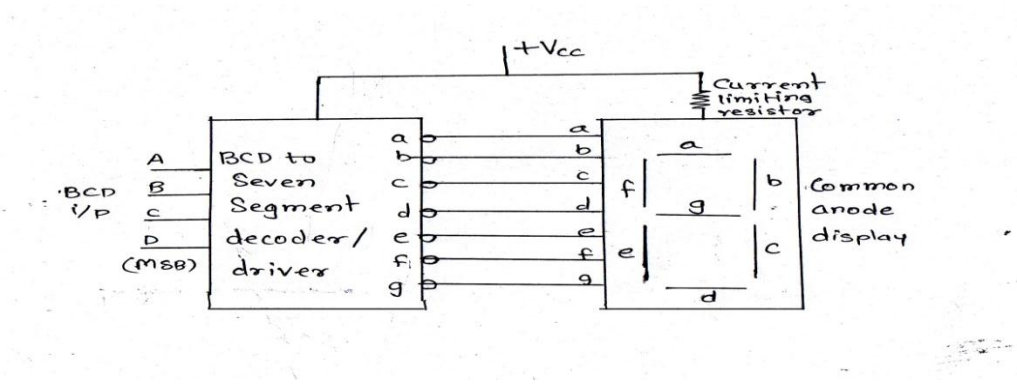
Carry = ∑m (3, 5, 6, 7) **(1 ½ marks)**



c) BCD to seven segment Decoder

(1 ½ marks for circuit diagram,1 ½ marks for truth table, 01 mark for explanation)

- Marks can be given to common cathode display circuit diagram and corresponding truth table

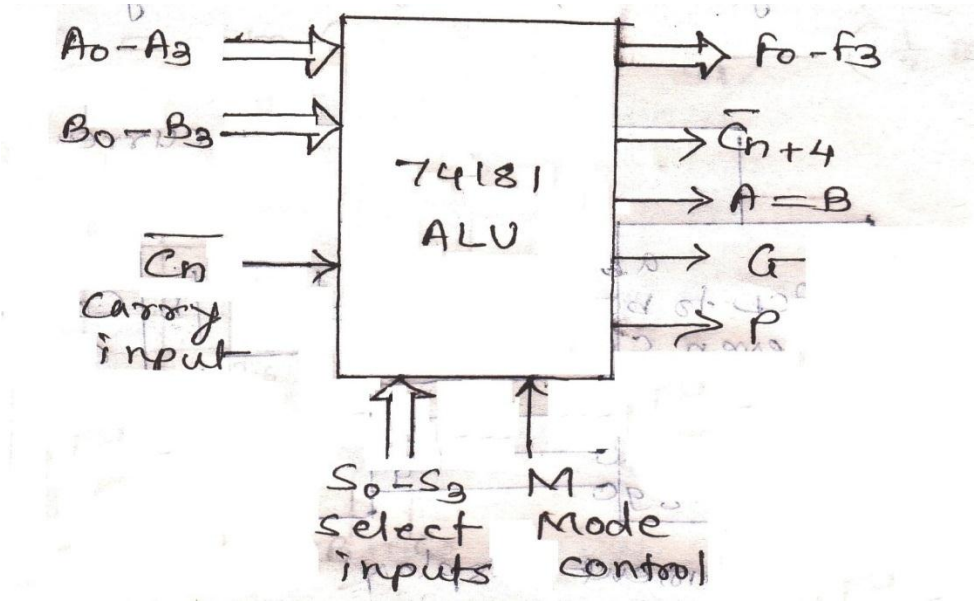


Seven segments is the device used as display device in digital system for displaying the data we have to convert the data from BCD to seven segment code. This is done by BCD to seven segment decoder / driver ICs. It has four input lines for BCD data and seven output lines to drive a seven segment display (active low output lines for common anode display and active high output lines for common cathode display) output terminals a through g of the decoder are to be connected to a through g terminals of display respectively, to make the particular segment ON or OFF as shown in truth table below.

BCD Input				7 – segment output (active low)						
D	C	B	A	a	b	c	d	e	f	g
0	0	0	0	0	0	0	0	0	0	1
0	0	0	1	1	0	0	1	1	1	1
0	0	1	0	0	0	1	0	0	1	0
0	0	1	1	0	0	0	0	1	1	0
0	1	0	0	1	0	0	1	1	0	0
0	1	0	1	0	1	0	0	1	0	0
0	1	1	0	1	1	0	0	0	0	0
0	1	1	1	0	0	0	1	1	1	1
1	0	0	0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	1	1	0	0

d) Block diagram of ALU 74181 **(04 marks)**

(02 marks for diagram and 02 marks for pin description)

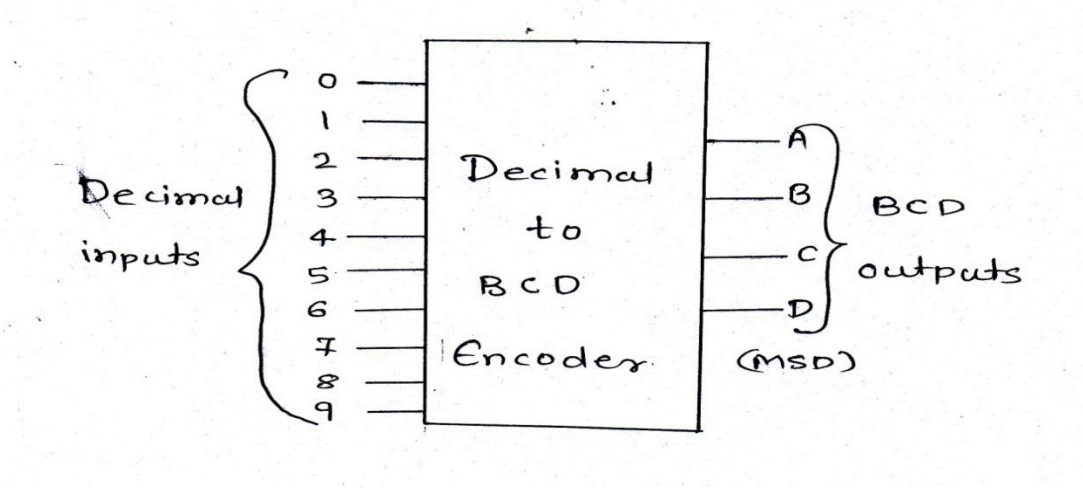


Pin Name	Description
$A_0 – A_3$	4 bit operand input
$B_0 – B_3$	4 bit operand input
$S_0 – S_3$	function select input
M	M=Mode control input
$\overline{Cn}$	$\overline{Cn}$ = Carry input (active low)
$f_0 – f_3$	4 bit function output
A = B	Comparator output
G	Carry generate output
P	Carry propagate output
$\overline{Cn + 4}$	Carry output (active low)

e) Decimal to BCD encoder

(02 mark explain + 02 marks for truth table)

Marks can be given for active low input and active low output truth table also



One of the most commonly used input device for a digital system is a set of ten switches, one for each numeral between 0 to 9. These switches generate 1 or 0 logic levels in response to turning them OFF or ON. When a particular number is to be fed to the digital circuit in BCD code the switch corresponding to that number is pressed. The block diagram is as shown above and truth table for active high input and active high output is as shown below.

Active High Input										Active high Output			
0	1	2	3	4	5	6	7	8	9	D	C	B	A
1	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	0	0	0	1	0	0
0	0	0	0	0	1	0	0	0	0	0	1	0	1
0	0	0	0	0	0	1	0	0	0	0	1	1	0
0	0	0	0	0	0	0	1	0	0	0	1	1	1
0	0	0	0	0	0	0	0	1	0	1	0	0	0
0	0	0	0	0	0	0	0	0	1	1	0	0	1

f) Convert into Standard Sop form

i) $AC + CD + BC$

$= AC(B+\bar{B})(\bar{D}+D) + (A+\bar{A})(B+\bar{B})CD$

$+ (A+\bar{A})(D+\bar{D})BC$ ....(1 marks)

$= ABCD + ABC\bar{D} + A\bar{B}CD + A\bar{B}C\bar{D} + ABCD$

$+ A\bar{B}CD + \bar{A}BCD + \bar{A}\bar{B}CD + ABCD + ABC\bar{D}$

$+ \bar{A}BCD + \bar{A}BC\bar{D}$ .... ($\frac{1}{2}$ mark)

$= ABCD + ABC\bar{D} + A\bar{B}CD + A\bar{B}C\bar{D} + \bar{A}BCD + \bar{A}\bar{B}CD + \bar{A}BC\bar{D}$

ii) $\bar{A}(B+\bar{C})$ ($\frac{1}{2}$ mark)

$= \bar{A}B + \bar{A}\bar{C}$

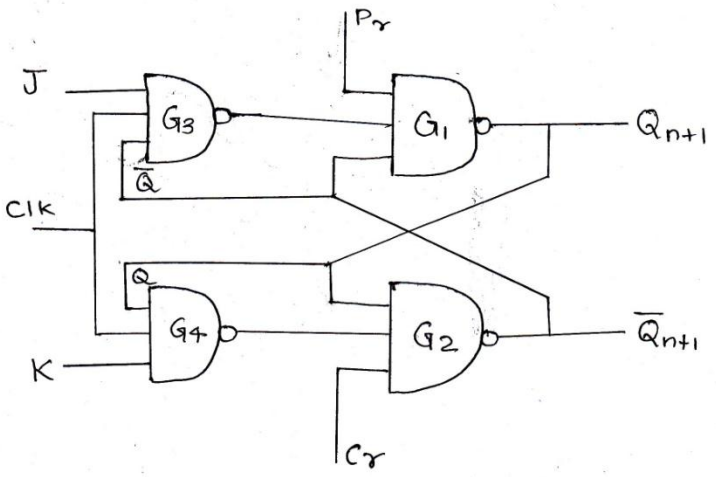
$= \bar{A}B(C+\bar{C}) + \bar{A}\bar{C}(B+\bar{B})$ .... (1 mark)

$= \bar{A}BC + \bar{A}B\bar{C} + \bar{A}B\bar{C} + \bar{A}\bar{B}\bar{C}$

$= \bar{A}BC + \bar{A}B\bar{C} + \bar{A}\bar{B}\bar{C}$ .... (1 mark)

Q4) Attempt any four of the following

a) JK Flip-flop using NAND gates only.



Truth Table

CLK	J	K	Q_{n+1}	
0	X	X	Q_n	No change
1	0	0	Q_n	No change
1	0	1	0	Reset
1	1	0	1	Set
1	1	1	$\overline{Q_n}$	Toggle

The clock signal is applied to clk input. NAND gates G1 &G2 form an SR latch. The other two NAND gates G3 & G4 have three inputs which are J,Q and clk and K,Q and clk respectively.

If clk=0 then Flip-flop is disabled and o/p Q and $\overline{Q}$ do not change.

If clk=1 and J=K=0 then $S^1=R^1=1$ and the o/p $\overline{Q}$ and Q will not change their state. If J=0 and K=1 then JK Flip-flop will reset and $\overline{Q}$=0 and Q =1 .

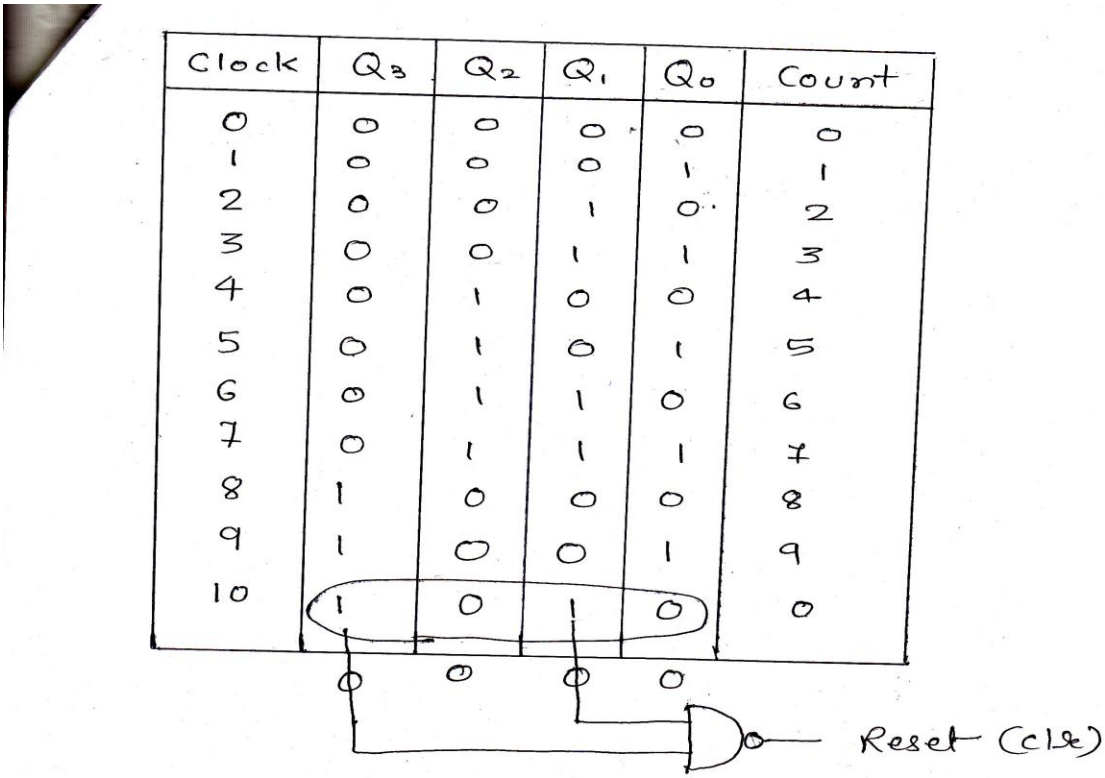
If J=1 and K=0 then output will set and Q=1 and $\overline{Q}$=0.

If J=1 and K=1 then Q and $\overline{Q}$ outputs are inverted and flip-flop will toggle.

b) Mod-10 asynchronous counter **(3marks ckt dig. + 1 mark truth table)**

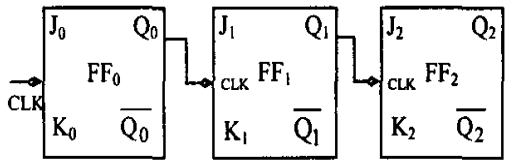
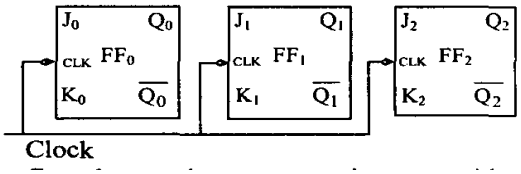
For design of mod-10 counter, four flip-flops are required. As it is asynchronous counter all the flip-flops are not clocked simultaneously JK or T flip-flops can be used. Count sequence is as shown below.

Clock	Q_3	Q_2	Q_1	Q_0	Count
0	0	0	0	0	0
1	0	0	0	1	1
2	0	0	1	0	2
3	0	0	1	1	3
4	0	1	0	0	4
5	0	1	0	1	5
6	0	1	1	0	6
7	0	1	1	1	7
8	1	0	0	0	8
9	1	0	0	1	9
10	1	0	1	0	0



(**Marks to be awarded for K- Map based approach also for design of CLR logic**)

c) Compare synchronous and asynchronous counter. **(Any 4 points -4 marks)**

No.	Asynchronous Counter	Synchronous Counter
1.	In an Asynchronous Counter the output of one Flip Flop acts as the clock Input of the next Flip Flop.	In a Synchronous Counter all the Flip Flop's are connected to a common clock signal.
2.	Speed is Low	Speed is High
3.	Only JK or T Flip Flop can be used to construct Asynchronous Counter	Synchronous Counter can be designed using JK, RS, T and D Flip Flop.
4.	Problem of Glitch arises	Problem of Lockout
5.	Only serial count either up or down is possible.	Random and serial counting is possible.
6.	Settling time is more	Settling time is less
7.	Also called as serial counter	Also called as Parallel Counter
8.		

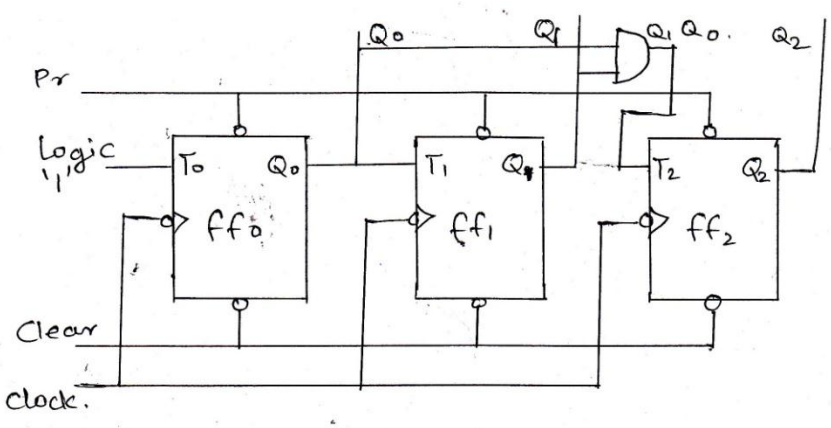
d) 3 bit synchronous counter. **(2 marks circuit diagram + 2 marks explanation)**

(Marks should be given to the circuit diagram by using JK F/F also)

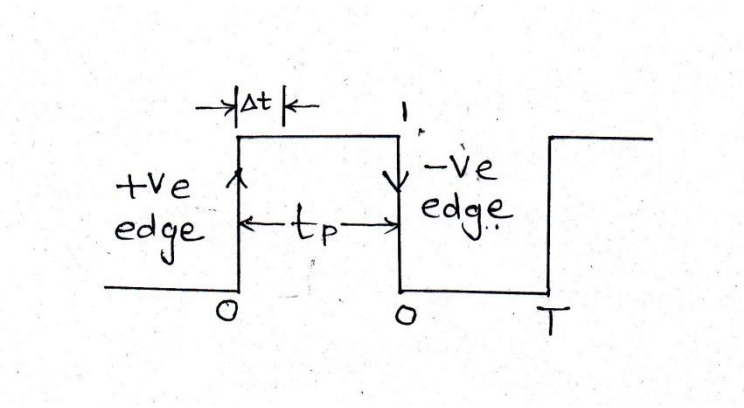
CLK	Q_2	Q_1	Q_0	Count
0	0	0	0	0
1	0	0	1	1
2	0	1	0	2
3	0	1	1	3
4	1	0	0	4
5	1	0	1	5
6	1	1	0	6
7	1	1	1	7
8	0	0	0	0

For three bit synchronous counter, 3 flip-flops are used which are clocked simultaneously. If we observe the count sequence, The output Q_0 of least significant flip-flop changes for every clock pulse. This can be achieved using a T-flip-flop with T_0=1 or JK F/F with J_0=K_0=1. The o/p Q_1 changes whenever Q_0 changes from 1 to 0. Therefore o/p Q_0 is connected T_1 input, Q_0 will change from 1 to 0(or 0 to 1). When Q_0 =1 (T_1 =1) otherwise remain unaffected. Similarly, we observe that, Q_2

changes whenever Q_1 and Q_0 are both 1. This can be achieved by making the T input (T_2) equal to $Q_1 . Q_0$, for JK flip-flops $J_0=K_0=1$, $J_1=K_1= Q_0$ and $J_2=K_2 = Q_1 Q_0$.



e) Race around condition **(1 mark waveform+2 marks explaination+1 mark for How to avoid)**

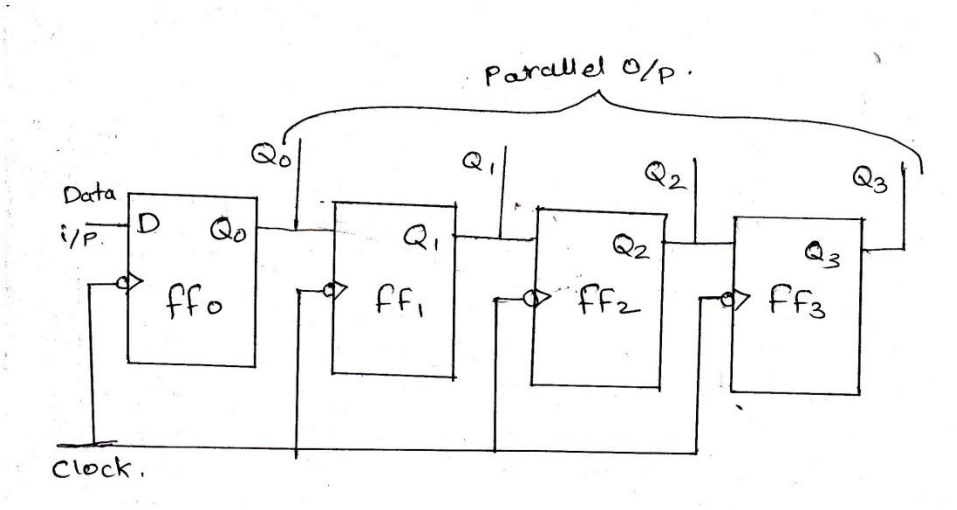


the truth table of JK Flip-flop assumes that the input do not change during the clock pulse ck=1, which is not true because of feedback connection. For ex inputs are J=K=1, and Q_0 =0 and a pulse as shown in fig. above is applied at the clock i/p i.e. ck=1. After a time interval Δt equal to propagation delay through two NAND gates to series the output will change to Q = 1. Now we have J=K=1 and Q =1 and after another time interval Δt the output will change back to Q =0. Hence output will oscillate in between 0 to 1 when ck=1 and at the end of clock pulse output is uncertain. This is Race around condition.

How to avoid

The Race around condition can be avoided if $t_p<\Delta t<T$. however it is difficult because of very small propagation delays. Another method is to use master-slave combination to overcome the drawback of Race around condition in JK F/F.

f) 4 bit SIPO shift register with truth table **(circuit table 1*1/2marks+ explain 1*1/2marks+ truth table 1 marks)**



In serial In Parallel Out shift register, data is shifted in serially, but shifted out in parallel. The data bits are entered into the register serially from data input. In order to shift the data out in parallel, it is simply necessary to have all the data bits available as outputs at the same time this is done by connecting the output of each flip-flop to an output pin. Once the data bits are stored, each bits appears on its respective output line and all bits are available simultaneously.

Truth Table

CLK	Data i/p	Q_3	Q_2	Q_1	Q_0
0	1	0	0	0	1
1	1	0	0	1	1
2	1	0	1	1	1
3	1	1	1	1	1

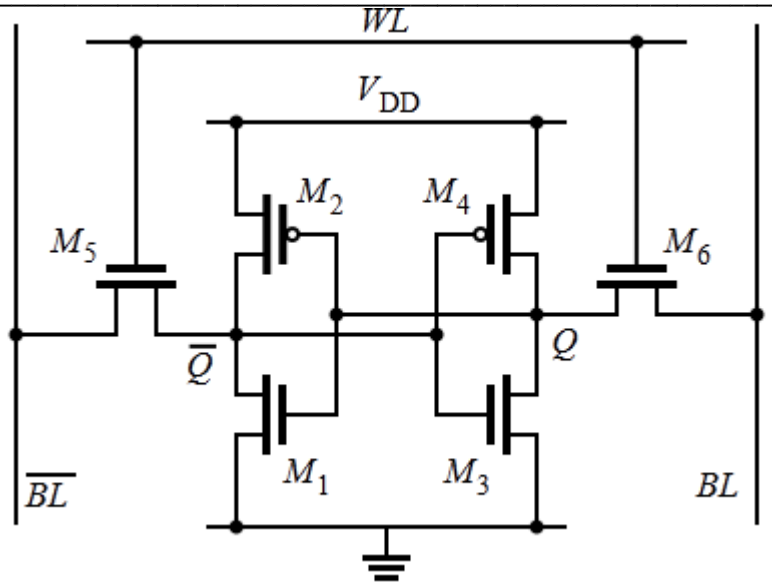
Q5)

a) Working of MOS RAM Cell with suitable circuit diagram

Ans. SINCE IT IS NOT MENTIONED IS IT MOS RAM Cell (STATIC or DYNAMIC) marks to be awarded for any 1

(2 marks for diagram+ 2 marks for explanation)

MOS STATIC RAM CELL



Each bit in an SRAM is stored on four transistors (M1, M2, M3, M4) that form two cross-coupled inverters. This storage cell has two stable states which are used to denote **0** and **1**. Two additional *access* transistors serve to control the access to a storage cell during read and write operations. A typical SRAM uses six MOSFETs to store each memory bit. In addition to such 6T SRAM, other kinds of SRAM chips use 8T, 10T, or more transistors per bit.

Access to the cell is enabled by the word line (WL in figure) which controls the two *access* transistors M_5 and M_6 which, in turn, control whether the cell should be connected to the bit lines: BL and BL. They are used to transfer data for both read and write operations.

During read accesses, the bit lines are actively driven high and low by the inverters in the SRAM cell. The size of an SRAM with *m* address lines and *n* data lines is 2^m words, or $2^m \times n$ bits.

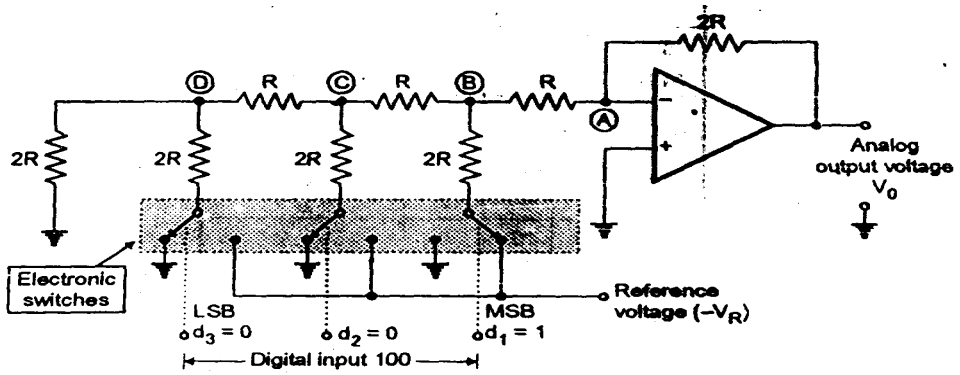
b) Differentiate between RAM and ROM

Ans.... **(any 4 points- 1 mark for each difference)**

Sr. No	**RAM**	**ROM**
1	Random Access Memory	Read Only Memory
2	It is a temporary type of storage.	It is a permanent type of storage.
3	It is used for reading and writing data.	It is used for reading data only
4	The various RAM types are SRAM,DRAM	The various ROM types are PROM, EPROM, EEPROM
5	The various applications are calculator, computer etc.	The various applications are calculator, microprocessors etc.

c) Working of R-2R ladder DAC. Give the output expression

Ans. (2 marks for circuit diagram, 1 marks for explanation, 1 marks for expression)

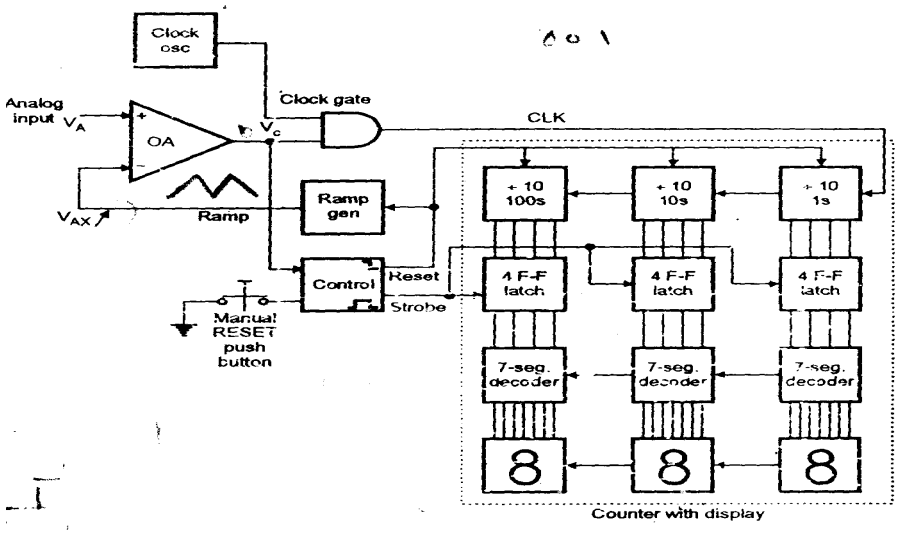


- R-2R Digital to analog converter makes uses of resistors of value R and 2R
- It makes use of the op-amp as a summing amplifier
- The digital input is provided by SPDT switches which connect between 0 and 1
- The output of the resistor network is in terms of current.
- The op-amp is used to convert the current output to voltage output.

Expression $\{V_0 = V_R [d_1 2^{-1} + d_2 2^{-2} + \ldots\ldots\ldots + d_n 2^{-n}]\}$

d) Explain the working of RAMP type DAC

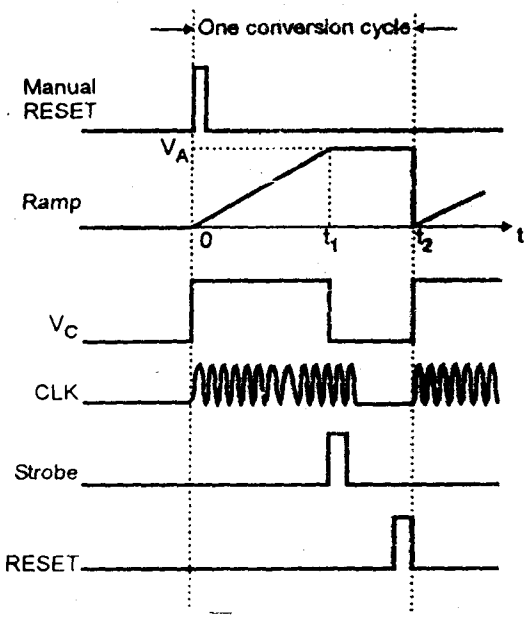
Ans. (2 marks for circuit diagram and 2 marks for working)



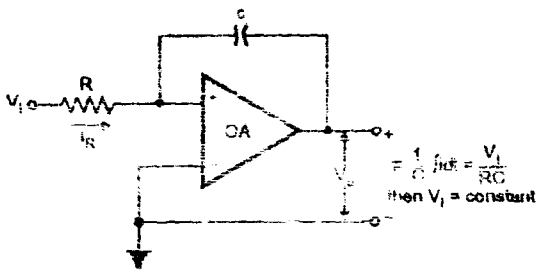
- The single slope ADC consists of a counter with display unit.
- The display unit consists of 7-segment decoder and 7 segment display.
- The circuits also contain a Control block, Ramp generator and OP-AMP as a comparator.
- The output of ramp generator is fed to comparator which compares the same with analog input voltage. Vc (output of comparator) controls the gating to the clock and also informs control circuit about completion of the conversion

WORKING

1. Manual RESET, will reset ramp generator as well as counter.
2. The analog voltage V_A has to be positive. Hence the RAMP begins at 0V.
3. Since $V_{AX} < V_A$, the output of the comparator Vc = 1 (HIGH).
4. This will enable CLOCK gate allowing the CLK input, to be applied to the counter.
5. The ramp generator may make use of counter type ADC or simple integrator.
6. As counter receives clock pulses, it will count up; and the RAMP continues upward. RAMP voltage rises till it reaches to V_A input voltage.
7. When the ramp voltage reaches the input analog voltage, the output Vc= 0 (LOW) and it will disable CLOCK gate and counter cease to advance.
8. The negative transition of Vc simultaneously generates a strobe signal in the CONTROL box that shifts the contents of the three decade counters into the three 4 FF latch circuit.
9. After the generation of STROBE signal, a reset pulse is generated by the CONTROL box that resets the RAMP and clears the decade counter to 0's (ZEROS) and another conversion cycle begins.
10. During this time the contents of the previous conversion, are contained in the latches and are displayed on the seven segment display.



(a) Single slope A/D converter



(b) An integrating circuit

e) State DAC specifications **(any 4 specification – 1 mark each specification)**

1. Resolution of a DAC can be defined in two different ways:

a. Resolution is the number of different analog output voltage values that can be provided by a DAC. For an n-bit DAC

Resolution= 2^n

b. Resolution is defined as the ratio of change in analog output voltage resulting from a change of 1 LSB at the digital input

$$\text{Resolution} = \frac{V_{FS}}{2^n - 1}$$

V_{FS} is defined as the full scale analog output voltage i.e the analog output voltage

when all the digital input with all digits 1.

2. Accuracy

- Accuracy indicates how close the analog output voltage is to its theoretical value. It indicates the deviation of actual output from the theoretical value. Accuracy depends on the accuracy of the resistors used in the ladder, and the precision of the reference voltage used. Accuracy is always specified in terms of percentage of the full scale output that means maximum output voltage

Example:- If the full scale output is 15 V and accuracy is ± 0.1 percent then the

Maximum error is 0.001 x 15 = 0.015V or 15 mV.

3. Linearity

- The relation between the digital input and analog output should be linear.
- However practically it is not so due to the error in the values of resistors used for the resistive networks.

4. Temperature sensitivity

- The analog output voltage of D to A converter should not change due to changes in temperature.
- But practically the output is a function of temperature. It is so because the resistance values and OPAMP parameters change with changes in temperature.

5. Settling time

- The analog output voltage should change instantaneously to the change in digital input.
- Practically the analog output of a D -A converter does not change instantaneously due to the resistors and OP-AMP in the circuit, oscillations are observed at the output.
- The time required to settle the analog output within 1/2 LSB of the final value, after the change in digital input is called as settling time.
- The settling time should be as short as possible.

6. Speed

- It is defined as the time needed to perform a conversion from digital to analog.
- It is also defined as the number of conversions that can be performed per second.
- The speed of DAC should be as high as possible.

7. Long term drift

- Long term drift are mainly due to resistor and semiconductor aging and can affect all the characteristics.

- Characteristics mainly affected are linearity, speed etc.

8. Supply rejection

- Supply rejection indicates the ability of DAC to maintain scale, linearity and other important characteristics when the supply voltage is varied.
- Supply rejection is usually specified as percentage of full scale change at or near full scale voltage at $25^{o}C$

f) Differentiate between statc and dynamic RAM

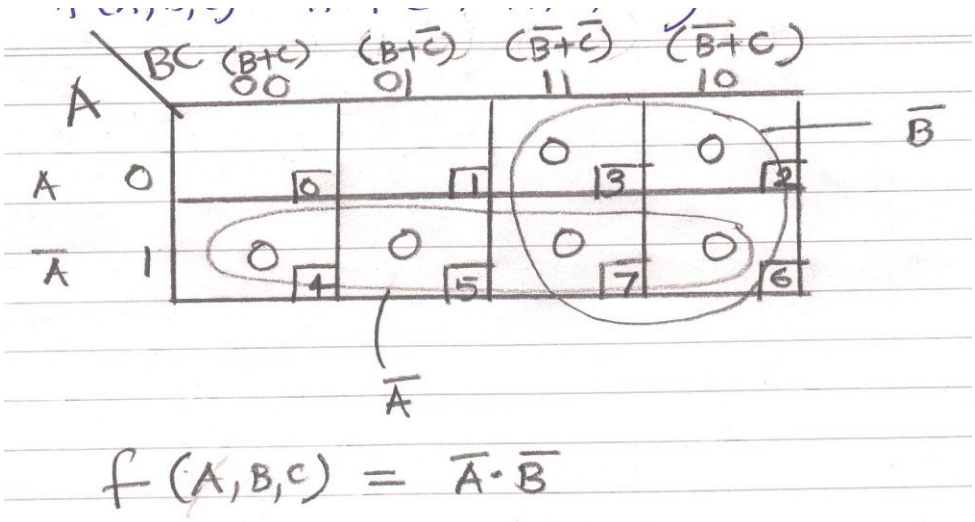
Ans. (Any 4 points- 1 mark for each)

Sr.No	STATIC RAM	DYNAMIC RAM
1	Each SRAM is designed from a flip flop	Each DRAM is designed from a MOSFET and capacitor
2	Refreshing is not required	Refreshing is required
3	Power consumption is less	Power consumption is more
4	Cost is more	Cost is less
5	Access time is less	Access time is more
6	Faster memory	Slower memory

Q6)

a) Solve POS f(ABC)=∏M(2,3,4,5,6,7)

Ans. (2 marks for K-map ,2 marks for output)

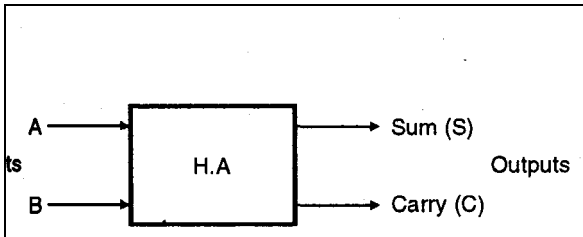


b) half adder truth table logic symbol and circuit

Ans.

(1 mark for explanation , 2 marks for truth table , 1 mark for block diagram)

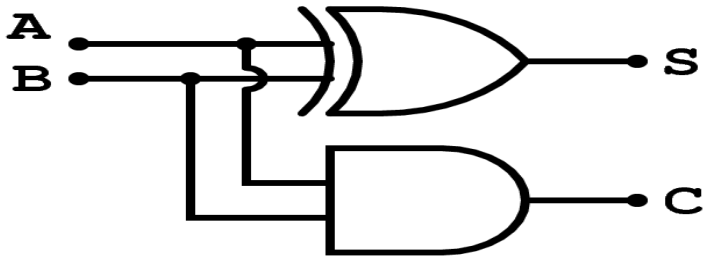
Half adder is a combinational logic circuit with two inputs and two outputs. It is the basic building block for addition of two "single" bit numbers. This circuit has two outputs "carry" and "sum".



(a) Block diagram

Inputs		Outputs	
A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

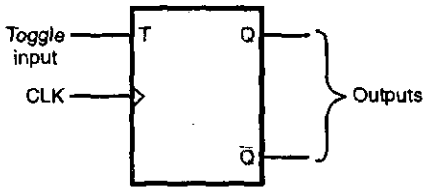
(b) Truth table



c) TRUTH table and symbol T and D flip flop

Ans.

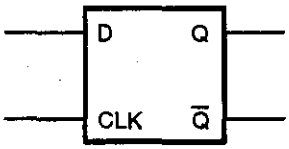
T- Flip FLOP (Toggle Flip Flop) 2 marks



Inputs		Outputs		State
CLK	T	Q_{n+1}	$\bar{Q}_{n+1}$	
↑	0	Q_n	$\bar{Q}_n$	No change

↑	1	$\bar{Q}_n$	Q_n	Toggle

D- Flip FLOP (Delay Flip Flop) -2marks



Inputs		Outputs		Comment
Clock	D	Q_{n+1}	$\bar{Q}_{n+1}$	
0	×	Q_n	$\bar{Q}_n$	No change (NC)
1	0	0	1	Reset condition
1	1	1	0	Set condition

d) advantages and disadvantages of dual slope

Ans. (3 marks for advantages and 1 mark for disadvantage—1 mark each point)

$$V_A = \frac{N \times V_{ref}}{T_1 \times f}$$

1. The expression for VA is independent of N, V_{REF} and T; Thus drifts in any of the components affects T_1 and T_2 in the same proportion and ADC output is unaffected.

2. If T_1 is chosen so that it is related to power supply period, the noise and hum on the input line get largely averaged out. Hence, dual slope ADC is capable of rejecting noise and hum.

3. Offset correction can be introduced by a relatively simple circuit, facilitating auto-zeroi

4. Low cost.

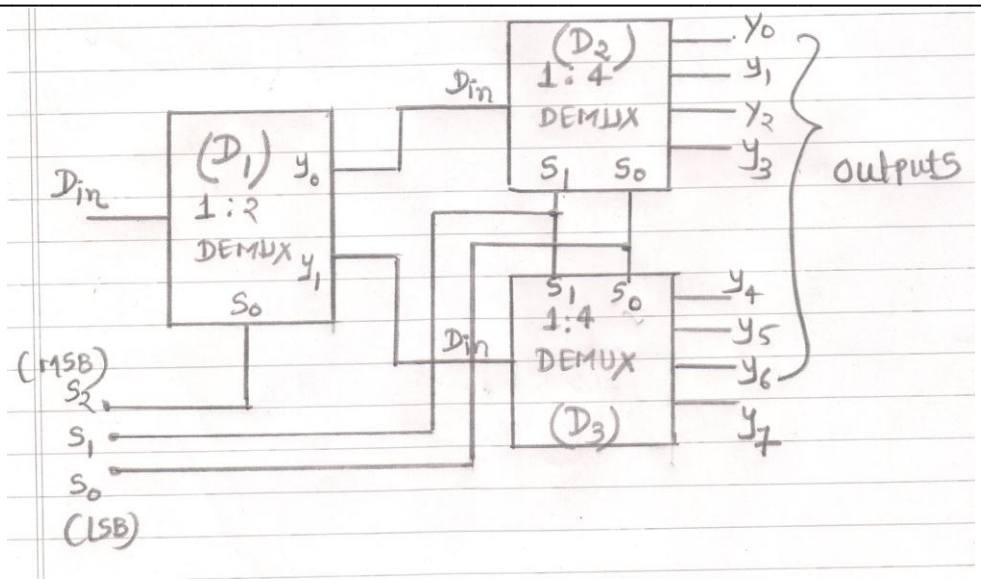
5. Accuracy of the dual-slope ADC can be of the order of 0.05 %, which is adequate for most applications.

Disadvantage of dual slope ADC

The only major drawback of a dual slope type ADC is its long conversion time as compared to other ADCs.

e) design 1:8 using 1:4 demux

Ans.



To design 1:8 demux using 1:4 demux we need 2 demux of 1:4 configuration

f) need for ADC and DAC and write 1 IC number

Ans.

(NEED FOR DATA CONVERTER (2 marks) and 1 mark for each IC number)

- Signals are analog or digital by nature.
- For some applications we need to convert analog signals into their digital equivalent and vice versa.
- Circuits used for such a conversion are called as data converters.
- Most of the physical quantities such as temperature, pressure, displacement, vibrations etc. are available in analog quantities are represented accurately in analog form but it is difficult to process store or transmit the analog because error due to noise is easily introduced in analog.
- Hence to reduce error A to D conversion is necessary.
- After the processing, transmission etc. is done the signal should be converted back to its analog form, for which the D to A conversion is essential.

IC Number for ADC :- IC ADC 0809

IC Number for DAC:- IC DAC 0808