Important Instructions to examiners:

1) The answers should be examined by key words and not as word-to-word as given in the model answer scheme.
2) The model answer and the answer written by candidate may vary but the examiner should assess the understanding level of the candidate.
3) The language errors such as grammatical, spelling errors should not be given importance (Not applicable for subject English and Communication Skills).
4) While assessing figures, examiner may give credit for principal components indicated in the figure. The figures drawn by candidate and model answer may vary. The examiner should give credit for any equivalent figure/figures drawn.
5) Credits to be given step wise for numerical problems. In some cases, the assumed constant values may vary and there may be some difference in the candidate's answers and model answer (as long as the assumptions are not incorrect).
6) In case of some questions credit may be given by judgment on part of examiner of relevant answer based on candidate's understanding.
7) For programming language papers, credit may be given to any other program based on equivalent concept

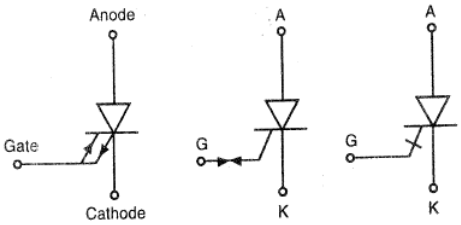
1 a) **Attempt any THREE of the following:** **12**

1 a) (i) Draw the symbol of the following:

1) GTO
2) SUS
3) LASCR
4) IGBT

Ans:

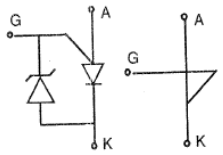
1) GTO:



GTO Symbols

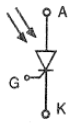
1 mark for any one correct symbol of each device = 4 marks

2) SUS:



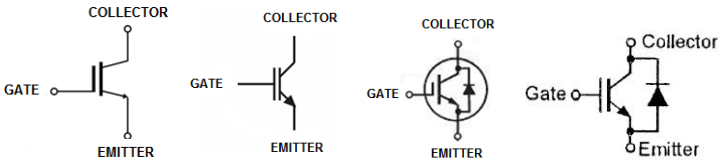
SUS Symbol

3) LASCR:



LASCR symbol

4) IGBT:

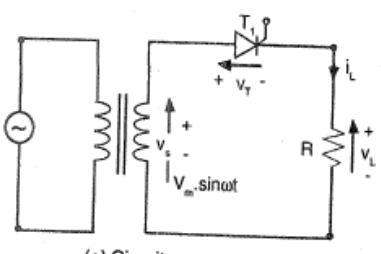


.

1 a) (ii) Draw a neat circuit diagram of single phase fully controlled half wave converter with R load and give its operation.

Ans:

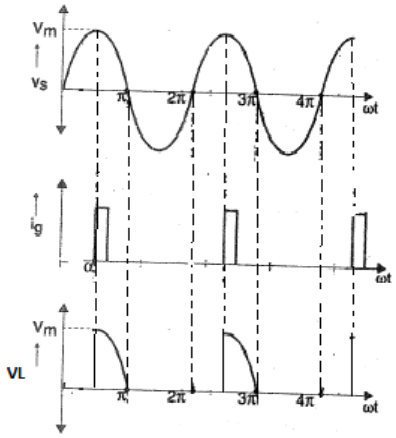
Single-phase Fully-controlled Half-wave converter:



(a) Circuit arrangement

2 marks for circuit diagram

The circuit diagram of 1 ϕ fully controlled half wave converter with resistive load is as shown in the fig. (a). During positive half cycle of input voltage v_s, the thyristor anode is positive with respect to its cathode. Thus thyristor is forward biased. If a short pulse is applied to the gate of the thyristor at ωt = α (here 90°), it is turned on and conducts for rest of the positive half cycle. When the input voltage starts to reverse after ωt = π, thyristor anode becomes negative with respect to its cathode, hence thyristor get reverse biased and is turned off. During off-state of thyristor, the supply voltage v_s appears across thyristor and load voltage remains zero. Thus during each positive half cycle, the supply voltage appears across load resistance from firing instant to end of that half cycle and during negative half cycle, load voltage remains zero.



2 marks for operation (Waveforms are optional)

1a) (iii) State the need of inverter. Give its classification.

Ans:

Need of Inverter:

There are certain situations in which the available AC supply does not satisfy the requirements such as-

2 marks for need

i) Supply reliability without failure (i.e uninterruptible power supply)
ii) Variable voltage
iii) Variable frequency

There are certain situations in which the AC supply is not available, but is required in cases as vehicles etc.

In such situations, the DC supply can be converted to AC as per the requirement. To convert DC supply into AC supply as per the requirement, we need the Inverter.

Classification of Inverters:

A) Classification based on the nature of Input source:

i) Voltage-Source Inverters (VSI)
ii) Current-Source Inverters (CSI)

B) Classification based on type of commutation:

i) Line-commutated inverters
ii) Force-commutated inverters:
   a) Class A: Self-commutated by resonating the load
   b) Class B: Self-commutated by an LC circuit
   c) Class C: C or LC switched by a load carrying SCR
   d) Class D: C or LC switched by an auxiliary SCR
   e) Class E: External pulse commutation

C) Classification based on configuration of the circuit:

i) Series inverter
ii) Parallel inverter

1 mark for each of any two classifications

iii) Bridge inverter:
  a) Half-bridge inverter
  b) Full-bridge inverter

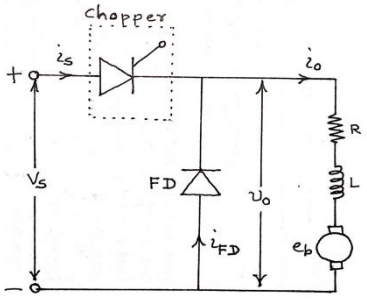
D) Classification based on the Waveshape of Output voltage:
  i) Square-wave inverter
  ii) Quasi-square-wave inverter
  iii) Pulse-width-modulation (PWM) inverter

1 a) (iv) Give the operation of speed control of DC series motor with step down chopper with a neat diagram. Also draw its waveform.

Ans:

Speed control of DC series motor with step down chopper:

Figure shows the basic arrangement for speed control of DC series motor using step down chopper. Armature current is assumed continuous and ripple free. The waveforms for the source voltage V_s, Motor terminal voltage v_0, motor current i_0, dc source current i_s and freewheeling diode current i_{FD} are also shown.



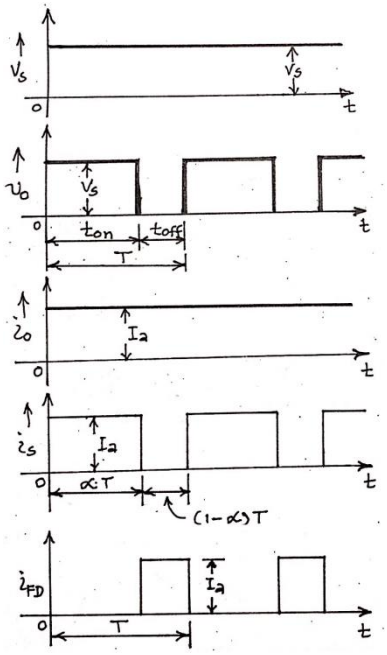
2 marks for Explanation

Average motor voltage is given by,

$$V_0 = \frac{t_{on}}{T} V_s = \alpha V_s = f t_{on} V_s$$

where α = duty cycle = $\frac{t_{on}}{T}$

and f = Chopping frequency = $\frac{1}{T}$



2 marks for Diagrams

Power delivered to motor is given by,

Power delivered to motor = Average motor voltage × Average motor current

$$= V_t I_a = \alpha\, V_s I_a$$

Motor voltage equation can be expressed as,

$$V_0 = \alpha\, V_s = E_b + I_a(R_a + R_{se})$$

The back emf is proportional to speed,

$$E_b \propto \omega_m \therefore E_b = K_m \omega_m$$

Thus voltage equation becomes,

$$V_0 = \alpha\, V_s = K_m \omega_m + I_a(R_a + R_{se})$$

The speed can be obtained as,

$$\omega_m = \frac{\alpha\, V_s - I_a(R_a + R_{se})}{K_m}$$

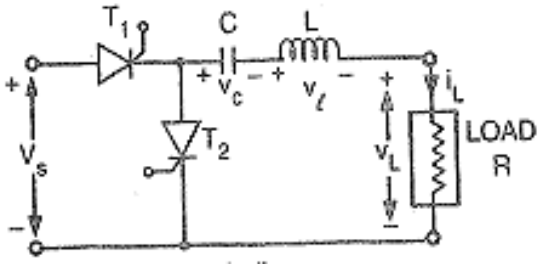
It is seen that by varying the duty cycle α of the chopper, armature terminal voltage can be controlled and thus speed of the dc series motor can be regulated.

1 b) **Attempt any <u>ONE</u> of the following:** **6**

1 b) (i) Give the operation of series inverter with a neat diagram. Draw its waveforms and also state its limitations.

Ans:

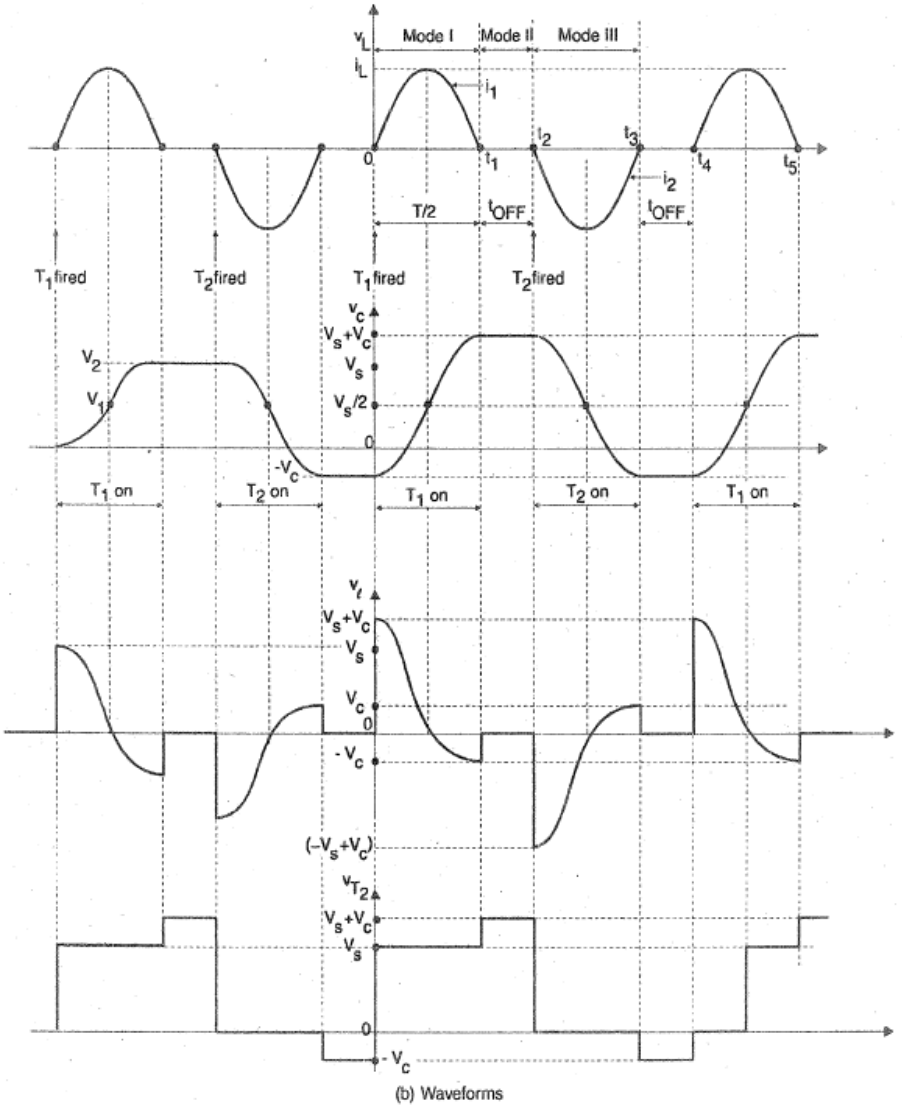
Series Inverter:



2 marks for circuit diagram

Assume initially that both the SCRs are off and there is no charge on the capacitor, so $v_c = 0$. Both the SCRs are forward biased by the input dc voltage V_s. If gate pulse is applied to T_1, it conducts and input voltage V_s appears across series combination C-L-R. The component values of C, L and load R are such that the R-L-C series combination is an underdamped circuit. For such underdamped circuit, when DC supply is given (which is the case when T_1 is fired), a current in the form of a pulse is observed as shown in the waveform. During this current pulse, the capacitor charges through inductor L and load resistor R. Due to inductor L, the capacitor charges with shown polarity to a

1 mark for description



1 mark for waveforms

voltage higher than the supply voltage and the current drops to zero, turning T_1 off. Due to the capacitor voltage T_2 is forward biased. If gate pulse is applied to T_2, it is turned on and it provides path for the discharge current of capacitor. The capacitor discharges through T_2, Load R and inductor L. Since discharging circuit is same under damped R-L-C combination, the current is in the form of pulse as before but now in the reverse direction. Thus alternate firing of T_1 and T_2 causes alternate positive and negative half cycles of current respectively as shown in the waveform.

Limitations of Series Inverter:

1) Limitation on output frequency: The maximum possible output frequency is limited to the ringing frequency of the resonant circuit
2) High distortion.
3) High rating of commutating components L and C.
4) Poor voltage regulation.
5) High peak current rating of input DC source.

2 marks for any two limitations

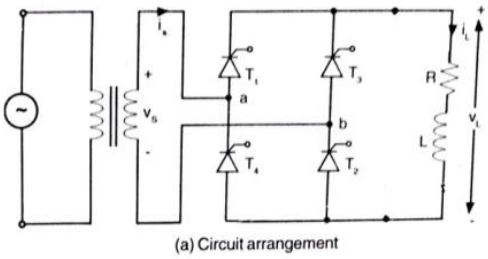
1b) (ii) Draw a neat circuit diagram of 1 ϕ fully controlled bridge converter with RL load and give its operation with waveform.

Ans:

Single phase fully controlled bridge converter with RL load

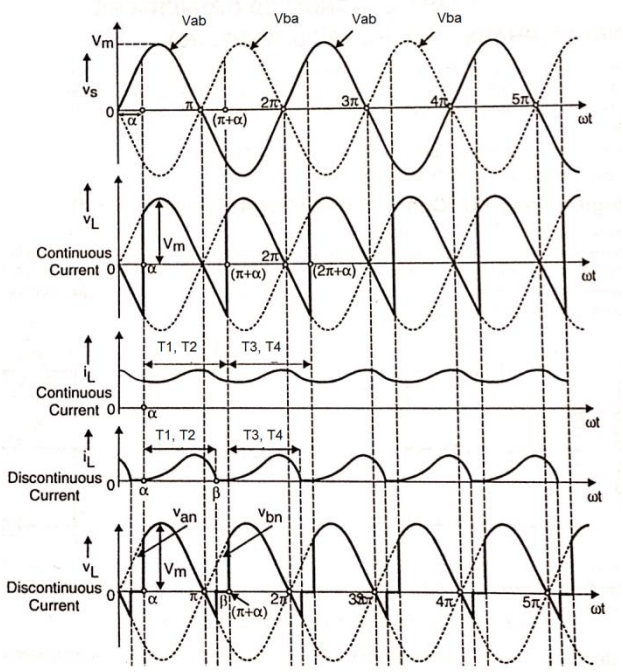
During positive half cycle of input voltage, T_1 and T_2 are forward biased and during negative half cycle, T_3 and T_4 are forward biased. Therefore, T_1-T_2 pair and T_3-T_4 pair are fired alternately in positive and negative half cycles of input voltage respectively, as shown in the waveform figure (b). In each half cycle, the respective SCRs are fired at firing or delay angle α, as shown. Once SCR pair conducts (at delay angle in each half cycle), the input source voltage appears across load, the current flows and if the load is inductive in nature, the conducting SCRs remain into conduction till the fall of current to zero or firing of next pair of SCRs as shown in the waveform diagram.

Due to load inductance, the current lags behind the output voltage and falls to zero after the end of that half cycle. Therefore, during the



(a) Circuit arrangement

2 marks for circuit diagram



(b) Waveforms

2 marks for operation explanation

2 marks for waveforms

time interval between voltage zero instant and current zero instant, the reversed supply voltage appears across load for discontinuous conduction. At current zero, the SCRs are turned off and load gets isolated from source, causing load voltage zero till the firing of next pair of SCRs.

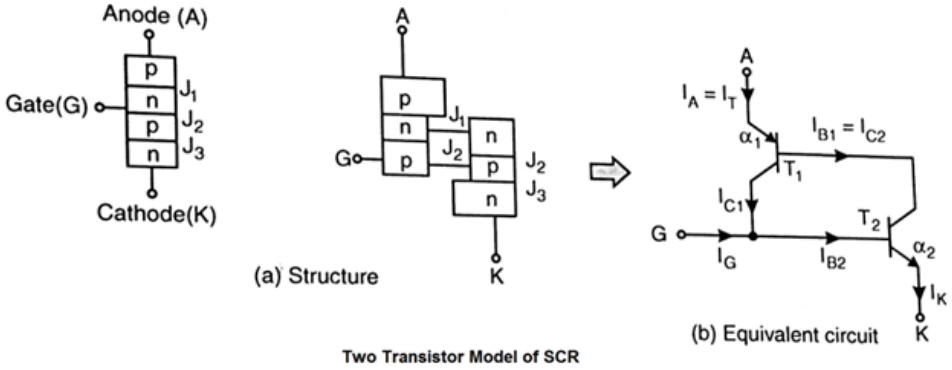
If load inductance is large, the load current never falls to zero. The current attempts to fall, but before it could fall to zero, the next pair of SCR get fired and we get continuous conduction. In this situation, the reversed voltage appears across load after the end of each half cycle till the firing of next pair of SCRs as shown in the waveform diagram.

2 **Attempt any FOUR of the following:** **16**

2a) Explain two transistor analogy of SCR.

Ans:

Two-transistor Analogy of SCR:



Two Transistor Model of SCR

1 mark for (a)
1 mark for (b)
= 2 marks for diagram

A simple p-n-p-n structure of thyristor can be visualized as consisting of two complimentary transistors: one pnp transistor T_1 and other npn transistor T_2 as shown in the figures. The collector current of transistor is related to emitter current and leakage current as:

$$I_C = \alpha I_E + I_{CBO}$$

where, α = common-base current gain

I_{CBO} = leakage current from collector to base with emitter open

For transistors T_1 and T_2, we can write,

$I_{C1} = \alpha_1 I_A + I_{CBO1}$ and $I_{C2} = \alpha_2 I_K + I_{CBO2}$

From KCL applied to T_1, we can write

$$I_A = I_{C1} + I_{C2} = \alpha_1 I_A + I_{CBO1} + \alpha_2 I_K + I_{CBO2}$$

From KCL applied to entire equivalent circuit,

$I_K = I_A + I_G$ and substituting in above equation,

$I_A = \alpha_1 I_A + I_{CBO1} + \alpha_2 (I_A + I_G) + I_{CBO2}$

$= I_A(\alpha_1 + \alpha_2) + \alpha_2 I_G + I_{CBO1} + I_{CBO2}$

$I_A(1 - [\alpha_1 + \alpha_2]) = \alpha_2 I_G + I_{CBO1} + I_{CBO2}$

$$I_A = \frac{\alpha_2 I_G + I_{CBO1} + I_{CBO2}}{1 - [\alpha_1 + \alpha_2]}$$

2 marks for mathematical treatment

From this equation it is clear that the anode current depends on the gate current, leakage currents and current gains.

If $(\alpha_1 + \alpha_2)$ tends to be unity, the denominator $1 - [\alpha_1 + \alpha_2]$ approaches zero, resulting in a large value of anode current and SCR will turn on. The current gains vary with their respective emitter currents. When gate I_G current is applied,

the anode current I_A is increased. The increased I_A, being emitter current of T_1, increases the current gain α_1. The gate current and anode current together form cathode current, which is emitter current of T_2. Thus increase in cathode current results in increase in current gain α_2. Increased current gains further increase the anode current and the anode current further increases the current gains. The cumulative action leads to the loop gain to approach unity and the anode current drastically rises which can be controlled by external circuit only.

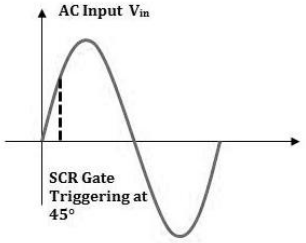
2b) Give the concept of firing angle and conduction angle with a neat waveform.

Ans:

Firing Angle(α):

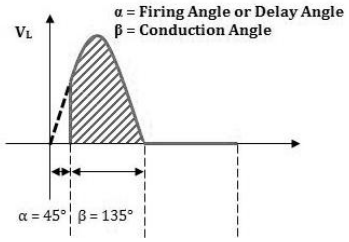
Firing angle is defined as the angle between the instant the SCR would conduct if it would be a diode and the instant it is triggered or fired.

Firing angle or delay angle can be defined as the angle measured from the angle that gives maximum average output voltage to the angle when the SCR is actually triggered or fired by gate pulse.



Conduction Angle (β):

Conduction angle is defined as the angle between the instant the SCR is triggered or turned on and the instant at which the SCR is turned off.



1 mark for each description and 1 mark for each waveform = 4 marks

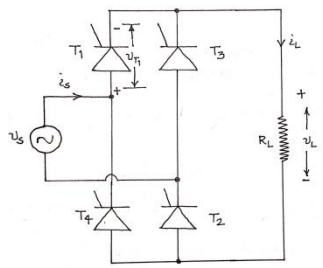
Assuming that the SCR is turned off naturally at the end of positive half cycle, the relation between the firing or delay angle (α) and conduction angle (β) can be expressed as:

$\alpha + \beta = \pi$ radian or 180°

2c) Give the operation of single phase full wave controlled converter with R load with a neat diagram.

Ans:

Single phase full wave controlled converter with R load:



(NOTE: Here Bridge type converter is considered. However, the marks should also be awarded to the circuit configuration with Centre-tapped transformer and two-SCRs)

2 marks for circuit diagram

During positive half cycle of input voltage, T_1 and T_2 are forward biased and during negative half cycle, T_3 and T_4 are forward biased. Therefore, T_1-T_2 pair and T_3-T_4 pair are fired alternately in positive and negative half cycles of input voltage respectively, as shown in the waveform diagram. In each half cycle, the respective SCRs are fired at firing or delay angle α, as shown. Before conduction of any pair, the load is isolated from input source, hence load current and voltage are zero. Once SCR pair conducts (at delay angle in each half cycle), the input source voltage appears across load till the end of that half cycle. Thus output DC voltage is in the form of pulses. The

1 mark for operation

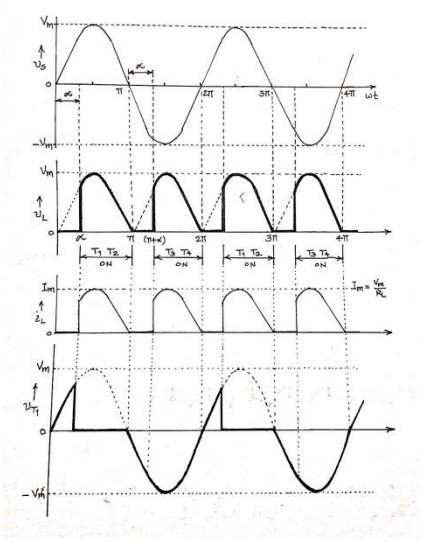
magnitude of average load voltage depends upon the firing angle α.

$V_{dc} = \frac{V_m}{\pi}(1 + cos\alpha)$

Since load is purely resistive, load current is given by $i_L = \frac{v_L}{R_L}$

Therefore, the waveform of load current is just similar to that of load voltage.

When any SCR is on, its voltage is approximately zero, and when it is off, the voltage across it is equal to alternating supply voltage. The waveform of voltage across T_1 is shown.



1 mark for waveforms

2d) Give the control techniques of a chopper with a neat waveform.

Ans:

Chopper Control Techniques:

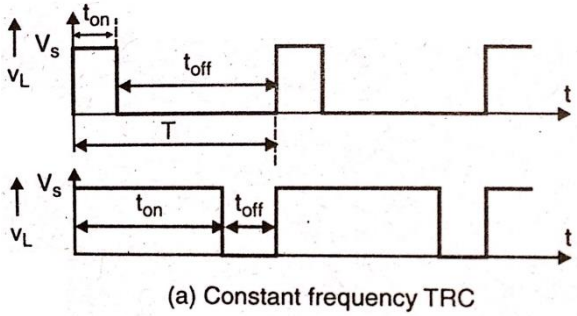
There are two ways of controlling the chopper operation:

1) Time Ratio Control (TRC)
   (i) Constant frequency system
   (ii) Variable frequency system
2) Current Limit Control (CLC)

Time Ratio Control:

In this technique, the duty cycle 'k' is controlled to control the output voltage. It is carried out by two ways:

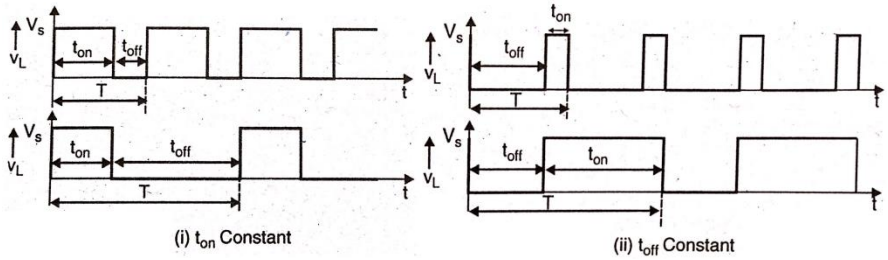
(i) Vary T_{on} keeping frequency constant i.e time period T=1/f constant



(a) Constant frequency TRC

1 mark for constant frequency TRC

(ii) Vary frequency f keeping T_{on} or T_{off} constant i.e time period T varies

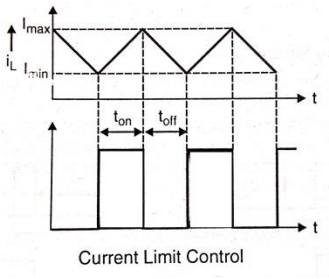


2 marks for variable frequency TRC

Current Limit Control:

In this technique, the load current is allowed to vary only between a predetermined maximum and minimum limit. If the load current tends to

increase beyond maximum limit, chopper switch is turned off and if the load current tends to fall below the minimum (lower) limit, the chopper switch is turned on. The load current is continuous.

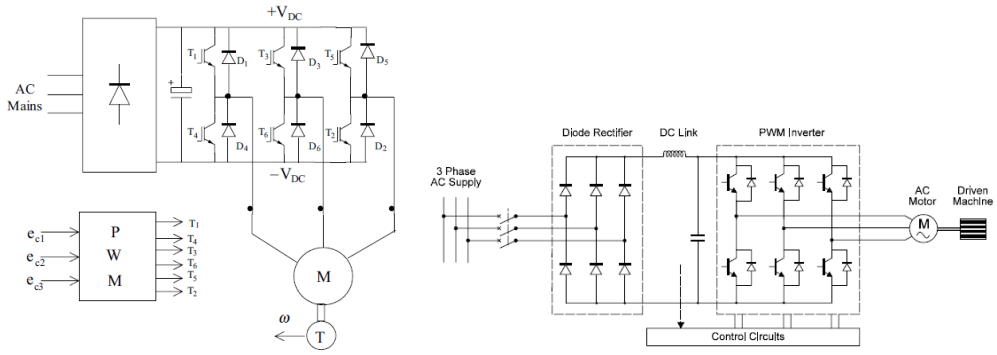


1 mark for CLC

2e) Give the operation of speed control of 3 ϕ Induction motor using variable frequency system with a neat diagram.

Ans:

Variable frequency control of induction motor:



2 marks for any one correct circuit configuration

The speed of an induction motor can be controlled by varying the supply frequency. When the supply frequency is changed, the synchronous speed N_s (=120f/P) is changed and accordingly the motor speed get changed.

If the supply frequency f is changed to f* such that f* = β.f, the synchronous speed at new frequency f*becomes,

2 marks for explanation

$N_S^* = \frac{120f^*}{P} = \frac{120\beta f}{P} = \beta N_s$ and the slip becomes $s^* = \frac{\beta N_s - N}{\beta N_s} = 1 - \frac{N}{\beta N_s}$

The maximum torque developed at any supply frequency is inversely proportional to the square of frequency. Therefore, maximum torque gets reduced in inverse proportion when frequency is increased.

When the frequency is changed, the values of the reactances in the equivalent circuit are changed and therefore circuit currents are also changed. If the frequency is increased above its rated value, the reactances are also increased, the currents fall, the flux and maximum torque get decreased but synchronous speed is increased and motor speed is also increased.

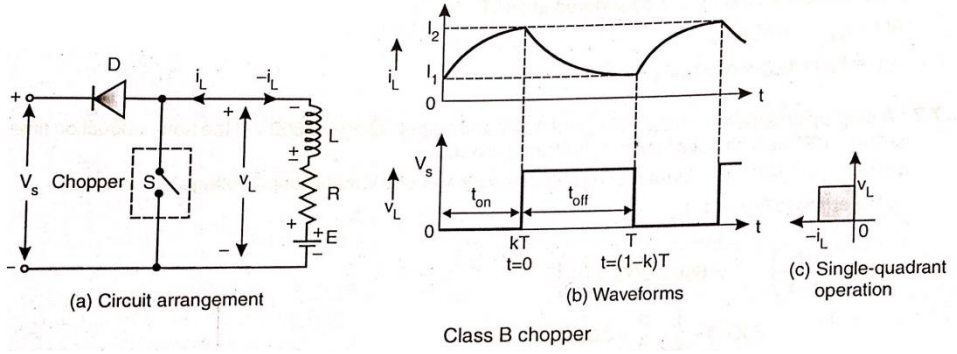
With a Sinusoidal Pulse Width Modulated (SPWM) inverter indicated in figure, the supply frequency to the motor can be easily adjusted for variable speed. However, if rated airgap flux is to be maintained at its rated value at all speeds, the supply voltage to the motor should be varied in proportion to the frequency. In the figure, the dc voltage obtained from diode rectifier remains constant and the PWM technique is applied to vary both the voltage and frequency within the inverter.

2f) Draw a neat circuit diagram of class B chopper and give its operation with waveform.

Ans:

Class B Chopper:

2 marks for circuit diagram



Class B chopper

1 mark for waveform

1 mark for explanation (Mathematical treatment optional)

The circuit arrangement of class B chopper is shown in Fig. (a). The load current i_L always flow out of load, hence considered negative. The load voltage is either zero or positive. This is a single-quadrant chopper operated in second quadrant and said to be operated as an inverter, power flows from output load to input source. When chopper is on, the load voltage $v_L = 0$ and the emf E drives current i_L through load parameters R-L. The voltage equation by KVL can be written as:

$$E - R.i_L - L\frac{di_L}{dt} = 0$$

The solution of this equation with initial condition $i_L(t=0) = I_1$ can be obtained as :

$$i_L = I_1 e^{\frac{-Rt}{L}} - \frac{E}{R}\left[1 - e^{\frac{-Rt}{L}}\right] \qquad \text{(for } 0<t<kT\text{)}$$

At t = kT, $i_L = I_2$

When chopper is turned off, the inductor L and emf E drive current through input DC source V_S. During off-time t_{off}, the current i_L falls. Redefining the time origin t = 0 at t = kT, the KVL can be expressed as:

$$V_S = E - R.i_L - L\frac{di_L}{dt}$$

The solution of this equation with initial condition $i_L(t=kT) = I_2$ is given by,

$$i_L = I_2 e^{\frac{-Rt}{L}} + \frac{(V_S - E)}{R}\left[1 - e^{\frac{-Rt}{L}}\right] \quad \{\text{for } 0 < t < (1\text{-}k)T\}$$

At the end of off period, i.e at t = (1-k)T,

$i_L = I_1$: for steady-state continuous current

= 0 : for steady-state discontinuous current

If E is considered as input dc voltage and V_S is considered as output voltage, then class B chopper is a step-up chopper.

3 **Attempt any <u>FOUR</u> of the following**: **16**

3a) Give the triggering methods of SCR and explain any one.

Ans:

SCR Triggering Methods:

2 marks for any four triggering methods

1) Forward voltage triggering
2) Thermal triggering (Temperature triggering)
3) Radiation triggering (Light triggering)
4) dv/dt triggering
5) Gate triggering
   (i) D.C. Gate triggering
   (ii) A.C. Gate triggering

(iii) Pulse Gate triggering

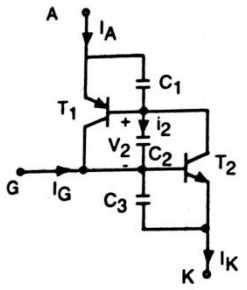
1) Forward Voltage Turn-on:

When the forward anode-to-cathode voltage V_{AK} is greater than forward break over voltage V_{BO} sufficient leakage current flows. The energy of leakage current carriers arriving at reverse biased junction is sufficient to dislodge additional carriers. These carriers in turn dislodge more carriers and this carrier multiplication due to regenerative action results in avalanche breakdown of junction. The anode current is sharply increased. This type of turn on may damage device by thermal runaway. Therefore this method is normally not adopted for turning on SCR, however it is employed to switch four layer diodes into conduction.

2 marks for explanation of any one triggering method

2) dv/dt turn-on or Triggering of Thyristor:

Any p-n junction has capacitance. Under transient conditions, these capacitances influence the characteristics of SCR. Fig. shows two-transistor transient model of SCR wherein the junction capacitances have been shown external to the transistors. If SCR is in forward blocking state and rapidly rising voltage is applied between anode and cathode, the high current will flow through the device to charge the capacitors. The current through capacitor C_2 (junction J_2) can be expressed as:



Two-traisistor transient model of thyristor

$$i_2 = \frac{d(q_2)}{dt} = \frac{d}{dt}(C_2V_2) = V_2\frac{dC_2}{dt} + C_2\frac{dV_2}{dt}$$

where, C_2 = capacitance of junction J_2

V_2 = voltage across junction J_2

q_2 = charge in the junction J_2

If the rate of rise of the voltage $\frac{dV_2}{dt}$ is large, then current i_2 would be large. As these capacitor currents are basically leakage currents, the transistor leakage currents i_{CBO1} and i_{CBO2} would be increased. The high values of leakage currents may cause $(\alpha_1 + \alpha_2)$ tending to unity and result in unwanted turn-on of the SCR by regenerative action. The rapidly rising anode voltage produces charging current through the junction capacitance, leading to gate terminal. This current then acts as gate current and SCR is triggered.

3) Temperature:

High temperature generates the additional carriers and hence leakage current is increased. At high temperatures, the leakage current in a reverse biased p-n junction is doubled approximately with 8°C rise in junction temperature. This increase in currents cause anode current I_A to

increase, which further causes α_1 and α_2 to increase. Due to regenerative action, $(\alpha_1+\alpha_2)$ may tend to be unity and thyristor may be turned on. Such turn-on may cause thermal runaway and therefore it is avoided.

4) Gate Turn-on:

With anode voltage positive with respect to cathode, if positive voltage is applied to gate with respect to cathode, the gate current is injected into the structure. In two-transistor analogy, the gate current I_G increases the emitter current of T_2i.e cathode current I_K, which further leads to increase in current gain α_2. So collector current I_{C2} which is base current I_{B1} is increased. This causes I_{C1} and I_{E1}i.e anode current I_A to increase. Thus emitter currents and current gains tend to increase in regenerative action and finally thyristor is turned on. This is the method normally adopted for turning on the conventional thyristors.

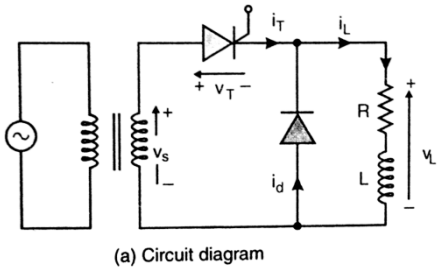
5) Radiant Energy (Light) Turn-on:

If light is allowed to strike the junctions of thyristor, due to incident radiant energy, considerable numbers of electron-hole pairs are released. This increase in current carriers, results in leakage currents to increase above a level when the regenerative action starts and the thyristor is turned on.

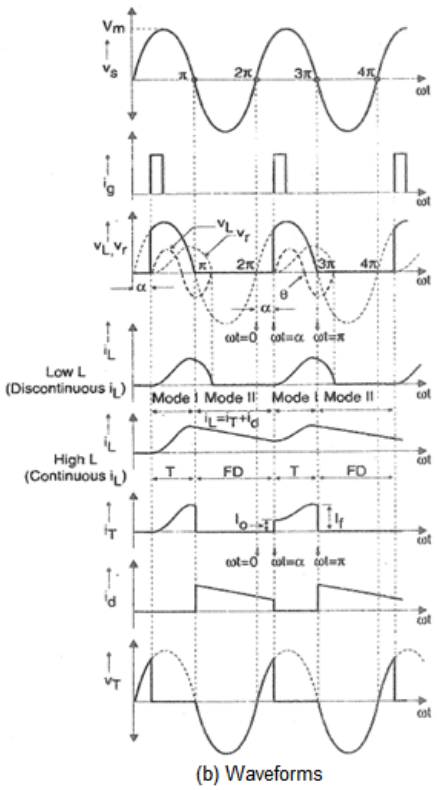
3b) Draw a neat diagram of single phase fully controlled half wave converter with RL load and freewheeling diode. Give its operation.

Ans:

Single-phase Fully controlled half-wave converter with R-L load:



(a) Circuit diagram



(b) Waveforms

2 marks for circuit diagram

2 marks for operation (Waveforms are optional)

The circuit diagram of 1ϕ half wave controlled rectifier with RL load and free-wheeling diode is shown in fig. (a). During positive half-cycle of v_s the SCR get forward biased. After the starting instant ωt = 0, at delay angle (α) gate pulse is provided to SCR and it is triggered. Once it conducts, the voltage v_s appears across load. As the load is inductive, the current starts from zero, then rises, attain peak and then falls. During positive half cycle, the reverse bias is maintained across free-wheeling diode through conducting SCR. At the end of positive half cycle, v_s becomeszero, but load inductance maintains current in the same direction through v_s and SCR. After ωt = π, the supply voltage is reversed, which causes

forward bias across free-wheeling diode and it is turned on. Once the diode conducts, the reversed supply voltage appears across the SCR. The load inductance forces current through the diode. Thus the load current which was flowing through SCR, now shifted to free-wheeling diode D. The SCR is subjected simultaneously to reverse voltage and zero current. Therefore, the SCR is turned off at $\omega t = \pi$. When the free-wheeling diode conducts, the load voltage becomes zero. Thus the effect of free-wheeling diode is that the load voltage never becomes negative in presence of free-wheeling diode and hence the average value of the load voltage is improved. The load current continues to flow after $\omega t = \pi$ for some time depending upon the value of the load inductance. If the load inductance is less, the current becomes zero, prior to the next firing of SCR in the next positive half cycle. Thus we get discontinuous load current. However, if the load inductance is large, the current continues after $\omega t = \pi$ and does not become zero until the SCR is fired again in the next positive half cycle. Thus we get continuous load current without any zero value. The waveforms are shown in fig.(b).

3c) Give any four specifications of SCR.

Ans:

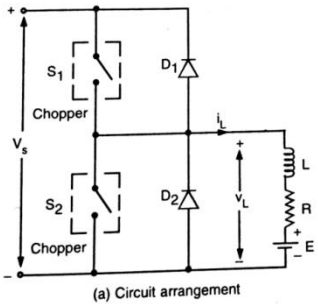
1. **Voltage Rating:**
   - i) Peak working forward-blocking voltage V_{DWM}
   - ii) Peak repetitive forward-blocking voltage V_{DRM}
   - iii) Peak surge or non-repetitive forward blocking voltage V_{DSM}
   - iv) Peak working reverse voltage V_{RWM}
   - v) Pear repetitive reverse voltage V_{RRM}
   - vi) Peak surge or non-repetitive reverse voltage V_{RSM}
   - vii) On-state voltage drop V_T
   - viii) Finger voltage
   - ix) Forward dv/dt rating (Critical rate of rise voltage)
2. **Current Rating:**
   - i) Average on-state current I_{TAV}
   - ii) RMS current I_{Trms}
   - iii) Surge current rating I_{TSM}
   - iv) I^2t rating
   - v) di/dt rating
3. **Power Rating:**
   - i) Maximum gate power P_{gm}
   - ii) Average gate power P_{gav}
   - iii) Average Power dissipation (Forward on-state conduction loss)
   - iv) Loss due to leakage current during forward and reverse blocking
   - v) Switching losses during turn-on and turn-off
4. **Temperature Rating:**
   Maximum junction temperature

1 mark for each of any four specifications

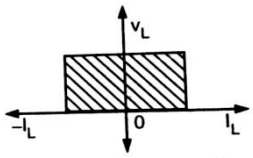
3d) Give the operation of class C chopper with a neat diagram. Also draw the waveform.

Ans:

Class C Chopper:



(a) Circuit arrangement



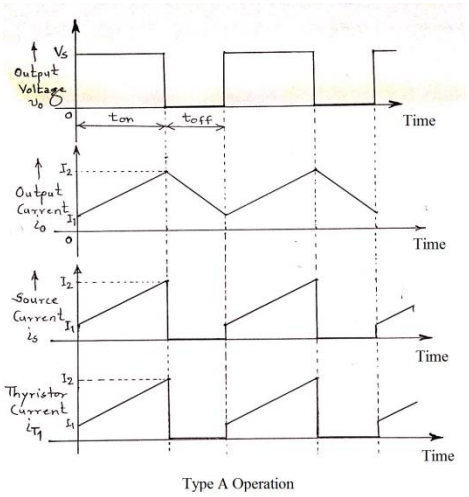
(b) Two-quadrant operation

The circuit configuration is shown in fig.(a). It is essentially a two-quadrant chopper in the sense that the load current can be either positive or negative but the load voltage is always positive, as shown in fig.(b). It is a combination of class A and class B chopper. Keeping switch S_2 inoperative, the circuit behaves as class A chopper and keeping S_1 inoperative, the circuit behaves as class B chopper.

1 mark for circuit diagram

(i) Class A operation (Switch S_2 maintained off):

In this operation the switch S_1 is turned on and turned off alternately. When the switch S_1 is turned on, the DC source voltage gets applied across the load and supplies load current. When the switch S_1 is turned off, the load inductance forces current through free-wheeling diode D_2 which makes the load voltage zero. Thus the load voltage is either positive or zero and the load current is positive as shown in the fig. (a). Thus the chopper is operated in first quadrant.



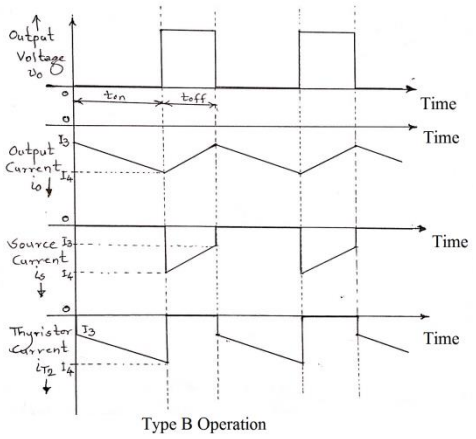
Type A Operation

1 mark for class A operation

½ mark for waveform

(ii) Class B operation (Switch S_1 maintained off):

In this operation, the load current is opposite to that shown in the fig.(a). When the switch S_2 is turned on, the load voltage becomes zero, the emf E drives load current i_L through load parameters R-L and S_2. When switch S_2 is turned off (opened), the load inductive voltage reverses its polarity and aids the emf E to force current through D_1 and V_s. The load voltage thus becomes equal to V_s. Thus the load voltage is either zero or positive and the load current is negative. Thus the chopper is operated in second quadrant.



Type B Operation

1 mark for class B operation

½ mark for waveform

The class C chopper can operate either as a rectifier or as an inverter. This chopper is used for controlling the motoring and regenerative braking of DC motors.

Basically Type C chopper is a combination of Type A and Type B choppers, as shown in figure. So depending upon the requirement, it can be operated as type-A (excluding S_2 and D_1) or type-B chopper (excluding S_1 and D_2).
The waveforms for both operations are shown separately in the following figure.
Conducting Devices:
Type A operation: During t_{on}: S_1 (SCR T_1) and during t_{off}: D_2
Type B operation: During t_{on}: S_2 (SCR T_2) and during t_{off}: D_1

3e) Give the principle of induction heating control with a neat representation.

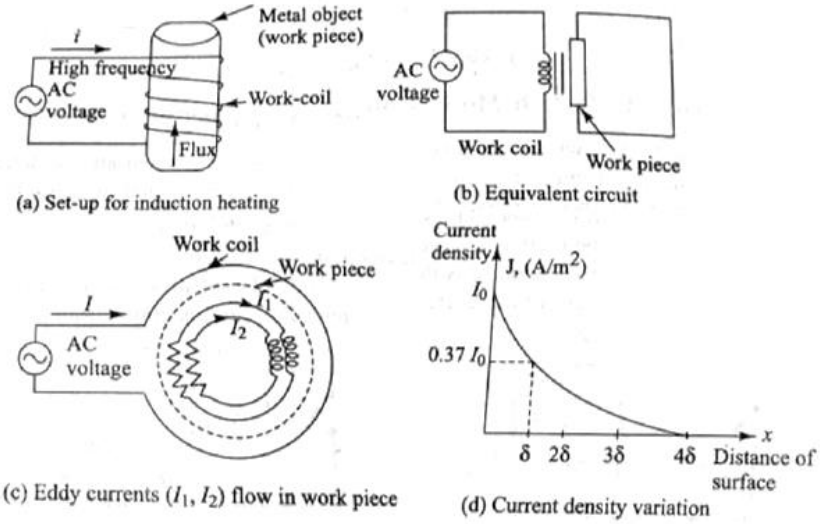
Ans:

Principle of induction heating:

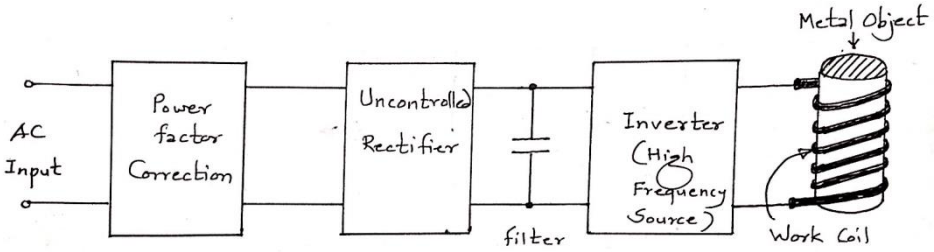
When a conducting object is subjected to a changing magnetic field, according to Faraday's laws of electromagnetic induction, emf is induced in the object. The object, being conductor, offers many short-circuited paths. So the circulating current flows through these paths. The currents are in the form of eddies (circular in nature), hence called "eddy currents". The eddy currents flowing through resistive paths in metal object cause power loss (i^2R loss) and heat is produced. Since the heat is produced by eddy currents, which are induced by electromagnetic induction, this heating is called "Induction heating". The material to be heated is known as the work piece and the coil around it is known as work coil, as shown in the figure. The coil acts as primary and work piece acts as short circuited secondary. When primary is excited by high frequency ac supply, eddy currents are set up in the work piece and electrical power loss heats up the object.

2 marks for Explanation

For induction heating, high frequency AC supply is obtained using thyristorised converter circuits. The block diagram of one of such arrangements is shown in the figure. The available AC supply is first converted to DC using uncontrolled rectifier and filter arrangement. Then the DC is converted to AC with required high frequency using thyristorised inverter. Since the load is highly inductive, the power factor of load is too low. So to improve it, power factor correction circuit is employed at the input stage.



2 marks for any one labeled figure (graphical figure optional)

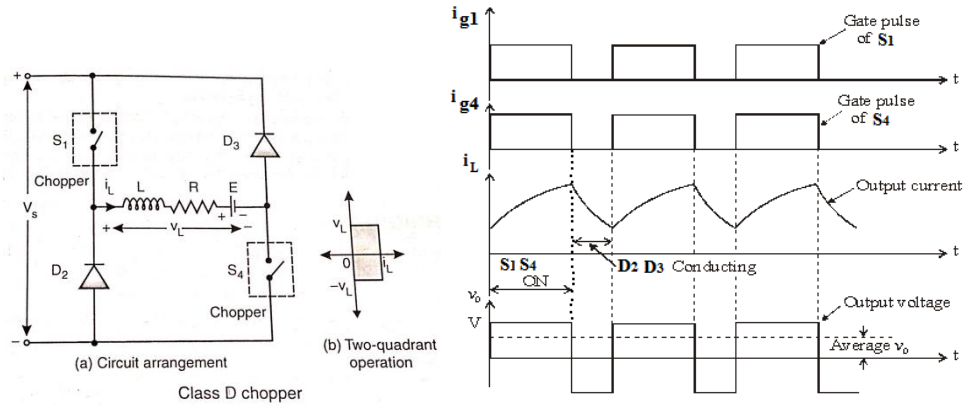


4 a) **Attempt any <u>THREE</u> of the following**: **12**

4 a) i) Draw a neat circuit diagram of class D chopper and give its operation with waveform.

Ans:

Class D Chopper:



Class D chopper

2 marks for circuit diagram

1 mark for waveform

In this chopper, the load current is always maintained positive as shown in the Fig. (a), but the load voltage can be either positive or negative.

When chopper switches S_1 and S_4 are on, the input dc source voltage appears across load and it drives the positive load current i_L as shown in Fig. (a). During this time, both v_L and i_L are positive, power is supplied by input dc source V_S to load and the chopper is said to be operated as rectifier in the first quadrant.

When chopper switches S_1 and S_4 are turned off, the load current i_L is maintained in the same direction by reversed load inductor voltage v_o, through D_3, V_S and D_2. The load inductance gives out stored energy. Due to the reversed load inductor voltage, the load voltage v_L becomes negative. During this time, i_L is positive, v_L is negative, power is supplied by load inductance to input dc source V_S and the chopper is said to be operated as an inverter in the third quadrant. The conducting devices and nature of load (output) voltage and current is shown in the waveform.

1 mark for explanation of operation

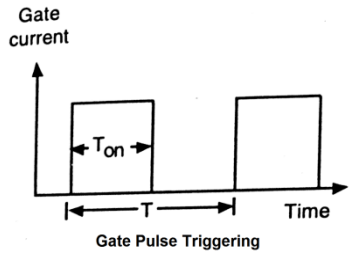
4 a) ii) What are the requirements of pulse gate triggering of SCR.

Ans:

Pulse Gate Triggering of SCR:

In pulse triggering, a current pulse of sufficient width is supplied to SCR gate to allow the anode current to exceed the latching current and turn-on the device. The pulse current with widths beyond 100 μsec are treated as DC. If the pulse widths are less than 100 μsec, higher gate voltage and current should be applied for faster turn-on. SCR is considered as a charge controlled device on short term basis. Higher magnitude gate current pulse takes lesser time to inject the

2 marks for pulse width explanation



Gate Pulse Triggering

required charge for turn on. In pulse triggering, with higher gate voltage and current, greater amount of gate power dissipation can be allowed, however it should be less than the peak instantaneous gate power dissipation P_{gm} as specified by the manufacturer. In any case, the average gate power dissipation should be less than or equal to the allowable average gate power dissipation P_{gav}. Thus if the gate pulse magnitude is such that instantaneous gate power dissipation is P_{gm}, pulse width is T_{on} and period is T, then

2 marks for gate power dissipation explanation

Average gate power dissipation ≤ Average gate power dissipation limit

i.e $\frac{P_{gm}T_{on}}{T} \leq P_{gav}$. If f = frequency of firing or pulse repetition rate in hz, f = 1/T

In the limiting case, $P_{gm}fT_{on} = P_{gav}$

And the frequency of firing is given by $f = \frac{P_{gav}}{T_{on}P_{gm}}$

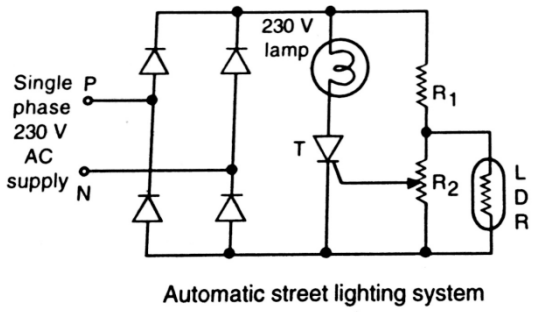
For safety of device, it should be ensured that

(Pulse voltage amplitude)(Pulse current amplitude)<P_{gm}

4 a) iii) Give the operation of automatic street lighting circuit using SCR with a neat diagram.

Ans:

Automatic Street Lighting Circuit Using SCR:



Automatic street lighting system

The circuit configuration of automatic street lighting system using SCR is shown in the fig. This circuit provides automatic glowing of street lamps in the evening. A light dependent resistor (LDR) is used as sensor for sensing the intensity of day light. When sufficient light falls on LDR, its resistance becomes very low as compared to R_2. The R_2 is then bypassed by LDR, and major part of current flowing through R_1, flows through LDR. Since negligibly small current flows through R_2, sufficient gate current is not received by SCR T and it is maintained off. Thus no current can flow through lamp and it remains off.

2 marks for circuit diagram

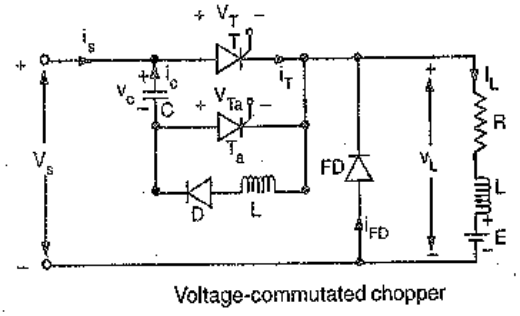
2 marks for operation

In the evening hours, the intensity of day light is reduced. Hence resistance of LDR increases. Therefore current through R_2 also increases. At certain darkness, the resistance of LDR becomes so high that the sufficient current flows through R_2 to provide sufficient gate current to SCR and it is fired. Therefore, current flow through lamp and it glows. Since bridge rectifier provides pulsating DC, the SCR is triggered in every positive pulse and turn-off at the end of pulse at natural current zero value, assuming lamp is purely resistive. However, if the lamp is inductive, the lagging current prevents SCR from turning off at the end of positive pulse. Thus once SCR is turned on, it loses control and separate arrangement is necessary to turn-off the SCR.

4 a) iv) Explain Auxiliary commutation with a neat diagram.

Ans:

Auxiliary Commutation



Voltage-commutated chopper

At start, the T_a is triggered and turned on to carry the load current. Due to the resonant circuit R-L-C, the current initially rises, attains peak and then falls to zero. This turns off the auxiliary SCR Ta. This current charges the capacitor C with upper plate positive. The capacitor thus forward biases the main SCR T. When main SCR T is triggered, it is turned on and charged capacitor C is placed across T_a so as to apply reverse bias across it. The load current now flows through T. The capacitor continues to discharge through T, L and D. Since this LC is resonant combination, the capacitor discharges completely first and then charges with opposite polarity till the current falls to zero. The capacitor current cannot reverse because of diode D. Now the oppositely charged capacitor forward biases the auxiliary SCR T_a. Thus when T_a is triggered, T is turned off and the same cycle is repeated. In this configuration, the firing of auxiliary SCR commutates the main SCR, hence name is auxiliary commutation.

2 marks for circuit diagram

2 marks for operation

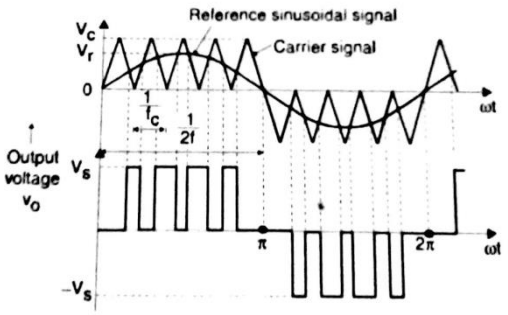
4 b) **Attempt any ONE of the following.** **6**

4 b) i) Explain sinusoidal pulse width modulation with a neat diagram.

Ans:

Sinusoidal pulse width modulation:

In this modulation technique, several pulses per half cycle are used to fabricate output AC waveform. The pulse width is a sinusoidal function of the angular position of the pulse in the half cycle. The gating signals for turning on the thyristors are generated by comparing a high frequency carrier signal v_c with a sinusoidal reference signal v_r of desired frequency. The trigger pulse is generated at the intersection point of v_c and v_r. The thyristor is maintained on during the interval when $v_r > v_c$. When v_r becomes equal to v_c the on thyristor is commutated by forced commutation. In fact, the comparison of v_c and v_r is carried out in comparator and when $v_r > v_c$, the comparator output is high, otherwise it is low. The comparator output is processed in such manner that the output voltage has pulse width in agreement with the comparator output pulse width.



Sinusoidal-pulse-width modulation (Sin M)

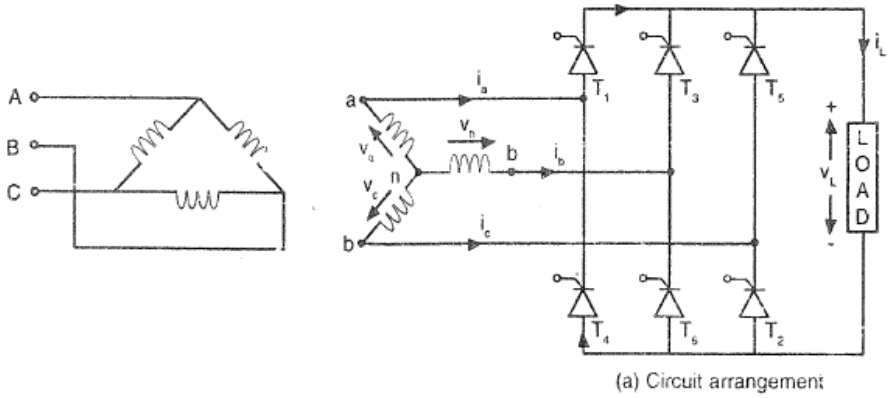
4 marks for explanation

2 marks for waveform diagram

4 b) ii) Give the operation of 3 ϕ fully controlled bridge converter with R load with a neat diagram. Also draw its waveform.

Ans:

Three-phase Fully Controlled Bridge Converter:



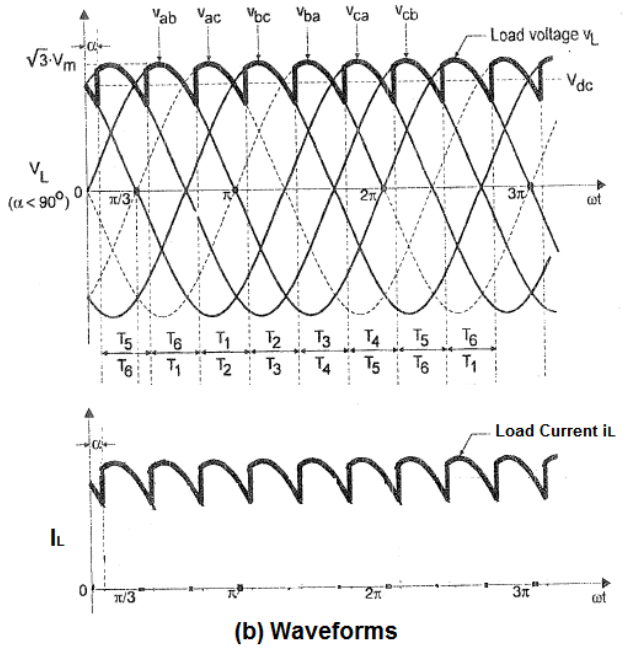
(a) Circuit arrangement

2 marks for circuit diagram

2 marks for circuit operation

The circuit diagram of 3ϕ fully controlled bridge converter is shown in fig.(a). Six thyristors are connected in bridge to obtain full wave rectification. One of the upper thyristors T_1, T_3, T_5 carry current from secondary winding to load and one of the lower thyristors T_2, T_4, T_6 carry current back from load to secondary winding. The pair of the thyristors which is connected to those lines having a positive instantaneous line-to-line voltage is fired. If v_{ab} is positive, then the thyristor connected to phase ai.e T_1 and thyristor connected to phase b i.e T_6 are fired. The thyristors are fired at an interval of π/3 rad or 60°. Each thyristor conducts for 2π/3 rad or 120°. The fig.(b) shows the waveforms of line voltage, output load voltage and load current.

2 marks for waveforms



(b) Waveforms

At ωt = 0, the line voltage v_{cb} is higher than any other line voltage, hence thyristor T_5 connected to phase c and thyristor T_6 connected to phase b are fired at delay angle α. After firing T_5 and T_6, the load voltage becomes equal to v_{cb}. The upper load terminal gets connected to phase c and voltage v_{ac} appears across T_1 and voltage v_{bc} across T_3. As both v_{ac} and v_{bc} are negative, both T_1 and T_3 are reverse biased. Similarly the lower load terminal gets connected to phase b through T_6 and voltage v_{ba} appears across T_4 and voltage v_{bc} across T_2. As both v_{ba} and v_{bc} are negative, both T_4 and T_2 are reverse biased. Thus firing of a pair of thyristors causes all other thyristors to be reverse biased. This condition is continued till ωt = π/3. After this the line voltage v_{ab} becomes higher than v_{cb}. At ωt = π/3, the line voltage v_{ac} crosses zero value and becomes positive, due to which T_1 get forward biased. So a gate pulse is applied to T_1 at ωt = (π/3)+α. Once T_1 is turned on, the upper load

terminal get connected to phase a, causing line voltage v_{ca} across conducting T_5. As v_{ca} is negative, T_5 get reverse biased and turned off. The load current get shifted fromT_5 to T_1. However, the thyristor T_6 remains on and continue to carry load current with T_1. The load voltage then becomes equal to v_{ab}. In this way the thyristors are fired in sequence and successively line voltages appear across load as shown in fig.(b).

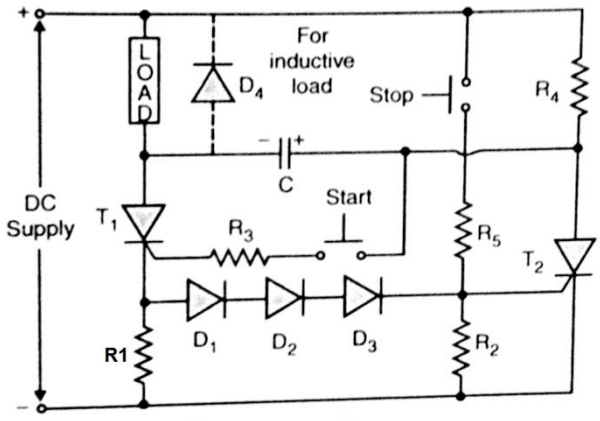
Since the load is purely resistive, the load current follows same variations as that of load voltage. The waveform of load current is similar to the load voltage waveform as shown in the fig.(b).

5 **Attempt any FOUR of the following** **16**

5a) Draw the circuit diagram of DC static circuit breaker and give its operation.

Ans:

DC Static Circuit Breaker:



DC static Circuit Breaker

The figure shows circuit configuration of DC static circuit breaker using SCR. When the 'Start' button is momentarily pressed, the SCR T_1 receives gate current through R_3 and starts to conduct. The turning on of T_1 causes major part of DC supply voltage to appear across the load and power is delivered to load. The capacitor C charges to load voltage with polarity as shown in the figure, through R_4. 2 marks for circuit diagram 2 marks for operation

If we attempt to break the DC load current i.e switch off the load, using mechanical contact type switch, since current is DC, heavy arcing may damage the switch. Instead, if we use this circuit configuration, the load current can be interrupted by turning off the SCR T_1. When 'Stop' button is pressed momentarily, SCR T_2 receives gate current through R_5 and it is turned on. The turning on of T_2 causes the charged capacitor C to place across conducting SCR T_1. The capacitor provides reverse bias across T_1 and discharges quickly through T_2, resistance and T_1. The discharge current is reverse current for T_1 and it is turned off. The load current is then continued through C and T_2. The capacitor C first discharges and then charges with reverse polarity to supply DC voltage. At this instant, the load current falls to zero, and further since current falls below holding current level, T_2 is turned off naturally. Thus manual firing of T_2 by pressing 'Stop' button interrupts load current through T_1.

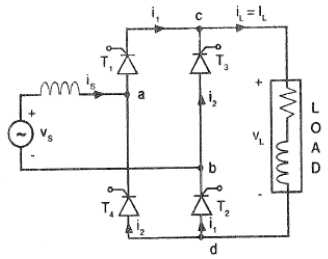
The load current can be automatically interrupted under overload condition. With T_1 on and carrying load current, if overload occurs, the voltage drop across R_1 exceeds the forward voltage drop of string of diodes D_1, D_2, D_3 and gate-cathode junction of T_2. Therefore, gate current is provided to T_2 and it is turned on. Turning on of T_2 immediately causes turning off of T_1 as mentioned above. The load current is interrupted and thus over-load protection is provided. Since no moving contact type mechanism is used for interruption of load current, this

circuit configuration is called DC static circuit breaker. By proper selection of R_1 and number of diodes in string and replacing 'Stop' button by NO relay contact in fault sensing circuit, the circuit can be made to trip and interrupt the overload and fault current.

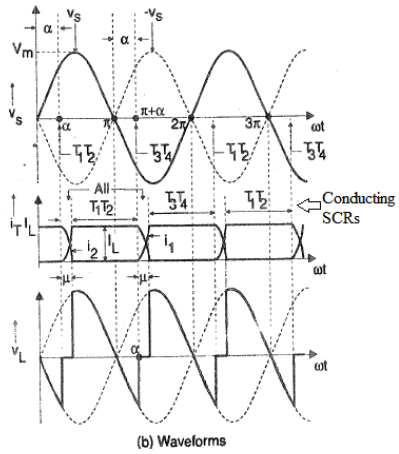
5b) Give the effect of source impedance on converter operation.

Ans:

Effect of source impedance on converter operation:



(a) Circuit diagram



(b) Waveforms

Effect of Source Inductance on the performance of 1-ph full converter.

For single-phase fully controlled bridge converter, the SCRs are triggered in pairs alternately. During positive half-cycle of input, SCRs T_1 and T_2 are triggered whereas during negative half-cycle, SCRs T_3 and T_4 are triggered. When T_1 and T_2 are conducting, T_3 and T_4 are off. On the reversal of supply voltage, firing of T_3 and T_4 causes application of reverse bias across T_1 and T_2 and they are turned off. The current shifts from T_1 T_2 to T_3 T_4. The instantaneous current shift is possible only when the voltage source has no internal impedance. In practice, the source always possesses some internal impedance may be due to the transformer on supply side.

(Circuit diagram & waveforms are optional)

1 mark for effect of source resistance

1) If the source impedance is purely resistive, then voltage drop across it causes reduction in input voltage and ultimately in the output voltage of converter.

3 marks for effect of source inductance

2) If the source impedance is largely inductive, then source current cannot change instantly. The current cannot get transferred immediately from outgoing SCRs to incoming SCRs. The commutation of SCRs is delayed. During current transfer, both pairs of SCRs conduct simultaneously and load voltage appears zero. As both pairs of SCRs conduct simultaneously, this commutation period is called "overlap period (μ)". The output dc voltage is given by,

$$V_{dc} = \frac{2V_m}{\pi} cos\alpha - \frac{\omega L_s}{\pi} I_L$$

As source inductance (L_s) increases, the commutation period (overlap angle μ) increases and as a consequence, the output dc voltage decreases.

5c) Draw a neat circuit diagram of basic parallel inverter and give its operation.

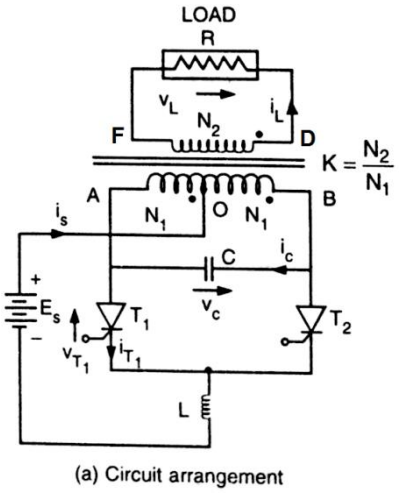
Ans:

Basic Parallel Inverter:

The circuit diagram of basic parallel inverter is shown in fig.(a). The load is connected on the secondary side of centre-tapped transformer. The commutating capacitor C is connected across full primary winding, hence appears effectively in parallel with load. This is the reason why the inverter is termed as parallel inverter.

When T_1 is turned on, the DC source voltage E_s appears across half primary

winding OA, neglecting small voltage drop in inductor L. Due to auto-transformer action, same voltage E_s is induced in other half primary winding OB. Thus total voltage across full primary becomes $2E_s$ with terminal B positive with respect to A. Since capacitor C is in parallel with full primary, it gets charged to $2E_s$ with right plate positive. The voltage is induced in secondary with terminal D positive with respect to terminal F. The charged capacitor C is placed across non-conducting SCR T_2 via conducting SCR T_1. Thus T_2 get forward biased is ready to conduct.



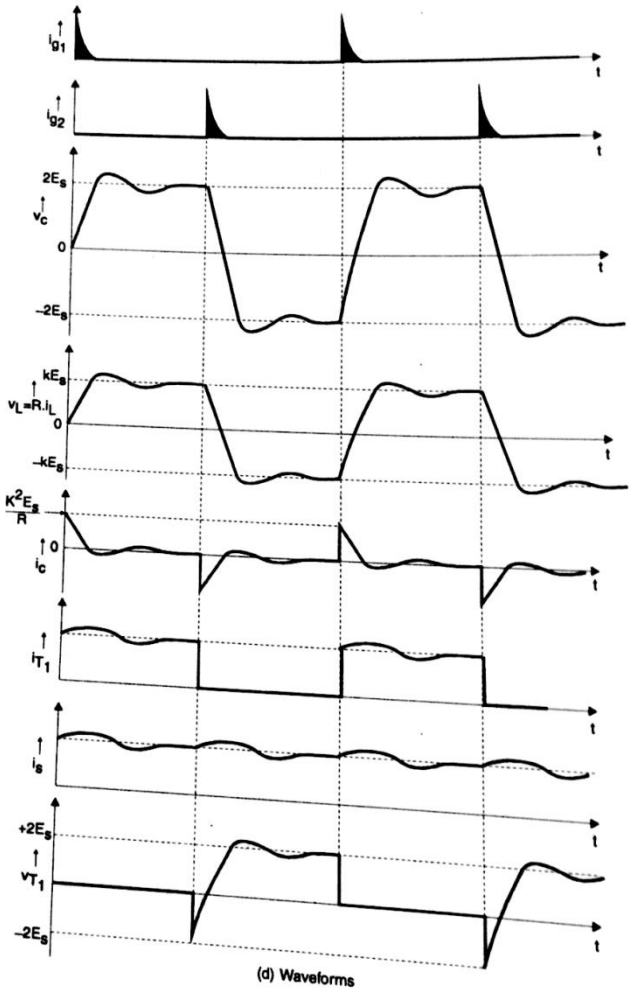
(a) Circuit arrangement

2 marks for circuit diagram

2 marks for operation

When gate pulse is applied to T_2, it is turned on and charged capacitor C is placed across T_1 via T_2. It causes reverse bias across T_1 and it is turned off. The capacitor then discharges through T_2, L and DC source and recharges with opposite polarity to $-2E_s$. Thus primary voltage gets reversed, which also cause reversal of secondary (load) voltage. It is seen that the charged capacitor always provides forward bias to non-conducting SCR. If that SCR is gate triggered, it is turned on and already conducting SCR is turned off due to reverse bias provided by the capacitor placed across it through just triggered SCR.

(Waveforms are optional)



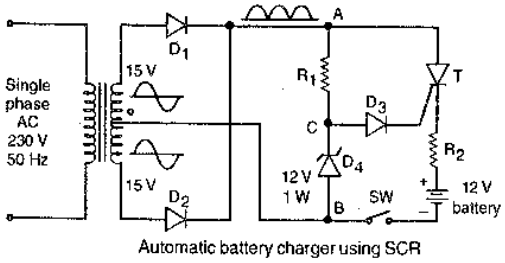
(d) Waveforms

Ideally the voltages across primary and secondary have rectangular waveforms but due to capacitor charging and non-linearities in magnetic circuit, the primary and secondary voltage waveforms appear close to trapezoidal. The waveforms of load voltage, SCR voltage, source current, SCR current and capacitor current are shown in Fig.(d).

5d) Give the operation of battery charger control with a neat diagram.

Ans:

Battery charger circuit using SCR:



Automatic battery charger using SCR

2 marks for circuit diagram

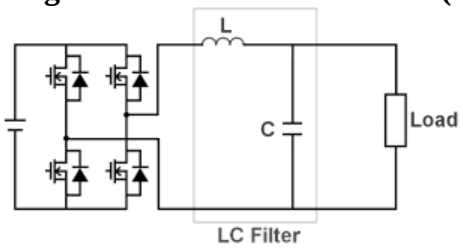
The figure shows the battery charger circuit using SCR. A 12V discharged battery is connected in the circuit and switch SW is closed. The single-phase 230V supply is stepped down to (15-0-15) V by a centre-tapped transformer. The diodes D_1 and D_2 forms full wave rectifier and pulsating DC supply appears across terminals A and B. When SCR is off, its cathode is held at the potential of discharged battery. During each positive half-cycle, when the potential of point C rises to sufficient level so as to forward bias diode D_3 and gate-cathode junction of SCR, the gate pulse is provided and SCR is turned on. When SCR is turned on, the charging current flows through battery. Thus during each positive half-cycle of pulsating DC supply, voltage across A-B, SCR is fired and charging current is passed till the end of that half-cycle. Due to Zener diode D_4, the maximum voltage at point C is held at 12V. Due to the charging process, the battery voltage rises and finally attains full value of 12V. When the battery is fully charged, the cathode of SCR is held at 12V. So the diode D_3 and gate-cathode junction of SCR cannot be forward biased, since the potential of point C can reach up to 12V. Therefore, no gate current is supplied and SCR is not fired. In this way, after full charging, further charging is automatically stopped.

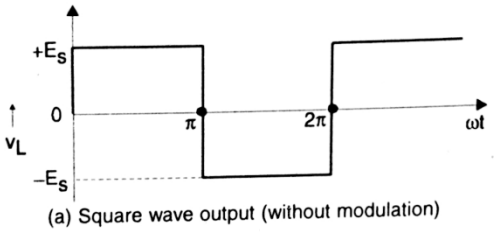
2 marks for operation

5e) Give the operation of single PWM using LC filter with a neat diagram.

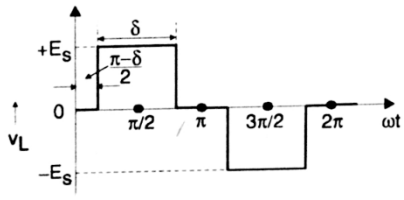
Ans:

Single Pulse-Width-Modulation (PWM):





(a) Square wave output (without modulation)



b) Quasi-square wave output (output with modulation)

1 mark for circuit diagram

2 marks for explanation

1 mark for waveforms (too much mathematical treatment not expected)

The circuit arrangement of Single PWM inverter with LC filter is shown in the figure above. The output voltage of bridge inverter is normally a square-wave as shown in fig.(a). The output voltage amplitude E_s depends on the input DC supply voltage.

In PWM control, the operation of inverter is controlled such that the width of the pulses in output is controlled. Varying the width of output pulses to control the output voltage is called Pulse Width Modulation (PWM).

In single-pulse modulation (SPM), the output pulse is delayed at start and advanced at the end by equal interval $(\pi-\delta)/2$, as shown in fig.(b), where δ is the

pulse width. Such a wave is called a quasi-square wave. In SPM control, the width of a pulse δ is varied to control the inverter output voltage.
From Fourier analysis, it is seen that the amplitude of the n^{th} harmonic component in quasi-square wave is given by,

$$V_{Lnm\_Qsw} = \frac{4E_s}{n\pi} \sin\left(\frac{n\delta}{2}\right)$$

The peak value of the fundamental component for pulse width δ is given by,

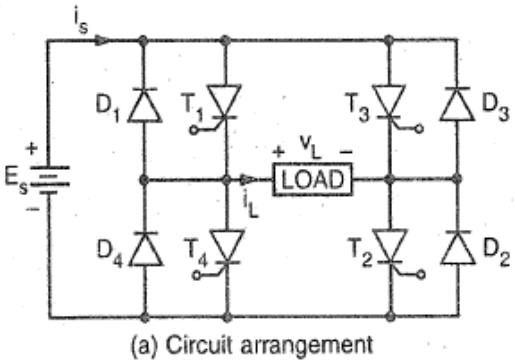
$$V_{L1m\_Qsw} = \frac{4E_s}{\pi} \sin\left(\frac{\delta}{2}\right)$$

From above equation it is clear that peak value of the fundamental component is sinusoidal function of (δ/2). Thus by controlling the pulse width δ, the peak and rms output voltage can be controlled.

5f) Draw a neat circuit diagram of single phase full bridge inverter with RL load and give its operation.

Ans:

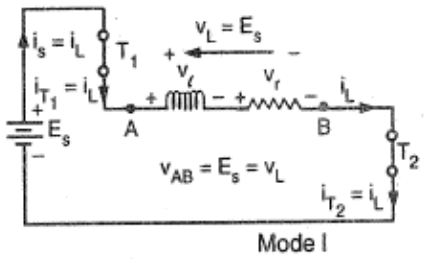
Single phase full bridge inverter with R-L load:



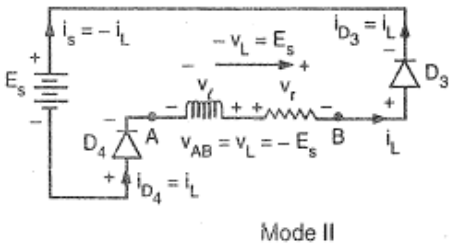
(a) Circuit arrangement

The circuit arrangement for single-phase full bridge inverter with R-L load is shown in fig.(a). All the SCRs are forward biased by the input DC source. When T_1 $T_2$are turned on, load voltage becomes positive and when T_3 T_4 are turned on the load voltage becomes negative. For inductive load the circuit operation is divided in four modes:

2 marks for circuit diagram

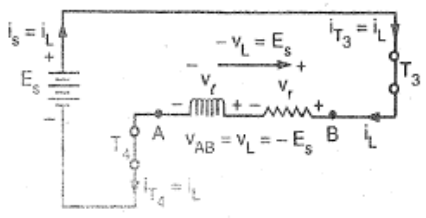


Mode I

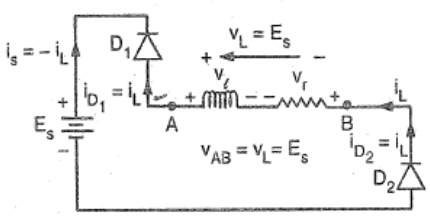


Mode II

2 marks for explanation (waveforms are optional)



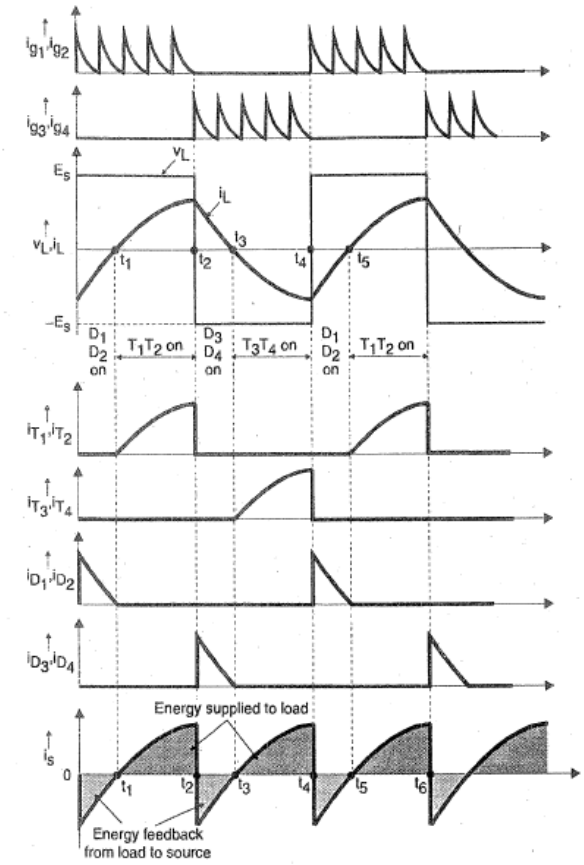
Mode III



(d) Mode IV

Mode I (t_1 to t_2): By gate pulses, the SCRs T_1 $T_2$are turned on at t_1. The supply voltage E_s appears across load, the load current starts rising gradually due to

inductive nature of load. The power flows from input DC source to load. During this mode the energy received by load is partly stored by its inductance.



Single-phase, full-bridge inverter waveforms

Mode II (t_2 to t_3): At t_2 the gate pulses of T_1 T_2 are prohibited and they are turned off by commutating components. Due to load inductance, the load current cannot be reduced to zero suddenly. The load current is maintained in the same direction by load inductance voltage. The load current flows through diode D_3, DC source E_s, diode D_4 and load. Due to conduction of diodes D_3 and D_4, the load voltage appears to be negative. The load power therefore becomes negative i.e load returns or supplies back power to DC source. With energy feedback, load inductance loses its energy. So the load current slowly decreases and finally falls to zero. So far diodes are conducting, reverse bias is maintained across T_3 T_4 and they cannot be turned on.

Mode III (t_3 to t_4): At t_3 the SCRs T_3 T_4 are turned on by gate pulses. The DC source voltage E_s appears as reversed voltage across load. The load current is also reversed and starts to establish. Since load inductance has already lost its energy, it starts absorbing energy from DC source. Thus during this mode, the load receives energy from DC source, just similar to mode I, but with reversed voltage and current. At t_4 gate pulses of T_3 T_4 are prohibited and they are turned off by forced commutation circuit.

Mode IV (t_4 to t_5) or (0 to t_1): The turning off of T_3 T_4 would block the current, but due to load inductance, the load current is maintained in the same reversed direction by forcing it through diodes D_1 and D_2 and DC source E_s. Through diodes D_1 and D_2, the load voltage appears to be positive, making load power negative i.e load returns or feedback the power to load.

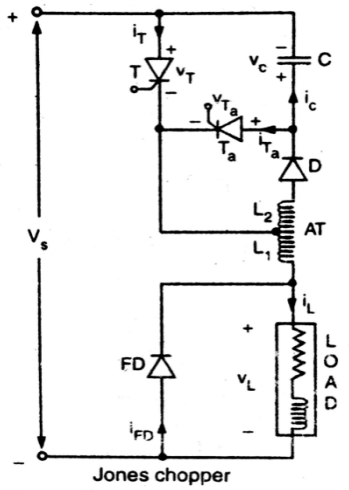
The waveforms of load voltage, load current, SCR currents, diode currents are shown in the figure.

6 **Attempt any FOUR of the following** **16**

6a) Draw a circuit diagram of Jones chopper and give its operation.

Ans:

Jones Chopper:



Jones chopper

The circuit diagram of Jones Chopper is shown in the figure. It employs class D commutation technique in which a charged capacitor is switched by an auxiliary SCR to commutate the main SCR. The circuit operation can be divided into various modes as follows:

Mode 1: In this mode, the main SCR T is triggered at start and then it conducts the load current. Since L_1 and L_2 are coupled inductors, the applied voltage across L_1 results in emf induced in L_2. This emf charges the capacitor C with shown polarity through diode D and conducting T. When capacitor is fully charged, the charging current falls to zero and cannot reverse due to diode.

2 marks for circuit diagram

2 marks for operation

Mode 2: In this mode, the auxiliary SCR T_a is triggered. Once T_a is turned on, the charged capacitor C is placed across main SCR T so as to apply reverse bias across it. Due to this reverse bias and alternate path provided by C and T_a to the load current, the main SCR is turned off. The load current now flowing through C and T_a causes capacitor to discharge fully.

Mode 3: The inductance L_1 and load inductance try to maintain the load current through C and T_a. The load current charges the capacitor with reverse polarity i.e upper plate positive. With rising capacitor voltage, the load current attempts to fall. To maintain the falling load current, the inductive voltages in L_1 and load changes their polarity. The reversal of load voltage V_L forward biases the free-wheeling diode and it conducts. The capacitor gets overcharged due to the energy supplied by V_s and L_1. The load current falls below holding current level of T_a , hence T_a is turned off.

Mode 4: The overcharged capacitor C, with upper plate positive, then starts discharging through V_s, FD, L_1, L_2 and D. The discharging current is in the form of a pulse. At the end of this mode, the capacitor voltage falls to a level less that V_s and therefore current falls to zero and attempts to reverse but diode stops conducting.

Mode 5: The capacitor voltage with upper plate positive is maintained till the next firing of T. The load current is continued through free-wheeling diode till the next conduction of main SCR T.

Jones chopper offers flexible control and effective use of trapped energy in coupled inductors. There is no starting problem and any SCR can be triggered at start.

6b) Give the operation of static VAR compensation system with a neat diagram.

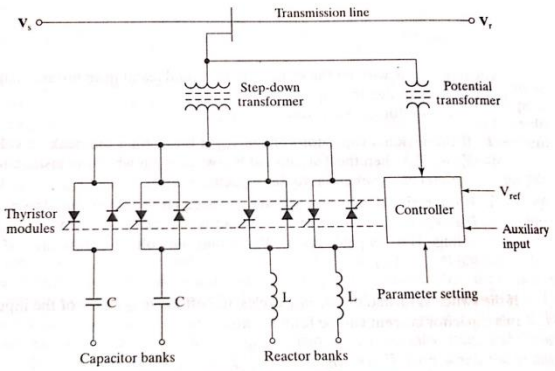
Ans:

Static VAR compensator:

Static VAR compensation is a process of compensating the reactive power in the power system using static switches (semiconductor switches). In this

process, the reactors and capacitors are switched to absorb or supply the reactive power respectively. 2 marks for operation

Static VAR compensators (SVC) consists of combinations of thyristor controlled reactor (TCR), thyristor switched capacitor (TSC) and fixed capacitor (FC). The electrical transmission and distribution networks are dominantly reactive in nature. During no or light load condition, the line capacitances play major role to produce the reactive power. If this reactive power is not absorbed by load then voltage rises and may cross the limit. In this situation, TCR is used to insert reactors in power system to absorb the reactive power. During peak load condition, most of the loads are inductive and they demand the reactive power. In this situation, TSC is used to insert capacitors in power system to generate the reactive power. 2 marks for diagram



General arrangement of static VAR compensator

In fact, SVC comprises combinations like (TCR+TSC), (TCR+FC) as per the need.

In TCR, phase control is used to vary the effective inductance of the inductor.

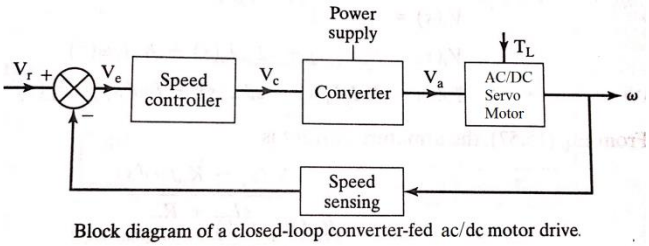
In TSC, the integral-cycle control is employed to vary the effective capacitance of the capacitor.

6 c) Give the operation of closed loop speed control method for DC servomotor with a neat diagram.

Ans:

(Examiner is requested to consider any other correct scheme as valid answer)

Closed loop speed control method for DC servomotor:



Block diagram of a closed-loop converter-fed ac/dc motor drive.

A general scheme of closed loop speed control for servomotors is shown in fig. For both types of servomotors, voltage control based speed control scheme is used. DC servomotor is fed from ac-dc converter and AC servomotor is fed from ac controller or inverter. The speed of motor changes with the load torque. To maintain a constant speed, the motor voltage should be varied continuously by varying the delay angle converter. In practical drive systems it is required to operate the drive at a constant torque or constant power with controlled acceleration and deceleration. A closed-loop control system has the advantage of improved accuracy, fast dynamic response and reduced effects of load disturbances and system nonlinearities. 2 marks for block diagram

2 marks for operation

If the speed of servomotor does not match with the set speed, the speed error V_e increases. The speed controller responses with as increased control signal V_c.

This control signal changes the operation of converter and voltage supplied to servomotor is changed so as to minimize the speed error.

6d) Give the principle of dielectric heating control with a neat diagram.

Ans:

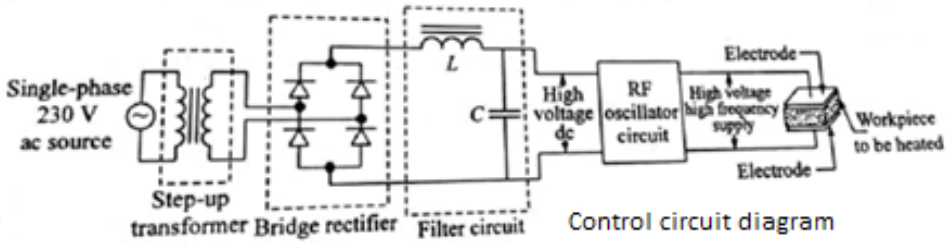
Principle of Dielectric Heating:

The non-conducting materials (also called insulators or dielectric materials) whenever subjected to an alternating electric field, some power loss takes place in them and heat is generated. This power loss is called "Dielectric Loss". The process wherein the heating takes place due to dielectric loss is known as "Dielectric Heating".

2 marks for Explanation

When dielectric material is subjected to an alternating electric field, the rapid reversal of the field distorts and agitates the molecular structure of the material. The internal molecular friction generates heat uniformly throughout all parts of the material. Even though the material is poor conductor of heat and electricity, thick layers of material can be heated in minutes instead of hours.

Thyristors are used in inverter which converts DC into high frequency AC. This high-frequency supply is applied across the electrodes to heat up the work-piece dielectric material, as shown in the following diagram.



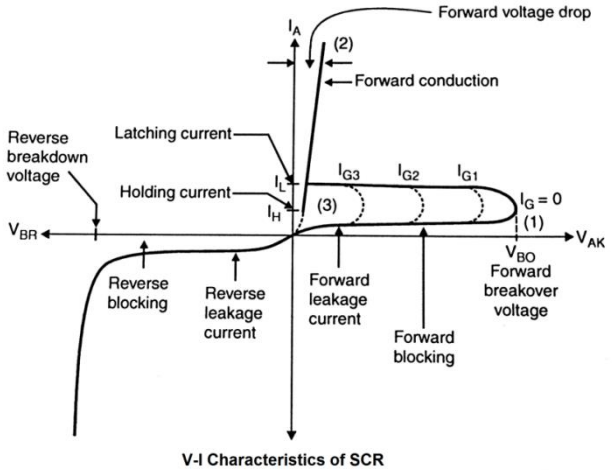
Control circuit diagram

2 marks for Control circuit diagram

6e) Draw a neat labelling VI characteristics of SCR and explain the region.

Ans:

V-I characteristics of SCR:



V-I Characteristics of SCR

2 marks for labeled diagram

1 mark for partially labeled diagram

Operating regions:

1) **Forward Blocking region**: In this region, the SCR is forward biased but not triggered. It carries only forward leakage current. The SCR in this region is treated as OFF switch.
2) **Forward conduction region**: In this region, the SCR conducts the

forward current and latched into conduction after triggering. The SCR in this region is treated as ON switch.

3) **Reverse blocking region**: In this region, the SCR is reverse biased, hence carries only reverse leakage current. The SCR in this region is treated as OFF switch.
4) **Reverse conduction region:** In this region, the SCR conducts the reverse current after the breakdown of reverse biased junctions. The SCR get damaged if operated in this region.

2 marks for four regions and proportionally reduced if all not covered.