Q.1 A) Attempt any four of the following: (3 * 4 = 12)

a) Write the functions of the following TTL IC's :

i) 74LS181 ii) 74LS373 iii) 74LS245 iv) 74LS83

Ans:- Function of following IC's (**1M each point)**

i) 74LS181- 4 bit ALU

ii) 74LS373-8 bit Latch

iii) 74LS245-Octal bus Trans-receiver/Bidirectional buffer

iv) 74LS83- 4 bit adder

b) State the function of the following pins of 8085 :

i) ALE ii) IO / $\overline{M}$

Ans :- Function of following 8085 pins (**Each pin 1.5 M)**

1) ALE: Address Latch Enable
-Used to demultiplex lower order address and data lines
-When ALE is low it indicates contents on AD0 to AD7 lines is 8 –bit data
-When ALE is high it indicates contents on AD0 to AD7 lines is lower order address

2) IO/$\overline{M}$: Input Output Memory
-This signal indicates input/output or memory operation
- When IO/$\overline{M}$ pin is low it indicates memory operation
-When IO/$\overline{M}$ pin is high it indicates input/output device operation

c) Compare volatile and non – volatile memory
Ans:- **(Any 3 valid points,01 mark for each point)**

Volatile Memory	**Non-Volatile Memory**
1)Information stored is lost when power is turned off	1) Information is not lost
2)Temporary memory	2) Permanent memory
3)Read /write operation is possible	3) only read operation is possible
4) ALL RAM's	4) ROM's EPROM etc

d) Give Maximum memory capacity which can be accessed by 8085. State the reason for the same

Ans :- Maximum memory capacity of 8085 is 64K **(1m)**

8085 has 16 address lines so one can access 2^{16} = 64K bytes of memory **(2m)**

e) Draw block diagram of 4 bit BCD adder using IC 7483 and gates.

Ans: - **(correct diagram 4M)**

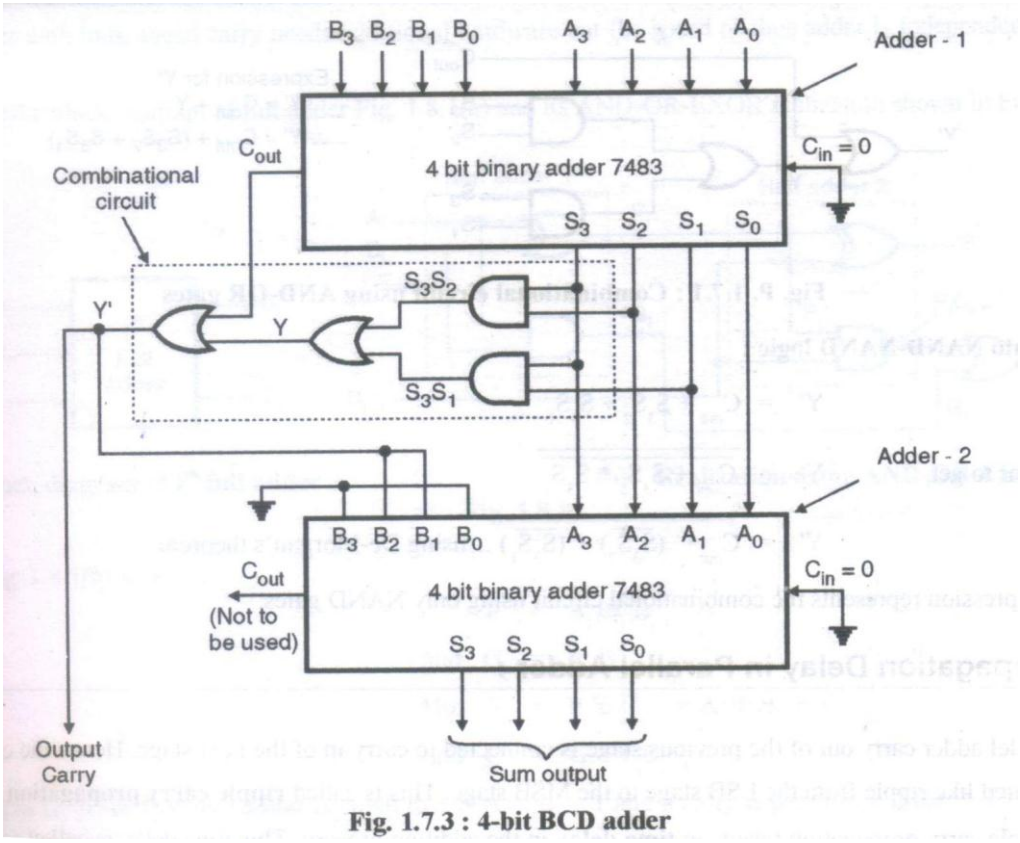


Fig. 1.7.3 : 4-bit BCD adder

Note:- Diagram drawn using NAND gates only should also be given 4M

f) What is priority encoder

Ans :- **(03 marks)**

Priority encoder is a combinational circuit .Priorities are given to input line. When two or more input lines are active at the same time then then the highest numbered input line is given the highest priority .

Q.1B) Attempt any two :- **(2 * 4 = 8)**

a) List the addressing modes of 8085, also write example of each

Ans :- **(2M For any 4 addressing modes and 2M for any valid example)**

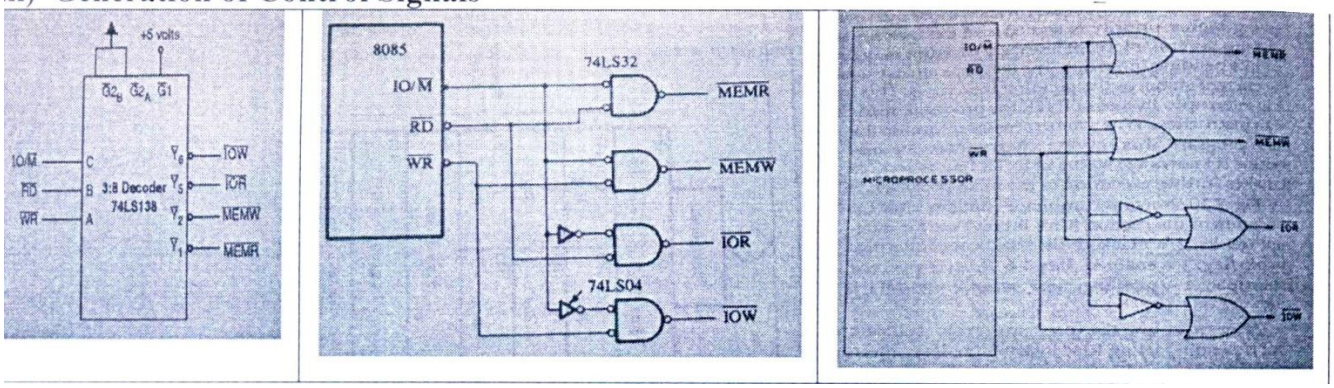
a) Addressing modes

-Register Addressing E.g. MOV B,C

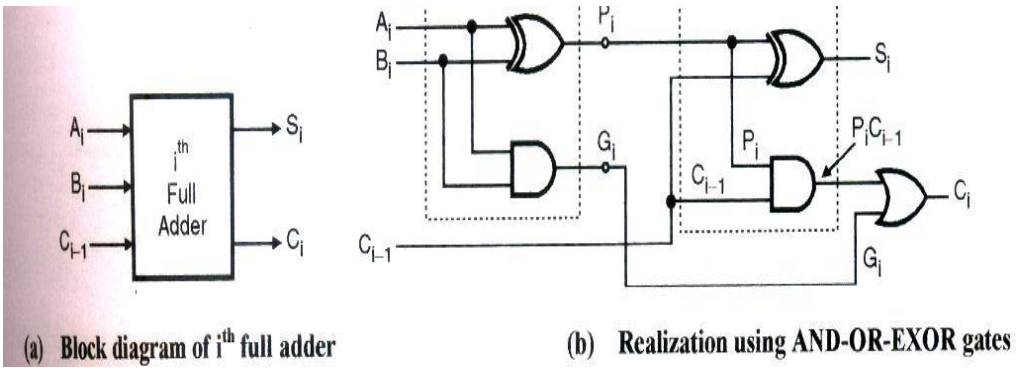
-Immediate Addressing E.g. MVI b, 05H
-Direct Addressing E.g. LDA 6000H
-Indirect Addressing E.g.MOV A,M
-Implied Addressing RAR

b) How control signal such as MEMR, MEMW, IOR and IOW are generated
Ans:- **(4M for any of the following figure)**

ii) Generation of Control Signals



c) What are carry look ahead adders. What are its advantages.
Ans:- **(2M for diagram 1M for explanation 1M for any two advantages)**



-Carry look ahead adders eliminate the problem due to interstage carry delay
-speeds up the addition process
-Requires additional hardware
-speed of adder is independent of number of bits
-The variable Gi is known as Carry generate its value does not depend on input carry
Gi=AiBi
- The variable Pi is known as Carry Propogate it is associated with the propogation of carry from C_{i-1} to ci
Pi=Ai EX-OR B

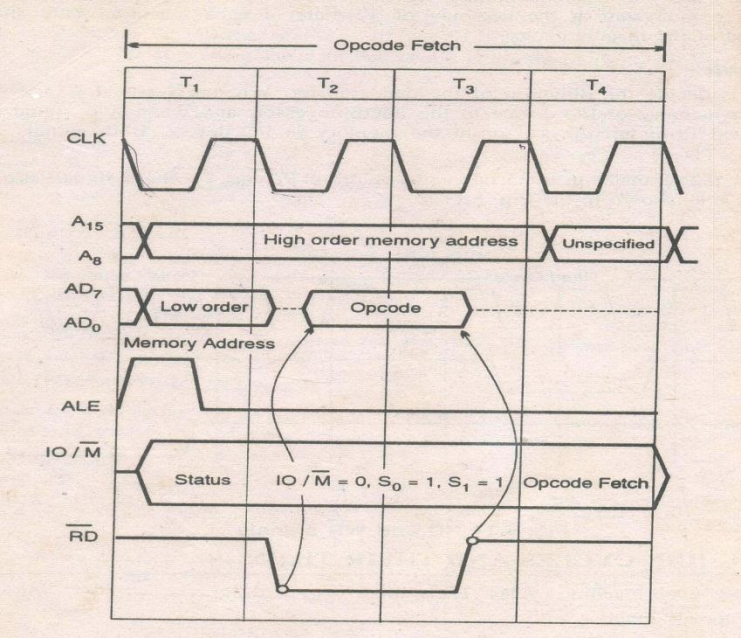
Advantages
-speeds up addition
-Propogation delay of only two gates will be involved
-Eliminates the problem of ripple carry

Q.2) Attempt any four of the following:- **(4 * 4 = 16)**

a) Draw the timing diagram of op- code fetch cycle

Ans: - **(full correct diagram 4 marks)**

TIMING DIAGRAM OF OPCODE FETCH MACHINE CYCLE



b) Register B contains $(FF)_H$. What will be the content of register B and Status of flag registers every time when INRB instruction is executed voice

Ans: - **(2marks for each INR B operation)**

B=FFH

first INR B

BEFORE EXECUTIONOF INR B CONTENTS OF B =FFH

AFTER EXECUTION OF INR B CONTENTS OF B =00H

CY=1 , Z=1 ,P=1 ,AC=1,S=0

Second INR B

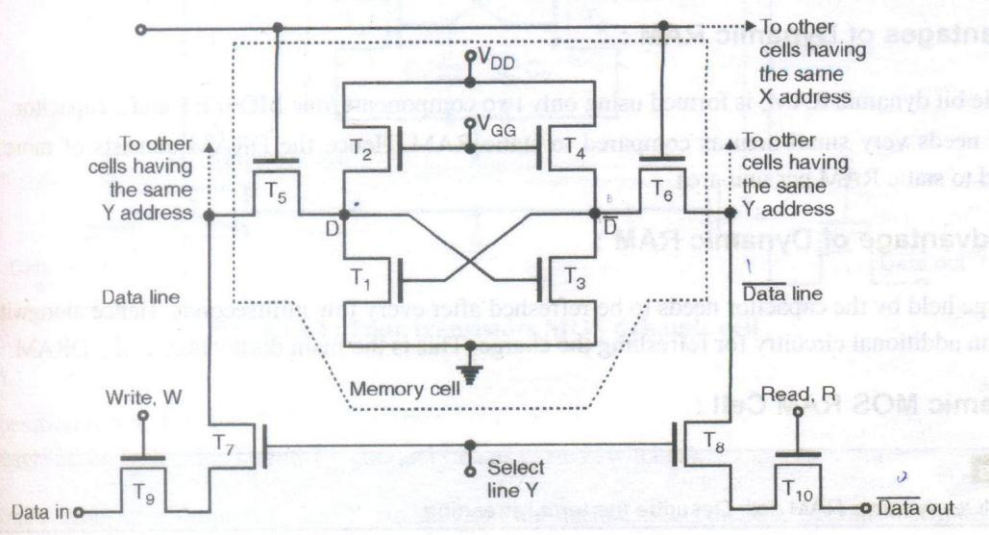
BEFORE EXECUTION OF INR B CONTENTS OF B =00H

AFTER EXECUTION OF INR B CONTENTS OF B =01H

CY=0 , Z=0 ,P=0 ,AC=0,S=0

c) Explain static RAM cell with N – MOS cell

Ans:- **(2 marks for diagram , 2 marks for explanation)**



Static RAM cell with NMOS CELL

T2 & T4 are acting as resistances. X & Y lines are used for addressing cell.

When X=Y=1 (high) ,the cell is selected . When X=1, the MOSFETS T5 & T6 are turned ON .,which will connect memory cell to the data line and data bar line.

When Y=1 ,the MOSFETS T 7 & T8 are turned ON .,which will make read & write operation possible

d) Compare software and hardware interrupt

Ans:- **(Any four valid points expected. Any other valid comparison points can be considered**

(01 mark for each comparison point)

Sr. no	**Software interrupt**	**Hardware interrupt**
1.	Generated by execution of interrupt instruction	Generated by external I/O device
2.	PC is incremented	PC is not incremented
3.	Cannot be ignored or masked	Can be ignored or masked
4.	It is synchronous event	It is asynchronous event
5.	e.g. RST 0 TO RST 7	RST 5.5,RST 6.5,RST 7.5,TRAP,INTR

e) What operation will be performed by following instructions

i) MVI B , 00H ii) LDAX B iii) ANI FFH iv) XRI 00H

Ans: - **(one mark for each instruction operation)**

i) **MVI B,00H**: Move immediately data 00h to Register B. (B=00H)

ii) **LDAX B:** Load accumulator with the contents of memory location pointed by BC register pair

iii) **ANI FFH :** Logically AND contents of accumulator with immediate data FFH and store result to accumulator.

iv) **XRI 00h :** Logically ex-or contents of accumulator with immediate data 00h and store result to accumulator

f) Compare I/O mapped I/O and memory mapped I/O (4 points)

Ans:- **(Any four valid points expected. Any other valid comparison points can be considered**

One mark for each comparison point)

Sr. no	**I/O MAPPED I/O**	**MEMORY MAPPED I/O**
1.	Device address is 8 bits	Device address is 16 bits
2.	Control signals used are $\overline{IOR}$ and $\overline{IOW}$	Control signals used are $\overline{MEMR}$ and $\overline{MEMW}$
3.	256 input and output devices can be interfaced using this technique	Theoretically 65536 (2^{16}) devices can be interfaced using this technique
4.	IN ,addr and OUT, addr instructions are used for accessing I/O devices	All memory related instructions are used for accessing I/O devices
5.	Data transfer is possible between only Accumulator and I/O devices.	Data transfer is possible between any register and I/O devices
6.	Execution speed is 10 T-states	Execution speed varies from 7 T-states to 13 T-states
7.	Arithmetic and logical operations are not possible	Arithmetic and logical operations are possible
8.	Decoding 8 bit address requires less hardware	Decoding 16 -bit address requires more hardware

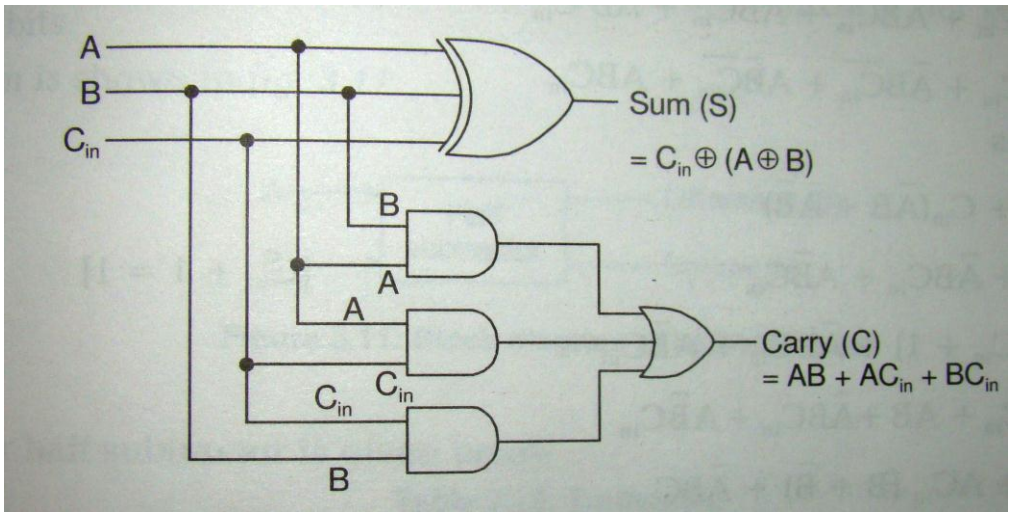
Q. 3. Attempt any FOUR of the following. (4x4 = 16 marks)

a) Designing full adder using basic gates.

Ans.:- **(2 marks –truth table, 2 marks- diagram)**

Truth table for full adder:-

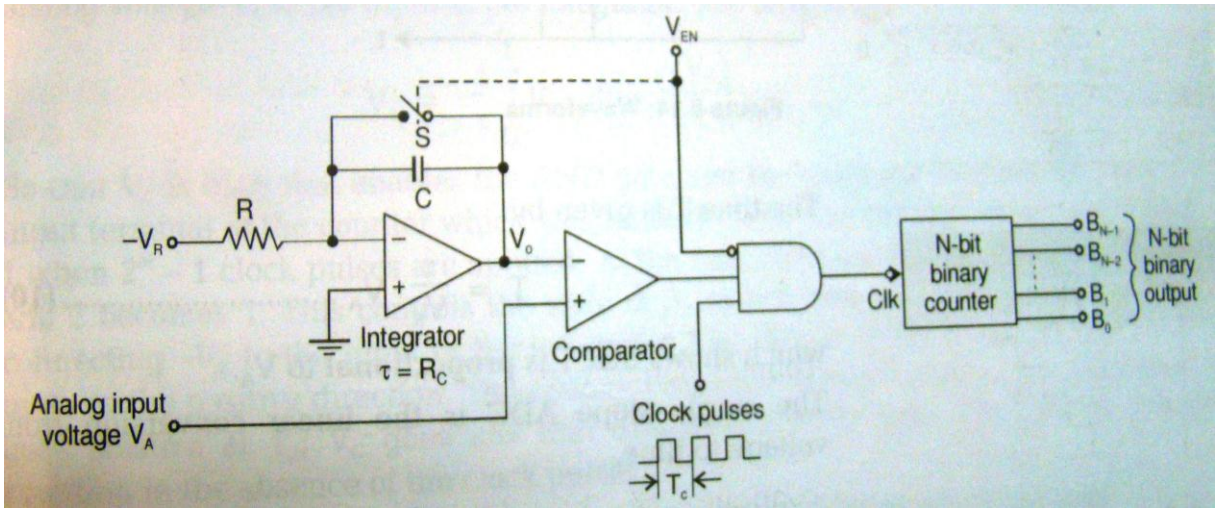
inputs			outputs	
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1



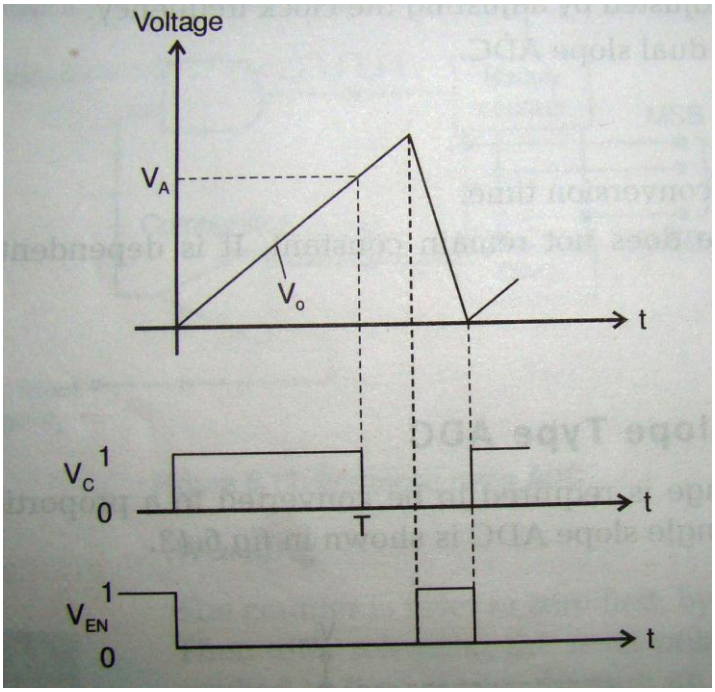
b) Draw and explain single slope ADC.

Ans.:- **(for diagram – 2marks, for waveforms – 1mark and description – 1mark)**

Single Slope ADC :- Here the analog voltage is required to be converted to a proportional time period. The circuit diagram of single slope ADC is shown in fig.



Working :- A negative(–ve) reference voltage $-V_R$ is applied to an integrator, whose o/p is connected to the inverting i/p terminal of the comparator. The analog voltage V_A is is applied at the non – inverting i/p terminals of the comparator. The o/p of the comparator Vc is at logic level 1 as long as the o/p of the integrator Vo is less than V_A , when Vo crosses VA at = T, Vc goes low. The AND gate is enabled when V_{EN} is low and switch remains open. When V_{EN} goes high, the switch S is closed so that capacitor discharges. Also the AND gate is disabled. When AND gate is enabled the clock pulse will reach the clock (clk) i/p terminal of the counter. The o/p of the counter is the digital o/p corresponding to V_A.



The time T is given by

$T = \tau / V_{R.} \times V_A$ ……(10)

Which shows that T proportional to VA.?

The single slope ADC is the linear conversion from voltage to time.

c) Write a program to exchange the content of register pair DE and BE. Assume suitable data and write result after execution.

Ans.:- (Program assumption – 1mark, result after execution – 1 mark and program – 2 marks)

(Program can also be written using MOV instruction)

Assume:- B = 32 h, C = 19 h, D = 52 h, E = A2h

Result :- D = 32 h, E = 19 h, B =52 h, C =A2h.

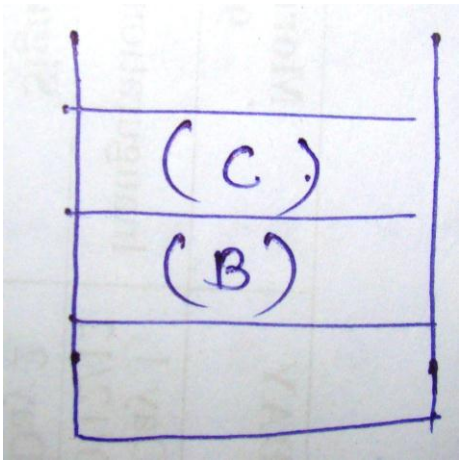
```
LXI   B, 3219h
LXI    D, 52A2h
XCHG.
HLT
```

d) Explain PUSH and POP instruction.

Ans.:-

PUSH B :- **(2marks)**

- Push or copy the content s of BC register pair in stack memory.
- Decrements stack pointer by 2.



FFFF h.

Assume stack pointer initialized at FFFF h.

POP B :- **(2marks)**

- Pop or copy content of stack memory location back to BC pair (first copy low order register i. e. 'c' and then higher order register i. e. 'B')
- Increments Stack pointer by2.

e) Classify the instruction s on the basis of number of byte i. e. length.

i) RAR, ii) DCRC, iii) IN80H, iv) LXI H, 0000H.

Ans.:- **(each instruction -1 mark)**

i) RAR – 1 byte

ii) DCRC – 1 byte.

iii) IN 80h – 2 bytes.

iv) LXI H, 0000h – 3 bytes.

Q.4) Attempt any four of the following :- (4 * 4 = 16)

a) How many bits are required for a resolution of 5 mV and full scale voltage is 15V

Ans:- **(2m for formula and 2m for correct answer)**

Resolution = $V_{FS}/2^n-1$

$5*10^{-3}=15/2^n-1$

$2^n=2999$

N=12 bits

b) Describe memory IC 2716

Ans: -

FEATURES OF IC 2716:- **(02m for any four features i.e ½ * 4 = 2)**

i) 2048 X 8 organization.
ii) 525mW max active power, 132mW max standby power.
iii) Access time
M 2716-1 is 450 ns.
M 2716 is 350 ns.
iv) Single 5V supply voltage
v) Static – no clock required.
vi) Inputs & output TTL compatible during both read and program modes.
vii) Extended temperature range
viii) Programming voltage : 25V
ix) Three state output with tied or capability.

MODES OF OPERATION: - **(2 marks=1/2m for the names of modes, 1/2 m for each mode explanation)**

2716 has 3 modes of operation

1. Read mode :-
   a. Read operation requires $\overline{G}$=V_{IL} , $\overline{EP}$=V_{IL} and address is stabilized
   b. Valid data will appear on the output pins after time t_{AVQV} or t_{ELQV}
2. Deselect Mode
   a. 2716 is deselected by $\overline{G}$ = V_{IH}. This is independent of $\overline{EP}$ and condition of addresses
   b. Outputs of high impedance (Hi-Z) when $\overline{G}$ = V_{IH}. This allows tied-OR of two or more IC's
3. Stand-by Mode (Power Down)
   a. 2716 is powered down by $\overline{EP}$=V_{IH}.
   b. Independent of $\overline{G}$ automatically puts the output in Hi-Z state. Power is reduced by 25% of normal operating power.

PROGRAMING MODE: - (2 marks=1/2m for the names of modes, 1/2 m for each mode explanation)

2716 has 3 programming modes

a. Program Mode
   1. All bits of 2716 are high initially or after full eraser
   2. It is programmed by introducing "0"s at desired location
   3. Any individual address or sequential address or random address can be programmed.
   4. Any or all 8 bits of a location can be programmed with a single program pulse to $\overline{EP}$ pin

b. Program Verify Mode
   1. Program can be verified one byte at a time during programming or entirely at the end of the program
   2. This is done with Vpp = 25V or 5V in either case.

c. Program Inhibit Mode
   1. This mode allows several 2716 to be programmed simultaneously with different data for each.
   2. All similar inputs may be paralleled. Pulsing the program pin will program a unit, inhibiting the program pulse will keep it from being programmed

- 2716 is a 2048X 8 memory, so 4 IC's are required to get 8 KB memory (2mark)

c) State the function of the following pins.
RESET OUT, READY, TRAP, SOD

Ans: - **(1M for function of each pin)**

RESET OUT: This is a active high signal used to indicate that processor is being reset .It can be used to reset other devices connected in the system

READY: This is an active high input signal used by the processor to check whether a peripheral is ready or not for data transfer. It is used to synchronize slower peripherals to the processor

TRAP: This is active high edge and level triggered non maskable highest priority hardware interrupt.

SOD (Serial Output Data): This signal enables the bit by bit transfer of serial data to the external device.

d) Define the following terms ;
i) Hardware ii) Software iii) BUS iv) Firmware

Ans:- **(1M for each definition)**

HARDWARE: Physical components of system consisting of electronic devices ,Integrated Circuit etc.

SOFTWARE: It is collection of programs .

BUS: A collection of wire through which data is transmitted from one part of computer to Another.

FIRMWARE: Firmware is a program that is embedded in a hardware device .

e) Compare machine language and high level language

Ans:- **(1M each for any 4 valid points)**

Machine language	**High Level Language**
1)Hardware dependent	1)Hardware independent
2)Less memory is required	2)More memory is required
3)Program execution is fast	3)Program execution is slow
4)Not easy to learn	4)Easy to learn
5)Uses binary numbers/codes	5)Uses keywords similar to English

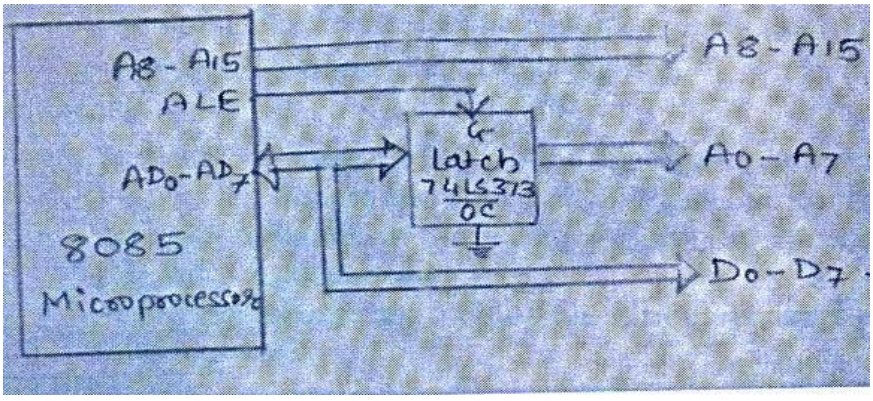
f) Which techniques is used to demultiplex the addresss Bus of 8085 microprocessor. Explain it

Ans:- **(2M for explanation and 2M for diagram)**

- Demultiplexing is a process of separating address and data lines .It is done with the help of

ALE(Address Latch Enable) signal of 8085 and octal latch 74LS373 .

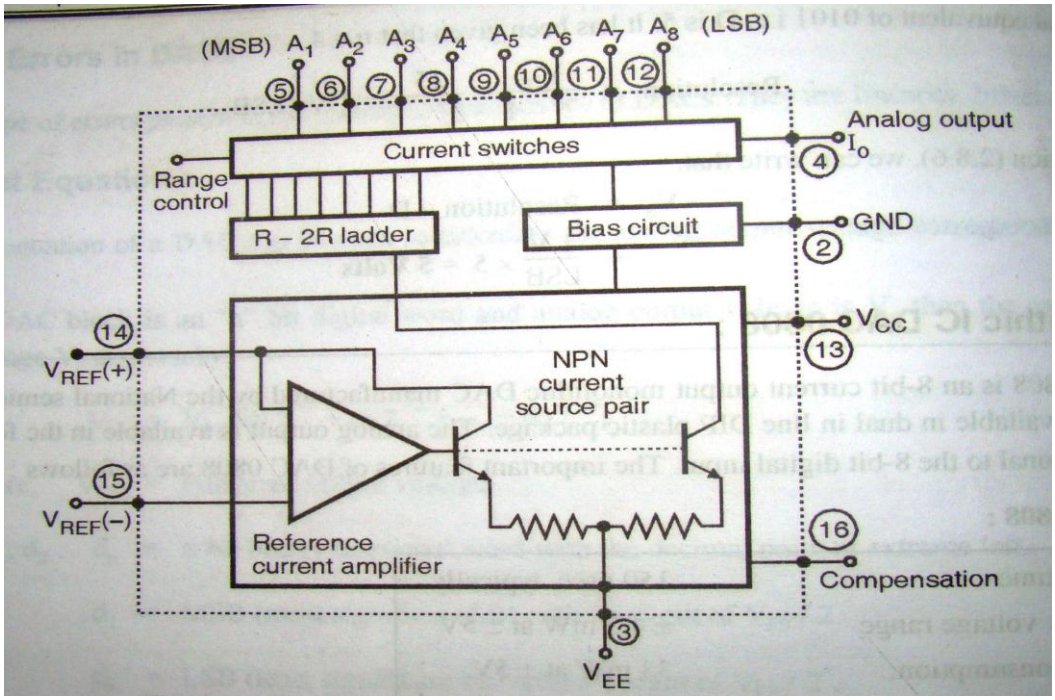
- When ALE is high for T1 state of each machine cycle the lower address is latched in 8-bit latch and the output of latch will be A0-A7
- After T1 state when ALE goes low the lower order address is removed from AD0 to AD7 lines and the same lines are used as data lines D0-D7.



Q. 5. Attempt any TWO of the following. (2x8=16 marks)

a) Draw block diagram of DAC0800. Define accuracy, resolution, linearity, settling time**.**

Ans.:- Block diagram of DAC 0808 :- (**diagram – 4 marks, each definition – 1 mark)**



Accuracy:-

- Accuracy indicates how close the analog o/p is to its theoretical value. In short it indicates the deviation of actual o/p from the theoretical value.

OR

- Accuracy is always specified in terms of percentage of the full scale o/p that means maximum o/p voltage e.g. if the full scale o/p is 15v and accuracy is ± 0.1 percent then the maximum error is given by 0.001 x 15 = 0..15v or 15mv.

Resolution:-

- Resolution describes the smallest possible change in the analog o/p voltage. Resolution should be as high as possible.

or

- Its value depends on the number of bits in the digital i/p applied to DAC. Higher the number of bits, higher is the resolution. Resolution of a DAC can be defined in two different ways.

or

- Resolution number of different analog o/p voltage value that can be provided by a DAC. For an n-bit DAC, Resolution = 2^n.

or

- Hence the resolution of a 4 – bit DAC is $2^4 = 16$ and that of a 3 – bit DAC is $2^3 = 8$. Hence resolution increases with the increase in number of bit.

Linearity :-

- The relation between the digital i/p and o/p should be linear. However practically it is not so due to the error in the value of resisters used for the resistive network.

Settling time:-

- Theoretically the analog o/p voltage should change instantaneously in response to the change in its digital i/p.

or

- The time required to settle the analog o/p within ½ LSB of the final value, after the change in digital i/p is called as settling time. The settling time should be as short as possible.

b) Draw complete interfacing diagram of 4k x 8 RAM to 8085 and also write complete memory map.

Ans.:-

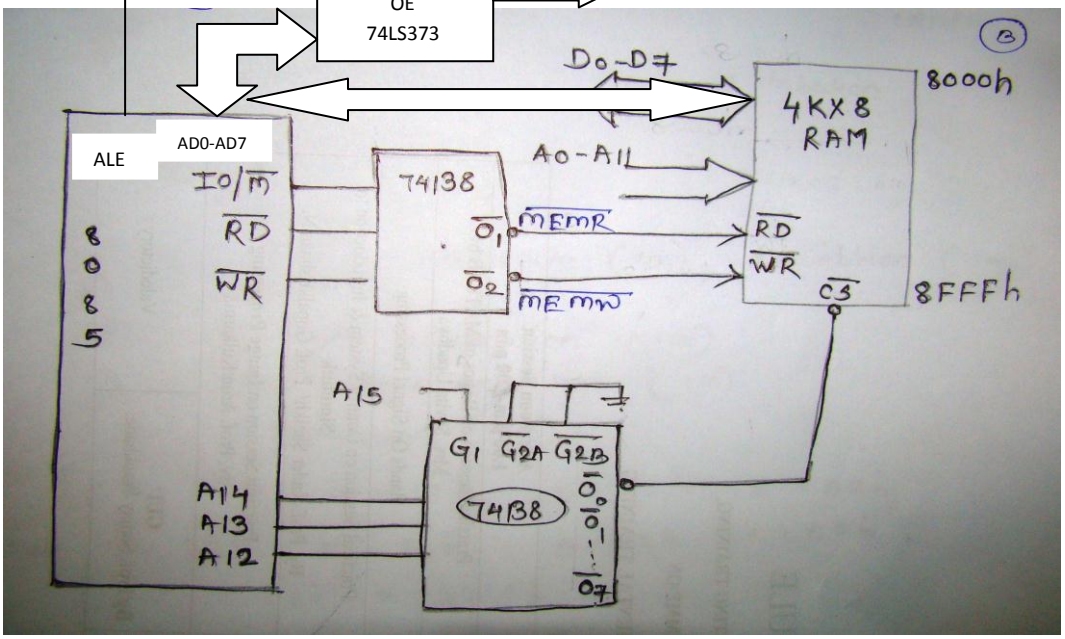
4kx8 RAM:- 2^{12} = 4k, 12 common address lines

i. e. ($A_0 – A_{11}$) .. …… **. (1Mark)**

	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
8000h	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
8fffh	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1

Any address is valid.

A0-A7 **(3 marks)**



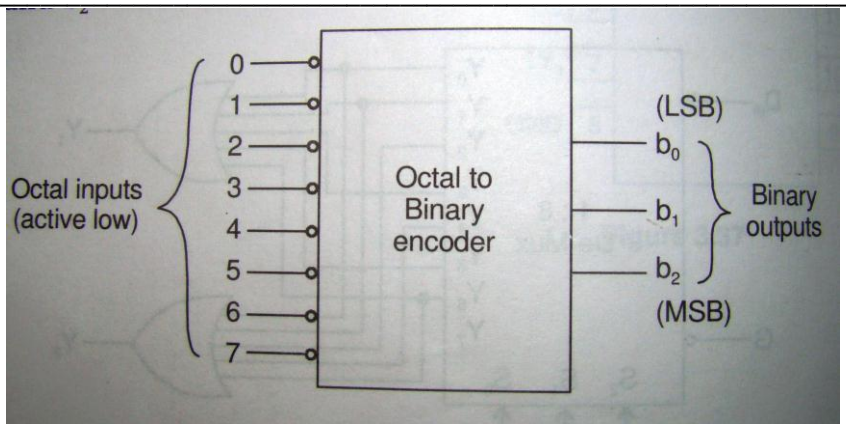
(diagram – 4 marks)

c) i) Explain octal to binary encoder. ii) Explain R- 2R ladder DAC.

Ans.:- **(2 –marks diagram, 2 truth table)**

i) octal to binary encoder:-

(generalized block diagram should be considered should be given full mark)



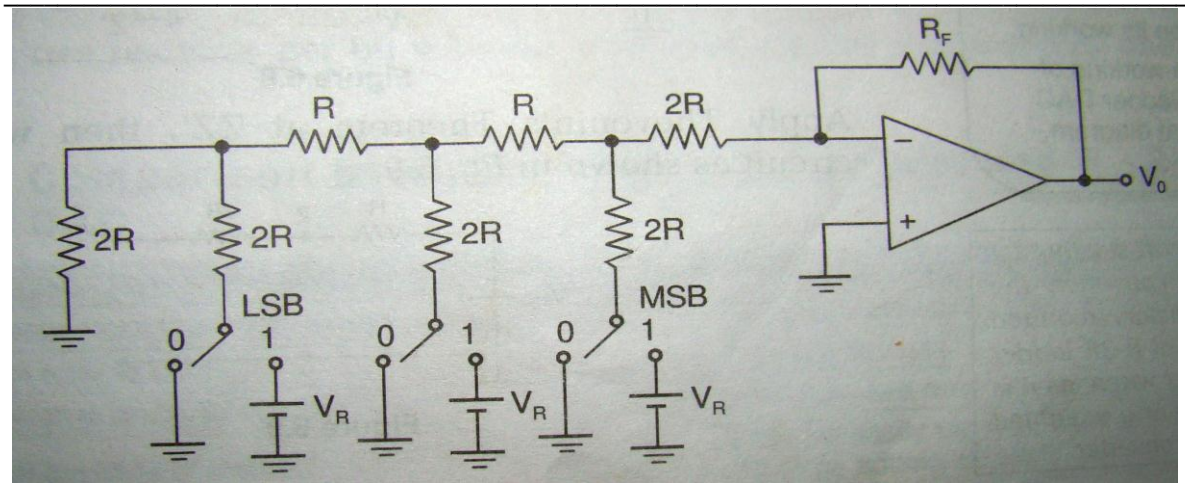
In octal to binary encoder eight i/p s corresponding to 0to 7 are represented through switches. These i/ps are active low i/ps. Three bits are required to represent binary output i. e. bo, and b2 which are active high.

Inputs (Active low)								Outputs (Active high)		
$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$	b_2	b_1	b_0
0	1	1	1	1	1	1	1	0	0	0
1	0	1	1	1	1	1	1	0	0	1
1	1	0	1	1	1	1	1	0	1	0
1	1	1	0	1	1	1	1	0	1	1
1	1	1	1	0	1	1	1	1	0	0
1	1	1	1	1	0	1	1	1	0	1
1	1	1	1	1	1	0	1	1	1	0
1	1	1	1	1	1	1	0	1	1	1

Here i/p are provided through switches and these are active low hence Block diagram and truth table is given below.

ii) R- 2R ladder DAC:- (diagram – 2 marks, equation -2 marks)

This network overcomes the problems of weighted resister network. It is also a resistive network to produce binary weighted current but uses only two value of resistor as R and 2R. it uses a ladder network containing series and parallel combination of two resistors of values R and 2R. the i/p to the resistor network are applied through digitally controlled switches. A switch is in position 0 or 1 corresponding to the digital i/p for that bit position 0 or 1 respectively.



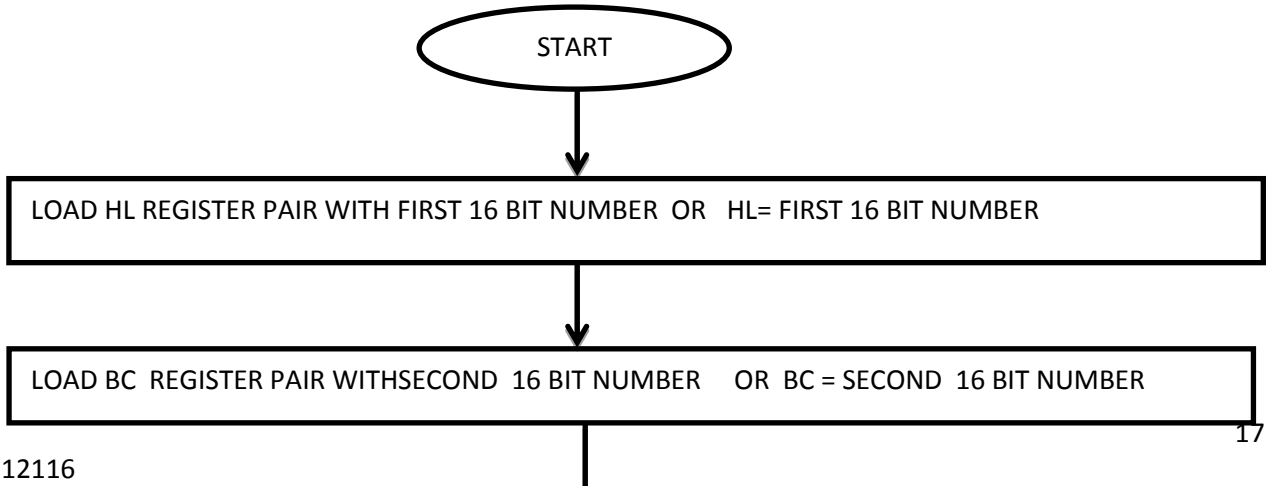
$$V_o = -\left(\frac{R_F}{3R} \cdot \frac{V_R}{2^3} b_0 + \frac{R_F}{3R} \cdot \frac{V_R}{2^2} b_1 + \frac{R_F}{3R} \cdot \frac{V_R}{2^1} b_2\right)$$

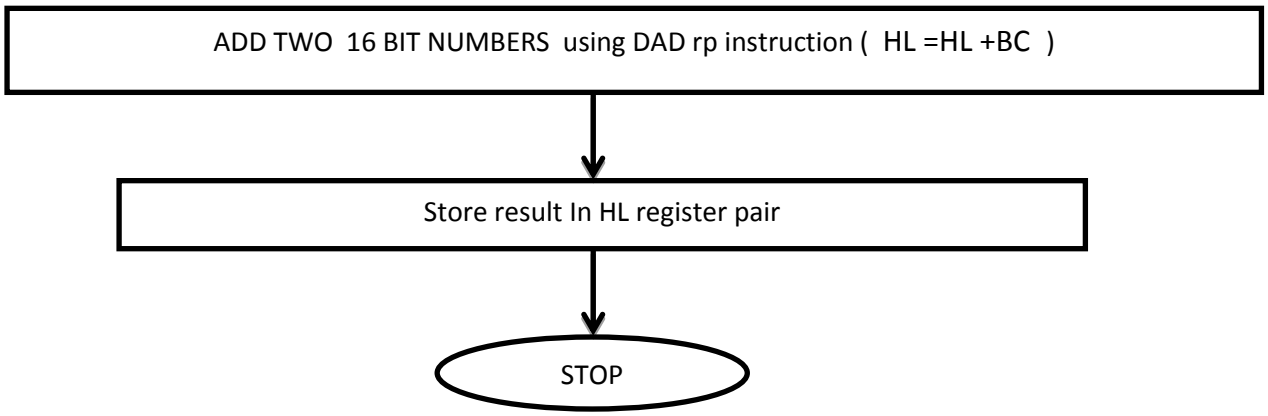
Q.6) Attempt any two of the following : (2 * 8 = 16)

a) Add two 16 bit numbers, Stored in HL and BC register pair. Store result in HL pair. Draw flow chart. Assume suitable data and write after execution.

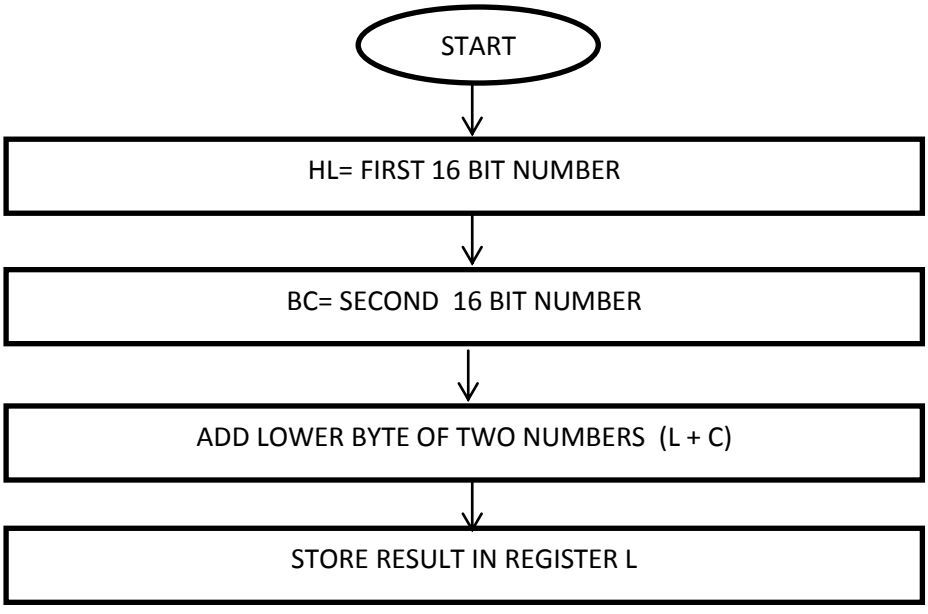
Ans:- (4 Marks – Flowchart, 4 marks – 16 bit addition operation with correct result)

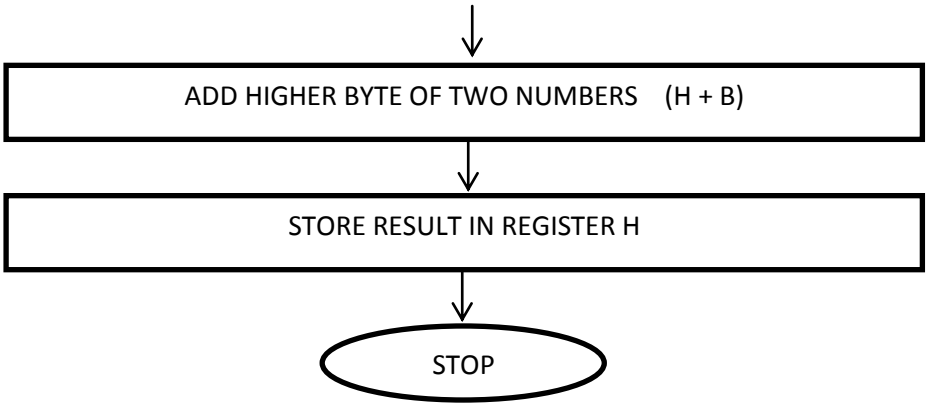
(any one flowchart should be considered or any other suitable flowchart can also be considered)




ADD TWO 16 BIT NUMBERS using DAD rp instruction (HL =HL +BC)
Store result In HL register pair
STOP

‘ OR ’


START
HL= FIRST 16 BIT NUMBER
BC= SECOND 16 BIT NUMBER
ADD LOWER BYTE OF TWO NUMBERS (L + C)
STORE RESULT IN REGISTER L



16 bit addition operation:

For example :

HL = 1234H = 0001 0010 0011 0100

\+ BC = 3251H = 0011 0010 0101 0001

HL = 4485H= 0100 0100 1000 0101

(Note: any two 16 bit numbers can be considered)

b) How SID and SOD pins can be used as a single bit o/p and i/p ports respectively

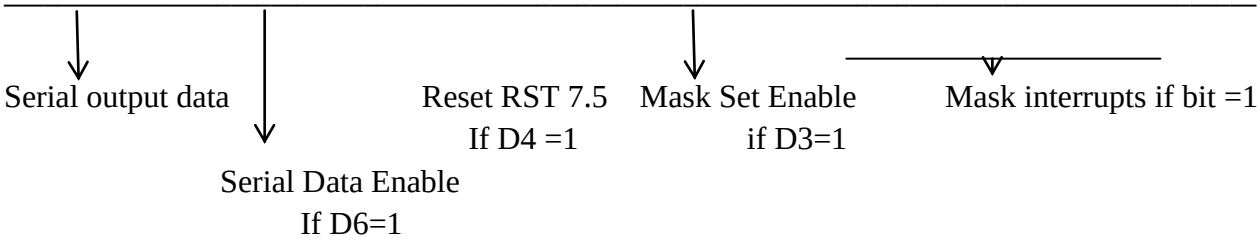
Ans:- (2 marks – SIM format, 2 marks –explanation, 2 marks – RIM format, 2 marks – explanation)

SOD : SERIAL OUTPUT DATA

Using this pin 8085 can send data serially bit by bit ,one bit at a time with the help of SIM instruction

SIM instruction format:

D7	D6	D5	D4	D3	D2	D1	D0
SOD	SDE	XX	R7.5	MSE	M7.5	M6.5	M5.5



In SIM instruction format D7 bit is used as data bit .

If SDE =1 , then A7 bit of accumulator is transmitted on SOD pin of 8085

E.g. For sending logic 1 on SOD pin , instruction are:

MVI A, C0H

SIM

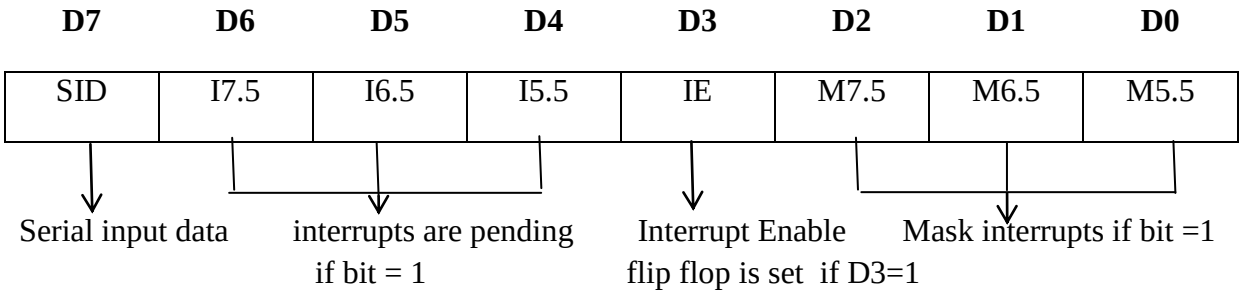
HLT

Thus SOD pin is used as 1-bit output port

SID : SERIAL INPUT DATA

Using this pin 8085 can receive data serially bit by bit ,one bit at a time with the help of RIM instruction

RIM instruction format:



When RIM instruction is executed data available on SID pin is copied in A7 bit of accumulator .

For e.g. after execution of RIM instruction if contents of accumulator are 85H (1000 0101) ,it indicates that logic 1 is read from SID pin of 8085 ,Thus SID pin is used as 1 bit input port.

c) A 4 bit DAC generates Vout of 1V for $(0010)_2$ digital i/p. Find Vout for $(1010)_2$ and $(0111)_2$

Ans:- (2 marks – Calculating V REF (VFS), 3 marks – Calculating VOUT for (1010)$_2$, 3 marks – Calculating VOUT for (0111)$_2$)

For 4 bit DAC,

$$\mathbf{V_{OUT} = V_{REF} (d1/2^1 + d2/2^2 + d3/2^3 + d4/2^4)}$$

NOW , d1 d2 d3 d4 = 0 0 1 0 , V_{OUT} = 1V

$1\ V = V_{REF}\ (0/2^1 + 0/2^2 + 1/2^3 + 0/2^4)$

$1\ V = V_{REF}\ (0 + 0 + 1/8 + 0)$

V_{REF} = 8 V

I) For $(1010)_2$

VOUT = $8\ (1/2^1 + 0/2^2 + 1/2^3 + 0/2^4)$
VOUT = 8 (1/2 + 0 + 1/8 + 0)
VOUT = 5 V

II) For $(0111)_2$

VOUT = $8\ (0/2^1 + 1/2^2 + 1/2^3 + 1/2^4)$
VOUT = 8 (0 + 1/4 + 1/8 + 1/16)
VOUT = 3.5 V