Important Instructions to examiners:

1) The answers should be examined by key words and not as word-to-word as given in the model answer scheme.
2) The model answer and the answer written by candidate may vary but the examiner may try to assess the understanding level of the candidate.
3) The language errors such as grammatical, spelling errors should not be given more Importance (Not applicable for subject English and Communication Skills).
4) While assessing figures, examiner may give credit for principal components indicated in the figure. The figures drawn by candidate and model answer may vary. The examiner may give credit for any equivalent figure drawn.
5) Credits may be given step wise for numerical problems. In some cases, the assumed constant values may vary and there may be some difference in the candidate's answers and model answer.
6) In case of some questions credit may be given by judgement on part of examiner of relevant answer based on candidate's understanding.
7) For programming language papers, credit may be given to any other program based on equivalent concept.

Q1. a) Attempt any six of the following:- **12M**

i) Specify the functions of IC 74381.

Ans:- IC 74381 is an ALU i.e. Arithmetic and Logic Unit IC. **01 M**

It performs:- **01 M**

I. Arithmetic operations

II. Logical operation

ii) State functions of following pins :-

1) ALE

2) SOD

Ans:-

ALE (Address Latch Enable):- **01 M**

This pin is used to demultiplex low order address and data bus.

SOD(Serial Output Data):- **01 M**

This pin is used to send data serially

iii) Give characteristics of memories (any four)

Ans:- **Four Characteristics :-** **(½ M each)**

i) Capacity & its organization

ii) Timing characteristics\

iii) Cost

iv) Physical dimensions

v) Power consumption

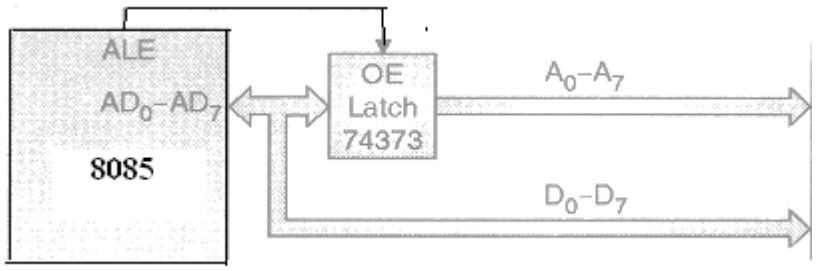
vi) Reliability

iv) Explain the demultiplexing of address and data bus by ALE signal.

Ans:- **02 M**

The bus $AD_7 – AD_0$ is connected as the input of latch. ALE signal is used as the enable pin of the latch. When ALE goes high, the latch becomes transparent and the address gets latched. When ALE goes low, the same lines are used as data bus & the output of the latch represents the low order address bus A_7 to A_0.

OR



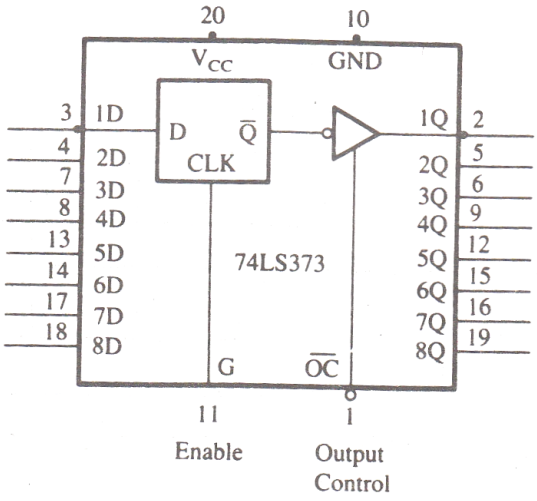
02 M

v) Explain the latches with an example IC 74373.

Ans:- **02 M**

IC 74373 is a 8 bit latch. It consists of 8 D – flip flops. When enable pin G is high and $\overline{OC}$ is low, output changes according to the input. $\overline{OC}$ enables tri state buffer.

Example-



vi) What do you mean by priority encoder? Give example.

Ans:- **01 M**

Encoder is a device which gives code corresponding to the active input. In priority encoder if two inputs active simultaneously output will be corresponding to the one which has higher priority.

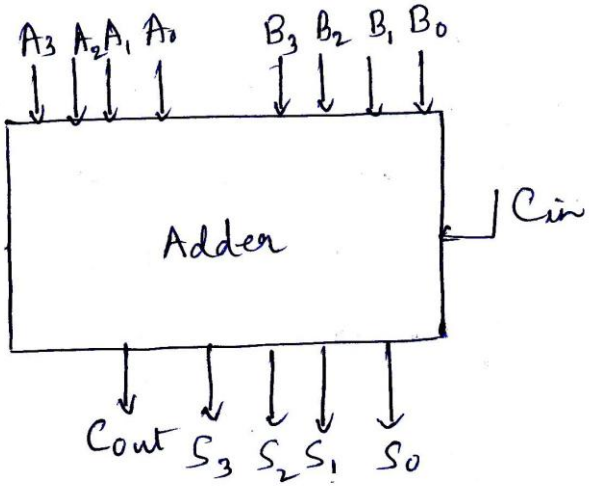
E.g. IC 74147 Decimal to BCD priority encoder **01 M**

OR

IC 7418 octal to binary priority encoder.

vii) Draw only block diagram of 4 bits parallel binary adder.

Ans:- **Block Diagram:-** **02 M**



viii) Compare RAM and Rom (any four points).

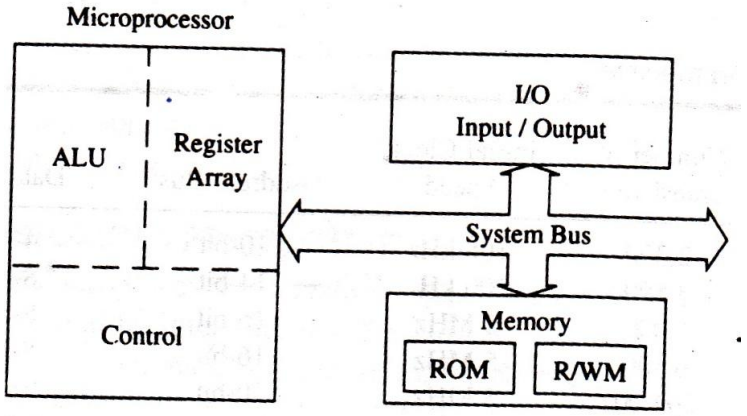
Ans:- Any four points **½ M each**

Sr. no	RAM	ROM
1.	Random Access Memory	Read Only Memory
2.	Memory is accessed randomly	Memory is accessed sequentially.
3.	Temporary memory	Permanent memory
4.	Volatile	Non Volatile
5.	Data stored can be changed.	Data stored cannot be changed
6.	Types :- SRAM, DRAM	Types :- ROM, PROM, EPROM, EEPROM

Q1. b) Attempt any two of the following :- **08 M**

i) Draw the block diagram of microprocessor based system and explain in brief.

Ans:- Block diagram :- **02 M**



Explanation:- **02 M**

Microprocessor performs computing functions and making decisions. It consists of Arithmetic Logic Unit, Control unit and Register array.

Memory stores binary information as instructions and data and provides that information to the microprocessor whenever necessary. Input/ Output devices are known as peripherals which communicate with outside world.

ii) Compare I/o mapped I/o and memory mapped I/o system.

Ans:- Any four points **01 M each**

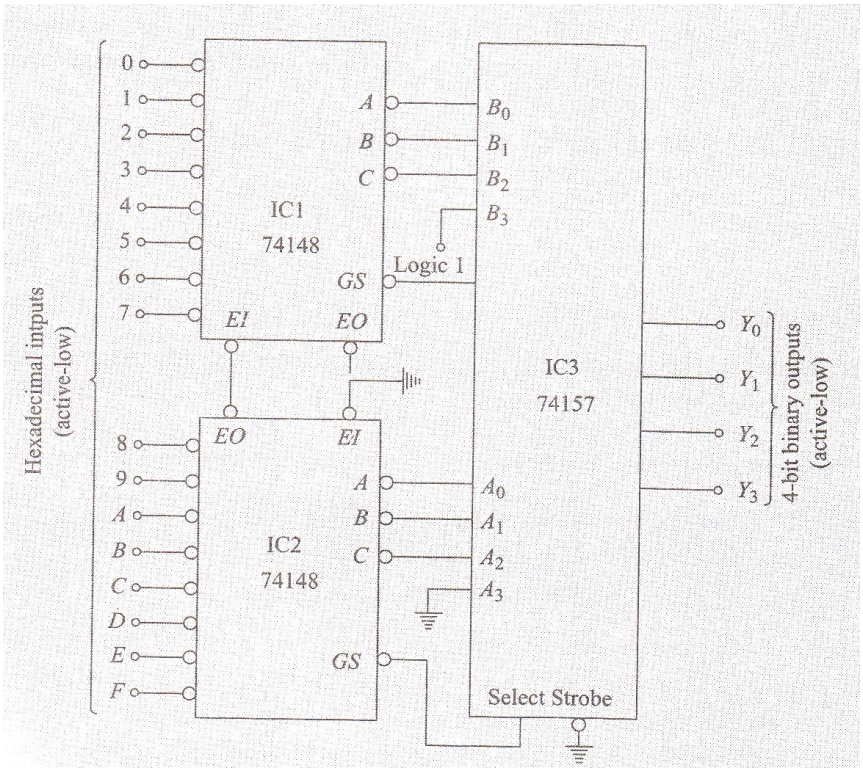
Sr. no	**I/O MAPPED I/O**	**MEMORY MAPPED I/O**
1.	Device address is 8 bits	Device address is 16 bits
2.	Control signals used are $\overline{IOR}$ and $\overline{IOW}$	Control signals used are $\overline{MEMR}$ and $\overline{MEMW}$
3.	256 input and output devices can be interfaced using this technique	Theoretically 65536 (2^{16}) devices can be interfaced using this technique
4.	IN ,addr and OUT, addr instructions are used for accessing I/O devices	All memory related instructions are used for accessing I/O devices
5.	Data transfer is possible between only Accumulator	Data transfer is possible between any register and I/O devices

	and I/O devices.	
6.	Execution speed is 10 T-states	Execution speed varies from 7 T-states to 13 T-states
7.	Arithmetic and logical operations are not possible	Arithmetic and logical operations are possible
8.	Decoding 8 bit address requires less hardware	Decoding 16 -bit address requires more hardware

Note :-. Any other valid comparison points can be considered

iii) Design a hexadecimal to binary priority encoder using 74148 encoder and multiplexer.

Ans:- **04 M**



Q2) Attempt any four of the following:- **16 M**

a) Describe the function of 'Program Counter and Instruction register' of the 8085 Microprocessor.

Ans:- Program Counter :- **02 M**

It is a 16 bit register used to hold address of next instruction to be executed. When one byte is being fetched, the program counter is incremented by one to point to the next memory location.

Instruction Register :- **02 M**

It is an 8 bit register. Any instruction brought from the memory will go to the instruction register and gets stored there temporarily.

b) Explain any four control signal in 8085.

Ans:- **01 M each**

Note :- Marks can be given for any four control signals

$\overline{RD}$:-

This is active low read control signal used to read the selected memory or I/o device.

$\overline{WR}$:-

This is active low write control signal used to write into the selected memory or I/o device.

ALE:-

This signal is used to demultiplex low order address and data bus.

IO/$\overline{M}$:-

When the signal is high it indicates I/o operation, and when the signal is low it indicates memory operation.

$\overline{MEMR}$:- **01 M**

This is active low read control signal. It indicates that the selected memory device is to be read and data are available on the data bus.

$\overline{MEWR}$:- **01 M**

This is an active low write control signal. This signal indicates that the data on the data bus are to be written into a selected memory.

$\overline{IOR}$:- **01 M**

This is active low read control signal. This indicates that the selected I/o device is to be read and the data is available on the data bus.

$\overline{IOW}$:- **01 M**

This is active low write control signal. This signal indicates that the data on the data bus is to be written in to a selected I/o location.

c) Compare Static and Dynamic RAM for four points.

Ans:- Any four points **01 M each**

Parameter	**Static RAM**	**Dynamic RAM**
Circuit configuration	Each SRAM cell is a flip flop	Each cell is one MOSFET & a capacitor
Bits stored	In the form of voltage	In the form of charges
No. of components per cell	More	Less
Storage capacity	Less than DRAM	More than SRAM
Refreshing	Not required	Required
The content of the memory location	Remains constant	Gets lost due to discharging of capacitor.
Cost	More	Less
Access time	More	Less
Power consumption	Less	More

d) Explain the Evolution of microprocessor.

Ans:- **04 M**

The first microprocessor was introduced by Intel in 1971. This was Intel 4004, a four bit processor with clock frequency of 750 KHz. In 1973 Intel introduced the first 8- bit microprocessor 8008. Later in 1974 this was followed by better version Intel 8080. It had 16 bit address line and 16 bit stack pointer with clock frequency of 2MHz. Within few years Motorola 6800, Z – 80 and Intel 8085 were developed. It integrated clock, the system control and interrupt prioritization within the microprocessor IC there by reducing the number of IC. 1978 onwards 16 bit processors such as 8086, 8088, 80186, 80286 were developed with a memory capacity of 1MB to 16MB and clock frequency 12.5 MHz . In 1989, Intel 80486 was developed which is a 32 bit processor with 4Gb memory and 20Mhz clock frequency.I860 is a 64 bit processor with 4Gb memory and 40MHz clock frequency.

e) Explain the subroutine with one example.

Ans:- Subroutine:- **02 M**

A subroutine is a group of instructions written separately from the main program to perform a function that occurs repeatedly in the main program.

Example :- **02 M**

For example, if a time delay is required between three successive events, three delays can be written in the main program. To avoid repetition of the same delays instructions, the subroutine techniques is used. Delay instructions are written once, separately from the main program and are called by the main program when needed.

f) Write an assembly language program to transmit 8 – bit serial data using SOD line.

Ans:-

```
        MVI  B, 8 bit data   ; Data to be transmitted
        MVI  C, 08           ; Initialise counter
BACK:   MOV  A, B            ; Take Number in accumulator
        RRC                  ; Rotate right A by one bit
        MOV  B, A            ; Save content of register B
        JNC  skip            ; If no carry skip
        MVI  A, C0H
        SIM                  ; if carry send 1 on SOD
        JMP  NEXT
skip:   MVI  A, 40H
        SIM  *
NEXT:   DCR  C               ; Decrement counter by one
        JNZ  BACK            ; Repeat 8 times
        HLT                  ; Stop program execution
* A delay program may be called.
```

Note: any other correct logic can be considered

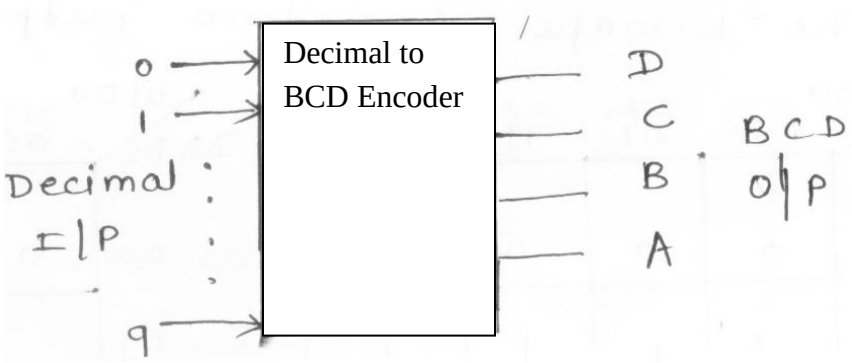
Q3) Attempt any FOUR of the following: **16 M**

a) Draw decimal to BCD encoder? Explain it.

Ans:-

Note:- Diagram drawn for IC 74147 should also be given equal weightage

Block diagram :- **01 M**



Truth table :- **02 M**

I/P Decimal	O/P D C B A
0	0 0 0 0
1	0 0 0 1
2	0 0 1 0
3	0 0 1 1
4	0 1 0 0
5	0 1 0 1
6	0 1 1 0
7	0 1 1 1
8	1 0 0 0
9	1 0 0 1

Explanation :- **01 M**

1) The decimal to BCD encoder has 10 inputs and 4 output it is called a 10:4 encoder.

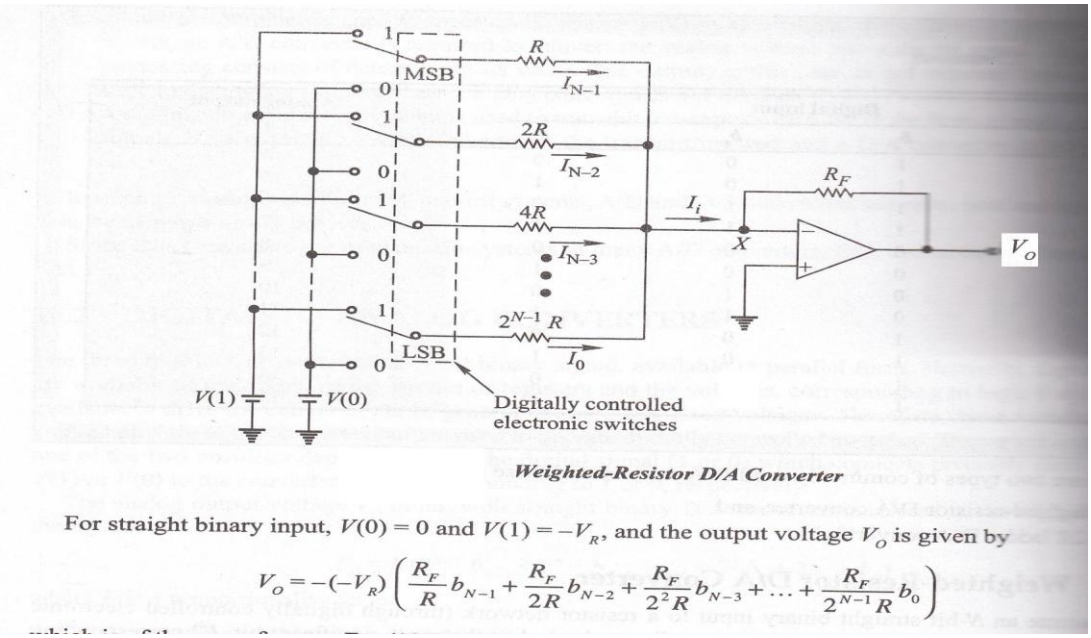
2) The D_0 input has lowest priority.

3) The D_9 input has highest priority.

4) The decimal to BCD encoder is available in IC from i.e. IC 74147

b) Explain weighted resistor type D/A converters with neat diagram .

Ans:- **Diagram :-** **02 M**



Weighted-Resistor D/A Converter

For straight binary input, $V(0) = 0$ and $V(1) = -V_R$, and the output voltage V_O is given by

$$V_O = -(-V_R)\left(\frac{R_F}{R}b_{N-1} + \frac{R_F}{2R}b_{N-2} + \frac{R_F}{2^2R}b_{N-3} + \ldots + \frac{R_F}{2^{N-1}R}b_0\right)$$

Explanation :- **02 M**

The basic building blocks of DAC are:-

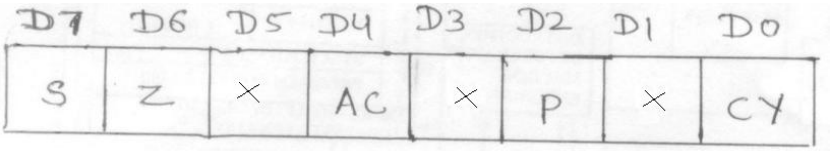
1) A resistive network
2) Digitally controlled switches
3) A voltage reference
4) A current to voltage converter

A digital input code is applied to the resistive network via digitally controlled switches.

The digitally controlled switches are turned ON/OFF by the digital input bits. The output of resistive network is in the form of current. It can be converted into proportional voltage with the help of I (current) to V (Voltage) converter. Thus we obtain output voltage proportional; to digital input.

c) Draw format of flag register of 8085 microprocessor and explain function of each flag(3m for

Ans:- format of flag register and 1m each for explaining 5 flags



1) Zero Flag:-

The zero flag is set if the result of operation in ALU is zero and flag is reset if the result is non – zero. The flag is also modified by result in other registers.

2) Sign Flag:-

If D_7 bit of the result in accumulator is 1 sign flag is set to 1 . If D_7 bit of the result in accumulator is 0 sign flag is reset to 0 .

3) Auxillary Carry:-

In an arithmetic operation when carry is generated from D3 bit to D_4 bit the AC flag is set. The flag is used for BCD operations and it is not available for the programmer.

4) Carry:-

This flag is set if there is a carry generated out of D_7 bit after an arithmetic or logical operation, otherwise it is reset. It also serves as borrow flag for subtraction.

5) Parity Flag :-

It indicates the number of ones in the result of arithmetic and logical operation. If the result in accumulator has even number of ones the parity flag is set. If the result in accumulator has odd number of ones the parity flag is reset.

d) Explain the address modes of 8085.

Ans:- **(any four addressing modes ,1 mark each.)**

1) Immediate Addressing mode:-

In this mode of addressing the 8 bit or 16 bit operand (data) is a part of instruction .

MVI A,20H

2) Register Addressing mode:-

In this mode of addressing the operand (data) is in one of the general purpose register or accumulator.

MOV B, A

3) Direct Addressing mode:-

In this mode of addressing the address of operand (data) is a part of instruction.

LDA 6020H

4) Indirect Addressing mode:-

In this mode of addressing the address of the operand (data) is specified by a register pair.

MOV B, M .

5) Implicit / Implied Addressing mode:-

In this mode of addressing the operand (data) is in accumulator.

RAR

Note: any valid example can be considered.

e) Write an ALP to arrange 10 given Nos. in descending order.

Ans:- **(4m for correct program any other correct logic can be considered)**

Program :

```
      MVI C, 0AH    ;  Initialize comparison or pass counter
UP1:  LXI H, D100H  ;  Initialize memory pointer to read number from
                       array
      MVI B, 09H    ;  initialize byte counter with length – 1 = 9
UP:   MOV A, M      ;  load number from the memory
      INX H         ;  increment memory pointer by 1 to read next
                       number
      CMP M         ;  Compare number with next number
      JNC DN        ;  If number > next number then go to DN
      MOV D, M      ;  exchange number and next number
                       D←[HL]
      MOV M, A      ;  [HL] ← A
      DCX H         ;  HL ← HL – 1
      MOV M, D      ;  [HL]← D
      INX H         ;  HL ← HL + 1
DN:   DCR B         ;  Decrement byte counter by 1
      JNZ UP        ;  If not zero, then go to UP
      DCR C         ;  Decrement comparison counter by 1
      JNZ UP1       ;  If not zero, then go to UP1
      HLT           ;  Stop
```

Q4) Attempt any FOUR of the following:- **16 M**

a) Write the specifications of ADC.

Ans:- any four specifications **(definition : 1mark each)**

Specifications of ADC are :

1. Resolution
2. Conversion time
3. Quantization error
4. Accuracy

1. Resolution : it is defined as ratio of change in value of input analog voltage required to change the digital output by 1 LSB, it is given as

$$\text{RESOLUTION} = V_{FS} / (2^n - 1)$$

2. Conversion time : total time required to convert the analog input signal into a corresponding digital output. It should be ideally zero.

3. **Quantization error :** error due to quantization process is called quantization error. It is the difference between the actual analog value and quantized digital value.

4. **Accuracy :** It is a measure of the difference between the actual output and the expected output

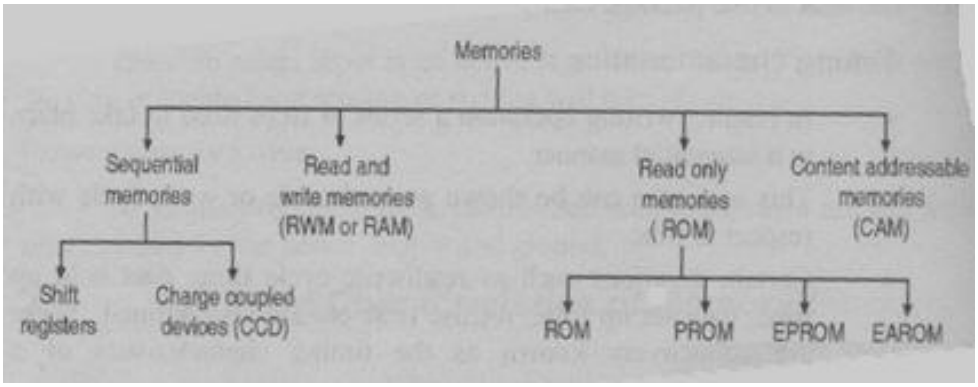
5. **Range of input voltage:** Range of input voltage which can be converted into digital output

b) Give the classification of memories.

Ans:- Classification of memories : (correct classification : 4 marks)

Memories can be classified based on following parameters:

1. Based on principle of operation : **01 M**



2. Based on Physical characteristics : **01 M**

a) Erasable or non- erasable

b) Volatile or non - volatile

3. Based on Mode of access : **01 M**

a) Sequential access

b) Random access

4. Based on fabrication technology : **01 M**

a) Bipolar technology

b) MOS technology

c) State the function of following pins of 8085 microprocessor.

1. X_1 and X_2
2. RESET OUT
3. S_0 and S_1
4. HLDA

Ans:- Functions of following pins of 8085 : 01 M each

i) **X1 and X2** : These are clock inputs of 8085. A crystal (or RC , LC network) is connected at these two pins . The frequency is internally divided by two.

ii) **RESET OUT :** It is active high output signal which indicates that microprocessor is being reset . It is used to reset peripheral devices connected to 8085 microprocessor

iii) **S_0 and S_1** : These are status signals / pin of 8085. It indicates the type of operation performed by 8085.

S1	S0	OPERATION
0	0	HALT
0	1	WRITE
1	0	READ
1	1	OPCODE FETCH

iv) **HLDA :** Hold acknowledge : This is an active high output signal use to acknowledge HOLD request.

d) List various features of 8085 Microprocessor.

Ans:-

Features of 8085 : (any four features) **01 M each**

i) It is an 8 bit microprocessor

ii) It operates on +5V DC SUPPLY

iii) It has on chip clock generator that divides oscillator frequency by 2

iv) It can operate with 3 MHZ clock frequency

v) It has 16 bit unidirectional address bus

vi) It has 8 bit bidirectional data bus (multiplexed address /data bus AD0 –AD7)

vii) It is 40 pin DIP

viii) it provides 5 hardware interrupts TRAP , RST 7.5 ,RST 6.5 , RST 5.5 ,& INTR and eight software interrupts RST 0 –RST 7.

Note :- Any other valid features can also be considered

e) How are the signals like $\overline{MEMR}$, $\overline{MEMW}$, $\overline{IOR}$ and $\overline{IOW}$ generated in 8085 based system

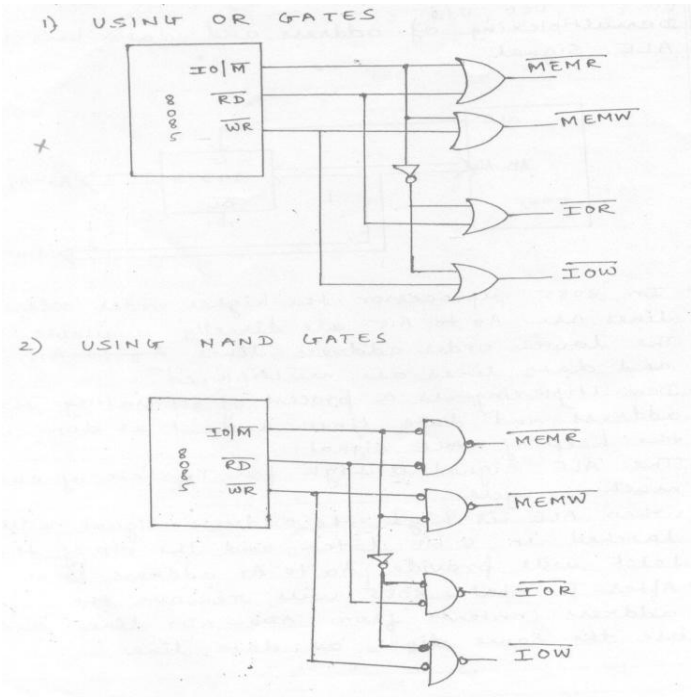
Ans:-

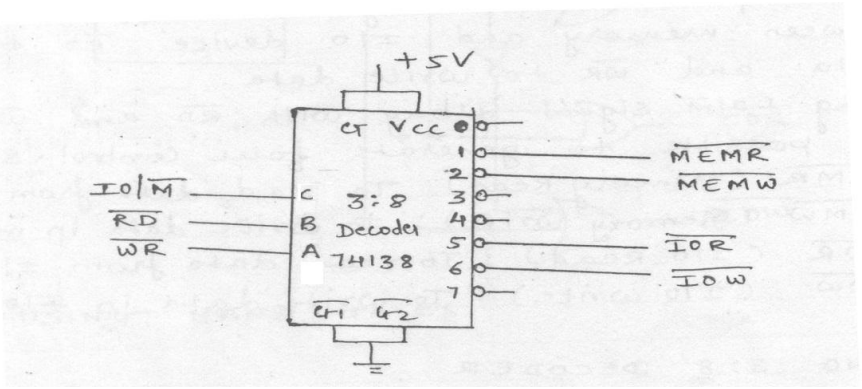
Generation of $\overline{MEMR}$, $\overline{MEMW}$, $\overline{IOR}$ and $\overline{IOW}$ Signals of 8085 (any one diagram :4 marks)

1) Using OR gates

2) Using NAND gates

3) Using 3:8 decoder



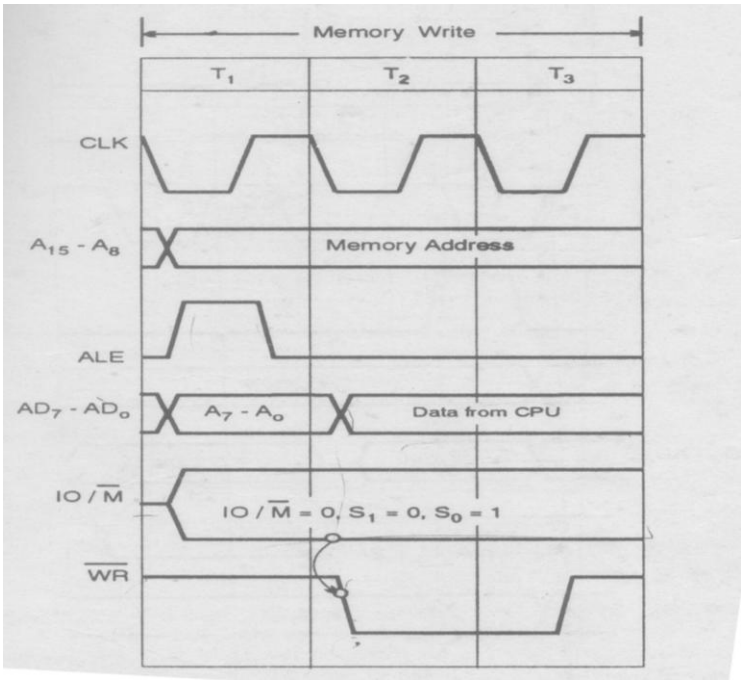


Using 3 : 8 decoder

f) Explain the memory write cycle in case of 8085 µP.

Ans:-

Memory write machine cycle of 8085: Diagram **02 M**



Explaination : **02 M**

In Memory write machine cycle microprocessor sends data from accumulator or any other register to the memory . It requires 3 –T states

T1-State : Microprocessor places memory address on the address lines & activates ALE signal to demultiplex AD0-AD7 lines . It aslo generates status signals IO/M =0 ,S1=0 ,S0=1

T2 –State: In T2 state data to be sent out to the memory is placed on the AD0-AD7 lines

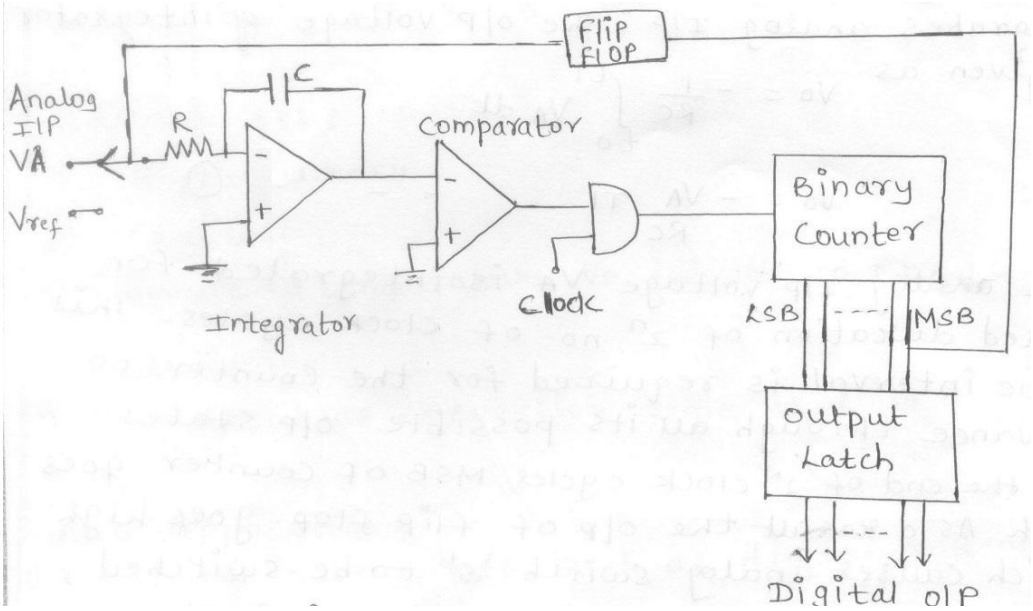
(dada dus)& WR signal goes low .

T3 state : In T3 state WR goes high terminating write operation

Q.5 Attempt any TWO of the following :- **16 M**

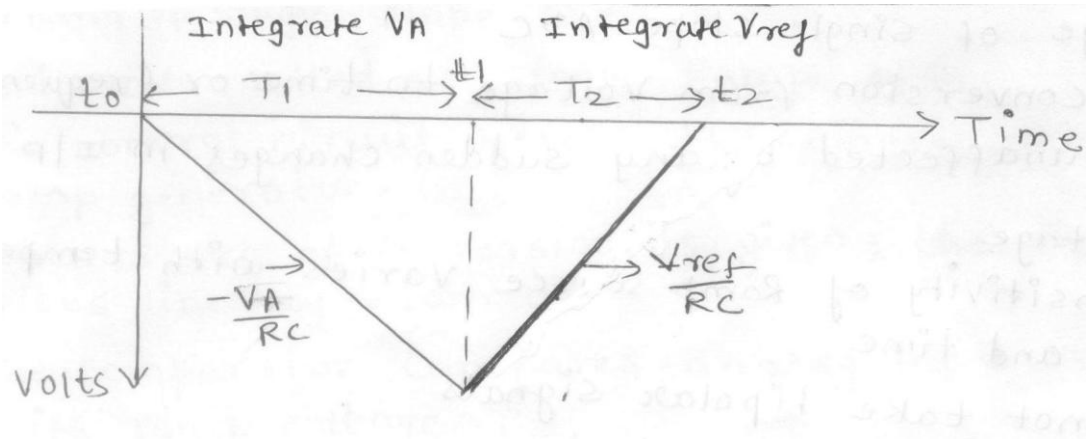
a) Explain working principle of dual slope A/D converter.

Ans:- **(2m for block diagram 2m for working principle 2m for waveform 2m for explanation)**



Explanation :-

The input voltage is integrated for fixed input sample time. The integrated value is then discharged at a fixed rate and time to do this is measured by the counter. The circuit is called as dual slope ADC because analog voltage V_A and reference voltage V_{ref} are converted to ramp signal of different slopes by the integrator.



1) The integrator output during time t0 to t1 is given by

$$V_0 = \frac{V_A}{RC}(T1)$$

2) The integrator output during time t1 to t2 is given by

$$V_0 = \frac{V_{ref}}{RC}(T2)$$

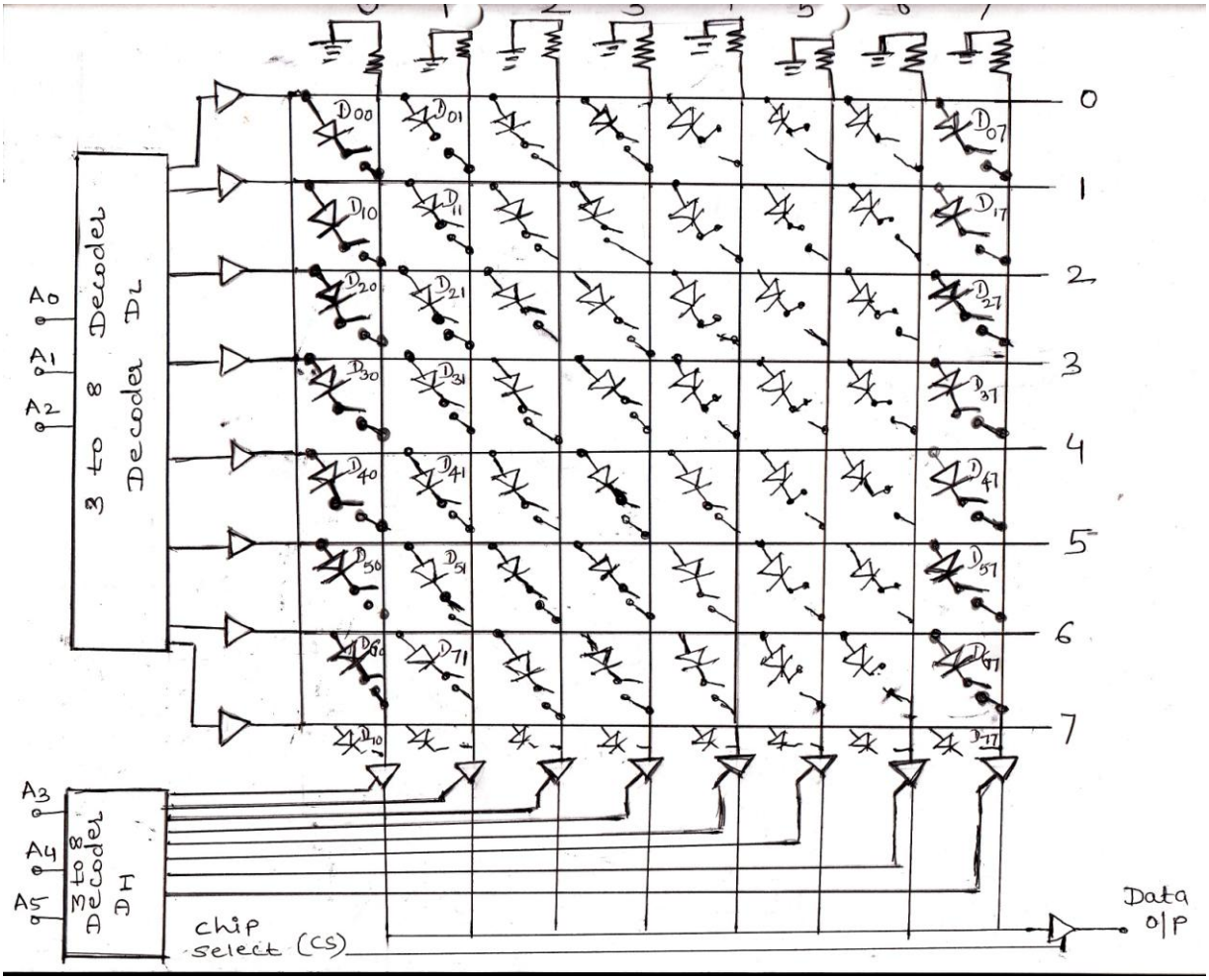
Equating equation 1 and 2

$$V_A = -V_{ref}\left(\frac{T2}{T1}\right)$$

From above expression we can say that unknown analog voltage is directly proportional to the time taken by the integrator to reduce to zero i.e. time T2. At time t2 conter o/p shows desired digital o/p code.

b) Draw and explain diode matrix ROM array

Ans:- Diagram :- **06 M**



Explanation :- **02 M**

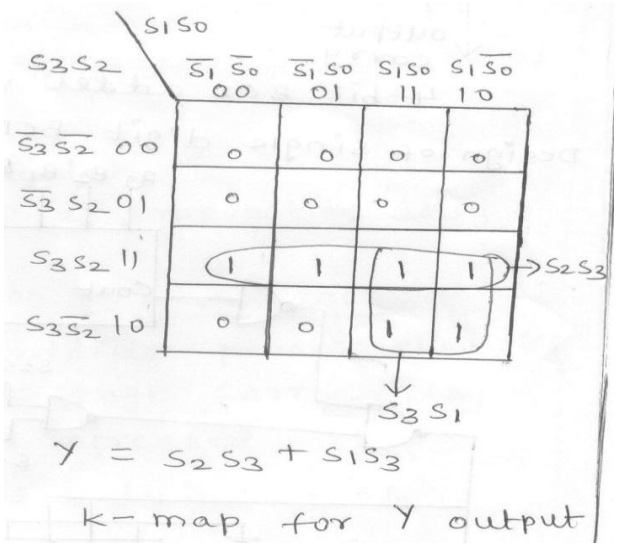
1) Read only memory is an array of selectively open and closed unidirectional contacts.
2) A 64 bit ROM array is shown above. To select any one of the bits a 6 bit address (A_5, A_4, A_3, A_2, A_1 , A_0) is required.
3) The lower order 3 bits (A_2, A_1 , A_0) are decoded by the decoder D_L which selects one of the eight rows.
4) The higher order three bits (A_5, A_4, A_3) are decoded by the decoder D_H which activates one of the eight columns.
5) The diode matrix is formed by connecting one diode along with switch between each row and columns.

c) Explain single digit BCD adder.

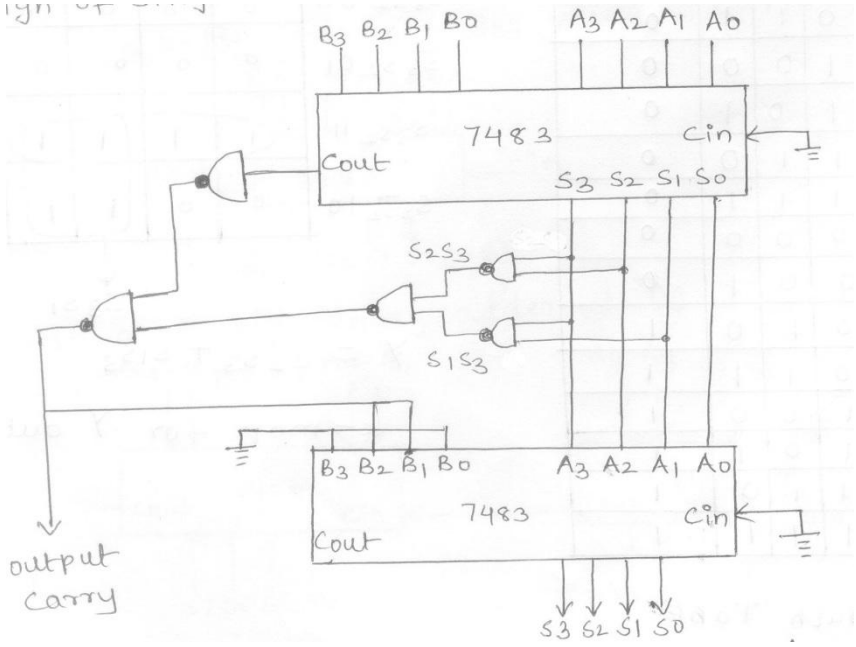
Ans:- **Truth table :-** **02 M**

Input				output
S_3	S_2	S_1	S_0	Y
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

K – Map :- **02 M**



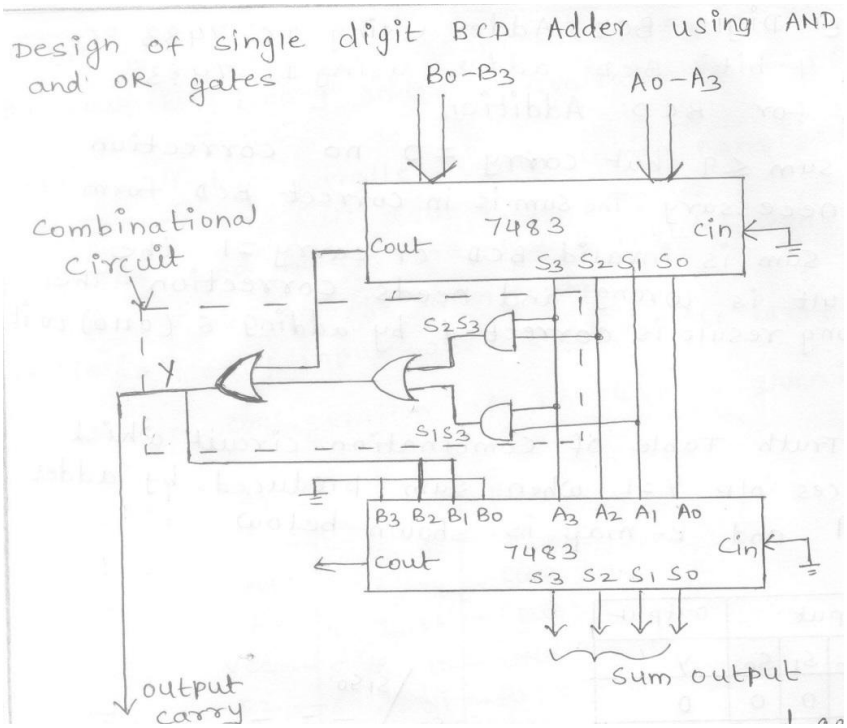
Design of single digit BCD adder using only NAND gates



4 – bit BCD adder using 7483 and gates

OR

Design of single digit BCD adder using AND and OR gates



4 – bit BCD adder using 7483 and gates

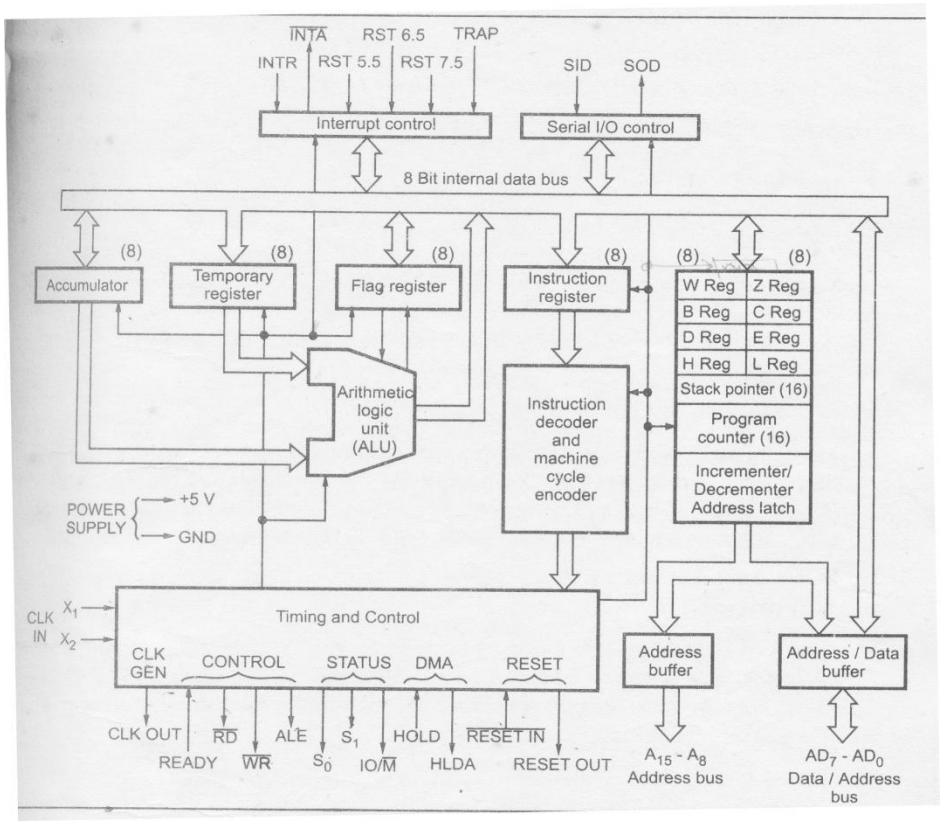
Q.6. Attempt any TWO of the following

a) Draw block diagram of 8085 microprocessor and explain function of following:-

1) ALU
2) Temporary register W and Z
3) Timing and control unit

Ans:-

Block diagram of 8085 microprocessor:- **05 M**



Explaination : **01 M each**

i) ALU : Arithmatic Logic unit : It performs arithmetic & logical operations like addition , subtraction, AND , OR , complement , rotate etc. on 8 bit data.

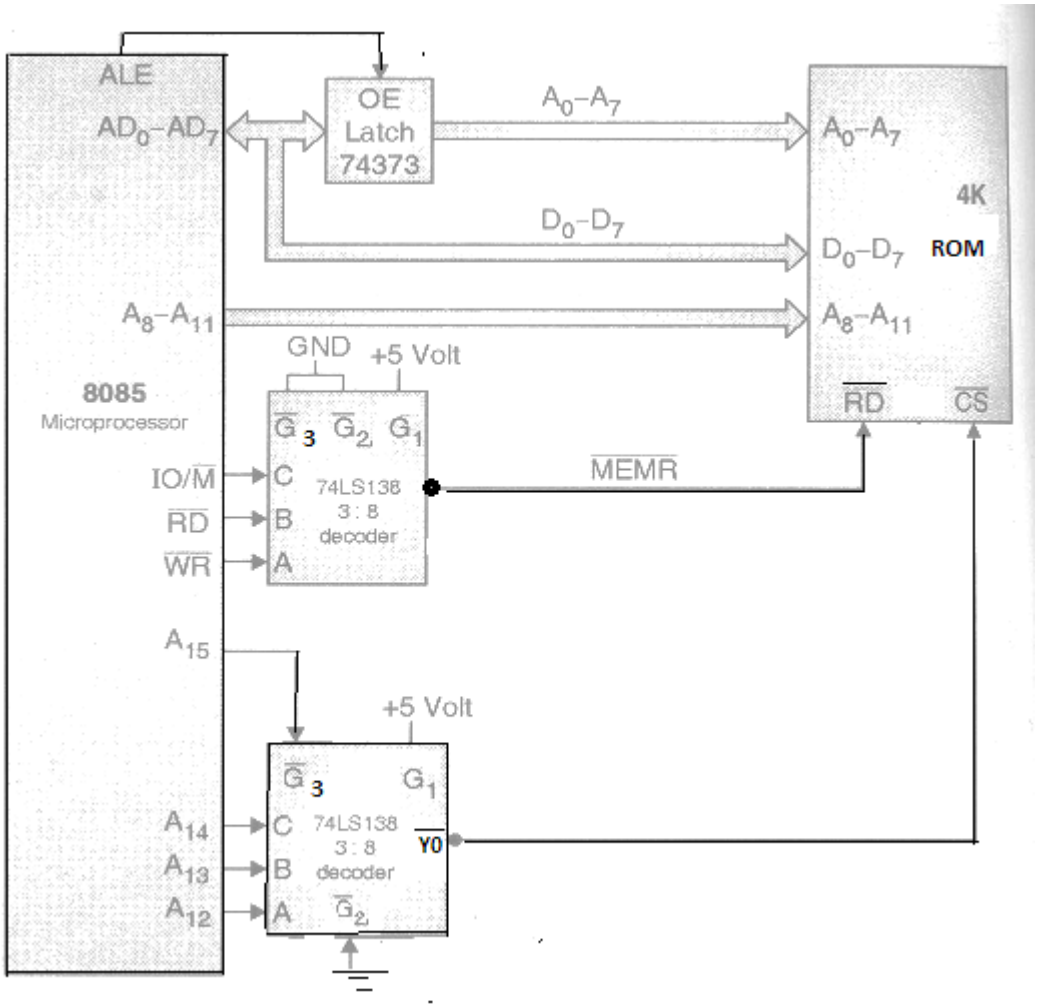
ii) Temporary registers W and Z : used internally by 8085 to hold 8 bit data temporarily during execution of some instructions

iii) Timing and Control unit : Synchronizes all microprocesor operations with clock and generatres control signals necessary for instruction execution and communication between peripheral devices & microprocessor.

b) Interface the 4K * 8 ROM to 8085 with starting address 0000H. Draw interface diagram.

Ans:-

Diagram:- **04 M**



Note :- Any other correct decoding logic can be used for generating $\overline{CS}$ signal such that starting address is 0000H

Address line calculation:- **02 M**

4K X 8 ROM : $2^{12} = 4$ K

Therefore 12 address lines are required ($A_0 - A_{11}$)

Address map:

Memory map:- **02 M**

Address		A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
START	0000H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
END	0FFFH	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1

c) Give any two advantage and disadvantage of:

i) Successive approximation method

ii) Dual slope ADC

Ans:-

i) Advantages of Succssive approximation method ADC: **(any two)** **02 M**

1.Conversion time is equal to 'n'clock cycle period for an n bit ADC .

2. Conversion time is constant & independent of amplitude of analog signal V_A

3. Fast speed as compared to dual slope

Disadvantages of Succssive approximation method ADC: **(any two)** **02 M**

1. Quantization errors are more

2. Moderately high cost

3. Circuit is complex

ii) Advantages of Dual slope ADC : **(any two)** **02 M**

1. Low cost
2. Accuracy is of order 0.05% ,adequate for most applications
3. Capable of rejecting noise & hum
4. Auto-zeroing possible

Disadvantages of Dual slope ADC: **(any two)** **02 M**

1. Long conversion time
2. Long input hold time
3. Slow speed

Note :- Any other valid points can be considered