Important Instructions to examiners:

1) The answers should be examined by key words and not as word-to-word as given in the model answer scheme.
2) The model answer and the answer written by candidate may vary but the examiner should assess the understanding level of the candidate.
3) The language errors such as grammatical, spelling errors should not be given importance (Not applicable for subject English and Communication Skills).
4) While assessing figures, examiner may give credit for principal components indicated in the figure. The figures drawn by candidate and model answer may vary. The examiner should give credit for any equivalent figure/figures drawn.
5) Credits to be given step wise for numerical problems. In some cases, the assumed constant values may vary and there may be some difference in the candidate's answers and model answer (as long as the assumptions are not incorrect).
6) In case of some questions credit may be given by judgment on part of examiner of relevant answer based on candidate's understanding.
7) For programming language papers, credit may be given to any other program based on equivalent concept.

**1 A) Attempt any six:** **12**

1 A) a) Give two examples of trivalent and pentavalent impurities. 2

**Ans:**

**Trivalent Impurities: (any two)**

1) Gallium (Ga)
2) Indium (In)
3) Aluminium (Al)
4) Boron (B)

½ mark each

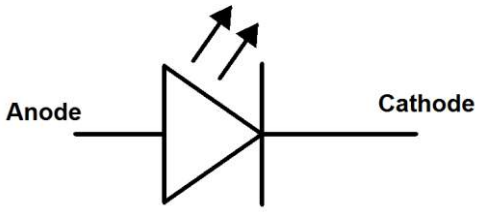
**Pentavalent Impurities: (any two)**

1) Phosphorus (P)
2) Antimony (Sb)
3) Arsenic (As)
4) Bismuth (Bi)

1 A) b) Draw the symbol of LED and photodiode. 2

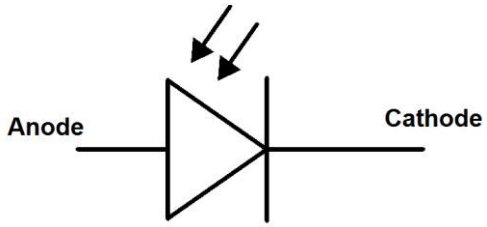
**Ans:**

**1) LED:**




1 mark

**2) Photodiode:**




1 mark

1 A) c) Define α and β of the transistor. 2

**Ans:**

**1) α :**

It is defined as the ratio of collector current ($I_C$) to emitter current ($I_E$). 1 mark

$$\alpha = \frac{I_C}{I_E}$$

**2) β :**

It is defined as the ratio of collector current ($I_C$) to base current ($I_B$). 1 mark

$$\beta = \frac{I_C}{I_B}$$

1 A) d) State the need of biasing of BJT. 2

**Ans:**

**Need of Biasing of BJT:**

The purpose of dc biasing of BJT is to obtain a certain dc collector current at a certain dc collector voltage i.e. $I_C$ and $V_{CE}$ (Q-point). 2 marks

The selected Q point is stabilized against variation in temperature.

1 A) e) List two types of oscillator, which generates frequency in RF range. 2

**Ans:**

**Types of Oscillators generating frequencies in RF range:**

i) Hartley Oscillator
ii) Colpitt's Oscillator
iii) Clapp Oscillator

1 mark each of any two

1 A) f) State two advantages of digital circuits. 2

**Ans:**

**Advantages of Digital Circuits:**

i) Digital circuits are easier to design.
ii) Information storage is easy.
iii) Accuracy and precision are greater.
iv) Less affected by noise.
v) Reliability is more.

1 mark each of any two

1 A) g) Write down output voltage for IC's 7818 and IC's 7924. 2

**Ans:**

i) For IC 7818, output voltage is +18 volt.
ii) For IC 7924, output voltage is -24 volt.

1 mark each

1 A) h) State any two applications of zener diode. 2

**Ans:**

**Applications of Zener Diode:**

i) As a voltage regulator.
ii) As a fixed reference voltage provider in transistor biasing circuits.
iii) As peak clippers or limiters in wave shaping circuits.

1 mark each of any two

**1 B) Attempt any two: 8**

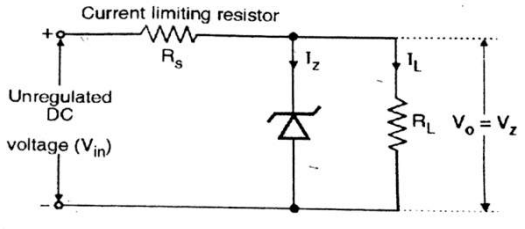
1 B) a) Draw circuit diagram and describe the working of Zener diode as voltage regulator. 4

**Ans:**

**Zener Diode as Voltage Regulator:**

A voltage regulator circuit should keep the load voltage constant in spite of changes in its input voltage or load current and temperature. The series resistance $R_s$ is connected to limit the total current drawn from the unregulated dc supply. The zener diode regulator, as shown in fig.(a), is a shunt type voltage regulator because

2 marks for diagrams

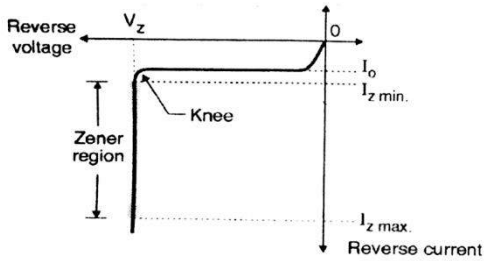



(a) Regulator circuit using Zener Diode

the control element i.e. zener diode is connected in parallel with the load resistance.

**Working of Zener Voltage Regulator:**

The input voltage $V_{in}$ is an unregulated dc voltage which is obtained from a rectifier filter combination. $R_s$ is the current limiting resistor and $R_L$ is the load resistor. The input voltage $V_{in}$ should always be higher than the breakdown voltage $V_Z$. The zener diode is reverse biased and operates in the zener region of the reverse characteristics, as shown in fig.(b)



(b) Reverse characteristics of Zener Diode

2 marks for explanation

If $V_{in}$ is higher than $V_Z$ and if the Zener current $I_Z$ is between $I_{Zmin}$ and $I_{Zmax}$ then the voltage across the Zener will remain constant equal to $V_Z$ irrespective of any changes in $V_{in}$ and $I_L$. As the output voltage is constant and equal to $V_Z$, we get regulated output voltage.

The Zener current $I_Z$ should not be higher than $I_{Zmax}$, otherwise excessive power dissipation will damage the Zener diode.

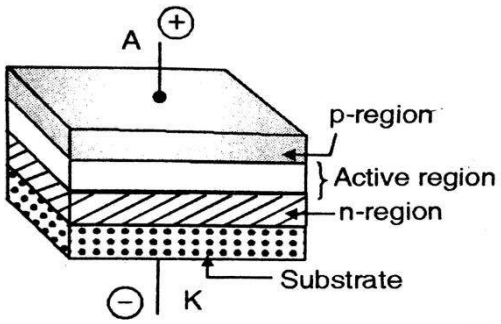
The Zener current $I_Z$ should not be less than $I_{Zmin}$ because the Zener diode then cannot operate in the zener region and cannot maintain constant voltage across it. The regulator keeps the load voltage constant in spite of changes in input voltage and load current.

1 B) b) Explain construction and working principle of LED. 4

**Ans:**

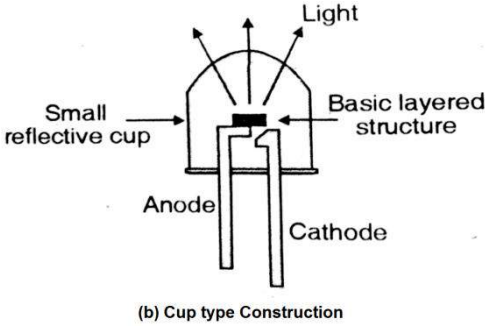
**Construction of LED:**

The basic structure of LED is shown in fig.(a). The active region exists between the p and n regions. The light emerges from the active side in all the directions when electron hole-pairs recombine. The disadvantage of this structure is that the LED emits light in all the directions. This problem is solved by placing the basic structure inside a small reflective cup so as to focus the light in the desired direction. Such a structure is called as a cup type construction and is shown in fig.(b).



(a) Basic Structure

2 marks for diagram



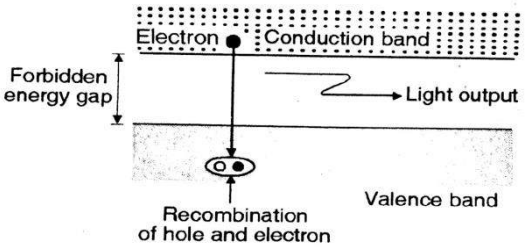
(b) Cup type Construction

2 marks for explanation

**Working Principle of LED:**

When the LED is forward biased, the electrons in the n-region will cross the junction and recombine with the holes in the p-type material. These free electrons reside in the conduction band and hence at a higher energy level than the holes in the valance band. When the recombination takes place, these electrons return back to the valance band which is at lower

energy level than the conduction band. While returning back, the recombining electrons give away the excess energy in the form of light. This process is called as "electroluminescence", shown in fig.(c). In this way an LED emits light. This is the principle of operation of LED.



(c) Working Principle of LED

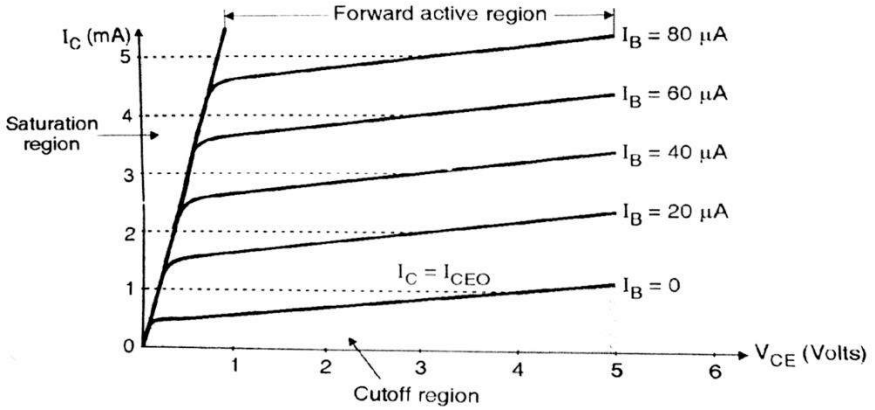
1 B) c) Draw output characteristic of CE configuration and show various region. 4

**Ans:**

**Output characteristic of CE configuration:**

2 marks for diagram

2 marks for showing regions



**Output characteristics of a n-p-n transistor in CE configuration**

**2 Attempt any Four:** **16**

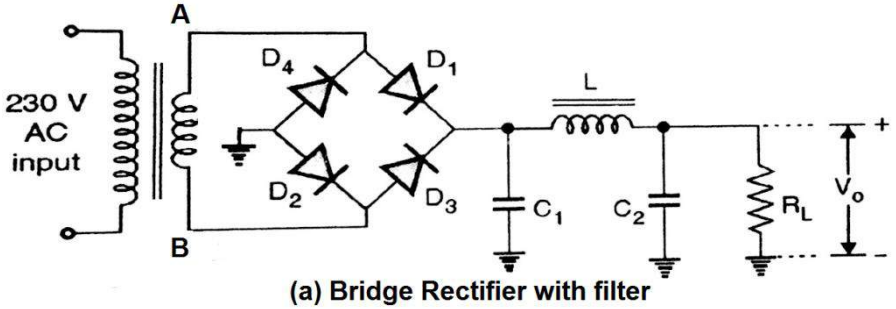
2 a) Draw the circuit diagram of bridge rectifier with π filter. Explain operation with I/P and O/P waveform. 4

**Ans:**

**Bridge rectifier with π filter:**

The circuit arrangement of bridge type rectifier with π type filter is shown in fig.(a). The π-filter is a combination of shunt capacitor filter and series L-filter. Due to the use of three filtering elements, the ripple factor of the filter is very low.

1 mark for circuit diagram

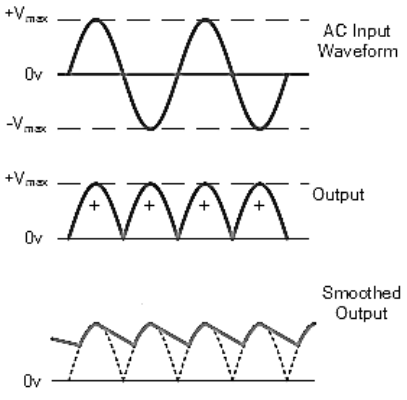


(a) Bridge Rectifier with filter

**Operation:**

During positive half-cycle of input, the secondary voltage $V_{AB}$ is positive, which

makes diodes $D_1$ and $D_2$ forward biased and $D_3$ and $D_4$ reverse biased. The load current flows from terminal A through $D_1$, L, $R_L$, $D_2$ to terminal B. The load voltage and load current are positive.




2 marks for explanation

1 mark for waveforms

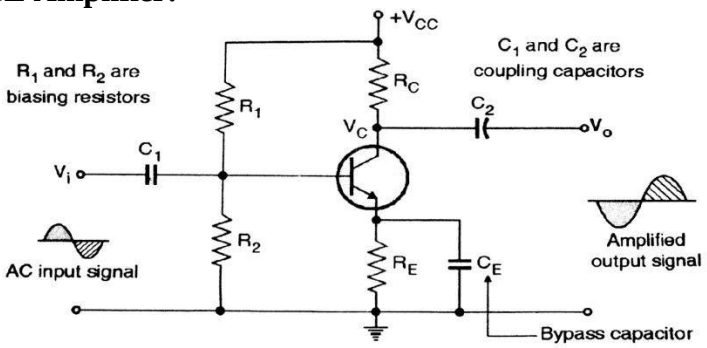
During negative half-cycle of input, the secondary voltage $V_{AB}$ becomes negative, i.e. $V_{BA}$ is positive, which makes diodes $D_3$ and $D_4$ forward biased and $D_1$ and $D_2$ reverse biased. The load current flows from terminal B through $D_3$, L, $R_L$, $D_4$ to terminal A. The load voltage and load current are once again positive.

The output of bridge rectifier is full wave rectified pulsating DC. The ripples in the current are reduced by filter inductor and the ripples in voltage are reduced by filter capacitors. Thus the pulsating DC is smoothened by filter and smooth DC voltage appears across the load. The input and output waveforms are shown in the figure.

2 b) Explain single stage CE amplifier with the help of circuit diagram. 4

**Ans:**

**Single-stage CE Amplifier:**




**Single stage RC coupled CE amplifier**

2 marks for circuit diagram

The capacitors $C_1$ and $C_2$ are called as the coupling capacitors. As the load resistor $R_L$ (not shown in the diagram) is coupled to the amplifier through the coupling capacitor, this amplifier is called as RC coupled amplifier. The transistor is connected in the common emitter (CE) configuration. Therefore, this amplifier is called CE amplifier.

2 marks for explanation

2 c) Draw diagram of class A push-pull amplifier and explain its operation. 4

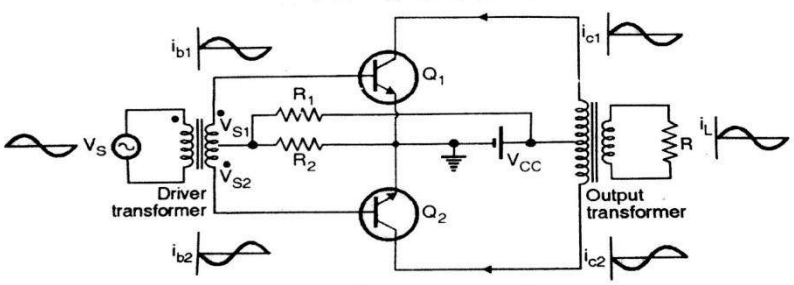
**Ans:**

**Class A Push-pull Amplifier:**

The circuit diagram of class A push-pull amplifier is as shown in the fig.(a).

**Operation:**

The resistors $R_1$ and $R_2$ along with $V_{cc}$ provide the dc biasing so as to keep the operating point (Q-point) at the centre of the dc load line, in order to achieve the class A operation. The driver transformer provides the phase splitting function and produces two voltages $V_{a1}$ and $V_{a2}$ which are equal in magnitude but 180° out of phase. The $V_{cc}$ is applied to the collectors of transistors $Q_1$ and $Q_2$ through the centre-tapped output transformer.




(a) Class A Pushpull Amplifier

1 mark for diagram

3 marks for explanation

**Operation Under dc conditions:**

The transistors $Q_1$ and $Q_2$ have identical characteristics. Therefore their dc collector currents $i_{c1}$ and $i_{c2}$ are equal. These currents will flow in opposite directions through the two halves of the primary windings of the output transformer. Therefore, there is cancellation of flux produced due to dc current and saturation of the transformer core is avoided. For complete cancellation of flux, it is essential that the two transistors are perfectly matched.

**Operation Under ac conditions:**

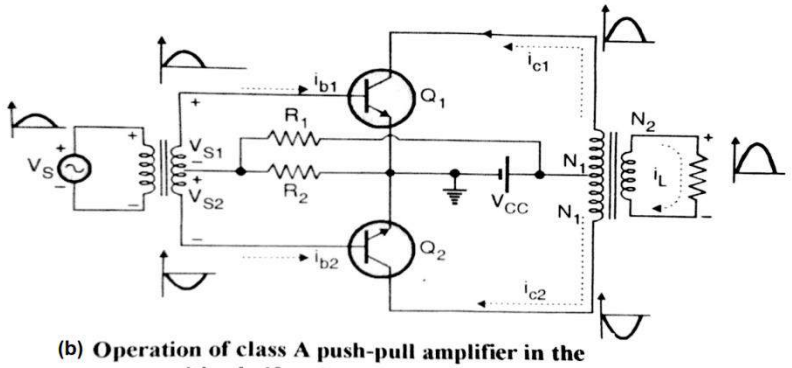
In the positive half cycle of input voltage $V_s$, the secondary voltage $V_{s1}$ will be positive while $V_{s2}$ will be negative, as shown in fig.(b). Therefore, transistor $Q_1$ is more forward biased while $Q_2$ is less forward biased. Therefore, $i_{c1}$ will increase and $i_{c2}$ will decrease. The output current $i_L$ is proportional to the difference between $i_{c1}$ and $i_{c2}$.

$i_L = \frac{N_1}{N_2}(i_{c1} - i_{c2})$ where, $\frac{N_1}{N_2}$ is the turns ratio of the output transformer.

Therefore in the positive half cycle of $V_s$, the output current will be positive. As the load is resistive, the load current will be in phase with the load voltage.

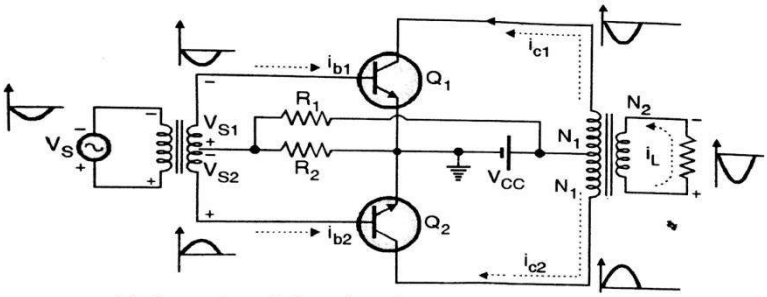
$$V_L = i_L R = \frac{N_1}{N_2}(i_{c1} - i_{c2})R$$

Therefore load voltage will be positive.




(b) Operation of class A push-pull amplifier in the positive half cycle

In the negative half cycle of input voltage $V_s$, the secondary voltage $V_{s1}$ will be negative while $V_{s2}$ will be positive, as shown in fig.(c). Therefore, transistor $Q_2$ will be more forward biased while $Q_2$ will be less forward biased. Therefore, $i_{c1}$ will decrease and $i_{c2}$ will increase. The output current $i_L$ is proportional to the difference between $i_{c1}$ and $i_{c2}$ and hence becomes negative. The load voltage, being in phase with load current, will also become negative.

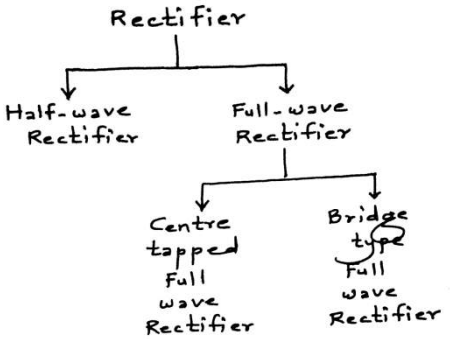



(c) Operation of class A push-pull amplifier in the negative half cycle

2 d) Classify rectifier and filter. 4

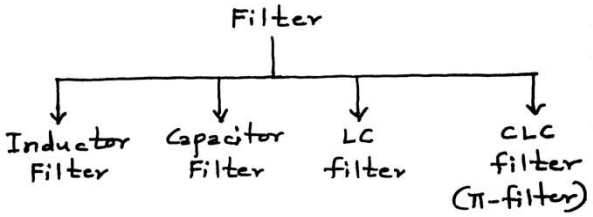
**Ans:**

**Classification of Rectifier:**




2 marks

**Classification of Filters:**




2 marks

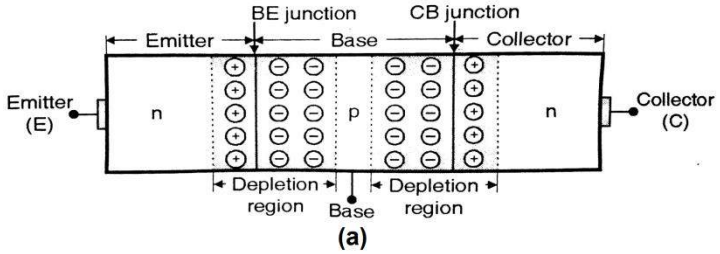
2 e) Explain construction and working principle of NPN transistor. 4

**Ans:**

**Construction of NPN transistor:**

A transistor is formed of two p-n junctions. For unbiased p-n junctions, the depletion regions are formed. The fig.(a) shows the depletion regions formed at the B-E and C-B junctions of n-p-n transistor.

1 mark for construction

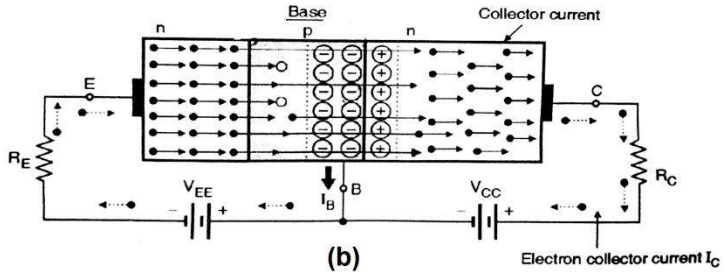



(a)

**Working Principle:**

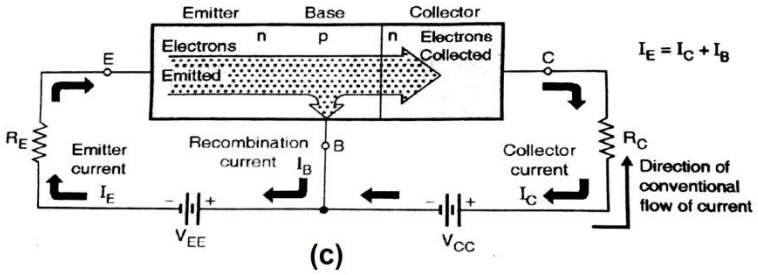
When the n-p-n transistor is biased, as shown in fig.(b), such that the emitter-base junction is forward biased and collector-base junction is reverse biased, the

minority and majority carriers are set into the motion. The majority carriers electrons from n-region enters into p-region and holes from p-region enters into n-region. Since the base is lightly doped than the emitter, almost all the current flowing across the B-E junction consists of electrons entering the base from the emitter. Hence the electrons are the majority carriers in n-p-n transistor. 3 marks for working principle




Some of the electrons entering into the base region do not reach the collector region. Instead they flow out of the base terminal via the base connection as shown in fig.(c) due to recombination. As the base region is very thin and lightly doped, there are very few holes available in the base region for recombination. Hence about 2% electrons will flow out of base due to recombination.

The remaining 98% electrons cross the reverse biased collector-base junction to constitute the collector current. They cross the collector region and collected by the supply $V_{cc}$. The emitter current is thus equal to the sum of the base current and collector current. $I_E = I_B + I_C$




2 f) A multistage amplifier is consisting of three stages, each having gain of 10. What is the overall voltage gain in dB? 4

**Ans:**

Data given:

Three stage amplifier

Gains: $Av_1 = Av_2 = Av_3 = 10$ Stepwise solution 4 marks

$\therefore$ Over-all gain = $Av_1 \times Av_2 \times Av_3$

$= 10 \times 10 \times 10$

$= 1000$

$\therefore$ Over-all gain in dB = $20 \log_{10}(1000)$

$= 60$ dB

**OR**

$Av_1 = 20 \log_{10}(10) = 20$ dB

$Av_2 = Av_3 = 20 \log_{10}(10) = 20$ dB

$\therefore$ Over-all gain in dB = $Av_1 + Av_2 + Av_3 = 20+20+20 = 60$ dB.

**3 Attempt any Four: 16**

3 a) Compare CB, CE and CC configurations on the basis of 4

i) Input impedance
ii) Current gain
iii) Voltage gain
iv) Output impedance

**Ans:**

**Comparison between CB, CE and CC configurations:**

| Parameter | CB | CE | CC |
|---|---|---|---|
| Input Impedance | Low<br>Or<br>50Ω | Medium<br>Or<br>600Ω to 4kΩ | High<br>Or<br>1 MΩ |
| Current Gain | Less than or equal to 1<br>Or<br>$\alpha = \frac{I_C}{I_E}$ | High<br>Or<br>$\beta = \frac{I_C}{I_B}$ | High<br>Or<br>$\gamma = \frac{I_E}{I_B}$ |
| Voltage Gain | Medium | Medium | Less than or equal to 1 |
| Output Impedance | High<br>Or<br>50 kΩ | Medium<br>Or<br>10 kΩ to 50 kΩ | Low<br>Or<br>50Ω |

1 mark for each point

3 b) Derive the relation between α and β with to BJT. 4

Ans:

**Relation between α and β:**

Current gain of transistor in CB configuration is ,

$$\alpha = \frac{I_C}{I_E}$$

But $I_E = I_B + I_C$

$$\alpha = \frac{I_C}{I_B + I_C}$$

Dividing numerator and denominator by $I_B$,

$$\alpha = \frac{\frac{I_C}{I_B}}{1 + \frac{I_C}{I_B}}$$

But $\beta = \frac{I_C}{I_B}$ the current gain of transistor in CE configuration.

Therefore,

$$\boldsymbol{\alpha = \frac{\beta}{1 + \beta}}$$

Stepwise derivation 4 marks

**OR**

Current gain of transistor in CE configuration is ,

$$\beta = \frac{I_C}{I_B}$$

But $I_E = I_B + I_C$, so $I_B = I_E - I_C$

$$\beta = \frac{I_C}{I_E - I_C}$$

Dividing numerator and denominator by $I_E$,

$$\beta = \frac{\frac{I_C}{I_E}}{1 - \frac{I_C}{I_E}}$$

Stepwise derivation 4 marks

But $\alpha = \frac{I_C}{I_E}$ the current gain of transistor in CE configuration.

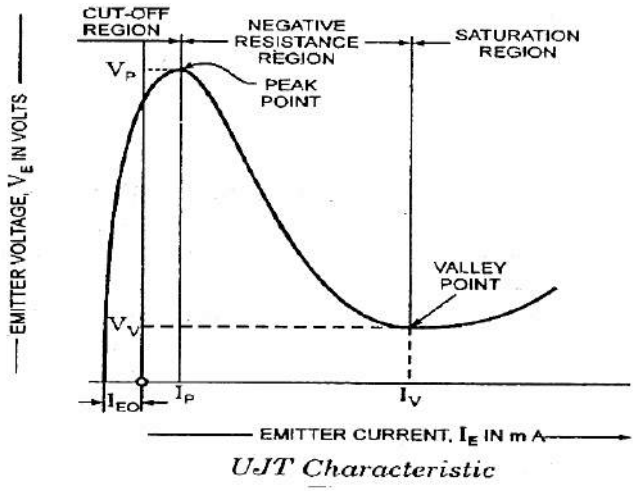
Therefore,

$$\boldsymbol{\beta = \frac{\alpha}{1 - \alpha}}$$

3 c) Draw and explain the characteristic of UJT. 4

**Ans:**

**UJT Characteristics:**




*UJT Characteristic*

2 marks for diagram with labels

The UJT characteristic is emitter voltage versus emitter current characteristic, as shown in the figure. For emitter voltages less than $V_P$ (peak point voltage) the UJT is in the off state and magnitude of $I_E$ is not greater than $I_{EO}$. The emitter current $I_{EO}$ corresponds very closely with the reverse leakage current $I_{CO}$ of a bipolar transistor. This region is known as the cut off region.

As the emitter voltage increases and reaches $V_P = (\eta V_{BB}+V_D)$, the UJT starts conducting. Then with increase in emitter $I_E$ the emitter voltage decreases as shown. The reduction in voltage across UJT is due to the drop in resistance $R_{B1}$ with increase in the value of $I_E$. This region of operation is known as a "Negative Resistance" region, which is stable enough to be used in various applications. Eventually the "valley point" will be reached and further increase in $I_E$ will place the device into saturation.

2 marks for explanation

3 d) Define load regulation and line regulation for regulated power supply with expression. 4

**Ans:**

**Load Regulation:**

It is defined as the change in output voltage expressed as fraction of full load output 2 marks for

voltage when the load current is changed from zero (no load) to full load value. definitions

$$\text{Load Regulation} = \frac{V_{NL}-V_{FL}}{V_{FL}} \text{ with } V_{in} \text{ constant}$$

$$\%\text{Load Regulation} = \frac{V_{NL}-V_{FL}}{V_{FL}} \times 100$$ 2 marks for expressions

where, $V_{NL}$ is the no load output voltage,
$V_{FL}$ is the full load output voltage

**Line Regulation:**
It is defined as the change in output voltage due to change in input voltage with load $R_L$ constant ($I_L$ constant)

$$\%\text{Line Regulation} = \frac{\Delta V_O \times 100}{V_O} \text{ with } R_L \text{ constant or } I_L \text{ constant.}$$

where, $V_O$ is the output voltage.

**OR**

Line Regulation$= V_{LH} - V_{LL}$
where, $V_{LH}$ is the load voltage with high line voltage,
$V_{LL}$ is the load voltage with low line voltage

3 e) Write important features of IC 723. 4

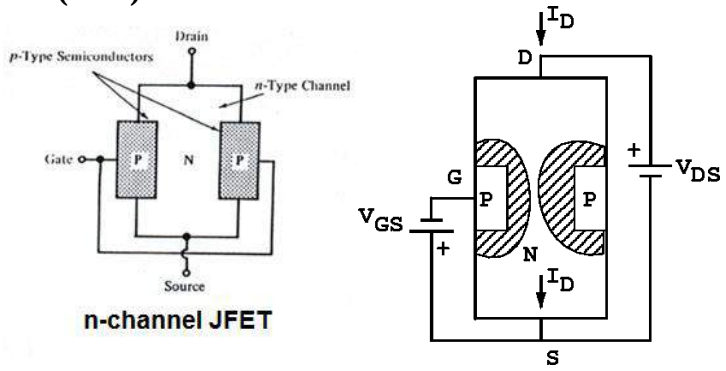
**Ans:**
**Important features of IC 723:**

i) It can be connected to function as a positive or negative voltage regulator with an output voltage ranging from 2V to 37V.
ii) Output current can be up to 150 mA.
iii) The maximum supply voltage is 40V.
iv) The line and load regulations are each 0.01%.
v) Built-in short circuit protection.
vi) Very low temperature drift.
vii) High ripple rejection.

1 mark for each of any four features

3 f) Draw and explain the construction of n-channel JFET (FET) 4

**Ans:**
**N-channel JFET (FET):**




2 marks for diagram

2 marks for explanation

**Construction:**
The n-channel JFET has n-type semiconductor used as a channel which has two terminals, drain and source. Two p-type semiconductors are attached at both sides of n-channel and forms third terminal gate. Thus pn junction exists between gate

and source.

1) When $V_{GS}$ = 0 volt:
When a voltage is applied between the drain and source with a DC supply voltage $V_{DD}$ with $V_{GS}$ = 0 V, the electrons flow from source to drain through the narrow channel existing between the depletion regions. This constitutes drain current $I_D$. The value of drain current is maximum when $V_{GS}$ = 0 V. This current is designated vy the symbol $I_{DSS}$.
2) When $V_{GS}$ is negative:
When $V_{GS}$ is increased below zero i.e negative, the reverse voltage across the gate source junction is incrased. As a result depletion regions are widened. This reduces effective width of channe and therefore controls the flow of drain current through the channel.
If $V_{GS}$ is increased further, two depletion regions touch each other. The drain current reduces to zero. The gate to source voltage at which current reduces to zero is called as pinch-off voltage.

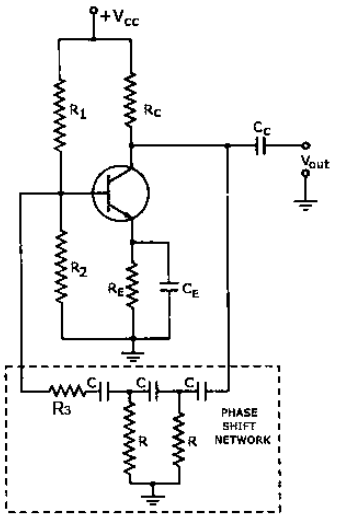
**4 Attempt any Four:** **16**

4 a) Draw the circuit diagram of RC phase shift oscillator. Write working in steps. Give the formula of frequency of oscillation. 4

**Ans:**

**RC Phase shift Oscillator:**

1) Circuit Diagram: 2 marks for circuit diagram
2) Working:
   - In RC phase shift oscillator, CE amplifier is used, which provides 180° phase shift between input and output.
   - In feedback network, three RC phase shift networks are used in which each network provides 60° phase shift, so that total phase shift is 180°. 1 mark for working
   - The total phase shift around whole circuit is 360°.
   - So circuit gets positive feedback and works as an oscillator. 1 mark



RC Phase Shift Oscillator

3) Frequency of Oscillations:

$$f_c = \frac{1}{2\pi RC\sqrt{6}}$$

4 b) In a Colpitt's oscillator, $C_1$ = 0.2 μF and $C_2$ = 0.02 μF. If the frequency of oscillation is 10kHz, find the value of inductor. Also find the required gain for the oscillation. 4

**Ans:**

Data Given:

$C_1$ = 0.2 μF $C_2$ = 0.02 μF $f_c$ = 10 kHz = $10\times10^3$ Hz.

To find out: Value of inductor (L) and Gain (A)

1) To find Inductor L:

In Colpitt's oscillator,

$f_c = \frac{1}{2\pi\sqrt{LC_T}} \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (i)$ 1 mark

where, $C_T = \frac{C_1C_2}{C_1+C_2} = \frac{0.2\times0.02}{0.2+0.02} = \frac{0.004}{0.22} = 0.018\mu F$ 1 mark

Substituting $C_T$ and $f_c$ into eq.(i),

$10 \times 10^3 = \frac{1}{2\pi\sqrt{L(0.018\times10^{-6})}}$

Squaring both sides,

$$L = \frac{1}{4\pi^2 \times 100 \times 10^6 \times 0.018 \times 10^{-6}}$$
$$= \frac{1}{4\pi^2\times1.8} = \frac{1}{70.99}$$
$$= 0.01408$$
$$= 14 \times 10^{-3}$$
$$\therefore \boldsymbol{L = 14\ mH}$$ 1 mark

2) To find A:

In Colpitt's oscillator,

$A > \frac{C_1}{C_2}$

$A > \frac{0.2}{0.02}$

$\therefore$ Gain A > 10. 1 mark

4 c) Convert the following decimal number into equivalent binary number. 4

i) 63.92 ii) 109

**Ans:**

**1) $(63.92)_{10} = (\ ?\ )_2$**

For integer part 63:

| | | | | |
|---|---|---|---|---|
| 2 | 63 | | | |
| 2 | 31 | 1 | LSB | 1 mark |
| 2 | 15 | 1 | ↑ | |
| 2 | 7 | 1 | | |
| 2 | 3 | 1 | | |
| 2 | 1 | 1 | | |
| | 0 | 1 | MSB | |

$(63)_{10} = (111111)_2$

For fractional part:

| | | | |
|---|---|---|---|
| 0.92×2 = | 1.84 | 1 | MSB |
| 0.92×2 = | 1.68 | 1 | ↓ |
| 0.92×2 = | 1.36 | 1 | |
| 0.92×2 = | 0.72 | 0 | 1 mark |
| 0.92×2 = | 1.44 | 1 | LSB |

$(.92)_{10} = (.11101)_2$

$\therefore \boldsymbol{(63.92)_{10} = (111111.11101)_2}$

**2) $(109)_{10} = (\ ?\ )_2$**

| | | | |
|---|---|---|---|
| 2 | 109 | | |
| 2 | 54 | 1 | LSB |
| 2 | 27 | 0 | ↑ |
| 2 | 13 | 1 | |
| 2 | 6 | 1 | |
| 2 | 3 | 0 | |
| 2 | 1 | 1 | |
| | 0 | 1 | MSB |

2 marks

**$\therefore (109)_{10} = (1101101)_2$**

4 d) Draw the symbol, logic expression and truth table for two input of the following gates: i) AND gate ii) OR gate. 4

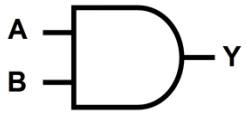
Ans:

**i) AND gate:**

Logical expression: Y = A·B

Truth Table:

| A | B | Y= A·B |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |



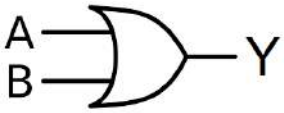

1 mark for symbol
1 mark for logical expression and truth table

**ii) OR gate:**

Logical expression: Y = A+B

Truth Table:

| **A** | **B** | Y= A+B |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |




1 mark for symbol
1 mark for logical expression and truth table

4 e) Draw and explain the O/P characteristic of JFET (FET). 4

**Ans:**

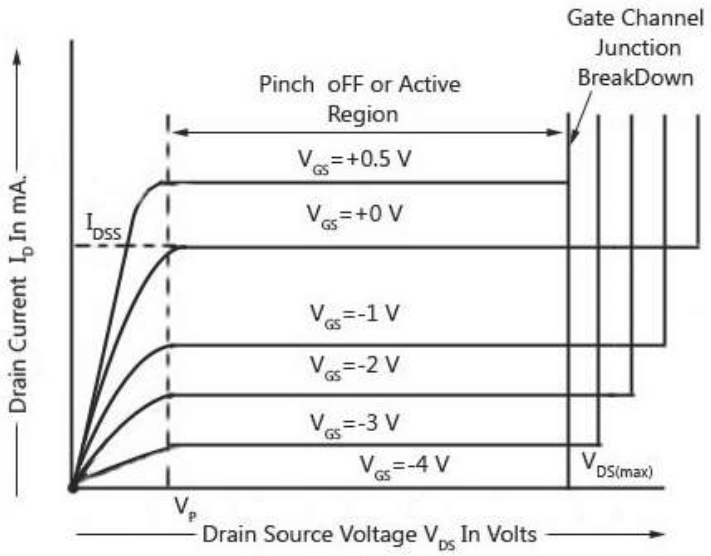
**Output Characteristics of JFET:**

- The output characteristics of JFET is plotted between the drain current $I_D$ and drain to source voltage $V_{DS}$ for constant gate to source voltage $V_{GS}$.
- When $V_{GS}$ = 0 volt constant, if we increase $V_{DS}$ , the drain current $I_D$ increases proportionally and remains constant after particular value of $V_{DS}$. This drain to source voltage is called pinch-off voltage $V_P$. This constant drain current is maximum current flowing through the JFET and known as source saturation current $I_{DSS}$.
- When we increase reverse bias on gate to source junction, the drain current

2 marks for explanation

decreases.

- When the reverse bias $V_{GS}$ is increased beyond certain value, the drain current becomes zero. This gate-source voltage is known as $V_{GS(Off)}$.




**Output Characteristics of JFET**

2 marks for diagram

4 f) Compare Hartley and Colpitt's oscillator. 4

**Ans:**

**Comparison between Hartley and Colpitt's oscillator:**

| Particulars | Hartley Oscillator | Colpitt's Oscillator |
|---|---|---|
| 1) Type of oscillator | It is a LC type of oscillator | It is a LC type of oscillator |
| 2) Components used | Two inductors and one capacitor are used in tank circuit. | Two capacitors and one inductor are used in tank circuit. |
| 3) Frequency of oscillation | $f_c = \frac{1}{2\pi\sqrt{L_T C}}$ $L_T = L_1 + L_2$ | $f_c = \frac{1}{2\pi\sqrt{L C_T}}$ $C_T = \frac{C_1 \times C_2}{C_1 + C_2}$ |
| 4) Advantages | Suitable at high frequencies<br>Small size<br>Low cost | Suitable at high frequencies<br>Small size<br>Low cost |
| 5) Disadvantages | Poor frequency stability | Poor frequency stability |

**5 Attempt any Four:** **16**

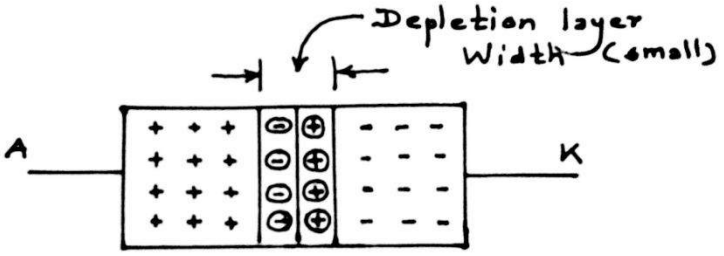
5 a) For a PN junction diode applied voltage are 0v, +5v, -10v. Draw the PN junction indicating relative width of the depletion region in each. 4

**Ans:**

**Relative Width of Depletion Region:**

**i) For 0 V:**

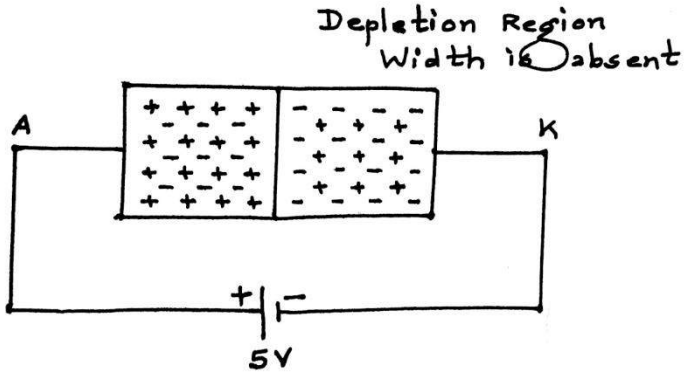
Depletion region width is comparatively small.




1 mark

**ii) For 5 V:**

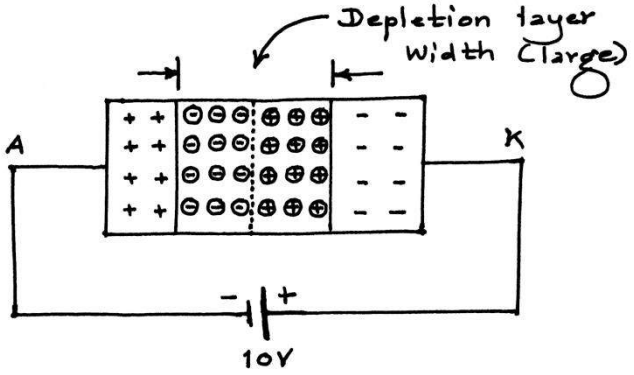
Diode is forward biased and conducting, hence depletion region is absent.




1 mark

**iii) For -10 V:**

Diode is reverse biased, the width of depletion region is increased.




2 marks

5 b) A full wave rectifier uses two diodes, the internal resistance of each diode may be assumed constant at 20Ω. The transformer r.m.s. secondary voltage from centre tap to each end of secondary is 50 V and load resistance is 980 Ω. Find: 4

i) the mean load current
ii) the rms value of load current

**Ans:**

Data Given: $V_{rms} = 50V$ $R_L = 980\ \Omega$ $R_S = 20\ \Omega$

To find out: $I_{dc} = ?$ $I_{rms} = ?$

In full-wave centre tap rectifier,

$$V_{rms} = \frac{V_m}{\sqrt{2}}$$

$$\therefore V_m = \sqrt{2} \times V_{rms} = \sqrt{2} \times 50$$

$$\therefore \boldsymbol{V_m = 70.71\ V}$$ 1 mark

Now the peak load current is given by, $I_m = \frac{V_m}{[R_S + R_L]} = \frac{70.71}{20+980} = 0.0707\ A$

$$\therefore \boldsymbol{I_m = 70.7\ mA}$$ 1 mark

The mean load current is given by,

$$I_{dc} = \frac{2I_m}{\pi} = \frac{70.7 \times 2}{3.142}$$

$$\boldsymbol{I_{dc} = 45.03\ mA}$$ 1 mark

The rms load current is given by,

$$I_{rms} = \frac{I_m}{\sqrt{2}} = \frac{70.7}{\sqrt{2}}$$

$$\boldsymbol{I_{rms} = 50.14\ mA}$$ 1 mark

5 c) List the type of biasing circuit. Draw the diagram of voltage divider bias method and describe its operation. 4

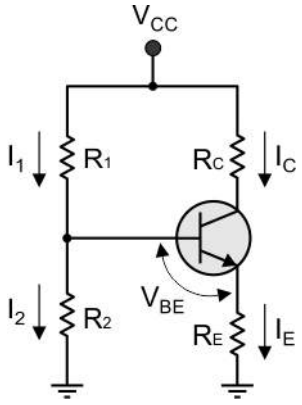
**Ans:**

**Types of Biasing Circuits:**

i) Base bias (Fixed bias)
ii) Base bias with emitter feedback (Emitter feedback bias)
iii) Base bias with collector feedback (Collector feedback bias)
iv) Voltage divider bias (Self bias)
v) Emitter bias

**Voltage Divider Bias:**

$R_1$, $R_2$ and $R_E$ are biasing resistors and $V_{CC}$ is biasing voltage.




Voltage at base of transistor is

$$V_B = \frac{R_2}{R_1 + R_2} V_{CC}$$

Applying KVL at input circuit,

$$V_B - V_{BE} - V_E = 0$$

Since $V_{BE}$ is very small

$$V_B = V_E$$

Now, $I_E = \frac{V_E}{R_E}$

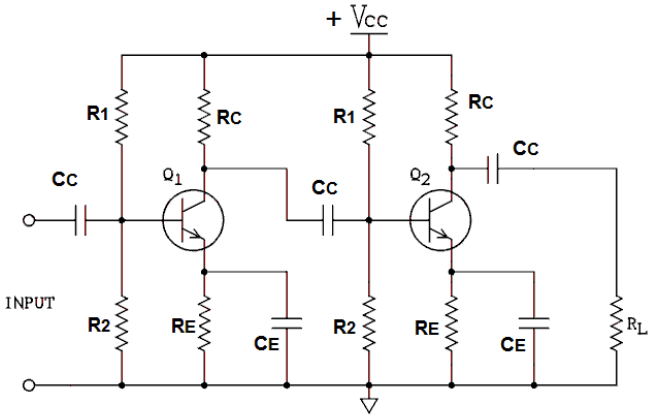
$$\therefore I_C = \frac{V_E}{R_E} \qquad [since\ I_C \cong I_E]$$

Applying KVL to output circuit,

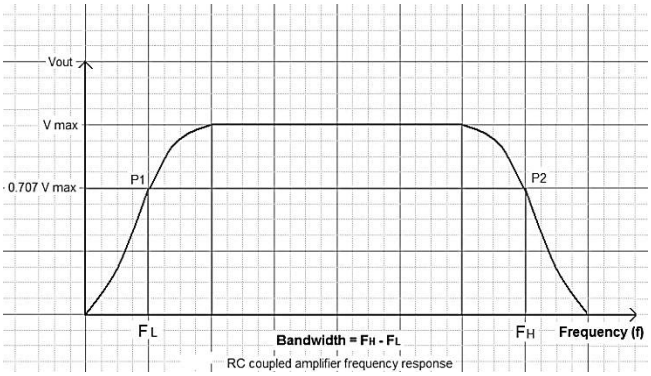
$$V_{CC} - I_C R_C - V_{CE} - V_E = 0$$
$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$
$$V_{CE} = V_{CC} - I_E(R_C + R_E) \qquad [since\ I_C \cong I_E]$$

5 d) Draw two stage RC coupled amplifier and draw its frequency response. Show the bandwidth. 4

**Ans:**




Two-stage RC coupled Amplifier




2 marks for circuit diagram

1 marks for frequency response plot

1 mark for bandwidth

5 e) Compare transformer coupled amplifier with RC coupled amplifier. 4

**Ans:**

| Particulars | RC Coupled Amplifier | Transformer Coupled Amplifier |
|---|---|---|
| 1) Size | Small | Comparatively large and bulky |
| 2) Cost | Low | Comparatively costly |
| 3) Frequency Response | Excellent in audio frequency range | Poor |
| 4) Impedance matching | Not good | Excellent |
| 5) Applications | Voltage amplification | Power amplification |

1 mark for each of any four points

5 f) Compare JFET with MOSFET. 4

**Ans:**

| Particulars | JFET | MOSFET |
|---|---|---|
| 1) Type | Voltage controlled device | Voltage controlled device |
| 2) Mode of operation | Operates only in depletion mode | Operates in depletion and enhancement mode |
| 3) Input impedance | Higher | Higher than JFET |

1 mark for each of any four points

| | | |
|---|---|---|
| 4) Characteristic curve | More flat | Less flat than FET |
| 5) Gate to source junction | Only reverse bias | Forward or reverse bias |
| 6) Gate connection | Not isolated from substrate | Isolated by $SiO_2$ layer from substrate |

**(Examiner may consider any other points of comparison during evaluation)**

**6 Attempt any Four: 16**

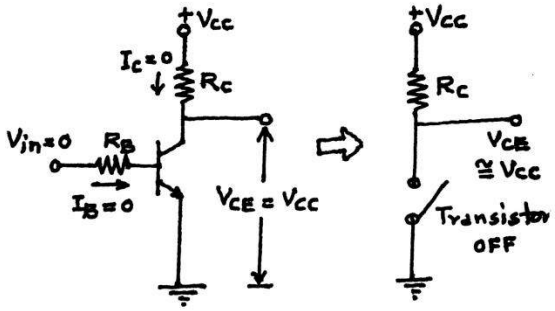
6 a) Describe transistor as a switch with neat diagram. 4

**Ans:**

**Transistor as Switch:**

A transistor can be used for two types of applications viz. amplification and switching. For amplification, the transistor is biased in its active region.
For switching applications, transistor is biased to operate in the saturation (full on) or cut-off (full off) region.

**(i) Transistor in cut-off region (Open switch):**

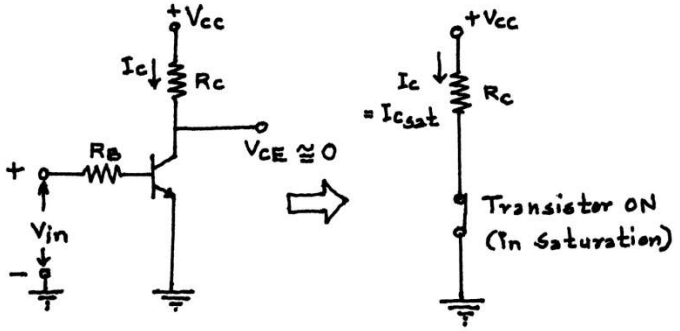



1 mark for diagram

In the cur-off region, both the junctions of transistor are reverse biased and very small reverse current flows through the transistor.
The voltage drop across the transistor ($V_{CE}$) is high, nearly equal to supply voltage $V_{CC}$. Thus, in cut-off region the transistor is equivalent to an open switch as shown in fig.(a).

1 mark for explanation

**(ii) Transistor in Saturation region (Closed switch):**




1 mark for diagram

When $V_{in}$ is positive, a large base current flows and transistor saturates. In the saturation region, both the junctions of transistor are forward biased. The collector current is very large, the voltage drop across the transistor ($V_{CE}$) is very small, of the order of 0.2V to 1 V, depending on

1 mark for explanation

the type of transistor. Thus in saturation region, the transistor is equivalent to a closed switch.

6 b) Define: 4

i) Drain resistance
ii) Transconductance
iii) Amplification factor
iv) Pinch off voltage of FET.

**Ans:**

**i) Drain Resistance:**

(a) DC drain resistance, also known as static or ohmic resistance of channel, is expressed as, $R_{DS} = \frac{V_{DS}}{I_D}$

(b) AC drain resistance, also known as dynamic resistance of channel, is defined as resistance between drain to source when JFET is operating in pinch-off or saturation region and expressed as,

$$r_d = \frac{\Delta V_{DS}}{\Delta I_D}$$

1 mark for each correct definition

**ii) Transconductance:**

It is also known as forward transconductance ($g_m$). It is the ratio of small change in drain current to corresponding change in gate to source voltage.

$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$, keeping $V_{DS}$ constant.

**iii) Amplification Factor:**

It is defined as the ratio of small change in drain voltage to small change in gate voltage at constant drain current.

Amplification factor $\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}}$ , keeping $I_D$ constant.

**iv) Pinch-off Voltage:**

It is the value of the drain to source voltage $V_{DS}$ at which the drain current $I_D$ reaches its constant saturation value. Any further increase in $V_{DS}$ does not have any effect on the value of $I_D$. It is denoted by $V_P$.

6 c) Draw transistorized series regulator and explain its working. 4

**Ans:**

**Transistorized Series Regulator:**

The figure shows a circuit of a transistor series regulator. Since the transistor is connected in series with the load, the circuit is known as a series regulator.

**Operation:**

i) The unregulated DC supply is fed to the input terminal as shown in the figure.

ii) The output voltage is given by $V_L = V_Z - V_{BE}$

iii) $V_Z$ being a zener voltage, can assumed constant. Therefore, if the output voltage varies, the $V_{BE}$ changes.

iv) If the output voltage increases due to some reason, then $V_{BE}$ decreases and due to this base current decreases. Therefore the collector current decreases.

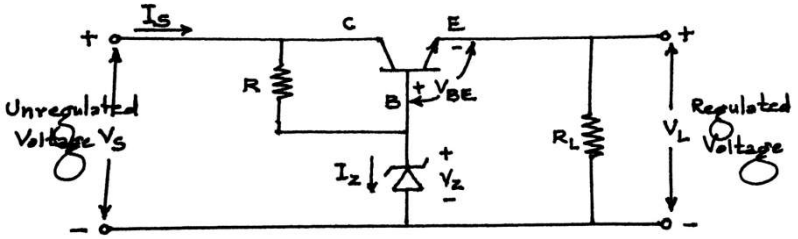
2 marks for operation

v) This will increase the collector to emitter voltage ($V_{CE}$) across the transistor and $V_L$ will be regulated, as $V_L = V_S - V_{CE}$

vi) If the output voltage decreases, then exactly opposite action will take place and the output voltage is regulated.

vii) The circuit action may be summarized in the form of following equation.

$V_L\downarrow \rightarrow V_{BE}\downarrow \rightarrow I_B\downarrow \rightarrow I_C\downarrow \rightarrow V_{CE}\uparrow \rightarrow V_L\downarrow$




2 marks for circuit diagram

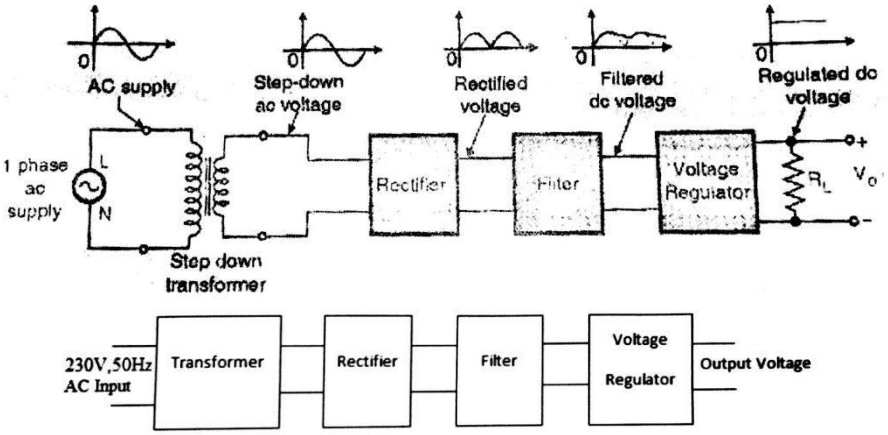
6 d) Draw the block diagram for DC power supply; explain the function of each block. 4

**Ans:**

**DC Power Supply:**

There are four basic blocks of a DC regulated power supply. They are:

1) Step-down transformer
2) Rectifier
3) Filter
4) Voltage Regulator




**Functions of Each Block:**

i) Step-down transformer: Reduces 230V, 50 hz ac voltage to required ac voltage level.

ii) Rectifier: Converts ac voltage into dc voltage. Typically bridge type full-wave rectifier is widely used.

iii) Filter: Used to remove fluctuations (ripples) present in dc output.

iv) Voltage regulator: Provides constant dc output voltage irrespective of changes in load current or changes in input voltage.
Voltage divider circuit is used to provide different dc voltages required for different electronic circuits.

6 e) Write advantages and disadvantages of positive and negative feedback. 4

**Ans:**

**Advantages of Positive Feedback:**

i) Voltage gain increases.
ii) No phase shift is provided.
iii) Feedback signal and input signal are in phase.
iv) Input and Output voltage increases.

**Disadvantages of Positive Feedback:**

i) Stability becomes poor as feedback increases.
ii) Noise increases with feedback.
iii) Bandwidth decreases.
iv) Input impedance decreases.

**Advantages of Negative Feedback:**

i) Stability becomes better as feedback increases.
ii) Noise decreases with feedback.
iii) Bandwidth increases.
iv) Input impedance increases.

**Disadvantages of Negative Feedback:**

i) Voltage gain decreases.
Phase shift of 180° is provided.
ii) Feedback signal and input signal are out of phase.
iii) Input and Output voltage decreases.

6 f) a) Define junction field effect transistor (JFET) and give an example. 2

**Ans:**

**Junction Field-Effect Transistor:**

It is a semiconductor device having three terminals, namely Gate, Drain and Source, in which the current flow is controlled by an electric field set up by an external voltage applied to gate terminal. — 1 mark for definition

Types of JFET are: i) n-channel JFET and ii) p-channel JFET — 1 mark for example

Examples of JFET: BFW 10, BFW 11

6 f) b) Convert $(AFB2)_{16}$ to Binary number. 2

**Ans:** — 1mark for step

Hexadecimal Number

| A | F | B | 2 |
|---|---|---|---|
| 1010 | 1111 | 1011 | 0010 |

1 mark for final ans

$\therefore (AFB2)_{16} = (1010\ \ 1111\ \ 1011\ \ 0010)_2$