WINTER– 16 EXAMINATION

Model Answer Subject Code: 17320

Important Instructions to examiners:

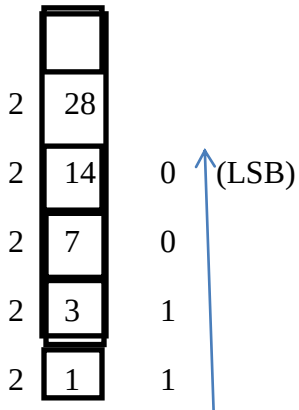
1) The answers should be examined by key words and not as word-to-word as given in the model answer scheme.
2) The model answer and the answer written by candidate may vary but the examiner may try to assess the understanding level of the candidate.
3) The language errors such as grammatical, spelling errors should not be given more Importance (Not applicable for subject English and Communication Skills.
4) While assessing figures, examiner may give credit for principal components indicated in the figure. The figures drawn by candidate and model answer may vary. The examiner may give credit for any equivalent figure drawn.
5) Credits may be given step wise for numerical problems. In some cases, the assumed constant values may vary and there may be some difference in the candidate's answers and model answer.
6) In case of some questions credit may be given by judgement on part of examiner of relevant answer based on candidate's understanding.
7) For programming language papers, credit may be given to any other program based on equivalent concept.

1. Attempt any TEN: 20

(a) Convert (i) $(28.56)_{10} = (?)_2$ (ii) $(372)_8 = (?)_{10}$

Ans:-(each conversion -1Mark)

i)



i.e $(28)_{10} = (11100)_2$

To convert the Fractional part

Decimal fraction	Product	Integer digit
0.56x2	1.12	1
0.12x2	0.24	0
0.24x2	0.48	0

0.48x2	0.96	0

i.e $(28.56)_{10}=(11100.1000)_2$

ii) $(372)_8=(\ )_{10}$

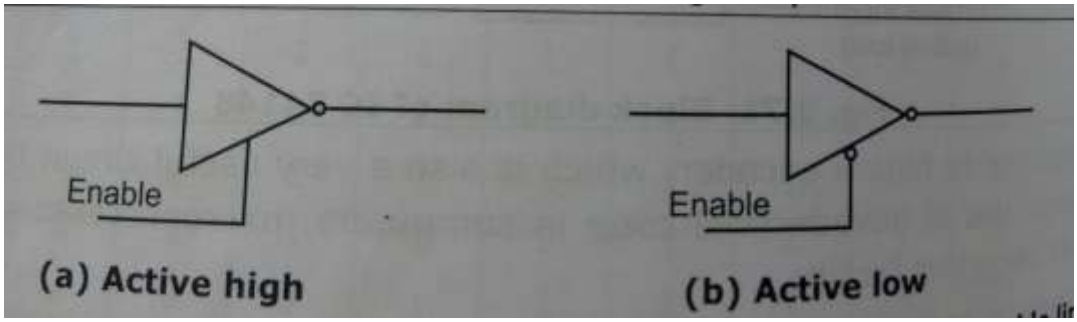
$(3x8^2)+(7x8^1)+(2x8^0)$

$= 192+56+2 =250$

$(372)_8 = (250)_{10}$

(b) Draw logic diagram of tristate buffer with active low enable and active high enable.

Ans:- (each – 1 mks)



(c) Draw truth table for logic gates represented by following IC's :
(i) IC7400
(ii) IC7402

Ans:- (each – 1 mks)

i)IC 7400---NAND gate

Input A	Input B	Output
0	0	1
0	1	1
1	0	1
1	1	0

ii)

IC 7402-----NOR gate

Input A	Input B	Output
0	0	1
0	1	0
1	0	0
1	1	0

(d) State triggering methods in digital circuits (any two)

Ans:- (1 mks each)

The triggering methods are-

1) Level triggering-Types: i) Positive Level triggering ii) Negative level triggering
2) Edge triggering- Types: i) Positive Edge triggering ii) Negative Edge triggering

(e) Identify SOP and POS equations:

(i) AB + CD

(ii) (A + B) (C + D)

Ans:- (each correct identification—1 mark)

i) AB+CD is a SOP equation

ii) (A+B)(C+D) is a POS equation

(f) Differentiate between RAM & ROM (2 points)

Ans:- (any 2 points- 2 mks)

	RAM	**ROM**
1	RAM is Random Access Memory	ROM is Read Only Memory
2	RAM is used for reading and writing purpose,	ROM is used only for reading purpose.
3	RAM is used for Temporary Data Storage	ROM is used for Permanent Data Storage.

4	Types : SRAM, DRAM	Types : PROM, EPROM, EEPROM
5	Applications : Calculators, Computers.	Applications : Computers, Microprocessors.

g) List any two non-weighted codes.

Ans (each code- 1 Mark)

1) Excess -3 code
2) Gray code

h) Add the binary numbers (1011) & (1100)
Ans: (proper calculation-2 mks)

$$\begin{array}{rr} & 1\,0\,1\,1 \\ + & 1\,1\,0\,0 \\ \hline & 1\,0\,1\,\;1\,1 \end{array}$$

i) Find Y1 and Y2 for fig 1 and 2 respectively

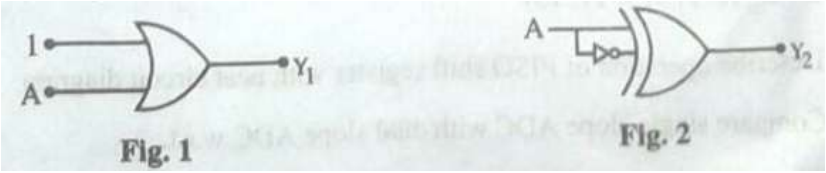
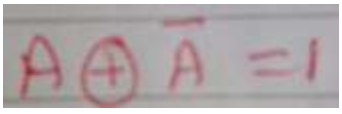


Fig. 1 Fig. 2

Ans (Each correct output—1 mark)

Fig 1, output Y1=1+A=A

Fig 2 , output Y2=



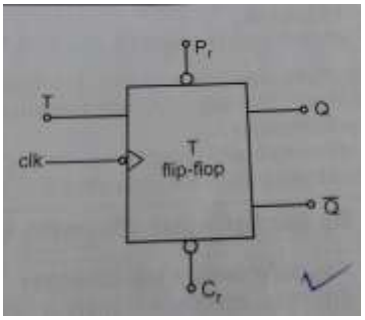
j) Define universal shift register.
Ans:- (2mks for relevant answer)

It is a register which can shift data in both directions as well as load it in parallel . Thus this register is capable of performing

1) Parallel loading
2) Shifting the data serially to the left
3) Shifting the data serially to the right.

k) Draw symbol of T FF & write its truth table.

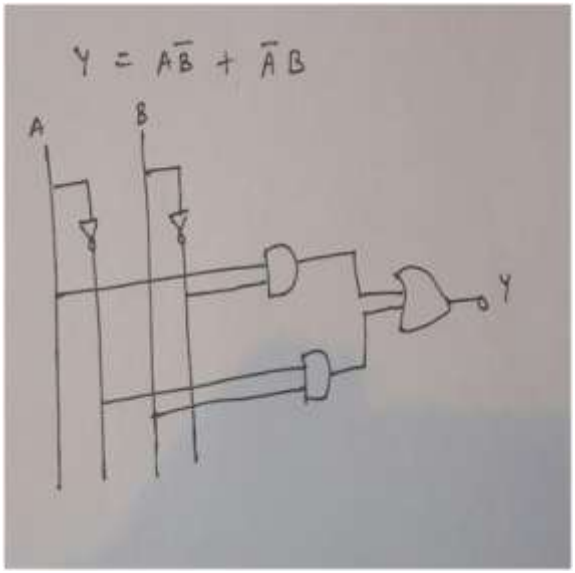
Ans:- (1 mks each)



clk	Input T_n	Output Q_{n+1}
↓	0	Q_n
↓	1	$\bar{Q}_n$

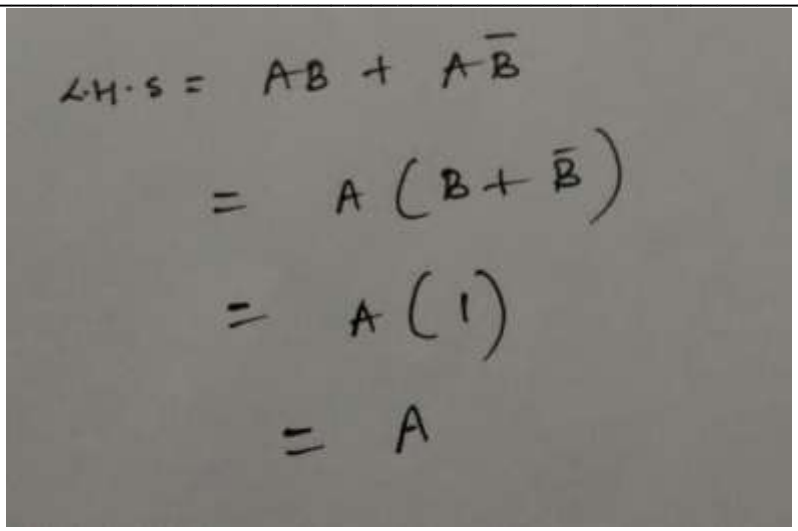
l) Implement given logic equations, using basic gates Y = 

Ans:- (2 mks for relevant proper diagram)



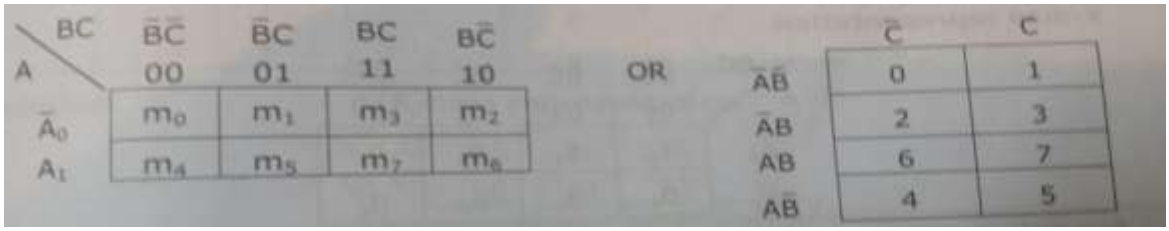
m) Prove that  = A, using laws of Boolean Algebra.

Ans:- (proper step by step answer – 2 mks)



n) Draw 3 variable K-map format.

Ans:- (any one – 2 mks)



2. Attempt any FOUR : 16

(a) Subtract $(1101)_2$ from $(1110)_2$ using 1's & 2's complement method.

Ans:(each method 2 Marks)

1"s complement method

Step1 1's complement of 1101—0010

Step 2 1 1 1 0
+ 0 0 1 0
---
1 0 0 0 0

Since End around carry is generated add it to the result and answer is positive

Step 3 0 0 0 0
\+ 1
---
0 0 0 1

Ans is $(0001)_2$

2"s complement method

Step 1 2"s complement of 1101-----0011

Step 2 1 1 1 0

\+ 0 0 1 1

---

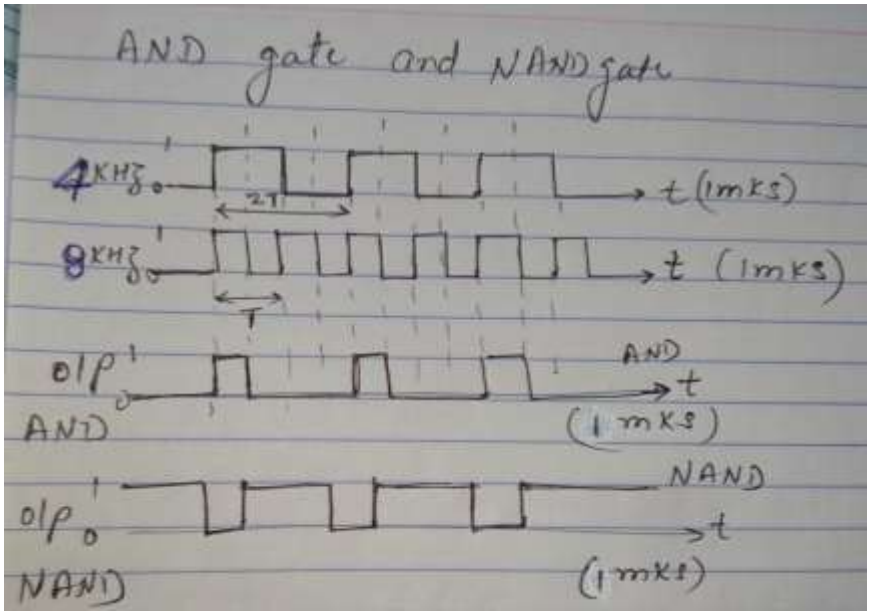
1 0 0 0 1

Since End around carry is generated it has to be neglected and answer is positive

Ans is $(0001)_2$

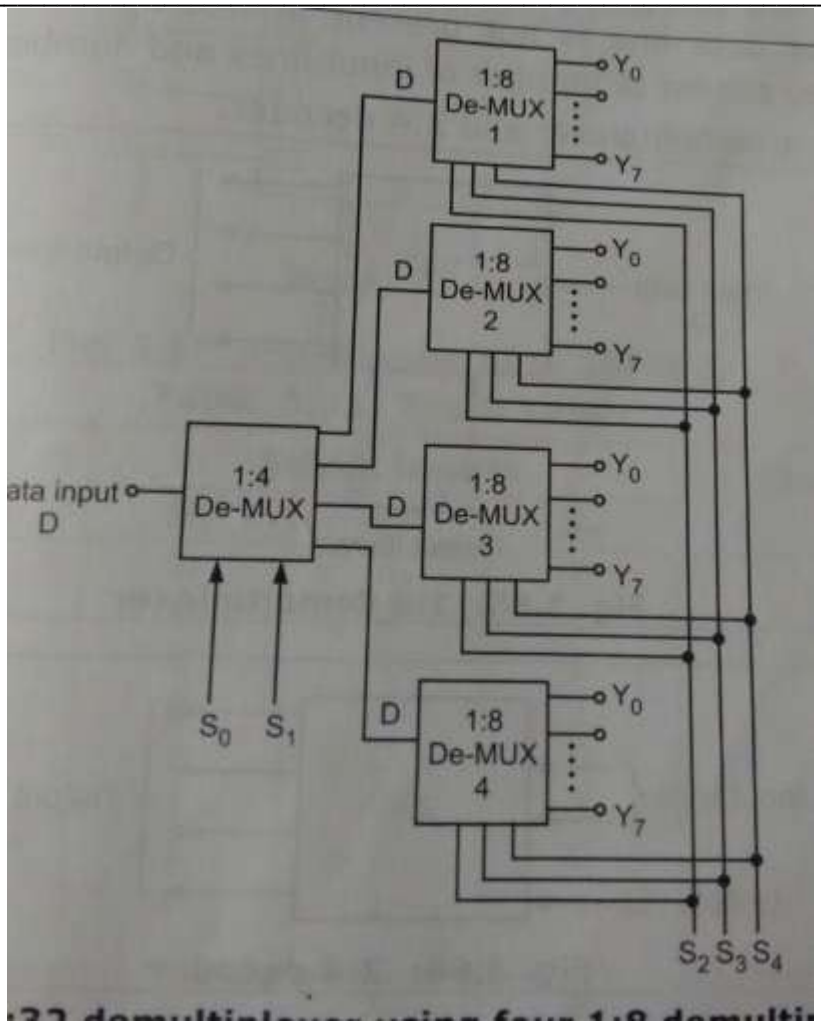
(b) Two square waves of 4 kH_Z & 8 kH_Z are applied as the inputs of AND gate & NAND gate. Draw the output waveform in each case. 1 mark each

Ans:-



(c) Design 1 : 32 De MUX using 1 :8 De MUX.

Ans:- (Relevant design- 4 mks)



(d) Write down excitation table of JK & DFF.

Ans:- (each excitation table -2 mks)

Excitation table of J-k FF

Q_n	Q_{N+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

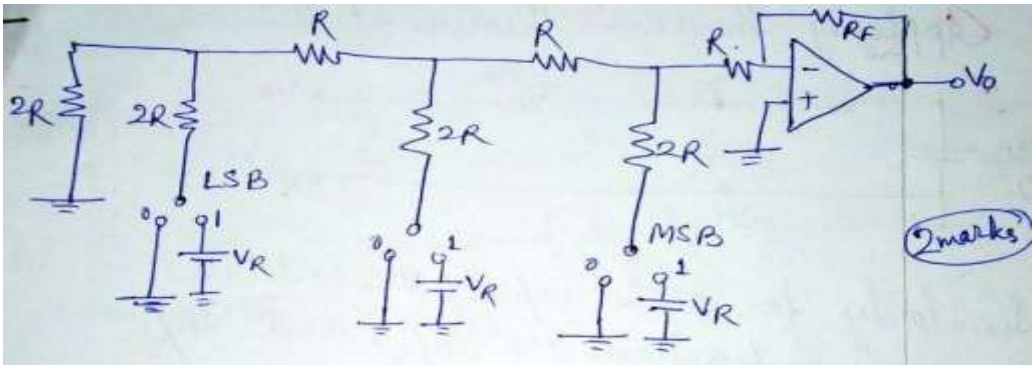
Excitation table of D FF

Q_n	Q_{n+1}	D

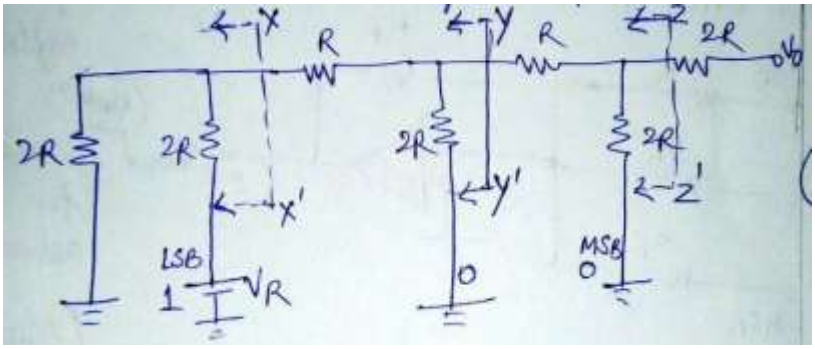
0	0	0
0	1	1
1	0	0
1	1	1

(e) Describe 3 bit R-2R ladder DAC with neat diagram.
Ans : Circuit diagram : 2 marks, description: 2 marks.

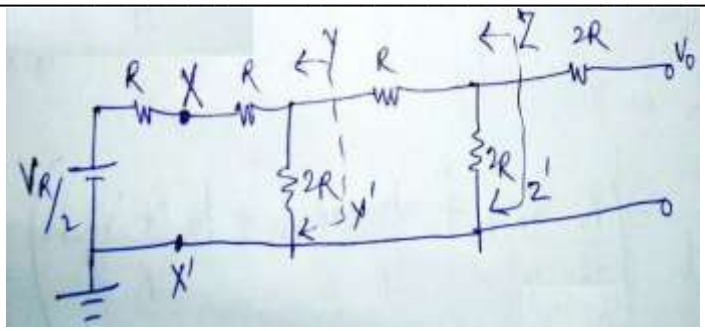
R -2R ladder DAC uses two resistors R & 2R. The input is applied through digitally controlled switches.



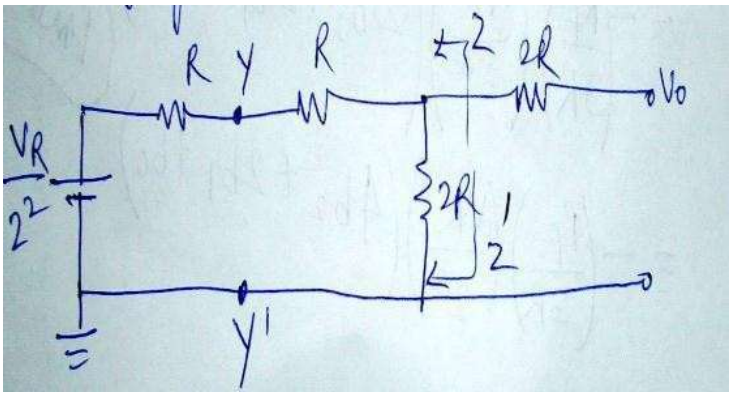
For example if the digital input is 001



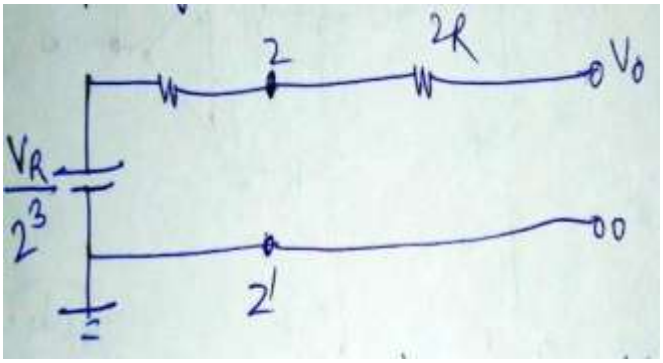
Applying Thevenins theorem at XX´



Applying Thevenins theorem at yy´

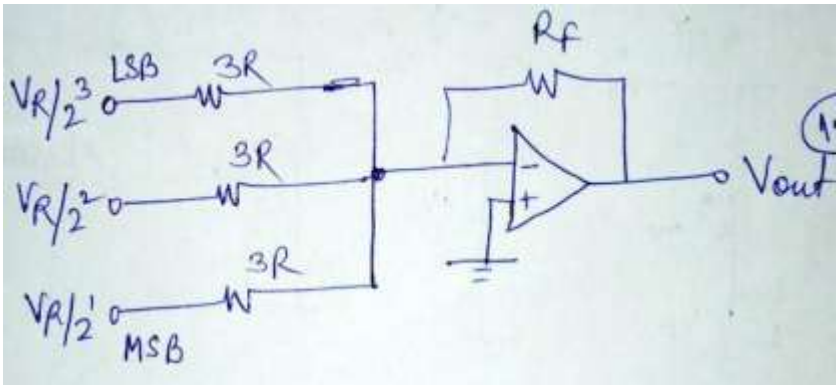


Applying Thevenins theorem at zz´



Similarly for digital input 010 and 100 the equivalent voltages are $V_R/2^2$

And $V_R/2^1$ respectively. The equivalent resistance is 3R in each case. So the simplified circuit of 3bit R-2R ladder DAC is



The analog output voltage for a given digital input is given by

Vout = - (RF/3R VR x b0/2^3 + RF/3R VR x b1/2^2 + RF/3R VR x b2/2^1)

= - (RF/3R) (VR/2^3) (2^2b2 + 2^1b1 + 2^0 b0)

= - (RF/3R) (VR/2^3) (4b2 + 2b1 + b0)

(f) Compare Static RAM & Dynamic RAM (any 4 points).

Ans:- (Relevant four comparison- 4 mks)

SR. NO.	PARAMETER	STATIC RAM	DYNAMIC RAM
1.	**Components**	Flip-flops, using bipolar or MOS transistors are used as basic memory cell.	Flip flops using MOS transistors& parasitic capacitance are used.
2.	**Refreshing**	Not required	Required as charge leaks
3.	**Speed**	Access time is less hence these are faster memories.	Access time is more hence these are slower memories.

4.	**Power Consumption**	More	Less
5.	**Space**	A Static RAM possesses more space in the chip than Dynamic RAM.	A Dynamic RAM possesses less space than a static RAM.
6.	**Cost**	More expensive	Less expensive.
7.	**Storage Capacity**	Less	High
8.	**No. of Components per cell**	More	Less
9.	**Bit Stored**	In the form of voltage.	In the form of charges.
10.	**Application**	Used in cars, household appliances, handheld electronic devices.	Used for computer memory.

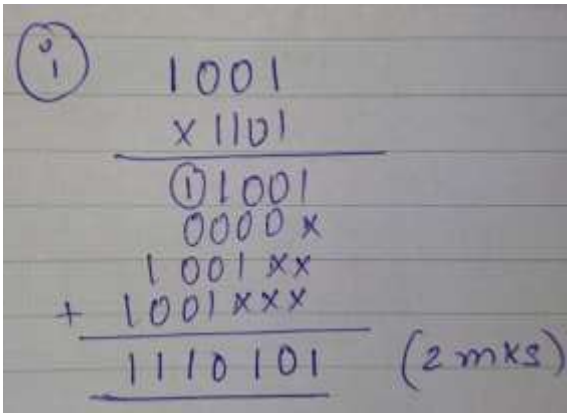
3. Attempt any FOUR : 16

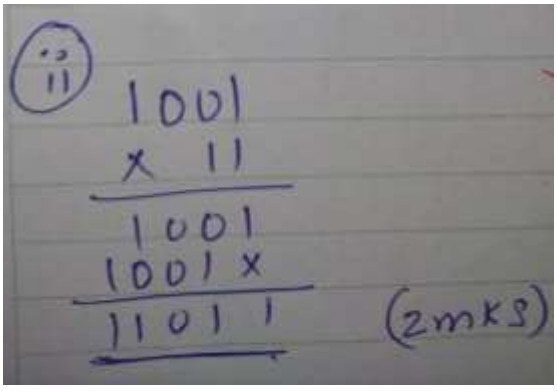
(a) Perform the following operations :

(i) $(1001)_2 \times (1101)_2$

(ii) $(1001)_2 \times (11)_2$

Ans:-





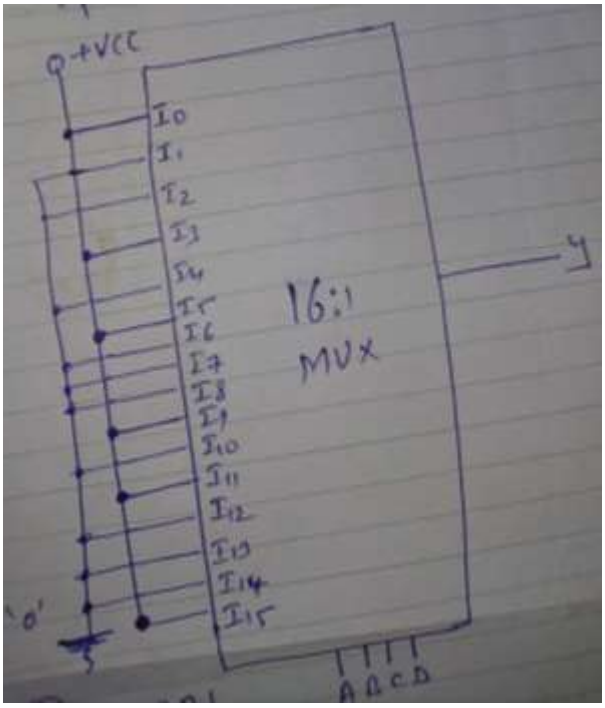
(b) Compare TTL, ECL & CMOS logic families (any 4 points)

Ans:- (Any 4 relevant point- 1 mks each)

Parameter	TTL	CMOS	ECL
Basic Gates	NAND	NOR or NAND	OR-NOR
Fan-out	10	50	25
Propagation delay	10 ns	70-105 ns	2 ns
Power dissipation	10 mW	1.01 mW	40-55 mW
Speed power product	100 pJ	0.7 pJ	100 pJ
Clock rate	35 MHz	10 MHz	760 MHz

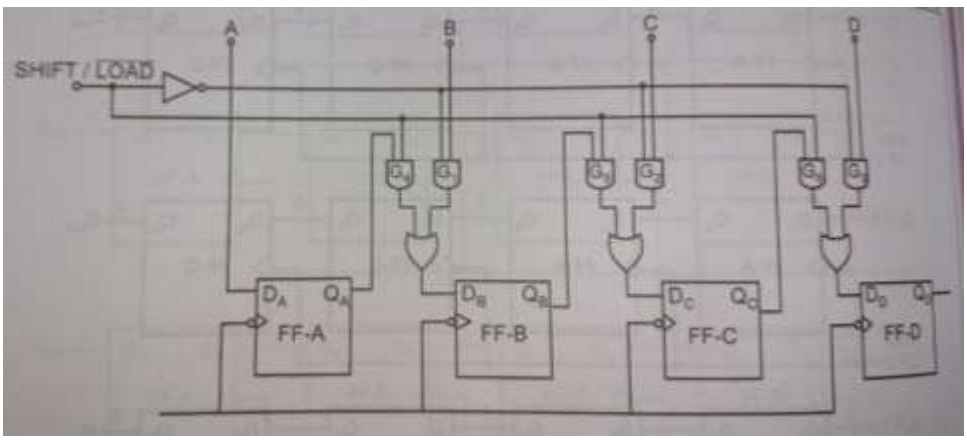
(c) Realize following expression using MUX: $f = \Sigma_m (0, 3, 5, 9, 11, 15)$

Ans:-(Proper relevant diagram-4 mks)

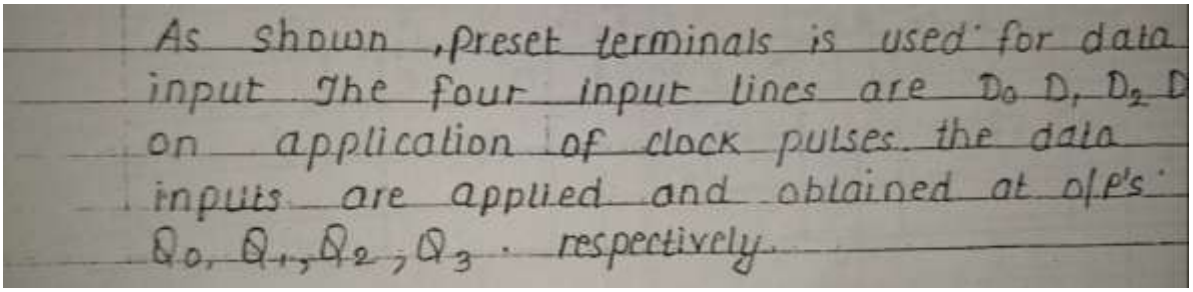


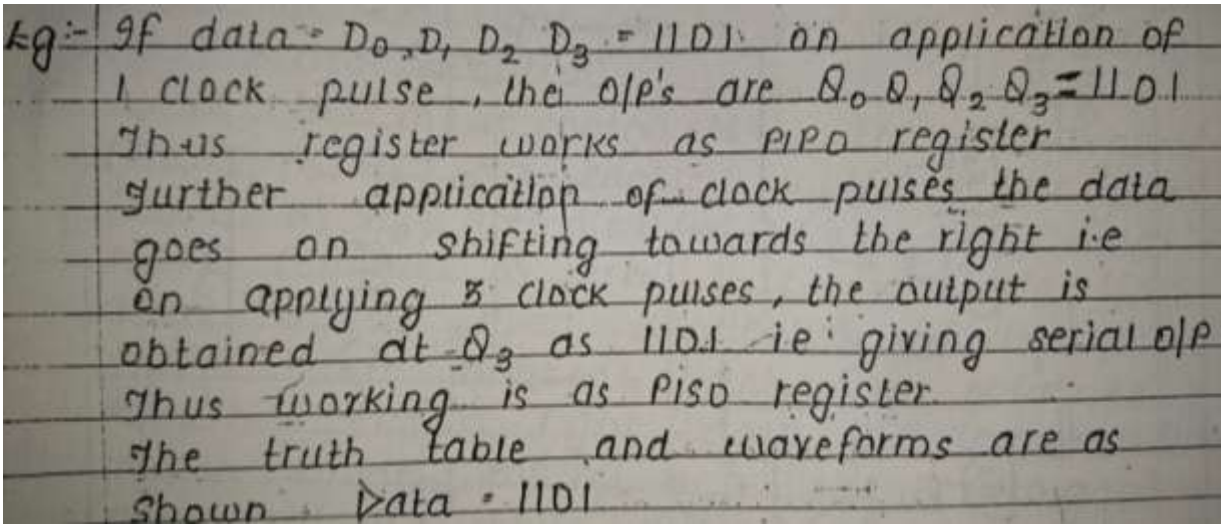
(d) Describe operation of PISO shift register with neat circuit diagram.

Ans:-(Circuit diagram-2 or 3 or 4 bit PISO- 2 mks , truth table- 1mks, explanation- 1 mks, waveforms- optional)

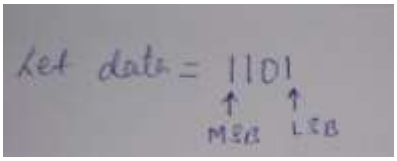


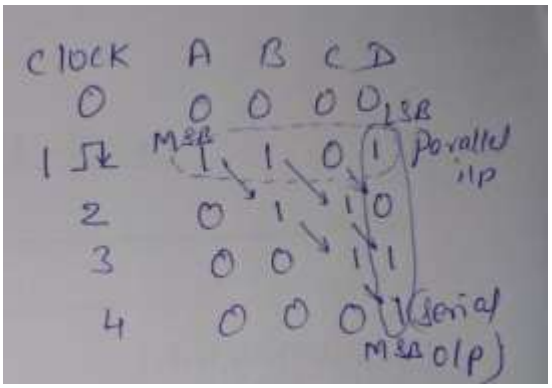
Explanation-



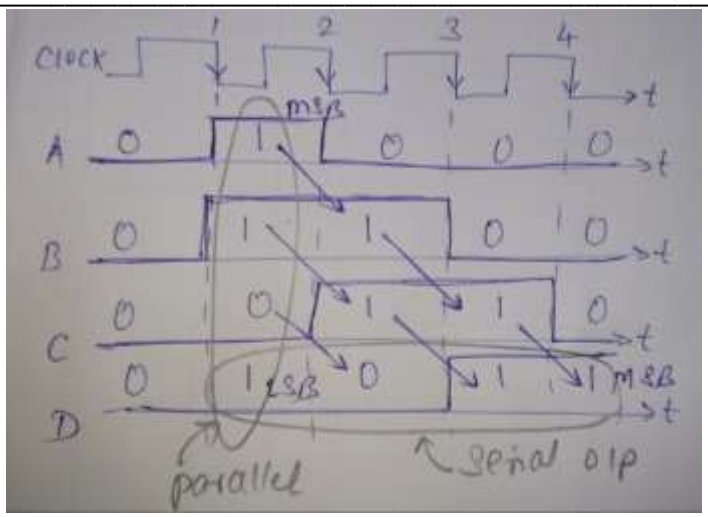


Truth table





Waveforms



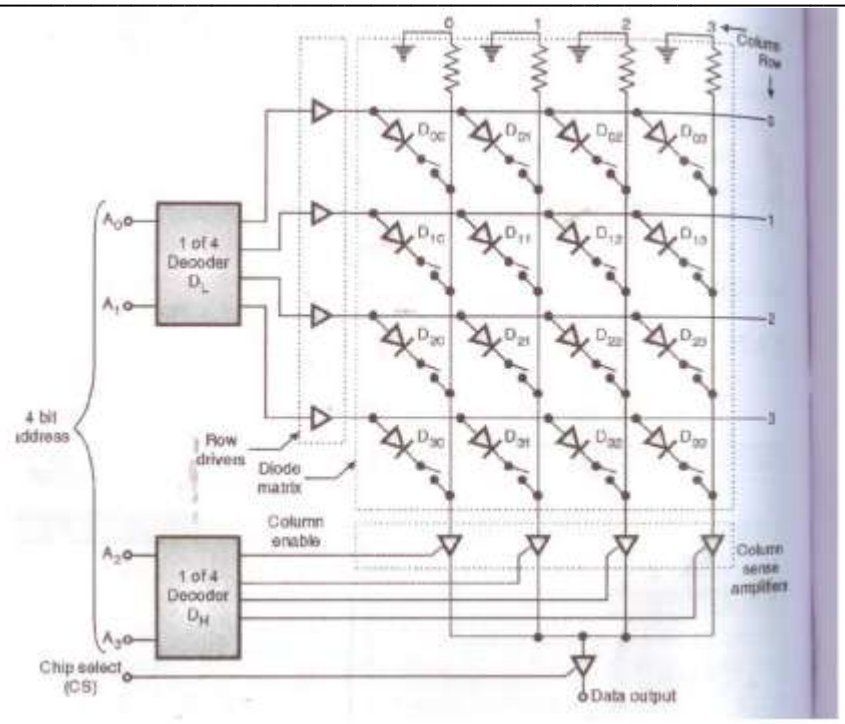
(e) Compare single slop ADC with dual slop ADC w.r.t.

Ans :- (Relevant comparison- 4 mks)

Single slope ADC	Dual slope ADC
Single-slope ADCs are appropriate for very high accuracy of high-resolution measurements where the input signal bandwidth is relatively low	Dual slope ADCs provides increased range, the increased accuracy and resolution, and the increased speed
Besides the accuracy these types of converters offer a low-cost alternative to others	Comparatively Dual slope ADCs are costlier
The name implies that single-slope ADC use only one ramp cycle to measure each input signal	Dual-Slope ADC operate on the principle of integrating the unknown input and then comparing the integration times with a reference cycle.
They provide less speed compared to dual slope	They provide increased speed compared to single slope.

(f) Draw organization of 4 × 4 memory and lable it.

Ans:- (proper labelled diagram- 4 mks)



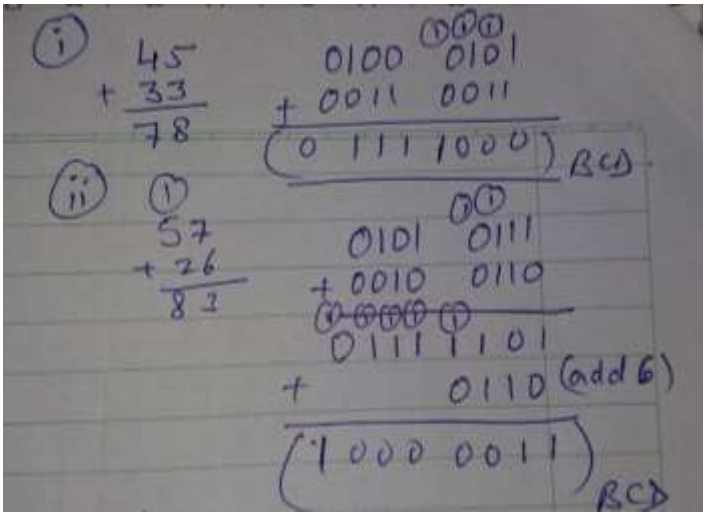
4. Attempt any FOUR : 16

(a) Perform BCD addition :

(i) $(45)_{10} + (33)_{10}$

(ii) $(57)_{10} + (26)_{10}$

Ans:- (2 mks each)



(b) Define following characteristics of logic families :

(i) Fan in

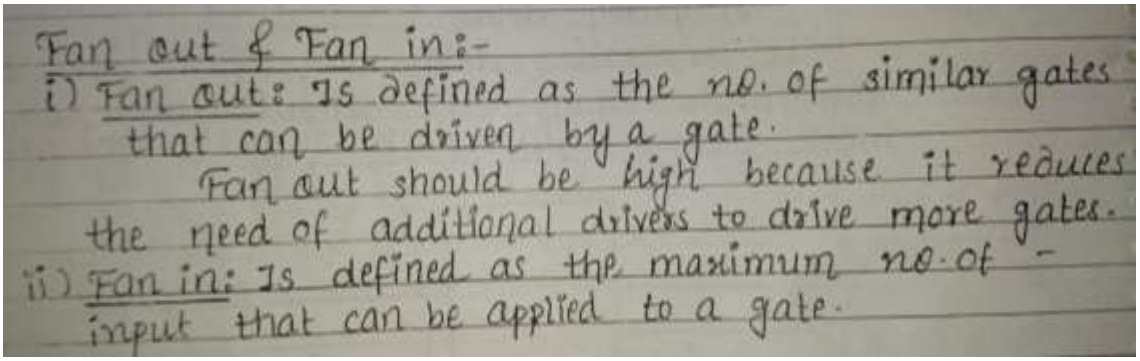
(ii) Fan out

(iii) Propagation delay

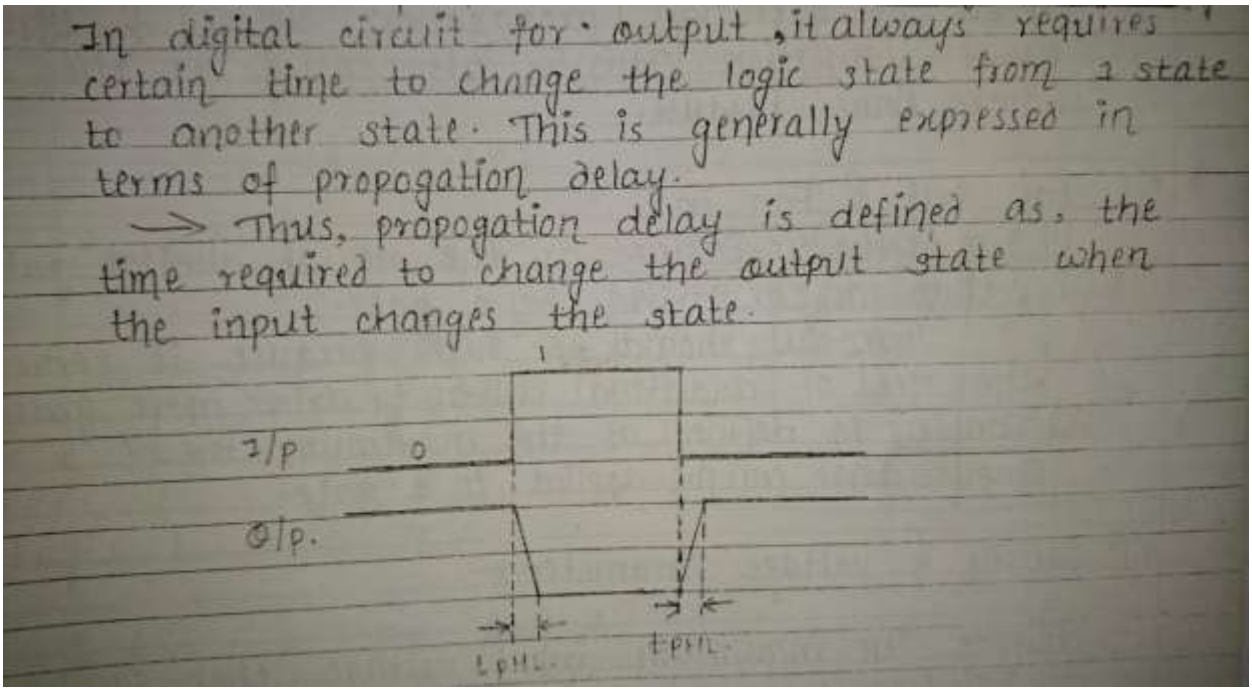
(iv) Power dissipation

Ans:- (Each definition- 1 mks)

Fan in and Fan out-

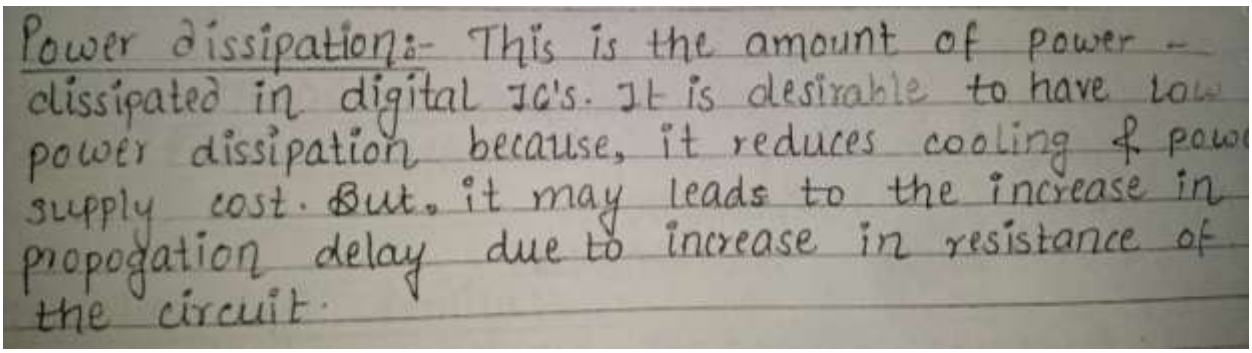

Fan out & Fan in:-
i) Fan out: Is defined as the no. of similar gates that can be driven by a gate.
Fan out should be high because it reduces the need of additional drivers to drive more gates.
ii) Fan in: Is defined as the maximum no. of input that can be applied to a gate.

3) Propagation delay-



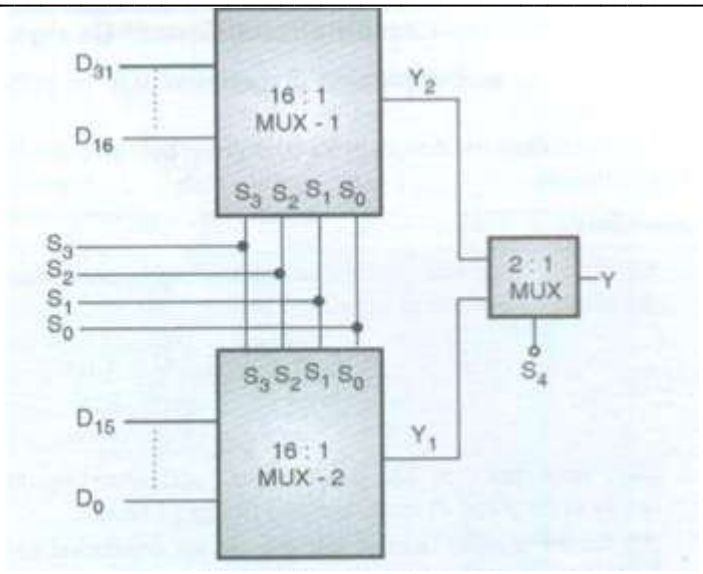
In digital circuit for output, it always requires certain time to change the logic state from 1 state to another state. This is generally expressed in terms of propogation delay.
→ Thus, propogation delay is defined as, the time required to change the output state when the input changes the state.

4) Power dissipation-


Power dissipation:- This is the amount of power dissipated in digital IC's. It is desirable to have low power dissipation because, it reduces cooling & pow supply cost. But, it may leads to the increase in propogation delay due to increase in resistance of the circuit.

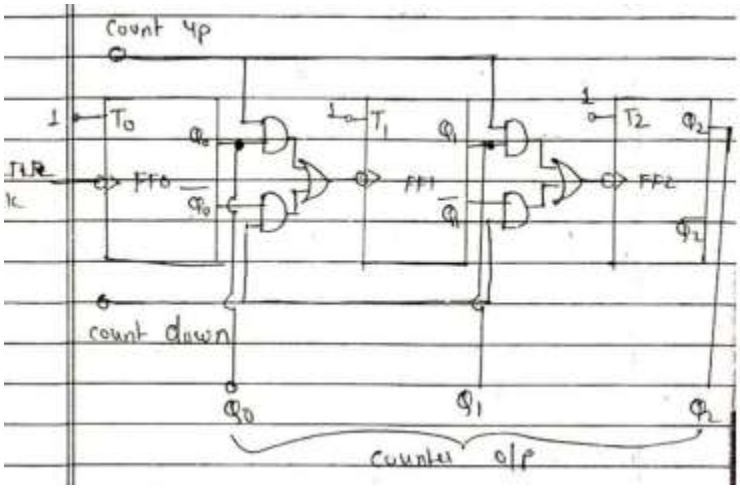
(c) Design 32 : 1 MUX using 16 : 1 MUX.

Ans:- (Proper relevant diagram- 4 mks)



(d) Draw logic diagram for 3 bit up-down counter.

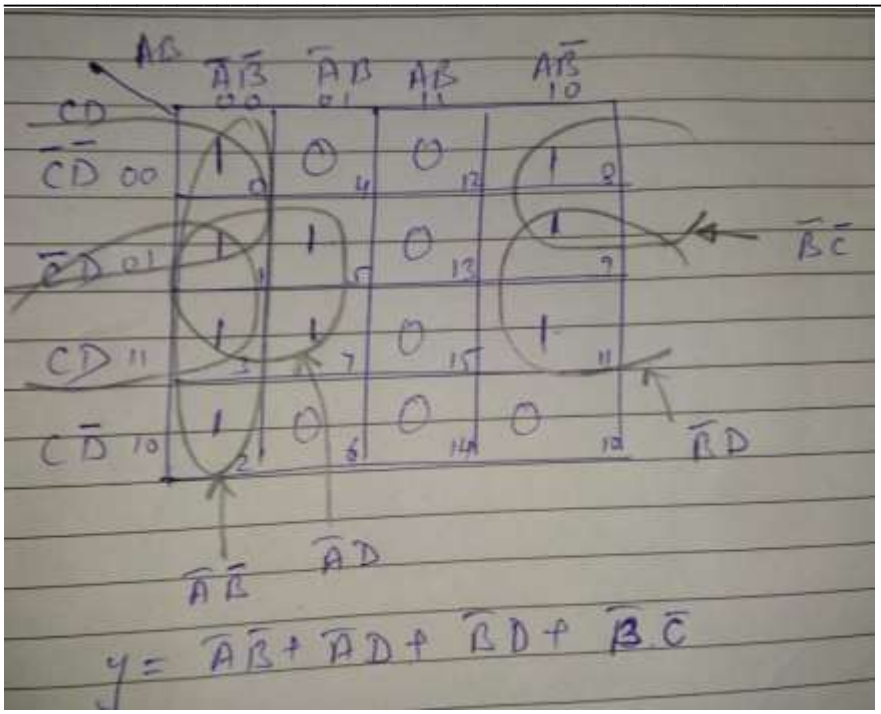
Ans:- (Proper relevant diagram-4 mks)



(e) Simplify given SOP equation using K map

$Y = \Sigma_m (0, 1, 2, 3, 5, 7, 8, 9, 11)$

Ans:- (Proper solution- 4 mks)



(f) Writer advantage (any 3) and disadvantage (any 1) of dual slope ADC.

Ans:- **Advantages – (any three)- 3 mks**

1) high resolution

2) good conversion accuracy

3) conversion time is constant and independent of analog input

4) less sensitive to noise

5) does not require crystal oscillator for stability

6) simple and less expensive

Disadvantages (any one) -1 mks

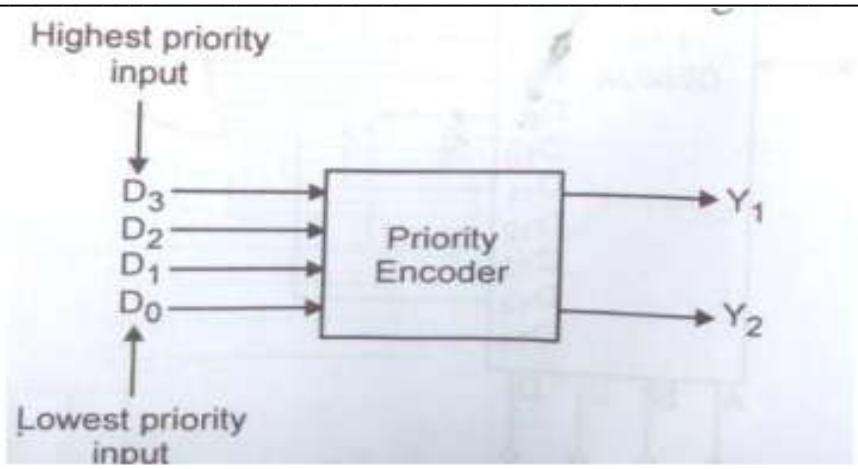
1) Large conversion time

5. Attempt any FOUR : 16

(a) Define priority encoder. Draw the generalized block diagram of priority encoder.

Ans:- (definition- 2 mks, Block diagram-2 mks)

Priority Encoder is a special type of encoder, that responds to just one input in accordance with some priority system, among all those that may be simultaneously high.
Priorities are given to the input lines.
If two or more inputs are 1, at the same time, then input line with highest priority will be considered.



(b) Compare R-2R ladder DAC with weighted resistor DAC (any 4 points)

Ans:- (Comparison on relevant point- 1 mks each)

Sr No.	Parameter	Weighted Resistor	R-2R Ladder Network
1.	Simplicity	Simple	Slightly complicated
2.	Range of resistor values	Wide range is required	Resistors of only two values are required
3.	Number of resistors per bit	One	Two
4.	Ease of expansion	Not easy to expand for more number of bits	Easy to expand

(c) Explain the operation TTL logic NAND gate. Draw the circuit diagram.

Ans:- (Diagram- 2 mks, Truth table – 1 mks, operation- 1 mks)

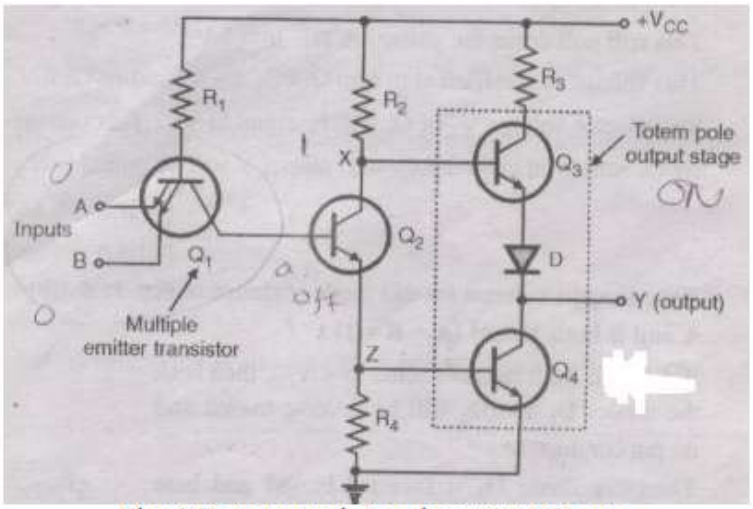


Fig: TTL totem pole two input NAND gate

Truth Table

Input		Output
A	B	Y=A.B
0	0	1
1	0	1
0	1	1
1	1	0

Operation-

1. A and B both LOW (A = B =0):

- If A and B both are connected to ground, then both the B- E junctions of transistors Q1 are forward biased.
- Hence diodes D1 and D2 will conduct to force the voltage at point C to 0.7 V.
- This voltage is insufficient to forward bias base emitter junction of Q2. Hence **Q2 will remain OFF.**
- Therefore its collector voltage Vx rises to Vcc.
- As transistor Q3 is operating in the emitter follower mode, output Y will be pulled up to high voltage. **Therefore, Y =1 (HIGH) …..For A =B= 0 (LOW)**

2. Either A or B LOW (A =0, B=1 or A=1, B=0):

- If any one input (A or B) is connected to ground with the other terminal left open or connected to +Vcc, then the corresponding diode (D1 & D2) will conduct.
- This will pull down the voltage at "C" to 0.7 V.

This voltage is insufficient to turn ON **Q2. So it remains OFF.**
So collector voltage Vx of Q2 will be equal to Vcc, voltage acts as base voltage for Q3.
As Q3 acts as an emitter follower, output Y will be pulled to Vcc.
Y= 1 ---- if A=0 and B=1 -----if A=1 and B=0

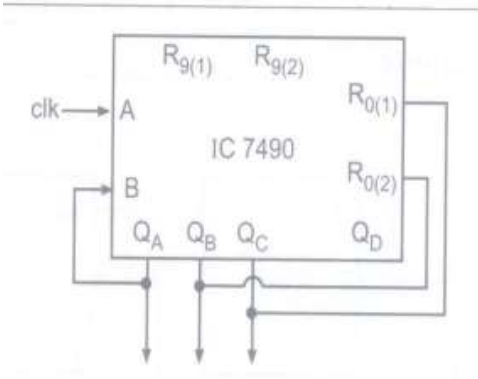
3. A and B =1

- If A and B both are connected to +Vcc, then both the diodes D1 & D2 will be reverse biased and do not conduct.
- Therefore diode D3 is forward biased and base current is supplied to transistor Q2 via R1 and D3.
- As Q2 conducts, the voltage at X will drop down and **Q3 will beOFF,** whereas voltage at Z (across R3) will increase **to turn ON Q4.**
- As Q4 goes into saturation, the output voltage Y will be pulled down to a low voltage, **Y=0.**

(d) Design MOD-6 counter using IC 7490.

Ans:- (Proper diagram- 4 mks)

To reset the counter after counting the first six states from 0 to 5, the counter outputs Q_C and Q_B should be connected to the reset inputs.



Truth table (optional)

State	Q_C	Q_B	Q_A	Output Y
0	0	0	0	1
1	0	0	1	1
2	0	1	0	1
3	0	1	1	1
4	1	0	0	1
5	1	0	1	1
6	0	0	0	0

(e) Compare combinational circuit with sequential circuit (any 4 points)

Ans: (Any four points) 01M each

PARAMETERS	COMBINATIONAL CIRCUIT	SEQUENTIAL CIRCUIT
Definition	The output at any instant of time depends upon the input present at that instant of time.	The output at any instance of time depends upon the present input as well as past input and output.
Need of Memory	No memory element required in the ckt	Memory element required to stored bit
Need of clock	Clock input not necessary	Clock input necessary
Examples	E.g. Adders, Subtractors ,Code converters, comparators etc.	E.g. Flip flop, Shift registers, counters etc,
Applications	Used to simplify Boolean expressions, k-map , Truth table	Used in counters & registers

(f) Compare EPROM and EEPROM (any four points).

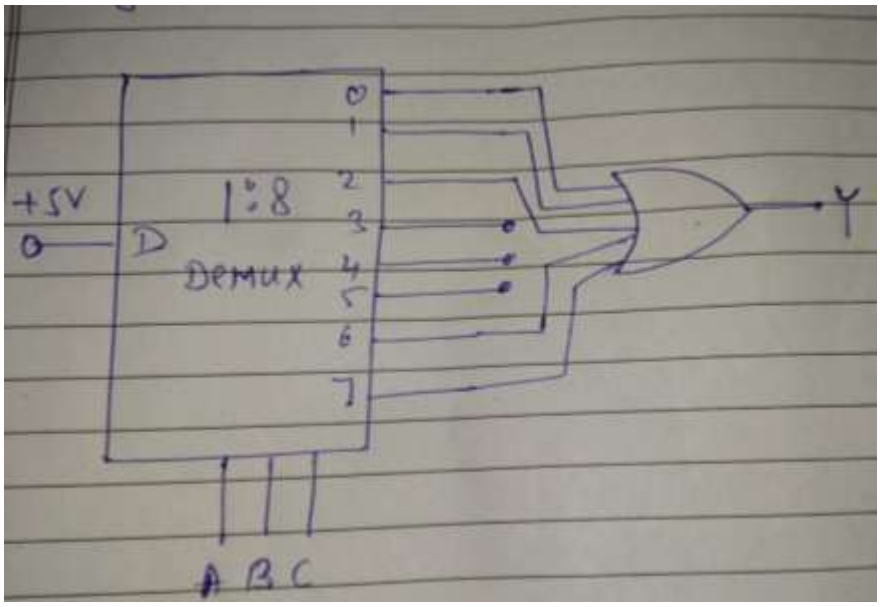
Ans:-(any four relevant comparison- 4 mks)

E^2PROM	EPROM
1. E^2PROM stands for Electrically Erasable Programmable Read Only Memory.	1. EPROM stands for Erasable Programmable Read Only Memory.
2. Can be programmed and erased electrically.	2. Cannot be erased electrically and require UV rays to erase the EPROM.
3. Can be erased in a small time of 10 ms.	3. Requires 20 to 30 min. for erasing the contents.
4. Not required to remove the chip from the circuit for erasing and reprogramming.	4. Chip has to be removed from the circuit for erasing and reprogram-ming.
5. Low density	5. High density
6. Expensive than EPROM.	6. Cheaper than E^2PROM.

6. Attempt any FOUR : 16

(a) Implement $Y = f(A,B,C) = \Sigma_m (0,1,2,6,7)$ using suitable DeMUX& logic gates.

Ans:- (proper relevant diagram- 4 mks)



(b) State the use of preset and clear terminal in a Flip-folp.

Ans: 2 Mks for explanation & 2 Mks for Truth Table.

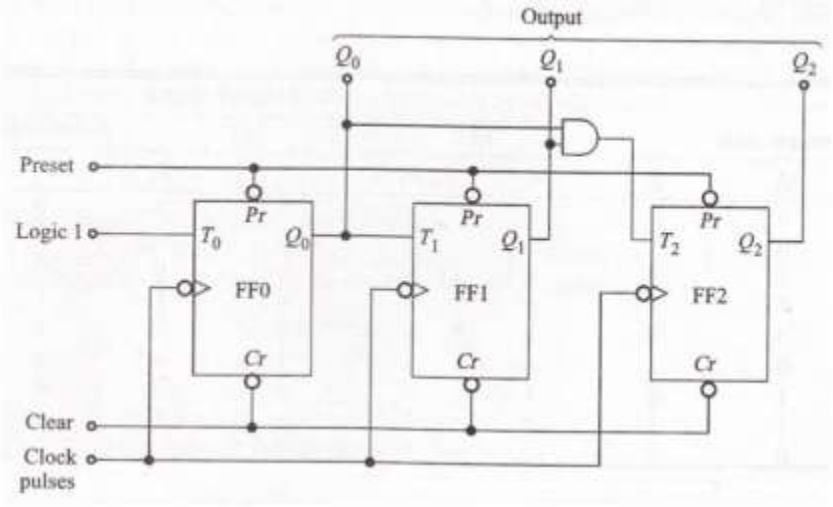
In the Flip-flop when the power is switched ON, the state of the circuit is uncertain.
It may be set (Q=1) or reset (Q=0) state.
In many applications it is desired to initially set or reset the flip-flop i.e. the initial state of flip-flop is to be assigned. This is done by using preset (Pr) & clear (Cr) inputs.
There inputs may be applied at any time between clock pulses & are not in synchronism with the clock.
Truth Table with Preset & Clear I/P.

Input			Output	Operation
CLK	Cr	Pr	Q	preformed
1	1	1	Q_{n+1}	Normal FF
×	0	1	0	FF is reset
×	1	0	1	FF is set

So, the O/P of the flip-flop changes whenever a clock signal is applied, it is necessary to set the output or reset the output i.e. to start with some definite intial state,then two additional inputs Preset & Clear are used.
These inputs sets or resets the flip-flop independent of clock.

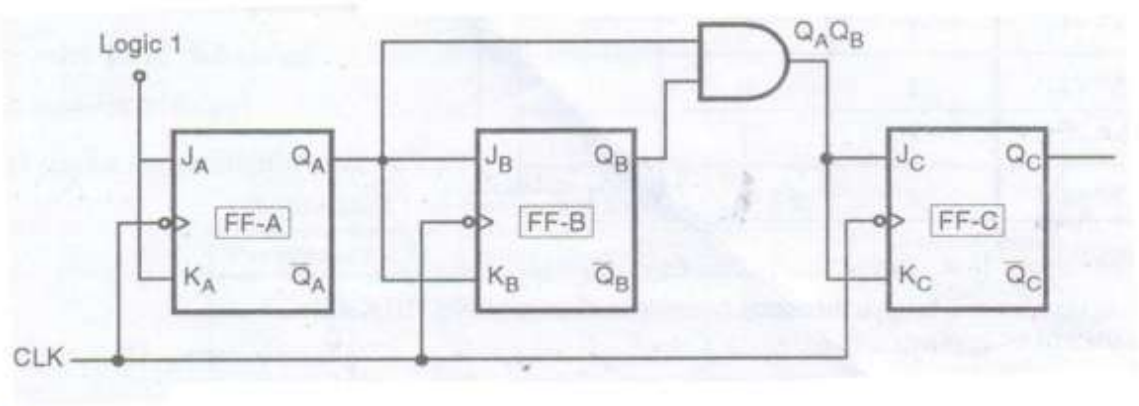
(c) Draw 3 bit synchronous up counter. Write its truth table.

Ans:- (Diagram- 2 mks, truth table – 2 mks)



OR

Diagram-



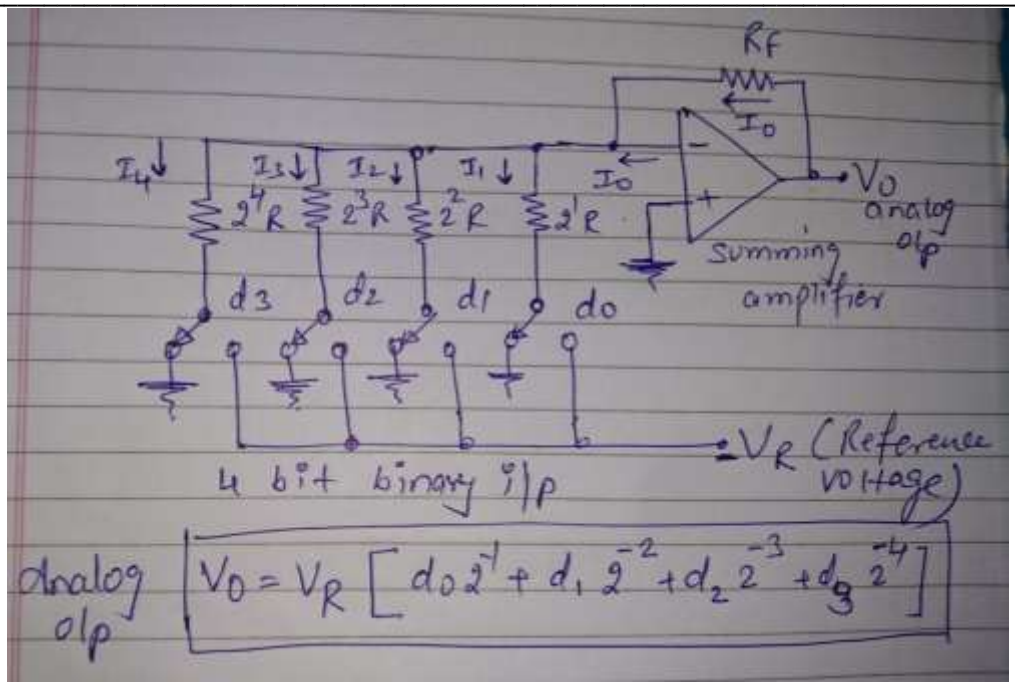
Truth Table-

Clock	Q_C	Q_B	Q_A
0	0	0	0
1st (↓)	0	0	1
2nd (↓)	0	1	0
3rd (↓)	0	1	1
4th (↓)	1	0	0
5th (↓)	1	0	1
6th (↓)	1	1	0
7th (↓)	1	1	1

(d) Draw 4 bit weighted resistor DAC and give expression for output voltage.

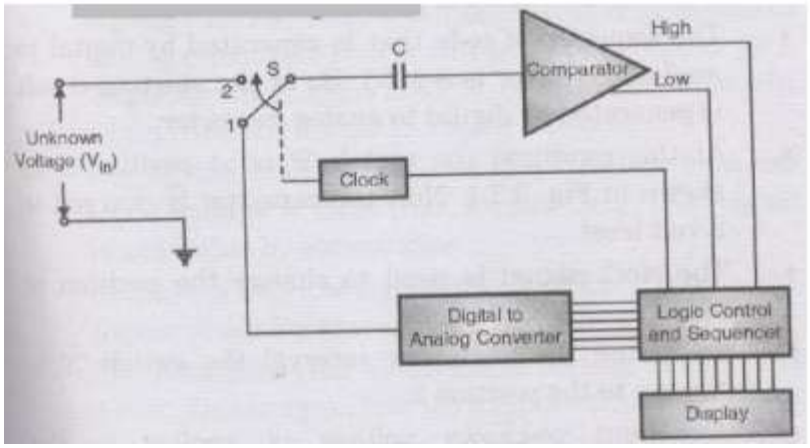
Ans:-(diagram-2 mks, o/p equation- 2 mks)

Consider 4 digital inputs d0,d1,d2 and d3 as shown with analog o/p Vo-



(e) Describe successive approximation ADC with neat diagram.

Ans:- (diagram- 2 mks, explanation- 2 mks)



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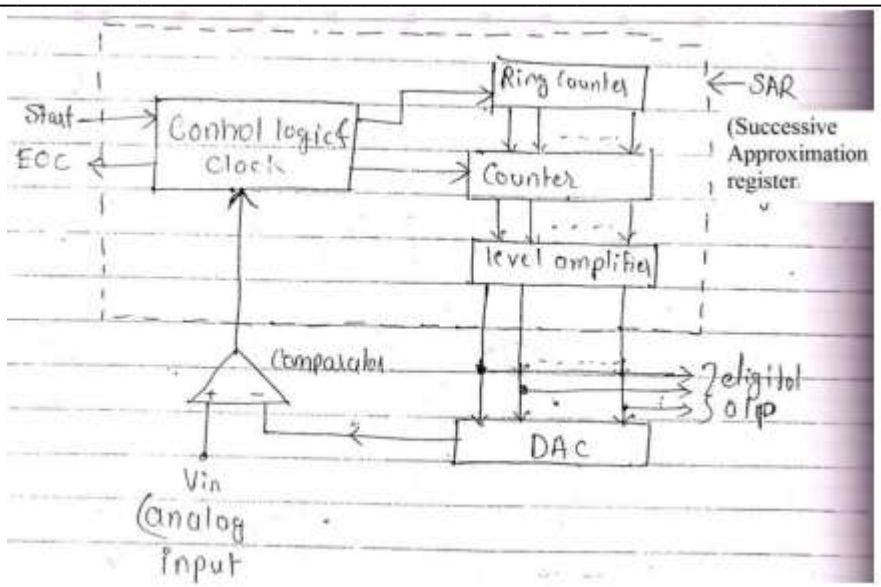

DAC = Digital-to-Analog converterEOC = end of conversion
SAR = successive approximation register
S/H = sample and hold circuit
V_{in} = input voltage
V_{ref} = reference voltage

The successive approximation Analog to digital converter circuit typically consists of four chief sub circuits:

1. A sample and hold circuit to acquire the input voltage (V_{in}).
2. An analog voltage comparator that compares V_{in} to the output of the internal DAC and outputs the result of the comparison to the successive approximation register(SAR).
3. A successive approximation register sub circuit designed to supply an approximate digital code of V_{in} to the internal DAC.
4. An internal reference DAC that supplies the comparator with an analog voltage equivalent of the digital code output of the SAR for comparison with V_{in}.

The successive approximation register is initialized so that the most significant bit (MSB) is equal to a digital 1. This code is fed into the DAC, which then supplies the analog equivalent of this digital code ($V_{ref}/2$) into the comparator circuit for comparison with the sampled input voltage. If this analog voltage exceeds V_{in} the comparator causes the SAR to reset this bit; otherwise, the bit is left a 1. Then the next bit is set to 1 and the same test is done, continuing

this binary search until every bit in the SAR has been tested. The resulting code is the digital approximation of the sampled input voltage and is finally output by the DAC at the end of the conversion (EOC).

(f) Describe the operation of 1 dig it BCD adder using IC 7483.

Ans:- 3 marks diagram 1 mark explanation

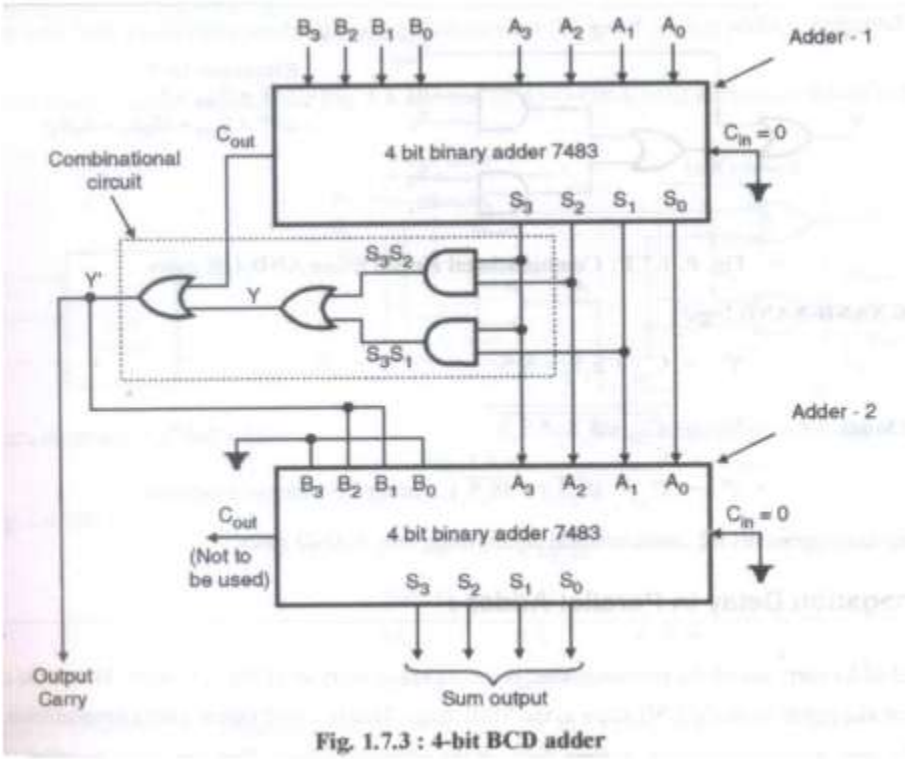

Fig. 1.7.3 : 4-bit BCD adder

A BCD adder adds two BCD digits and produces a BCD digit.
The two given BCD numbers are to be added using the rules of binary addition.
If sum is less than or equal to 9 and carry=0 then no correction is necessary.The sum is correct and in the true BCD form.
But if sum is invalid BCD or carry=1 then the result is wrong and needs correction.
The wrong result can be corrected by adding six(0110) to it.