SUMMER – 13 EXAMINATION

Subject Code: **12069** **Model Answer**

Important Instructions to examiners:

1) The answers should be examined by key words and not as word-to-word as given in the model answer scheme.
2) The model answer and the answer written by candidate may vary but the examiner may try to assess the understanding level of the candidate.
3) The language errors such as grammatical, spelling errors should not be given more Importance (Not applicable for subject English and Communication Skills).
4) While assessing figures, examiner may give credit for principal components indicated in the figure. The figures drawn by candidate and model answer may vary. The examiner may give credit for any equivalent figure drawn.
5) Credits may be given step wise for numerical problems. In some cases, the assumed constant Values may vary and there may be some difference in the candidate's answers and model answer.
6) In case of some questions credit may be given by judgement on part of examiner of relevant answer based on candidate's understanding.
7) For programming language papers, credit may be given to any other program based on equivalent concept.

1) Attempt any ten: **(10X2=20Marks)**

a) Find the Gray code of $(46)_{10}$.

Ans a.

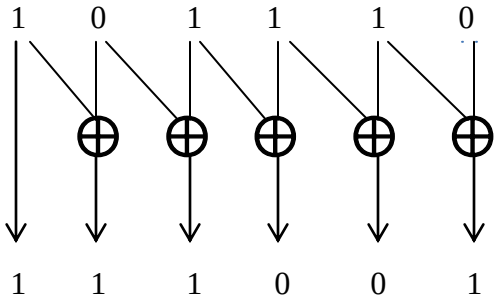
Step 1:- Convert given decimal no. into binary
$(46)_{10} = (1\ 0\ 1\ 1\ 1\ 0)_2$ **----1 Mark**

Step 2:- Write MSB bit as it is and EX-OR each binary bit with next bit.

Step 3:- Continue Step 2 till we reach LSB.

Binary no. MSB LSB

B_5	B_4	B_3	B_2	B_1	B_0
1	0	1	1	1	0



1	1	1	0	0	1

$(46)_{10} = (1\ 1\ 1\ 0\ 0\ 1)_{\text{Gray code}}$ **-------1 Mark**

b) Write AND laws in Boolean algebra.

Ans b. **Each law – ½ Mark**

The AND laws are as follows:

1. A · 0 = 0 i.e. ANDing with a 0, always result in 0 output.
2. A · 1 = A i.e. ANDing of A with a 1, result in 0 output.
3. A · A = A i.e. ANDing of an input with itself will produce the same output.
4. A · $\overline{A}$ = 0 i.e. ANDing of an output with its complement results in a 0 output.

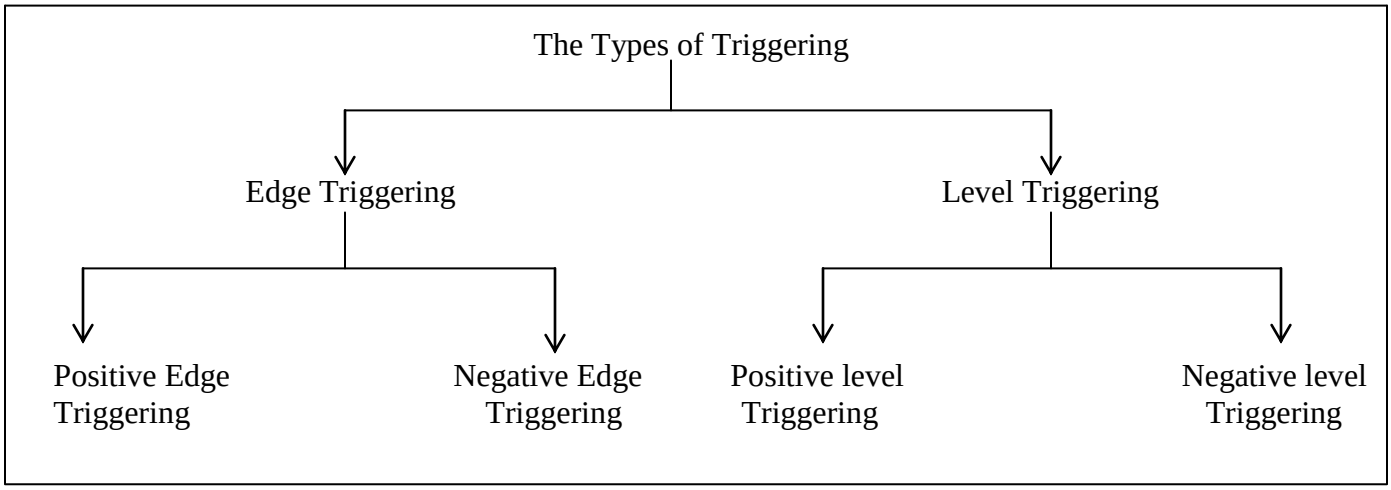
c) State the necessity of multiplexes.

Ans c. **Necessity of multiplexer any two points – 2Marks**

- In most of the electronic systems, the digital data is available on more than one lines. It is necessary to route this data over a single line.
- Under such circumstances we require a circuit which selects one of the many inputs at a time.
- This circuit is nothing else but a multiplexer. Which has many inputs, one output and some select inputs.
- Multiplexer improves the reliability of the digital system because it reduces the number of external wired connections

d) What are the types of triggering?

Ans d. **Types of triggering – 2Marks**



e) Define Fan- out and power dissipation with respect to logic families.

Ans e. **Definition Fan- out -1Mark & Definition of Power Dissipation- 1Mark**

Fan- out:

- Fan- out is defined as the maximum number of inputs of the same IC family that a gate can drive without falling outside the specified output voltage limits.
- Higher the fan out higher the current supplying capacity of a gate.
- For example, a fan out of 5 indicate that the gate can drive (supply current to) at the most 5 inputs of the same IC family.

Power dissipation:

- As a result of applied voltage and currents flowing through the logic ICs, some power will be dissipated in it, in the form of heat.
- This power is in milliwatts. The power dissipation taking place in the logic IC in order to protect the IC against damage due to excessive temperature, to reduce the loading on power supplies etc.
- The product of power dissipation and propagation time is always constant.
- Therefore, reduced power dissipation may lead to increase in propagation delay.
- The power drawn by an IC from the power supply is given by, $P= V_{cc} X I_{cc}$
  Where I_{cc} is the current drawn from the power supply.

f) Write the truth table for full subtractor.

Ans f. **Correct truth table- 2 Marks**

Truth Table for full subtractor.

Inputs			**Outputs**	
A (Minuend)	**B (Subtrahend)**	**Previous Borrow C_{in-1}**	**Difference $A \oplus B \oplus C_{in-1}$**	**Borrow (C)**
0	**0**	**0**	**0**	**0**
0	**0**	**1**	**1**	**1**
0	**1**	**0**	**1**	**1**
0	**1**	**1**	**0**	**1**
1	**0**	**0**	**1**	**0**
1	**0**	**1**	**0**	**0**
1	**1**	**0**	**0**	**0**
1	**1**	**1**	**1**	**1**

Fig: Truth Table for full subtractor

g)How J- K flip- flop can be converted into D- flip- flop. Draw its symbol.

Ans g. **J- K flip- flop can be converted into D- flip- flop – 1Mark.**
Symbol – 1 Mark

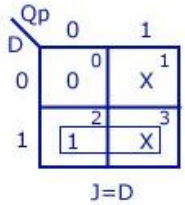
D is the external input and J and K are the actual inputs of the flip flop. D and Qp make four combinations. J and K are expressed in terms of D and Qp. The four combination conversion table, the K-maps for J and K in terms of D and Qp, and the logic diagram showing the conversion from JK to D are given below.

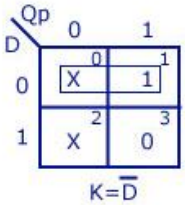
J-K Flip Flop to D Flip Flop

Conversion Table

D Input	Outputs Qp	Qp+1	J-K Inputs J	K
0	0	0	0	X
0	1	0	X	1
1	0	1	1	X
1	1	0	X	0

K-maps





Logic Diagram

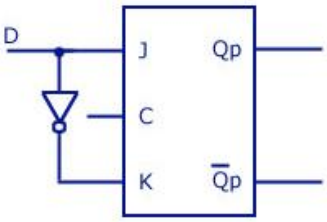


Fig: Symbol

h) Find 2's complement of (i) $(1\ 0\ 1\ 0\ 1\ 1)_2$ (ii) $(0\ 1\ 1\ 1\ 0\ 1)_2$

Ans h. (i)**1's complement of $(1\ 0\ 1\ 0\ 1\ 1)_2$ – 1/2Mark; 2's complement of $(1\ 0\ 1\ 0\ 1\ 1)_2$ – 1/2Mark**

(ii)1's complement of $(0\ 1\ 1\ 1\ 0\ 1)_2$ – 1/2Mark; 2's complement of (ii) $(0\ 1\ 1\ 1\ 0\ 1)_2$ – 1/2Mark

a) $(1\ 0\ 1\ 0\ 1\ 1)_2$
2's complement of $(1\ 0\ 1\ 0\ 1\ 1)_2$ = 1's complement of $(1\ 0\ 1\ 0\ 1\ 1)_2$ + 1

1's complement of $(1\ 0\ 1\ 0\ 1\ 1)_2$ is obtained by replacing '1's by 0's and replacing 0's by 1's

Therefore, **1's complement of $(1\ 0\ 1\ 0\ 1\ 1)_2 = (0\ 1\ 01\ 0\ 0)_2$**
Therefore, **2's complement of $(1\ 0\ 1\ 0\ 1\ 1)_2 = 0\ 1\ 0\ 1\ 0\ 0 + 1$**

Therefore, 2's complement of $(1\ 0\ 1\ 0\ 1\ 1)_2 = (0\ 1\ 0\ 1\ 0\ 1)_2$

ii) $(0\ 1\ 1\ 1\ 0\ 1)_2$
2's complement of $(0\ 1\ 1\ 1\ 0\ 1)_2$ = 1's complement of $(0\ 1\ 1\ 1\ 0\ 1)_2$ + 1

1's complement of $(1\ 0\ 1\ 0\ 1\ 1)_2$ is obtained by replacing '1's by 0's and replacing 0's by 1's

Therefore, **1's complement of $(0\ 1\ 1\ 1\ 0\ 1)_2 = (1\ 0\ 0\ 0\ 1\ 0)_2$**
Therefore, **2's complement of $(0\ 1\ 1\ 1\ 01)_2 = 1\ 0\ 0\ 0\ 1\ 0 + 1$**

Therefore, 2's complement of $(0\ 1\ 1\ 1\ 0\ 1)_2 = (1\ 0\ 0\ 0\ 1\ 1)_2$

i)Draw the logic circuit diagram of 1- bit memory cell.

Ans i. **Correct Logic circuit diagram – 2 Marks**

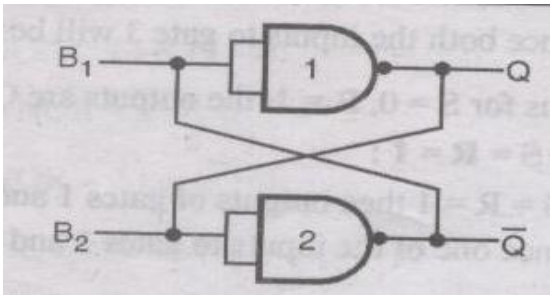


Fig: 1 bit memory cell using NAND gates.

j) Comment on the speed of ECL logic family.

Ans j. **Any two points – 2marks**

- Transistor operate in either cut off or active regions. They are not allowed to operate in saturation.
- They can switch at very fast speeds. In fact ECL is the fastest logic family. Therefore it is preferred in all the high speeds applications.
- Typically the propagation delay is 1 ns per gate.
- It is fastest logic family.
- Excellent speed power products.
- Its high speed generates voltage and current transients.

k) Draw the circuit of CMOS Inverter.

Ans k. **correct circuit of CMOS Inverter – 2Marks**

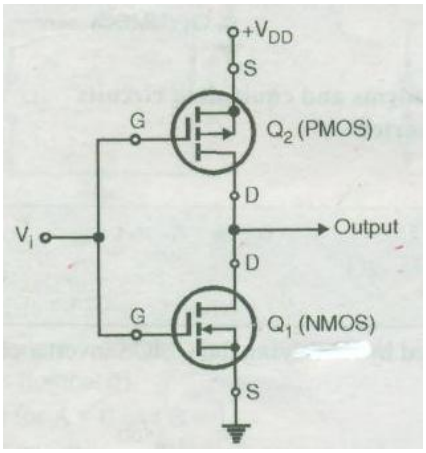


Fig: CMOS Inverter

l) State the rules of BCD addition.

Ans l**. Any Two Rules of BCD addition – 2Marks**

1) Sum equal to or less than 9 with carry 0; then do not add $(6)_{10}$ or BCD (0 1 1 0) to the sum.

2) Sum greater than 9 but carry =0 (invalid BCD no.) then add $(6)_{10}$ or BCD (0 1 1 0) to the sum.

3) Sum less than or equal to 9 but carry= 1; then add $(6)_{10}$ or BCD (0 1 1 0) to the sum.

2. Attempt **any four:** **(4X4= 16 Marks)**

a) Write the symbol, Truth –table and logical expression of NOR gate.

Ans a. **Symbol -- 1Mark; Truth Table -- 2Marks; Logical expression-- 1Mark**

- **Symbol of the 2 input NOR gate.**

- **Truth table**

Input		**Output**
A	**B**	**$Q = \overline{A+B}$**
0	0	1
0	1	0
1	0	0
1	1	0

- **Logical Output Equation:** $Q = \overline{A+B}$

b) Perform binary multiplication of $(11001)_2$ X $(10011)_2$

Ans b. **Correct binary multiplication—4marks**

					1	1	0	0	1
				X					
					1	0	0	1	1
					1	1	0	0	1
				1	1	0	0	1	0
			0	0	0	0	0	0	0
			0	0	0	0	0	0	0
1		1	0	0	1	0	0	0	0

		1	1					
1	1	1	0	1	1	0	1	1

c) Write the expression of full- adder. Write it truth- table. Draw it logical diagram.

Ans c. **Expression of Carry —1/2 Mark, Expression of Sum —1/2Mark**
Truth Table —1 1/2Marks, Logical Diagram --- 1 1/2Marks

Expression of full- adder:

Carry (C_o) = $AB + AC_{in} + BC_{in}$
Sum (S) = $A \oplus B \oplus C_{in}$

Truth Table:

Inputs			Outputs	
A	B	C_{in}	S	C_o
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Fig: Truth Table for full adder

Logic Diagram:

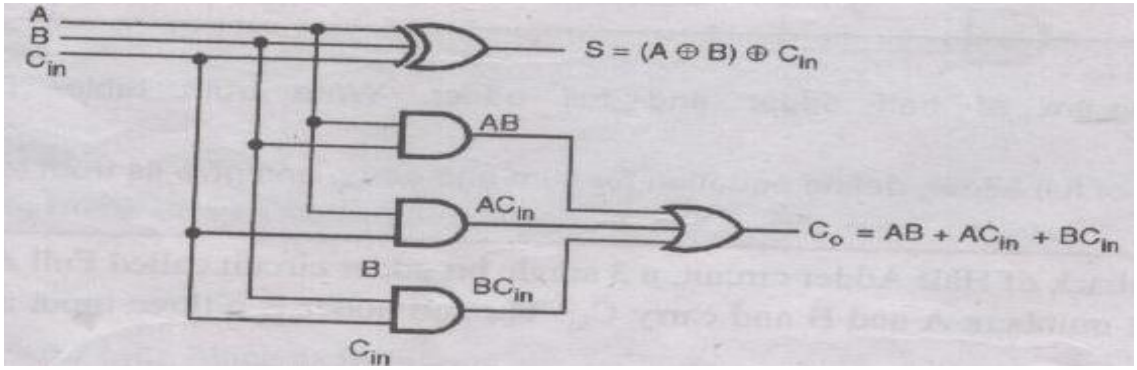
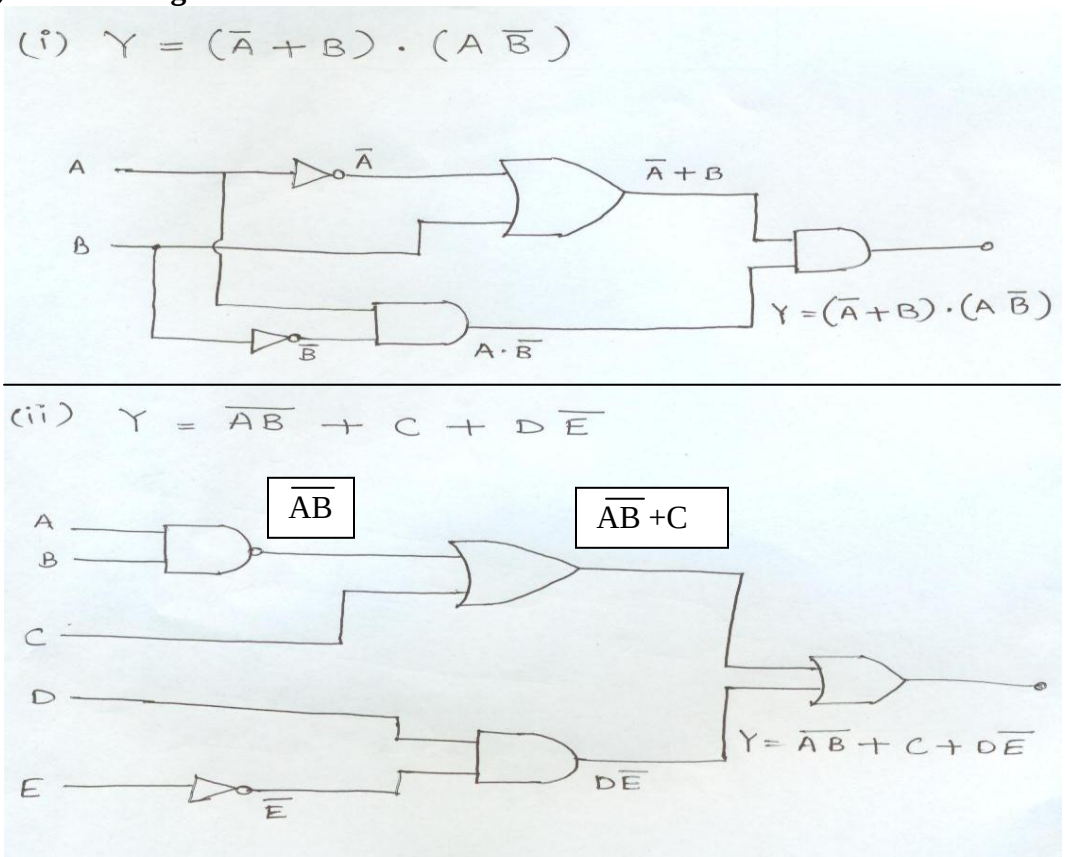


Fig: Logical Diagram for full adder

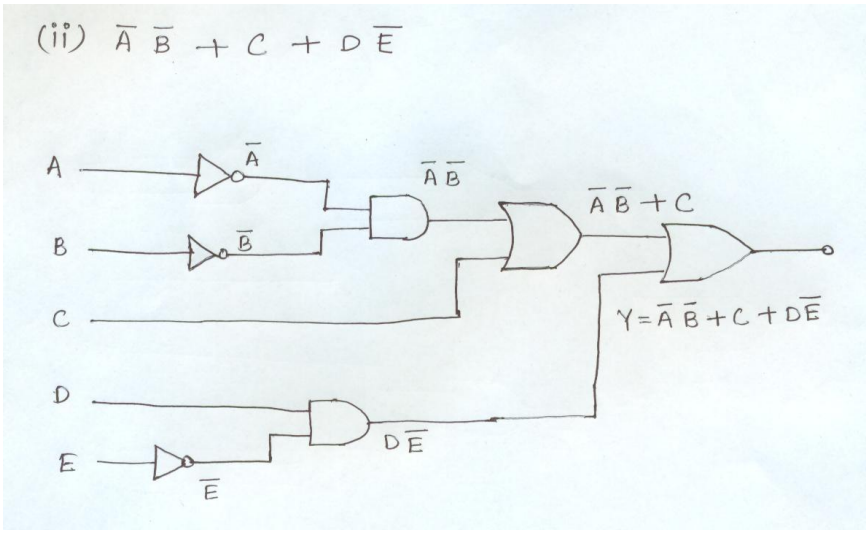
d) Realize the following Boolean expression using basic gates.

i) $y = (\overline{A} + B).\ (A\overline{B})$ ii) $y = \overline{A}\ \overline{B} + C + \overline{D}E$

Ans d. **(i) Correct diagram—2marks.**
(ii) Correct diagram – 2 marks.



OR



e) Explain the working of BCD to 7 segment decoder with truth table and circuit diagram

Ans e. **Weightage is to be given for common anode or common cathode display**

Truth table 2 Marks; Circuit Diagram—2 Marks

For common anode, the output of the converter should be "0" if a display segment is to be turned on.
For common anode, the output of the converter should be "1" if a display segment is to be turned off

Decimal	**Inputs**				**Outputs**						
	B_3	B_2	B_1	B_0	a	b	c	d	e	f	g
0	0	0	0	0	0	0	0	0	0	0	**1**
1	0	0	0	1	**1**	0	0	**1**	**1**	**1**	**1**
2	0	0	1	0	0	0	**1**	0	0	1	0
3	0	0	1	1	0	0	0	0	**1**	**1**	0
4	0	1	0	0	**1**	0	0	**1**	**1**	0	0
5	0	1	0	1	0	**1**	0	0	**1**	0	0
6	0	1	1	0	0	**1**	0	0	0	0	0
7	0	1	1	1	0	0	0	**1**	**1**	**1**	**1**
8	1	0	0	0	0	0	0	0	0	0	0
9	1	0	0	1	0	0	0	0	**1**	0	0

Fig: Truth table for BCD to 7 segment decoder

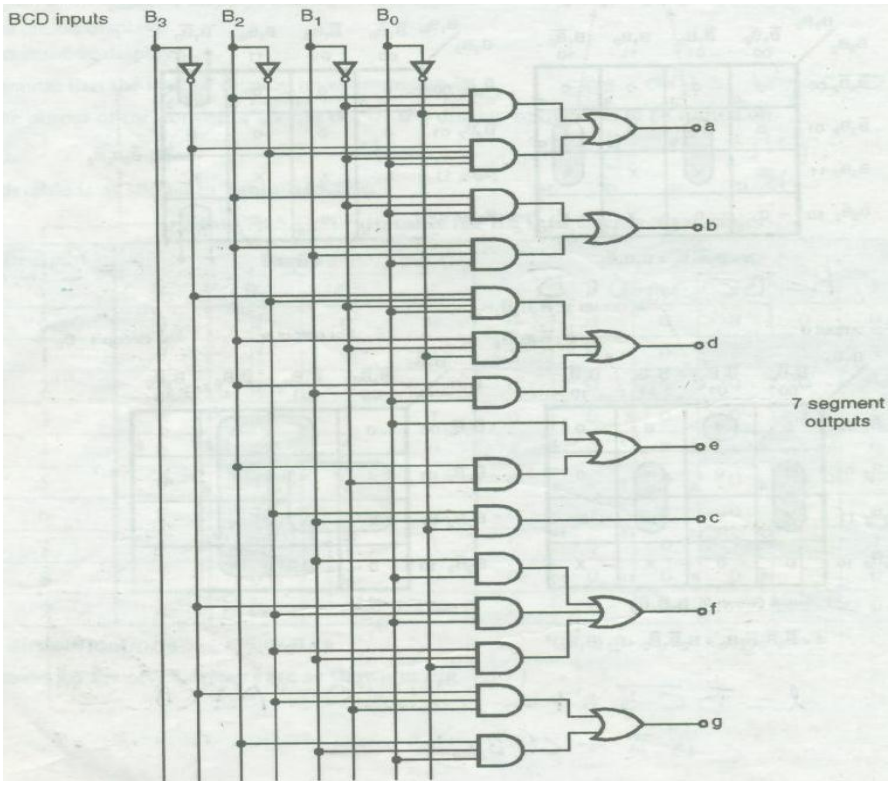


Fig: BCD to seven segment decoder.

OR

For common cathode, the output of the converter should be "1" if a display segment is to be turned off.
For common cathode, the output of the converter should be "0" if a display segment is to be turned on.

Decimal	**Inputs**				**Outputs**						
	B_3	B_2	B_1	B_0	a	b	c	d	e	f	g
0	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	1	0	1	1	0	0	0	0
2	0	0	1	0	1	1	0	1	1	0	1
3	0	0	1	1	1	1	1	1	0	0	1
4	0	1	0	0	0	1	1	0	0	1	1
5	0	1	0	1	1	0	1	1	0	1	1
6	0	1	1	0	1	0	1	1	1	1	1
7	0	1	1	1	1	1	1	0	0	0	0
8	1	0	0	0	1	1	1	1	1	1	1
9	1	0	0	1	1	1	1	1	0	1	1

Fig: Truth table for BCD to seven segment decoder with a common cathode display.

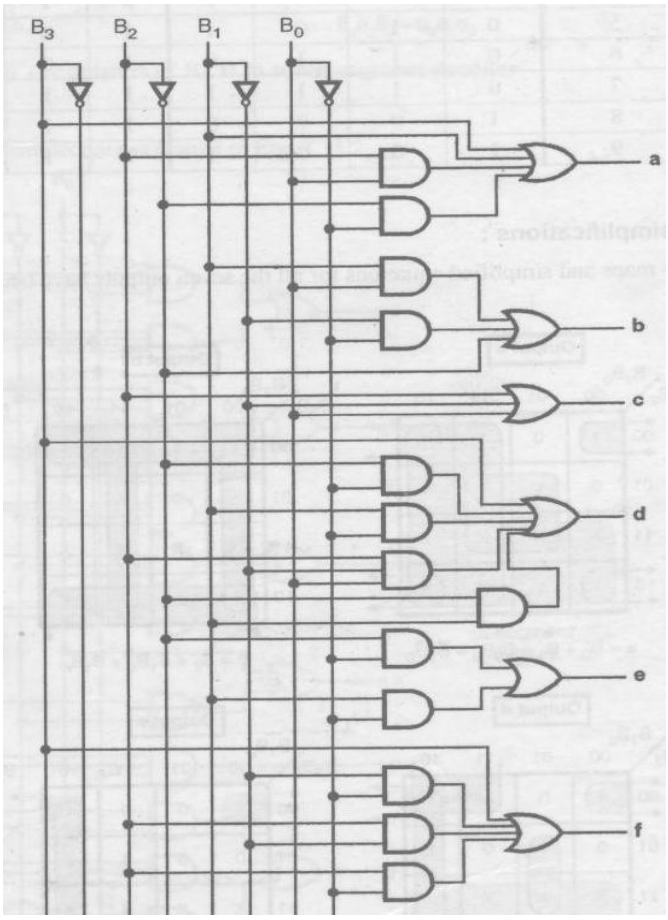


Fig: BCD to seven segment decoder for a common cathode type display.

f) Add $(412)_{10}$ and $(932)_{10}$ in BCD.

Ans f.

$(412)_{10}$ = (0100 0001 0010) BCD ----- **1 Mark**

$(932)_{10}$ = (1001 0011 0010) BCD ----- **1 Mark**

$(4\ \ 1\ \ 2)_{10}$

$+\ (9\ \ 3\ \ 2)_{10}$

$(1\ \ 3\ \ 4\ \ 4)_{10}$

(0 1 0 0 0 0 0 1 0 0 1 0) BCD

\+ (1 0 0 1 0 0 1 1 0 0 1 0) BCD

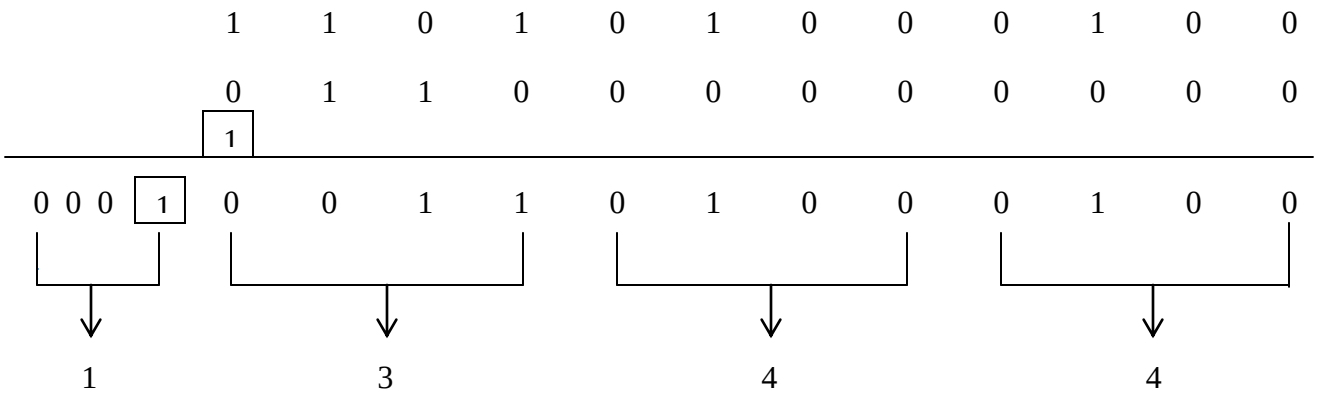
1 1 1

1 1 0 1 0 1 0 0 0 1 0 0

Invalid BCD Valid BCD Valid BCD

(Therefore, Add $(6)_{10}$ i.e. BCD 0 1 1 0)

----- **1Mark**



----- **1Mark**

Ans: $(4\ 1\ 2)_{10}$ + $(9\ 3\ 2)_{10}$ = $(1\ 3\ 4\ 4)_{10}$

= (0 0 0 1 0 0 1 1 0 1 0 0 0 1 0 0)$_{BCD}$

3. Attempt any four: **(4×4=16Marks)**

a) Convert the following expression into standard SOP form.

a. y =AB + AC+ $\overline{B}$C

b. y=X+X$\overline{Y}$+$\overline{XY}$

a) Y= AB+AC+$\overline{B}$C

= AB(C+$\overline{C}$) +AC(B+ $\overline{B}$) + $\overline{B}$ C(A+$\bar{A}$) **-- 1 Mark**

= ABC+ AB $\overline{C}$+ABC+A $\overline{B}$ C+A $\overline{B}$ C+ $\overline{A}$ $\overline{B}$ + C

= ABC+A $\overline{B}$ C+AB$\overline{C}$ + $\overline{A}$ $\overline{B}$ C **-- 1 Mark**

b) Y= X+X$\overline{Y}$+$\overline{X}$ $\overline{Y}$

= X(Y+$\overline{Y}$) + X $\overline{Y}$+ $\overline{X}$ $\overline{Y}$ **--1 Mark**

$= XY + X\overline{Y} + X\overline{Y} + \overline{X}\ Y$

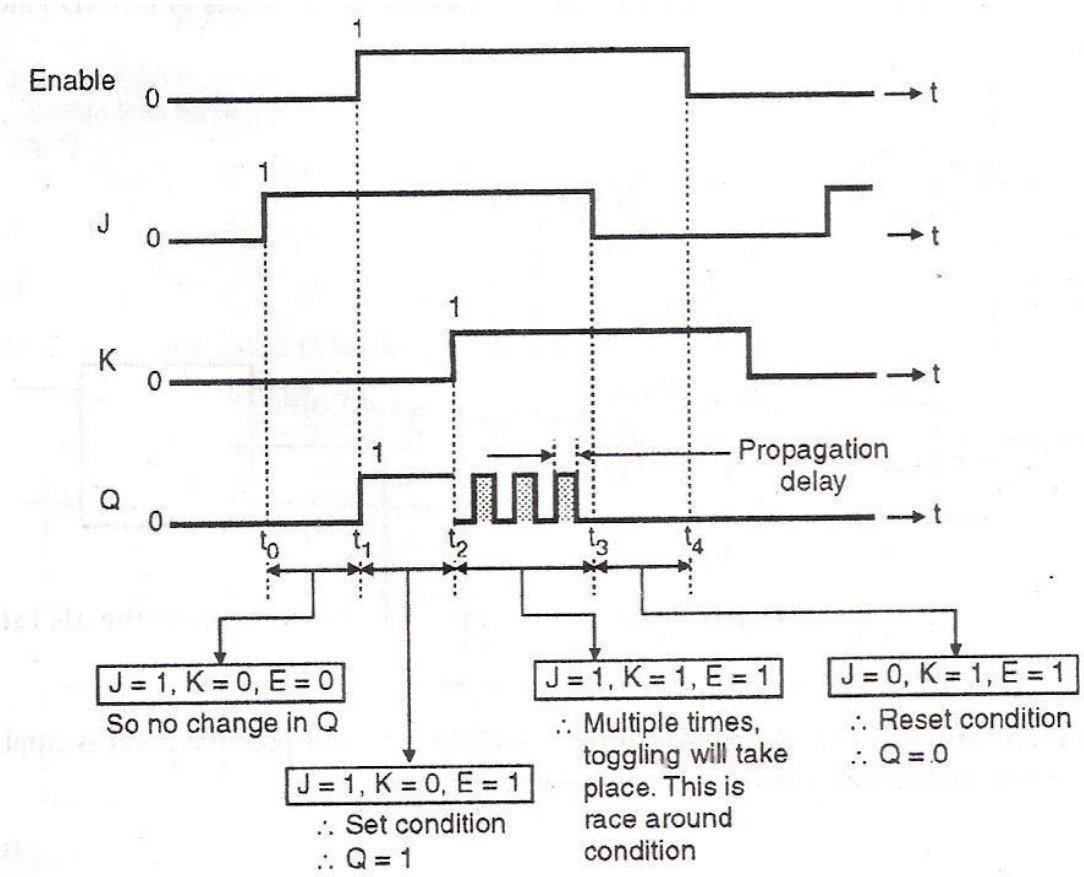
$= XY + X\overline{Y} + \overline{X}\ \overline{Y}$ **-- 1 Mark**

b) Explain the race-around condition in J-K flip-flop. How it can be avoided?

Ans b. **Diagram ----2 Marks**

Explanation ----2 Marks

Race around condition occurs in J K Flip-flop only when J=K=1 and clock/enable is high (logic 1) as shown below



Explanation:-

- In JK Flip-flop when J=K=1 and when clock goes high, output should toggle (change to opposite state), but due to multiple feedback output changes/toggles many times till the clock/enable is high.
- Thus toggling takes place more than once, called as racing or race around condition. Thus to avoid RAC following methods can be used-

1. Design the clock with time less than toggling time (this method is not economical)

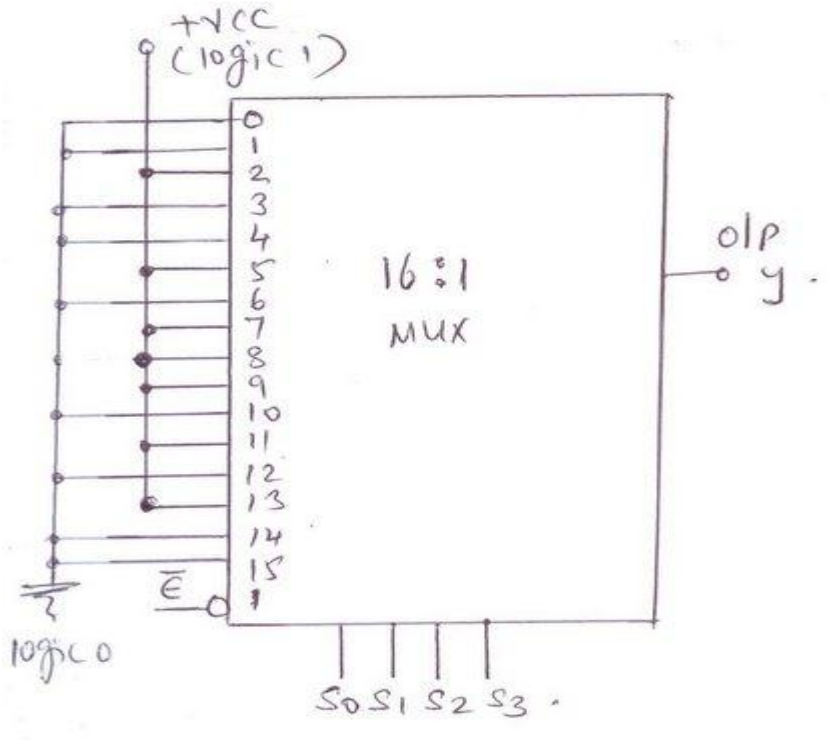
2. Use edge triggering.

3 Use Master Slave J-K flip flop.

c) Implement the following expression using multiplexer.

Ans c. Y=f(A,B,C,D) = ∑m(2,5,7,8,9,11,13)

Any correct implementation—4 Marks.



d) Identify the following circuit as combinational circuit or sequential circuit.

Ans d**. For each correct answer --- 1Mark**

i) 3-bit ring counter --Sequential circuit

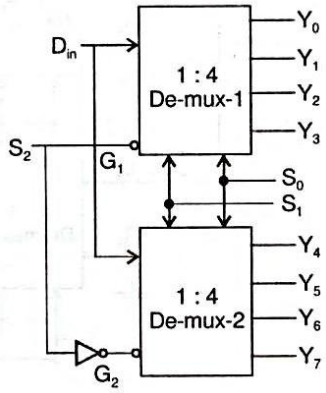
ii) Clocked J-K f/f –Sequential circuit

iii) Full-adder—Combinational circuit

iv) 4:1 MUX—Combinational circuit

e) Design 1:8 demultiplexers using 1:4 demultiplexers.

Ans e. **Logic diagram ---2 Marks**
Truth table ---2 Marks



Truth Table

Inputs			Outputs								
S_2	S_1	S_0	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7	
0	0	0	1	0	0	0	0	0	0	0	
0	0	1	0	1	0	0	0	0	0	0	$S_2 = 0$ 1^{st} Demultiplexer Selected
0	1	0	0	0	1	0	0	0	0	0	
0	1	1	0	0	0	1	0	0	0	0	
1	0	0	0	0	0	0	1	0	0	0	$S_2 = 1$ 2^{nd} Demultiplexer Selected
1	0	1	0	0	0	0	0	1	0	0	
1	1	0	0	0	0	0	0	0	1	0	
1	1	1	0	0	0	0	0	0	0	1	

f) Simplify the following SOP using K-map.

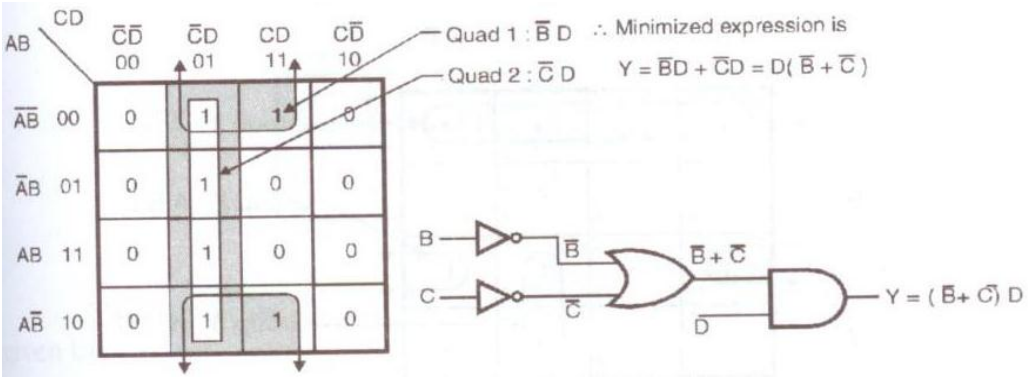
Y = f(A,B,C,D)=∑m(1,3,5,9,11,13).

Ans f **K map --- 2Marks**
Proper Answer --- 2Marks

The given expressions can be expressed in terms of minterms as,

$Y=m_1+m_3+m_5+m_9+m_{11}+m_{13}$

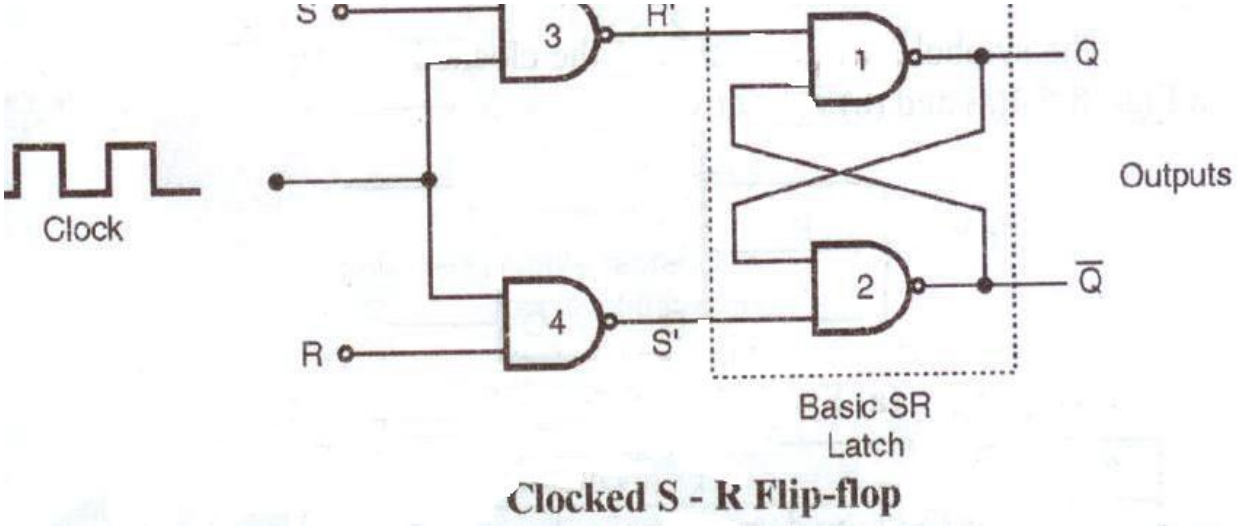
The corresponding K-map is shown in the figure:



4. Attempt any four: **(4×4=16 Marks)**

a) Explain clocked S-R flip-flop with logical diagram and truth-table.

Ans a. **Logical diagram --- 2 marks**
Truth table --1 mark; explanation -- 1 mark



Clocked S - R Flip-flop

The circuit will operate as an SR flip flop if clock = 1 but there is no change in the outputs if clock = 0.

Operation:

Case 1: S=X, R=X, clock =0

Since clock=0, the outputs of NAND gates 3 and 4 will be forced to be 1 irrespective of the values of S and R.

That means R'=S'=1. These are the inputs of the SR latch.

Hence the outputs of basic SR F/F i.e. Q and will not change. Thus if clock = 0, then there is no change in the output of the clocked SR flip-flop.

Case 2: S=R=0: No change

If S=R=0 then the outputs of NAND gates 3 and 4 are forced to become 1.

Hence R and S' both will be equal to 1. Since S' and R' are the inputs of the basic S-R Flip-flop using NAND gates there will be no change in the state of outputs.

Case 3: S=0, R=1, clock=1

Since S=0, output of NAND = 3 i.e. R' = 1. And as R=1 and E=1, the output of NAND=4 i.e. S'=0.

Hence $Q_{n+1}=0$ and $\overline{Q}_{n+1}=1$. This is the reset condition.

Case 4: S=1, R=0, clock=1

Output of NAND 3 i.e. R'=0 and output of NAND 4 i.e. S'=1.

Hence output of SR flip-flop is $Q_{n+1}=1$ and $\overline{Q}_{n+1}=0$.

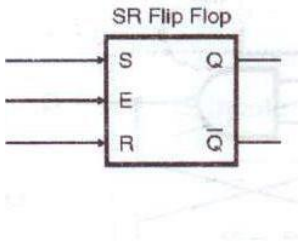
This is the set condition.

Case 5: S=1, R=0, clock=1

As S=1, R=1 and E=1, the output of NAND gates 3 and 4 both are 0, i.e. S'=R'=0.

Hence the "Race" condition will occur in the basic SR flip-flop.

Inputs				Outputs		Comment
Case	Clock	S	R	Q_{n+1}	$\overline{Q_{n+1}}$	
I	0	x	x	Q_n	$\overline{Q_n}$	No change as E=0
II	1	0	0	Q_n	$\overline{Q_n}$	No change (NC)
III	1	0	1	0	1	Reset condition
IV	1	1	0	1	0	Set condition
V	1	1	1	Intermediate		Avoid this condition

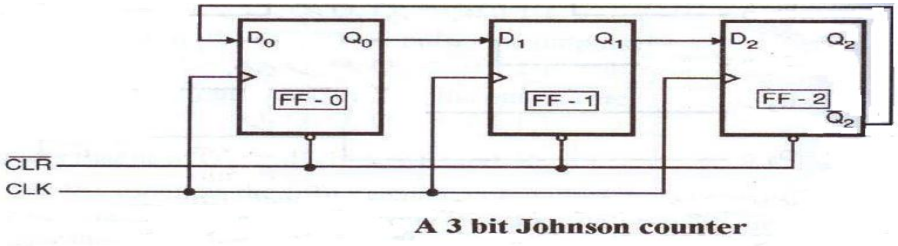


b) Describe with diagram 3-bit twisted ring counter using D flip-flops.

Ans b. **2 Marks diagram, waveforms, table.**

2 Marks -Explanation

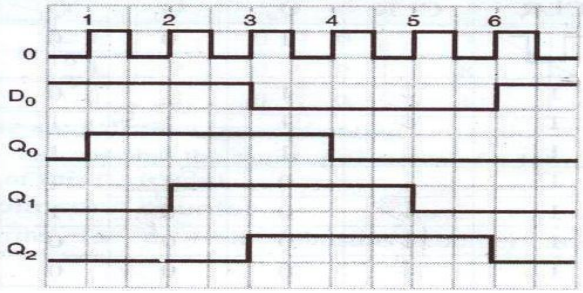
When the outputs are cross coupled to the inputs i.e. if Q_2 is connected to D_0 then the circuit is called as 3bit twisted ring counter or Johnsons counter.



A 3 bit Johnson counter

Summary of operation of Johnson's counter

Clear	CLK	Q_2	Q_1	Q_0	$Q_0 = \overline{Q}_2$
⊓	Initially	0	0	0	1
1	↑	0	0	1	1
1	↑	0	1	1	1
1	↑	1	1	1	0
1	↑	1	1	0	0
1	↑	1	0	0	0
1	↑	0	0	0	1



Explanation –

- All the flip flops are positive edge triggered and clock pulses are applied to all simultaneously.
- The clear inputs of all flip-flops are connected to clear signal and this will reset all the flip flops initially.
- AT the first positive edge of the clock FF-0 will be set so Q_0 will become 1.But no change in status of other flip-flops.
- At the second positive edge of the clock FF-0 continues in set mode and FF-1 will also set. No change in third flips flop.
- At the third positive edge of the clock FF-0 continues to be set, FF-1 continues to be set and FF-2 will also set.
- At the fourth positive edge of the clock FF-0 will reset and other flip flops remain unchanged. The operation continues till we reach all zero outputs state.
- The operation is shown in the truth table and in waveforms.

c) Compare TTL and CMOS logic families (any four points)

Ans c. **Each correct comparison ---- 1 mark**

Parameters	**CMOS**	**TTL**
Device used	P- Channel & N-Channel MOSFET	BJT (transistor)
Noise Margin	1.45 v	0.4v
Noise immunity	Better than TTL	Less than CMOS
Propagation delay	105 nsec	10 nsec
Switching speed	Less than TTL	Faster than CMOS
Power dissipation	Less 0.1 mW	More 10 mW
Fan out	50	10
Unused input	Connect to ground or VCC	Input can remain floating & treated as logic 1
Operating region	Ohmic & cutoff region	Saturation or cutoff region
Component density	Need Smaller space	Need more space than CMOS
Figure of merit	0.7PJ	100 PJ
VIH(min) VIL(max) VOH(min) VOL(max)	3.5V 1.5v 4.95v 0.05	2 v 0.8v 2.7v 0.4v

d) Design 4-bit Binary to Gray code converter using K-map.

Ans d. **Truth table ---1 mks, kmap ----2 Marks, logical diagram ---1 Mark**

Truth table relating binary and gray codes

Decimal	Binary inputs				Gray outputs			
	B_3	B_2	B_1	B_0	G_3	G_2	G_1	G_0
0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	1
2	0	0	1	0	0	0	1	1
3	0	0	1	1	0	0	1	0
4	0	1	0	0	0	1	1	0
5	0	1	0	1	0	1	1	1
6	0	1	1	0	0	1	0	1
7	0	1	1	1	0	1	0	0
8	1	0	0	0	1	1	0	0
9	1	0	0	1	1	1	0	1
10	1	0	1	0	1	1	1	1
11	1	0	1	1	1	1	1	0
12	1	1	0	0	1	0	1	0
13	1	1	0	1	1	0	1	1
14	1	1	1	0	1	0	0	1
15	1	1	1	1	1	0	0	0

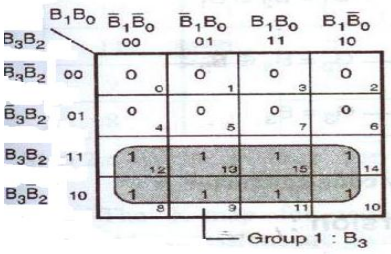
Write K-map for each Gray output and obtain the simplified expression :

∴ Simplified equation : $G_3 = B_3$

∴ Simplified equation : $G_2 = \bar{B}_3 B_2 + B_3 \bar{B}_2$

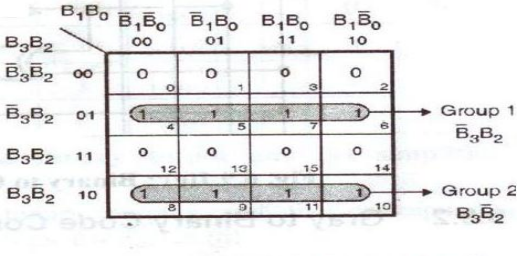
∴ $G_2 = B_3 \oplus B_2$

For output B_3



K-map for G_3

For output B_2



K-map for G_2

∴ Simplified equation : $G_1 = B_2\bar{B}_1 + \bar{B}_2 B_1$

$= B_2 \oplus B_1$

∴ Simplified equation : $G_0 = B_1 B_0 + B_1 B_0$

$= B_1 \oplus B_0$

e) State and prove De-Morgan's First and second theorem for two variables.

Ans e. **Each Theorem ---- 2 marks**
Statement ----- 1 Mark
Proof ----- 1 Mark

Ans:- Demorgans 1st Theorem- It states that complement of product is equal to sum of their compliments.

i.e $\overline{AB} = \overline{A} + \overline{B}$

1	2	3	4	5	6
A	B	$\overline{AB}$	$\overline{A}$	$\overline{B}$	$\overline{A} + \overline{B}$
0	0	1	1	1	1
0	1	1	1	0	1
1	0	1	0	1	1
1	1	0	0	0	0

Column 03 = column 06

thus $\overline{AB} = \overline{A} + \overline{B}$

Demorgans 2nd Theorem - It states that complement of sum is equal to product of their compliments.

i.e $\overline{A+B} = \overline{A} \cdot \overline{B}$

1	2	3	4	5	6
A	B	$\overline{A+B}$	$\overline{A}$	$\overline{B}$	$\overline{A} \cdot \overline{B}$
0	0	1	1	1	1
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	0

Column 03 = column 06

$\therefore \overline{A+B} = \overline{A} \cdot \overline{B}$

Hence proved.

f) With neat logic circuit realize the expression Y=AB+CD by
NOR gates only

NAND gates only

Ans f. **NOR gates only -- 2 Marks**
NAND gates only -- 2 Marks.

Using NOR gates only $Y = AB + CD$

Take double inversion

$$\therefore Y = \overline{\overline{AB + CD}} = \overline{\overline{M + N}}$$

$$\therefore Y = \overline{\overline{M} \cdot \overline{N}} = \overline{(\overline{AB}) \cdot (\overline{CD})}$$

Now let us use the De-Morgan's first law i.e.

$$\overline{A \cdot B} = \overline{A} + \overline{B}$$

$$\overline{AB} = \overline{A} + \overline{B} \text{ and } \overline{CD} = \overline{C} + \overline{D}$$

$$\therefore Y = \overline{(\overline{A} + \overline{B})\ (\overline{C} + \overline{D})}$$

Now let $\overline{A} + \overline{B} = P$ and $\overline{C} + \overline{D} = Q$

$$\therefore Y = \overline{P \cdot Q}$$

Use De-Morgan's first law again to write

$$Y = \overline{P} + \overline{Q}$$

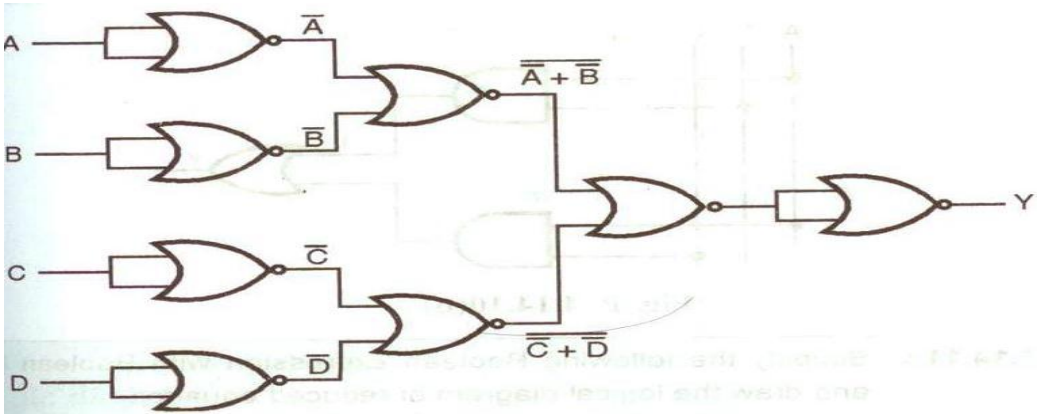
$$Y = \overline{(\overline{A} + \overline{B})} + \overline{(\overline{C} + \overline{D})}$$

Take double inversion of RHS to write

$$Y = \overline{\overline{\overline{A} + \overline{B} + \overline{C} + \overline{D}}}$$

The logic diagram for this expression is shown in Fig.

(i)



(ii)

Using NAND gates.

Y=AB+CD

Let AB=M and CD=N

Y=M+N

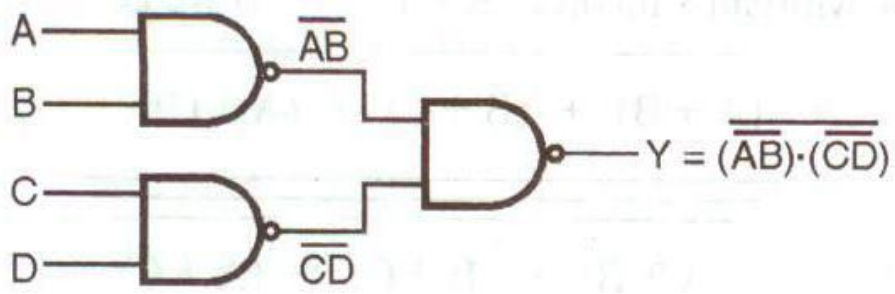
Take double inversion on both the sides

Therefore, $Y=\overline{\overline{M+N}}$

$=\overline{\overline{M}\cdot\overline{N}}$ (As per De Morgan's second law)

Substitute the value of M and N.

The logic diagram is as shown.



5. Attempt any four: (4×4=16)

a) Draw the circuit diagram of 4:1 MUX and explain its working with truth-table.

Ans:-

Circuit Diagram ---2 Marks ; Truth Table --- 1 Mark

Explanation ----1 Mark

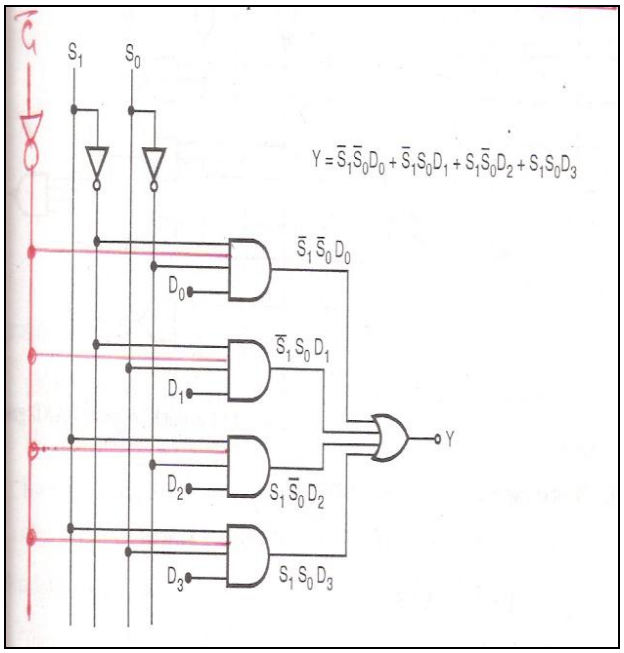


Fig: Circuit diagram of 4:1 MUX

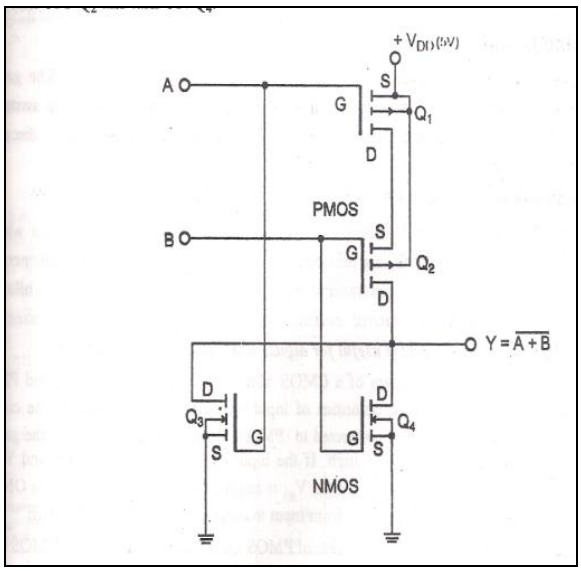
Strobe $\bar{G}$	Select inputs S_1	Select inputs S_0	Output Y
0	0	0	D_0
0	0	1	D_1
0	1	0	D_2
0	1	1	D_3
1	X	X	0

Truth table of 4:1 MUX

As shown a 4:1 MUX consists of 4 data inputs D_0, D_1,D_2 and D_3,two select lines S_1 and S_0, a strobe terminal and a o/p Y. Among the 4 inputs ,any one input will be steered at the output that depends on the combination of the select lines as shown in the truth table .Also if the strobe is active high, it doesn't care for the combination of the select lines and output is zero. But if the strobe is given active low then MUX will function as per the select inputs.

b) Draw and explain the circuit of CMOS-NOR gate.

Ans:- circuit of CMOS-NOR gate ---------2 Marks Truth table ----------1 Mark
Explanation ----------1 Mark



Inputs		Output
A	B	$Y = \overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

Explanation:

The operation of CMOS NOR gate is as shown below in table form (the same can be explained in words also.

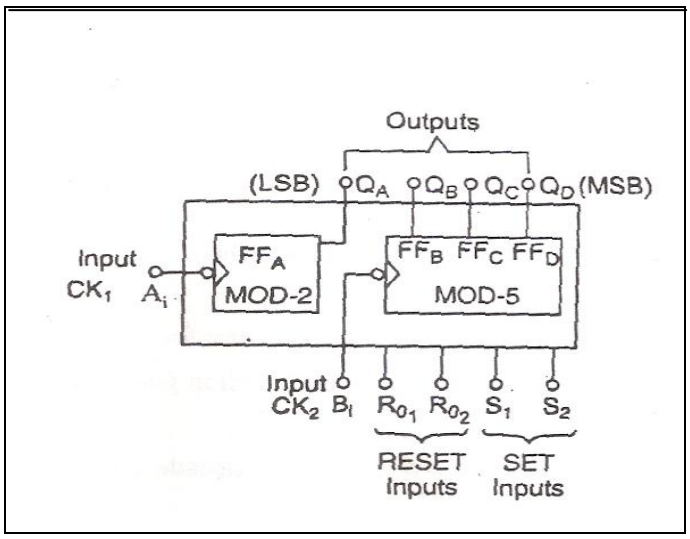
Inputs		State of CMOS				Output
A	B	Q_1	Q_2	Q_3	Q_4	Y
Low (0)	Low (0)	ON	ON	OFF	OFF	High (1)
Low (0)	High (1)	ON	OFF	OFF	ON	Low (0)
High (1)	Low (0)	OFF	ON	ON	OFF	Low (0)
High (1)	High (1)	OFF	OFF	ON	ON	Low (0)

c) **Draw the internal diagram of IC 7490 and explain**.

Ans:-

Internal Diagram of IC 7490 ----------2 Marks

Explanation ---------- 2 Marks



Explanation:-

- IC 7490 is a Asynchronous decade counter IC which consists of a MOD 2 counter and a MOD 5 Counter .
- IC 7490 consists of four Master Slave J-K flip-flops grouped internally so as to provide a MOD-2 and MOD-5 counters.
- Flip Flop FF_A operates as a MOD-2 counters, whereas the combination of flip flops FF_B, FF_C, and FF_D form a MOD-5 counter.
- There are two RESET inputs, R_{01} and R_{02}, both of which are to be connected to logic 1 level for clearing all the Flip Flops.
- There are also two SET inputs S_1 and S_2 which are to be connected to logic 1 level for setting the initial output of the counter to logic 1. (2 mks)

d) Explain the working of Maser-Slave J-K flip-flop with truth-table.

Ans:-Logical Diagram -----2 Marks

Truth Table -----1 Mark

Explanation -----1 Mark

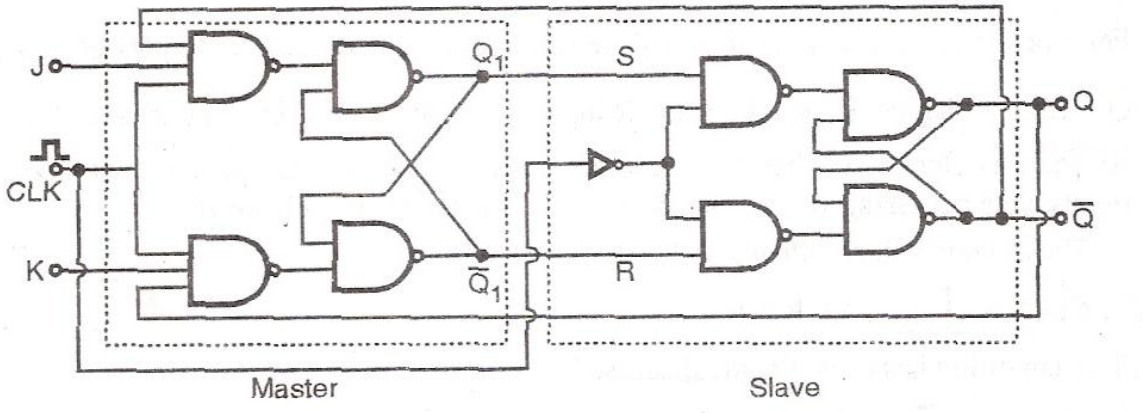


Fig: Logic Diagram of Master-Slave J-K Flip Flop

Case	Inputs			Outputs		Remark
	CLK	J	K	Q_{n+1}	$\bar{Q}_{n+1}$	
I	×	0	0	Q_n	$\bar{Q}_n$	No change
II	⎍ (1)	0	0	Q_n	$\bar{Q}_n$	No change
III	⎍ (1)	0	1	0	1	Reset
IV	⎍ (1)	1	0	1	0	Set
V	⎍ (1)	1	1	$\bar{Q}_n$	Q_n	Toggle

Truth Table of Master-Slave J-K Flip Flop

Explanation:-

case1:- when clock is not applied output doesn't change.

case2:- when clock is applied as J and K both are zero then output doesn't change.

case3:- when clock is applied as J=0 and K=1 then Q=0.This state is also called as Reset state.

case4:- when clock is applied as J=1 and K=0 then Q=1. This state is also called as set state.

case5:- when clock is applied as J=1 and K=1 then output will be toggled to the next state

e) Explain with circuit diagram, the principle of TTL gate (NAND) with totem-pole.

Ans:-3 i/p TTL gate is as shown ------- 2 Marks

Truth Table ------- 1 Mark

Explanation ------- 1 Mark

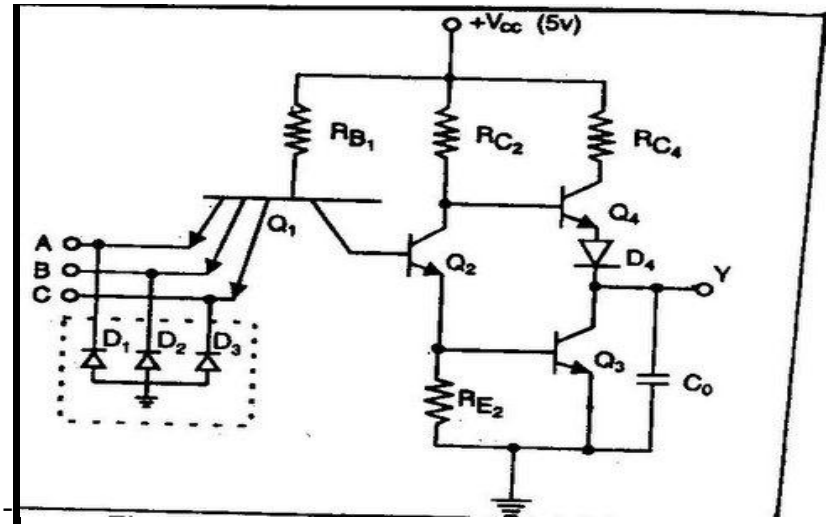


Fig: TTL NAND gate with Totem - Pole

Truth Table :-

Input			Output
A	B	C	Y
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Explanation:-

If any of the inputs or all the inputs are active low. i.e. logic 0.

Under this state, the transistor Q_1 is in saturate state.The above vol of Q_2 is at logic low(0.7).

So Q_2 and Q_4 remain in cutoff state.off state of Q_2 causes potential at point x at logic 1 level ie. +Vcc.This causes Q_3 and diode D to be forward bias.so the o/p is a logic 1(+Vcc)

When A=B=1

Under this condition,Transistor Q_1 is in cutoff state.So collector potential V_{C1} is at +Vcc.This causes Q_2 and Q_4 to operate in saturation region.so potential at point x is at logic 0 level.This makes Q_3 and diode to remain in cutoff.So o/p is at logic 0 level.

Function fo Diode D:

Diode D prevents transistor Q_3 turn ON when transistor Q_2 and Q_4 are conducting state.When Q_2 is in saturation,the potential at point x is calculated as-

$V_x=V_{c2}= V_{CE2SAT} + V_{R3}$

$=V_{CESat} + V_{BE4Sat}$

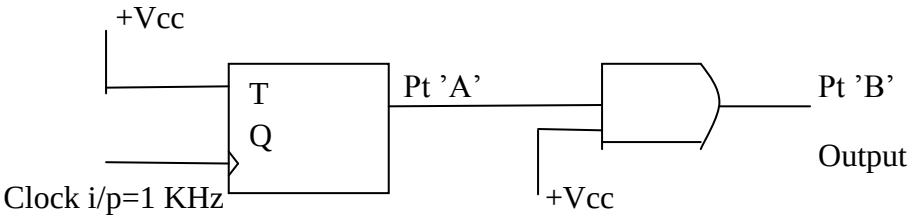
$= 0.2+0.7$

$= 0.9$ V

Therefore,this collector potential is not sufficient enough to turn on Q_3 and diode D.Thus when Q_2 and Q_4 are conducting,Q_3 remains off because of Diode D.

This configuration at o/p ie.when Q_3 is conducting,Q_4 should remain in cutoff and when Q_4 is conducting,Q_3 should be in cutoff is called as totem pole o/p configuration.

f) Refer the figure no 1 and answer the following:



If the clock input frequency is 1 KHz, draw the waveforms at point A and at point B. Write down the frequencies for the same.

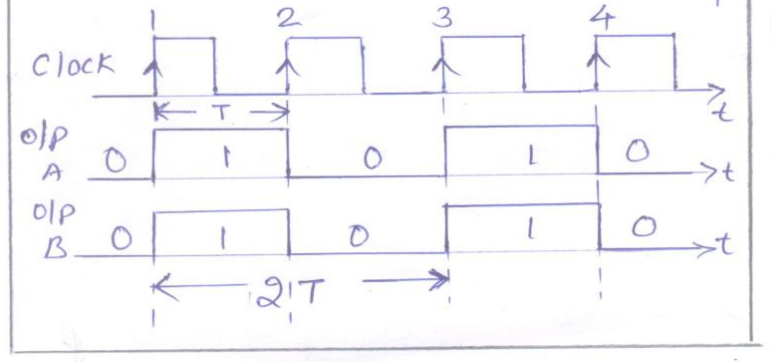
Ans:- Truth Table ----- 1 Mark

Waveform ----- 2 Marks

Correct Frequencies ----1 Mark

Let the outputs at A=0 and hence output at B is also Zero (AND Gate) So the truth table and waveform is as shown

Clock ↓	T +Vcc	O/P A	O/P B
0	1	0	0
1	1	1	1
2	1	0	0
3	1	1	1
4	1	0	0



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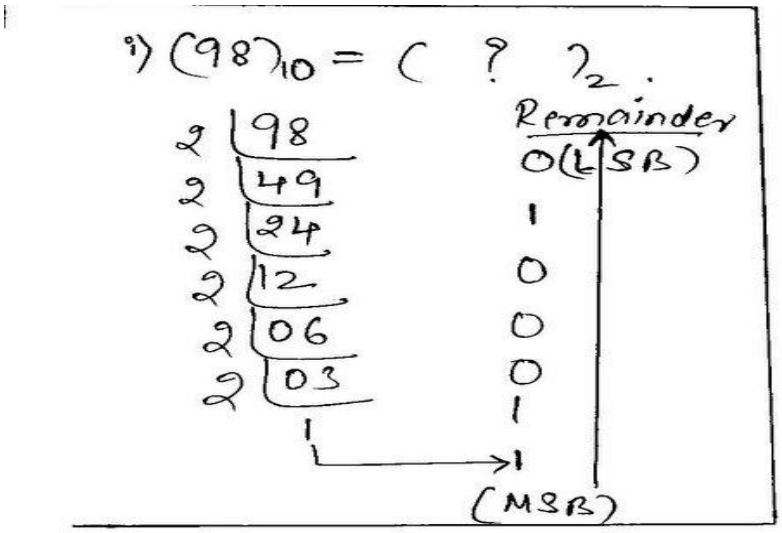
So the circuit acts like MOD 2 i.e. divide by 2 Counter i.e. the frequency at the o/p A and B is half of the clock frequency i.e. 500Hz.

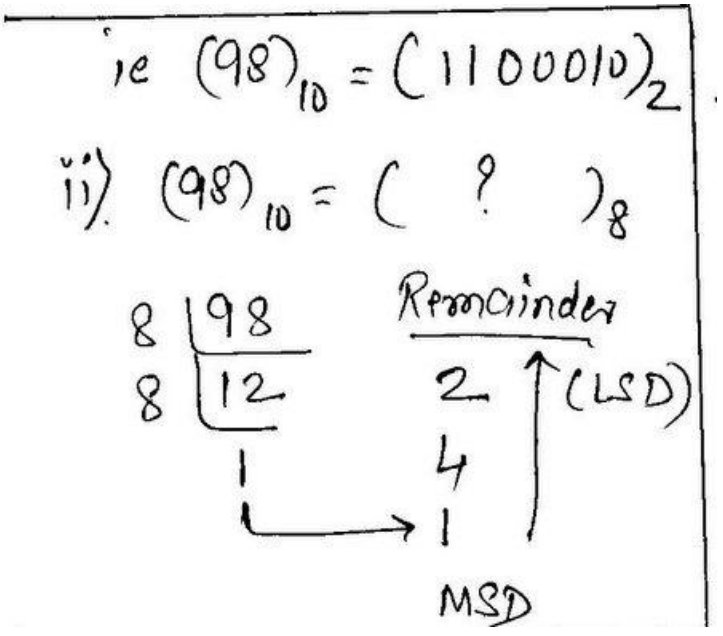
Attempt any four: (4×4=16)

a) **Convert $(98)_{10}$ into**

- **i) Binary**
- **ii) Octal no.**
- **iii) Hex no**
- **iv) BCD no.**

Ans:- **Each correct Ans. ---- 1 Mark**





$(98)_{10} = (142)_8$

iii) $(98)_{10} = (\ ?\ )_{16}$

Remainder (LSD)

16 | 98

6 — 2

6 (MSD)

ie $(98)_{10} = (62)_{16}$.

iv) $(98)_{10} = (\ ?\ )_{BCD}$.

9 8

↓

$(1001\ \ 1000)_{BCD}$.

a) Describe with neat diagram and truth-table the 3-bit ripple UP-counter.

Ans:- **Diagram of 3-bit ripple UP-counter -----1 Mark**
Description ----------1 Mark
Truth table --------1 Mark
Waveform --------1 Mark

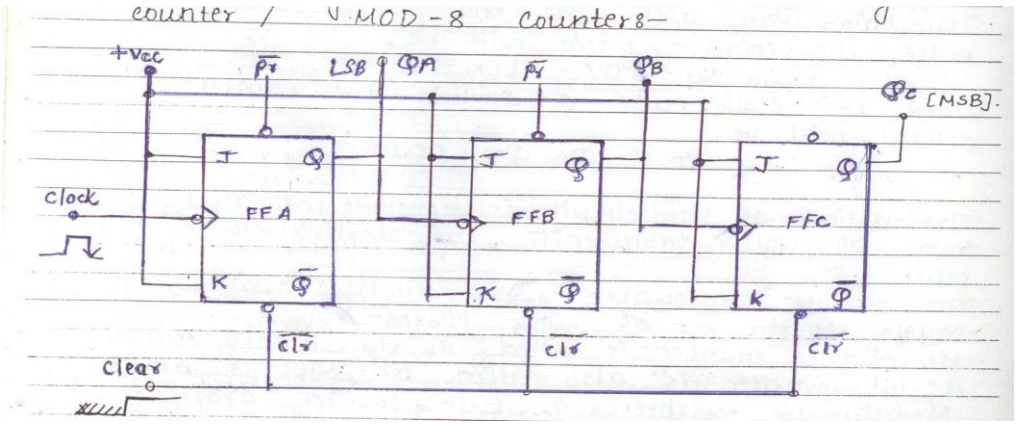


Fig: Diagram of 3 bit Ripple Up-Counter

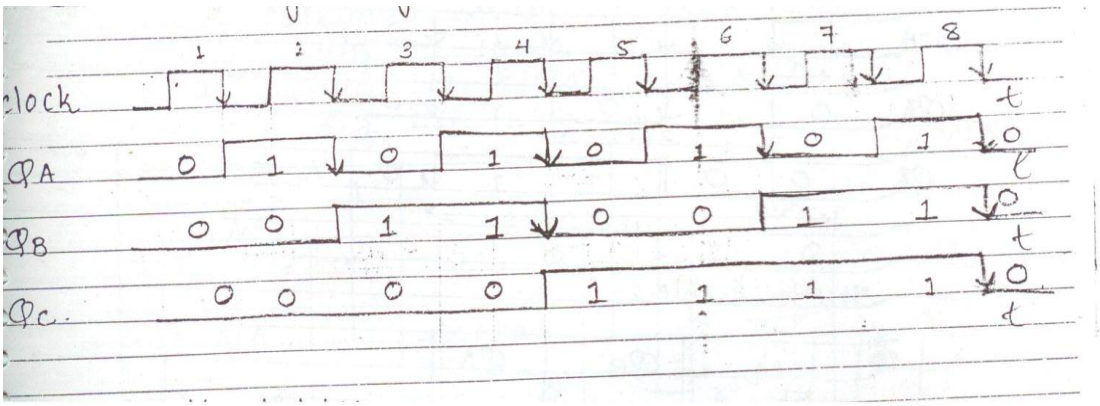
Description:- As shown in the diagram the counter consists of 3 flipflops, in which clock is applied to first flipflop ,o/p of first flipflop acts as clock for second fliipflop,o/p of second acts as clock for third.o/ps are taken at Q_A(LSB),Q_B and Q_C (MSB) .After application of clock pulses (high to low transition only) ,o/p of flipflop toggles to next state .Thus giving binary count from 000 to 111,called as MOD 8 Counter/3 bit ripple counter.

The truth table is as shown below-

Truth table:-

Clear	clock ↓	Q_C MSB	Q_B	Q_A LSB	
0	0	0	0	0	
1	1	0	0	1	
1	2	0	1	0	
1	3	0	1	1	
1	4	1	0	0	
1	5	1	0	1	
1	6	1	1	0	
1	7	1	1	1	
1	8	0	0	0	← Initial state

The waveforms are as shown below-



b) Prove that

i) $XY+\overline{XY}.Z=XY+Z$

ii) $AB+\overline{A}B+A\overline{B}=\overline{A}+B$

Ans:-Solution:- **(2 Marks each)**

i) $XY+\overline{XY}\cdot Z = XY+Z$

Solution :- Let $XY=A$, $Z=B$.

So, $LHS = XY+\overline{XY}\cdot Z = A+\bar{A}B$

$=(A+\bar{A})(A+B)$ (Use distributive law)

$= A+B \quad (A+\bar{A}=1)$

$= XY+Z$ (Substituting)

$= RHS.$

ii) $AB+\bar{A}B+\bar{A}\bar{B} = \bar{A}+B.$

$LHS = AB+\bar{A}B+\bar{A}\bar{B}$

$= B(A+\bar{A})+\bar{A}\bar{B}$

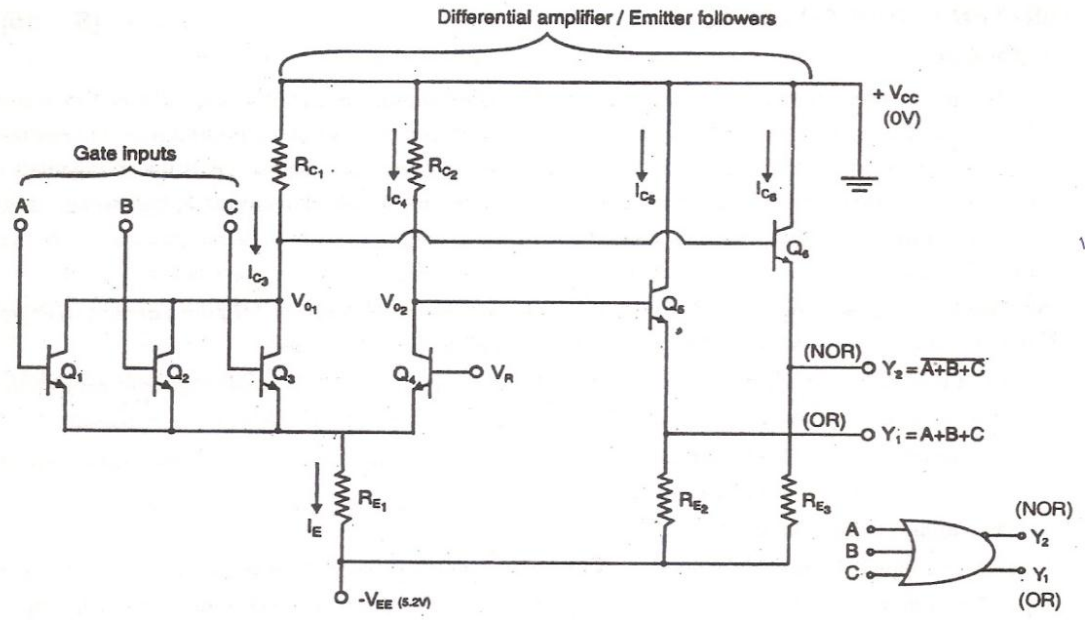
$= B+\bar{A}\bar{B} \quad (A+\bar{A}=1)$

$=(\bar{A}+B)(B+\bar{B})$ (using distributive law)

$= \underline{\underline{\bar{A}+B}} = RHS.$

c) Draw the circuit diagram and explain the working principle of ECL logic family.
Ans:-

Circuit Diagram ECL logic family. ----2 Marks
Truth table ------1 Mark
Working Principle ---------2 Marks



Truth Table:

ECL family Truth table

A	B	C	Y	$\bar{Y}$
0	0	0	0	1
0	0	1	1	0
0	1	0	1	0
0	1	1	1	0
1	0	0	1	0
1	0	1	1	0
1	1	0	1	0
1	1	1	1	0

Explanation :-

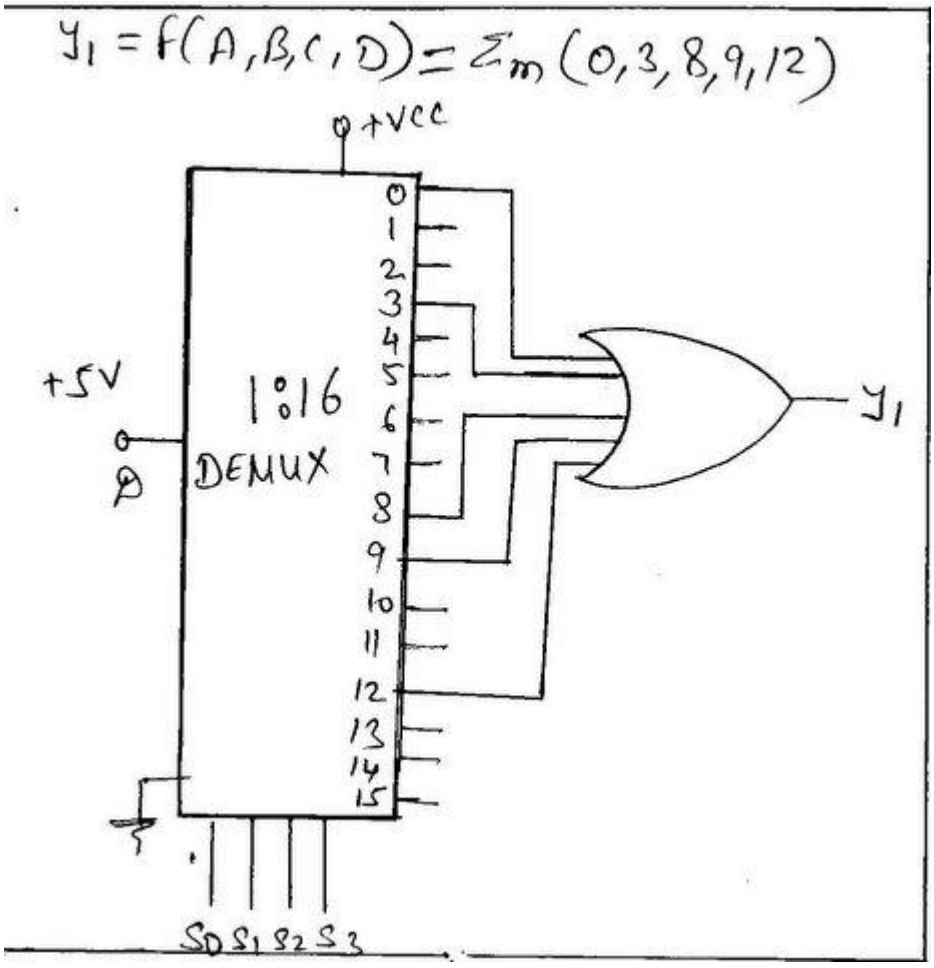
- As shown the ECL gate consists of fan in circuit, emitter coupled differential amplifier and emitter followers.
- The emitter coupled difference amplifier is realized by transistors Q3 and Q4 and it performs the logic operation. Additional transistors Q1 and Q2 are used in parallel with Q3 to get the required fan in capacity.
- The fan in capacity is 3.The o/p stage is emitter follower .It has two o/ps Y1 and Y2 which are complementary to each other.The o/p Y1 to OR logic and Y2 to NOR logic and called as OR/NOR gate.

d) Implement the following functions using 1:16 Demultiplexer

i) $y_1 = f(A,B,C,D) = \sum m(0,3,8,9,12)$

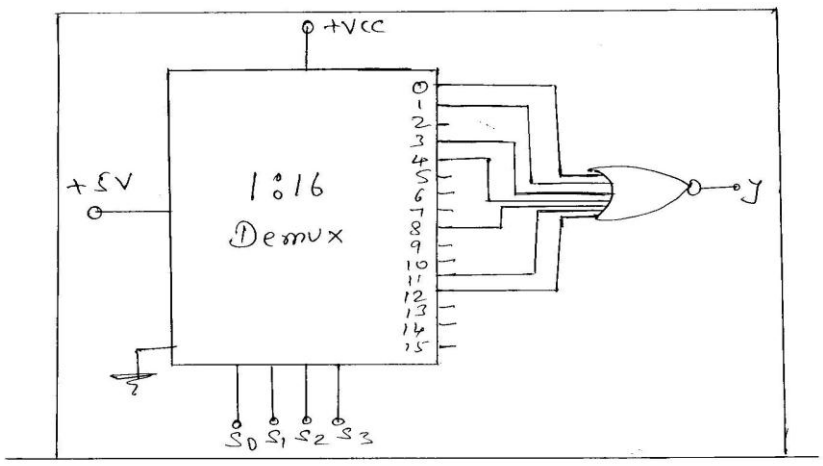
ii) $y_2 = f(A,B,C,D) = \prod m(0,1,3,4,8,11,12)$

Ans:- i) $y_1 = f(A,B,C,D) = \sum m(0,3,8,9,12)$ correct implementation---------2 Marks

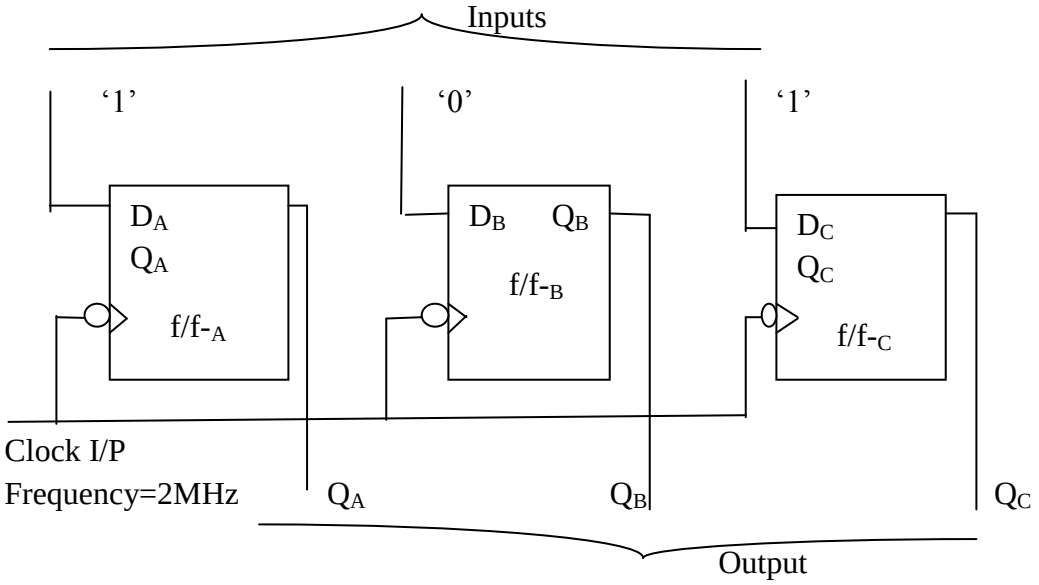


ii) $y_2 = f(A,B,C,D) = \prod m(0,1,3,4,8,11,12)$ Correct implementation---- 2Marks

Ans:- For POS ,O/P y2 should be at logic 0 (so mks to be given for proper logical connection).



e) Study the given fig.no.2.of PIPO register. Calculate the time required to get the output $Q_AQ_BQ_C$=101.



Ans:-The given register is PIPO and it requires only one clock pulse for its operation. As the clock frequency is 2 MHz, so the time period is given as

$T = 1/F = 1/(2 * 10^6) = 0.5\ \mu Sec.$

So time required for PIPO operation is only 0.5 µSec. (4 mks)

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