Important Instructions to examiners:

1) The answers should be examined by key words and not as word-to-word as given in the model answer scheme.
2) The model answer and the answer written by candidate may vary but the examiner may try to assess the understanding level of the candidate.
3) The language errors such as grammatical, spelling errors should not be given more Importance (Not applicable for subject English and Communication Skills).
4) While assessing figures, examiner may give credit for principal components indicated in the figure. The figures drawn by candidate and model answer may vary. The examiner may give credit for any equivalent figure drawn.
5) Credits may be given step wise for numerical problems. In some cases, the assumed constant values may vary and there may be some difference in the candidate's answers and model answer.
6) In case of some questions credit may be given by judgement on part of examiner of relevant answer based on candidate's understanding.
7) For programming language papers, credit may be given to any other program based on equivalent concept.

Q1 Attempt any ten of the following : 10*2=20

a) Define power dissipation and figure of merit.

Ans : Power dissipation: This is the amount of power dissipated in an IC. 1

Figure of merit : The product of propagation time(t_{pd}) and power dissipation (P_o) is known as figure of merit.

b) Convert the following Binary number into Hex. Number: 1

Ans : (i) $\left(\frac{10}{2}\frac{1011}{B}\right)_2$ $= (2B)_{16}$

Alternate method

$= 1*2^5 + 0*2^4+1*2^3+0*2^2+1*2^1+1*2^0$

$= 32+8+2+1$

$= (43)_{10}$

16 | 43

2 → 11 (B) $(2B)_{16}$

(ii) $(1101001) = (0110\ \ 1001)_2 = (69)_{16}$

Alternate Method

$= 1*2^6+1*2^5+0*2^4+1*2^3+0*2^2+0*2^1+1*2^0$

$= 64+32+8+1$

$= (105)_{10}$

16 | 105

6 → 9 $=(69)_{16}$

c) Find 2's complement of following numbers

i) $(110110)_2$

Take 1's complement of $(110110)_2 = 0001001$

Add = + 1

001010

2's complement is $(001010)_2$ 1

ii) $(010100)_2$

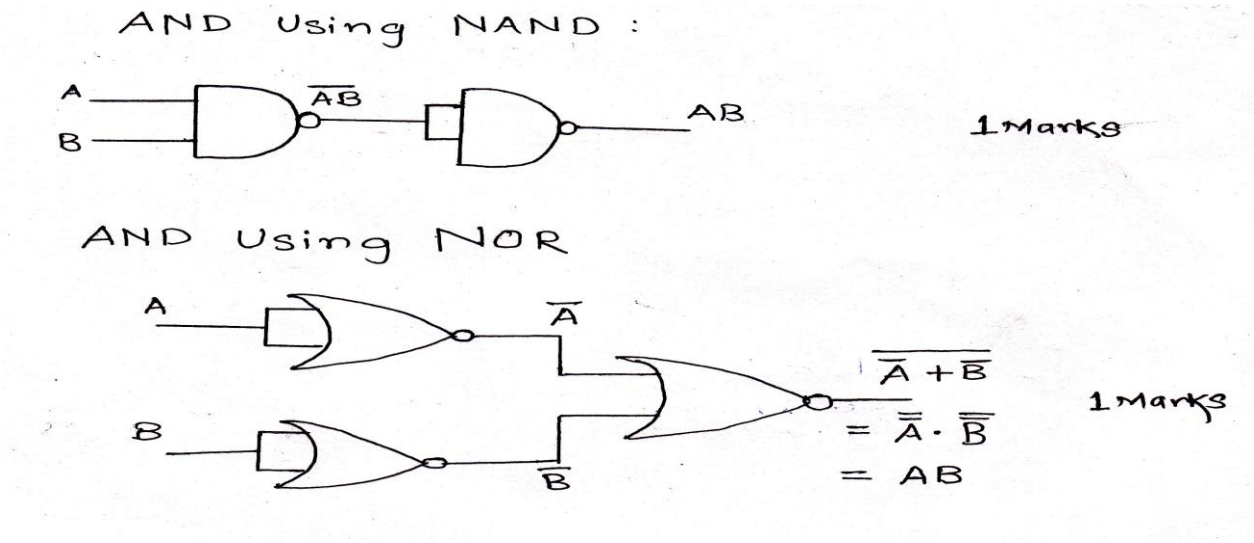
Take is complement of $(010100)_2 = 101011$

Add = + 1

101100

2's complement is $(101100)_2$ 1

d) Draw AND gate using NAND gate only and NOR gate only



e) Perform the following Binary addition **1**

i) $(101011)_2 + (10110)_2$

```
  101011
+ 10110
--------
 1000001
```

Ans : $(1000001)_2$

ii) $(11001)_2 + (10101)_2$ 1

```
   11001
+ 10101
--------
  101110
```

Ans : $(101110)_2$

f) Convert the following octal number into Hex number

i) $(626)_8$

ii) $(1245)_8$

Ans i) $(626)_8$ 1

Binary Is $(110\ \ 010\ 110)_2 = (0001\ \ 1001\ \ 0110)_2 = (196)_{16}$

Equivalent of hexadecimal is $(196)_{16}$

Alternative method

Convert into decimal i.e.

$= 6*8^2+2*8^1+6*8^0$

$= 384+16+6$

$= (406)_{10}$

Now convert into hexa decimal i.e.

16 | 406

16 | 25 ⟶ 6

1 ⟶ 9

$=(196)_{16}$

i) $(1245)_8$ 1

Convert into equivalent binary is

Binary Is $(001\ \ 010\ 100\ 101)_2 = (0010\ \ 1010\ \ 0101)_2 = (2A5)_{16}$

Equivalent of hexadecimal is $(2A5)_{16}$

Alternative method

Convert into decimal i.e.

$= 1*8^3+2*8^2+4*8^1+5*8^0$

$= 512+128+32+5$

$= (677)_{10}$

Now convert decimal into hexadecimal number i.e.

16 | 677

16 | 42 → 5

2 → 10(A)

$=(2A5)_{16}$

g) Define min and max term

Ans : Minterm – The product of all the variables in complimented and uncomplimented form is called minterm 1

OR

Minterm – Each individual term in STD SOP is called as a Minterm 1

called minterm

Maxterm – The summation of all the variable in complimented and uncomplimented form is called Maxterm 1

OR

Maxterm – Each individual term in STD POS is called as a Maxterm

h) Define counter and modulus of counter

Ans : Counter : A circuit which generates a prescribed sequence of bits, in synchronism with a clock. 1

Or

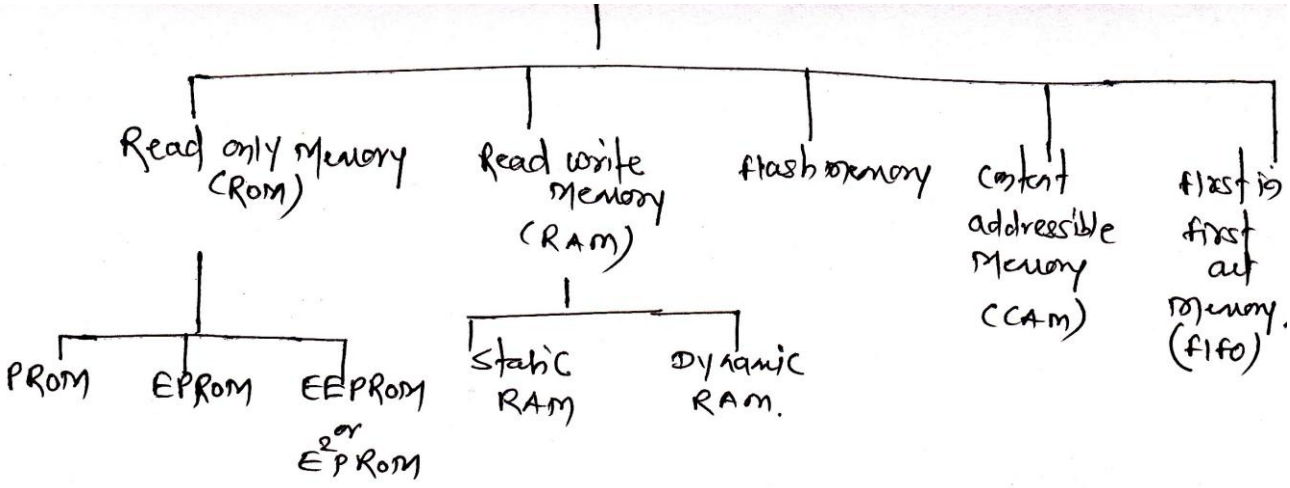
A circuit which is used to count the number of clock cycles.

Modulus of counter : 1

The number of unique states that a counter may have before the sequence repeats itself is the modulus of the counter.

i) Give the classification of different types of semiconductor memories 2

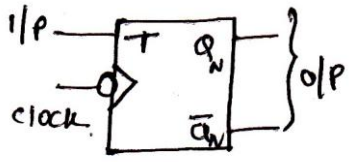
Semiconductor Memories



j) Draw symbol and truth table of negative edge triggered T flip flop and positive edge triggered D flip flop

Ans Negative edge triggered T f/f 1

Symbol

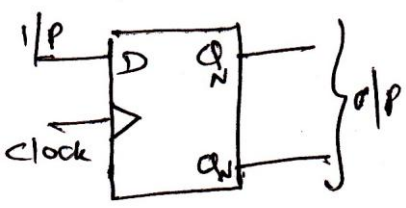


Truth table

Clock	i/p T	Output Q_N	$\overline{Q_N}$
0	X	No change or Q_{N-1}	No change or $\overline{Q_{N-1}}$
↓	0	No change or Q_{N-1}	No change or $\overline{Q_{N-1}}$
↓	1	$\overline{Q_{N-1}}$	Q_{N-1}

Positive edge trigger D f/f 1

Symbol



Truth table

Clock	i/p D	Output Q_N	$\overline{Q_N}$

0	X	Q_{N-1} or No change	$\overline{Q_{N-1}}$ or No change
	0	0	1
	1	1	0

k) State De- Morgan's theorem

De-Morgan's first theorem :- 1

Complement of a sum equals the product of the individual complements

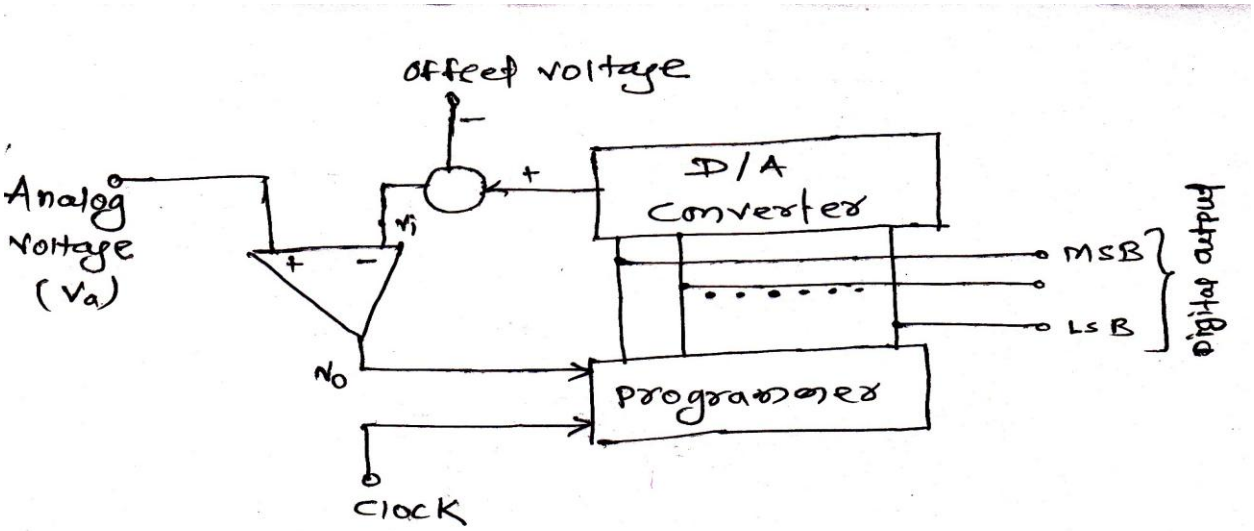
$\overline{A+B} = \overline{A}.\overline{B}$ De-

Morgan's second theorem :- 1

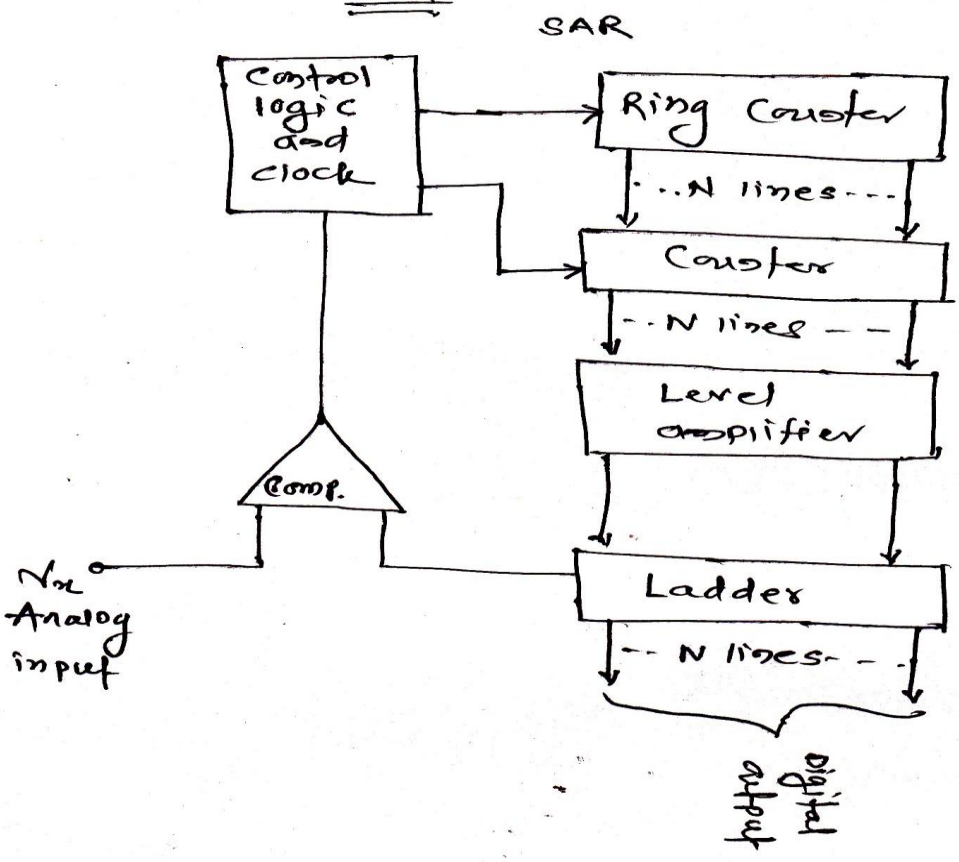
Complement of a product equals the sum of the individual complements

$\overline{AB} = \overline{A} + \overline{B}$

l) Draw Successive approximation ADC. **2**



OR



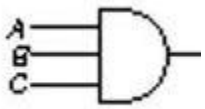
Q2 Attempt any four of the following

a) Draw symbol, logical equation and truth table of 3 i/p AND gate and 3 i/p OR gate

Name of gate

3I/P AND Gate

Symbol ½



Y= ABC

Logical equation: ½

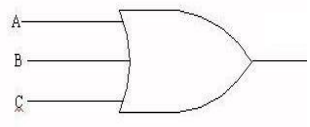
Y = ABC

Truth table 1

I/P			O/P
A	B	C	Y= ABC
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

3 i/p OR Gate

Symbol ½



Logical equation: ½

Y = A+B+C

Truth table 1

I/P			O/P
A	B	C	Y= A+B+C
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

b) List the different Boolen laws. Also write Duality theorem

[Note : List any 4 laws- 2marks]

Ans: 1) Annlment law-

a) A.0=0

b) A+1=1

2) Identity law-

a) A+0 = A

b) A.1 = A

3) indempotent law-

a) A+A = A

b) A.A = A

4) Complement law-

a) $A.\bar{A} = 0$

b) $A+ \bar{A} = 1$

5) Commutative law-

a) A.B = B.A

b) A + B = B + A

6) Double Negation law-

a) $\overline{\overline{A}} = A$

7) De morgan's theorem

$\overline{A + B} = \overline{A} \cdot \overline{B}$

$\overline{A.B} = \overline{A} + \overline{B}$

8) Distributive law

A (B + C) = AB + AC

A + BC = (A+B) . A+C)

9) Associative law

(A.B).C = A.(B.C)

(A+B) + C = A+(B+C)

Duality theorem:- 2

In a two valued Boolean algebra, the dual of an algebraic expression can be obtained by interchanging OR and AND operators & by replacing 1_s by O_s & O_s by 1_s

or

According to this theorem, any algebraic equality relation, which we derive from the statement of Boolean algebra, remains true when the operator(.) and operator (+) are interchange and also the identity elements are interchanged.

Eg. Duality of a+1=1 expression is a.0=0

c) Subtract the given number using 1's & 2's complements

$(11011)_2 – (11100)_2$

Ans: Subtracting using 1's complement. 2

$(11011)_2 – (11100)_2$

1's complement of $(11100)_2$ is 00011

11011

+ 00011

11110

As no carry, answer is negative and in 1's complement form i.e. $(-1)_{10} = (11110)_2$ for getting true Value take the 1's complement of final result i.e. $(+1)_{10} = (00001)_2$

Subtracting using 2's complement 2

2's complement of $(11100)_2$ is 1'

	00011	11011
i.e.	+ 1	+ 00100
	00100	11111

As there is no carry answer is negative & it is in complemented form i.e. $(-1)_{10} = (11111)_2$

For getting true value take 2's complement of final result

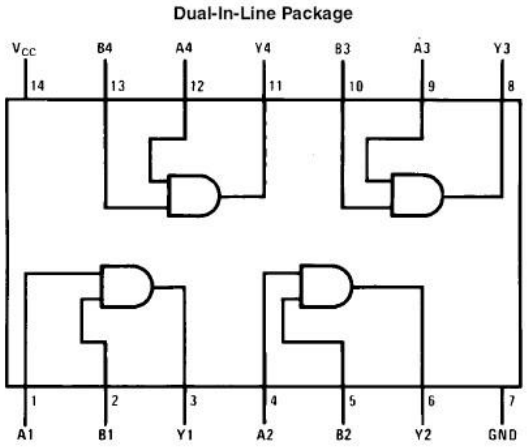
i.e. $(+1)_{10} = 00000+1$

$= (00001)_2$

d) Draw pin configuration of TTL IC used for AND gate and NAND gate.

Ans : TTL IC for AND gate is 7408 2

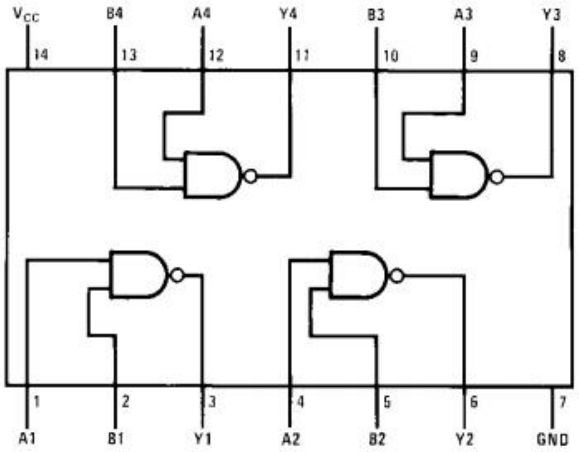
Pin diagram 7408



[Note where A & B are input to the AND gate and Y is Output of AND gate]

TTL IC for NAND gate is 7400 2

Pin diagram of 7400



[Note where A & B are input to the NAND gate and Y is Output of NAND gate]

e) Convert following octal number to Decimal & Binary numbers.

i) $(1024)_8$

ii) $(66)_8$

Ans : i) $(1024)_8 = (?)_{10}$ 1

$= 1*8^3+0*8^2+2*8^1+4*8^0$

$= 512 + 16 + 4$

$= (532)_{10}$

$(1024)_8 = (?)_2$ 1

Take equivalent 3 bit of octal no.

i.e. $(001000010100)_2$

ii) $(66)_8 = (?)_{10}$ 1

$= 6*8^1+6*8^0$

$= 48+6$

$= (54)_{10}$

$(66)_8 = (?)_2$ 1

Take equivalent 8 bit of octal no.

i.e. $(110110)_2$

f) Perform the following BCD addition

i) 0110 + 0111, ii) 1001 + 1001

i) 0110 + 0111 1

0110

+ 0111

1101 - 13 in decimal (greater than 9)

+ 0110 Add 6

1 0011

1 3 in BCD

ii) 1001 + 1001 1

1001

+ 1001

10010 - 18 in decimal (greater than 9)

+ 0110 Add 6

11000

1 8 in BCD

Q3 Attempt any four of the following.

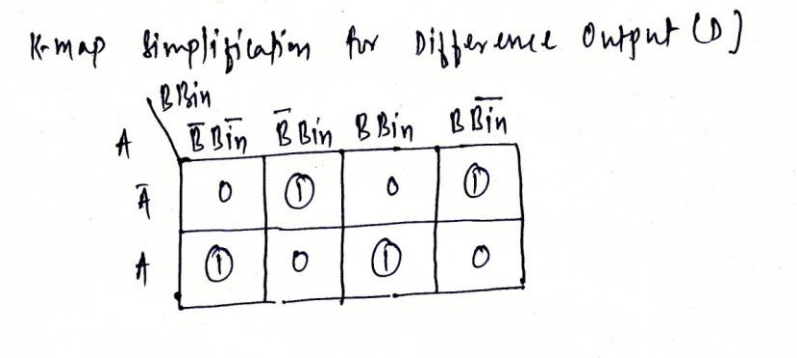
a) Design full subtractor using logic gates?

Ans:- No of Inputs = 3 (A,B, Bin)

No. of Outputs=2 (D and Bout)

Truth Table **1 mark**

Input			Output	
A	B	Bin	D	Bout
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1



1 mark

$D = \bar{A}\,\bar{B}\,B_{in} + \bar{A}\,B\,\bar{B}_{in} + A\,\bar{B}\,\bar{B}_{in} + ABB_{in}$

$= B_{in}(\bar{A}\,\bar{B} + AB) + \bar{B}_{in}(\bar{A}B + A\,\bar{B})$

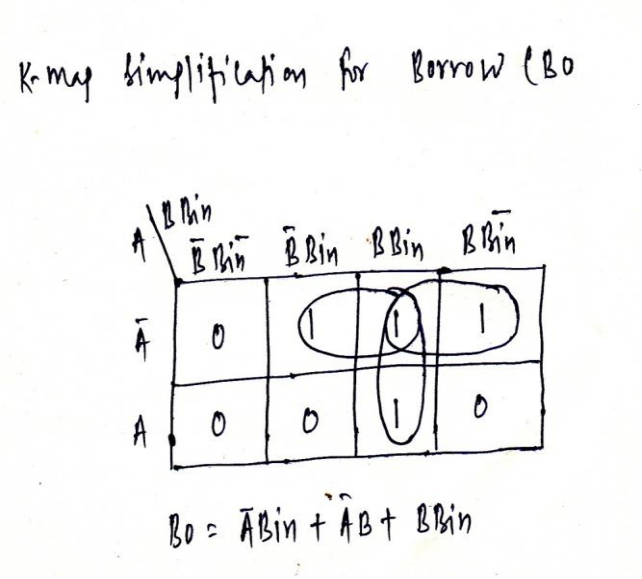
$= B_{in}(\overline{A \oplus B}) + \bar{B}_{in}(A \oplus B)$

Put $A \oplus B = x$

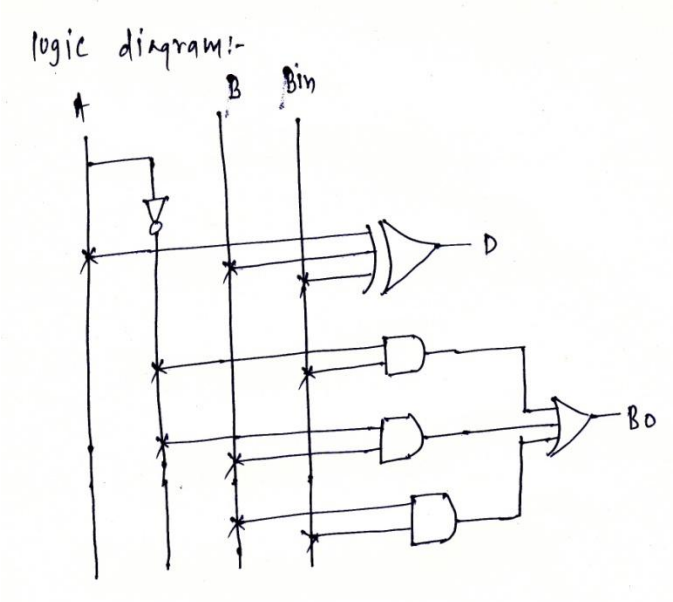
$D = B_{in}\,\overline{x} + \overline{B}_{in}\,x$

$D = B_{in} \oplus x$

$D = A \oplus B \oplus B_{in}$



1 mark

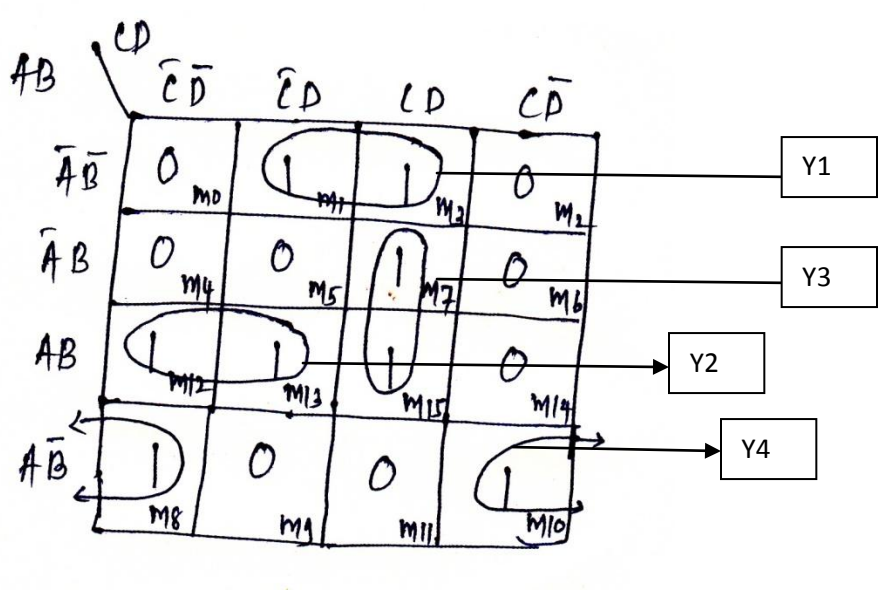


1 mark

b) Simplify the following equation using k – map and realize it using basic gates only.

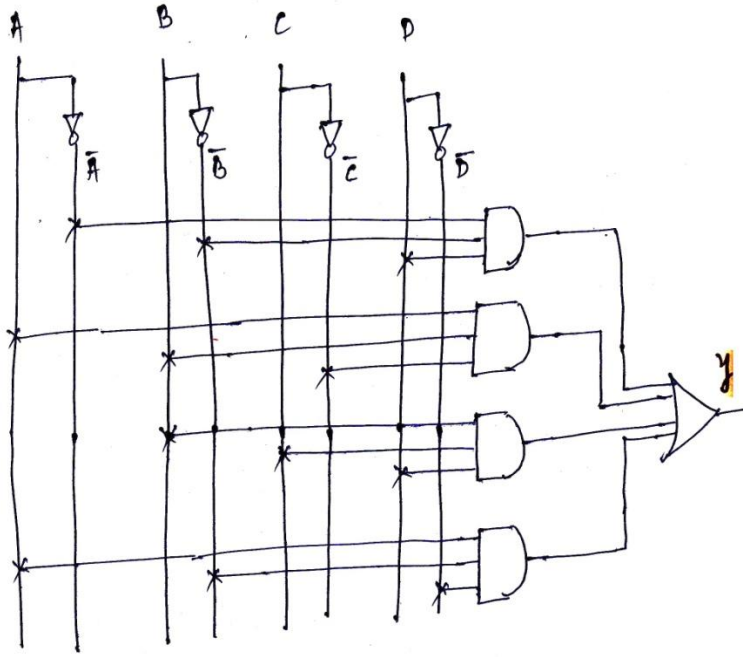
$F(A,B,C,D) = \sum m\,(1,3,7,8,10,12,13,15)$

Ans: (2 marks for K-Map and 2 marks for logic Diagram)



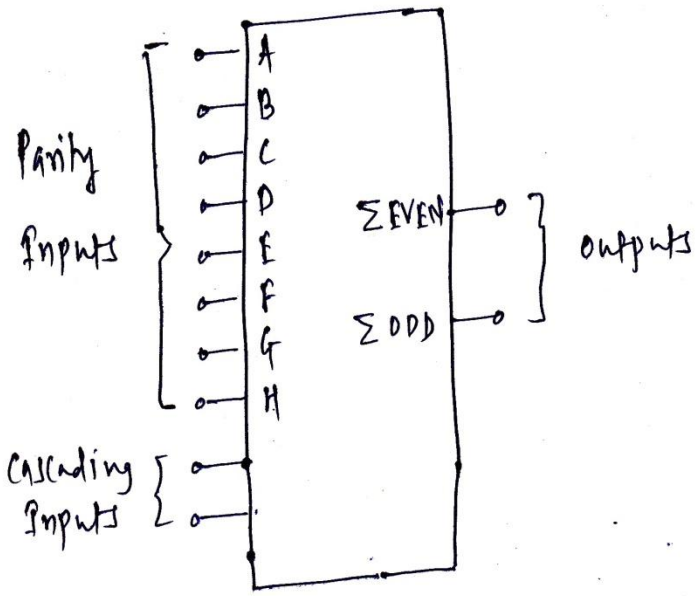
Y= F(A,B,C,D)= Y1+Y2+Y3+Y4 = $\bar{A}\,\bar{B}$ D + A B $\bar{C}$ + BCD + A $\bar{B}$ $\bar{D}$

logic Diagram:-



c) Draw block diagram and function table of parity generator IC 74180

Ans: Figure shows the block diagram of 74180 in which there are eight parity i/ps A through H, with two cascading inputs. There are two outputs ∑ EVEN & ∑ ODD. (2marks)



Block diagram of 74180 Parity Generator

Function Table of 74180 (2 marks)

Parity of i/ps A through 4	Cascading i/ps		Output	
	EVEN	ODD	∑ EVEN	∑ ODD
EVEN	1	0	1	0
ODD	1	0	0	1
EVEN	0	1	0	1
ODD	0	1	1	0
X	1	1	0	0
X	0	0	1	1

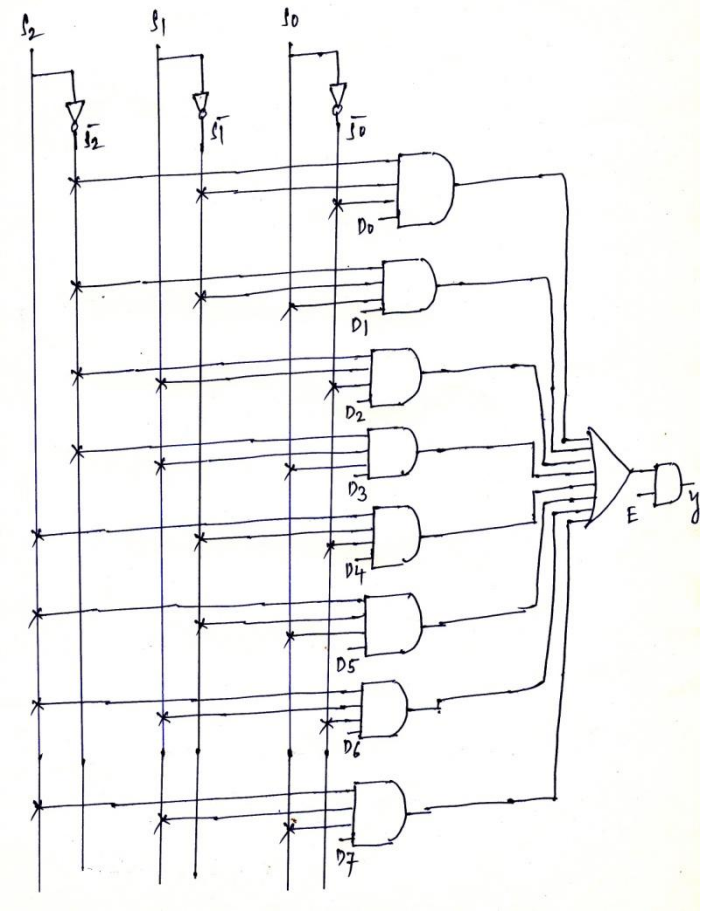
d) Design 8:1 multiplexer using basic gates

Ans :- Truth Table (1 mark)

Enable E	Select i/ps			Output Y	O/p Expression
	S_2	S_1	S_0		
1	0	0	0	D_0	$E\ \bar{S_2}\ \bar{S_1}\ \bar{S_0}\ D_0$
1	0	0	1	D_1	$E\ \bar{S_2}\ \bar{S_1}\ S_0\ D_1$
1	0	1	0	D_2	$E\ \bar{S_2}\ S_1\ \bar{S_0}\ D_2$
1	0	1	1	D_3	$E\ \bar{S_2}\ S_1 S_0\ D_3$
1	1	0	0	D_4	$E\ S_2\ \bar{S_1}\ \bar{S_0}\ D_4$
1	1	0	1	D_5	$E\ S_2 \bar{S_1}\ S_0\ D_5$
1	1	1	0	D_6	$E\ S_2 S_1\ \bar{S_0}\ D_6$
1	1	1	1	D_7	$E\ S_2 S_1 S_0\ D_7$

$Y = E \{ \bar{S_2}\ \bar{S_1}\ \bar{S_0}\ D_0 + \bar{S_2}\ \bar{S_1}\ S_0\ D_1 + \bar{S_2}\ S_1\ \bar{S_0}\ D_2 + \bar{S_2}\ S_1 S_0\ D_3 + S_2\ \bar{S_1}\ \bar{S_0}\ D_4 + S_2 \bar{S_1}\ S_0\ D_5 + S_2 S_1\ \bar{S_0}\ D_6 + S_2 S_1 S_0\ D_7 \}$

(3 marks)



NOTE :- 3 Marks to be awarded to the circuit without enable.

e) Convert the following Boolean equation into standard SOP form

i) AB + $\bar{A}$C ii) A $\bar{c}$ D + B

Ans

i) Y = AB + $\overline{A}$ C

= AB(C + $\overline{C}$) + $\overline{A}$ C (B + $\overline{B}$) (A + $\overline{A}$ = 1)

Y = ABC + AB$\overline{C}$ + $\overline{A}$ BC + $\overline{A}$ $\overline{B}$ C (2 marks)

ii) Y = A$\overline{C}$ D + B

= A$\overline{C}$ D (B +$\overline{B}$) + B (A + $\overline{A}$) (C + $\overline{C}$) (D + $\overline{D}$)

$= AB\overline{C}\,D + A\,\overline{B}\,\overline{C}\,D + (AB + \overline{A}\,B)\,\{(C + \overline{C})\,(D + \overline{D})\}$

$= AB\overline{C}\,D + A\,\overline{B}\,\overline{C}\,D + (AB + \overline{A}\,B)\,\{CD + C\overline{D} + \overline{C}D + \overline{C}\,\overline{D}\}$

$= \underline{AB\overline{C}\,D} + A\,\overline{B}\,\overline{C}\,D + ABCD + ABC\overline{D} + \underline{AB\overline{C}\,D} + AB\overline{C}\,\overline{D} + \overline{A}\,BCD + \overline{A}\,BC\overline{D} + \overline{A}B\overline{C}D + \overline{A}B\overline{C}\,\overline{D}$

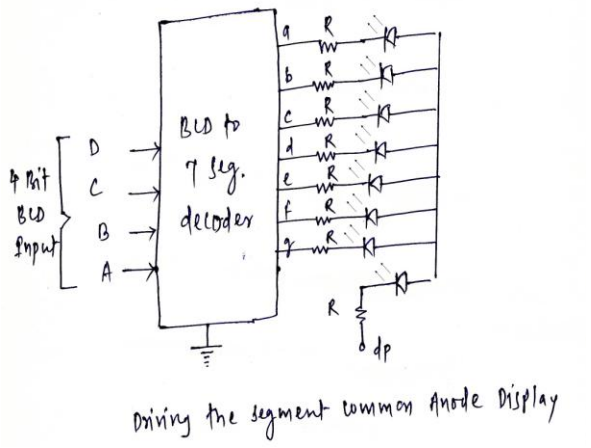
$Y = AB\overline{C}D + A\,\overline{B}\,\overline{C}\,D + ABCD + ABC\overline{D} + AB\overline{C}D + AB\overline{C}\,\overline{D} + \overline{A}\,BCD + \overline{A}\,BC\overline{D} + \overline{A}B\overline{C}D + \overline{A}B\overline{C}\,\overline{D}$ …

{since A + A = A} (2 marks)

f) Explain BCD to 7 segment Decoder

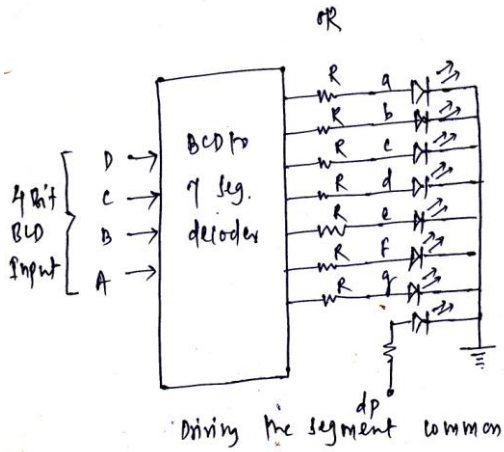
Ans:-

- The use of BCD to 7 segment decoder for driving the seven segment display.
- Most of the times the seven segment LED displays are connected at the output of display IC's such as counters.
- Counter output is in BCD form which has four lines it cannot drive the seven segment display directly.
- Therefore we have to use BCD to 7- segment decoder IC between the counter output and the seven segment display.
- The decoder accepts the four bit BCD counts from counter and converts it to a seven bit code suitable for the seven segment display which is used to drive the display as shown in following figure.



Driving the segment common Anode Display

OR



Driving the segment common cathode display

Q4 Attempt any four of the following (4 * 4 = 16)

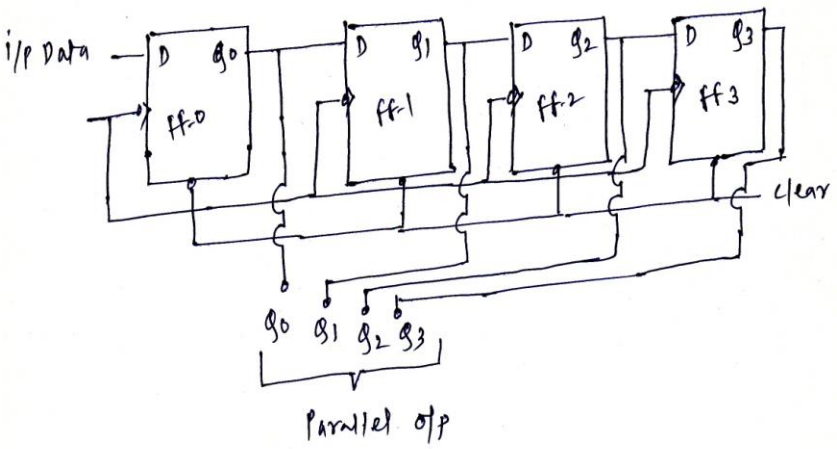
a) What is race around condition? How to eliminate it?

Ans:-

- In level triggered J – K flip flop as long as J = K = 1and CLK = 1, the outputs will keep toggling indefinitely. This multiple toggling in J – K latch is called as race Around Condition.
- The race around condition can be avoided using edge triggered JK flip flop or using master slave JK flip flop.

b) Explain 4 bit SIPO shift register with the help of block diagram, truth table and timing diagram?

Ans:- 4 - bit SIPO shift Register



Explanation:-

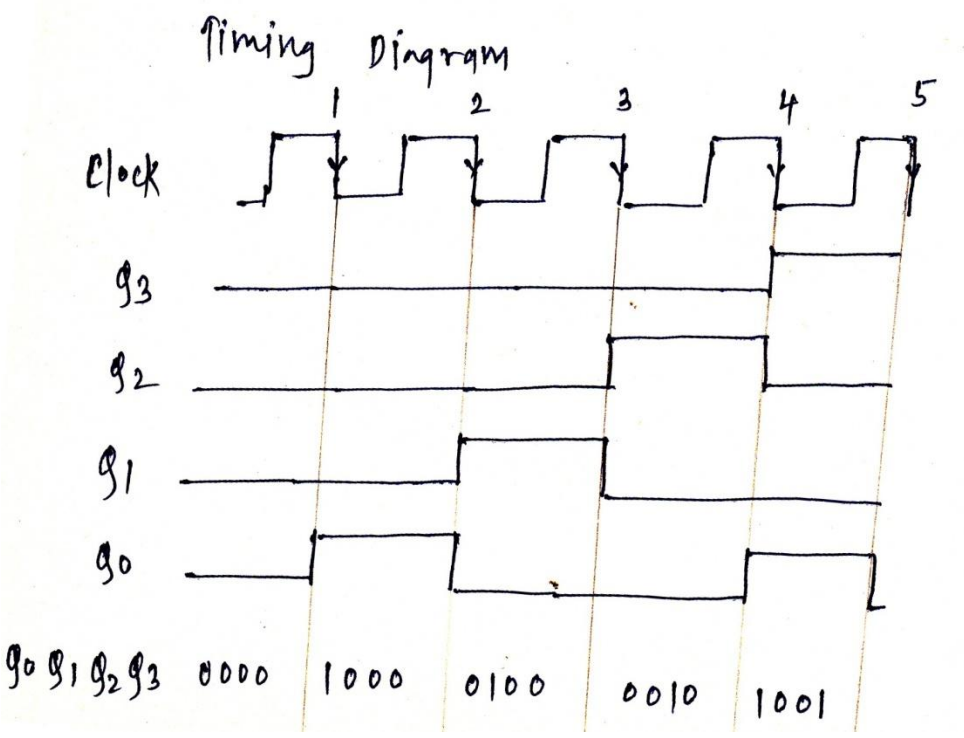
- In this method data is entered in serial manner & o/p has to be taken in parallel manner.
- It means there are two stages namely loading & shifting.

- The o/p of flip flop are disabled while the data is to be loaded.
- As soon as loading is finished all the flip flop have their required data at their i/ps.
- Now the o/p are enabled so that all the loaded data is made available at the outputs simultaneously.

Assume i/p data is 1001

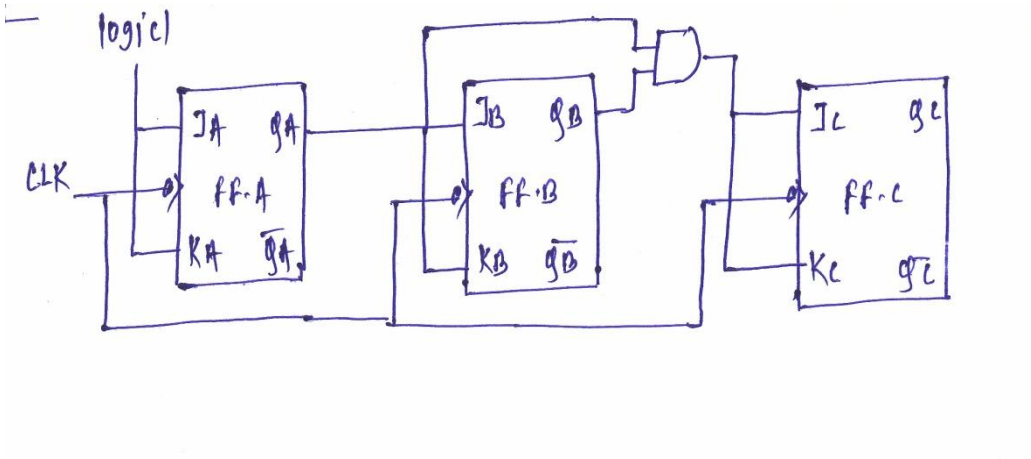
Truth Table :-

CLK	i/p	Q_0	Q_1	Q_2	Q_3
Initially	0	0	0	0	0
1^{st}	1	1	0	0	0
2^{nd}	0	0	1	0	0
3^{rd}	0	0	0	1	0
4^{th}	1	1	0	0	1



c) Explain 3 bit synchronous counter?

Ans:-

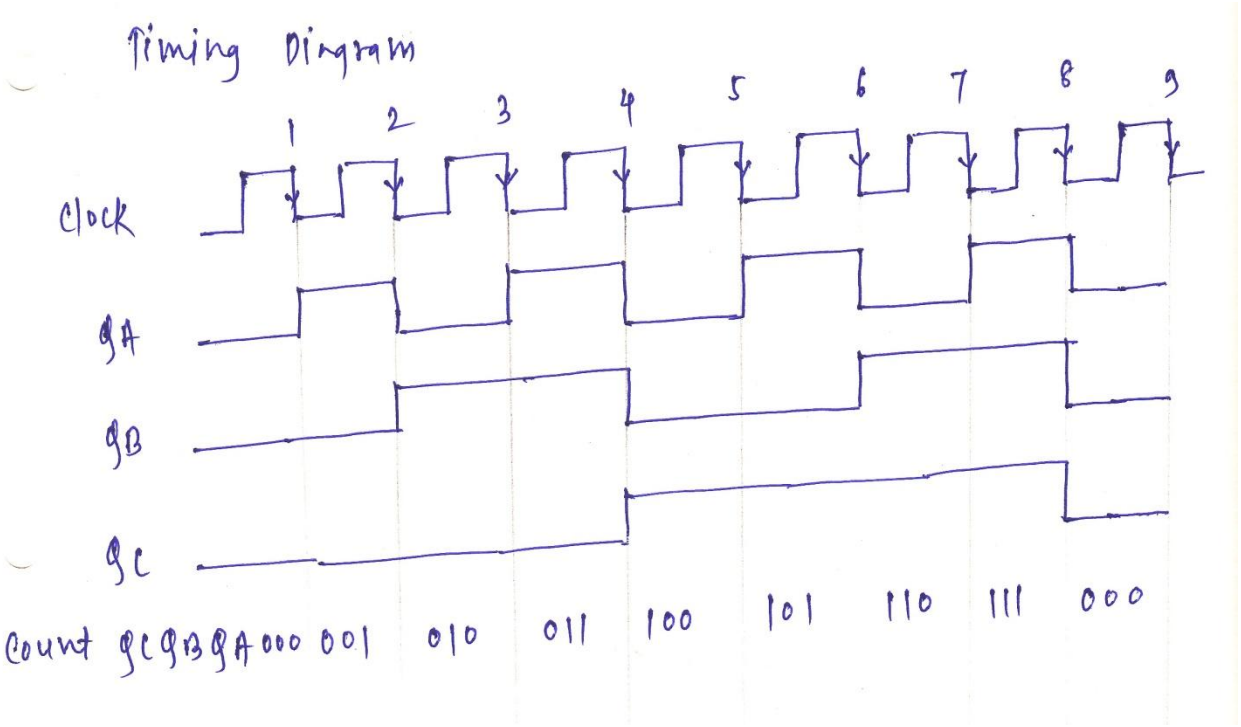


Truth table for 3 bit synchronous up counter

Clock	Q_C	Q_B	Q_A	Decimal equivalent of counter o/p
Initially	0	0	0	0
1st (↓)	0	0	1	1
2nd (↓)	0	1	0	2
3rd (↓)	0	1	1	3
4th (↓)	1	0	0	4
5th (↓)	1	0	1	5
6th (↓)	1	1	0	6

7th (↓)	1	1	1	7
8th (↓)	0	0	0	0

Timing Diagram:-



Explanation :-

1) Initially Q_C Q_B Q_A = 000
2) During 1st negative going clock edge hits flip flop – A it will toggle as TA = 1, therefore Q_A = 1. But Q_A is connected to the clock i/p of flip flop/B as Q_A changes from 0 to 1 so that flip flop – B will be disabled. Hence the o/p of flip flop B will not change. Therefore Q_B = 0. Similarly flip flop C is also disabled, therefore Q_C = 0. So finally o/p of the flip flop are as Q_C Q_B Q_A = 001
3) In the similar way as per clock signal & the i/p of the respective flip lop the o/p of the flip flop will be toggle or no change.
4) Hence , we will get the o/p as per the truth table shown

d) Explain the types of triggering methods?

Ans:- There are two types of triggering methods

A) Level triggering method

B) Edge triggering method

1. Level Triggering :- The flip flop circuits which respond to their inputs only if their enable input (E) held at an active High or Low level are called level triggering flip flop

Level triggering method has two types:-

i) Positive level triggering 

ii) Negative level triggering 

2. Edge triggering :- The flip flop circuits which generally samples its inputs & changes its output only at particular instants of time

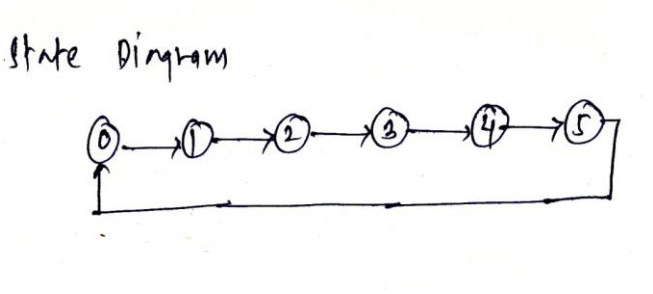
Edge triggering method has two types

i) Positive edge triggering 

ii) Negative edge triggering 

e) Design mod – 6 asynchronous counter

Ans:- State Diagram: (1 mark)

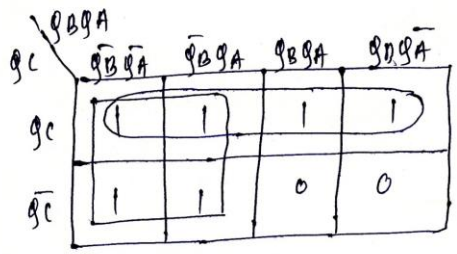


Truth Table for reset logic (1 mark)

Flip flop output				Output (Y) of reset logic
State	Q_C	Q_B	Q_A	
0	0	0	0	1
1	0	0	1	1
2	0	1	0	1
3	0	1	1	1
4	1	0	0	1
5	1	0	1	1
6	1	1	0	0
7	1	1	1	0

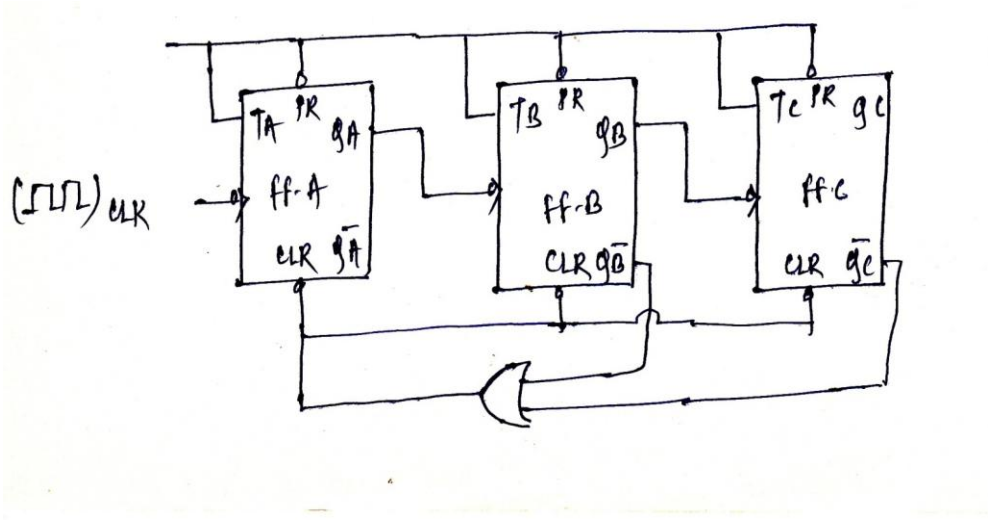
K- map Simplification For Output (Y) (1 mark)

K-map simplification for Reset logic o/p (Y)



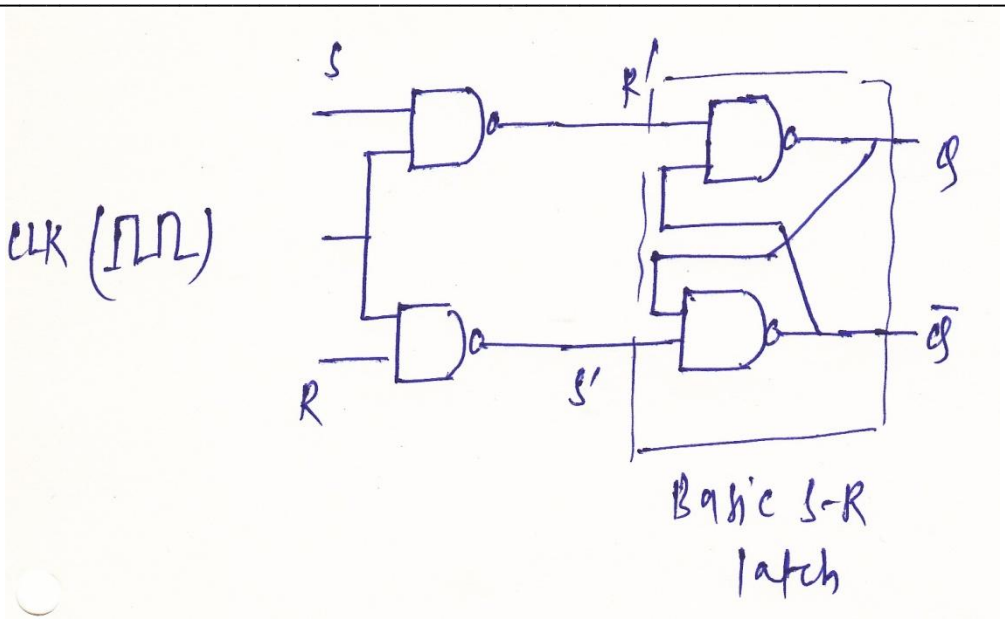
$Y = \bar{Q}_C + \bar{Q}_B$

Logic Diagram (1 mark)



f) Explain clocked SR flip flop using NAND gate?

Ans:-



(2 marks)

Truth table of clocked S – R flip flop (2 marks)

Clock	S	R	$Q_N + 1$	$\overline{Q_n} + 1$	Comments
1	0	0	Q_N	$\overline{Q_n}$	No change
1	0	1	0	1	Reset
1	1	0	1	0	Set
1	1	1	Interminate		Avoid this condition

Explanation :-

1) When S = R = 0, CLK = 1

   If S = R = 0, then output of NAND gates are 1 therefore S' & R' both are 1. These i/p are of basic S – K flip flop using NAND gates, So there will be no change in state of outputs.

2) When S = 0 & R = 1, CLK = 1

   As S = 0, R = 1 then R' = 1 & S' = 0 so the o/p of the SR flip flop are as Q = 0& $\bar{Q}$ = 1

3) When S = 1 & R = 0, CLK = 1

   As S = 1, R = 0 then R' = 0 & S' = 1 so the o/p of the S - R flip flop are as Q = 1 & $\bar{Q}$ = 0

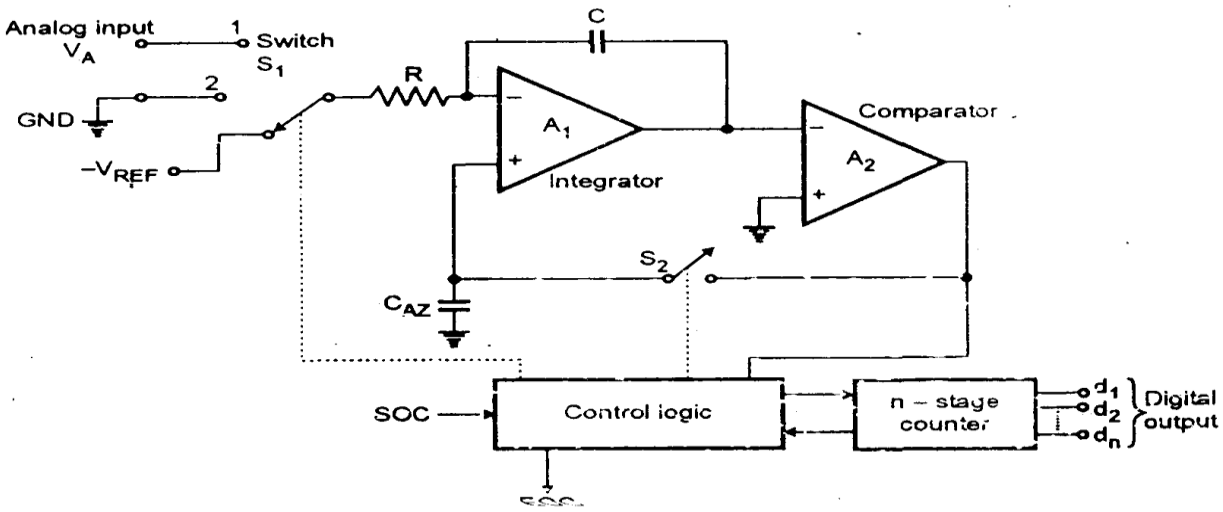
4) When S = 1 & R = 1, CLK = 1

As S = 1, R = 1 then R' = 0 & S' = 0 so then the o/p of the S - R flip flop are in the interminate state.

Q5 Attempt any four of the following

a. Explain dual slope ADC?

Ans. Diagram 2



2

The dual slope ADC consists of OPAMP's being used as integrator and comparator. The control

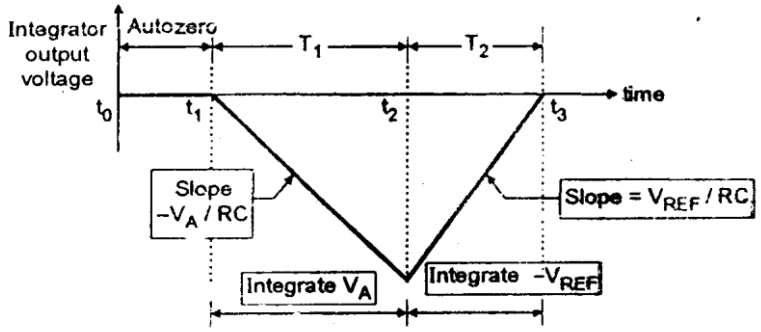
logic accepts the SOC signal and generates EOC signal when the conversion is over. It also controls the two switches S1 and S2 out of which S1 is a single pole three way switch whose one terminal is connected to analog voltage V_A, second one is connected to ground and the third one is connected to a negative reference voltage - $V_{REF.}$

At the out Initially assume that the integrator output voltage V_0= 0 and the counter is in RESET condition i.e. counter output is 00.

1. At t = t_0 switch S1 is connected to ground and switch S2 is closed. The capacitor C_{AZ} gets connected across the comparator output
2. Any offset voltage present in the OP-AMPs will appear across the capacitor C. This will provide an automatic compensation for the input offset voltage of all the amplifiers. Therefore integrator output voltage is zero for the interval t_0 to t_1
3. At instant t_1 the SOC command is given to the control logic. Switch S1 is connected to VA and Switch S2 is open circuited. C_{AZ} acts as a memory to hold the voltage required to keep the offset zero. Hence C_{AZ} is known as the autozero capacitor.

4. From t_1 to t_2 ,this ADC will integrate the analog input VA, for a fixed duration of clock cycles. This time interval is requited for the counter to advance through all its possible output states, because for an n-bit counter there will be 2^n possible output states.
5. The counter output then reduces to zero. The time duration t_1 to t_2 t is represented by T1.The integrator output during this period is given by,

$$V_o = -\frac{1}{RC}\int_{t_1}^{t_2} V_A\,dt = \frac{-V_A T_1}{RC}$$



6. This expression represents a straight line with a slope of - VA / RC. Thus we get a decreasing ramp. The time period T is thus represented by 2^n clock cycles.
   $T = 2^n \times T$ where T = One clock cycle period
7. At the end of interval T_1 the integrator input is connected to a fixed negative reference voltage ($-V_{REF}$) via switch S1
8. The integrator output now starts increasing towards zero with positive slope. The slope of the line is V_{REF} / RC for the duration t_2 to t_3.
9. The counter starts counting from 0. The integration will continue till the integrator output is non-zero. At instant t_3 the integrator output reduces to zero then the comparator output goes from HIGH to LOW and the clock pulses given to the counter are stopped.
10. At t_3. the counter output shows a number corresponding to N clock cycles it has counted during period t_2 to t_3.
11. Thus this number N represents the time taken for integrator output to reduce from -VA to 0. Hence N represents the desired digital output code proportional to the analog input VA.
12. If VA increases, then the integrator capacitor vi1l charge to a higher negative voltage during the time interval T Therefore the time T required to reduce the integrator output to zero increases.
13. Therefore the counter output count (N) will be higher. Thus N is proportional to VA.

put of the counter we get the n-bit digital output..

b. Compare Static and Dynamic RAM

Ans *(Any 4 Points- 1 mark for each point)*

No.	SRAM	DRAM

1	Each SRAM cell is a flip flop	Each DRAM consists of MOSFET and capacitor
2	The number of components per unit is more	The number of components per unit is less
3	Refreshing of memory is not required	Refreshing of memory is required
4	Costly to implement	Less costly to implement
5	Power consumption is less	Power consumption is more
6	Memory is fast	Memory is slow

c. Explain EPROM **4**

Ans.

- EPROM stands for Erasable Programmable Read Only Memory.
- An EPROM is reprogrammable, i.e. it can be programmed again and again.
- Once programmed, the EPROM is non-volatile memory,that holds stored data indefinitely.
- EPROM can be erased by exposure to strong ultraviolet light typically for 20 minutes or longer.
- It can then be rewritten with the help of EPROM programmer by applying higher voltage than usual.
- The programming process is usually performed by EPROM programmer which is separate from the circuit in which an EPROM will be used.
- EPROMs are also called as ultraviolet light erasable PROM (UVPROM). EPROMs are easily identified due to the presence of the transparent quartz window in the top of the package, through which a silicon chip can be seen, and which permits ultraviolet light during erasing.
- A programmed EPROM retains its data for about ten to twenty years and can be read an unlimited number of times. The erasing window must be kept covered with a foil label to prevent accidental erasure by sunlight.

Disadvantages

1. The erase operation erases the entire chip, even if change is required for a single byte.
2. The entire chip is required to be reprogrammed even if one byte is required to be reprogrammed.

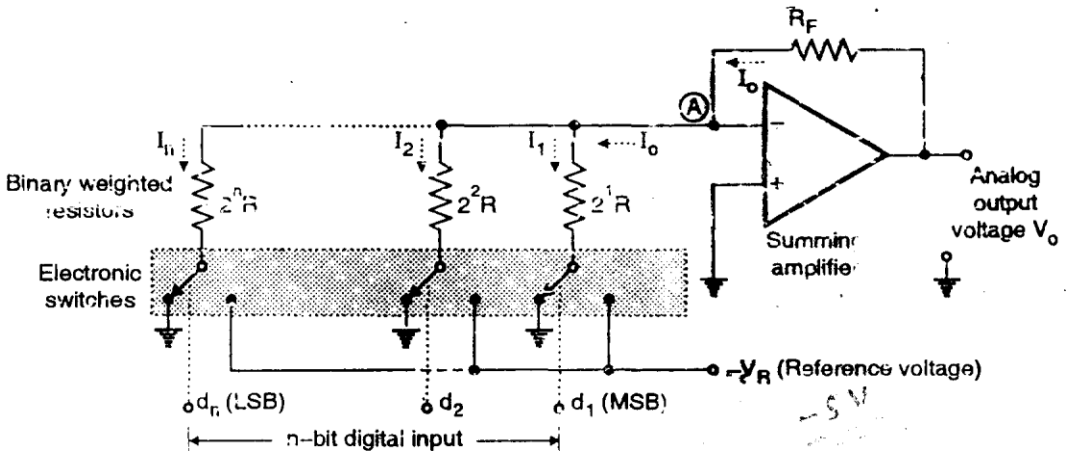
3. The erase and reprogramming processes typically take 20 minutes or more.
4. EPROMs are required to be removed from their circuit to be erased and reprogrammed.

Advantages

1. Reprogrammable
2. More reliable
3. Less expensive

d) Explain weighted resistor DAC

Ans Diagram. 2



CONSTRUCTION and WORKING **2**

1. This circuit uses a network of binary weighted resistors (i.e 2^1R, 2^2R… 2^nR) and a summing amplifier.
2. There are "n" number of electronic switches used, one per digital bit. They are single pole double throw (SPDT) type switches.
3. The switch when connected to ground the input provided is '0' while connected to negative reference voltage ($-V_R$) and when the binary input is '1'
4. Depending on the positions of various switches, the currents will start flowing through the resistors 2^1R, 2^2R… 2^nR.
5. The op-amp is used as summing amplifier to convert the current to voltage

Let the n-bit digital input word to the DAC be $d_1d_2 \ldots d_n$ with d_1 as MSB (most significant bit) and d_n as LSB (least significant bit).Let R_F be the feedback resistor and Io be the output current. Assume the Op-amp to be an ideal OP-AMP so that the current flowing between its input terminals is zero.

$$I_o = I_1 + I_2 + \ldots\ldots + I_n = \frac{V_R}{2R} d_1 + \frac{V_R}{2^2 R} d_2 + \ldots\ldots + \frac{V_R}{2^n R} d_n$$

The output current Io is the sum of individual currents through the weighted resistors.

$$I_o = \frac{V_R}{R}\left[d_1 2^{-1} + d_2 2^{-2} + \ldots\ldots + d_n 2^{-n} \right]$$

The output voltage Vo is given by,

$$V_o = I_o R_F = V_R \cdot \frac{R_F}{R}\left[d_1 2^{-1} + d_2 2^{-2} + \ldots\ldots + d_n 2^{-n} \right]$$

This is the required expression for output voltage.

Now comparing Equalioits (9.2.4) and (9.4.3), we can conelude that,

$$K = \frac{R_F}{R} \quad \text{and} \quad V_{FS} = V_R$$

So if $R_F = R$ then $K = 1$.

$$V_o = V_R\left[d_1 2^{-1} + d_2 2^{-2} + \ldots + d_n 2^{-n} \right]$$

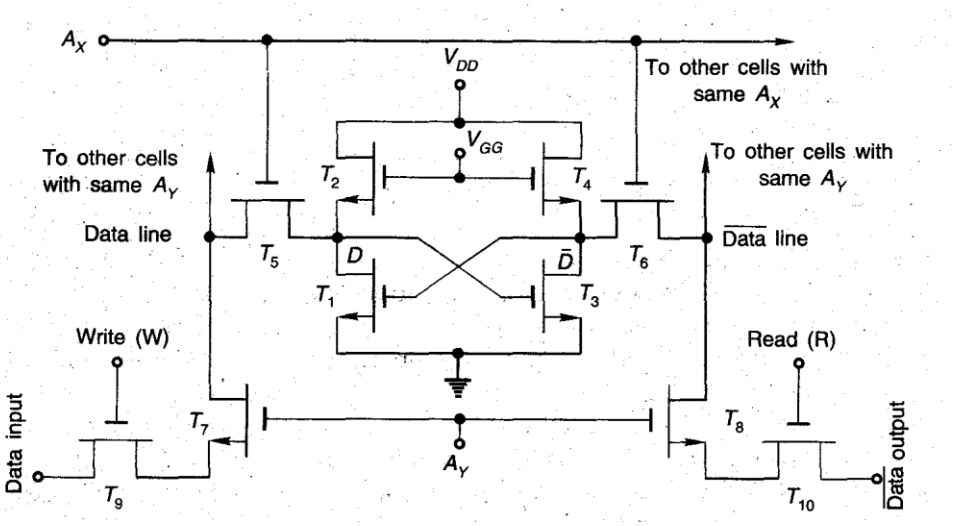
Let the 3-bit digital input word to the DAC be $d_1d_2d_3$.d_1 is the MSB and d_3 is the LSB.

$$Vo = V_R [\ d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3}]$$

Digital input			Analog output voltage V_o
d_1	d_2	d_3	
0	0	0	0
0	0	1	$V_R / 8$
0	1	0	$2 V_R / 8$
0	1	1	$3 V_R / 8$
1	0	0	$4 V_R / 8$
1	0	1	$5 V_R / 8$
1	1	0	$6 V_R / 8$
1	1	1	$7 V_R / 8$

e) Draw and explain static RAM using CMOS transistor **2**

Ans. Note:- The basic SRAM explained with the help of diagram should be considered



2

- A RAM memory cell consist of two cross-coupled MOS inverters.
- It addressed by setting Ax and Ato.1. When A= 1, the cell is connected to the data and daL. 1ine.WhenA=1, T7 and T8 are ON.
- To write into the cell, set W = 1, T9 then becomes ON. If data input is 1, the voltage at node D will correspond to level 1 making T3 ON and level at D will be 0.
- On the other hand, if the data input is at logic 0, then T3 will be OFF and D would be at 1. To read the state of the FLIP-FLOP, we set R= 1.
- This connects the data output to D .
- Thus, the complement of the data level written into the cell is read at data output

f) The LSB of 3-bit DAC represent 02 V What value of voltage will be represented by following binary words? i100, ii) 110

Ans.

Let the 3-bit digital input word to the DAC be $d_1d_2d_3$.d_1 is the MSB and d_3 is the LSB.

$$Vo= V_R [d_1 2^{-1}+ d_2 2^{-2} + d_3 2^{-3}]$$

The LSB intends the smallest change i.e the RESOLUTION is 0.2 V

Therefore the output for (001)is 0.2 V

$$V_R = Vo / [\ d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3}]$$

$$= 0.2V/ (0X 2^{-1} + 0X2^{-2} + 1X2^{-3}) = 1.6\ V$$

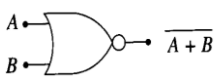
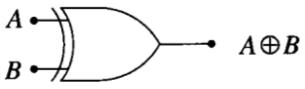
4

OUTPUT for BINARY value of 100	OUTPUT for BINARY value of 110
$V_0 = VR . [\ d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3}]$ $=1.6\ X(1X\ 2^{-1} + 0X2^{-2} + 0X2^{-3}) = 0.8\ V$	$V_0 = VR . [\ d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3}]$ $=1.6\ X\ (1X\ 2^{-1} + 1X2^{-2} + 0X2^{-3}) = 1.2\ V$

2. Attempt any four of the following: . . (4x4=16)

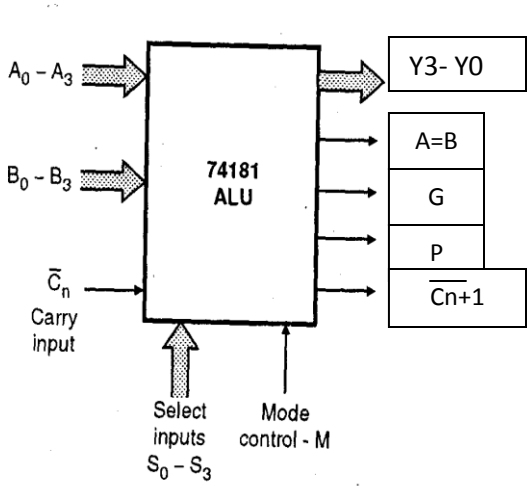
a. Draw symbol, logical equation, truth table and TTL IC used for I. 2i/p EX-OR and N0R gate

Ans. *(1/2 Mark for each correct information)*

Logic Gate	**NOR GATE**	**EX-OR GATE**
SYMBOL		
LOGICAL EQUATION	**Y= A+B**	$A \oplus B = A \cdot \bar{B} + \bar{A} \cdot B$
TRUTH TABLE	A B $\overline{A+B}$ 0 0 1 0 1 0 1 0 0 1 1 0	A B $A \oplus B$ 0 0 0 0 1 1 1 0 1 1 1 0
TTL IC used	7402	7486

b. Explain ALU IC 741B1 with neat diagram

Ans. *(Block Diagram – 2 Marks+ Explanation of Block Diagram/ Function Table – 2 Marks)*



- 74181 is a 24-pin IC in dual in line (DIP) package.
- A (A0 — A3 and B (B0 — B3) are the two 4 bit variables.
- It can perform a total of 16 arithmetic operations which includes addition, subtraction, compare and double operations. It provides many logic operations such as AND, OR, NOR, NAND, EX-OR, compare, etc. on the two four bit variables.
- 74181 is a high speed 4 bit parallel ALU.
- It is controlled by four function select inputs(S0 — S3). These lines can select 16 different operations for one mode (arithmetic) and 16 another operations for the other mode (logic). M is the mode control input. It decides the mode of operation to be either arithmetic or logic.
- Mode M= 0 For arithmetic operations.
- M = 1 For logic operations.
- G and P outputs are used when a number of 74181 circuits are to be used in cascade alongwith 74182 the look ahead carry generator circuit to make the arithmetic operations faster.

Functional Table

Function Select Inputs				Active high data and $\bar{C}_n = 1$	
S_3	S_2	S_1	S_0	Logic operations (M = 1)	Arithmetic operations (M = 0)
0	0	0	0	$F = \bar{A}$ (Inversion)	F = A
0	0	0	1	$F = \overline{A + B}$ (NOR)	F = A + B
0	0	1	0	$F = \bar{A} \cdot B$	$F = A + \bar{B}$
0	0	1	1	F = 0	F = minus 1 (2's comp)
0	1	0	0	$F = \overline{AB}$ (NAND)	$F = A$ plus $A\bar{B}$
0	1	0	1	$F = \bar{B}$ (Invert)	$F = (A + B)$ plus $A\bar{B}$
0	1	1	0	$F = A \oplus B$ (EXOR)	F = A minus B minus 1
0	1	1	1	$F = A\bar{B}$	$F = A\bar{B}$ minus 1
1	0	0	0	$F = \bar{A} + B$	F = A plus AB
1	0	0	1	$F = \overline{A \oplus B}$ (EXNOR)	F = A plus B
1	0	1	0	F = B	$F = (A + \bar{B})$ plus AB
1	0	1	1	F = AB (AND)	F = AB minus 1
1	1	0	0	F = logic 1	F = A plus A *
1	1	0	1	$F = A + \bar{B}$	$F = (A + B)$ plus A
1	1	1	0	F = A + B (OR)	$F = (A + \bar{B})$ plus A
1	1	1	1	F = A	F = A Minus 1

C. Determine the frequency at the output of last (MSB) flip-flop for an. input clock frequency of 2 MHz.

Ans.

Note:-Since no of flip flops are not provided, the student can assume any 2/3/4/8 flip flops. However the solution is solved using 4 flip flops in asynchronous mode. However assumption to be awarded suitable marks

Consider a 4 bit flip flop for asynchronous counter with a clock of 2 MHz. 4

The LSB flip flop (FF0) is divide by 2 (÷2) = 1 MHz

The next flip flop (FF1) is divide by 4 (÷4) = 0.5 MHz

The next flip flop (FF2) is divide by 8 (÷8) = 0.25 MHz

The MSB flip flop (FF3) is divide by 16 (÷16) = 0.125 MHz

. **Write advantages and disadvantages of dynamic RAM.**

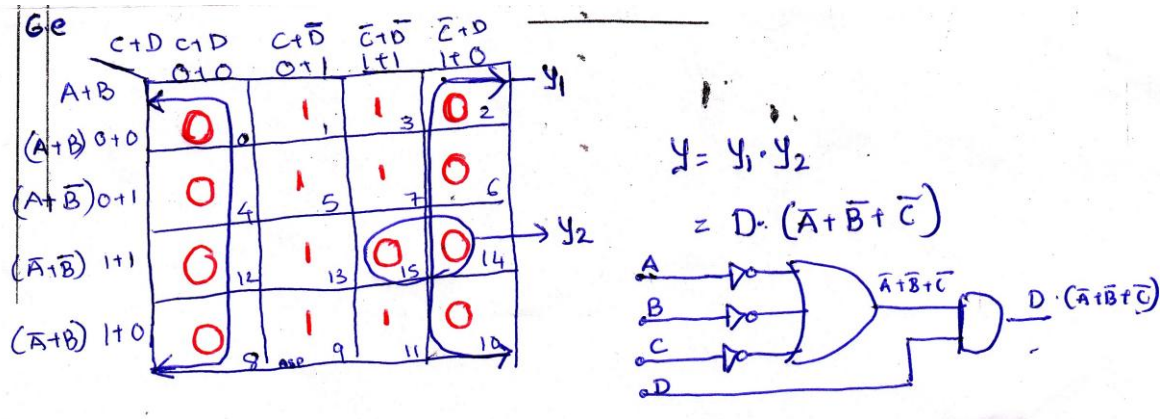
Ans.

- **Advantages of DRAM** 2
  - Each DRAM consists of MOSFET and capacitor .
  - The number of components are less.
  - Less costly to implement per unit is less
- **Disadvantages of DRAM** 2
  - Refreshing of memory is required
  - Power consumption is more
  - Memory is slow

e. Solve using kmap and realize it. F(v, x, y, z) = π M (0, 2, 4, 6, 8, 10, 12, 14, 15)

Ans.

(2 marks for K-Map+ 1 mrk for Equation +1 mark for circuit diagram)



f) Define specifications of ADC.

Ans.

(Any 4 Specifications- 1 mark for each correct specification)

Resolution

The resolution of an ADC is defined in two ways

1. Resolution is defined as the maximum number of digital output codes.

   Resolution = 2^n

2. Resolution can also be defined as the ratio of the change in the value of the input analog voltage V_A required to change the digital output by 1 LSB.

$$\text{Resolution} = \frac{V_{FS}}{2^n - 1}$$

Conversion Time

1. It is the total time required to convert the analog input signal into a corresponding digital output
2. The conversion time depends on the conversion technique used for an ADC. The conversion time is also dependent on the propagation delays introduced by the circuit components.
3. Conversion time should ideally be zero and practically be as small as possible.

Quantization Error

1. This approximation process is called as quantization and the error due to the quantization process is called as quantization error.
2. The maximum value of quantization error is ± 1/2 LSB.
3. The quantization error should be as small as possible. It can be reduced by increasing the number of bits. The increase in number of bits also improves the resolution.

Linearity

1. The relation between the analog input and digital output should be linear.

Temperature sensitivity

1. The digital output voltage of A to D converter should not change due to changes in temperature. But practically the output is a function of temperature. It is so because the resistance values and OPAMP parameters change with changes in temperature.