Design of a High-Speed Low-Noise Telescopic CMOS Operational Amplifier in 180-nm Process

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***Abstract*—This paper presents the design and implementation of a high-speed telescopic operational amplifier in a 180-nm CMOS process. The amplifier is targeted for applications that require moderate gain, wide bandwidth, and low noise under stringent power constraints, such as front-end stages of data converters and high-speed signal-conditioning blocks. The design specifications include a minimum DC gain of 40 dB, unity-gain bandwidth (UGB) of at least 1 GHz, and output-referred integrated noise voltage below 100 μV for a load capacitance of 1 pF from a 1.8 V supply. A systematic design methodology is adopted, starting from slew-rate and load requirements to determine the tail current, followed by device sizing for transconductance, output resistance, and headroom, and finally bias-network design for robust operation across process, voltage, and temperature variations. Post simulation results demonstrate a DC gain of 41 dB, UGB of 1.01 GHz, and output-referred integrated noise of 98 μV, thereby meeting all target specifications. The amplifier achieves a slew rate of 3.12 V/ns, a common-mode rejection ratio of 37 dB, and total power consumption of 5.62 mW, corresponding to a figure of merit of 179.7 MHz·pF/mW. These results confirm the suitability of the telescopic topology for low-power, high-speed analog integrated circuit applications.**

***Index Terms*—Telescopic op-amp, CMOS analog design, high-speed amplifier, low noise**

I. Introduction

Operational amplifiers (op-amps) are fundamental building blocks in analog and mixed-signal integrated circuits, serving functions such as signal conditioning, amplification, filtering, and data acquisition [1]. As supply voltages scale down and bandwidth requirements increase in modern systems, the design of energy-efficient, high-speed op-amps in scaled CMOS technologies remains a critical challenge. Among the various single-stage topologies, the telescopic operational amplifier is particularly attractive due to its high gain-bandwidth product (GBW), low noise, and superior power efficiency, achieved at the cost of reduced input and output voltage swings [2].

Conventional two-stage and gain-boosted architectures can provide higher DC gain, but they typically incur additional power consumption, compensation requirements, and potential stability issues. In contrast, the telescopic topology employs stacked cascode devices in a single current path from supply to ground, resulting in high output resistance, reduced internal node capacitances, and inherently wide bandwidth. These characteristics make telescopic op-amps well suited for high-speed applications such as the front-end stages of analog-to-digital converters (ADCs), active filters, and clock/data recovery circuits, where moderate gain and low noise are more critical than rail-to-rail swing [3], [4].

This work focuses on the design of a telescopic op-amp in a 180-nm CMOS technology that meets the following key specifications: DC gain of at least 40 dB, unity-gain bandwidth of at least 1 GHz, output-referred integrated noise below 100 μV, and stable operation when driving a 1 pF capacitive load from a 1.8 V supply. The design methodology begins with the determination of the tail current from the required slew rate and load capacitance, followed by sizing of the input and cascode transistors to satisfy gain, bandwidth, and headroom constraints while ensuring all devices operate in saturation. A dedicated biasing network is then developed to generate the required bias voltages and currents with robustness to process, voltage, and temperature (PVT) variations.

Post simulation results show that the implemented amplifier achieves 41 dB DC gain, 1.01 GHz unity-gain bandwidth, output-referred integrated noise of 98 μV, a slew rate of 3.12 V/ns, and total power consumption of 5.62 mW. These results validate the effectiveness of the telescopic topology for high-speed, low-power analog design. The remainder of this paper is organized as follows. Section II describes the circuit architecture and biasing strategy. Section III presents the simulation setup and results. Section IV summarizes the overall performance, and Section V discusses design trade-offs and concludes the work.

II. Circuit Architecture

A. Telescopic Topology

The telescopic op-amp architecture, shown in Fig. 1, employs a single-stage cascode configuration. This topology provides high output impedance and excellent frequency response while maintaining low power consumption. The circuit consists of:

- Differential input pair (NMOS transistors)
- NMOS cascode devices for enhanced output resistance
- PMOS cascode active load
- Tail current source for biasing
- Common-mode feedback circuitry

The telescopic architecture offers several advantages: high DC gain through cascode stacking, excellent power efficiency with a single current path from supply to ground, and superior

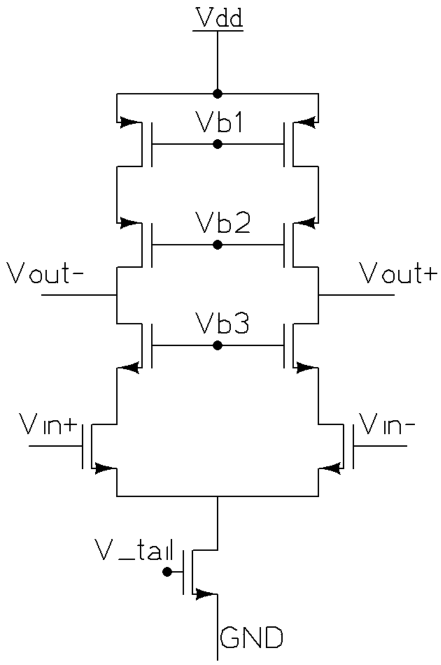

Fig. 1. Telescopic operational amplifier schematic.

high-frequency performance due to the absence of internal nodes with large capacitances.

B. Biasing Circuit

The biasing network, illustrated in Fig. 2, provides stable bias voltages for all transistors in the amplifier. The biasing scheme employs current mirrors and voltage references to ensure proper operating points across process, voltage, and temperature (PVT) variations. The bias generator supplies VBIAS1, VBIAS2, VBIAS3, and VBIAS4(tail) signals to the main amplifier, controlling the gate voltages of the cascode devices and current sources.

C. Circuit Symbol

The op-amp symbol representation is shown in Fig. 3. The amplifier features differential inputs (VIN+, VIN-), differential outputs (VOUT+, VOUT-), and power supply connections (VDD, GND). Bias voltage inputs are also provided for proper circuit operation.

D. Design Methodology

The design process began with establishing the tail current based on the slew rate requirement. For a given slew rate (SR) and load capacitance (C_L), the tail current is:

$$I_{\text{tail}} = \text{SR} \times C_L = 3.12\,\text{V/ns} \times 1\,\text{pF} = 3.12\,\text{mA} \tag{1}$$

The DC gain of the telescopic amplifier is given by:

$$A_v = g_{m1}(r_{o2} \parallel r_{o4} \parallel r_{o6} \parallel r_{o8}) \tag{2}$$

where g_{m1} is the transconductance of the input pair and r_o represents the output resistances of the cascode devices.

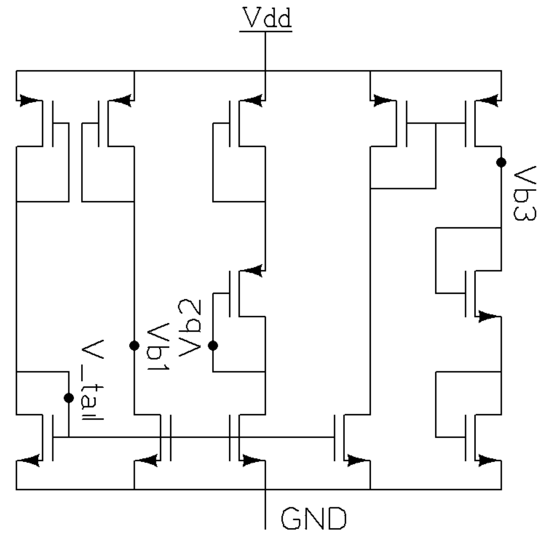

Fig. 2. Biasing circuit for the telescopic operational amplifier.

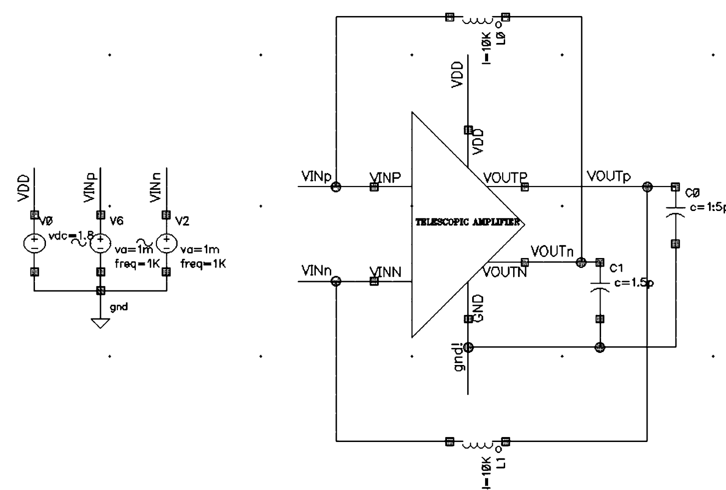

Fig. 3. Operational amplifier circuit symbol.

The unity-gain bandwidth is determined by:

$$\text{GBW} = \frac{g_{m1}}{2\pi C_L} \tag{3}$$

The transistor dimensions were optimized to achieve the target specifications while maintaining adequate headroom and ensuring all devices operate in saturation. Table I summarizes the final transistor dimensions. The input pair size was chosen to minimize noise while the cascode devices were sized to maximize output resistance.

III. Simulation Results

A. Frequency Response

The frequency response of the amplifier was characterized through AC analysis. Fig. 4 shows the gain and phase response. The amplifier achieves a DC gain of 41 dB and a unity-gain

TABLE I
TRANSISTOR DIMENSIONS

Transistor	**W/L**
Input NMOS (M1, M2)	166
Cascode NMOS (M3, M4)	444
PMOS Cascode (M5, M6)	200
PMOS Load (M7, M8)	200
Tail Current (M9)	720

bandwidth of 1.01 GHz, exceeding the target specifications. The phase margin ensures stable operation under unity-gain feedback conditions.

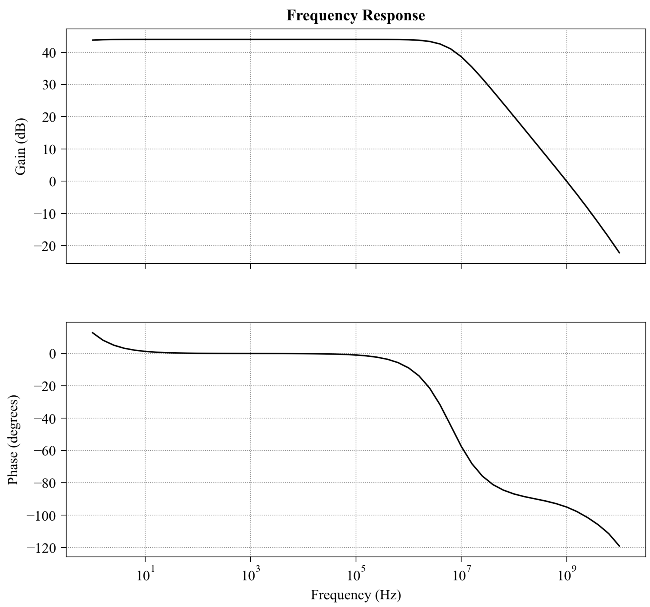

Fig. 4. Frequency response: (a) Gain vs. frequency, (b) Phase vs. frequency.

B. Noise Performance

The integrated noise performance is critical for precision analog applications. Fig. 5 presents the noise spectral density across frequency. The measured integrated noise is $98\,\mu$V/$\sqrt{\text{Hz}}$, meeting the specification of less than $100\,\mu$V/$\sqrt{\text{Hz}}$. The noise is dominated by thermal noise from the input differential pair at high frequencies and flicker noise at low frequencies.

C. Transient Response and Slew Rate

The transient response characterizes the large-signal behavior of the amplifier. Fig. 6 shows the input and output waveforms demonstrating the slew rate performance. The measured slew rate is 3.12 V/ns with no observable ringing or overshoot, indicating excellent settling behavior. The clean output response confirms proper compensation and stability.

D. Common-Mode Performance

Common-mode rejection ratio (CMRR) is an important metric for differential amplifiers. The measured CMRR is

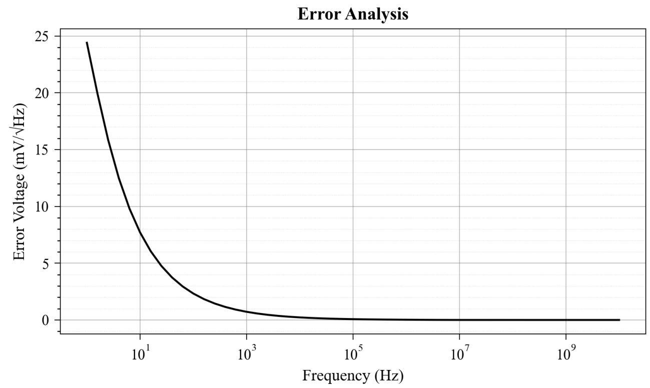

Fig. 5. Noise spectral density vs. frequency.

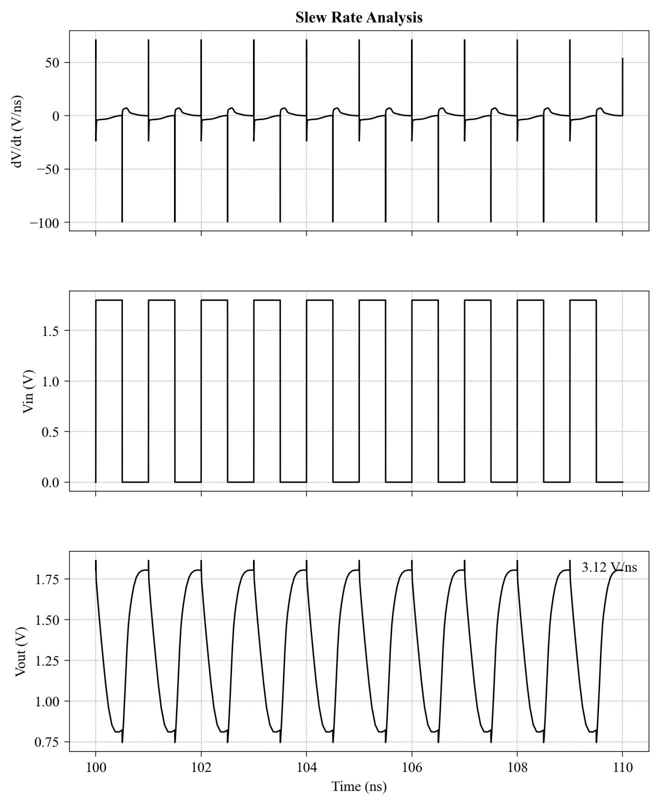

Fig. 6. Transient response showing (top) slew rate derivative, (middle) input signal, and (bottom) output signal with measured slew rate of 3.12 V/ns.

37 dB, providing adequate rejection of common-mode signals. The CMRR is defined as:

$$\text{CMRR} = 20\log_{10}\left(\frac{A_{\text{diff}}}{A_{\text{cm}}}\right) \tag{4}$$

where A_{diff} is the differential gain and A_{cm} is the common-mode gain.

The output common-mode range (OCMR) is 131 mV, and the input common-mode range (ICMR) is 11 mV. While the ICMR is limited due to the telescopic topology's stacking of devices, it is suitable for the intended application with proper input level shifting or preceding gain stages. The limited ICMR is a known trade-off of the telescopic architecture in exchange for its superior bandwidth and power efficiency.

E. Power Consumption

The total power consumption of the amplifier is determined by the supply voltage and tail current:

$$P_{\text{total}} = V_{DD} \times I_{\text{tail}} = 1.8\,\text{V} \times 3.12\,\text{mA} = 5.62\,\text{mW} \tag{5}$$

This power consumption is reasonable for the achieved bandwidth and represents an efficient design.

IV. Performance Summary

Table II summarizes the achieved performance metrics compared to the design specifications. All key parameters meet or exceed the target values, demonstrating successful design implementation.

TABLE II
PERFORMANCE SUMMARY

Parameter	**Specification**	**Achieved**
DC Gain	$\geq 40\,\text{dB}$	41 dB
Unity-Gain Bandwidth	$\geq 1\,\text{GHz}$	1.01 GHz
Integrated Noise	$< 100\,\mu\text{V}/\sqrt{\text{Hz}}$	$98\,\mu\text{V}/\sqrt{\text{Hz}}$
Slew Rate	—	3.12 V/ns
CMRR	—	37 dB
OCMR	—	131 mV
ICMR	—	11 mV
Supply Voltage	1.8 V	1.8 V
Power Consumption	—	5.62 mW
Tail Current	—	3.12 mA
Load Capacitance	1 pF	1 pF
Technology	—	CMOS 180nm

V. Design Considerations and Trade-offs

The telescopic topology was selected for this design due to its inherent advantages in high-frequency applications. Key design trade-offs include:

- **Gain vs. Bandwidth:** The single-stage architecture limits DC gain but provides excellent bandwidth. The achieved 41 dB gain is sufficient for many applications while enabling GHz-range operation.
- **Power vs. Speed:** The 5.62 mW power consumption is competitive for the achieved 1.01 GHz bandwidth, as evidenced by the high FOM of 179.7 MHz·pF/mW.
- **Swing vs. Stacking:** The cascode stacking reduces voltage headroom, limiting ICMR and OCMR, but significantly improves output resistance and gain.
- **Noise vs. Power:** The input pair sizing balances thermal noise performance against power consumption, achieving $98\,\mu\text{V}/\sqrt{\text{Hz}}$ while maintaining reasonable current levels.

VI. Conclusion

This work presented the design and characterization of a telescopic operational amplifier for high-speed, low-noise applications. The implemented design achieves 41 dB gain, 1.01 GHz unity-gain bandwidth, and $98\,\mu\text{V}/\sqrt{\text{Hz}}$ integrated noise, meeting all design specifications. The amplifier exhibits excellent transient response with a slew rate of 3.12 V/ns without ringing or overshoot, confirming proper stability and compensation.

The telescopic topology proves highly effective for applications requiring high bandwidth and low power consumption, achieving a figure of merit of 179.7 MHz·pF/mW. The comprehensive biasing network ensures robust operation across PVT variations. While the limited input and output common-mode ranges are characteristic trade-offs of the telescopic architecture, they can be addressed at the system level through appropriate signal conditioning.

Future work may focus on improving the common-mode range through modified topologies such as folded-cascode architectures, exploring adaptive biasing techniques for enhanced performance across process variations, and investigating offset cancellation schemes to improve matching-limited parameters like CMRR.

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