Total No. of Questions : 8]

SEAT No. : [ ]

PD4619

[Total No. of Pages : 2

[6404]-125

B.E. (Electronics & Telecommunication Engineering)
VLSI DESIGN & TECHNOLOGY
(2019 Pattern) (Semester - VII) (404182)

Time : 2½ Hours] ***[Max. Marks : 70***

Instructions to the candidates:

1) ***Answer Q.1 or Q.2, Q.3 or Q.4, Q.5 or Q.6, Q.7 or Q.8.***
2) ***Neat diagrams must be drawn wherever necessary.***
3) ***Figures to the right indicate full marks.***
4) ***Use of electronic pocket calculator is allowed.***
5) ***Assume suitable data, if necessary.***

Q1) a) Compare CPLD with FPGA. **[8]**

b) Draw the block diagram of FPGA and explain it in brief. **[9]**

OR

Q2) a) Explain in brief PLD Design flow. **[8]**

b) Draw the block diagram of CPLD and explain it in brief. **[9]**

Q3) a) What is technology scaling? Explain any one type of scaling with its effect at least 4 parameters. **[8]**

b) Explain the working of a transmission gate and implement a circuit of 4:1 MUX using transmission gate. **[10]**

OR

Q4) a) Draw and explain CMOS inverter transfer characteristics. **[6]**

b) Explain : Channel Length Modulation, Body Effect, Velocity saturation. **[12]**

Q5) a) Explain ASIC Design flow. **[6]**

b) Explain DC and transient analysis using SPICE. **[6]**

c) Explain Antenna Effect in brief. **[6]**

OR

Q6) a) Explain LAMBDA rules used for CMOS layout design. **[6]**

b) Write short note on Cross talk. **[6]**

c) Write SPICE code for CMOS invertor for AC analysis. **[6]**

P.T.O.

Q7) a) What is DFT? Explain the need for DFT in brief. **[7]**

b) Explain the following terms with respect to testability: **[10]**

i) Fault coverage

ii) Fault Models

iii) Observability

iv) Controllability

v) Physical Defects

OR

Q8) a) What is need of BIST? Explain typical BIST in detail. **[8]**

b) Explain path sensitizing algorithm in detail. **[9]**

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