Title: Design and Implementation of CMOS NAND & NOR gate

1. **Statement of the Problem:** In this experiment we're going to implement NAND and NOR gate using DSCH and Microwind software.

2. **Hypothesis:** NAND and NOR gates are called the universal gates, all other gates can be implemented using these two gates. The truth tables of NAND and NOR gates are as follows

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Truth Table: NAND Gate

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Truth Table: NOR Gate

Since the PMOS turns off current flow from source to drain if we put a voltage in gate, on the other side the NMOS does the opposite. So, In NAND gate we connect two PMOS in parallel and the drain is connected to the source of the series connection of two NMOS. NMOS drain is connected to ground.

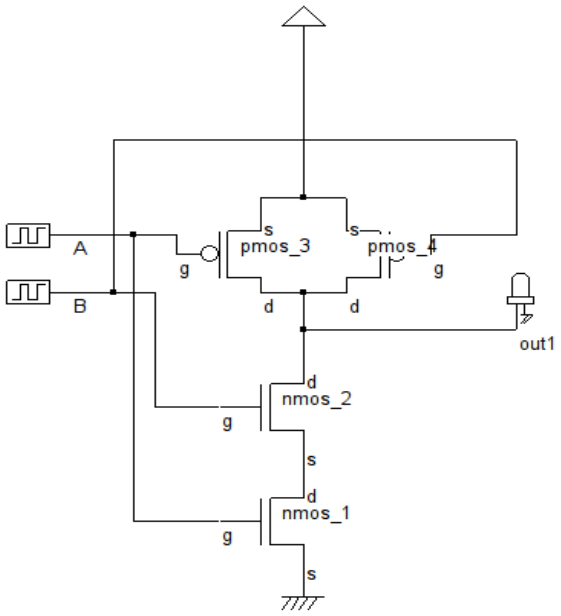
In NOR gate design, we connect two PMOS in series, the drain of PMOS is connected to the Source of two NMOS that are connected in parallel. Output is measured from the poing of PMOS-NMOS connection. The NAND and NOR gate design is shown below with simulation results.

3. **Materials:**
    - DSCH Software
    - Microwind Software
    - Windows/Linux Operating System

4. Procedure:

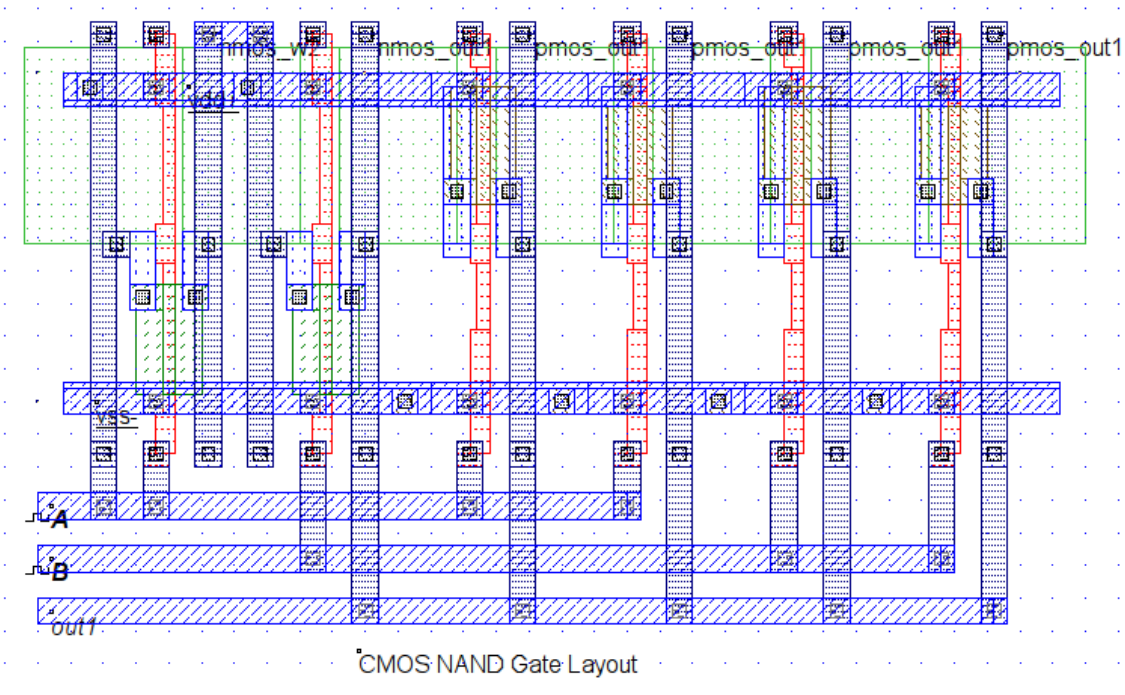
NAND Gate:

Using two PMOS in parallel and two NMOS in series we complete the NAND gate design as bellow, PMOS source is connected to +VDD and drain of NMOS is connected to ground



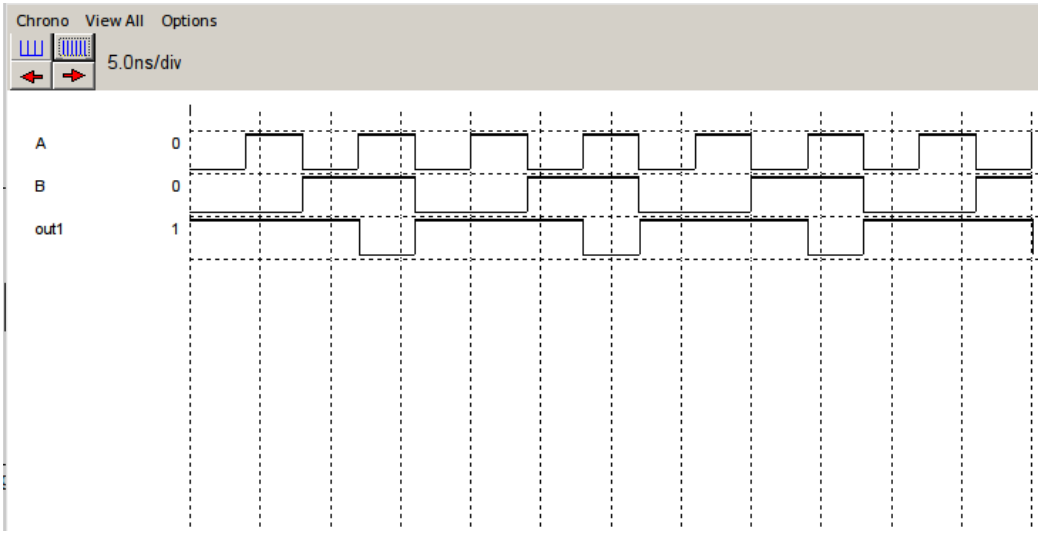
CMOS NAND Gate

Layout Diagram of NAND Gate: Generated by compiling verilog file from NAND gate level diagram in Microwind.



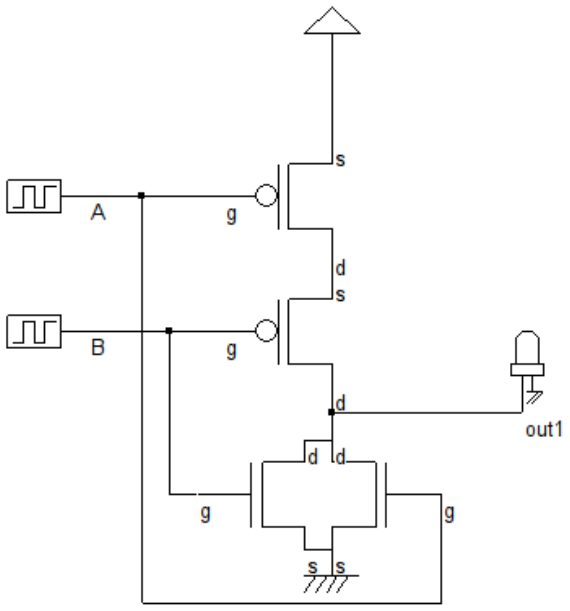
CMOS NAND Gate Layout

Timing Diagram of NAND Gate: Based on the simulation of NAND gate in DSCH



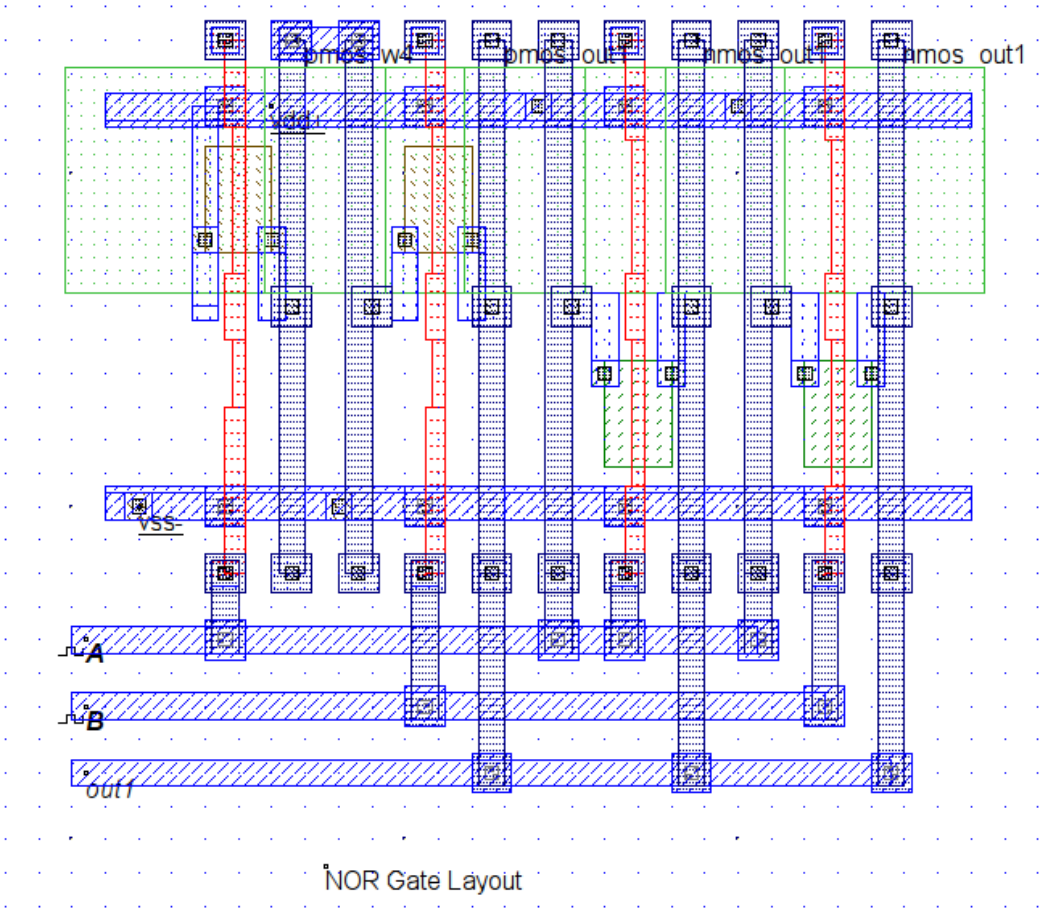
NOR Gate:

In NOR gate we connect two PMOS in series first, +VDD is connected to the source of PMOS, The drain is connected to the two NMOS that are connected in parallel. The Drain of the NMOS is connected to ground. We measure output from the PMOS-NMOS connection point using an LED.

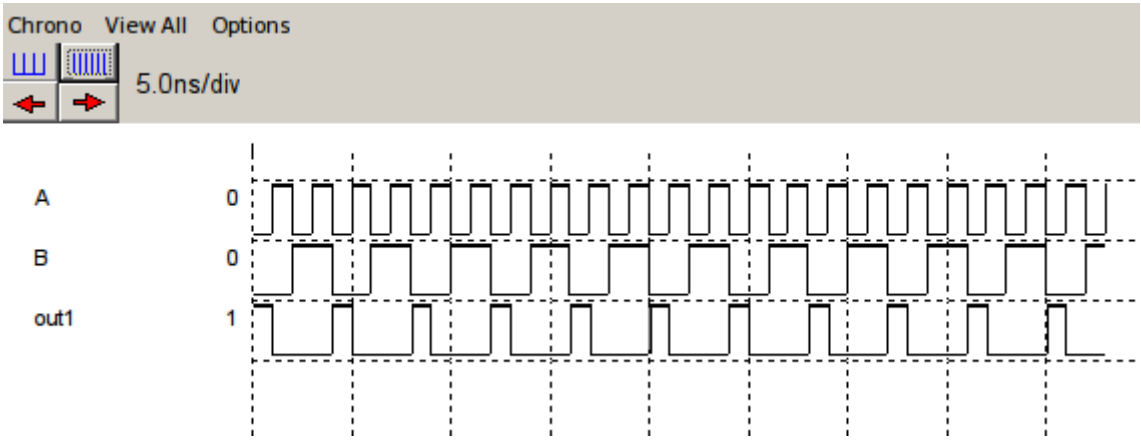


CMOS NOR Gate

Layout Diagram: We generate a verilog file from DSCH after designing the Gate level diagram of NOR gate, Compiling the verilog file in Microwind automatically generates the Layout level diagram of NOR gate.



Timing Diagram of NOR Gate:



5. **Conclusions:**

In this experiment we've used CMOS025 technology as foundary, there are several design principles which results a variety of performances of the same Logical Gates. In this experiment we've also tested manual layout design using Microwind Software.