Title: Observation and Verification of transfer characteristics of CMOS inverter.

1) **Objectives:**

   i. We can see the change of the output rate in the graph of voltage vs voltage and the voltage vs time .
   ii. Layout design simulation using Micro wind.
   iii. Here we use inverter to see the output result. Inverter is contain both pMOS and nMOS.
   iv. To observe the deviation in results with default layout

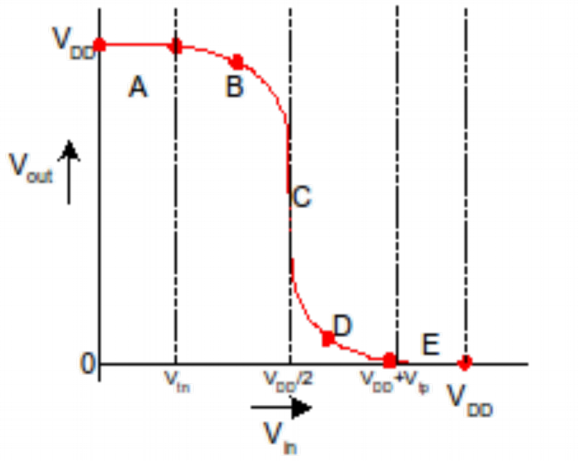
2) **Aparatus:**

   i. Microwind software.

   ii. Windows/Linux Operating System

3) **Theory:** Transfer characteristics of CMOS inverter:

It has 5 region , A,B,C,D,E . Transistor operating regions are given below in chart.



For Region A.$0 \leq V_{in} \leq V_{tn}$.NMOS is off, $I_{dsn}= 0$; where PMOS is in linear region.In this circuit $I_{dsn} = -I_{dsp.}$ Therefore both current will be zero,since $I_{dsn}= 0$Now $V_{dsp} = V_{DD}-V_{out}$ Or, $0 = V_{DD}-V_{out}$; in linear region $V_{dsp} \approx 0$.Therefore $V_{out} = V_{DD}$.In region B, the nMOS transistor starts to turn ON, pulling the output down. In region C, both transistors are in saturation. Notice that ideal transistors are only in region C for Vin = VDD /2 and that the slope of the transfer curve in this example is –8 in this region, corresponding to infinite gain. Real transistors have finite output resistances on account of channel length modulation, described in Section 2.4.2, and thus have finite slopes over a broader region over a broader region C. Other 2 resion D and E will be like this .

We can measure this change by the, Beta ratio

If $\beta_p / \beta_n \neq 1$, switching point will move from $V_{DD}/2$.This is called *skewed* gateOther gates: collapse into equivalent inverter

βp=mobility of pMOS =constant=W/L

βn=mobility of nMOS =constant=W/L, Here w=width and L=Length

βp/ βn=constant , Which is depend on its transfer characteristics is changes.

4) Procedure:

Table:

Inverter	pMOS		nMOS		βp/ βn
	Width	Length	Width	Length	
1st	50	1	5	1	0.1
2nd	5	1	5	1	1
3rd	5	1	50	1	10

Schematic Diagram:

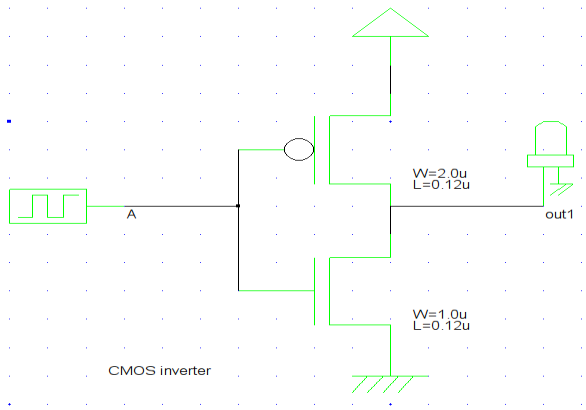
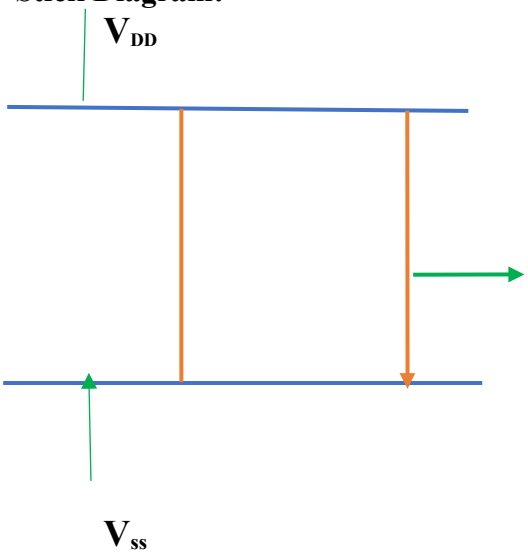


Illustration 1: CMOS Inverter

Stick Diagram:



Step by Step Procedure is as follows:

- First we start a new file in Microwind and take two metal lines at a distance of 85 lambda, each of which is 10 lamda wide. Both of them are the same metal.

- Then add a V_{DD} to the upper metal and a V_{SS} to the lower one. The figure will be as bellow.

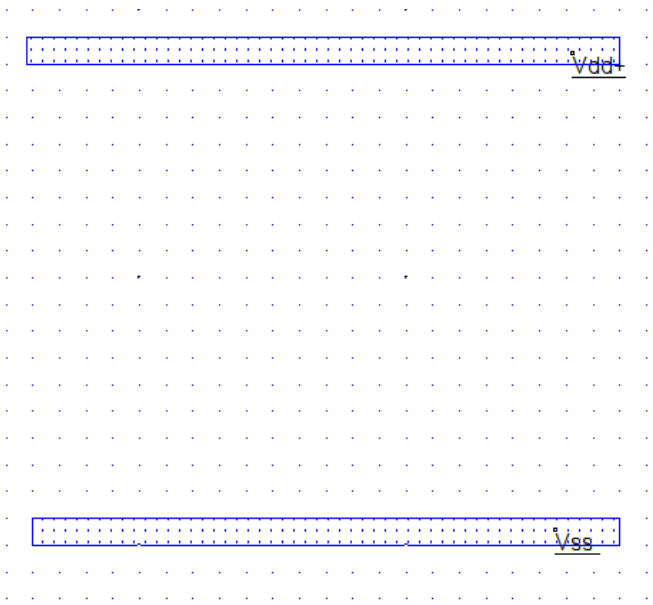


Illustration 2: Figure: Two metal plates

- Then generate one pMOS and one nMOS and connect them to the metal plates as show below. The pMOS and nMOS should be sized as shown in first row of the table

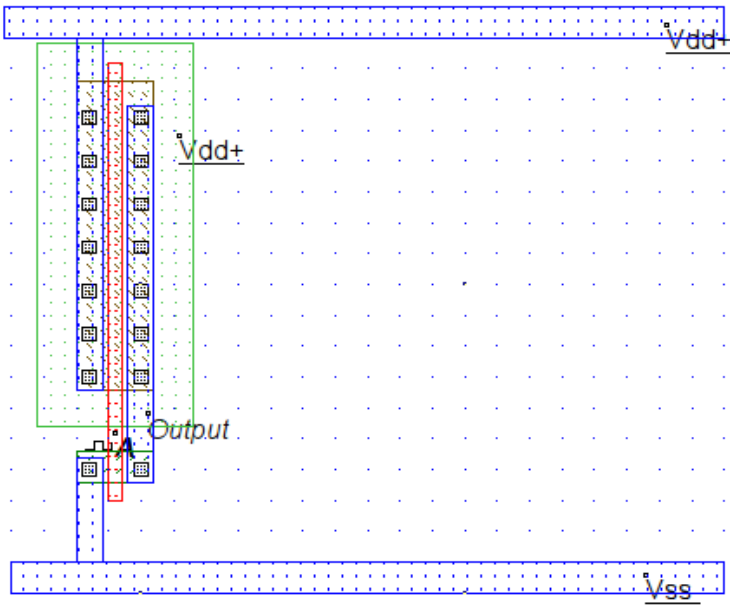


Illustration 3: First pMOS and nMOS placed

- After the first pMOS and nMOS is placed we'll generate two more pMOS and nMOS using the size mentioned in 2nd row of the table. And place them as follows

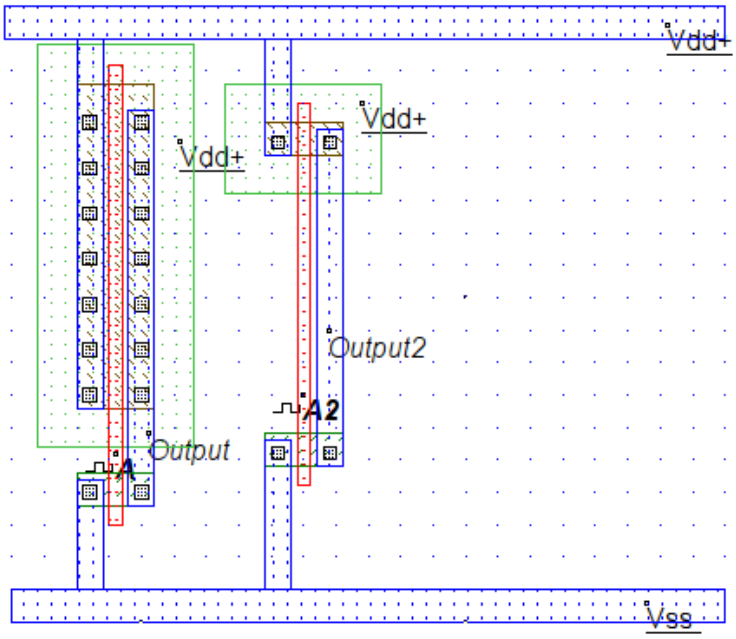


Illustration 4: After placing 2nd couple of pMOS & nMOS

- After 2nd couple of pMOS and nMOS is placed,we'll generate one more couple of pMOS & nMOS using the dimension mentioned in 3rd row of the table, and place them inside the two metal plates as shown below

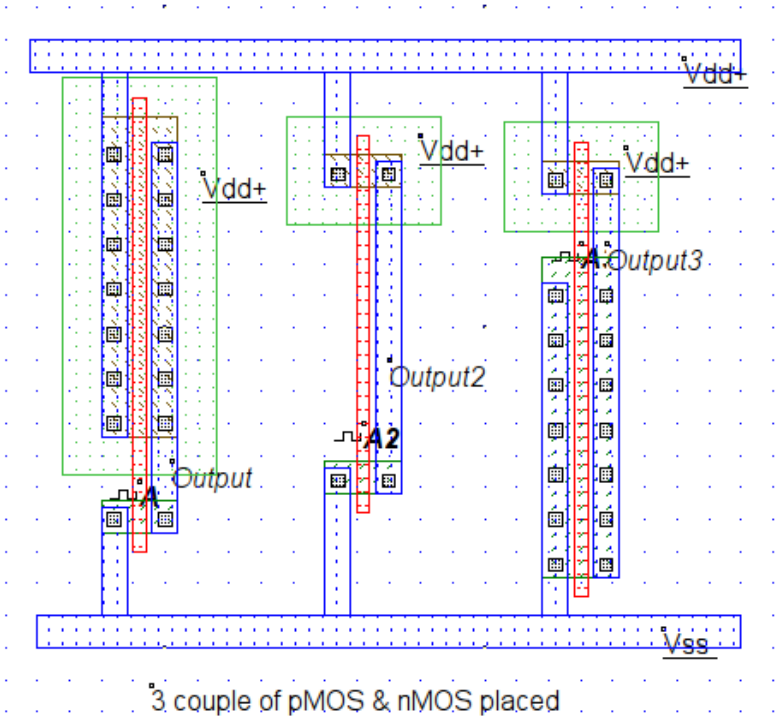


Illustration 5: After placing all 3 MOS

- Now we simulate the circuit to evaluate different characteristics of the Inverter Circuit

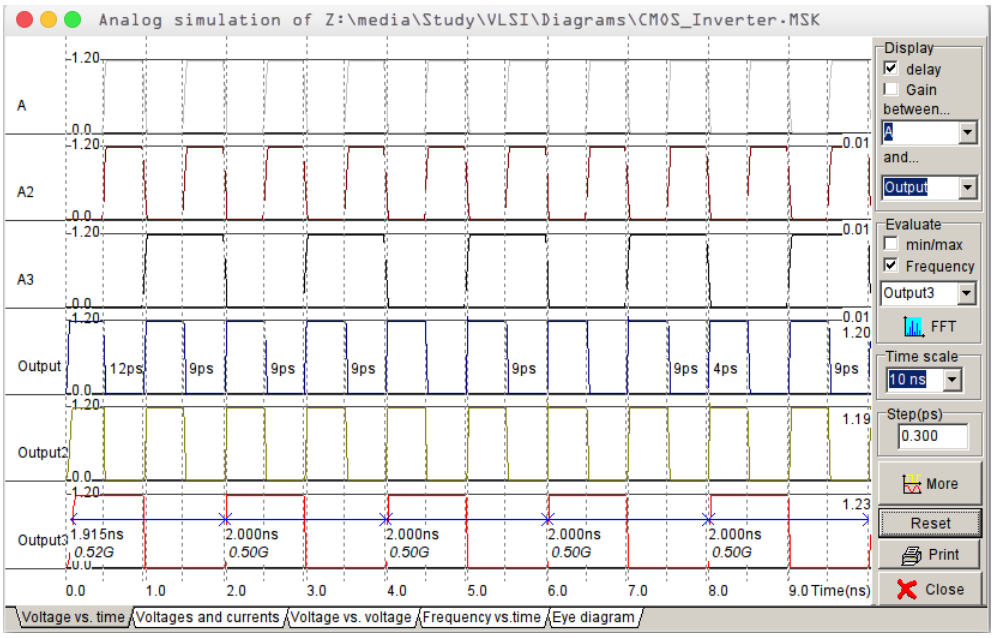


Illustration 6: Voltage vs Time characteristics Curve of CMOS inverter

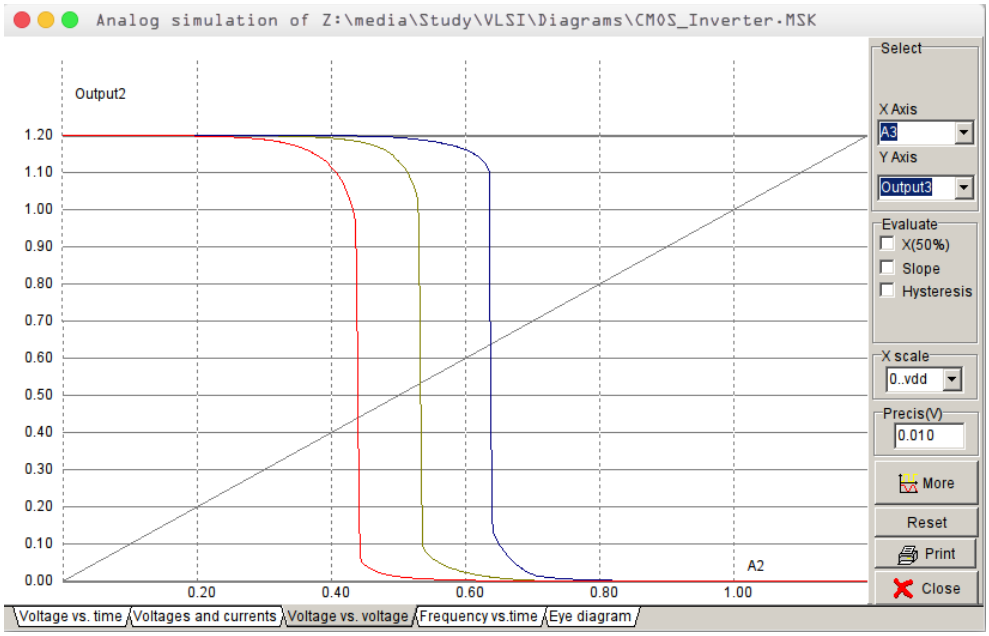


Illustration 7: Input Voltage vs Output Voltage Characteristics

5) Conclusion: The CMOS INVERT gate is implemented using three pMOS and three nMOS with different ratio. The required waveforms were obtained, observed and noted down using Microwind. And we observe the change of output in the voltage vs time graph and the voltage vs voltage graph .