Experiment Name : Verification of nMOS and pMOS DC-Characteristics

Objective:

* To find the MOS model parameters for the transistors and then “paper and pencil” manually calculate the DC characteristics of Ids current vs Vds voltage, using simple current equation for MOS model level 1 to determine a number of corresponding value pair of(Ids:Vds) with gate source voltage Vgs= a constant> Vth.
* Using circuit simulator of Microwind to do a DC simulation of Ids current vs Vds voltage and result of the two method compare.
* Calculation of the threshold voltage.

**Apparatus:**

We use the Micro wind software for layout design.

**Theory:**

The nMOS transistor vs Vds voltage equation are follows:

**Cut-off mode:** Ids =0 when Vds<0

**Linear region: Ids= Kn {(Vgs-Vth)Vds-Vds²/2} Vds< Vgs-Vth----------------------------(1)**

**Saturation Region: Ids=1/2 Kn {(Vgs-Vth)²} Vds>Vgs-Vth-------------------------------(2)**

The current gain factor Kn is constant with unit [A/V²]. This is depend on MOS transistor geometry, fabrication process parameters.

The factor Kn can be calculated as Kn = Kn’ W/L where the process conductance parameter Kn’= [A/V²]. The parameter stands for gate oxide capacitance per unit area depent on gate oxide thikness this can be expressed as where the in the silicon dioxide permittivity which can be calculated with the knowledge of the relative dielectric constant value of silicon dioxide and the dielectric constant of vacuum . So the = =3.97\*8.86\*10^-12[F/m]=3.51\*10^-11[F/m]. The additional parameter of Ids and Vds is the threshold voltage Vt. The threshold voltage with zero source substrate (bulk) voltage can be expressed as Vt0. When the source-substrate (bulk) voltage VSB is not zero then we call it for nMOS transistor is Vt0 and for pMOS is Vtp can be expressed as follows:

1.)

2.) )

Now Let us now relate the theoretical transistor parameters with our simulation software microwind. Here, we used all essential lvele 1 MOS models with a parameter value ans SI unit. The table shows the relationship.

|  |  |  |  |
| --- | --- | --- | --- |
| Micowind SPICE symbol | Meaning | Theoritical symbol | Unit |
| VTO | Threshold Voltage |  | V |
| TOX | Oxide thickness |  | nm |
| UO | Low-field mobility |  | m²/V-sec |
| PHI | Surface potential | 2|ф| | V |
| GAMMA | Body –bias coefficient |  | V^1/2 |

Procedure:

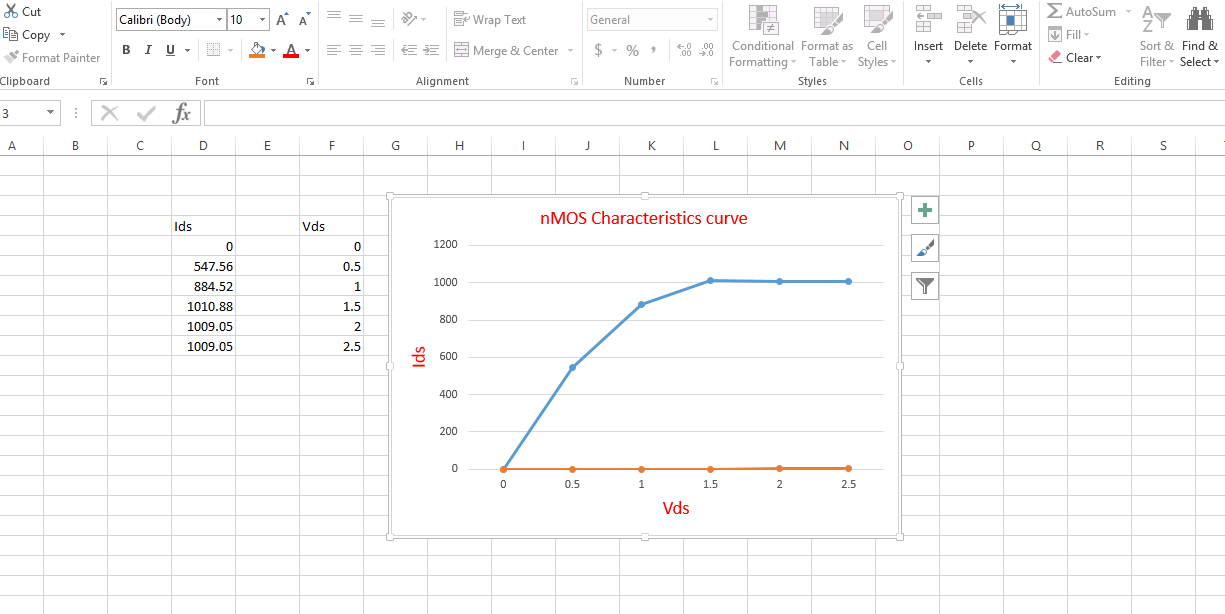
Level 1 MOS model equation to calculate DC values for the drain current vs drain-source voltage

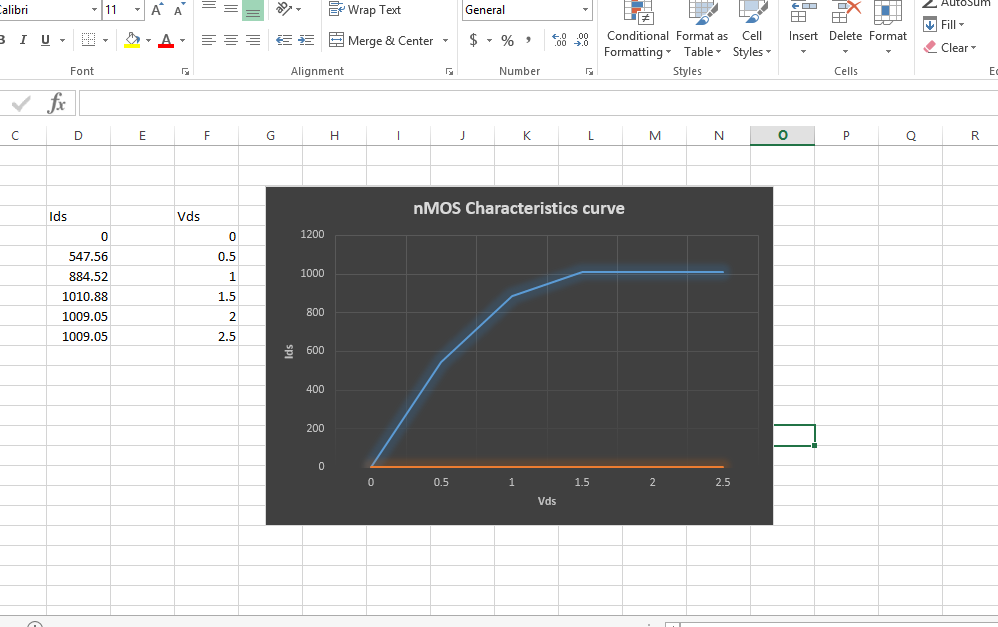
* First calculate with a gate-source voltage =+2.0v, for each drain-source voltage =0.5V,1V,1.5V,2.0V,2.5V the difference -(- to determine in which region the transistor work.Mark in Table equation number (1) or (2) that should be chosen to calculate the drain current for corresponding point .If we consider the .25µm CMOS process then =0.45, µ0=µn=0.06, Ƴ=0.4.
* Calculate for the voltage the drain current Ids for each point( after having determined a region the transistor works in Fill in corresponding value pairs( in table 2 for given drain source DC voltages .

Table 2: and Wn/Ln=2

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | 0.5 | 1 | 1.5 | 2 | 2.5 |
|  | -1.05 | -0.5 | -0.05 | 0.45 | 0.95 |
| Manual calculation | 547.50 | 884.52 | 1010.88 | 1009.05 | 1009.05 |

Now plot the characteristics curve using excel based on data values of table 2. The curve would be shown below:

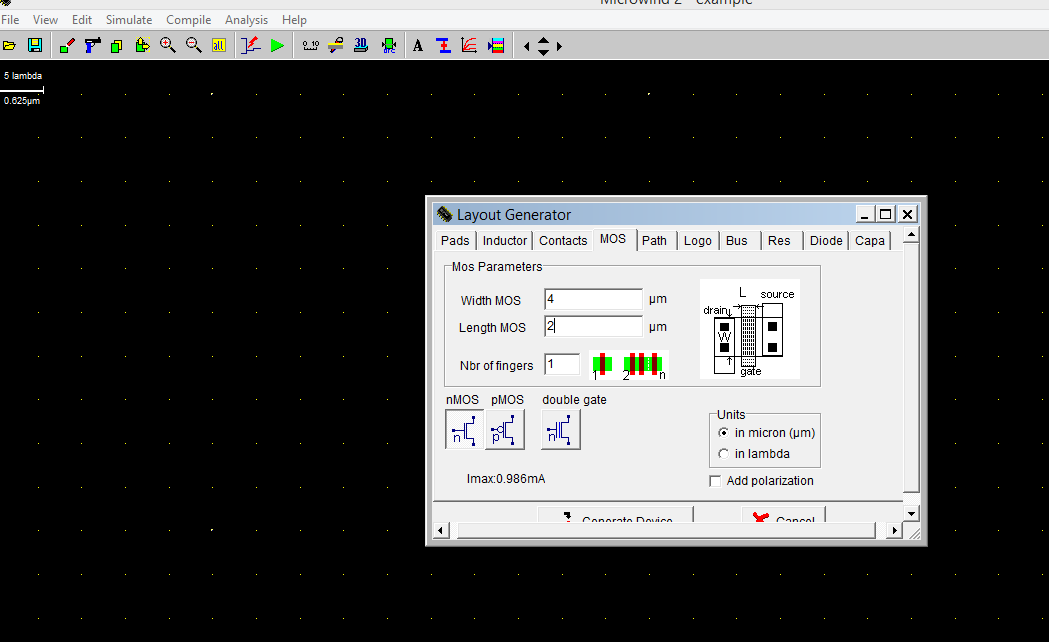


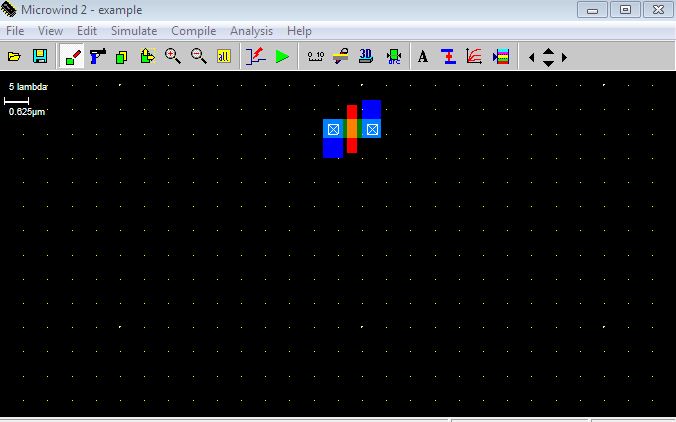


The simulation process for nMOS transistor

Do of Simulation >” MOS characteristics “ to generate the DC characteristics Ids vs Vds for the NMOS transistor in microwind.

* Open the microwind window and Check that the selected foundary is 0.25 µm CMOS process form file->select foundry and choose cmos 0.25 rul. Use Level 1 MOS transistor model.
* Now generate the nMOS transistor of width and length ration 4Ƴ:2Ƴ from palate .The nMOS generation process is shown in fig below:





**Fig: nMOS generation process in microwind**

* **Now click the Simulation->MOS characteristics and then point to the NMOS transistor .In the upper left corner of the window we can now choose functions to plot .Choose to show for the nMOS transistor the current Ids vs Vds for Vgs=2.0V**
* **On the bottom row to the left in the plot window ,fill in the to-value of Vdd, the to-value of Vg and the step-value of Vg so that we can rest the text “Vd from 0 to 2.50 For Vg from 0 to 2.00 Step.**
* **From the generated curve show in the fig find the value pairs of Ids and VDs and fill in the values of the point value pairs from the generated DC Characteristics curve into table:**

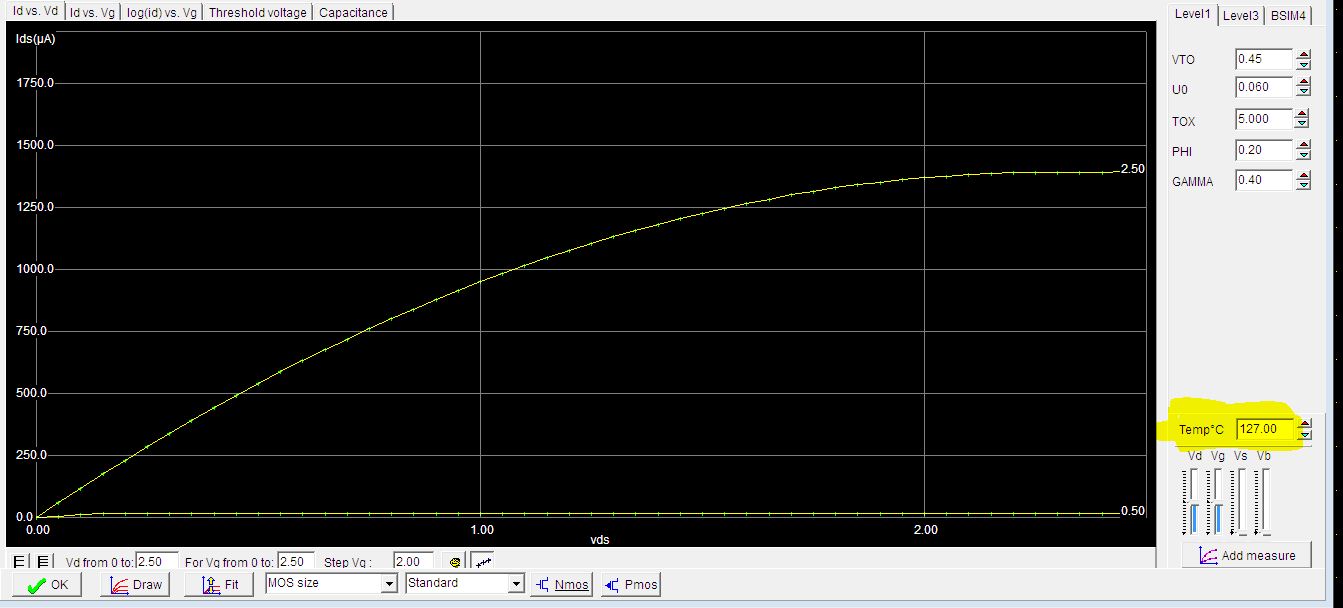
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Fig: nMOS charectaristics curve

Table 2: Vgs=2.0V

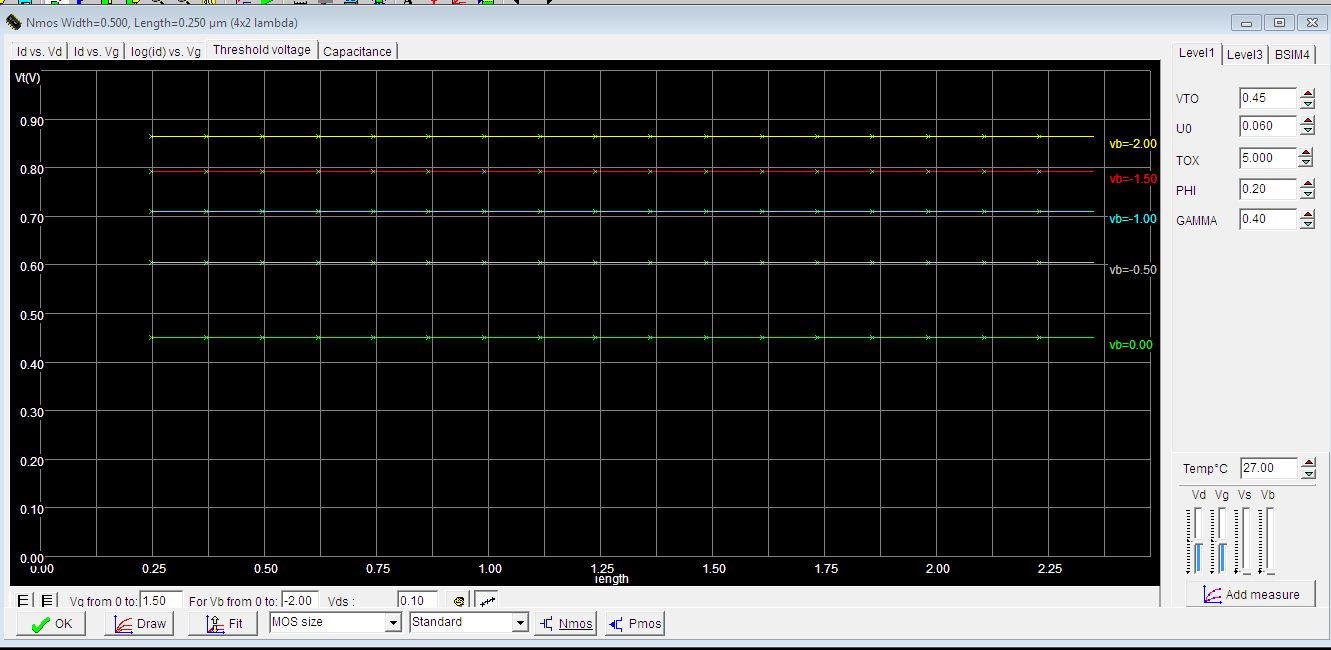
Table 2: and Wn/Ln=2

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | 0.5 | 1 | 1.5 | 2 | 2.5 |
| =Manual calculation | 547.50 | 884.52 | 1010.88 | 1009.05 | 1009.05 |

Compare hand calculated result and the simulated result .

* Calculation of the threshold voltage factor:

Variation of threshold voltage dependence of the bulk-to source voltage Vsb. Called the Body effect .In the upper experiment we have consider that the threshold voltage factor gamma=0.The threshold voltage tab in the Ids vs Vds simulation window when the voltage of substrate voltage bias Vsb=0 shown below in fig;



Now let us calculate the threshould voltage from gamma=0.40 and= Vsb=-1v then the equation will be:

1.)

🡺Vtn=0.45+0.40(1.095-0.447)

🡺Vtn=0.709293V

Comparing the calculated result shown in fig for Vsb=-1V

**Result :** The lab objectives are successfully observed and verify with theoretical calculation

For pMOS the equation are:

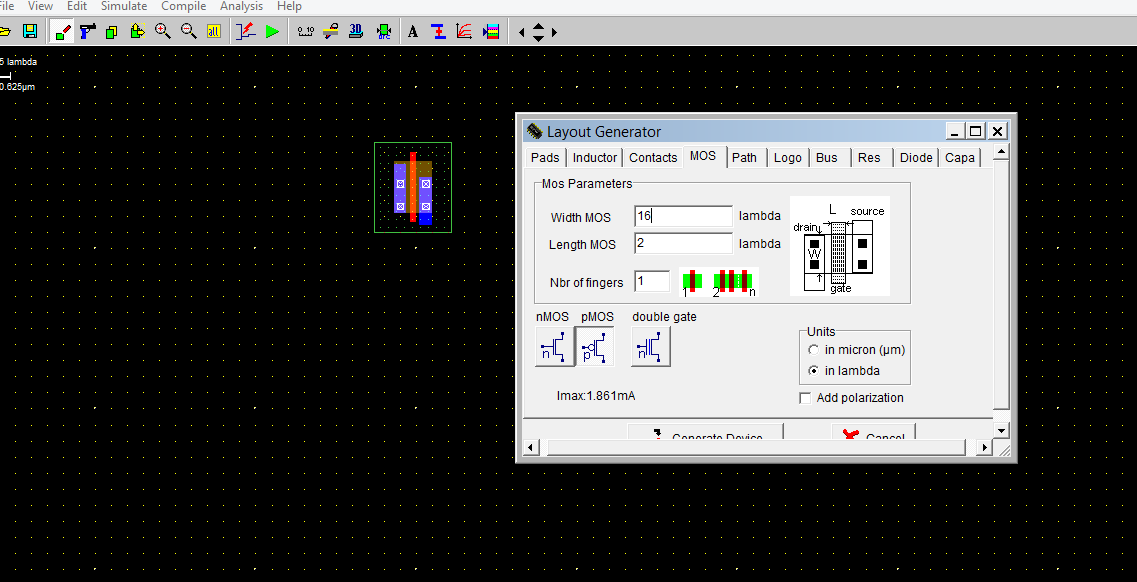


Here Vgs=2 and Vds =0.45 so Ids is in cutoff region and always Ids=0.

Do the simulation process for pMOS transistor

Do of Simulation >” MOS characteristics “ to generate the DC characteristics Ids vs Vds for the NMOS transistor in microwind.

* Open the microwind window and Check that the selected foundary is 0.25 µm CMOS process form file->select foundry and choose cmos 0.25 rul. Use Level 1 MOS transistor model.
* Now generate the nMOS transistor of width and length ration 4Ƴ:2Ƴ from palate .The nMOS generation process is shown in fig below:



**Fig: nMOS generation process in microwind**

* **Now click the Simulation->MOS characteristics and then point to the NMOS transistor .In the upper left corner of the window we can now choose functions to plot .Choose to show for the nMOS transistor the current Ids vs Vds for Vgs=2.0V**
* **On the bottom row to the left in the plot window ,fill in the to-value of Vdd, the to-value of Vg and the step-value of Vg so that we can rest the text “Vd from 0 to 2.50 For Vg from 0 to 2.00 Step.**
* **From the generated curve show in the fig find the value pairs of Ids and VDs and fill in the values of the point value pairs from the generated DC Characteristics curve into table:**

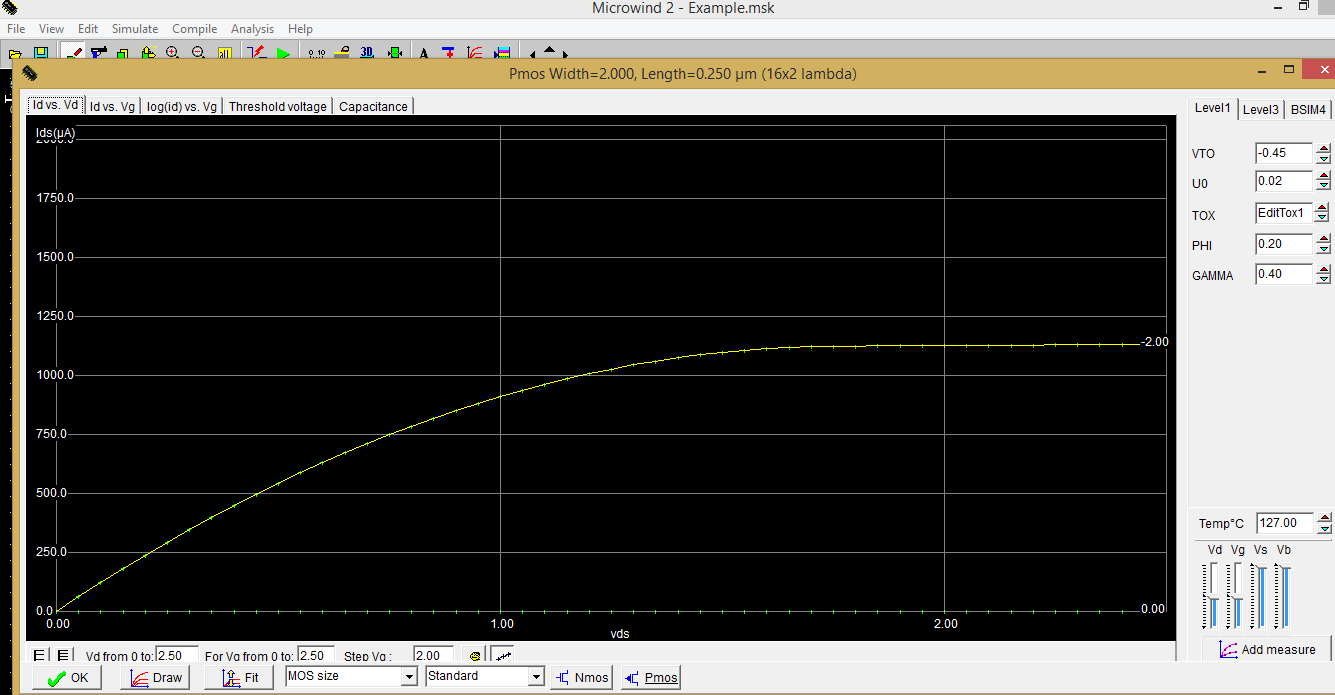
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Fig: nMOS charectaristics curve

**Conclusion: Here we show the both nMOS and pMOS characteristics for both theoretical and simulation.**