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Media Engineering and Technology
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Computer System Architecture, Spring Semester 2022
Practice Assignment 8

Discussion: 14/05/2022 - 19/05/2022

Exercise 8-1

a) Consider the following component times:

- IF: 200ps
- ID: 100ps
- EX: 200ps
- MEM: 200ps
- WB: 100ps

1. What is the frequency of the processor in case of a Single-Cycle (SC) implementation?
2. What is the frequency of the processor in case of a Pipelined (PL) implementation?

b) Draw the execution of the following instructions for Single-Cycle (SC) and Pipelined (PL) implementations.
We assume the write to the register file occurs in the first half of the clock cycle and the read from the register file occurs in the second half.

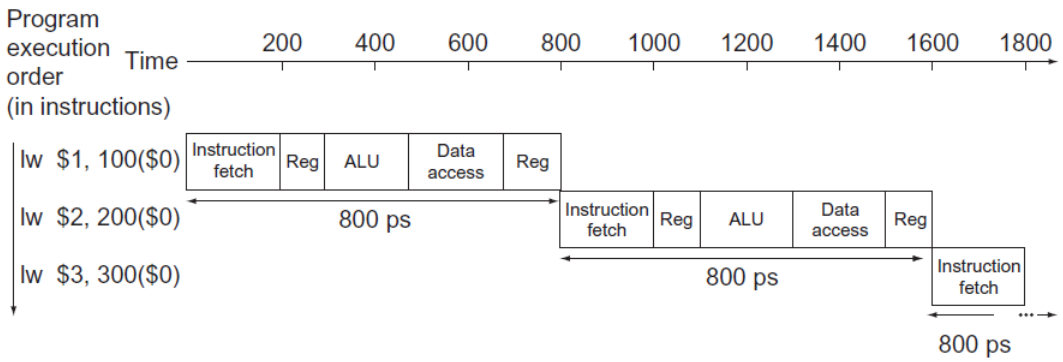
```
lw $s1, 100($s0)
lw $s2, 200($s0)
lw $s3, 300($s0)
```

c) By how much did pipelining improve the performance? What would happen if 1,000,000 instructions are added?

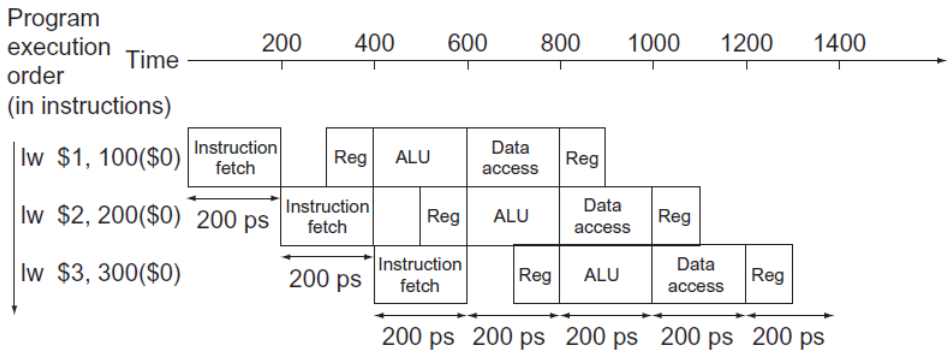
Solution:

a)
1. Load Word (LW) is the slowest instruction in MIPS, therefore: 200 +100+200+200+100 = 800ps.
   Frequency = $(1*10^{12})/800$ = 1.25 GHz
2. Slowest stage is 200ps, so frequency = $(1*10^{12})/200$ = 5 GHz.

b) Single-Cycle (SC):



Pipelined (PL):
We assume the write to the register file occurs in the first half of the clock cycle and the read from the register file occurs in the second half.



c) When we had 3 instructions:

- Single-Cycle (SC) = 800+800+800 = 2400ps
- Piple-Lined (PL) = 200+200+200+200+200+200+200 = 1400ps
- 2400/1400 = 1.71

When we add 1 million instructions to the already existing 3 instructions:

- Single-Cycle (SC): (1000000*800ps) + 2400ps = 800002400ps
- Pipelined (PL): (1000000*200ps) + 1400ps = 200001400ps
- 800002400/200001400 = 4