



Project 1



Eng/ Kareem Waseem

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1-RTL code

```
1 module Reg_Mux(In,Sel,Out,Clk,Rst,Enable);
2
3 parameter WIDTH_REG_MUX_IN = 18;
4 parameter WIDTH_REG_MUX_OUT=18;
5 parameter TYPE = "SYNC";
6
7 input [WIDTH_REG_MUX_IN-1:0] In;
8 input Sel,Rst,Clk,Enable;
9
10 output [WIDTH_REG_MUX_OUT-1:0] Out;
11
12 reg [WIDTH_REG_MUX_IN-1:0] In_reg;
13 //Async or Sync Rst
14 generate
15     if (TYPE == "SYNC") begin
16         always @(posedge Clk) begin
17             if(Rst)
18                 In_reg <= 0;
19             else begin
20                 if(Enable)
21                     In_reg <= In;
22             end
23         end
24     end
25     else begin
26         always @(posedge Clk or posedge Rst) begin
27             if(Rst)
28                 In_reg <= 0;
29             else begin
30                 if(Enable)
31                     In_reg <= In;
32             end
33         end
34     end
35 endgenerate
36
37 assign Out = (Sel)? In_reg : In;
38
39 endmodule
```

```
1 module Mux(In0,In1,Sel,Out);
2
3 parameter WIDTH_MUX_IN0 = 18;
4 parameter WIDTH_MUX_IN1 = 18;
5 parameter WIDTH_MUX_OUT = 18;
6
7 input [WIDTH_MUX_IN0-1:0] In0;
8 input [WIDTH_MUX_IN1-1:0] In1;
9 input Sel;
10
11 output [WIDTH_MUX_OUT-1:0] Out;
12
13 assign Out = (Sel)? In1 : In0;
14
15 endmodule
```

```
1 module Mux_4x1(In0,In1,In2,In3,Sel,Out);
2
3 input [47:0] In0,In1,In2,In3;
4 input [1:0] Sel;
5
6 output wire [47:0] Out;
7
8 assign Out = (Sel == 2'b00) ? In0 :
9             (Sel == 2'b01) ? In1 :
10            (Sel == 2'b10) ? In2 :
11            (Sel == 2'b11) ? In3 :
12            In0; // Default case
13
14 endmodule
```

```

1  module Spartan_6(
2      A,B,D,C
3      ,CLK,CARRYIN
4      ,OPMODE,BCIN,RSTA,RSTB,RSTM,RSTP,RSTC,RSTD,RSTCARRYIN,RSTOPMODE
5      ,CEA,CEB,CEM,CEP,CEC,CED,CECARRYIN,CEOPMODE
6      ,PCIN
7      ,BCOUT,PCOUT,P,M,CARRYOUT,CARRYOUTF
8      );
9      //parameters for A and B inputs that define whether the mux out is reg or not (SELECT LINE OF REG_MUX)
10     parameter AOREG = 0;
11     parameter BOREG = 0; //0 refers to no registers
12     parameter AIREG = 1; //1 refers to registers
13     parameter BIREG = 1;
14     //parameters for C,D,M,P,CARRYIN,CARRYOUT,OPMODE that define whether the mux out is reg or not (SELECT LINE OF REG_MUX)
15     parameter CREG = 1;
16     parameter DREG = 1;
17     parameter MREG = 1;
18     parameter PREG = 1;
19     parameter CARRYINREG = 1;
20     parameter CARRYOUTREG = 1;
21     parameter OPMODEREG = 1;
22     //CARRYINSEL either the CARRYIN input will be considered or the value of opcode[5] , Values = "CARRYIN" , "OPMODE5"
23     wire CARRYIN_SEL;
24     parameter CARRYINSEL = "OPMODE5";
25
26     assign CARRYIN_SEL = (CARRYINSEL == "OPMODE5")? 1 : 0;
27
28     //B_INPUT defines whether the input to the B port is <B input> (DIRECT) or <cascaded input BCIN> from the previous DSP48A1 (CASCADE)
29     wire B_SEL;
30     parameter B_INPUT = "DIRECT";
31
32     assign B_SEL = (B_INPUT == "DIRECT")? 1 : 0;
33
34     //RSTTYPE selects whether all resets for the DSP48A1 should have a synchronous or asynchronous reset , Values = "ASYNC" , "SYNC"
35     parameter RSTTYPE = "SYNC";
36     //Inputs
37     input [17:0] A,B,D,BCIN;
38     input [7:0] OPMODE;
39     input [47:0] C,PCIN;
40
41     input CARRYIN,CLK;
42     input CEA,CEB,CEC,CECARRYIN,CED,CEM,CEOPMODE,CEP; //clk enable for the Reg_Mux for each input
43     input RSTA,RSTB,RSTC,RSTCARRYIN,RSTD,RSTM,RSTOPMODE,RSTP; //rst active high for the Reg_Mux for each input, Sync or Async depending on RSTTYPE

```

```

44     //output
45     output CARRYOUT,CARRYOUTF;
46     output [17:0] BCOUT;
47     output [35:0] M;
48     output [47:0] PCOUT,P;
49     //Needed Internal Signals
50     wire CIN,COUT,Carry_Cascade;
51     wire [7:0] OPMODE_Mux;
52     wire [17:0] D_Mux,B_Mux,B0_Mux,A0_Mux,Pre_Add_Mux_Out,B1_Mux,A1_Mux;
53     reg [17:0] Pre_Add;
54     wire [35:0] Multi_Value,M_Reg_Mux_Out;
55     wire [47:0] C_Mux,Concatenation,X_Out,Z_Out,Post_Add;
56     wire [48:0] Full_Add;
57     //Inputs into Reg_Mux
58     Mux_B_Input (.In0(BCIN),.In1(B),.Sel(B_SEL),.Out(B_Mux)); //which will be B_port
59
60     Reg_Mux #(.TYPE(RSTTYPE)) D_Entry (.In(D),.Sel(DREG),.Out(D_Mux),.Clk(CLK),.Rst(RSTD),.Enable(CED)); //D input entry
61     Reg_Mux #(.TYPE(RSTTYPE)) B_Entry (.In(B_Mux),.Sel(BOREG),.Out(B0_Mux),.Clk(CLK),.Rst(RSTB),.Enable(CEB)); //B input entry
62     Reg_Mux #(.TYPE(RSTTYPE)) A_Entry (.In(A),.Sel(AOREG),.Out(A0_Mux),.Clk(CLK),.Rst(RSTA),.Enable(CEA)); //A0 input entry
63     Reg_Mux #(.WIDTH_REG_MUX_IN(48),.WIDTH_REG_MUX_OUT(48),.TYPE(RSTTYPE)) C_Entry (.In(C),.Sel(CREG),.Out(C_Mux),.Clk(CLK),.Rst(RSTC),.Enable(CEC)); //C input entry
64     Reg_Mux #(.WIDTH_REG_MUX_IN(8),.WIDTH_REG_MUX_OUT(8),.TYPE(RSTTYPE)) OPMODE_Entry (.In(OPMODE),.Sel(OPMODEREG),.Out(OPMODE_Mux),.Clk(CLK),.Rst(RSTOPMODE),.Enable(CEOPMODE));
65     //operations till multiplication
66     always@(*) begin
67         if(OPMODE_Mux[6])
68             Pre_Add = D_Mux - B0_Mux;
69         else
70             Pre_Add = D_Mux + B0_Mux;
71     end
72     Mux_Pre_Add_Mux (.In0(B0_Mux),.In1(Pre_Add),.Sel(OPMODE_Mux[4]),.Out(Pre_Add_Mux_Out));
73     //B1,A1 reg
74     Reg_Mux #(.TYPE(RSTTYPE)) B1_Reg_Mux (.In(Pre_Add_Mux_Out),.Sel(B1REG),.Out(B1_Mux),.Clk(CLK),.Rst(RSTB),.Enable(CEB));
75     Reg_Mux #(.TYPE(RSTTYPE)) A1_Reg_Mux (.In(A0_Mux),.Sel(A1REG),.Out(A1_Mux),.Clk(CLK),.Rst(RSTA),.Enable(CEA));
76     assign BCOUT = B1_Mux;
77     //Multiplication
78     assign Multi_Value = (B1_Mux * A1_Mux);
79     Reg_Mux #(.WIDTH_REG_MUX_IN(36),.WIDTH_REG_MUX_OUT(36),.TYPE(RSTTYPE)) M_Reg_Mux (.In(Multi_Value),.Sel(MREG),.Out(M_Reg_Mux_Out),.Clk(CLK),.Rst(RSTM),.Enable(CEM));
80     assign M = M_Reg_Mux_Out;
81     //X,Mux = 7,30x
82     assign Concatenation = {D_Mux[11:0],A1_Mux[17:0],B1_Mux[17:0]};
83
84     Mux_4x1_X (.In0(48'b0),.In1({12'b0,M_Reg_Mux_Out}),.In2(P),.In3(Concatenation),.Sel(OPMODE_Mux[1:0]),.Out(X_Out));
85
86     Mux_4x1_Z (.In0(48'b0),.In1(PCIN),.In2(P),.In3(C_Mux),.Sel(OPMODE_Mux[3:2]),.Out(Z_Out));

```

```

87     //preparing CIN for the 2nd ADD
88     assign Carry_Cascade = (CARRYIN_SEL)? OPMODE_Mux[5] : CARRYIN;
89     Reg_Mux #(.TYPE(RSTTYPE),.WIDTH_REG_MUX_IN(1),.WIDTH_REG_MUX_OUT(1)) CYI (.In(Carry_Cascade),.Sel(CARRYINREG),.Out(CIN),.Clk(CLK),.Rst(RSTCARRYIN),.Enable(CECARRYIN));
90     //second Add
91     assign Full_Add = (OPMODE_Mux[7])? ({1'b0,Z_Out}-{1'b0,X_Out}+CIN) : ({1'b0,Z_Out}+{1'b0,X_Out}+CIN);
92     assign Post_Add = Full_Add [47:0];
93     assign COUT = Full_Add [48];
94
95     Reg_Mux #(.WIDTH_REG_MUX_IN(48),.WIDTH_REG_MUX_OUT(48),.TYPE(RSTTYPE)) P_Reg_Mux (.In(Post_Add),.Sel(PREG),.Out(P),.Clk(CLK),.Rst(RSTP),.Enable(CEP));
96     assign PCOUT = P;
97     Reg_Mux #(.TYPE(RSTTYPE),.WIDTH_REG_MUX_IN(1),.WIDTH_REG_MUX_OUT(1)) COUT_Reg_Mux (.In(COUT),.Sel(CARRYOUTREG),.Out(CARRYOUT),.Clk(CLK),.Rst(RSTCARRYIN),.Enable(CECARRYIN));
98     assign CARRYOUTF = CARRYOUT;
99
100 endmodule

```

2-Testbench code

```
1 module Spartan_6_tb();
2
3 //stimuls and response
4 reg [17:0] A_tb,B_tb,D_tb,BCIN_tb;
5 reg [7:0] OPMODE_tb;
6 reg [47:0] C_tb,PCIN_tb;
7
8 reg CARRYIN_tb,CLK_tb;
9 reg CEA_tb,CEB_tb,CEC_tb,CECARRYIN_tb,CED_tb,CEM_tb,CEOPMODE_tb,CEP_tb;
10 reg RSTA_tb,RSTB_tb,RSTC_tb,RSTCARRYIN_tb,RSTD_tb,RSTM_tb,RSTOPMODE_tb,RSTP_tb;
11
12 wire CARRYOUT_DUT,CARRYOUTF_DUT;
13 wire [17:0] BCOUT_DUT;
14 wire [35:0] M_DUT;
15 wire [47:0] PCOUT_DUT,P_DUT;
16
17 reg CARRYOUT_Expected;
18 reg [17:0] BCOUT_Expected;
19 reg [35:0] M_Expected;
20 reg [47:0] P_Expected;
21
22 //DUT
23 Spartan_6 DUT (
24 // -- Inputs --
25 .A(A_tb),
26 .B(B_tb),
27 .D(D_tb),
28 .C(C_tb),
29 .CLK(CLK_tb),
30 .CARRYIN(CARRYIN_tb),
31 .OPMODE(OPMODE_tb),
32 .BCIN(BCIN_tb),
33 .PCIN(PCIN_tb),
34
35 // -- Reset Inputs --
36 .RSTA(RSTA_tb),
37 .RSTB(RSTB_tb),
38 .RSTC(RSTC_tb),
39 .RSTD(RSTD_tb),
40 .RSTM(RSTM_tb),
41 .RSTP(RSTP_tb),
42 .RSTCARRYIN(RSTCARRYIN_tb),
43 .RSTOPMODE(RSTOPMODE_tb),
```

```
44
45 // -- Clock Enable Inputs --
46 .CEA(CEA_tb),
47 .CEB(CEB_tb),
48 .CEC(CEC_tb),
49 .CED(CED_tb),
50 .CEM(CEM_tb),
51 .CEP(CEP_tb),
52 .CEOPMODE(CEOPMODE_tb),
53 .CECARRYIN(CECARRYIN_tb),
54
55 // -- Outputs --
56 .BCOUT(BCOUT_DUT),
57 .PCOUT(PCOUT_DUT),
58 .P(P_DUT),
59 .M(M_DUT),
60 .CARRYOUT(CARRYOUT_DUT),
61 .CARRYOUTF(CARRYOUTF_DUT)
62 );
63 //clk generation
64 initial begin
65     CLK_tb = 0;
66     forever
67         #1 CLK_tb = ~CLK_tb;
68 end
69 //start from known states <wait> >> (Randomize - wait - check)for loop
70 initial begin
71 //rst check
72 RSTA_tb = 1;
73 RSTB_tb = 1;
74 RSTC_tb = 1;
75 RSTCARRYIN_tb = 1;
76 RSTD_tb = 1;
77 RSTM_tb = 1;
78 RSTOPMODE_tb = 1;
79 RSTP_tb = 1;
80
81 A_tb = $random;
82 B_tb = $random;
83 D_tb = $random;
84 BCIN_tb = $random;
85 OPMODE_tb = $random;
86 C_tb = $random;
```

```

67 PCIN_tb = $random;
68 CARRYIN_tb = $random;
69
70 CEA_tb = $random;
71 CEB_tb = $random;
72 CEC_tb = $random;
73 CECARRYIN_tb = $random;
74 CED_tb = $random;
75 CEM_tb = $random;
76 CEOPMODE_tb = $random;
77 CEP_tb = $random;
78
79 @(negedge CLK_tb);
80 if(CARRYOUT_DUT != 0 || CARRYOUTF_DUT != 0 || BCOUT_DUT != 0 || M_DUT != 0 || PCOUT_DUT != 0 || P_DUT != 0) begin
81     $display("ERROR In Reset");
82     $stop;
83 end
84 //Path 1 check
85 RSTA_tb = 0;
86 RSTB_tb = 0;
87 RSTC_tb = 0;
88 RSTCARRYIN_tb = 0;
89 RSTD_tb = 0;
90 RSTM_tb = 0;
91 RSTOPMODE_tb = 0;
92 RSTP_tb = 0;
93
94 CEA_tb = 1;
95 CEB_tb = 1;
96 CEC_tb = 1;
97 CECARRYIN_tb = 1;
98 CED_tb = 1;
99 CEM_tb = 1;
100 CEOPMODE_tb = 1;
101 CEP_tb = 1;
102
103 OPMODE_tb = 8'b11011101;
104 A_tb = 20;
105 B_tb = 10;
106 C_tb = 350;
107 D_tb = 25;
108
109 BCOUT_Expected = 'hff;
110 M_Expected = 'h12c;

```

```

111 P_Expected = '122;
112 CARRYOUT_Expected = 0;
113
114 repeat(4) @(negedge CLK_tb);
115 if(BCOUT_DUT != BCOUT_Expected || M_DUT != M_Expected || P_DUT != P_Expected || PCOUT_DUT != P_Expected || CARRYOUT_DUT != CARRYOUT_Expected || CARRYOUTF_DUT != CARRYOUT_Expected) begin
116     $display("ERROR In Path 1");
117     $stop;
118 end
119 //path 2 check
120 OPMODE_tb = 8'100010000;
121 A_tb = 20;
122 B_tb = 10;
123 C_tb = 350;
124 D_tb = 25;
125
126 BCOUT_Expected = '122;
127 M_Expected = '12bc;
128 P_Expected = '10;
129 CARRYOUT_Expected = 0;
130
131 repeat(3) @(negedge CLK_tb);
132 if(BCOUT_DUT != BCOUT_Expected || M_DUT != M_Expected || P_DUT != P_Expected || PCOUT_DUT != P_Expected || CARRYOUT_DUT != CARRYOUT_Expected || CARRYOUTF_DUT != CARRYOUT_Expected) begin
133     $display("ERROR In Path 2");
134     $stop;
135 end
136 //path 3 check
137 OPMODE_tb = 8'100010110;
138 A_tb = 20;
139 B_tb = 10;
140 C_tb = 350;
141 D_tb = 25;
142
143 BCOUT_Expected = '1a;
144 M_Expected = '1cd;
145 P_Expected = '10;
146 CARRYOUT_Expected = 0;
147
148 repeat(3) @(negedge CLK_tb);
149 if(BCOUT_DUT != BCOUT_Expected || M_DUT != M_Expected || P_DUT != P_Expected || PCOUT_DUT != P_Expected || CARRYOUT_DUT != CARRYOUT_Expected || CARRYOUTF_DUT != CARRYOUT_Expected) begin
150     $display("ERROR In Path 3");
151     $stop;
152 end
153 //path 4 check
154 OPMODE_tb = 8'101010111;

```

Active
Go to 54

```

175 A_tb = 5;
176 B_tb = 6;
177 C_tb = 350;
178 D_tb = 25;
179 PCIN_tb = 3000;
180
181 BCOUT_Expected = 'h6;
182 M_Expected = 'h1e;
183 P_Expected = 'hfe6fffc0bb1;
184 CARRYOUT_Expected = 1;
185
186 repeat(3) @(negedge CLK_tb);
187 if(BCOUT_DUT != BCOUT_Expected || M_DUT != M_Expected || P_DUT != P_Expected || PCOUT_DUT != P_Expected || CARRYOUT_DUT != CARRYOUT_Expected || CARRYOUTF_DUT != CARRYOUT_Expected) begin
188     $display("ERROR In Path 4");
189     $stop;
190 end
191 else
192     $display("DSP Is Working");
193
194
195 $stop;
196 end
197
198 endmodule

```

3-Do file

 run_DSP_tb.do - Notepad

File Edit Format View Help

Create library

vlib work

Compile the Verilog file

vlog Spartan_6_tb.v

Start the simulation with full visibility

vsim -voptargs=+acc Spartan_6_tb

Add specific waves for debugging

add wave CLK_tb

add wave *RST*_tb

add wave OPMODE_tb

add wave A_tb

add wave B_tb

add wave C_tb

add wave D_tb

add wave PCIN_tb

add wave BCOUT_DUT

add wave M_DUT

add wave P_DUT

add wave PCOUT_DUT

add wave CARRYOUT_DUT

add wave BCOUT_Expected

add wave M_Expected

add wave P_Expected

add wave CARRYOUT_Expected

Run the simulation until it finishes

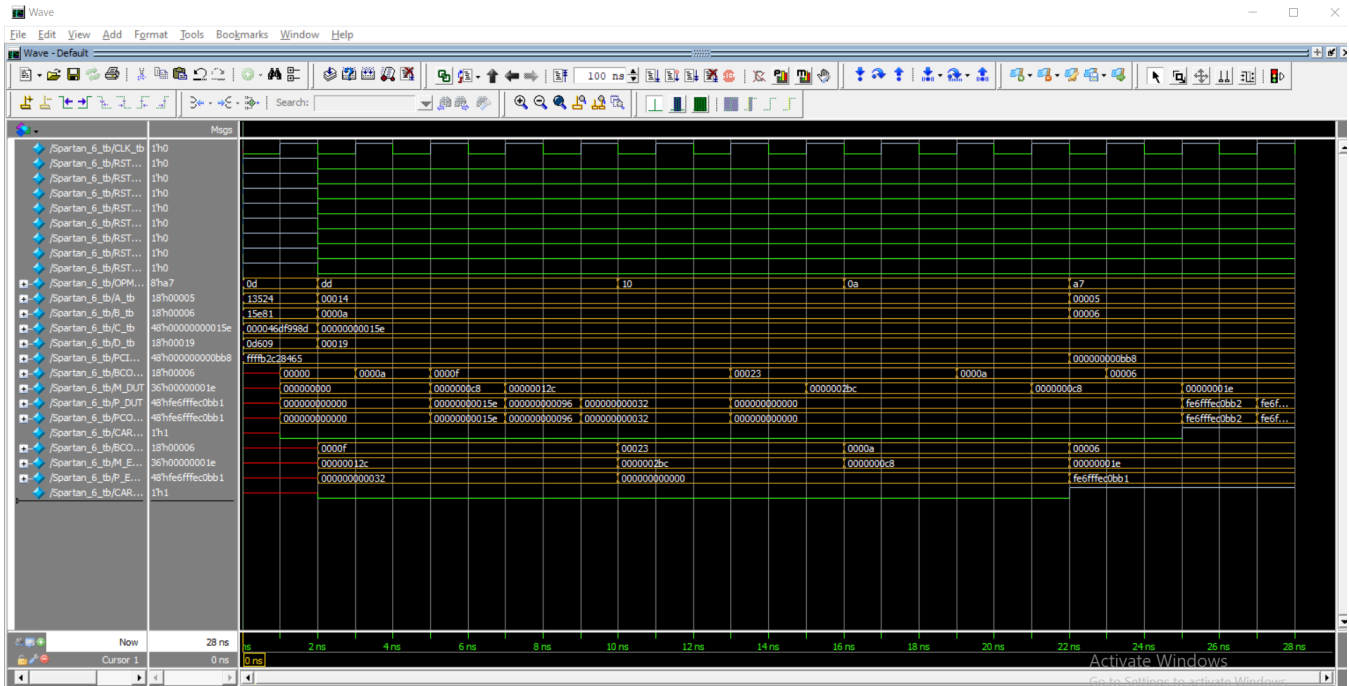
run -all

uncomment to automatically close the simulation

quit -sim

4-QuestaSim Snippets

```
# DSP Is Working
# ** Note: $stop      : Spartan_6_tb.v(195)
#      Time: 28 ns    Iteration: 1   Instance: /Spartan_6_tb
# Break in Module Spartan_6_tb at Spartan_6_tb.v line 195
```

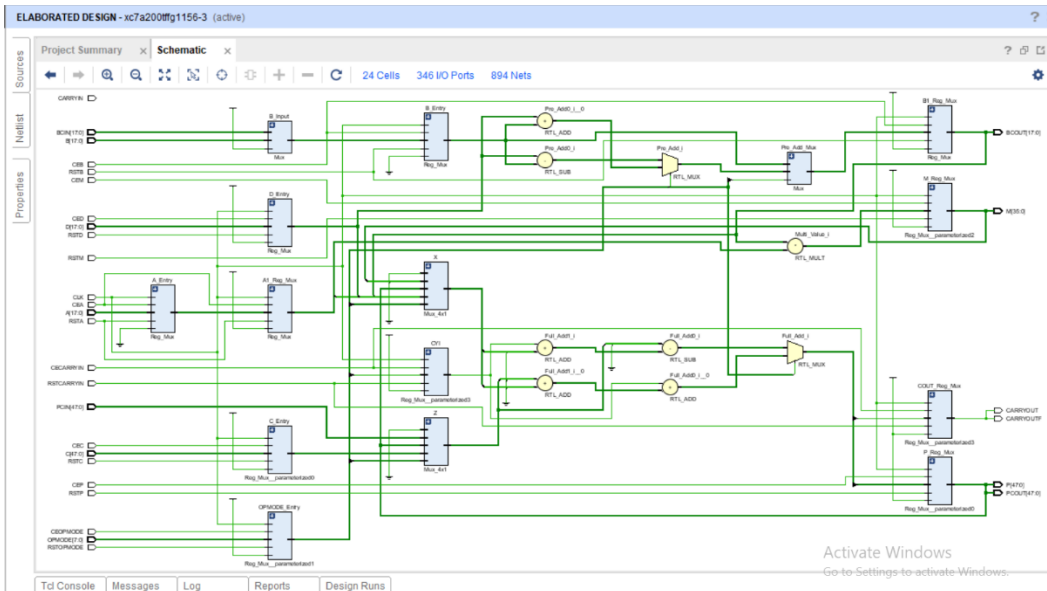
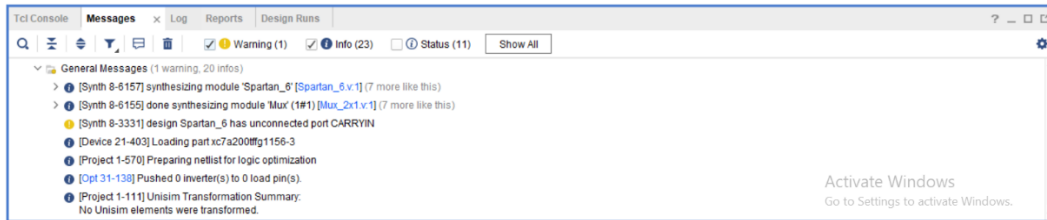


5-Constraint File

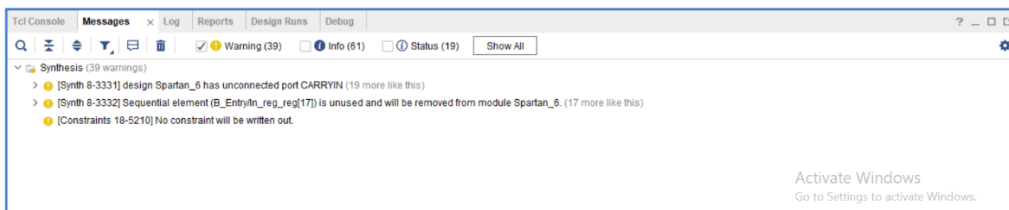
```
1 ## This file is a general .xdc for the Basys3 rev B board
2 ## To use it in a project:
3 ## - uncomment the lines corresponding to used pins
4 ## - rename the used ports (in each line, after get_ports) according to the top level signal names in the project
5
6 ## Clock signal
7 set_property -dict { PACKAGE_PIN W5    IOSTANDARD LVCMOS33 } [get_ports CLK]
8 create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports CLK]
```

6-Vivado Snippets

6.1 - Elaboration ("Messages" tab & Schematic snippets)



6.2 - Synthesis ("Messages" tab, Utilization report & Schematic snippets)



The Utilization report window displays the hierarchy of the design, showing the utilization of various resources across different modules. The report is organized into a table with columns for Name, Slice LUTs, Slice Registers, DSPs, Bonded IOB, and BUFGCTRL.

Name	Slice LUTs (134600)	Slice Registers (269200)	DSPs (740)	Bonded IOB (500)	BUFGCTRL (32)
Spartan_6	230	160	1	327	1
A1_Reg_Mux (Reg_Mux)	0	18	0	0	0
B1_Reg_Mux (Reg_Mux)	0	18	0	0	0
C_Entry (Reg_Mux_p)	0	48	0	0	0
COUT_Reg_Mux (Reg_Mux)	0	1	0	0	0
CY1 (Reg_Mux_para)	1	1	0	0	0
D_Entry (Reg_Mux_2)	0	18	0	0	0
OPMODE_Entry (Reg_Mux)	210	8	0	0	0
P_Reg_Mux (Reg_Mux)	0	48	0	0	0
Pre_Add_Mux (Mux)	19	0	0	0	0

Spartan_6 - ID:Engineering\ASU\3_Summer2\Kareem_Waseem\Project_1\VIAD0\Spartan_6\Spartan_6.xpr - Vivado 2019.2

File Edit Flow Tools Reports Window Layout View Help Quick Access

SYNTHESIZED DESIGN - xc7a200t#g1155-3 (active)

Report Methodology Report DRC Report Noise Schematic

SYNTHESIS

- Run Synthesis
- Open Synthesized Design
 - Constraints Wizard
 - Edit Timing Constraints
 - Set Up Debug
 - Report Timing Summary
 - Report Clock Networks
 - Report Clock Interaction
 - Report Methodology
 - Report DRC
 - Report Noise
 - Report Utilization
 - Report Power
 - Schematic

IMPLEMENTATION

- Run Implementation
- Open Implemented Design

Sources

- Spartan_6
 - Leaf Cells (332)
 - A1_Reg_Mux (Reg_Mux)
 - B1_Reg_Mux (Reg_Mux_0)
 - C_Entry (Reg_Mux_parameterized0)
 - COUT_Reg_Mux (Reg_Mux_parameterized3)
 - CW (Reg_Mux_parameterized3_1)

Netlist

Net Properties

Name: OPMODE_EntryIn_reg_reg_n_0_2

General Properties Connectivity Power

Schematic

338 Cells 346 IO Ports 781 Nets

Tcl Console Messages Log Reports Design Runs Timing Debug

Design Timing Summary

General Information

Timer Settings

Design Timing Summary

Clock Summary (1)

Check Timing (336)

Intra-Clock Paths

Inter-Clock Paths

Other Paths Groups

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 5.168 ns	Worst Hold Slack (WHS): 0.182 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 106	Total Number of Endpoints: 106	Total Number of Endpoints: 162

All user specified timing constraints are met.

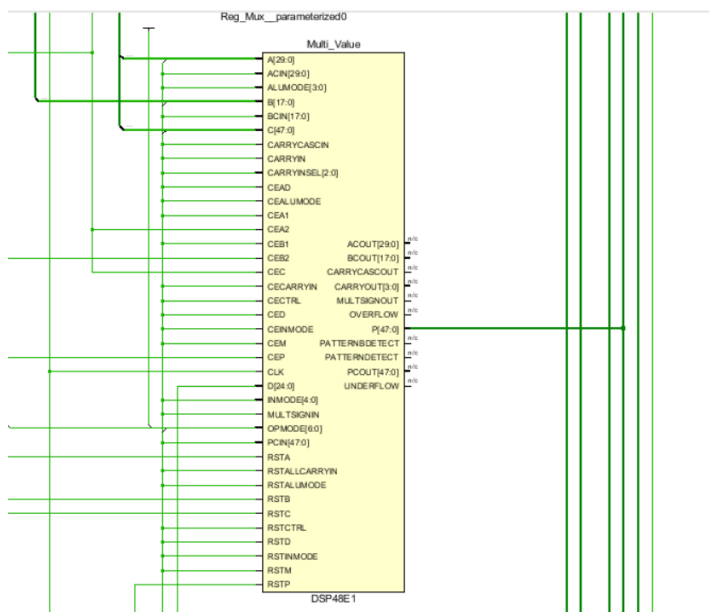
Activate Windows
Go to Settings to activate Windows.

SYNTHESIZED DESIGN - xc7a200t#g1155-3 (active)

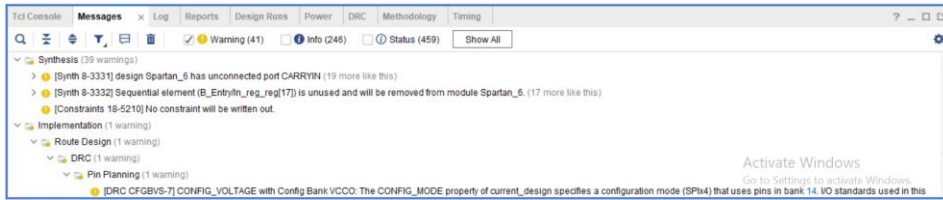
Schematic

338 Cells 346 IO Ports 781 Nets

Activate Windows
Go to Settings to activate Windows.



6.3 - Implementation (“Messages” tab, Utilization report, timing report & device snippets)



UTILIZATION - xc7a200tsg1156-3 (active)

Name	Slice LUTs (133800)	Slice Registers (267600)	Slice (33450)	LUT as Logic (133800)	LUT Flip Flop Pairs (133800)	DSPs (740)	Bonded IOB (500)	BUFGCTRL (32)
Spartan_6	229	179	100	229	50	1	327	1
A1_Reg_Mux (Reg_Mux)	0	18	7	0	0	0	0	0
B1_Reg_Mux (Reg_Mux)	0	36	11	0	0	0	0	0
C_Entry (Reg_Mux_p)	0	48	13	0	0	0	0	0
COUT_Reg_Mux (Reg_Mux)	0	2	2	0	0	0	0	0
CWI (Reg_Mux_para)	1	1	1	1	1	0	0	0
D_Entry (Reg_Mux_2)	0	18	5	0	0	0	0	0
OPMODE_Entry (Reg_Mux)	210	8	65	210	0	0	0	0
P_Reg_Mux (Reg_Mux)	0	48	12	0	0	0	0	0
Pre_Add_Mux (Mux)	18	0	10	18	0	0	0	0

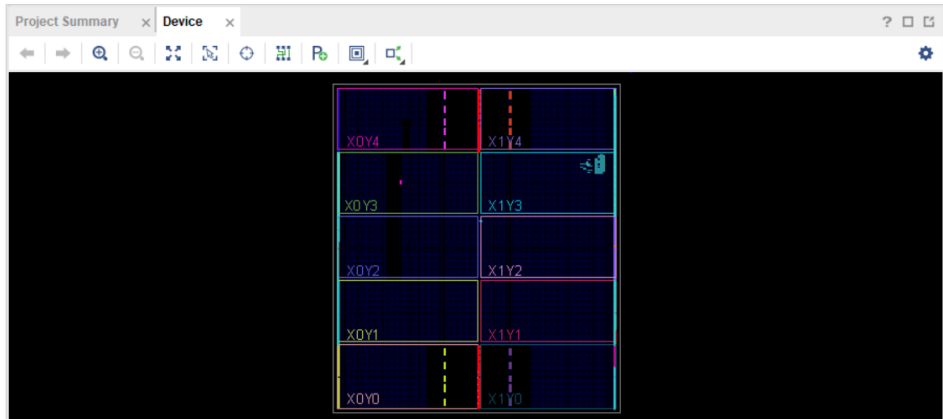
Project Summary

Implementation Complete

Timing Summary

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 3.574 ns	Worst Hold Slack (WHS): 0.225 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 125	Total Number of Endpoints: 125	Total Number of Endpoints: 181

All user specified timing constraints are met.



7-QuestaLint Snippets

Questa Lint 2021.1 (C:/Kareem_Waseem/Project_1/Q_LINT/lint.db)

File Edit View Lint Checks Window Help

Design D:/Engineering/ASU/3 Summer2/Kareem_Waseem/Project_1/Q_LINT/Spartan_6.v [Spartan_6]

Search: Type Search...

Instance Module

Spartan_6 (15) Spartan_6

```
1 module Spartan_6
2   A, B, D, C
3   , CLK, CARRYIN
4   , OPMODE, BCIN, RSTA, RSTB, RSTM, RSTP, RSTC, RSTD, RSTCARRYIN, RSTOPMODE
5   , CEA, CEB, CEM, CEP, CEC, CED, CECARRYIN, CEOPMODE
6   , PCIN
7   , BCOUT, PCOUT, P, M, CARRYOUT, CARRYOUTF
8 );
9
10 //parameters for A and B inputs that define whether the mux out is reg or not (SELECT)
11 parameter A0REG = 0;
12   0
13 parameter B0REG = 0; //0 refers to no registers
14   0
15 parameter A1REG = 1; //1 refers to registers
16   1
17 parameter B1REG = 1;
18   1
19
20 //parameters for C,D,M,P,CARRYIN,CARRYOUT,OPMODE that define whether the mux out is
21 parameter CREG = 1;
22   1
23 parameter DREG = 1;
24   1
25 parameter MREG = 1;
26   1
27 parameter PREG = 1;
28   1
```

Flow Navigator Design

Lint Summary (Type Search Text (Press Enter))

Name	Count
Open(uninspected, pendi...	18 (25)
Warning	7
Info	11 (18)

Lint Checks

Filter: Type here

Waived Fixed Pending 2/ Uninspected Bug Verified Total : 18 Selected : 0

Severity	Status	Check	Alias	Message	Module	Category	State	Owner	STARC Reference
Warning	2	mux_select_const		Constant value drives mux select pin. Signal B_Input...	Mux	Connectivity	open	unassign...	
Warning	2	mux_select_const		Constant value drives mux select pin. Signal CY1.Out, ...	Reg_Mux	Connectivity	open	unassign...	
Warning	2	mux_select_const		Constant value drives mux select pin. Signal C_Entry...	Reg_Mux	Connectivity	open	unassign...	
Warning	2	mux_select_const		Constant value drives mux select pin. Signal D_Entry...	Reg_Mux	Connectivity	open	unassign...	
Warning	2	mux_select_const		Constant value drives mux select pin. Signal M_Reg...	Reg_Mux	Connectivity	open	unassign...	
Warning	2	mux_select_const		Constant value drives mux select pin. Signal OPMOD...	Reg_Mux	Connectivity	open	unassign...	

Transcript Message Viewer Lint Checks Design Metrics Design Information Status History Lint Dashboard

...n_6.v [Spartan_6]