Small-Project

The manager of the *PipeLine* Company, located in north coast, is proposing to install an embedded system to monitor the temperature of the pipe lines and report temperature to database system. The proposed system, *PipeTemp*, is to display information about the status of the pipe line. Detailed specification is as follows:

- The temperature range is around 100 - 300 C.
- In normal operation, the temperature is reported to database using UART Communication every 15 minutes.
- The system should produce an alarm after 250 C, at 300 C it gives a signal to shut down the production process.
- A responsible person should have the capability of resetting the system.

The design team has met few times to decide on the following for the *PipeTemp* architecture:

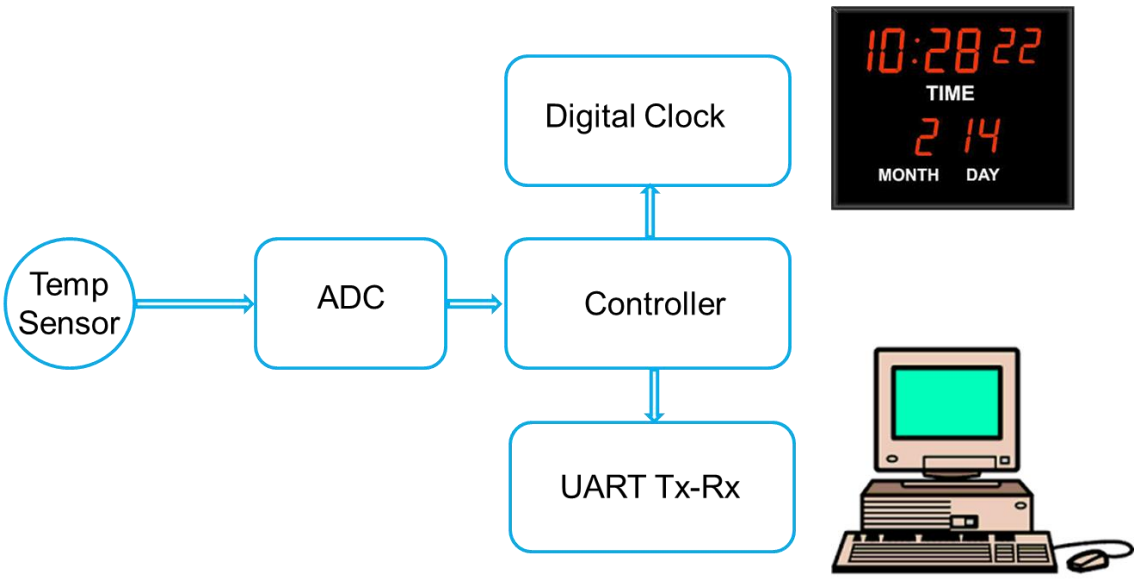
- It was decided to use a small FPGA, Cmod S6 [1], to implement the *PipeLine* Embedded System. This decision is based on that system will be extended in the future and more specifications will be added.
- Your team leader asks you to develop the controller (FSM), UART Communication with PC and a digital clock, since reporting temperature data is including time and date.
- In this design, the temperature is reported by 8-bits ADC.

In this project, you are going to model the operation of *PipeTemp* and verify it via simulation. Then, you will synthesis the model. Here is the list of deliverables:

a) In a table, identify *PipeTemp* inputs and outputs and briefly describe their meaning and possible values.
b) Draw an icon for the *PipeTemp*, clearly showing its input and output signals.
c) Report the accuracy of the system according to 8-bits ADC and temperature sensor. Do you suggest a certain sensor, if not what is the limitation do you think for the sensor.
d) Deliver the Verilog models for your design.
e) Design a testbench to verify the operation of the *PipeTemp,* Provide the test vectors and test plan for your implementation.
f) Synthesize the *PipeTemp* architecture. Include a diagram of the synthesize output with your submision.

Hint:

- You need to implement the UART Tx and Rx.
- You need to implement PLL on FPGA in order to adjust timing.
- When you connect Led for alarm or seven segments for digital clock to FPGA, you should take care about the maximum current that can be drawn from FPGA pin.



Reference:

[1] **https://www.digilentinc.com/Products/Detail.cfm?NavPath=2,400,1227&Prod=CMOD-S6**