COMPUTER ARCHITECTURE

[CSE311s]

PIC-8259A REPORT

TEAM 23:

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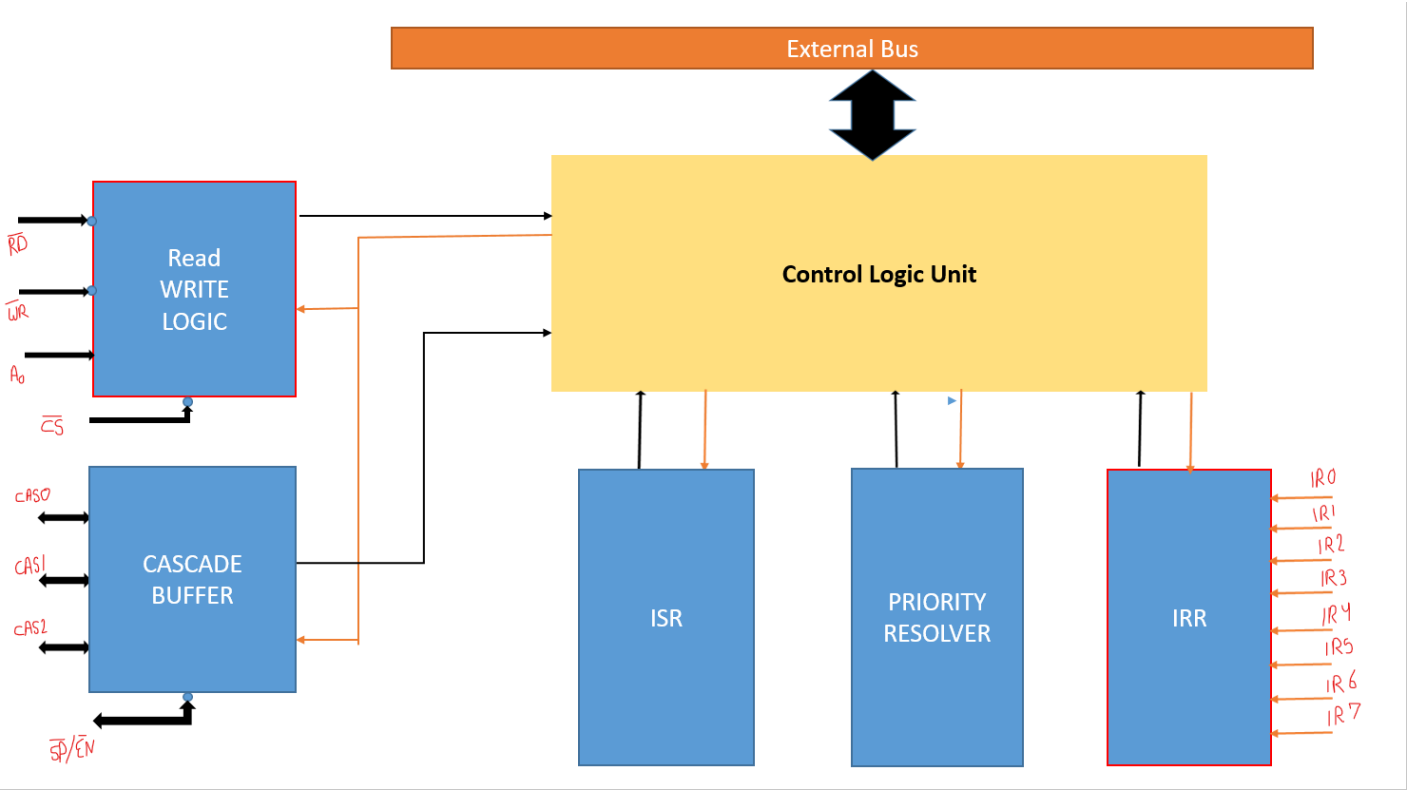
For more details GitHub Rep link: https://github.com/omardoesart/PIC-8259.git

Content of Project

Block Diagram

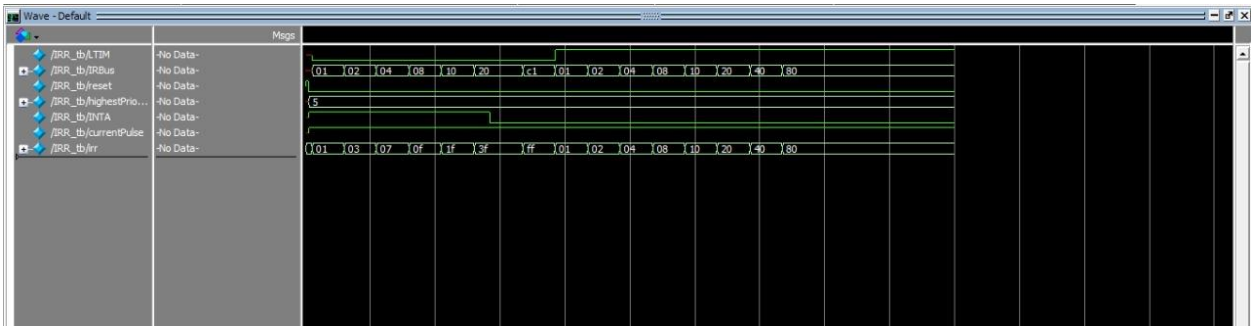


Interrupt Request Reg (IRR)

Signals Description:

Name	Direction	Description
reset	Input	Resets signal to initial state
LTIM	Input	For determining whether it will be edge or level triggered
IRBus	Input	Vectorized input for interrupt signals
highestPriority	Input	Input priority signal
INTA	Input	Input active low signal
currentPulse	Input	Input signal indicating current pulse
irr	Output reg	Interrupt request register

Snapshots for simulation wave:

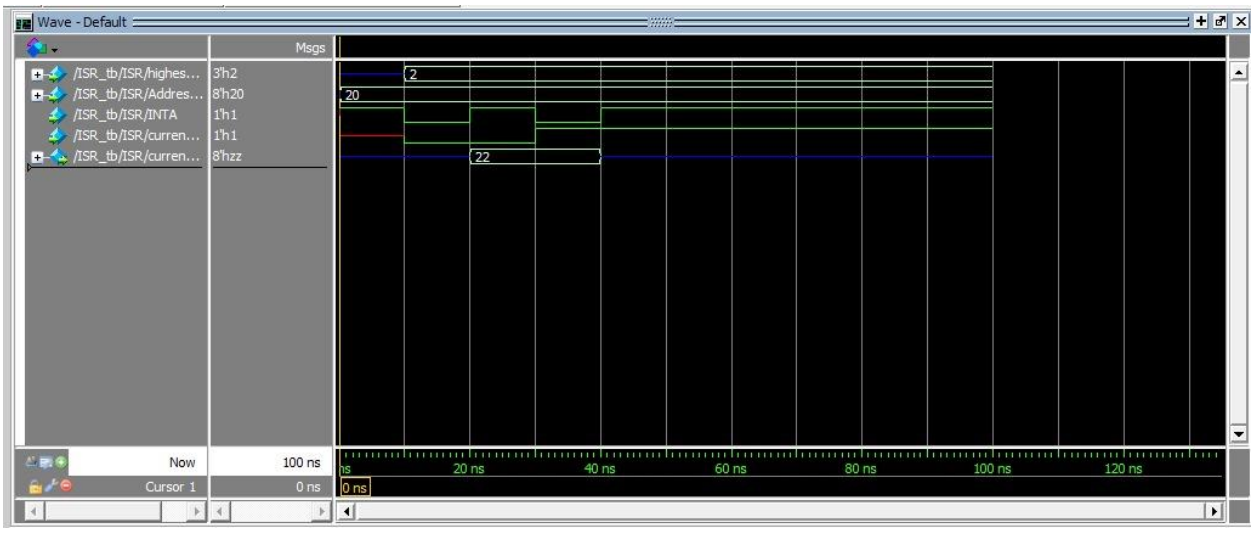


In Service Reg (ISR)

Signals Description:

Name	Direction	Description
highestPriority	Input	Input priority signal
AddressBase	Input	Input address base signal coming from the ICW2 T7-T3 pins
INTA	Input	Input active low signal
currentPulse	Input	Input signal indicating current pulse
currentAddress	Output reg	Output address signal
highestPriority	Internal	Internal signal to store the highest priority
AddressBase	Internal	Internal signal to store the AddressBase

Snapshots for simulation wave:

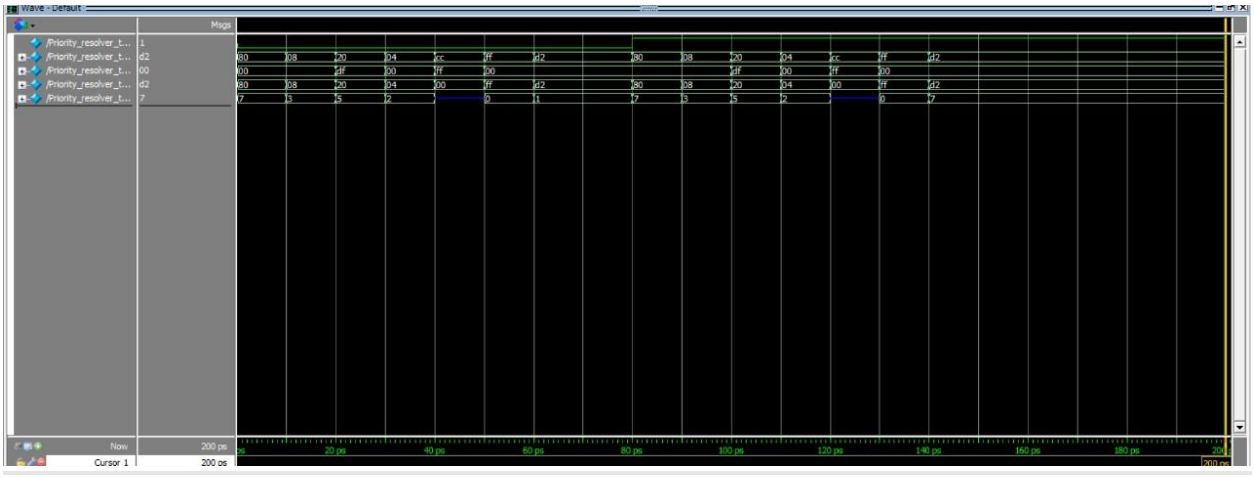


Priority Resolver

Signals Description:

Name	Direction	Description
autoRotateMode	Input	Auto rotate mode signal
irr	Input	Interrupt request register signal
imr	Input	Interrupt mask register signal
highestPriority	Output reg	Output signal representing the highest priority interrupt
maskedIRR	Wire	Result of irr & (~imr) operation
dataHighImpedance	Reg	Flag indicating whether the data bus is in high impedance
highestPriorityPos	Reg [2:0]	Position of the highest priority interrupt

Snapshots for simulation wave:

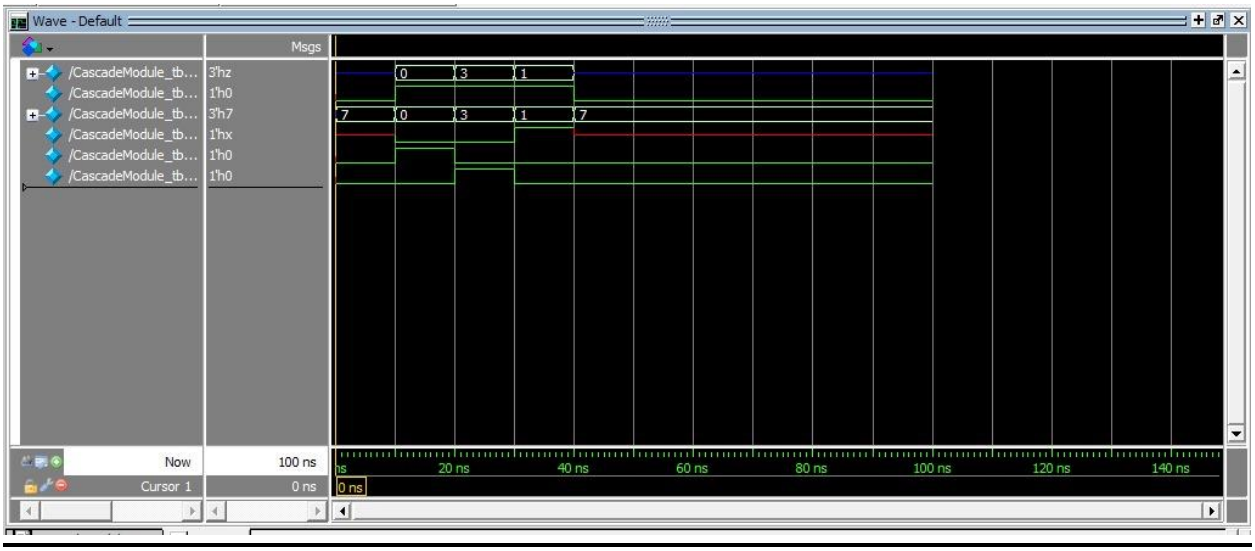


Cascade Buffer

Signals Description:

Name	Direction	Description
SP	Input	1 for master, 0 for slave
SNGL	Input	1 for single, 0 for cascade
ICW3	Input	Master: port numbers of slaves, Slave: interrupt location
Interrupt_Location	Input	Interrupt location with the highest priority
interruptExists	Input	1 if there is an interrupt
CAS	Inout	Current active slave
Address_Write_Enable	Output	1 if this module should write to the bus
isSingle	Internal	Computed: SNGL == 1'b1
isMaster	Internal	Computed: SP == 1'b1
CAS_Reg	Internal	Register for storing the current active slave

Snapshots for simulation wave:



Read Write logic

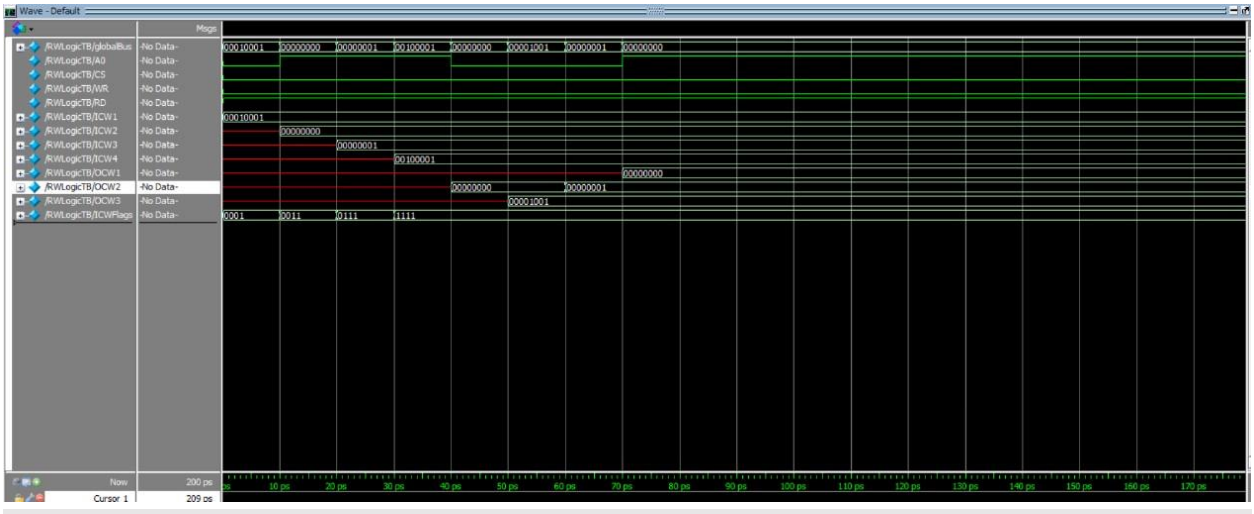
Signals Description:

Name	Direction	Description
globalBus	Input	8-bit global bus
A0	Input	Indicates the command words
CS	Input	Chip select (active low)
WR	Input	Write signal (active low)
RD	Input	Read signal (active low)
ICW1	Output	ICW1 register
ICW2	Output	ICW2 register
ICW3	Output	ICW3 register
ICW4	Output	ICW4 register
OCW1	Output	OCW1 register
OCW2	Output	OCW2 register
OCW3	Output	OCW3 register
ICWFlags	Output	4-bit flags to check if ICW1, ICW2, ICW3, ICW4 have been written to
shouldInitiateFlags	Output	Flag to indicate if ICWFlags should be reset
chipSelected	Internal	Computed: ~CS
writeSignal	Internal	Computed: ~RD
readSignal	Internal	Computed: ~WR

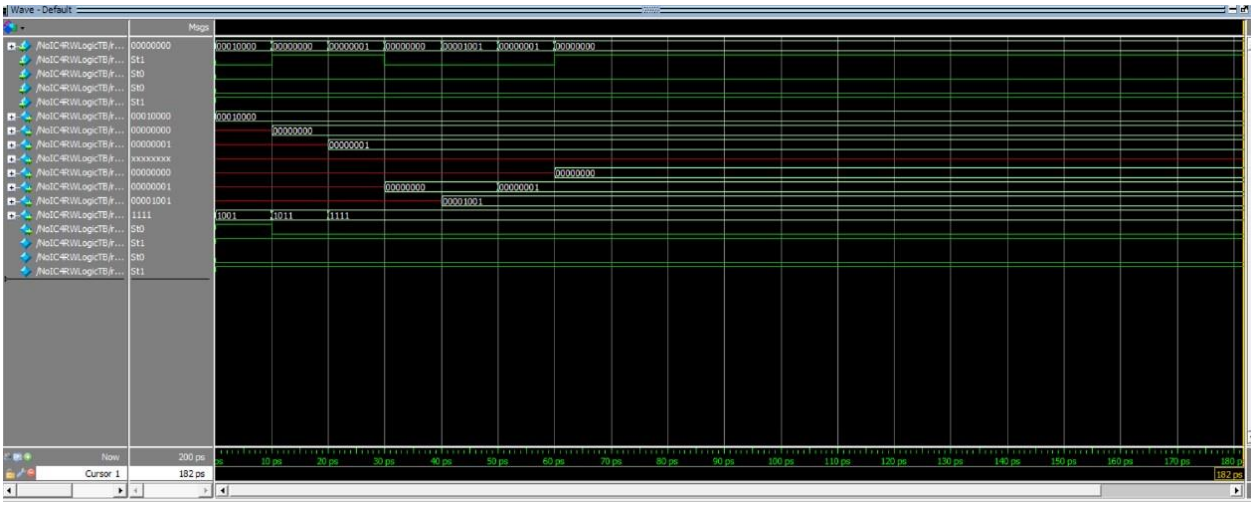
Read Write logic

Snapshots for simulation wave:

RWLogicTB



NoIC4RWLogicTB



Control Logic

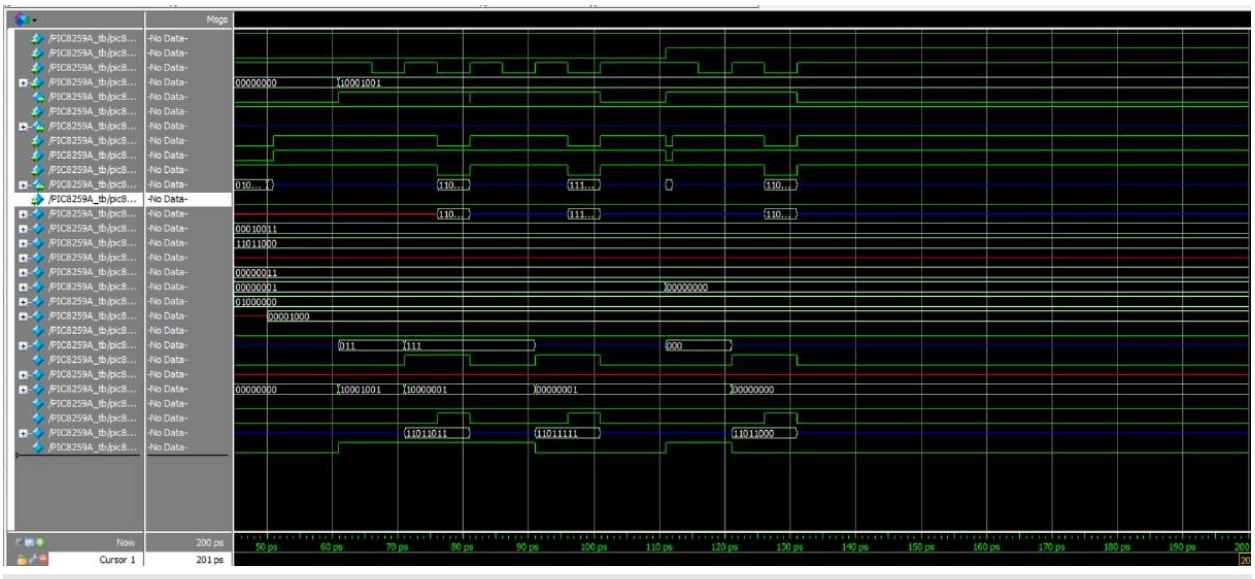
Signals Description:

Name	Direction	Description
VCC	Input	5V power supply or 1 in simulation
A0	Input	Address line 0
INTA	Input	Interrupt acknowledge
IRBus	Input	Interrupt request bus
INT	Output	Interrupt output
SPEN	Input	Used for cascading, buffer control is ignored in this simulation
CASBus	Inout	Cascade bus
CS	Input	Chip select
WR	Input	Write signal
RD	Input	Read signal
DBus	Inout	Data bus
GND	Input	Ground or 0 in simulation
ICW1, ICW2, ICW3, ICW4	Internal	ICW registers (input to RWLogic)
OCW1, OCW2, OCW3	Internal	OCW registers (output from RWLogic)
shouldInitiateFlags	Internal	Flag to indicate if flags should be initiated
highestPriority	Internal	Highest priority interrupt
currentPulse	Internal	Current pulse for interrupt handling
shouldSendStatus	Internal	Status sending control signal
irr	Internal	Interrupt request register
DBusReg	Internal	Register for data bus
ISROutput	Internal	Output from ISR module (address for data bus)
interruptExists	Internal	Flag indicating if an interrupt exists

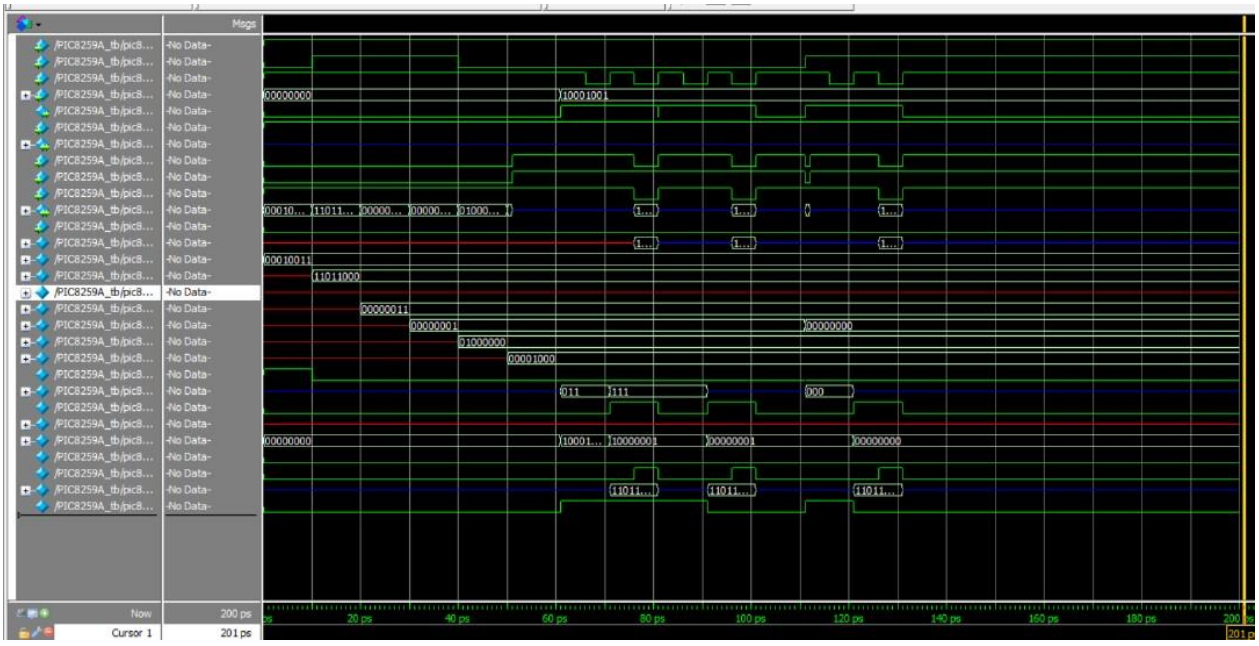
Control Logic

Snapshots for simulation wave:

PIC8259A_tb



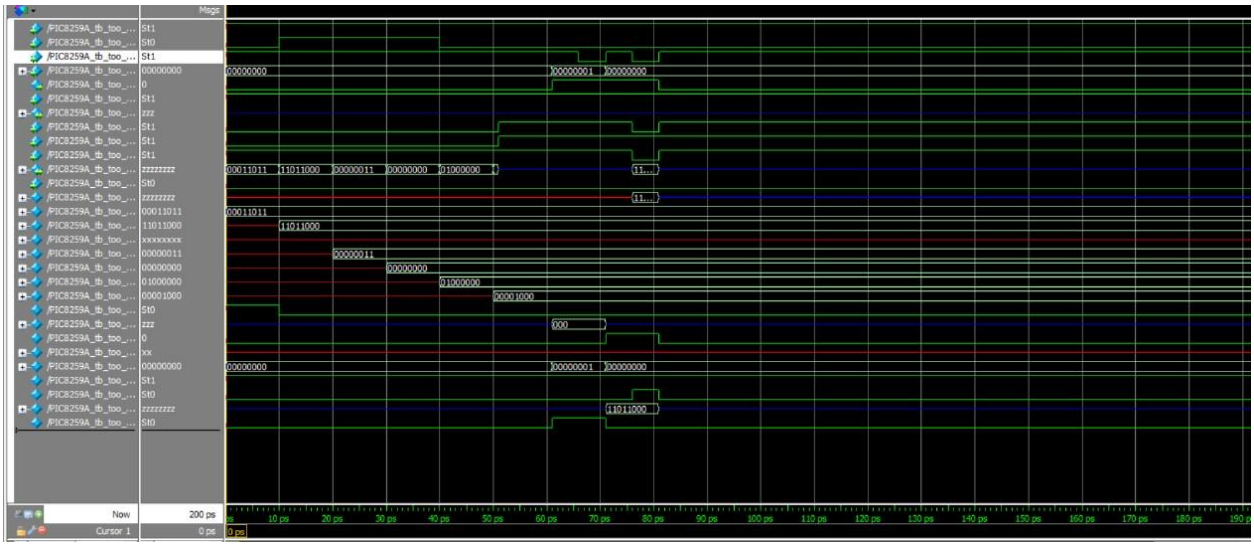
PIC8259A_tb_level_trigger



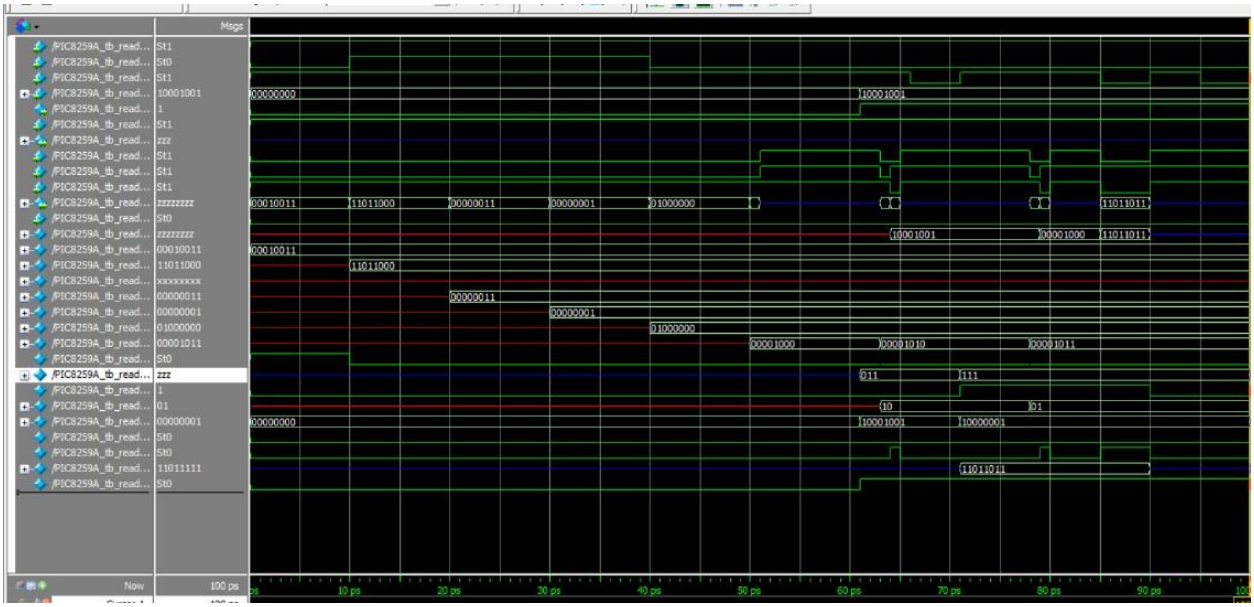
Control Logic

Snapshots for simulation wave:

PIC8259A_tb_too_soon



PIC8259A_tb_read_status



Description of Testing

i. All initialization command words and OCW1 are sent from 8086 to the RW and are saved on registers in the read write logic and sent to control block and is able to receive other OCWs at any other time.

ii. When an interrupt is received, the priority resolver automatically chooses the highest priority request and sends the vector address to the control block.

iii. the control block sends begins the interrupt process by raising the INT signal to the 8086 and sends the vector address on the data bus and
control will set itself into busy mode.

iv. 8086 will send an acknowledge signal to the control block so the ISR will save the current interrupt request in service and the IRR will get updated.

v. 8086 will send a second acknowledge signal to the control block so the address will get pushed onto the bus and then control marks process as done.

For cascading mode:

i. When an interrupt is received, the priority resolver automatically chooses the highest priority request and sends the vector address to the control block.

ii. the slave control block sends begins the interrupt process by raising the INT signal to the master control block.

iii. once the slave cascade block receives the CAS signal from the master control block, it will send the vector address on the data bus

Member Name		His Contribution
Mohaned Khaled Hassan	2001372	Cascade Buffer
Mohammed Montasser	2100416	Control Logic
Mohammed Magdy	2000927	IRR and ISR
Mostafa Hessin Ahmed	2000931	Read Write Logic
Omar Mohamed	2001109	Priority Resolver
Maged Mohamed	2001951	Simulation, Testing bench of read write, Report (Leader)