



Milestone 2 Report

AUTOMATIC CLOCK GATE

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➤ ***Plan***

We will synthesize a Verilog file using the yosys tool, this will give us the gate level netlist. Then we will take this and ask the user to enter the name of the clock gate cell in the library they are using. Then in the gate level netlist we will replace the input multiplexers for the flip flops with a clock gating cell that acts as an enable for the flip flops. This should decrease the circuit power consumption.

➤ ***Libraries and Languages***

We're going to utilize the pyverilog library in the python language. This will allow us to parse and manipulate the gate level netlist.