



AIN SHAMS UNIVERSITY

FACULTY OF ENGINEERING

International Credit Hour Programs (ICHEP)

Computer and Systems Engineering Program

Summer 2019

Course Code: CSE012/ENGR120/CSE031

Time allowed: 3Hrs.

Engineering computation

The Exam Consists of Five Questions in Two Pages. Maximum Marks: 40 Marks

1 / 2

تعليمات هامة

- حيازة telephones المحمول مفتوحا داخل لجنة الامتحان يعتبر حالة غش تستوجب العقاب وإذا كان ضروري الدخول بالموصل فيوضع مغلق في الحقائب.
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Question (1): [6 marks]

Briefly explain each of the following terms showing its use/functionality: [1 mark each]

- Embedded Computers.
- Cache memory.
- Video card.
- Hub.
- Laser beam in a laser printer.
- Color depth.

Support your answer with three examples for parts a, and f.

Question (2): [6 marks]

Calculate the result of each of the following (Show the calculations steps). [1 mark each]

- The decimal value of $(11001010)_2$ if it is represented in sign -magnitude form, and its value if it is represented in two's complement form.
- The result in binary of $(2^{10})_{10} - (2^{12})_{10}$ in two's complement form.
- The value of b if $(603)_b = (751)_8$.
- The value in hexadecimal of ((NOT X) XOR Y), when X= 77, and Y = 220. X and Y are declared as unsigned char.
- The size of A 65536 colors 1024x1024 pixels image file in mega bytes.
- The size in Mega bytes of A 3 seconds 200x150 video file recorded at 15 fps with an 8-bit color depth (without sound).

Question (3): [10 marks]

- Write a C program that accepts two numbers x, and y and prints a rectangular of width x, and height y. For example, if x = 4, and y = 6, the output should be as shown below [5 Marks]
- Write the output from the following C program, when x = 10, 20, 30, 40, 50. [5 Marks]

```
#include "stdio.h"

int main()
{
    int x;
    scanf("%d", &x);
    switch (x) {
        case 10:
            x++;
        case 20:
            x--;
            break;
        case 30:
            x -= 20;
        case 40:
            x += 20;
            break;
        default:
            x = 500
    }
    printf("\n x = %d", x);
}
```

```
*****
*****
*****
*****
*****
*****
```

Width=4, Height=6

Question (4): [12 marks]

For the system operation shown in the following table, calculate the average turn-around time, the average waiting time, and the average response time in case of using:

- a) Preemptive SJF scheduling
- b) Non-Preemptive SJF scheduling.

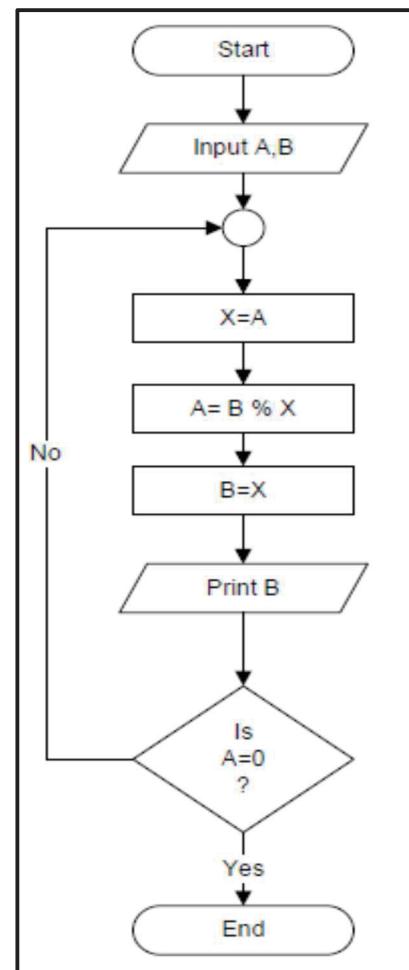
[6 Marks]
[6 marks]

Process#	Arrival Time	CPU Time
1	9:00	30
2	9:15	14
3	9:25	14
4	9:26	2

Question (5): [6 marks]

The flowchart shown finds the greatest common divisor of two numbers A, and B ($A > 0$, and $B > 0$).

Write the output of the program represented by the flow chart if the inputs (A,B) are (140,48):





AIN SHAMS UNIVERSITY
FACULTY OF ENGINEERING
i- CREDIT HOURS ENGINEERING PROGRAMS
MECHATRONICS PROGRAM

Summer Semester 2019

Course Code: CSE115

Time allowed: 3Hrs.

Digital Design

The Exam Consists of **Five Questions in Four Pages.**

Maximum Marks: 40 Marks

1 / 4

تعليمات هامة

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Question (1): [7 marks]

A) Choose the correct answer

[2 marks]

1) Using DeMorgan's law, $F(A, B, C, D) = [(AB + C) D']'$ will be equals to

- | |
|----------------------|
| a) $A' + B'C' + D$ |
| b) $A'C' + B'C' + D$ |
| c) $A' + B' + C + D$ |
| d) $(A' + B'C') D$ |

2) Given a **lowest** priority 4×2 encoder, in order to have a value 1 0 on its outputs, its inputs $D_0 - D_3$ can be equal to respectively.

- | | | | |
|---------------|---------------|---------------|---------------|
| a) x, x, 1, 0 | b) 0, 1, x, x | c) x, 1, 0, 0 | d) 0, 0, 1, x |
|---------------|---------------|---------------|---------------|

3) For a $8M \times 16$ RAM the number of output OR gates equals.....

- | | | | | |
|-------|------|-------|------|------|
| a) 8M | b) 8 | c) 16 | d) 4 | e) 3 |
|-------|------|-------|------|------|

4) For a $8M \times 16$ RAM, the number of address lines equal

- | | | | | |
|------|-------|-------|-------|------|
| a) 8 | b) 16 | c) 23 | d) 13 | e) 3 |
|------|-------|-------|-------|------|

B) Simplify the following function using Kmap

$$F(A, B, C, D) = BC' + A'B'C + A'CD + ACD$$

[3 marks]

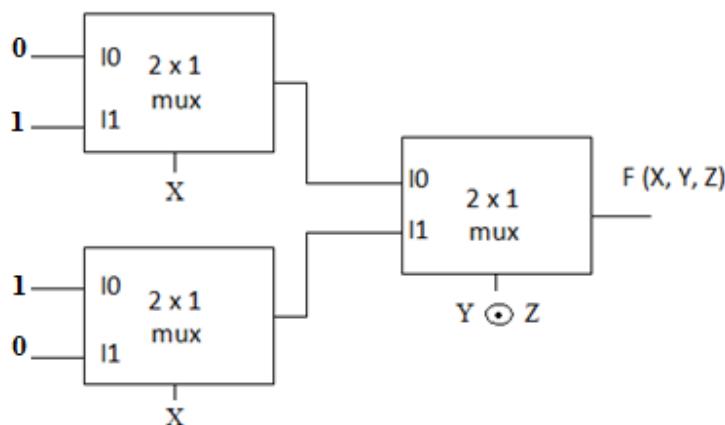
C) Implement the following truth table using suitable ROM. (show full ROM diagram)

[2 marks]

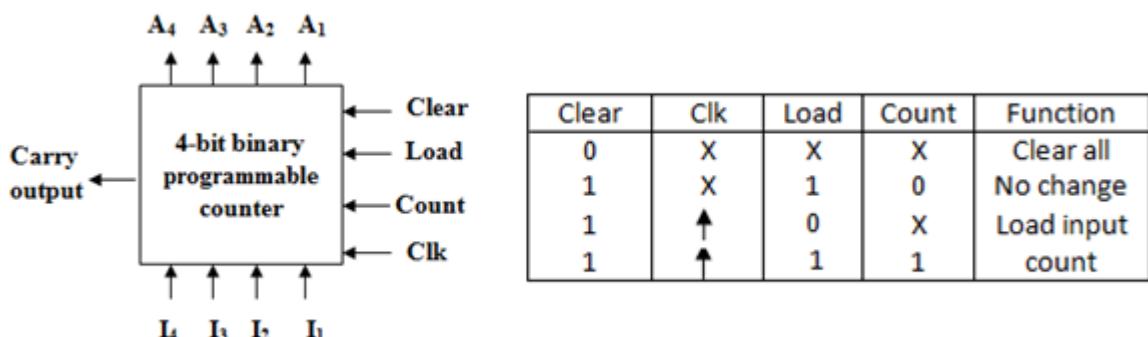
I_2	I_1	I_0	A_3	A_2	A_1	A_0
0	0	0	0	0	0	1
0	0	1	0	0	0	0
0	1	0	1	0	1	0
0	1	1	0	1	0	1
1	0	0	1	1	1	1
1	0	1	1	0	1	0
1	1	0	0	0	0	1
1	1	1	1	0	1	0

Question (2): [7 marks]A) Analyze the following function and find $F(X, Y, Z)$.

[4 marks]



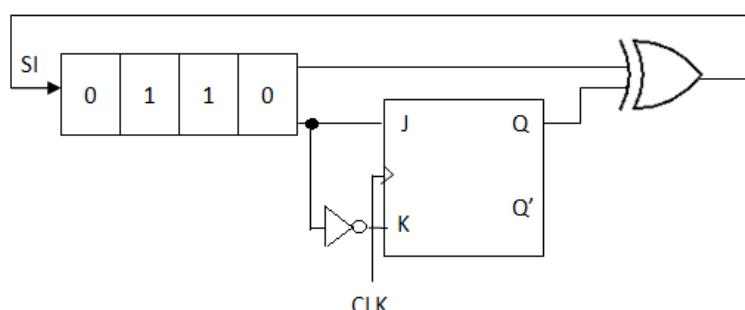
- B) Using the following counter-module with the given function table, show the full connection to obtain a divider by 7 using Carryout. [3 marks]

**Question (3): [9 marks]**

- A) Design a counter that counts the sequence 1, 3, 4, 2 and 7 using T flipflops . [6 marks]

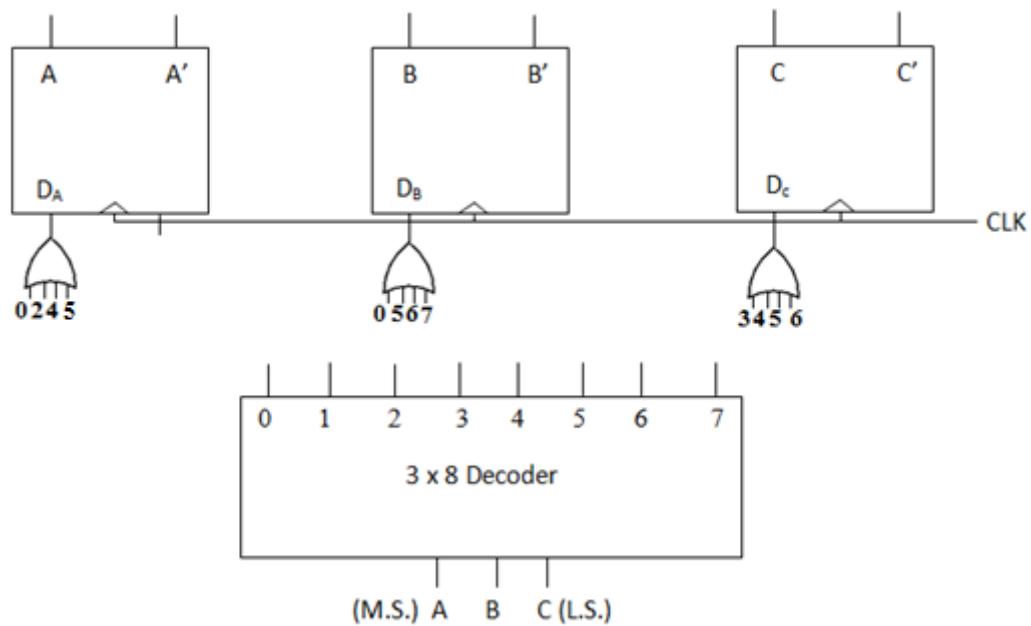
- B) Find the content for the 4-bit shift register of the following sequential circuit during 4 clocks.

[The initial value for Q is zero] [3 marks]

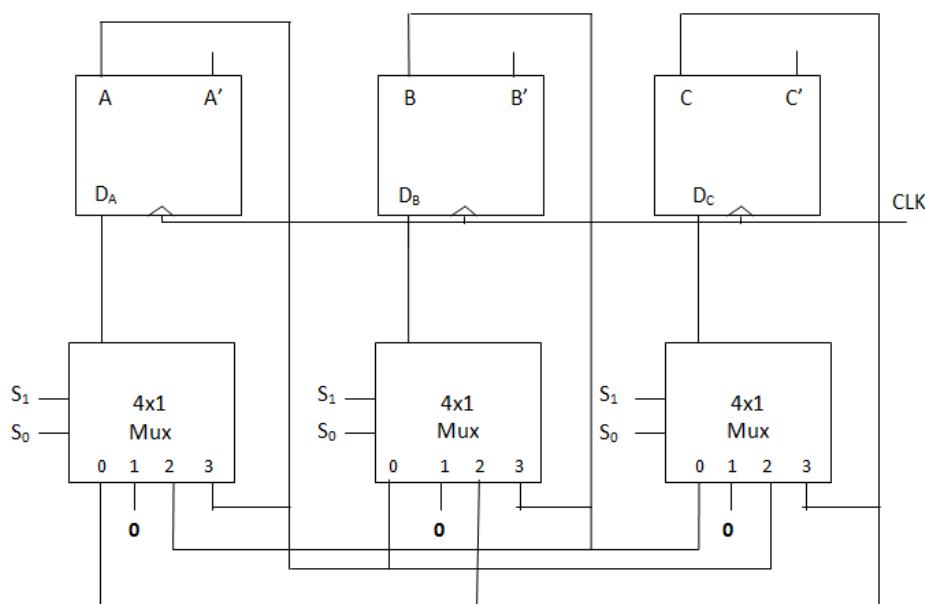


Question (4): [9 marks]

- A) Analyze the following counter circuit then find its state table, state diagram and the repeated sequence. Is it a selfcorrecting counter ? why? [6 marks]

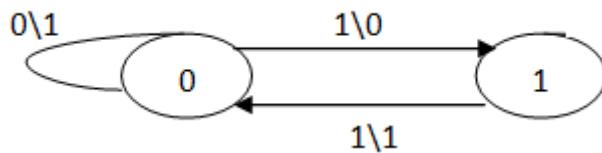


- B) Follow the circuit connections, then find the function table of the given universal shift register of 4 different functions. (All muxs have the same selection control). [3 marks]



Question (5): [8 marks]

A) Design a sequential circuit according to the following state diagram using JK flip flops. [5 marks]



B) Implement the following Function using 8x1 mux and let W, X and Z be the selectors

$$F(W, X, Y, Z) = \sum(0, 2, 4, 5, 6, 7, 10, 12)$$

[3 marks]

AIN SHAMS UNIVERSITY

FACULTY OF ENGINEERING

International Credit Hour Programs (ICHEP)

**Program of Communication Systems and Mechatronics Engineering
and Automation**



Summer 2019

Course Code: CSE 122, CSE 125, CSE131

Time allowed: 3 Hrs.

Computer Programming

The Exam Consists of Six Questions in Two Pages.

Maximum Marks: 40 Marks

1 / 2

تعليمات هامة

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Try All Questions and Assume Any Missing Information

Question (1):

[6 Marks]

Evaluate the following programs step by step explaining the change of the corresponding variables as well as the screen output.

<u>(a)</u>	<u>(b)</u>
<pre> int exam(int n) { if (n == 1) return 3; cout << n << endl; int x = n * exam(n - 3); cout << x << endl; return (n + x); } int main() { int x = exam(7); cout << x << endl; return 0; } </pre>	<pre> void main () { char c; for (c='a'; c<'g'; ++c) { switch (c) { case 'a': c += 2; case 'c': c += 1; case 'g': ++c; cout << c-- << endl ; default:++c; } cout << c << endl ; } </pre>

Question (2):**[7 Marks]**

Write a C program that takes a number n and displays the opposite pattern for n=3:

0
1 0
2 1 0
3 2 1 0 ...
4 3 2 1 0 ..
5 4 3 2 1 0 .
6 5 4 3 2 1 0

Question (3):**[7 Marks]**

Write a C++ function that calculates the histogram of numbers in an input array as demonstrated in the following example.

For example, if the given array is {-1, -1, 5, 5, 80, 70, 70, -1}, then the output will be:

-1	3
5	2
80	1
70	2

Question (4):**[7 Marks]**

Write a program to replace a substring by another substring in a given string:

For example, if the given string is “abc12abdfabc” and it is required to replace the substring “abc” with the string “wxyz” then the output string will be “wxyz12abdfwxyz”.

Question (5):**[6 Marks]**

Write a program to read a 100x100 2D array of integer numbers from the user. Then search and count the number of values that satisfy the following condition: All 8 neighbors' values are less than the center value.

..
..	1	3	6	..
..	3	7	5	..
..	3	3	4	..
..

Accepted

..
..	2	9	9	..
..	5	3	8	..
..	6	4	7	..
..

Rejected

Question (6):**[7 Marks]**

Write function that translates a text to Pig Latin. English is translated to Pig Latin by taking the first letter of every word, moving it to the end of the word and adding ‘ay’.

For example, “The quick brown fox” becomes “heTay uickqay rownbay oxfay”.



AIN SHAMS UNIVERSITY
FACULTY OF ENGINEERING
i-CREDIT HOURS ENGINEERING PROGRAMS
COMPUTER ENGINEERING & SOFTWARE SYSTEMS PROGRAM

Summer Semester 2019

Course Code: CSE126

Time allowed: 3Hrs.

Computer Programming (2)

The Exam Consists of **Three Questions** in **Three Pages**.

Maximum Marks: 40 Marks

1 / 3

تعليمات هامة

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Question (1): [8 marks]

Choose the correct answer (**Only one. No credit otherwise**)

- a) Which among the following is **true**?
A) The private members can't be accessed by public members of the class. B) The private members can be accessed by public members of the class.
C) The private members can be accessed only by the private members of the class. D) The private members can't be accessed by the protected members of the class.
- b) A JavaFX action event handler contains a method _____.
A) public void actionPerformed(ActionEvent e) B) public void actionPerformed(Event e)
C) public void handle(ActionEvent e) D) public void handle(Event e)
- c) Which Feature of OOP illustrated the code reusability?
A) Polymorphism B) Abstraction
C) Encapsulation D) Inheritance
- d) Which of the following statements is true?
A) Methods declared in interfaces are implicitly private. B) Fields declared in interfaces are implicitly public, static and final.
C) Fields are not allowed to be declared in interfaces. D) An interface can only extend one interface.
- e) Which of the following expressions must be true if you create a thread using Thread = new Thread(object)?
A) object instanceof Thread B) object instanceof Frame
C) object instanceof Applet D) object instanceof Runnable
- f) Why do we need to handle exceptions?
A) To prevent abnormal termination of program. B) To encourage exception prone program.
C) To avoid syntax errors. D) To save memory.
- g) Any changes made to static data member from one member function
A) Is reflected to only the corresponding object. B) Is reflected to all the variables in a program.
C) Is reflected to all the objects of that class. D) Is constant to that function only.
- h) You can use the _____ method to force one thread to wait for another thread to finish.
A) sleep(long milliseconds) B) yield()
C) stop() D) join()

Summer Semester 2019	Course Code: CSE126	Time Allowed: 3 Hrs.
Computer Programming (2)		

The Exam Consists of **Three** Questions in **Three** Pages.

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Question (2): [17 marks]

- a) Consider the following code fragment:
- What is the relationship between class A and class B? [2 marks]
 - Draw the UML class diagram for the given code. [5 marks]

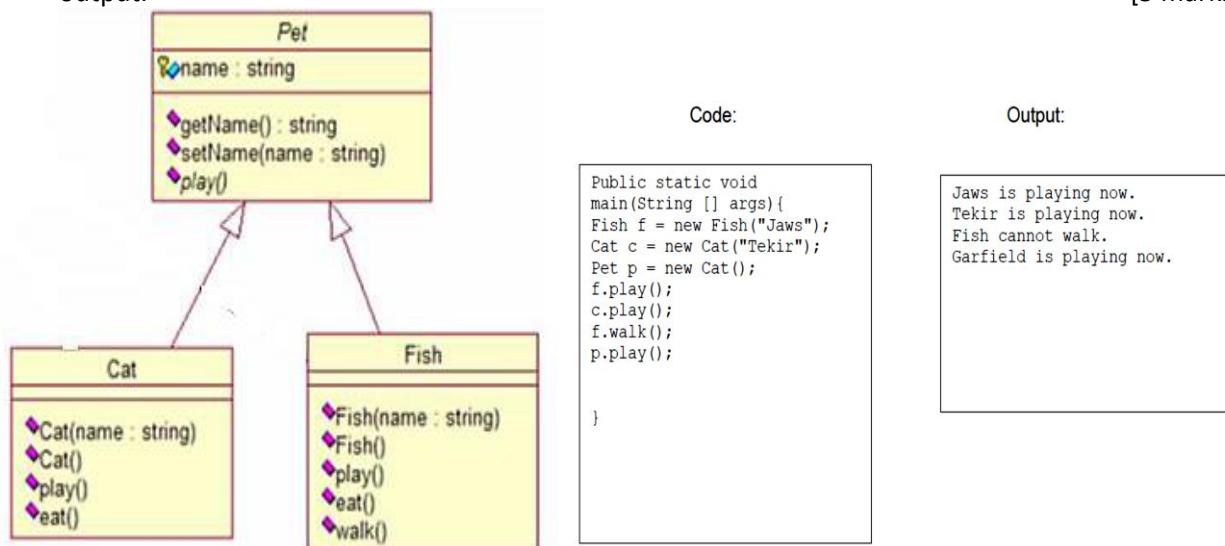
```

public class A
{
    private int a;
    protected int b;
    public int c;
    public A();
    public void seta(int new_a);
    public void setb(int new_b);
    public void setc(int new_c);
    public int geta();
    public int getb();
    public int getc();
}

public class B
{
    private A myA;
    private int d;
    public B();
    public void setd(int new_d);
    public int getd();
}

```

- b) Based on the UML class diagram given below, You will create a hierarchy of pets that is rooted in class Pet.
- Write the **class definitions**. [5 marks]
 - Write the **implementation of the methods** so that the following code will produce the given output. [5 marks]



Question (3): [15 marks]

- a) Show the output of the following code segments. [8 marks]

<pre> import javafx.application.Application; import javafx.scene.Scene; import javafx.scene.control.Button; import javafx.stage.Stage; public class MyJavaFX extends Application { @Override public void start(Stage primaryStage) { Button btOK = new Button("OK"); Scene scene = new Scene(btOK, </pre>	<pre> class Test { String str = "a"; void A() { try { str += "b"; B(); } catch (Exception e) </pre>
---	---

Summer Semester 2019	Course Code: CSE126	Time Allowed: 3 Hrs.
Computer Programming (2)		

The Exam Consists of **Three** Questions in **Three** Pages.

3 / 3

<pre> 200, 250); primaryStage.setTitle("MyJavaFX"); primaryStage.setScene(scene); primaryStage.show(); } public static void main(String[] args) { Application.launch(args); } </pre>	<pre> { str += "c"; } } void B() throws Exception { try { str += "d"; C(); } catch(Exception e) { throw new Exception(); } finally { str += "e"; } str += "f"; } void C() throws Exception { throw new Exception(); } void display() { System.out.println(str); } public static void main(String[] args) { Test object = new Test(); object.A(); object.display(); } } </pre>
(i)	(ii)

b) Why do we need to use the following: [4 marks]
 i. Thread pools.
 ii. Thread synchronization

c) What is the difference between event-driven programming and procedural programming? [3 marks]

END of Exam, Good Luck

Examination Committee

Dr. Maryam Al-Berry

Exam. Date : 29th of Aug., 2019



AIN SHAMS UNIVERSITY FACULTY OF ENGINEERING

International Credit Hour Programs (ICHEP)

Computer Engineering and Software Systems Program

Summer 2019

Course Code: CSE127

Time allowed: 3Hrs.

Data Structures and Algorithms

The Exam Consists of Six Questions in Three Pages.

Maximum Marks: 40 Marks

1 / 3

تعليمات هامة

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Question 1: (7 Marks)

- (a) Order these functions in order of asymptotic growth rate, with the most rapidly growing first. If two of them have the same asymptotic growth rate, state that fact.

$$\lg(n^2), 0.000001n, \lg(n), 2^{2^n}, 4^n, n\lg(n), \lg(2^n)$$

- (b) Design an algorithm that takes two arrays, and returns true if the arrays are disjoint, i.e. have no elements in common. You can use standard data structures without explaining how they are implemented. Write down your algorithm as pseudocode. Give the complexity of your algorithm.

Question 2: (7 Marks)

- (a) Draw the recursion tree to find a guess to the following recurrence:

$$T(n) = \begin{cases} 2 & \text{if } n = 2 \\ 2T(n/2) + n & \text{if } n = 2^k, \text{ for } k > 1 \end{cases}$$

Prove your guess using mathematical induction.

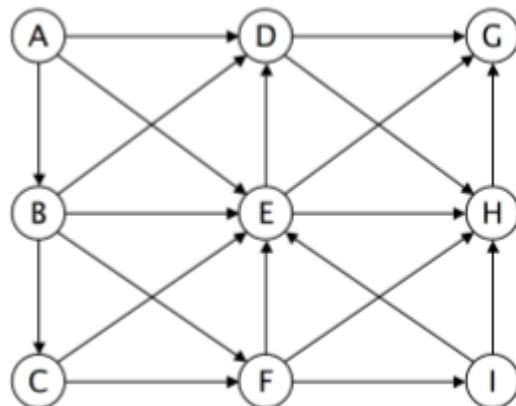
- (b) Solve the following recurrence using the master method:

$$\begin{aligned} T(n) &= 4T(n/2) + n^2\sqrt{n} \\ T(n) &= 3T(n/2) + n \lg(n) \end{aligned}$$

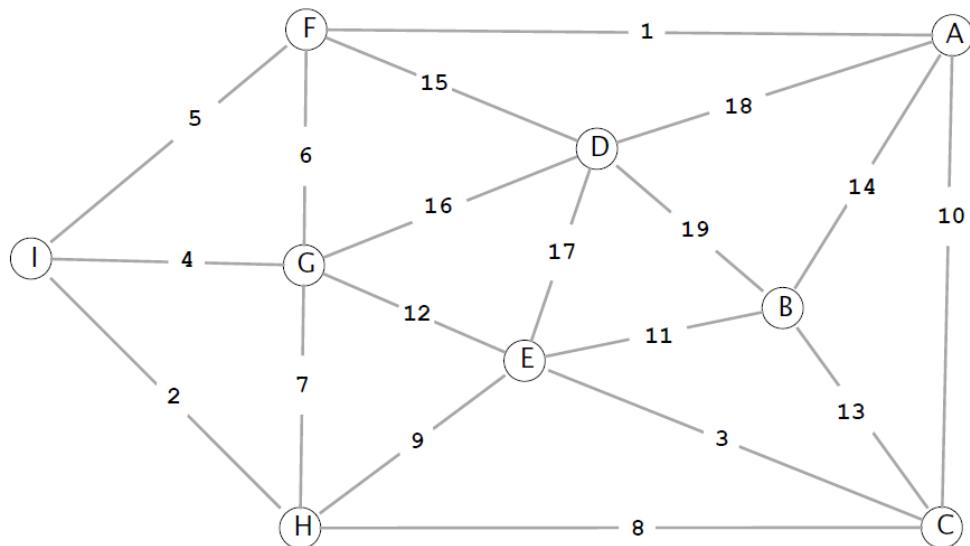
Question 3: (6 Marks)

Given the following directed graph:

- (a) Run depth-first search, starting at vertex A. Assume the adjacency lists are in lexicographic order, e.g., when exploring vertex E, consider E-D before E-G or E-H. Give the list of vertices in preorder (the order they are first discovered by DFS).
- (b) Run breadth-first search, starting at vertex A. Assume the adjacency lists are in lexicographic order. Give the list of vertices in the order in which they are enqueued.

**Question 4: (7 Marks)**

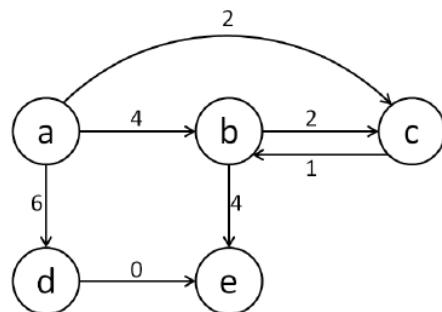
Given the following graph



- Use Kruskal's algorithm to get the sequence of edges in the MST (Minimum Spanning Tree).
- Use Prim's algorithm to get the sequence of edges in the MST (Minimum Spanning Tree).

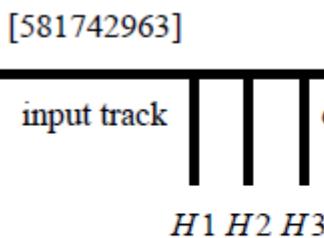
Question 5: (6 Marks)

Given the following graph, use Dijkstra's algorithm to find the shortest path from *a* to *e*. (You should show the status of all data structures maintained by the algorithm before each iteration of the main loop.)

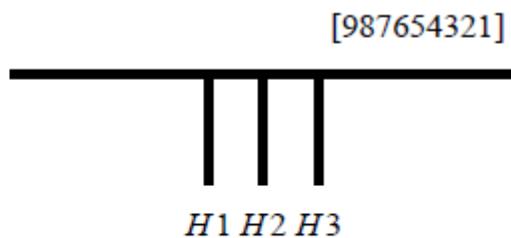
**Question 6: (7 Marks)**

A freight train has n railroad cars. Each is to be left at a different station. Assume that the n stations are numbered 1 through n and that the freight train visits these stations in the order n through 1. The railroad cars are labeled by their destination. To facilitate removal of the railroad cars from the train, we must reorder the cars so that they are in the order 1 through n from front to back. When the cars are in this order, the last car is detached at each station. We rearrange the cars at a shunting yard that has an input track, an output track, and k holding tracks between the input and output tracks. The following figure shows a shunting yard with $k = 3$ holding tracks $H1$, $H2$, and $H3$. The n cars of the freight train begin in the input track and are to end up in the output track in the order 1 through n from right to left.

In the following figure, $n = 9$; the cars are initially in the order 5, 8, 1, 7, 4, 2, 9, 6, 3 from back to front. Figure (b) shows the cars rearranged in the desired order.



(a) Initial



(b) Final

Write a program to solve this problem. Define your data structure clearly. Trace your solution by giving the status of the tracks for the given example.



AIN SHAMS UNIVERSITY

FACULTY OF ENGINEERING

International Credit Hours Engineering Programs (i-CHEP)
Computer Engineering and Software Systems (CESS) Program

Summer 2019 Semester

Course Code: CSE128

Time Allowed: 3 Hrs.

Software Engineering (1)

The Exam Consists of Four Questions in Two Pages.

Maximum Marks: 40 Marks

1 / 2

تعليمات هامة

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ANSWER ALL QUESTIONS

Question (1): [13 marks]

A software system is going to be developed for a health-care facility. The software shall be able to register doctors and patients, reserve clinical appointments for out-patients in the different medical specializations, manage the fees for the services provided by the facility, provide the medical history of the patients, register the prescription for the patients, communicate the prescription to the pharmacies from which the patient can get his medications, and transfer patient medical history to other medical facilities if needed. Additionally, it allows the patient to use his credit/debit card to pay the service fees. It shall be able to make patient transfer for the specializations that are not provided by the medical facility. It will have on-line capabilities, where patients can search for physicians and get information about their profiles. The software should be able to serve a large number of patients in addition to being reachable from mobile devices. The project will have an estimated development duration of 6 months. It shall be implemented using a reasonable programming language and shall conform to all applicable medical practices and standards.

- i. State the functional requirements of the project. **(3 marks)**
- ii. State the non-functional requirements of the project. **(2 marks)**
- iii. Sketch the source traceability matrix. **(2 marks)**
- iv. Discuss the ambiguity of the requirements stated in the project description and provide more appropriate re-phrasing (from the software engineering point of view) of all ambiguous requirements. **(2 marks)**
- v. Sketch the UML use-case diagram for this system, select one of the use-cases and write its detailed narrative description. **(4 marks)**

Question (2): [7 marks]

- a. Compare waterfall and transformation software engineering process models from the following perspectives: **(4 marks)**
 - i. Main differences between each model.
 - ii. Typical projects that can adopt each of them.
- b. Differentiate system requirements and user requirements focusing on the following aspects: **(3 marks)**
 - i. How each of them can be described?
 - ii. The contents of each of them.
 - iii. When to use each of them.

Question (3): [10 marks]

Consider a software project that is going to be developed for an automatic driving system of a shipping-train in a seaport. It uses a set of wireless sensors to detect the exact location of the train on the track, in addition to a set of other sensors that are used by the software to guide the train to the correct direction and throttle its engine to the best speed according to the track condition and the train payload. The system should provide audio-visual warning before entering the platform by 50 seconds. Audio-visual signals are also used for warning if another train comes in the other direction. Sensors on the train can detect obstacles on the track and, in this case, the software makes appropriate computations to stop the train.

- i. Sketch the state diagram for this system using UML notation. (3 marks)
- ii. Use noun extraction to find the potential classes of this system. (2 marks)
- iii. Sketch the class diagram using UML notation. Show the relationships among classes and the attributes of each class. (3 marks)
- iv. Sketch the sequence diagram using UML notation for the given scenario in the project description. (2 marks)

Question (4): [10 marks]

- a. What are CASE tools? Differentiate Upper and Lower CASE tools. (2 marks)
- b. Compare Client-Server and Data-Centered software architecture from the following perspectives:
 - i. Typical situations for using each of them.
 - ii. Advantages
 - iii. Disadvantage
(3 marks)
- c. State the human factors that affect the user interface design. Then, explain the effect of each of them on user interface design. (3 marks)
- d. Explain with the aid of examples how user interface can be evaluated. (2 marks)

Examination Committee:*Dr. Gamal A. Ebrahim and Dr. Mahmoud I. Khalil****Exam Date: Aug. 25, 2019***



AIN SHAMS UNIVERSITY

FACULTY OF ENGINEERING

International Credit Hours Engineering Programs (i-CHEP)
Computer Engineering and Software Systems (CESS) Program

Summer 2019 Semester

Course Code: CSE223

Time Allowed: 3 Hrs.

Operating Systems

The Exam Consists of Four Questions in Two Pages.

Maximum Marks: 40 Marks

1 / 2

تعليمات هامة

- حيازة التيلفون المحمول مفتوحاً داخل لجنة الامتحان يعتبر حالة غش تستوجب العقاب وإذا كان ضروري الدخول بالمحمول فيوضع مغلقاً في الحقائب.
- لا يسمح بدخول سماعة الأذن أو البليوتوث.
- لا يسمح بدخول أي كتب أو ملازم أو أوراق داخل اللجنة والمخالفه تعتبر حالة غش.

ANSWER ALL QUESTIONS

Question (1): [12 marks]

- a. Define the following terms: (5 marks)
- Double buffering
 - System call
 - Starvation
 - Page fault
 - Deadlock
- b. Mention the function of each of the following: (3 marks)
- File control block
 - Semaphores
 - Dispatcher
- c. Differentiate each pair of the following: (4 marks)
- Monolithic operating system and microkernel-based operating system
 - Medium-term scheduler and short-term scheduler
 - Internal and external fragmentation
 - Safe state and unsafe state

Question (2): [10 marks]

- a. Consider a system that has four jobs A, B, C, and D. These jobs come to the system at almost the same time with the specified order. The required processing time for each job and the job priority are given in the shown table. Job priorities are represented with numbers, where the job priority decreases as the corresponding number increases. Compute the average process turnaround time, and the average waiting time for this set of jobs in the following cases (assume no I/O is done during the execution of any of these jobs): (5 marks)

Job	Required Processing Time (in seconds)	Job Priority
A	8	1
B	12	4
C	16	2
D	4	3

- If preemptive priority scheduling algorithm is used with a quantum of 5 seconds.
- If round-robin scheduling algorithm is used with a quantum of 4 seconds.
- If shortest job first scheduling algorithm is used.

- b. Sketch the process state diagram; show all possible transitions among states. Then, list the contents that should be located in Process Control Block. **(2 marks)**
- c. Compare one-to-one and many-to-one thread models focusing on how each model is implemented, the advantages, and the disadvantages of each of them. **(3 marks)**

Question (3): [8 marks]

- a. Consider a file system that uses a modified contiguous-allocation model with support for extents. Hence, the file in this system is composed of a collection of extents, with each extent corresponding to a contiguous set of blocks. List the advantages and disadvantages of each of the following scenarios: **(3 marks)**
- All extents are of the same size, and the size is predetermined.
 - Extents can be of any size and are allocated dynamically.
- b. Assume that the free disk space can be kept track of by either using free-space list that uses counting or a bitmap. Disk address requires D bits, and each count of free blocks is inserted in a data structure of size C. For a disk with B blocks, F of them are free and no free block is contiguous to any other free blocks, state the condition under which the free-space list that uses counting utilizes less space than the bitmap. **(3 marks)**
- c. A computer with 48-bit virtual address uses a two-level page table with a page-size of 16KB. Logical addresses are split into 10-bit top-level page table field, a second-level page table field, and an offset. Sketch the logical address; show the size of each field in this address. **(2 marks)**

Question (4): [10 marks]

- a. Mention the conditions that will lead to deadlock, then discuss the impact of negating each of these conditions to prevent deadlock. **(3 marks)**
- b. Suppose we have four processes (A, B, C, and D) and seven resources ($R_1, R_2, R_3, R_4, R_5, R_6$, and R_7) the following table shows the resources held and requested by each of these processes: **(4 marks)**
- | Process | Resources Held | Resources Requested |
|---------|----------------|---------------------|
| A | R_6, R_7 | R_1, R_3 |
| B | R_1, R_4 | R_3 |
| C | R_2, R_3 | R_5, R_7 |
| D | R_5 | R_2, R_6 |
- Sketch the resource-allocation graph for this scenario.
 - Find the deadlocked processes (if any), then, identify the best process(es) that should be killed to resolve the deadlock.
- c. Assume an operating system that uses paging, it allocates 3 frames to each process, assume a new process that has been initially allocated 3 empty frames, then it generates the following page reference string 1, 6, 5, 6, 1, 3, 4, 3, 1, 2, 1, 5, 1, 0, 5, 4, 2, 3, 6, 3. Compute the optimal number of page faults, then compute the number of page faults that occur when each of the following page replacement algorithms is used: **(3 marks)**
- FIFO
 - LRU



AIN SHAMS UNIVERSITY

FACULTY OF ENGINEERING

International Credit Hours Engineering Programs (i-CHEP)
Computer Engineering and Software Systems (CESS) Program

Summer 2019 Semester

Course Code: CSE224

Time Allowed: 3 Hrs.

Design and Analysis of Algorithms

The Exam Consists of Four Questions in Two Pages.

Maximum Marks: 40 Marks

1 / 2

تعليمات هامة

- حيازة التيلفون المحمول مفتوحاً داخل لجنة الامتحان يعتبر حالة غش تستوجب العقاب وإذا كان ضروري الدخول بال محمول فيوضع مغلقاً في الحقائب.
- لا يسمح بدخول سماعة الأذن أو البليوتوث.
- لا يسمح بدخول أي كتب أو ملازم أو أوراق داخل اللجنة والمخالفه تعتبر حالة غش.

ANSWER ALL QUESTIONS

Question (1): [10 marks]

- a. Find $\Theta(n)$ for the function $f(n) = 3n^2 \log(5n)^3 + (n - 5)^2 \log\left(\frac{n}{3}\right)$. (2 mark)
- b. Compute the efficiency class of the following algorithm: (3 mark)

```

ALGORITHM Alg( $A[0..n - 1]$ )
//Input: A matrix  $A[0..n - 1, 0..n - 1]$  of real numbers
for  $i \leftarrow 0$  to  $n - 2$  do
    for  $j \leftarrow i + 1$  to  $n - 1$  do
        if  $A[i, j] \neq A[j, i]$ 
            return false
    return true

```

- c. Find the recurrence relation of the following algorithm, then solve it in terms of n : (3 mark)

```

ALGORITHM Compute( $A[0..n - 1]$ )
//Input: An array  $A[0..n - 1]$  of real numbers
if  $n = 1$  return  $A[0]$ 
else  $x \leftarrow \text{Compute}(A[0..n - 2])$ 
    if  $x \leq A[n - 1]$  return  $x$ 
    else return  $A[n - 1]$ 

```

- d. Compute the order of growth for the problem described by the following recurrence equation: (2 marks)
- $$T(n) = 20T\left(\frac{n}{4}\right) + 3n^2 \quad \text{for } n > 1, \text{ assume } T(1) = 2$$

Question (2): [10 marks]

- a. You have a row of $2n$ binary digits, n zeros and n ones. They alternate: zero, one, zero, one, and so on. You want to get all the zeros to the right-hand end, and all the ones to the left-hand end. The only moves you are allowed to make are those that interchange the positions of two neighboring digits. (4 marks)
- Design a brute-force algorithm for solving this problem, write your algorithm in pseudo-code form.
 - Determine the number of moves it takes to get all the zeros to the right-hand end, and all the ones to the left-hand end.
 - Find the big-O for the designed algorithm.

Design and Analysis of AlgorithmsThe Exam Consists of **Four Questions in Two Pages.****2 / 2**

- b. Use geometric method to compute the solution for the following linear programming problem: **(3 marks)**

$$\text{maximize } 3x + y$$

$$\text{subject to } -x + y \leq 1, \quad 2x + y \leq 4, \quad x \geq 0, \quad y \geq 0$$

- c. Assume we have a set of symbols that we need to encode them using Huffman code, assume these symbols are A, B, C, D, and the "_" symbol. Each of these symbols appears in a sample text with the following probabilities:

Symbol	A	B	C	D	-
Probability	0.1	0.15	0.25	0.3	0.2

Construct the Huffman code for these symbols, show all the steps you used to construct this code. **(3 marks)**

Question (3): [10 marks]

- a. Assume we have a knapsack problem with knapsack capacity $M = 6$ and we have 5 items with the weight and value of each item given in the shown table. Use dynamic programming to find the optimal solutions of this problem. **(4 marks)**

Item Number	1	2	3	4	5
Weight	5	4	3	2	1
Value	5	6	4	3	2

- b. Explain with the aid of examples each of the following: **(6 marks)**
- i. Tight lower bound
 - ii. Greedy algorithm
 - iii. Class P problems
 - iv. Double hashing

Question (4): [10 marks]

- a. Explain with the aid of examples the differences between NP-Problem and NP-Complete problem. Then, discuss what can be concluded if we find that $P = NP$. **(3 marks)**

- b. Explain with the aid of examples how overflow can be handled in hashing tables. **(2 marks)**

- c. Assume we have a hash table with size $b = 11$, with each bucket can hold only one key-value pair, assume also we use the hash function $H(key) = \text{key mod } 11$. Additionally, we need to insert a set of items into the hash table. These items have the following keys: 20, 15, 14, 12, 9, 31, and 42, and we need to insert them in the given order assuming linear probing is adopted for resolving collisions.

- i. Sketch the contents of the hash table after inserting these items. **(2 marks)**

- ii. Assume we need to delete the item 31 and then delete item 42, sketch the contents of the hash table after deleting each of these items. **(3 marks)**

Examination Committee:

Dr. Gamal A. Ebrahim and Dr. Mahmoud I. Khalil

Exam Date: Aug. 26, 2019



Summer Semester 2019

Course Code: CSE225

Time allowed: 3Hrs.

Software Testing, Validation, and Verification

The Exam Consists of **Four Questions** in **Two Pages**.

Maximum Marks: 40 Marks

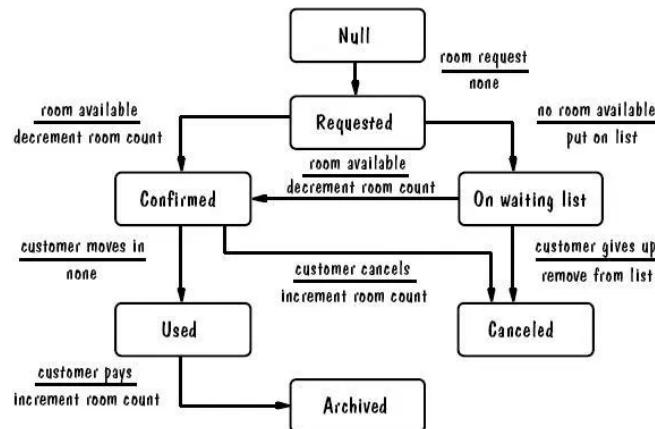
1 / 2

- تعليمات هامة**
- حيارة التيلفون المحمول مفتوحا داخل لجنة الامتحان يتوجب العقب وإذا كان ضروري الدخول بالمحظوظ فيوضع مغلق في الحقائب.
 - لا يسمح بدخول سماعة الأذن أو البلوتوث.
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Question (1): [8 marks]

Consider the following state transition diagram for a hotel reservation service:

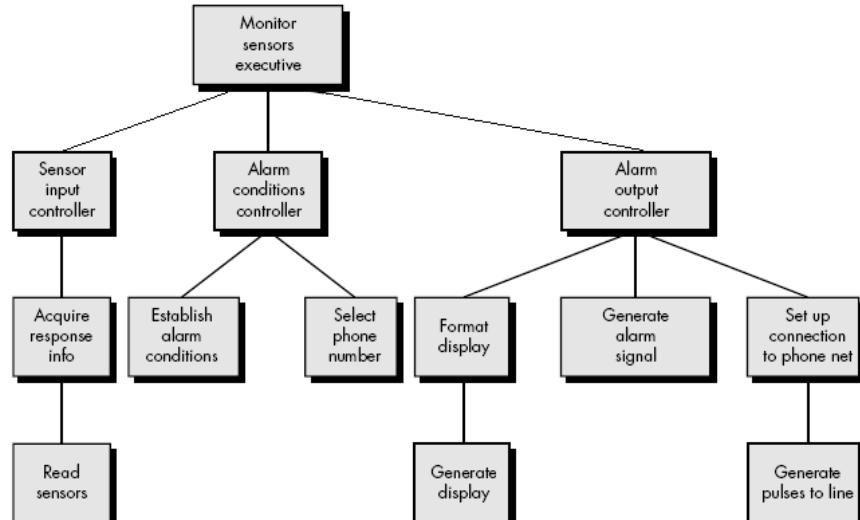
1. Generate test cases to apply all state coverage.
2. Generate the test case to apply transition-tour coverage.
3. What faults can be detected when performing FSM based testing?
4. What is the difference between transition-tour and distinguishing sequence methods?



Question (2): [8 marks]

Consider the following software skeleton for a system:

1. What testing sequence to follow to apply Bottom-up Integration Testing?
2. What testing sequence to follow to apply top-down Integration Testing?
3. If “Aquire response Info”, “Select phone number”, “Generate alarm signal” are not developed yet. Which testing approach would you recommend to minimize stubs/drivers?
4. What is the advantage of applying the Modified Sandwich approach?



Question (3): [8 marks]

Determine the most appropriate system testing technique for each of the following cases:

1. Testing a new design of ipods specially designed for jogging practitioners.
2. Testing a platform that is expected to operate on a distributed system with several backup solutions.
3. Testing the maximum number of users that an e-commerce platform can handle at the same time.
4. Your company is the system provider in a certain project, many hardware and software vendors participate in the system and you want to test that the overall solution is working fine.
5. Testing the behavior of a flight reservation system after announcing a last-minute deal.
6. Testing a new design of smart air conditioners at different contexts.
7. Your company is about to release a new software and you want to test it for the last time before public release.
8. Testing the break point of the system.

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i-CREDIT HOURS ENGINEERING PROGRAMS, COMPUTER ENGINEERING AND SW SYSTEMS PROGRAM		
Summer Semester 2019	Course Code: CSE225	Time Allowed: 3 Hrs.
Software Testing, Validation, and Verification		
The Exam Consists of Four Questions in Two Pages.		2 / 2

Question (4): [16 marks]

Please answer the following questions.

1. What is the difference between software safety failures and software security failures? Clarify the steps to apply software security testing. **[6 marks]**
2. A supermarket has a loyalty scheme that is offered to all customers. Loyalty card holders enjoy the benefits of either additional discounts on all purchases or the acquisition of loyalty points that can be converted into vouchers for the supermarket. A customer without a loyalty card can receive a discount only if he spends more than 500EGP on any one visit to the store, otherwise only the special offers offered to all customers apply.
 - a. Draw the cause-effect graph of this system. **[1 mark]**
 - b. Apply decision table testing to identify the test cases needed for this system. **[2 marks]**
3. Consider the following pseudo code to display prime numbers within an interval:

```

1 public DisplayPrimes(int low, int high) {
2     while (low < high) {
3         boolean flag = false;
4         for(int i = 2; i <= low/2; ++i) { // condition for nonprime number
5             if(low % i == 0) {
6                 flag = true;
7                 break;
8             }
9         }
10        if (!flag)
11            System.out.print(low + " ");
12        ++low;
13    }
14 }
```

- a. Draw the control flow graph of this pseudo code. **[2 marks]**
- b. How many test cases are needed to test statement coverage? Determine the different sequence of nodes to test this code statement coverage. **[2 marks]**
- c. Calculate the cyclomatic complexity of this pseudo code. **[1 mark]**
- d. Determine the different sequence of nodes to test this pseudo code path coverage. Suggest values for test cases to apply this path coverage testing. **[2 marks]**

END of Exam, Good Luck

Examination Committee
Dr. Sherin Moussa

Exam. Date : 31st of Aug, 2019



Summer 2019	Course Code: CSE 316/CSE318	Time allowed: 3Hrs.
Microcontrollers and Interfacing		
The Exam Consists of Three Questions in Two Pages.	Maximum Marks: 40 Marks	1 / 12
تعليمات هامة		
<ul style="list-style-type: none">• حيازة التليفون المحمول مفتوحا داخل لجنة الامتحان يعتبر حالة غش تستوجب العقاب وإذا كان ضروري الدخول بالمحمول فيوضع مغلق في الحقائب.• يسمح بدخول الـ حاسـيـه عـادـيه - غـير مـبرـمـجه• لا يـسمـح بـدخـول سـمـاعـه الأـذـن أو الـلـوـبـوتـوـث• لا يـسمـح بـدخـول أي كـتـب أو مـلـازـم أو أورـاق دـاـخـل اللـجـنـه وـالـمـخـالـفـه تـعـتـبـر حـلـة غـشـ.		

Question (1): [5 marks]

For each of the following multiple choice questions, circle the ONE best answer. Unless otherwise stated, assume that all statements are in the context of the AVR architecture.

1. How many times is this loop going to get executed?

LDI R20, 10
now: LDI R21, 70
DEC R21
BRNE now
OUT PORTB, R20

- a) 10
- b) 70
- c) 700
- d) none of the mentioned

2. Which of the following is correct about BRNE instruction in AVR microcontrollers?

- a) it is used to compare two registers
- b) it is used to compare two values
- c) it is used to check the zero flag
- d) it is used to jump to the given mentioned label when the zero flag accounts to 1

3. In AVR, which registers are there for the I/O programming of ports?

- a) PORT
- b) PIN
- c) DDR
- d) All of the mentioned

4. Which of the following statements are correct?

- a) PIN register of a port is used to bring data into CPU from pins
- b) PORT register is used to send data out to pins
- c) DDR register is used to control the direction of a port
- d) All of the mentioned

5. Which of the following is not a single bit instruction in AVR?

- a) SBI
- b) PORT
- c) CBI
- d) All of the mentioned

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Credit Hours Engineering Programs
Computer Engineering and Software Systems

Summer 2019	Course Code: CSE 316/CSE318	Time allowed: 3Hrs.
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Microcontrollers and Interfacing

The Exam Consists of **Five** Questions in **Twelve** ages.

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6. Which of the timer can operate in the 16 bit condition?

- a) timer0
- b) timer1
- c) timer2
- d) all of the mentioned

7. TIMSK register is used for?

- a) knowing the status of the timer count
- b) used for masking the interrupts flags of the Timer0, Timer1 and Timer2
- c) it is used for enabling all the timer interrupts
- d) it is used for resetting the value of the interrupts

8. What will happen in that condition, if an interrupt occurs while the microcontroller is serving any other interrupt?

- a) both the interrupts will be handled simultaneously
- b) the interrupt which is being done first will be served first
- c) the interrupt that is more priority in the interrupt vector table will be served first
- d) the interrupt having low priority in the interrupt vector table will be served first

9. With fosc=8 MHz, what will the count that has to filled in the UBRR register to account for the 9600 baud rate?

- a) 67H
- b) CEH
- c) 33H
- d) 34H

10. Which of the following parameters should the transmitter and the receiver agree upon before starting a serial transmission?

- a) baud rate
- b) frame size
- c) stop bit
- d) all of the mentioned

Question 2 [5 Marks]

Mark each of the following statements as true or false. Unless otherwise stated, assume that all statements are in the context of the AVR architecture.

N	Statement
1	The overflow flag is used in the case of signed numbers to indicate an overflow of bits.
2	The MOV instruction can be used to copy data between GPR registers
3	The instruction BST Rd, b copies the T Flag in the SREG (Status Register) to bit b in register Rd, whereas BLD Rd, b stores bit b from Rd to the T Flag in SREG (Status Register).
4	If two systems are communicating serially in full-duplex. This implies that there are two different wires connecting the two systems.
5	It is common to initialize the stack pointer to the highest (upper most) memory location indicated by (RAMEND).

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Computer Engineering and Software Systems

Summer 2019

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Microcontrollers and Interfacing

The Exam Consists of **Five** Questions in **Twelve** ages.

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Question 2 (cont.)

6	It is common to save the Status Register SREG directly onto the stack.
7	The following instruction can be used as a bitwise shift operation to generate a number with only 1 in position D7 $1 \ll 7$
8	EEPROM cannot be used to save variables that should not change after power shutdown, such as the temperature of a cooling system.
9	When writing to EEPROM, it is possible to start read or write operations before the last write operation is finished.
10	There are two separate flags for each of Timer1 OCR registers, which act independently of each other.

Question 3 [10 Marks]

- (a) Write an assembly program to toggle all the bits of PORTB and PORTC continuously using the COM instruction. [5 Marks]

(b) Write an assembly program to monitor the PB5 and PB6 bits continuously. When both of them are HIGH, send \$AA to PORTC; otherwise, send \$55 to PORTC. [5 Marks]

Question 4 [10 Marks]

- (a) Assume that XTAL = 8 MHz. Find the TCNT0 value needed and write a C program to generate a time delay of 20 μ s. Use normal mode and no prescaler mode. [5 Marks]

(b) Write an AVR C program that continuously reads the analog signal value applied on Channel 2 (PC2) using polling and write the value to Port B and D. After every conversion, send a high-to-low pulse on PC0 and wait for 50 ms. The value of the input signal is in the range of 0 to 5V. [5 Marks]

Question 5 [10 Marks]:

- (a) Assume that the INT0 pin is connected to a switch that is normally high. Write a C program that toggles PORTB.0, whenever INTO pin goes low. Use the external interrupt in falling-edge trigger mode. [4 Marks]
 - (b) Write a C program to receive bytes of data serially and output them on Port B. Use Receive Complete Interrupt instead of polling. [3 Marks]
 - (c) Write an AVR C program to read the content of location 0x005F of EEPROM and write it to PORTB. [3 Marks]

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Credit Hours Engineering Programs
Computer Engineering and Software Systems

Summer 2019

Course Code: CSE 316/CSE318

Time allowed: 3Hrs.

Microcontrollers and Interfacing

The Exam Consists of **Five** Questions in **Twelve** ages.

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Appendix A: AVR Instruction Set

Mnemonics	Operands	Description	Operation	Flags	#Clocks
Arithmetic and Logic Instructions					
ADD	Rd, Rr	Add without Carry	$Rd \leftarrow Rd + Rr$	Z,C,N,V,S,H	1
ADC	Rd, Rr	Add with Carry	$Rd \leftarrow Rd + Rr + C$	Z,C,N,V,S,H	1
ADIW	Rd, K	Add Immediate to Word	$Rd \leftarrow Rd + 1:Rd + K$	Z,C,N,V,S	2
SUB	Rd, Rr	Subtract without Carry	$Rd \leftarrow Rd - Rr$	Z,C,N,V,S,H	1
SUBI	Rd, K	Subtract Immediate	$Rd \leftarrow Rd - K$	Z,C,N,V,S,H	1
SBC	Rd, Rr	Subtract with Carry	$Rd \leftarrow Rd - Rr - C$	Z,C,N,V,S,H	1
SBCI	Rd, K	Subtract Immediate with Carry	$Rd \leftarrow Rd - K - C$	Z,C,N,V,S,H	1
SBIW	Rd, K	Subtract Immediate from Word	$Rd + 1:Rd \leftarrow Rd + 1:Rd - K$	Z,C,N,V,S	2
AND	Rd, Rr	Logical AND	$Rd \leftarrow Rd \cdot Rr$	Z,N,V,S	1
ANDI	Rd, K	Logical AND with Immediate	$Rd \leftarrow Rd \cdot K$	Z,N,V,S	1
OR	Rd, Rr	Logical OR	$Rd \leftarrow Rd \vee Rr$	Z,N,V,S	1
ORI	Rd, K	Logical OR with Immediate	$Rd \leftarrow Rd \vee K$	Z,N,V,S	1
EOR	Rd, Rr	Exclusive OR	$Rd \leftarrow Rd \oplus Rr$	Z,N,V,S	1
COM	Rd	One's Complement	$Rd \leftarrow \$FF - Rd$	Z,C,N,V,S	1
NEG	Rd	Two's Complement	$Rd \leftarrow \$00 - Rd$	Z,C,N,V,S,H	1
SBR	Rd,K	Set Bit(s) in Register	$Rd \leftarrow Rd \vee K$	Z,N,V,S	1
CBR	Rd,K	Clear Bit(s) in Register	$Rd \leftarrow Rd \cdot (\$FFh - K)$	Z,N,V,S	1
INC	Rd	Increment	$Rd \leftarrow Rd + 1$	Z,N,V,S	1
DEC	Rd	Decrement	$Rd \leftarrow Rd - 1$	Z,N,V,S	1
TST	Rd	Test for Zero or Minus	$Rd \leftarrow Rd \cdot Rd$	Z,N,V,S	1
CLR	Rd	Clear Register	$Rd \leftarrow Rd \oplus Rd$	Z,N,V,S	1
SER	Rd	Set Register	$Rd \leftarrow \$FF$	None	1
MUL	Rd,Rr	Multiply Unsigned	$R1:R0 \leftarrow Rd \times Rr \text{ (UU)}$	Z,C	2
MULS	Rd,Rr	Multiply Signed	$R1:R0 \leftarrow Rd \times Rr \text{ (SS)}$	Z,C	2
MULSU	Rd,Rr	Multiply Signed with Unsigned	$R1:R0 \leftarrow Rd \times Rr \text{ (SU)}$	Z,C	2
FMUL	Rd,Rr	Fractional Multiply Unsigned	$R1:R0 \leftarrow Rd \times Rr \ll 1 \text{ (UU)}$	Z,C	2
FMULS	Rd,Rr	Fractional Multiply Signed	$R1:R0 \leftarrow Rd \times Rr \ll 1 \text{ (SS)}$	Z,C	2
FMULSU	Rd,Rr	Fractional Multiply Signed with Unsigned	$R1:R0 \leftarrow Rd \times Rr \ll 1 \text{ (SU)}$	Z,C	2
Branch Instructions					
RJMP	k	Relative Jump	$PC \leftarrow PC + k + 1$	None	2
IJMP		Indirect Jump to (Z)	$PC(15:0) \leftarrow Z,$ $PC(21:16) \leftarrow 0$	None	2
EIJMP		Extended Indirect Jump to (Z)	$PC(15:0) \leftarrow Z,$ $PC(21:16) \leftarrow EIND$	None	2
JMP	k	Jump	$PC \leftarrow k$	None	3
RCALL	k	Relative Call Subroutine	$PC \leftarrow PC + k + 1$	None	3/4

AIN SHAMS UNIVERSITY, FACULTY OF ENGINEERING
Credit Hours Engineering Programs
Computer Engineering and Software Systems

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Course Code: CSE 316/CSE318

Time allowed: 3Hrs.

Microcontrollers and Interfacing

The Exam Consists of **Five** Questions in **Twelve** ages.

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ICALL		Indirect Call to (Z)	PC(15:0) ← Z, PC(21:16) ← 0	None	3/4
EICALL		Extended Indirect Call to (Z)	PC(15:0) ← Z, PC(21:16) ← EIND	None	4
CALL	k	call Subroutine	PC ← k	None	4/5
RET		Subroutine Return	PC ← STACK	None	4/5
RETI		Interrupt Return	PC ← STACK	I	4/5
CPSE	Rd,Rr	Compare, Skip if Equal	if (Rd = Rr) PC ← PC + 2 or 3	None	1/2/3
CP	Rd,Rr	Compare	Rd - Rr	Z,C,N,V,S,H	1
CPC	Rd,Rr	Compare with Carry	Rd - Rr - C	Z,C,N,V,S,H	1
CPI	Rd,K	Compare with Immediate	Rd - K	Z,C,N,V,S,H	1
SBRC	Rr, b	Skip if Bit in Register Cleared	if (Rr(b) = 0) PC ← PC + 2 or 3	None	1/2/3
SBRS	Rr, b	Skip if Bit in Register Set	if (Rr(b) = 1) PC ← PC + 2 or 3	None	1/2/3
SBIC	A, b	Skip if Bit in I/O Register Cleared	if (I/O(A,b) = 0) PC ← PC + 2 or 3	None	1/2/3
SBIS	A, b	Skip if Bit in I/O Register Set	If (I/O(A,b) = 1) PC ← PC + 2 or 3	None	1/2/3
BRBS	s, k	Branch if Status Flag Set	if (SREG(s) = 1) then PC ← PC + k + 1	None	1/2
BRBC	s, k	Branch if Status Flag Cleared	if (SREG(s) = 0) then PC ← PC + k + 1	None	1/2
BREQ	k	Branch if Equal	if (Z = 1) then PC ← PC + k + 1	None	1/2
BRNE	k	Branch if Not Equal	if (Z = 0) then PC ← PC + k + 1	None	1/2
BRCS	k	Branch if Carry Set	if (C = 1) then PC ← PC + k + 1	None	1/2
BRCC	k	Branch if Carry Cleared	if (C = 0) then PC ← PC + k + 1	None	1/2
BRSH	k	Branch if Same or Higher	if (C = 0) then PC ← PC + k + 1	None	1/2
BRLO	k	Branch if Lower	if (C = 1) then PC ← PC + k + 1	None	1/2
BRMI	k	Branch if Minus	if (N = 1) then PC ← PC + k + 1	None	1/2
BRPL	k	Branch if Plus	if (N = 0) then PC ← PC + k + 1	None	1/2
BRGE	k	Branch if Greater or Equal, Signed	if (N ⊕ V = 0) then PC ← PC + k + 1	None	1/2
BRLT	k	Branch if Less Than, Signed	if (N ⊕ V = 1) then PC ← PC + k + 1	None	1/2
BRHS	k	Branch if Half Carry Flag Set	if (H = 1) then PC ← PC + k + 1	None	1/2
BRHC	k	Branch if Half Carry Flag Cleared	if (H = 0) then PC ← PC + k + 1	None	1/2
BRTS	k	Branch if T Flag Set	if (T = 1) then PC ← PC + k + 1	None	1/2
BRTC	k	Branch if T Flag Cleared	if (T = 0) then PC ← PC + k + 1	None	1/2
BRVS	k	Branch if Overflow Flag is Set	if (V = 1) then PC ← PC + k + 1	None	1/2
BRVC	k	Branch if Overflow Flag is Cleared	if (V = 0) then PC ← PC + k + 1	None	1/2
BRIE	k	Branch if Interrupt Enabled	if (I = 1) then PC ← PC + k + 1	None	1/2
BRID	k	Branch if Interrupt Disabled	if (I = 0) then PC ← PC + k + 1	None	1/2

Data Transfer Instructions

MOV	Rd, Rr	Copy Register	Rd ← Rr	None	1
MOVW	Rd, Rr	Copy Register Pair	Rd+1:Rd ← Rr+1:Rr	None	1
LDI	Rd, K	Load Immediate	Rd ← K	None	1

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LDS	Rd, k	Load Direct from data space	$Rd \leftarrow (k)$	None	2
LD	Rd, X	Load Indirect	$Rd \leftarrow (X)$	None	2
LD	Rd, X+	Load Indirect and Post-Increment	$Rd \leftarrow (X),$ $X \leftarrow X + 1$	None	2
LD	Rd, -X	Load Indirect and Pre-Decrement	$X \leftarrow X - 1,$ $Rd \leftarrow (X)$	None	2
LD	Rd, Y	Load Indirect	$Rd \leftarrow (Y)$	None	2
LD	Rd, Y+	Load Indirect and Post-Increment	$Rd \leftarrow (Y),$ $Y \leftarrow Y + 1$	None	2
LD	Rd, -Y	Load Indirect and Pre-Decrement	$Y \leftarrow Y - 1,$ $Rd \leftarrow (Y)$	None	2
LDD	Rd, Y+q	Load Indirect with Displacement	$Rd \leftarrow (Y + q)$	None	2
LD	Rd, Z	Load Indirect	$Rd \leftarrow (Z)$	None	2
LD	Rd, Z+	Load Indirect and Post-Increment	$Rd \leftarrow (Z),$ $Z \leftarrow Z + 1$	None	2
LD	Rd, -Z	Load Indirect and Pre-Decrement	$Z \leftarrow Z - 1,$ $Rd \leftarrow (Z)$	None	2
LDD	Rd, Z+q	Load Indirect with Displacement	$Rd \leftarrow (Z + q)$	None	2
STS	k, Rr	Store Direct to Data Space	$(k) \leftarrow Rd$	None	2
ST	X, Rr	Store Indirect	$(X) \leftarrow Rr$	None	2
ST	X+, Rr	Store Indirect and Post-Increment	$(X) \leftarrow Rr,$ $X \leftarrow X + 1$	None	2
ST	-X, Rr	Store Indirect and Pre-Decrement	$X \leftarrow X - 1$	None	2
			$(X) \leftarrow Rr$		
ST	Y, Rr	Store Indirect	$(Y) \leftarrow Rr$	None	2
ST	Y+, Rr	Store Indirect and Post-Increment	$(Y) \leftarrow Rr,$ $Y \leftarrow Y + 1$	None	2
ST	-Y, Rr	Store Indirect and Pre-Decrement	$Y \leftarrow Y - 1,$ $(Y) \leftarrow Rr$	None	2
STD	Y+q, Rr	Store Indirect with Displacement	$(Y + q) \leftarrow Rr$	None	2
ST	Z, Rr	Store Indirect	$(Z) \leftarrow Rr$	None	2
ST	Z+, Rr	Store Indirect and Post-Increment	$(Z) \leftarrow Rr,$ $Z \leftarrow Z + 1$	None	2
ST	-Z, Rr	Store Indirect and Pre-Decrement	$Z \leftarrow Z - 1,$ $(Z) \leftarrow Rr$	None	2
STD	Z+q, Rr	Store Indirect with Displacement	$(Z + q) \leftarrow Rr$	None	2
LPM		Load Program Memory	$RO \leftarrow (Z)$	None	3
LPM	Rd, Z	Load Program Memory	$Rd \leftarrow (Z)$	None	3
LPM	Rd, Z+	Load Program Memory and Post-Increment	$Rd \leftarrow (Z),$ $Z \leftarrow Z + 1$	None	3
ELPM		Extended Load Program Memory	$RO \leftarrow (RAMPZ:Z)$	None	3

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ELPM	Rd, Z	Extended Load Program Memory	$Rd \leftarrow (RAMPZ:Z)$	None	3
ELPM	Rd, Z+	Extended Load Program Memory and Post-Increment	$Rd \leftarrow (RAMPZ:Z), Z \leftarrow Z+1$	None	3
SPM		Store Program Memory	$(RAMPZ:Z) \leftarrow R1:R0$	None	-
SPM	Z+	Store Program Memory and Post-Increment by 2	$(RAMPZ:Z) \leftarrow R1:R0, Z \leftarrow Z + 2$	None	-
IN	Rd, A	In From I/O Location	$Rd \leftarrow I/O(A)$	None	1
OUT	A, Rr	Out To I/O Location	$I/O(A) \leftarrow Rr$	None	1
PUSH	Rr	Push Register on Stack	STACK $\leftarrow Rr$	None	2
POP	Rd	Pop Register from Stack	$Rd \leftarrow \text{STACK}$	None	2
XCH	Z, Rd	Exchange	$(Z) \leftarrow Rd, Rd \leftarrow (Z)$	None	1
LAS	Z, Rd	Load and Set	$(Z) \leftarrow Rd \vee (Z), Rd \leftarrow (Z)$	None	1
LAC	Z, Rd	Load and Clear	$(Z) \leftarrow (\$FF - Rd).(Z), Rd \leftarrow (Z)$	None	1
LAT	Z, Rd	Load and Toggle	$(Z) \leftarrow Rd \oplus (Z), Rd \leftarrow (Z)$	None	1

Bit and Bit-test Instructions

LSL	Rd	Logical Shift Left	$Rd(n+1) \leftarrow Rd(n), Rd(0) \leftarrow 0$	Z,C,N,V,H	1
LSR	Rd	Logical Shift Right	$Rd(n) \leftarrow Rd(n+1), Rd(7) \leftarrow 0$	Z,C,N,V	1
ROL	Rd	Rotate Left Through Carry	$Rd(0) \leftarrow C, Rd(n+1) \leftarrow Rd(n), C \leftarrow Rd(7)$	Z,C,N,V,H	1
ROR	Rd	Rotate Right Through Carry	$Rd(7) \leftarrow C, Rd(n) \leftarrow Rd(n+1), C \leftarrow Rd(0)$	Z,C,N,V	1
ASR	Rd	Arithmetic Shift Right	$Rd(n) \leftarrow Rd(n+1), n=0..6$	Z,C,N,V	1
SWAP	Rd	Swap Nibbles	$Rd(3..0) \leftrightarrow Rd(7..4)$	None	1
BSET	s	Flag Set	$SREG(s) \leftarrow 1$	SREG(s)	1
BCLR	s	Flag Clear	$SREG(s) \leftarrow 0$	SREG(s)	1
SBI	A, b	Set Bit in I/O Register	$I/O(A, b) \leftarrow 1$	None	2
CBI	A, b	Clear Bit in I/O Register	$I/O(A, b) \leftarrow 0$	None	2
BST	Rr, b	Bit Store from Register to T	$T \leftarrow Rr(b)$	T	1
BLD	Rd, b	Bit load from T to Register	$Rd(b) \leftarrow T$	None	1
SEC		Set Carry	$C \leftarrow 1$	C	1
CLC		Clear Carry	$C \leftarrow 0$	C	1
SEN		Set Negative Flag	$N \leftarrow 1$	N	1
CLN		Clear Negative Flag	$N \leftarrow 0$	N	1
SEZ		Set Zero Flag	$Z \leftarrow 1$	Z	1
CLZ		Clear Zero Flag	$Z \leftarrow 0$	Z	1
SEI		Global Interrupt Enable	$I \leftarrow 1$	I	1

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CLI		Global Interrupt Disable	$I \leftarrow 0$	I	1
SES		Set Signed Test Flag	$S \leftarrow 1$	S	1
CLS		Clear Signed Test Flag	$S \leftarrow 0$	S	1
SEV		Set Two's Complement Overflow	$V \leftarrow 1$	V	1
CLV		Clear Two's Complement Overflow	$V \leftarrow 0$	V	1
SET		Set T in SREG	$T \leftarrow 1$	T	1
CLT		Clear T in SREG	$T \leftarrow 0$	T	1
SEH		Set Half Carry Flag in SREG	$H \leftarrow 1$	H	1
CLH		Clear Half Carry Flag in SREG	$H \leftarrow 0$	H	1
Control Instructions					
BREAK		Break		None	1
NOP		No Operation		None	1
SLEEP		Sleep		None	1
WDR		Watchdog Reset		None	1

Appendix B: EEPROM Registers

EECR	-	-	EEP1	EEP0	EERIE	EEMPE	EEPE	EERE
Bit	7	6	5	4	3	2	1	0
EEPM1	EEP1	Programming Time	Operation					
0	0	3.4ms	Erase and Write in one operation (Atomic Operation)					
0	1	1.8ms	Erase Only					
1	0	1.8ms	Write Only					
1	1	-	Reserved for future use					
EEARH	-	-	-	-	-	-	EEAR9	EEAR8
EEARL	EEAR7	EEAR6	EEAR5	EEAR4	EEAR3	EEAR2	EEAR1	EEAR0
Bit	7	6	5	4	3	2	1	0

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Appendix C: Timer registers

7	6	5	4	3	2	1	0	
COM0A1	COM0A0	COM0B1	COM0B0	-	-	WGM01	WGM00	TCCR0A
7	6	5	4	3	2	1	0	
FOC0A	FOC0B	-	-	WGM02	CS02	CS01	CS00	TCCR0B
-	-	-	-	-	OCF0B	OCF0A	TOV0	TIFR0

CS02	CS01	CS00	Description	Mode	WGM02	WGM01	WGM00	Timer/Counter Mode of Operation
0	0	0	No clock source (Timer/Counter stopped)	0	0	0	0	Normal
0	0	1	clk _{IO} /(No prescaling)	1	0	0	1	PWM, Phase Correct
0	1	0	clk _{IO} /8 (From prescaler)	2	0	1	0	CTC
0	1	1	clk _{IO} /64 (From prescaler)	3	0	1	1	Fast PWM
1	0	0	clk _{IO} /256 (From prescaler)	4	1	0	0	Reserved
1	0	1	clk _{IO} /1024 (From prescaler)	5	1	0	1	PWM, Phase Correct
1	1	0	External clock source on T0 pin, Clock on falling edge.	6	1	1	0	Reserved
1	1	1	External clock source on T0 pin, Clock on rising edge.	7	1	1	1	Fast PWM

Appendix D: Interrupts

Vector No	Program Address	Source	Interrupt Definition	Arduino/C++ ISR() Macro Vector Name
1	0x0000	RESET	Reset	
2	0x0002	INT0	External Interrupt Request 0 (pin D2)	(INT0_vect)
3	0x0004	INT1	External Interrupt Request 1 (pin D3)	(INT1_vect)
4	0x0006	PCINT0	Pin Change Interrupt Request 0 (pins B0 to B7)	(PCINT0_vect)
5	0x0008	PCINT1	Pin Change Interrupt Request 1 (pins C0 to C6)	(PCINT1_vect)
6	0x000A	PCINT2	Pin Change Interrupt Request 2 (pins D0 to D7)	(PCINT2_vect)
7	0x000C	WDT	Watchdog Time-out Interrupt	(WDT_vect)
8	0x000E	TIMER2 COMPA	Timer/Counter2 Compare Match A	(TIMER2_COMPA_vect)
9	0x0010	TIMER2 COMPB	Timer/Counter2 Compare Match B	(TIMER2_COMPB_vect)
10	0x0012	TIMER2 OVF	Timer/Counter2 Overflow	(TIMER2_OVF_vect)
11	0x0014	TIMER1 CAPT	Timer/Counter1 Capture Event	(TIMER1_CAPT_vect)
12	0x0016	TIMER1 COMPA	Timer/Counter1 Compare Match A	(TIMER1_COMPA_vect)
13	0x0018	TIMER1 COMPB	Timer/Counter1 Compare Match B	(TIMER1_COMPB_vect)
14	0x001A	TIMER1 OVF	Timer/Counter1 Overflow	(TIMER1_OVF_vect)
15	0x001C	TIMERO COMPA	Timer/Counter0 Compare Match A	(TIMERO_COMPA_vect)
16	0x001E	TIMERO COMPB	Timer/Counter0 Compare Match B	(TIMERO_COMPB_vect)
17	0x0020	TIMERO OVF	Timer/Counter0 Overflow	(TIMERO_OVF_vect)
18	0x0022	SPI, STC	SPI Serial Transfer Complete	(SPI_STC_vect)
19	0x0024	USART, RX	USART Rx Complete	(USART_RX_vect)
20	0x0026	USART, UDRE	USART, Data Register Empty	(USART_UDRE_vect)
21	0x0028	USART, TX	USART, Tx Complete	(USART_TX_vect)
22	0x002A	ADC	ADC Conversion Complete	(ADC_vect)
23	0x002C	EE READY	EEPROM Ready	(EE_READY_vect)
24	0x002E	ANALOG COMP	Analog Comparator	(ANALOG_COMP_vect)
25	0x0030	TWI	2-wire Serial Interface (I2C)	(TWI_vect)
26	0x0032	SPM READY	Store Program Memory Ready	(SPM_READY_vect)

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-	-	-	-	-	OCIE0B	OCIE0A	TOIE0	TIMSK0
-	-	ICIE1	-	-	OCIE1B	OCIE1A	TOIE1	TIMSK1
-	-	-	-	-	OCIE2B	OCIE2A	TOIE2	TIMSK2
-	-	-	-	-	-	INT1	INT0	EIMSK
-	-	-	-	-	-	INTF1	INTF0	EIFR
-	-	-	-	ISC11	ISC10	ISC01	ISC00	EICRA

ISCn1	ISCn0		Description
0	0		The low level of INT0 generates an interrupt request.
0	1		Any logical change on INT0 generates an interrupt request.
1	0		The falling edge of INT0 generates an interrupt request.
1	1		The rising edge of INT0 generates an interrupt request.

The number n can be 0 or 1

-	-	-	-	-	PCIE2	PCIE1	PCIE0	PCICR
PCINT23	PCINT22	PCINT21	PCINT20	PCINT19	PCINT18	PCINT17	PCINT16	PCMSK2
-	PCINT14	PCINT13	PCINT12	PCINT11	PCINT10	PCINT9	PCINT8	PCMSK1
PCINT7	PCINT6	PCINT5	PCINT4	PCINT3	PCINT2	PCINT1	PCINT0	PCMSK0

Appendix E: ADC

7	6	5	4	3	2	1	0	
REFS1	REFS0	ADLAR	-	MUX3	MUX2	MUX1	MUX0	
REFS1	REFS0	V_{ref}						
0	0	AREF pin		Set externally				
0	1	AVCC pin		Same as VCC				
1	0	Reserved		----				
1	1	Internal 1.1 V		Fixed regardless of VCC value				

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MUX[3:0]	Input
0000	ADC0
0001	ADC1
0010	ADC2
0011	ADC3
0100	ADC4
0101	ADC5
0110	ADC6 (not used in ATmega328p)
0111	ADC7 (not used in ATmega328p)
1000	ADC8 (internal Temperature Sensor)

(PCINT14/RESET) PC6	1	PC5 (ADC5/SCL/PCINT13)
(PCINT16/RXD) PD0	2	PC4 (ADC4/SDA/PCINT12)
(PCINT17/TXD) PD1	3	PC3 (ADC3/PCINT11)
(PCINT18/INT0) PD2	4	PC2 (ADC2/PCINT10)
(PCINT19/OC2B/INT1) PD3	5	PC1 (ADC1/PCINT9)
(PCINT20/XCK/T0) PD4	6	PC0 (ADC0/PCINT8)
VCC	7	GND
GND	8	AREF
(PCINT8/XTAL1/TOSC1) PB6	9	AVCC
(PCINT7/XTAL2/TOSC2) PB7	10	PB5 (SCK/PCINT5)
(PCINT21/OC0B/T1) PD5	11	PB4 (MISO/PCINT4)
(PCINT22/OC0A/AIN0) PD6	12	PB3 (MOSI/OC2A/PCINT3)
(PCINT23/AIN1) PD7	13	PB2 (SS/OC1B/PCINT2)
(PCINT0/CLK0/ICP1) PB0	14	PB1 (OC1A/PCINT1)

7	6	5	4	3	2	1	0
ADEN	ADSC	ADATE	ADIF	ADIE	ADPS2	ADPS1	ADPS0

ADPS2	ADPS1	ADPS0	ADC Clock
0	0	0	CK/2
0	0	1	CK/2
0	1	0	CK/4
0	1	1	CK/8
1	0	0	CK/16
1	0	1	CK/32
1	1	0	CK/64
1	1	1	CK/128

Appendix F: PWM

Compare Output Mode, Fast PWM Mode

COM0A1	COM0A0	Description
0	0	Normal port operation, OC0A disconnected.
0	1	Normal Port Operation, OC0A Disconnected.
1	0	Clear OC0A on Compare Match, set OC0A at BOTTOM, (non-inverting mode).
1	1	Set OC0A on Compare Match, clear OC0A at BOTTOM, (inverting mode).

Compare Output Mode, Phase Correct PWM Mode

COM0A1	COM0A0	Description
0	0	Normal port operation, OC0A disconnected.
0	1	Normal Port Operation, OC0A Disconnected.
1	0	Clear OC0A on Compare Match when up-counting. Set OC0A on Compare Match when down-counting.
1	1	Set OC0A on Compare Match when up-counting. Clear OC0A on Compare Match when down-counting.

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Appendix G: Serial Programming

Bit No.	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	RXCIE0	TXCIE0	UDRIE0	RXEN0	TXEN0	UCSZ02	RXB80	TXB80
Value	0	0	0	1	1	0	0	0

Bit No.	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	UMSEL01	UMSEL00	UPM01	UPM00	USBS0	UCSZ01	UCSZ00	UCPOL0
Value	0	0	0	0	0	1	1	0

UCSZn2	UCSZn1	UCSZn0	Character Size
0	0	0	5-bit
0	0	1	6-bit
0	1	0	7-bit
0	1	1	8-bit
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	9-bit

END of Exam, Good Luck

Examination Committee

Exam. Date : 28th of August., 2019

Dr. Haytham Azmi

AIN SHAMS UNIVERSITY
FACULTY OF ENGINEERING
i-CREDIT HOURS ENGINEERING PROGRAMS
COMPUTER ENGINEERING AND SOFTWARE SYSTEMS PROGRAM



Summer Semester 2019 Course Code: CSE325 Time allowed: 3Hrs.

Agile Software Engineering

The Exam Consists of **Three** Questions in **Two** Pages.

Maximum Marks: 40 Marks

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تعليمات هامة

- حيازة التليفون المحمول مفتوحا داخل لجنة الامتحان يعتبر حالة غش تستوجب العقاب وإذا كان ضروري الدخول بالمحمول فيوضع مغلق في الحقائب.
- لا يسمح بدخول سماعة الأذن أو البلوتوث.
- لا يسمح بدخول أي كتب أو ملائم أو أوراق داخل اللجنة والمخالفة تعتبر حالة غش.

Question (1): [5 marks]

Please select **ONE** choice that best fits the statement and **JUSTIFY YOUR CHOICE**.

1. What should a Development Team do during a Sprint Planning meeting when they have realized that they have selected more than the items they can complete in a Sprint?

a) Seek help from the other Scrum Team Members.	c) Work overtime.
b) Get more developers onboard.	d) Inform the Product Owner.
2. What is done during a Sprint Review Meeting?

a) Discuss improvements for upcoming sprints.	c) Demo of the Increment.
b) Inspect progress towards Sprint Goal.	d) Discuss technical aspects of the project.
3. What happens when all the Sprint Items cannot be completed?

a) The Sprint should be extended.	c) Unfinished items are removed from Sprint Backlog.
b) The Sprint ends with the done items.	d) Start next Sprint with unfinished items first.
4. Which of the following activity is not timeboxed?

a) Sprint Retrospective.	c) Daily Scrum.
b) Product Backlog Grooming.	d) Sprint Review.
5. When can a Sprint be canceled?

a) Whenever the Product Owner says.	c) Data required to start development is not available.
b) The Sprint items are no longer needed.	d) When Development is unable to complete work.

Question (2): [10 marks]

Please compare between the following terminologies.

- | | |
|--|-----------|
| a) Burn-up and Burn-down charts. | [2 marks] |
| b) Product backlog, Sprint Backlog and Insights Backlog. | [3 marks] |
| c) Epic, User stories and Tasks. | [3 marks] |
| d) Task board and Insight Card Wall | [2 marks] |

Question (3): [25 marks]

Please answer the following questions.

- a) Discuss the sprint retrospective activity, clarifying its goal, participants, prework activities, inputs, outputs and process. [5 marks]
- b) What is each participant expected to do during the sprint planning activity? Are external stakeholders permitted to attend? [5 marks]
- c) How is the Planning Poker used for sizing PBIs? Clarify the concepts that is based on and the rules it applies. [5 marks]
- d) During the sprint planning of a certain sprint of 2-week duration iterations, an agile team composed of 5 persons (working 40 hours a week) has picked 4 stories: [10 marks]

AIN SHAMS UNIVERSITY, FACULTY OF ENGINEERING		
i-CREDIT HOURS ENGINEERING PROGRAMS, COMPUTER ENGINEERING AND SW SYSTEMS PROGRAM		
Summer Semester 2019	Course Code: CSE325	Time Allowed: 3 Hrs.
	Agile Software Engineering	
The Exam Consists of Three Questions in Two Pages.		2 / 2

Story 1 – 5 story points

Story 2 – 4 story points

Story 3 – 6 story points

Story 4 – 8 story points

At the end of the sprint, the team delivered Story 1 and Story 2 and the customer accepted these. The team almost completed Story 3 as well, but there were few small bugs identified in the acceptance testing, while completed 50% of Story 4.

- i. Calculate the velocity of this team in terms of story points.
- ii. If the team has successfully passed the acceptance testing of Story 3 in that iteration, will the velocity calculation change?
- iii. If the team completed user-stories estimated to be 320 hours of ideal time in that sprint, calculate the focus factor of this team.
- iv. If the current release has been estimated to include 270 story points, determine how many sprints are expected to have in order to finalize this release.
- v. As shown, Story 4 has double story points than Story 2. What is the relation between these estimated story points and the business value of these two user stories? Does this indicate double business value as well?

END of Exam, Good Luck

Examination Committee

Dr. Sherin Moussa

Exam. Date : 25thof Aug, 2019



Summer Semester 2019

Course Code: CSE 347

Time allowed: 3 Hrs.

Embedded System Design

The Exam Consists of **Four** Questions in **two** Pages.

Maximum Marks: 40 Marks

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تعليمات هامة

- حيازة التيلفون المحمول مفتوحا داخل لجنة الامتحان يعتبر حالة عش تستوجب العقاب وإذا كان ضروري الدخول بالمحمول فيوضع مغلق في الحقائب.
- لا يسمح بدخول سماعة الأذن أو البلوتوث أو الأجهزة الإلكترونية.
- غير مسموح بدخول أي كتب أو ملازم أو أوراق داخل اللجنة.

Question 1: (10 Marks)

- What is the worst response time for the background process in a foreground-background system in which the background requires 100 milliseconds to complete, foreground task F executes every 50 milliseconds and requires 25 milliseconds to complete, and context switching requires no more than 100 microseconds (recall that background task may be preempted)
- Calculate processor utilization and hyper-period for the following task set:

Task#	E	P
1	3	7
2	5	16
3	3	15

Question 2: (10 Marks)

- Verify the schedulability under earliest deadline first algorithm and construct the schedule of the following task set: $\tau_1 \equiv \{1, 5, 4\}$, $\tau_2 \equiv \{2, 8, 6\}$, and $\tau_3 \equiv \{1, 4, 3\}$. Here, the notation $\tau_i \equiv \{e_i, p_i, D_i\}$ gives the execution time, e_i , period, p_i , and relative deadline, D_i , of task τ_i .
- An I²C system is built with 2 masters and 3 slaves, the addresses of the devices in hexadecimal are 1A, 1B, 05, 07 and 0C respectively. Consider the case where master 1A is writing to slave 05 and master 1B is reading from slave 0C:
 - Draw a complete connectivity diagram showing the five devices.
 - How would the clock of the entire bus is synchronized?
 - Show which master will succeed to access the desired slave in a bit by bit fashion assuming the 2 masters sensed the bus idle at the same time

Question 3: (10 Marks)

- Consider the following Free RTOS code snippet, identify how many tasks are scheduled, and identify the period of each task (assuming a rate monotonic processes). Draw a time diagram to show the scheduling of the tasks.

```
int main( void )
{
    xTaskCreate( vTaskFunction1, "Task 1", 240, NULL, 1, NULL );
    xTaskCreate( vTaskFunction1, "Task 2", 240, NULL, 2, NULL );
    xTaskCreate( vTaskFunction2, "Task 3", 240, NULL, 2, NULL );
    vTaskStartScheduler();
    for(;;);
}
```

```

void vTaskFunction1( void *pvParameters )
{
    for(;;)
    {
        // Do Something
        vTaskDelay( 250 / portTICK_RATE_MS );
    }
}
void vTaskFunction2( void *pvParameters )
{
    for(;;)
    {
        // Do Something
        vTaskDelay( 350 / portTICK_RATE_MS );
    }
}

```

- b. Consider a system that has 3 tasks with the same priorities and periods of 150, 200, and 200 ms. Use the free RTOS task scheduling to construct a program that performs the required tasks scheduling. Write down a skeleton for each task

Question 4: (10 Marks)

a. A system is designed to handle the following situation, A pipeline is used to prepare a certain type of food by a series of 5 heating operations. At the beginning of each operation a sensor is used to measure the temperature, and for each operation an electrical heater is turned on or off to control the temperature. Sensors are numbered 1 to 5. Each sensor is sampled on a period of 10 seconds and its value and sensor ID is pushed into a queue (assume there is some tasks that do so). A control task is executed every 15 seconds to check if any of the readings is lower than the desired set value, if so the corresponding heater is turned ON, otherwise it is turned off. Assume an array holds the desired set temperatures for each stage, prepare a program using Free RTOS Queue and APIs to perform the described tasks. You need to define a suitable data structure for the data in the queue and you need only to define the queue size and write the control task logic. Assume for the heaters an 8 bits integer variable h is used to turn on and off the heater by setting (1) or resetting (0) a bit respectively. For example to turn heater 1 and 4 ON and the rest OFF, the variable h=should hold the value (000001001) in binary or 09 in hexadecimal.

b. Write a Free RTOS code that will respond to an interrupt on PORT B by differing the control to a task function called Task1. The necessary startup is done and the function void InterruptHx(void) is the corresponding ISR.

Good Luck

Examiner(s): Prof. Ayman M. Bahaa-Eldin



Summer Semester 2019

Course Code: CSE 429

Time allowed: 3 Hrs.

Software Quality Assurance

The Exam Consists of **Four** Questions in **Two** Pages.

Maximum Marks: 40 Marks

1 / 2

تعليمات هامة

- حيازة التليفون المحمول مفتوحا داخل لجنة الامتحان يعتبر حالة غش تستوجب العقاب وإذا كان ضروري الدخول بالمحظوظ فيوضع مغلق في الحقائب.
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Final Exam

Question 1: (10 Marks)

- a- For the following C program, compute Halstead Purity Ratio, number of lines of code (KLOC) and Cyclomatic Complexity **(4 marks)**

```
if (k < 3)
{
    if (k > 2)
        x = x*k;
}
```

- b- Provide one example for both software Project, Process and Product metrics and compare their effort and benefits **(3 marks)**

- c- Compare between the **Halstead** metrics, **McGabbey** cyclomatic complexity and **KLOC** (kilo lines of code) metrics which of them could be better to estimate the productivity of development teams. **(3 marks)**

n1 - number of distinct operators, n2 - number of distinct operands

N1 - total number of operators, N2 - total number of operands

Program length: $N = N_1 + N_2$, Program vocabulary: $n = n_1 + n_2$

Estimated length: $EN = n_1 \log_2 n_1 + n_2 \log_2 n_2$ **measure for well structured programs**

Purity ratio: $PR = EN / N$

Question 2: (10 Marks)

It is required to build a software House of Quality (HoQ) for a software application of a scientific calculator that solves advanced non-linear equations

- a) List at least **Four** what's of relevant user requirements/quality and prioritize them (give rank of 4 to the most important one and rank of 1 to the least important one) **(3 marks)**

- b) If the following are possible hows

- the designed number of iterations for the solving algorithm
- the time to finish the computation
- the value of the time interval

Fill the matrix cells between what and how with values either (empty, 1,3,9) **(3 marks)**

how vs how (house ceiling) with (1 , empty or -1) **(2 marks)**

- c) compute the relative importance of each of the hows and reorder them **(2 marks)**

Summer Semester 2019	Course Code: CSE429	Time Allowed: 3 Hrs.
Software Quality Assurance		
The Exam Consists of four Questions in Two Pages.		2/ 2

Question 3: (10 Marks)

Consider an online auction software application, fill the following FMEA table with all relevant data for each of the following failure modes:

- System delays members' bids
 - System lets incorrect member or IP address win the auction
 - System reveals the privacy of the members
- a) Why can FMEA be useful for software quality assurance? **(1 mark)**
- b) for each failure mode, list consequences and possible causes and then estimate SEV, OCC, DET from 1-10 and hence compute RPN **(6 marks)**
- c) Suggest one solution to enhance the RPN of each failure mode and estimate the new values for SEV, OCC, DET and PRN **(3 marks)**

Potential Failure Mode and Effects Analysis																		
(Design FMEA)																		
System Subsystems Component Model/Year / Vehicle(s); Core Team:																		
Design Responsibility: Key Date : FMEA Number: Prepared by: FMEA Date (Orig.): (Rev.):																		
Item / Function	Requirements	Potential Failure Mode	Potential Effects of Failure	S E V S	L A S S	C P O C	Potential Causes / Mechanisms of Failure	Current Design Controls Prevention	O C C	Current Design Controls Detection	D E T	R P N	Recommended Actions	Responsibility & Target Completion Date	Action Results			
															Actions Taken			

Question 4: (10 Marks)

- a. Explain what the KAIZEN process is **(2 marks)**
- b. Suggest which stage of software development can be enhanced more using KAIZEN, provide some example support your suggestion **(3 marks)**
- c. Explain the process of affinity diagram **(2 marks)**
- d. list the benefits that can be gained from applying affinity diagram to software quality assurance (SQA) **(3 marks)**

AIN SHAMS UNIVERSITY
FACULTY OF ENGINEERING

Credit Hours Engineering Programs - CHEP

Computer Engineering and Software Systems Program

Computer and Systems Engineering Department



Summer 2019

Course Code: ECE 141

Time Allowed : 3.00 Hrs

Electrical and Electronic Circuits

The Exam Consists of **Three** Questions in **Three** Pages.

Total Marks: 40 Marks

1 / 3

تعليمات هامة

(1) لا يسمح بدخول التليفون لجنة الامتحان و يعتبر حالة غش تستوجب العقاب.

(2) لا يسمح بدخول سماعة الأذن أو البلوتوث.

(3) لا يسمح بدخول أي كتب أو ملازم أو أوراق داخل اللجنة والمخالفه تعتبر حالة غش.

Question 1 [15 marks]

A) Find v_1 in the circuit of Figure 1. [2 marks]

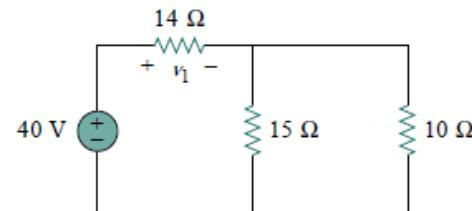


Figure 1

B) Using nodal analysis, write down the equations required to calculate v_o in the circuit in Figure 2. [4 marks]

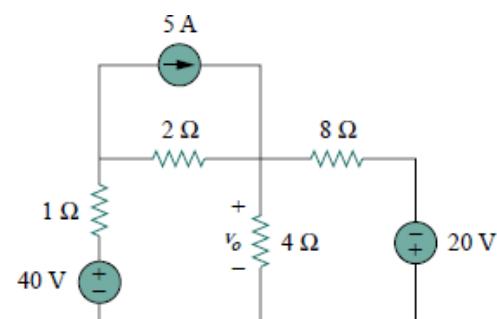


Figure 2

C) Using source transformation, find v_x in the circuit of Figure 3. [4 marks]

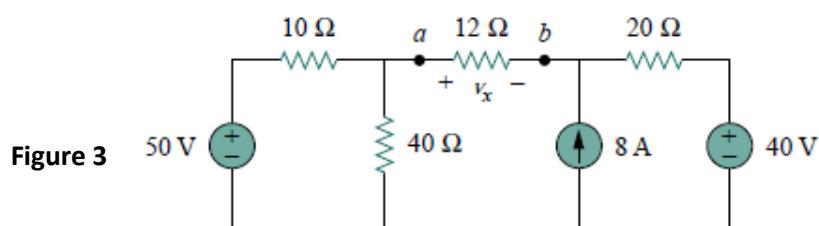


Figure 3

D) For the circuit in Figure 4, calculate the Thevenin equivalent between a and b . [5 marks]

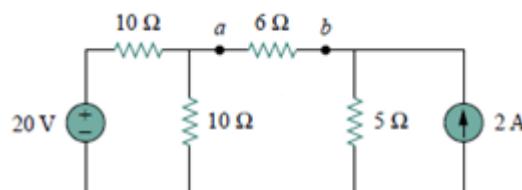


Figure 4

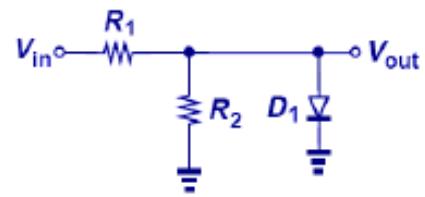
Question 2: [13 marks]

A) For the shown circuit in Figure 5, calculate V_{out} for the following cases:

(4 marks)

(i) $V_{in} = +5 \text{ V}$

(ii) $V_{in} = -5 \text{ V}$



Assume constant voltage drop model $V_D = 0.7 \text{ V}$

Figure 5

B) For the shown circuit in Figure 6, sketch v_o for a sinusoidal input $v_{in} = V_m \sin \omega t$. Assume ideal diodes. [3 marks]

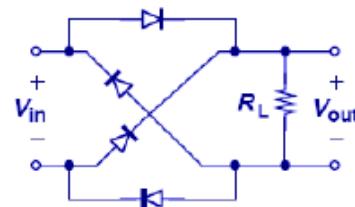


Figure 6

C) Sketch v_o for $v_i = V_m \sin \omega t$ for the circuit in Figure 7 with $V_m > V$. Assume an ideal diode. [3 marks]

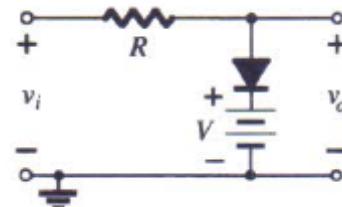


Figure 7

D) For the opamp in Figure 8, Calculate v_o . [3 marks]

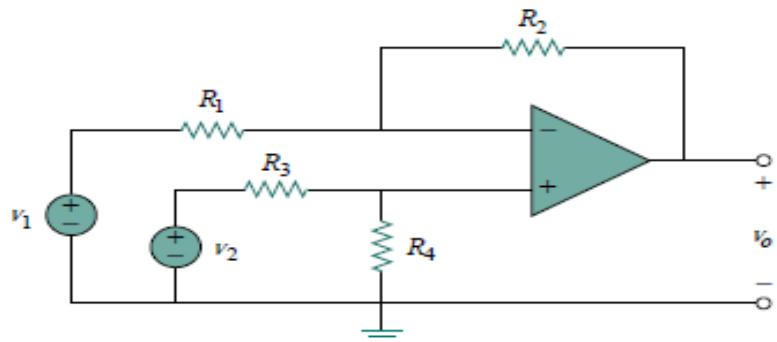


Figure 8

Question 3 [12 marks]

- A) For the circuit shown in Figure. 9, $k_n \frac{W}{L} = 60 \mu A / V^2$ and $V_t = 1 V$. Calculate V_2 and I_L . [6 marks]

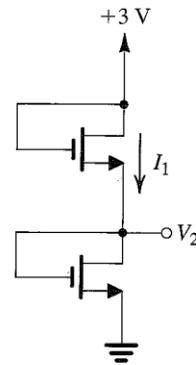


Figure 9

- B) For the shown amplifier using NMOS in Fig. 10, the DC analysis shows that $V_S = 3 V$.

The transistor has $V_t = 1 V$, $V_A = 100 V$,
 $k_n \frac{W}{L} = 2 mA/V^2$.

- (i) What is the function of each capacitor in the circuit [2 marks]
(ii) Calculate v_o/v_{sig} . [3 marks]
(iii) Calculate R_{in} . [1 mark]

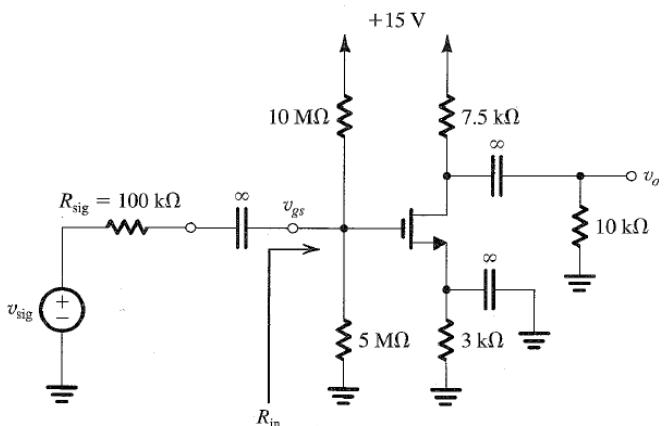


Figure 10

Useful Equations

For NMOS:

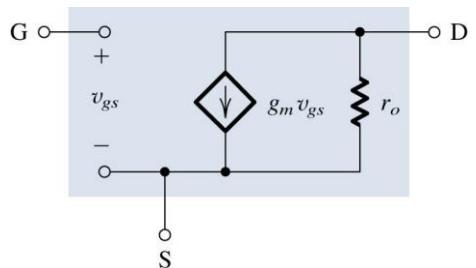
In the triode region ($V_{DS} < V_{GS} - V_t$), we have: $I_D \approx \frac{W}{L} k'_n (V_{GS} - V_t)V_{DS}$

In the saturation region ($V_{DS} > V_{GS} - V_t$), we have:

$$I_D = \frac{W}{2L} k'_n (V_{GS} - V_t)^2$$

$$r_o = \frac{V_A}{I_D} \text{ and}$$

$$g_m = \frac{W}{L} k'_n (V_{GS} - V_t)$$



END of Exam, Good Luck