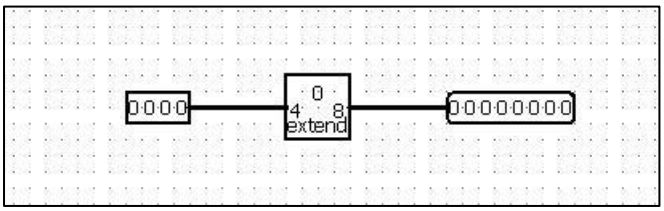
Logic Project Report

Sunday 4-6		
ID	**Name**	**Tasks**
1190419	Zyad Khaled Salah	4-Bit Adder Multiplier
1190384	Moaz Ahmed Abomousa	Negative Subtract Not
1190477	Omar Mohamed Faheem	Shift Left Shift Right Move
1190423	Nourhan Ahmed Helmy	And Or Xor

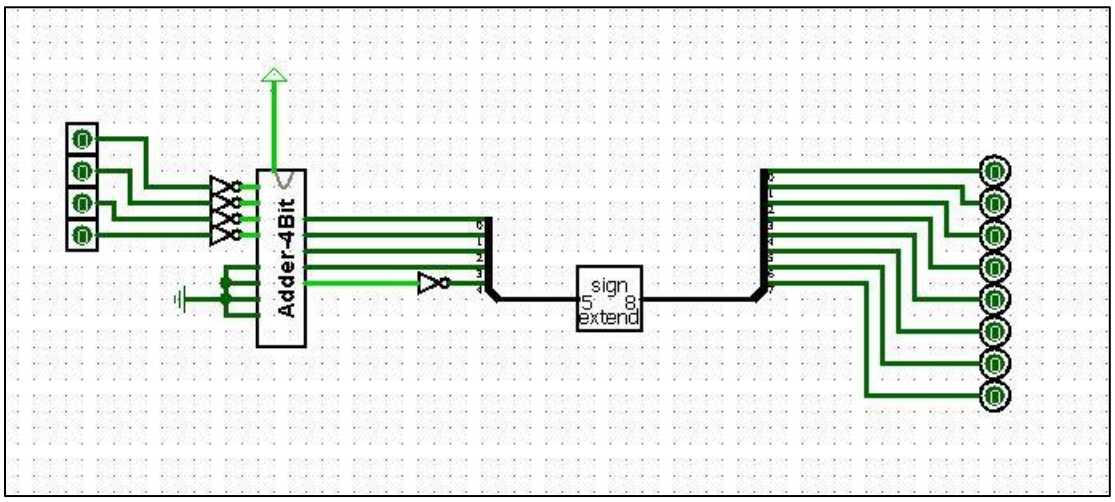
Block Diagrams & No. of Gates

1-Move:



- **Gates: 0**

2-Negative:

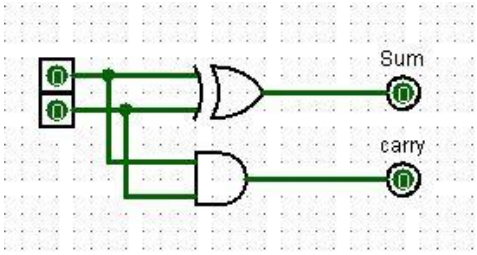


- **Gates:**

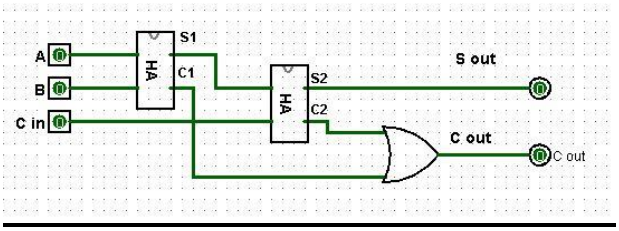
Gate	Number of occurrences
2-AND	8
2-OR	4
XOR	8
NOT	5
Total	225

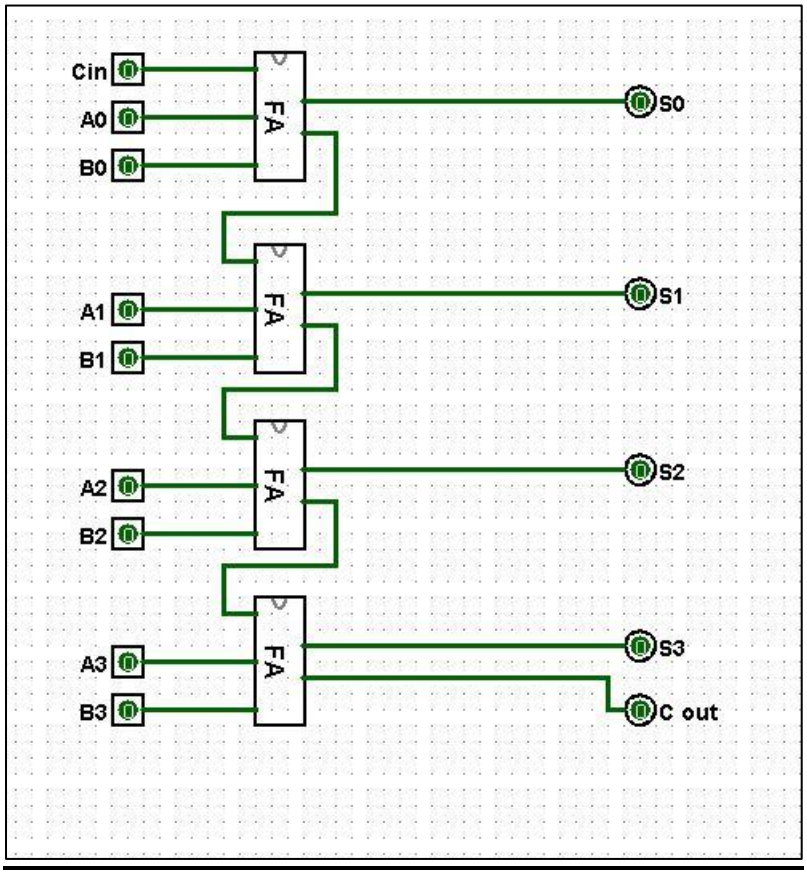
3-Bit Adder:

Half Adder:



Full Adder:

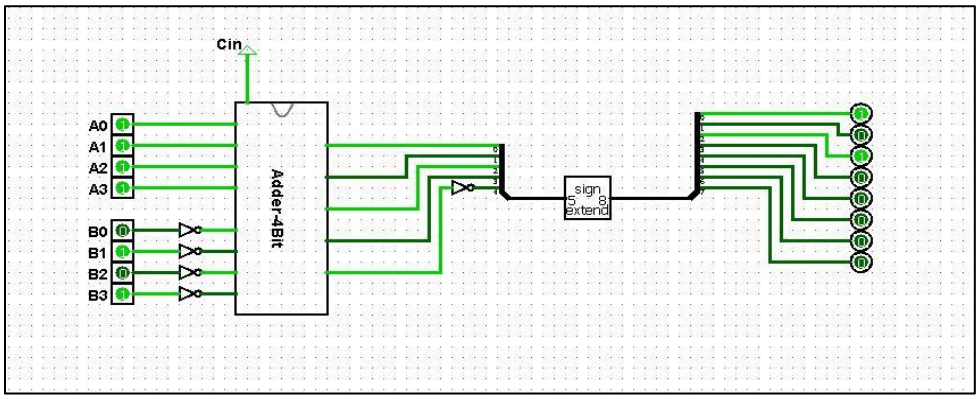




- **Gates:**

Gate	Number of occurrences
2-AND	8
2-OR	4
XOR	8
Total	20

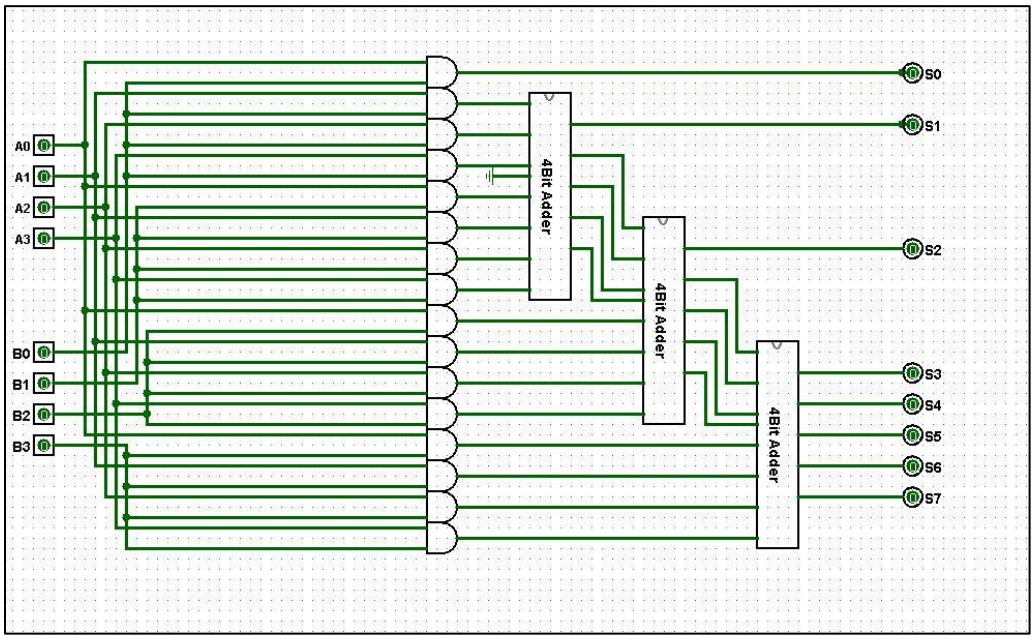
4-Subtractor:



- **Gates:**

Gate	Number of occurrences
2-AND	8
2-OR	4
XOR	8
NOT	5
Total	225

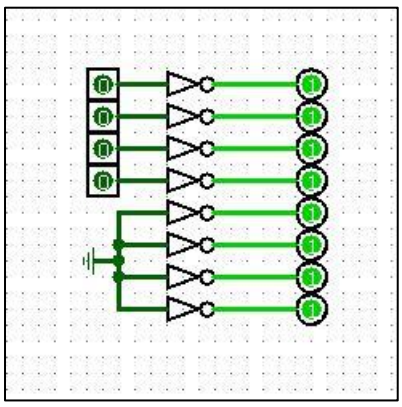
5-Multiplier:



- **Gates:**

Gate	Number of occurrences
2-AND	40
2-OR	12
XOR	24
Total	76

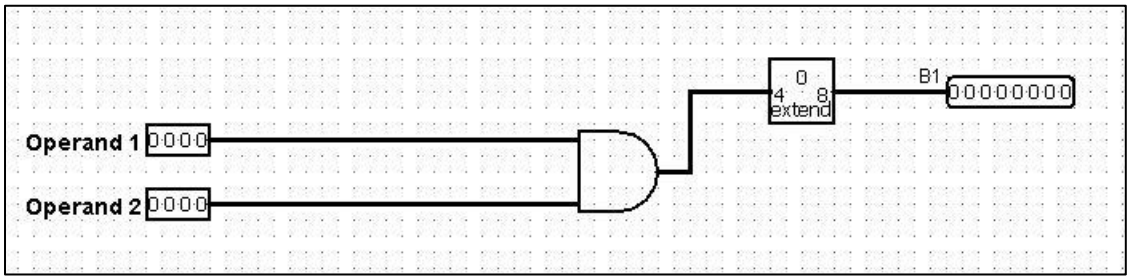
6-Not:



- **Gates:**

Gate	Number of occurrences
NOT	8
Total	8

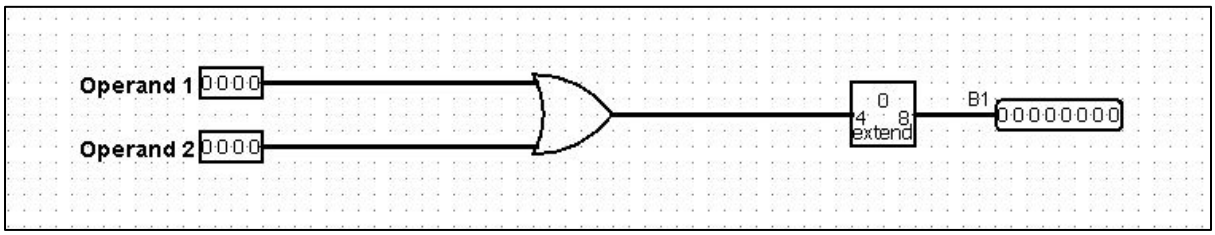
7-And:



- **Gates:**

Gate	Number of occurrences
AND	1
Total	1

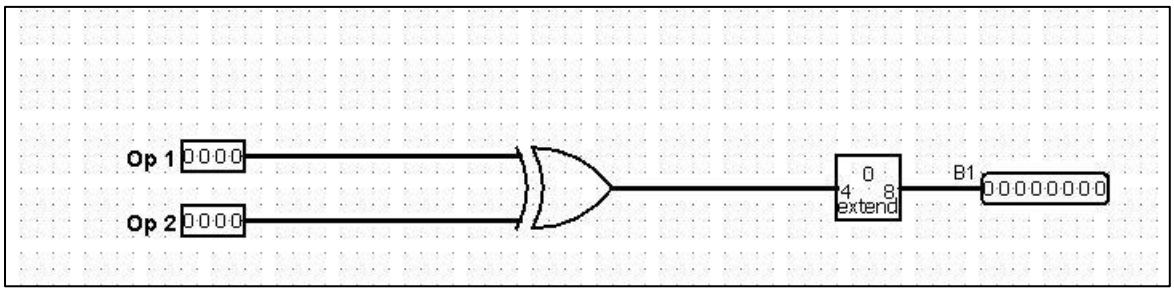
8-Or:



- **Gates:**

Gate	Number of occurrences
OR	1
Total	1

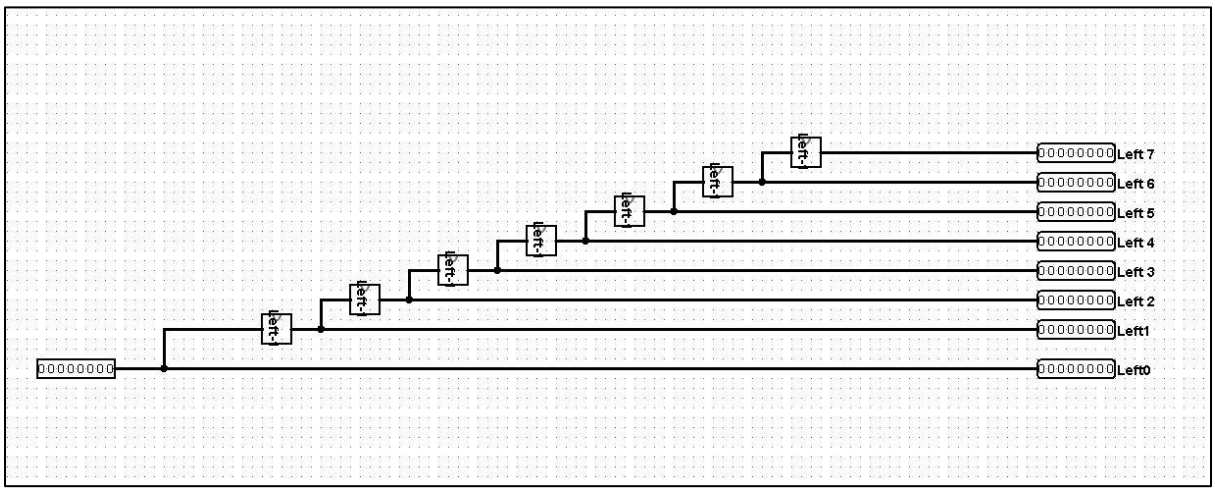
9-Xor:

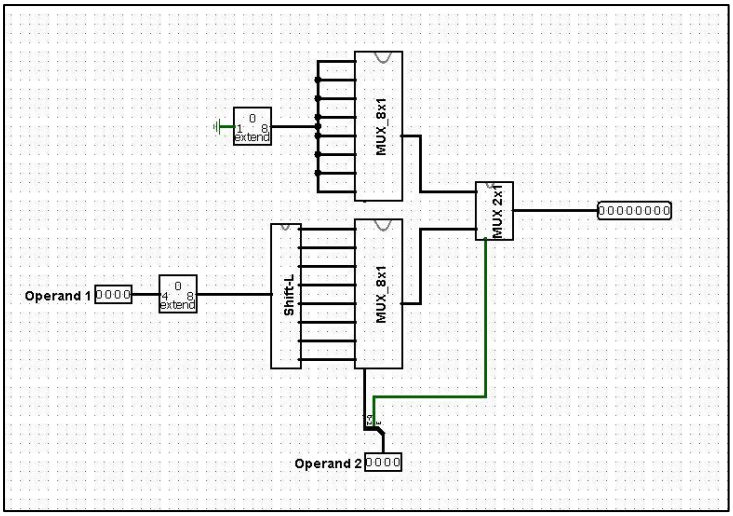


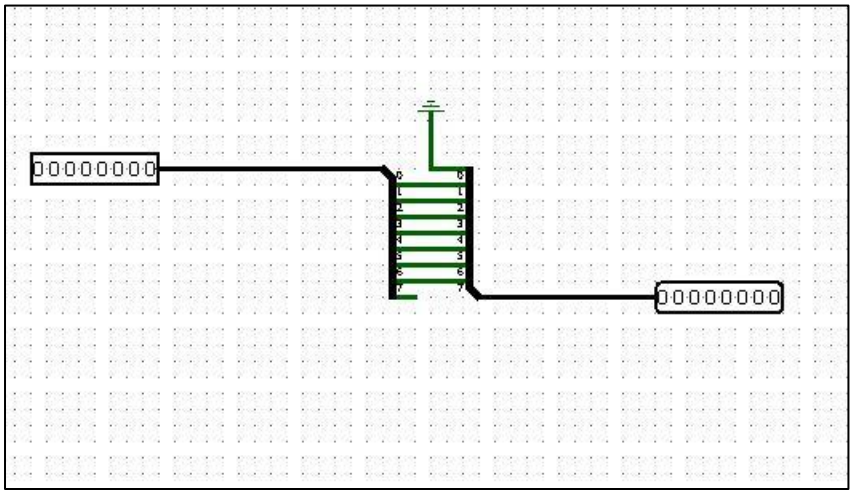
- **Gates:**

Gate	Number of occurrences
XOR	1
Total	1

10-Shift Left:



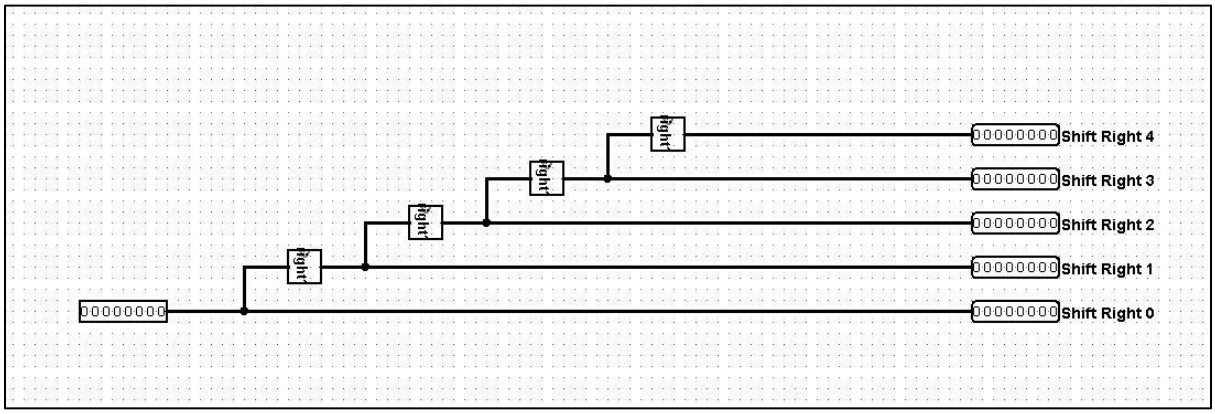


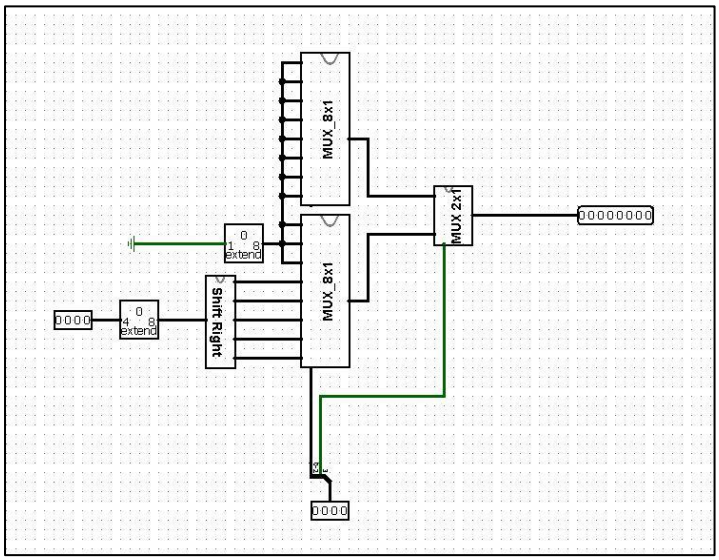


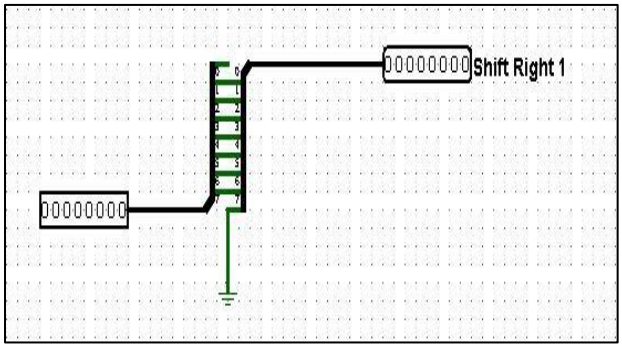
- **Gates:**

Gate	Number of occurrences
2-AND	30
2-OR	15
NOT	15
Total	60

11-Shift Right:







- **Gates:**

Gate	Number of occurrences
2-AND	30
2-OR	15
NOT	15
Total	60

Final Circuit Presentation