Remember...

1. turn projector off
2. do NOT lock tables
3. push chairs in

4/7 (1)

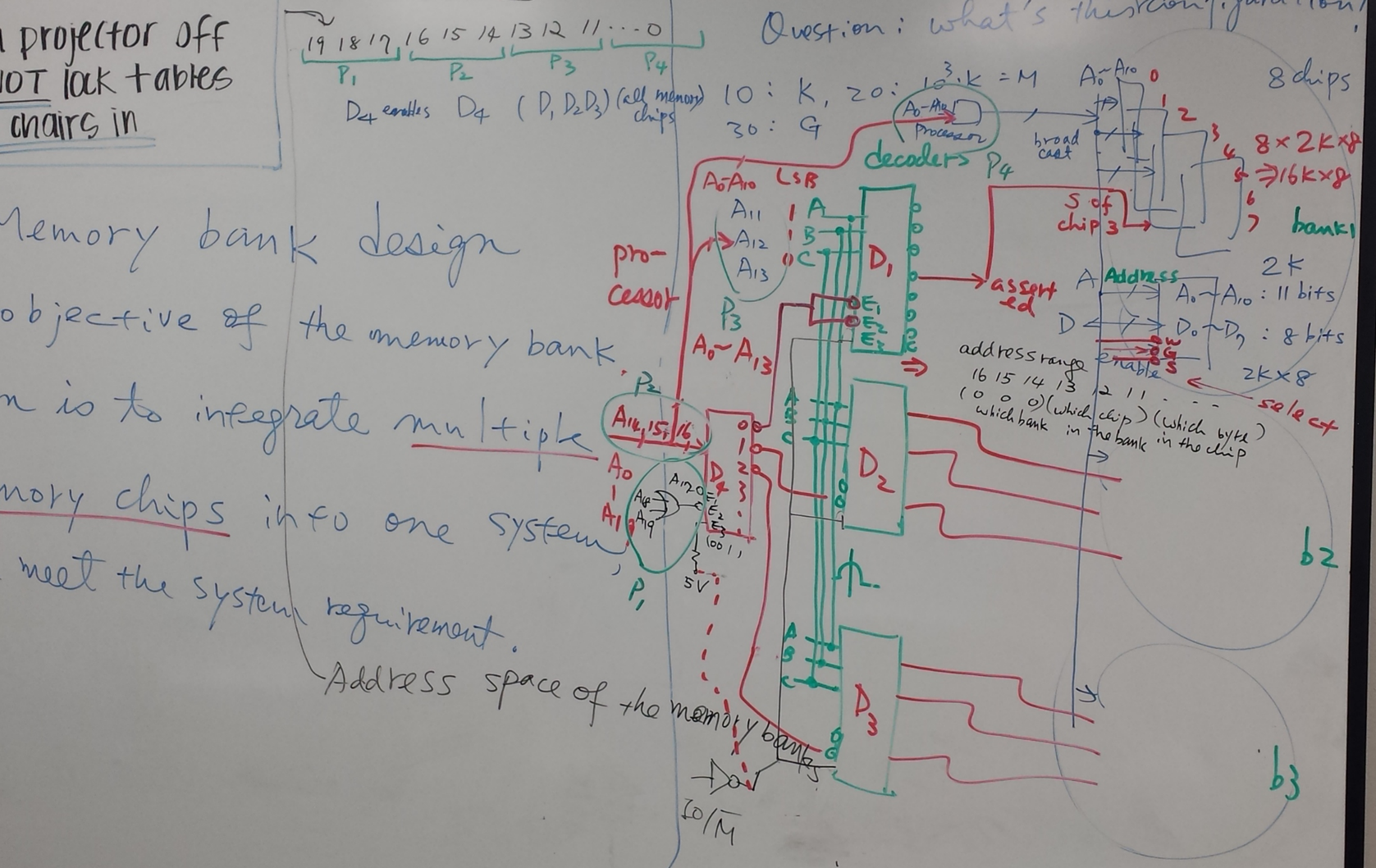
Memory bank design

The objective of the memory bank design is to integrate multiple memory chips into one system, and meet the system requirement.

Address space of the memory banks

example P193.

Question: what's this memory configuration?



when (19,18,17) = (0 0 0),
D_4 enabled, it will assert one output based on the input value
the input: (16, 15, 14)

each output corresponds to one bank: {8 chips}

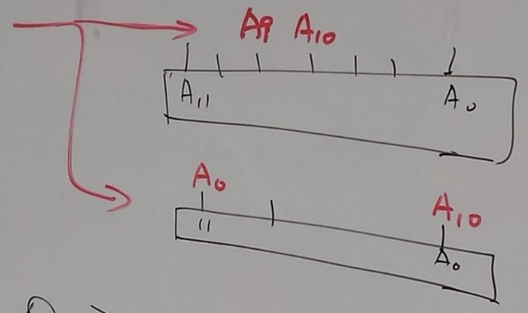
- For the chosen decoder, say D_2, it asserts the output corresponding to its inputs (13, 12, 11).

each output corresponds to one chip in a particular bank

- The asserted output enables its connected chip, in
- $A_0 - A_{10}$ broadcast to all chips
- Data lines all "tied" together
  ⇒ only the asserted chip will set values on D lines

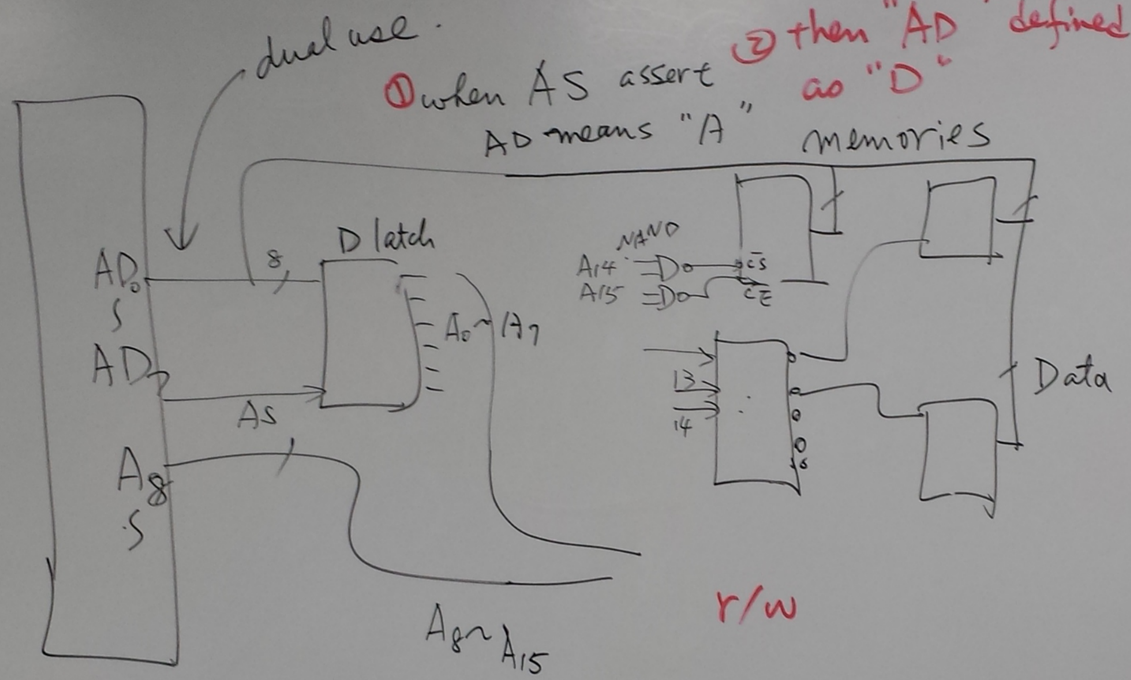
$A_0 - A_{11}$, some junior engineer made a mistake. swap 2 lines

A_{11} A_{10} ---- A_0



Q ⇒ what would happen? can a software test detect the error?

What if this happens to D_4's inputs?



what's the address space distribution?