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Cortex A9 Technical Reference Manual

• The Cortex-A9 processor is a single core processor. • The multiprocessor variant, the Cortex-A9 MPCore™ processor, consists of between one and four Cortex-A9 processors and a Snoop Control Unit (SCU). See the Cortex-A9 MPCore Technical Reference Manual for a description. Using this book This book is organized into the following chapters:

Cortex-A9 Technical Reference Manual - ARM architecture

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Cortex-A9 Technical Reference Manual - ARM architecture

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• Cortex™ -A9 Technical Reference Manual (ARM DDI 0388) • Cortex-A9 MPCore Technical Reference Manual (ARM DDI 0407) • Cortex-A9 Configuration and Sign-Off Guide (ARM DII 0146) • AMBA AXI Protocol Specification (ARM IHI 0022) • ARM Architecture Reference Manual, ARMv7-A and ARMv7-R edition (ARM DDI 0406).

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• ARMv7-M Architecture Reference Manual (ARM DDI 0403) • ARM Cortex-M4 Integration and Implementation Manual (ARM DII 0239) • ARM ETM-M4 Technical Reference Manual (ARM DDI 0440) • ARM AMBA® 3 AHB-Lite Protocol (v1.0) (ARM IHI 0033) • ARM AMBA™ 3 APB Protocol Specification (ARM IHI 0024) • ARM CoreSight™ Components Technical ...

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13 June 2007 E Non-Confidential Minor update with no technical changes 11 April 2008 F Confidential Limited release for SC300 r0p0 26 June 2008 G Non-Confidential First Release for r2p0

Cortex-M3 Technical Reference Manual - Keil

List of Tables ARM DDI 0337E Copyright © 2005, 2006 ARM Limited. All rights reserved. ix Table 9-1 MPU registers 9-3

Cortex-M3 Technical Reference Manual - Keil

The ARM Cortex-A9 MPCore is a 32-bit processor core licensed by ARM Holdings implementing the ARMv7-A architecture. It is a multicore processor providing up to 4 cache-coherent cores.

ARM Cortex-A9 - Wikipedia

This preface introduces the Cortex-A9 MBIST Controller Technical Reference Manual. ... In this book, the generic term MBIST controller means the Cortex-A9 MBIST controller, and Cortex-A9 processor means the Cortex-A9 processor family. Product revision status The r npn identifier indicates the revision status of the product described in this manual,

Cortex -A9 MBIST Controller - ARM architecture

See the Cortex-A9 Technical Reference Manual for information on these registers. To use the FPU in Secure state only To use the FPU in Secure state only, you must define the CPACR and Floating-Point Exception Register (FPEXC) registers to enable the FPU: 1.

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