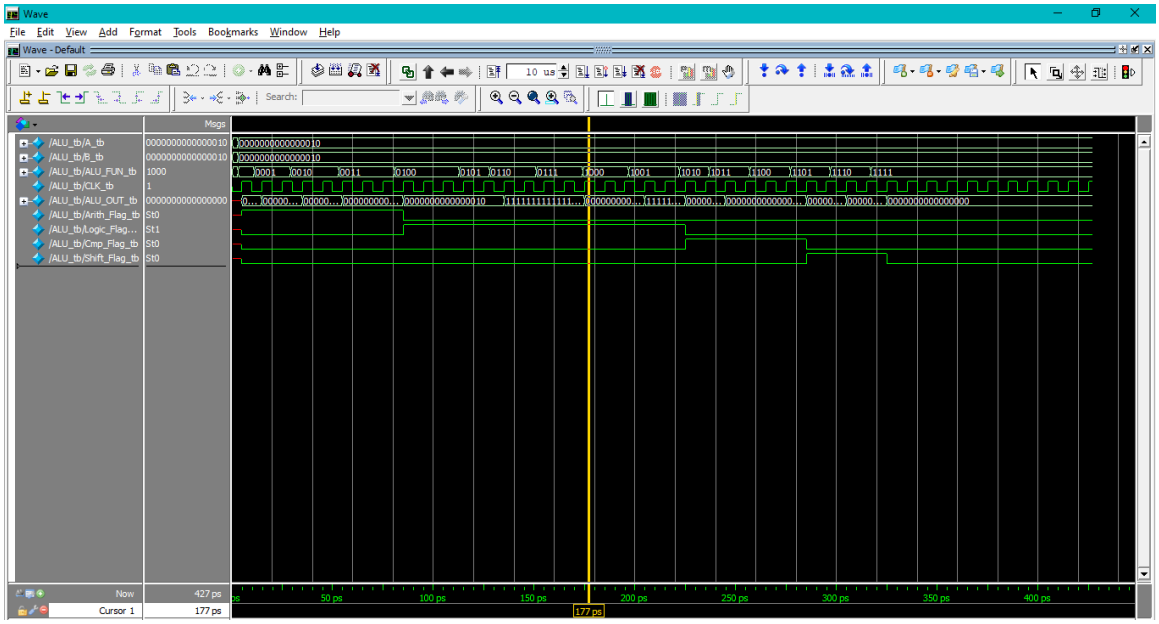

Figure 1:Simulation output

```
VSIM 14> restart
# Closing VCD file "ALU.vcd"
VSIM 15> run -all
# A=    0,B=    0
# TEST CASE 1 Check addition
# TEST CASE 1 IS Passed,        A=    2,        B=    2,        OUT=    4
# TEST CASE 2 Check Subtraction
# TEST CASE 2 IS Passed,        A=    2,        B=    2,        OUT=    0
# TEST CASE 3 Check Multiplication
# TEST CASE 3 IS Passed,        A=    2,        B=    2,        OUT=    4
# TEST CASE 4 Check division
# TEST CASE 4 IS passed,        A=    2,        B=    2,        OUT=    1
# TEST CASE 5 Check AND
# TEST CASE 5 IS passed,        A=    2,        B=    2,        OUT=    2
# TEST CASE 6 Check OR
# TEST CASE 6 IS PASSED,        A=    2,        B=    2,        OUT=    2
# TEST CASE 7 Check NAND
# TEST CASE 7 IS PASSED,        A=    2,        B=    2,        OUT=1111111111111101
# TEST CASE 8 Check NOR
# TEST CASE 8 IS PASSED,        A=    2,        B=    2,        OUT=1111111111111101
# TEST CASE 9 Check XOR
# TEST CASE 9 IS PASSED,        A=    2,         B=    2,       OUT=0000000000000000
# TEST CASE 10 Check XNOR
# TEST CASE 10 IS PASSED,       A=    2,        B=    2,        OUT=1111111111111111
# TEST CASE 11 Check CMP :A=B
# TEST CASE 11 IS PASSED,       A=    2,        B=    2,        OUT=    1
# TEST CASE 12 Check CMP:A>B
# TEST CASE 12 IS PASSED,       A=    2,        B=    2,        OUT=    0
# TEST CASE 13 Check CMP:A<B
# TEST CASE 13 IS PASSED,       A=    2,        B=    2,        OUT=    0
# TEST CASE 14 Check Shift:A>>1
# TEST CASE 14 IS PASSED,       A=    2,        B=    2,        OUT=    1
# TEST CASE 15 Check Shift A <<1
# TEST CASE 15 IS PASSED,       A=    2,        B=    2,        OUT=    4
# TEST CASE 16 Check Default
# TEST CASE 16 IS PASSED,       A=    2,        B=    2,        OUT=    0
# Break in Module ALU_tb at E:/cairo university enginner 5 years/Digitaldesgin/CROCODILE/verilog/Session three/ALU_tb.v line 223
```

Figure 2:Display screen for testbench