OMKAR BHILARE

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EDUCATION

University of Toronto (UofT), Toronto, Canada — ***Advisor:*** *Prof. Jason Anderson*
Masters in Applied Science in Electrical Computer Engineering [**GPA**: 3.8/4] — *September 2023 - PRESENT*

- **Relevant Coursework: ECE552** (Computer architecture) | **ECE1718** (Advanced computer architecture) | **ECE1756** (Reconfigurable computing & FPGA architecture) | **ECE1755** (Parallel computer architecture & programming) | **ECE1387** (CAD for digital circuit synthesis and layout)

Veermata Jijabai Technological Institute (VJTI), Mumbai, India — ***Thesis Advisor:*** *Prof. Faruk Kazi*
B.Tech in Electronics Engineering [**GPA**: 9.13/10] — *July 2019 - May 2022*

TEACHING EXPERIENCE

- **ECE1387: CAD for Digital Circuit Synthesis and Layout** [Fall@2024] — *Prof. Jason Anderson*
  - **Assignment Grading:** Evaluated CAD assignments on advanced algorithms like A*, branch-and-bound, and analytical placement techniques, providing feedback to enhance student understanding.
  - **Exercise Grading:** Co-created and graded an exercise using the UGRAMM toolchain, which I optimized for better functionality and a seamless experience for students and instructors.
- **CSC258: Computer Organization** [Fall@2024] — *Prof. Steve Engels*
  - **Lab Management & Grading:** Conducted digital circuits lab sessions on Logisim and Intel FPGA, assisting students and ensuring smooth lab operations.
- **ECE 241: Digital Systems** [Fall@2023] [Fall@2024] — *Prof. Bruno Korst*
  - **Lab Management & Exam Assessment:** Facilitated lab sessions for digital and FPGA circuits, offering student guidance and conducting exam assessments to monitor progress.
  - **Float TA:** Supported students and fellow TAs, addressing lab questions and solving problems across multiple sections.
- **ECE 532: Digital Systems Design** [Winter@2024] [Summer@2024] — *Prof. Jason Anderson*
  - **Tutorial Management & Project Mentoring:** Managed FPGA lab tutorials and mentored two student groups through a semester-long digital design project, assessing progress with weekly milestones and providing feedback during demos.
  - **Course Development:** Contributed to integrating a new Microchip FPGA discovery kit into the course.

PUBLICATIONS

Conference Papers

[1] Haoran Wei, ***Omkar Bhilare***, Hamas Waqar, and Jason H. Anderson. "CAD Techniques for NoC-Connected Multi-CGRA Systems." *HEART '24: Proceedings of the 14th International Symposium on Highly Efficient Accelerators and Reconfigurable Technologies*, 2024. https://dl.acm.org/doi/10.1145/3665283.3665297

[2] ***Omkar Bhilare***, Rahul Singh, Vedant Paranjape, Sravan Chittupalli, Shraddha Suratkar, and Faruk Kazi. "DEEP-FAKE CLI: Accelerated Deepfake Detection Using FPGAs." *Parallel and Distributed Computing, Applications and Technologies (PDCAT 2022)*, 2022. https://doi.org/10.1007/978-3-031-29927-8$_4$

RESEARCH EXPERIENCE

Processor Architecture Laboratory (LAP), EPFL — **Prof. Paolo Ienne, Mr. Andrea Guerrieri**
Summer@EPFL — *June 2022 - August 2022*

- Designed a framework for Dynamatic (a dynamic HLS compiler) to access external memory using AXI interconnect [BLOG]
- Developed a custom-built AXI master with burst support and successfully tested it with load-store queues (LSQs) of Dynamatic
- Added Burst support in a dynamic environment of Dynamaitc using special-built BOM (Burst & Outstanding Manager) modules
- **Dynamatic's memory handling capabilities were substantially expanded by the unit, at a mere 2% LUT and 4% FF count increase**

Centre of Excellence in Complex and Non-Linear Dynamical Systems, VJTI — **Prof. Faruk Kazi**
Bachelor's thesis: Accelerated Deepfake detection on VCK5000 Versal FPGA [BLOG] — *June 2021 - May 2022*
Research Associate

- Trained, quantized, and compiled various AI models for Xilinx Zynq and Versal FPGA platforms
- Benchmarked and achieved a **120% improvement in model inference speed** on the VCK5000 over the state-of-the-art Nvidia Tesla T4 GPU inference speed
- Impact of employing different quantization levels of a deep learning model on inference speed and optimization of Deepfake detection model for VCK5000 FPGA led to a conference paper at (PDCAT'22)

Shakti Lab, RISE Group, IIT Madras **Prof. V. Kamakoti, Mrs. Lavanya J**
Research Verification Intern [REPORT] *March 2021 - July 2021*

- Worked under the guidance of Prof. V. Kamakoti, who is the director of IITM and head of the SHAKTI, RISE group. They made **SHAKTI, which is India's first indigenous processor**. I designed and developed a **framework to verify the SHAKTI RISC-V processors on FPGAs**
- Developed an automation flow called *AAPG on FPGA* which automatically generates single and multiple tests produced by Automated Assembly Program Generator (AAPG), which are suitable to run on FPGA directly
- Successfully verified the framework by running a softcore VAJRA SoC on an Arty A7 FPGA. Obtained signature dumped from FPGA using OpenOCD and RISC-V GDB and compared it with the golden signature from *S*pike, a RISC-V ISA Simulator
- The proposed work **accelerated verification speed while maintaining visibility and control** in FPGA flow

WORK EXPERIENCE

AMD **Bangalore, India**
Silicon Design Engineer I *September 2022 - Present*

- Responsible for SoC Level Verification Suite of Debug Unit related IPs in various AMD Processors
- Worked on verifying the low power mode of USB with SoC level verification test. That involved putting the USB into low power mode and afterward reading the block of the ID of the USB IP over IO pads to make sure it is working

AMD **Remote**
Verification Co-op Intern *Dec 2021 - June 2022*

- Verified Debug Unit test suite at SoC Level using various constrained random test cases
- Designed and verified CPU core access test case, which was configurable enough to select one core inside AMD CPU according to the test input and check its accessibility
- Developed verification test case for CPU cross-trigger network between multiple IPs

Google Summer of Code 2021, BeagleBoard Organization **Remote**
Open-Source Developer [REPORT] *June 2021 - Aug 2021*

- Built and tested a **gateware for BeagleWire** (Lattice iCE40 FPGA) cape for Beaglebone Black (a single board computer)
- **Interfaced Arm Chip with Lattice FPGA** using General Purpose Memory Controller (GPMC) and Wishbone protocols
- Developed and tested Wishbone slave and Intercon designs for BeagleWire
- Interfaced BeagleWire with SDRAM using *litedram* core, which included *serv*—a bit-serial RISC-V CPU for initialization of SDRAM IP

AWARDS AND RECOGNITION

- **Adaptive Computing Challenge 2021 by AMD-Xilinx** (Third Place with a prize worth $3000)—an award winner from 165 qualified entries from developers spanning 35 countries
- Received **VCK5000—a Versal architecture-based FPGA** board as a hardware grant (worth $2700)—only 20 such boards were distributed globally among 547 applications
- ***Summer@EPFL*** Scholar: Three-month summer fellowship to conduct cutting-edge research at EPFL
- Selected participant in the prestigious ***Google Summer of Code*** program—a Google-run program that focuses on bringing new contributors into open-source development

PROJECTS

RISC-V core github.com/riscv-core
Icarus Verilog, GTKWAVE, Yosys, Openlane, Magic, TD IDE Jan 2021 - March 2021

- Designed and verified a RISC-V core in Verilog
- For analog VLSI and tapeout process understanding, converted the basic design into silicon (GDSII) format using *Openlane* and *sky130* PDK
- Designed FPGA drivers such as VGA and others for SoC integration
- Validated the VGA driver on Tang primer FPGA with simple DAC made from binary-weighted resistors

8 Bit Computer using 74LS series ICs github.com/8-bit-computer
Logisim, Multisim May 2020 - Nov 2020

- Designed an entire 8 Bit Computer circuit using 74LS series ICs and simulated it in Logisim
- Two cascaded 74LS181 are used for the Arithmetic Logical Unit (ALU) in an 8-bit computer capable of performing 8-bit arithmetic and logical operations. It also has basic general-purpose registers and a program counter made from flipflops

SKILLS

Languages:	Verilog, VHDL, C, Python, Assembly Language(x86, RISC-V)
EDA Tools:	Quartus Prime, Xilinx Vivado, IceStorm
Software & Frameworks:	CoCotb, Icarus Verilog, GTKWave, Proteus, Multisim, Logisim, Git, Linux