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Omkar Bhilare

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Summary — I combine research, industry, teaching experience, and hands-on projects to address complex problems in hardware architectural design, verification, CAD optimization, and FPGA applications for scalable digital systems.

Education

University of Toronto (UofT), Toronto, Canada — ***Advisor:*** *Prof. Jason Anderson*
Masters in Applied Science (MASc) in ECE [**GPA**: 3.8/4] — *September 2023 - Present*

→ **Relevant Coursework: ECE552** (Computer Arch.) || **ECE1718** (Advanced Computer Arch.) || **ECE1756** (Reconfigurable Computing & FPGA Arch.) || **ECE1755** (Parallel Computer Arch. & Prog.) || **ECE1387** (CAD for Digital Circuits Synthesis)

Bachelor's in Engineering (EE), VJTI, Mumbai, India [**GPA**: 9.13/10] — *July 2019 - May 2022*

Publications

[1] H. Wei, **O. Bhilare**, H. Waqar, J.H. Anderson, "CAD Techniques for NoC-Connected Multi-CGRA Systems," *HEART '24* [link]

[2] **O. Bhilare**, *et al.*, "DEEPFAKE CLI: Accelerated Deepfake Detection Using FPGAs," *PDCAT 2022* [link]

Teaching Experience

ECE1387: CAD for Digital Circuit Synthesis and Layout [Fall 2024] — Prof. Jason Anderson

→ Graded assignments focused on advanced CAD algorithms such as A*, branch-and-bound, and analytical placement techniques, providing constructive feedback to help students grasp complex concepts

→ Collaborated on designing and grading an exercise using the UGRAMM toolchain, which I enhanced to improve usability and functionality for both students and instructors

CSC258: Computer Organization [Fall 2024] — Prof. Steve Engels

→ Managed digital circuits lab sessions, guiding students in using tools like Logisim and Intel FPGA to implement and debug their designs

→ Monitored student progress during labs and provided on-the-spot assistance to clarify doubts and troubleshoot issues

ECE 241: Digital Systems [Fall 2023, Fall 2024] — Prof. Bruno Korst

→ Supervised digital systems and FPGA labs, helping students implement circuits, troubleshoot problems, and complete hands-on projects

→ Acted as a float TA, resolving lab queries and supporting other TAs during high-demand periods

ECE 532: Digital Systems Design [Winter 2024, Summer 2024, Winter 2025] — Prof. Jason Anderson

→ Mentored two student groups through semester-long digital design projects, guiding them through weekly milestones, reviewing designs, and offering actionable feedback during project demonstrations

→ Contributed to updating the course by integrating a new Microchip FPGA discovery kit, enhancing the curriculum with modern hardware and tools

Projects

Determining and bridging Area gap between ASIC and CGRA *(Master's Thesis)* — *Aug 2024 - Present*

→ Analyzing programmability costs in modern CGRA architectures by comparing Power, Performance, and Area results from diverse benchmark suites run on both ASIC and CGRA platforms

→ Conducting architectural exploration to identify trade-offs between programmability and performance in CGRA designs

→ Bridging the power gap in CGRA architectures by leveraging fracturable processing elements and analyzing their impact on Performance and Area

NoC-Connected Multi-CGRA Systems — *Jan 2024 - May 2024*

→ Developed a partitioning-based CAD flow for NoC-connected large CGRAs, reducing run time by 33× compared to traditional CAD methods

→ Integrated and customized an open-source min-cut partitioner, TritonPart, to fit specific CGRA CAD requirements

→ Enhanced CAD flexibility with a multi-stage framework, enabling the use of advanced mapping algorithms alongside the partitioning stage, simplifying CAD exploration for large CGRAs

Research Experience

Processor Architecture Laboratory (LAP), EPFL, Switzerland Prof. Paolo Ienne, Mr. Andrea Guerrieri
Summer@EPFL *June 2022 - August 2022*

→ Developed a framework to enable Dynamatic (a dynamic HLS compiler) to access a multi-cycle memory system via a custom AXI interconnect, integrated with its complex out-of-order load-store queues (LSQs)

→ Added burst support within Dynamatic's elastic environment using a custom Burst & Outstanding Manager (BOM) module

→ Enhanced memory accessing capabilities of Dynamatic with only a 2% increase in LUT and a 4% in FF usage

Shakti Lab, RISE Group, IIT Madras, India Prof. V. Kamakoti, Mrs. Lavanya J
Research Verification Intern [REPORT] *March 2021 - July 2021*

→ Designed and developed a framework for verifying SHAKTI, India's first indigenous RISC-V processor family, on FPGAs

→ To verify the processor, the framework produces random assembly tests, executes them on a softcore processor on an FPGA, and compares the execution signatures from FPGA with the golden signature from Spike, an ISA emulator

→ The framework enhanced verification speed, executing 500k RISC-V instructions in jusr 64 seconds on the FPGA softcore— a process that would need hours in conventional techniques— while preserving visibility and control within the flow

Centre of Excellence in Complex and Non-Linear Dynamical Systems, VJTI Prof. Faruk Kazi
Research Associate [Bachelor's thesis] *June 2021 - May 2022*

→ Trained, quantized, and compiled various AI models for deployment on Xilinx Zynq and Versal FPGA platforms

→ Examined the Versal AI architecture and optimized the Deepfake Detection AI model by quantizing it to INT8 and deploying it on Xilinx's CNN accelerator on the VCK5000 Versal FPGA, leveraging AI engines for enhanced performance

→ Achieved a **120% improvement** in the Deepfake Detection model's inference speed on the VCK5000 compared to the state-of-the-art Nvidia Tesla T4 GPU

Work Experience

AMD **Bangalore, India**
Co-Op + Silicon Design Engineer I *Dec 2021 - July 2023*

→ Contributed to SoC-level verification of Design for Debug (DFD) IPs in 3 AMD processors, aiding in successful tapeouts

→ Verified debug infrastructure in IPs, including USB, memory, and CPU cores, etc., using constrained-random test cases, ensuring functional correctness

→ Developed and ported a verification testsuite for DFD IPs across AMD processors, ensuring maximum test coverage and robustness

Google Summer of Code 2021, BeagleBoard Organization **Remote**
Open-Source Developer [REPORT] *June 2021 - Aug 2021*

→ Designed and tested gateware for BeagleWire, a Lattice iCE40 FPGA cape for the BeagleBone Black single-board computer

→ Established seamless communication between the ARM processor and the FPGA using General Purpose Memory Controller (GPMC) and Wishbone protocols

→ Integrated BeagleWire with SDRAM by leveraging the LiteDRAM core, enabling memory initialization through SERV, a lightweight, bit-serial RISC-V CPU

Skills

Language: Verilog, VHDL, C, C++, Python **Systems:** Git, Linux
EDA Tools: Quartus Prime, Xilinx Vivado, Microchip Libero, Yosys, IVerilog, Synopsys Design Compiler, Cadence Innovus

Awards AND Recognition

→ **Adaptive Computing Challenge 2021 by AMD-Xilinx** (3rd place, $3000 prize) – Top 3 out of 165 entries

→ ***Summer@EPFL*** Scholar: Three-month summer fellowship to conduct research at EPFL

→ Selected for the prestigious ***Google Summer of Code*** program, aimed at encouraging new contributors to open-source development.