



MOTOROLA

MCM68A364 MCM68B364

8192 X 8-BIT READ ONLY MEMORY

The MCM68A364/MCM68B364 is a mask-programmable byte-organized memory designed for use in bus-organized systems. It is fabricated with N-channel silicon-gate technology. For ease of use, the device operates from a single power supply, and has compatibility with TTL. The addresses are latched with the Chip Enable input — no external latches required.

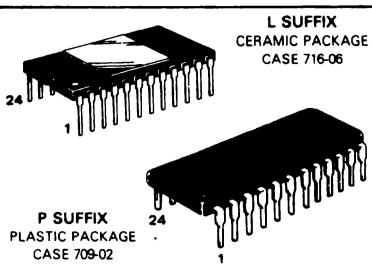
The memory is compatible with the M6800 Microcomputer Family, providing read only storage in byte increments. The Chip Enable input deselects the output and puts the chip in a power-down mode.

- Automatic Power Down
- Low Power Dissipation — 150 mW active (typical)
35 mW standby (typical)
- Single $\pm 10\%$ 5-Volt Power Supply
- High Output Drive Capability (2 TTL Loads)
- Three-State Data Output for OR-Ties
- TTL Compatible
- Maximum Access Time — 250 ns — MCM68B364
350 ns — MCM68A364
- Pin Compatible with 8K — MCM68A308, 16K — MCM68A316E, and 32K — MCM68A332 Mask-Programmable ROMs
- Pin Compatible with 24-pin 64K EPROM MCM68764

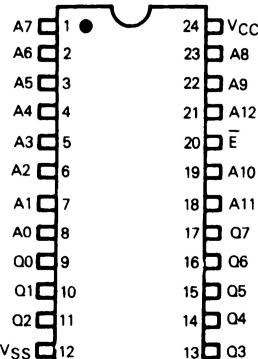
MOS

(IN-CHANNEL, SILICON-GATE)

8192 X 8-BIT READ ONLY MEMORY



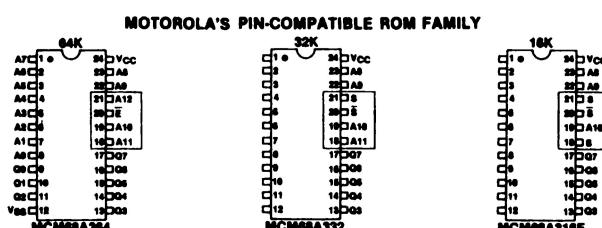
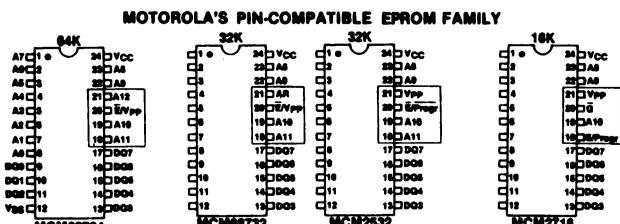
PIN ASSIGNMENT



PIN NAMES

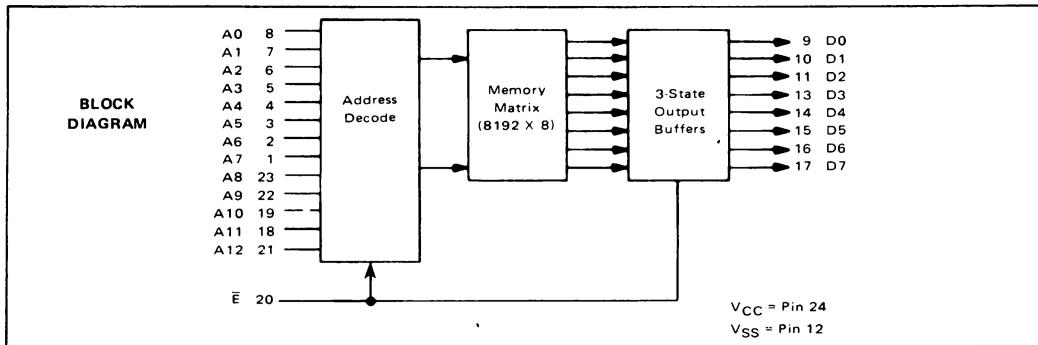
A0 - A12	Address
E	Chip Enable
Q0 - Q7	Data Output
VCC	+ 5 V Power Supply
VSS	Ground

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.



INDUSTRY STANDARD PINOUTS

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ABSOLUTE MAXIMUM RATINGS (See note)

Rating	Symbol	Value	Unit
Supply Voltage	V _{CC}	-0.5 to +7.0	Vdc
Input Voltage	V _{in}	-0.5 to +7.0	Vdc
Operating Temperature Range	T _A	0 to +70	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage (V _{CC} must be applied at least 100 μ s before proper device operation is achieved)	V _{CC}	4.5	5.0	5.5	Vdc
Input High Voltage	V _{IH}	2.0	—	5.5	Vdc
Input Low Voltage	V _{IL}	-0.5	—	0.8	Vdc

RECOMMENDED OPERATING CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Input Current (V _{in} = 0 to 5.5 V)	I _{in}	-10	—	10	μ Adc
Output High Voltage (I _{OH} = -220 μ A)	V _{OH}	2.4	—	—	Vdc
Output Low Voltage (I _{OL} = 3.2 mA)	V _{OL}	—	—	0.4	Vdc
Output Leakage Current (Three-State) (E = 2.0 V, V _{out} = 0 V to 5.5 V)	I _{LO}	-10	—	10	μ Adc
Supply Current — Active* (Minimum Cycle Rate)	I _{CC}	—	25	40	mAdc
Supply Current — Standby (E = V _{IH})	I _{SB}	—	7	10	mAdc

*Current is proportional to cycle rate.

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested)

Characteristic	Symbol	Max	Unit
Input Capacitance	C _{in}	8	pF
Output Capacitance	C _{out}	15	pF

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AC OPERATING CONDITIONS AND CHARACTERISTICS

Read Cycle

RECOMMENDED OPERATING CONDITIONS

($T_A = 0$ to 70°C , $V_{CC} = 5.0 \text{ V} \pm 10\%$. All timing with $t_r = t_f = 20 \text{ ns}$, load of Figure 1)

Parameter	Symbol	MCM68B364		MCM68A364		Unit
		Min	Max	Min	Max	
Chip Enable Low to Chip Enable Low of Next Cycle (Cycle Time)	t_{EEL}	375	—	450	—	ns
Chip Enable Low to Chip Enable High	t_{ELEH}	250	—	300	—	ns
Chip Enable Low to Output Valid (Access)	t_{ELQV}	—	250	—	300	ns
Chip Enable High to Output High Z (Off Time)	t_{EHQZ}	—	60	—	75	ns
Chip Enable Low to Address Don't Care (Hold)	t_{ELAX}	60	—	75	—	ns
Address Valid to Chip Enable Low (Address Setup)	t_{AVEL}	0	—	0	—	ns
Chip Enable Precharge Time	t_{EHEL}	125	—	150	—	ns

TIMING DIAGRAM

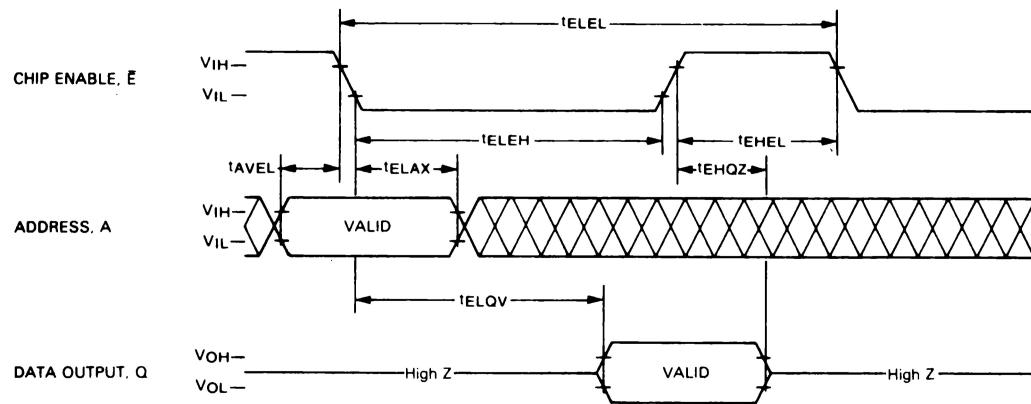
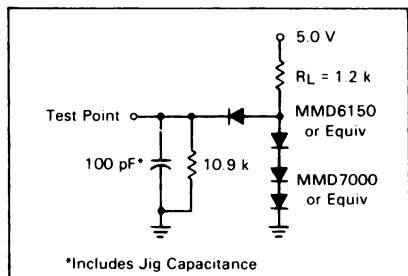


FIGURE 1 – AC TEST LOAD

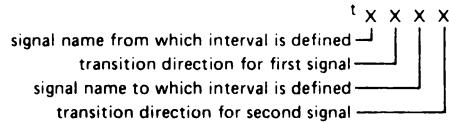


WAVEFORMS

Waveform Symbol	Input	Output
—	MUST BE VALID	WILL BE VALID
/\ / \ / \ /	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
/ \ / \ / \ /	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
XXXXXX	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
—		HIGH IMPEDANCE

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TIMING PARAMETER ABBREVIATIONS



The transition definitions used in this data sheet are:

- H = transition to high
- L = transition to low
- V = transition to valid
- X = transition to invalid or don't care
- Z = transition to off (high impedance)

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

CUSTOM PROGRAMMING

By the programming of a single photomask for the MCM68A364/MCM68B364, the customer may specify the contents of the memory.

Information for custom memory content may be sent to Motorola in one of two forms (shown in order of preference):

1. Magnetic Tape — 9 Track, 800 bpi, odd parity written in EBCDIC character code. Motorola's R.O.M.S. format.
2. EPROMs — one 64K (MCM68764), two 32K (MCM2532), four 16K (MCM2716 or TMS2716), or eight 8K (MCM2708).
3. IBM Punch Cards
 - A. Hexadecimal Format
 - B. INTEL Hexadecimal Format

IBM PUNCH CARDS, HEXADECIMAL FORMAT

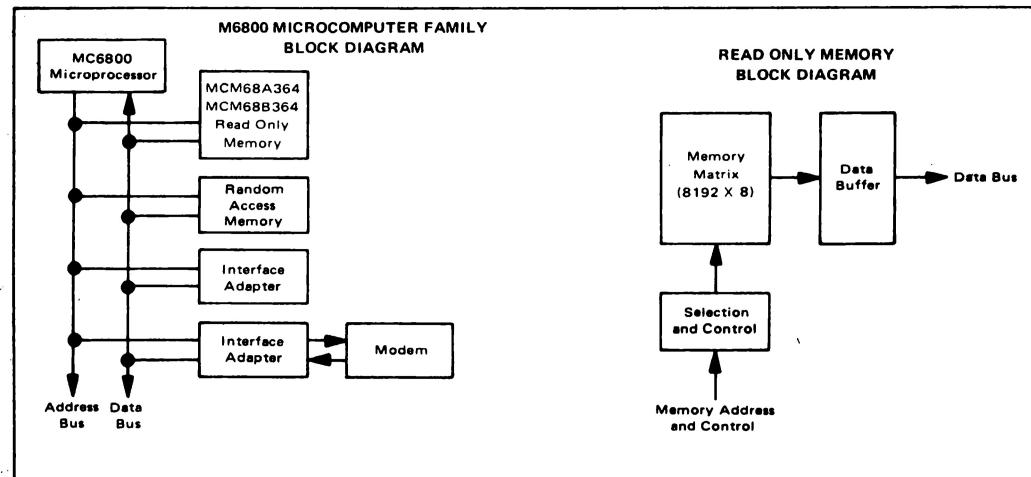
The hexadecimal equivalent (from Figure 2) may be placed on 80 column IBM punch cards as follows:

Step	Column	
1	12	Byte "0" Hexadecimal equivalent for outputs Q7 through Q4 (Q7=M.S.B.)
2	13	Byte "0" Hexadecimal equivalent for outputs Q3 through Q0 (Q3=M.S.B.)
3	14-75	Alternate steps 1 and 2 for consecutive bytes
4	77-79	Card number (starting 001) Total number of cards must equal 256

FIGURE 2 – BINARY TO HEXADECIMAL CONVERSION

Binary Data				Hexadecimal Character
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	A
1	0	1	1	B
1	1	0	0	C
1	1	0	1	D
1	1	1	0	E
1	1	1	1	F

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PRE-PROGRAMMED MCM68A364P3/L3

The -3 standard ROM pattern contains log (base 10) and antilog (base 10) lookup tables for the 64K ROM.

Locations 0000 through 3599 contain log base 10 values. The arguments for the log table range from 1.00 through 9.99 incrementing in steps of 1/100. Each log value is represented by an eight-digit decimal number with decimal point assumed to be to the left of the most-significant digit.

Antilog (base 10) are stored in locations 4096 through 8095. The arguments range from .000 through .999 incrementing in steps of 1/1000. Each antilog value is

represented by an eight-digit decimal number with decimal point assumed to be to the right of the most-significant digit.

Locations 3600 through 4095 and 8096 through 8191 are zero filled.

All values are represented in absolute decimal format with eight digit precision. They are stored in BCD format with the two most significant digits in the lower byte and the remaining six digits in the three consecutive locations.

Example:
 $\log_{10}(1.01) = .00432137$ decimal

Address	Contents
4	0000 0000
5	0100 0011
6	0010 0001
7	0011 0111