

Fig. 1-1. Diagram of the Apple II RFI mother board. (Courtesy Apple Computer Inc.)

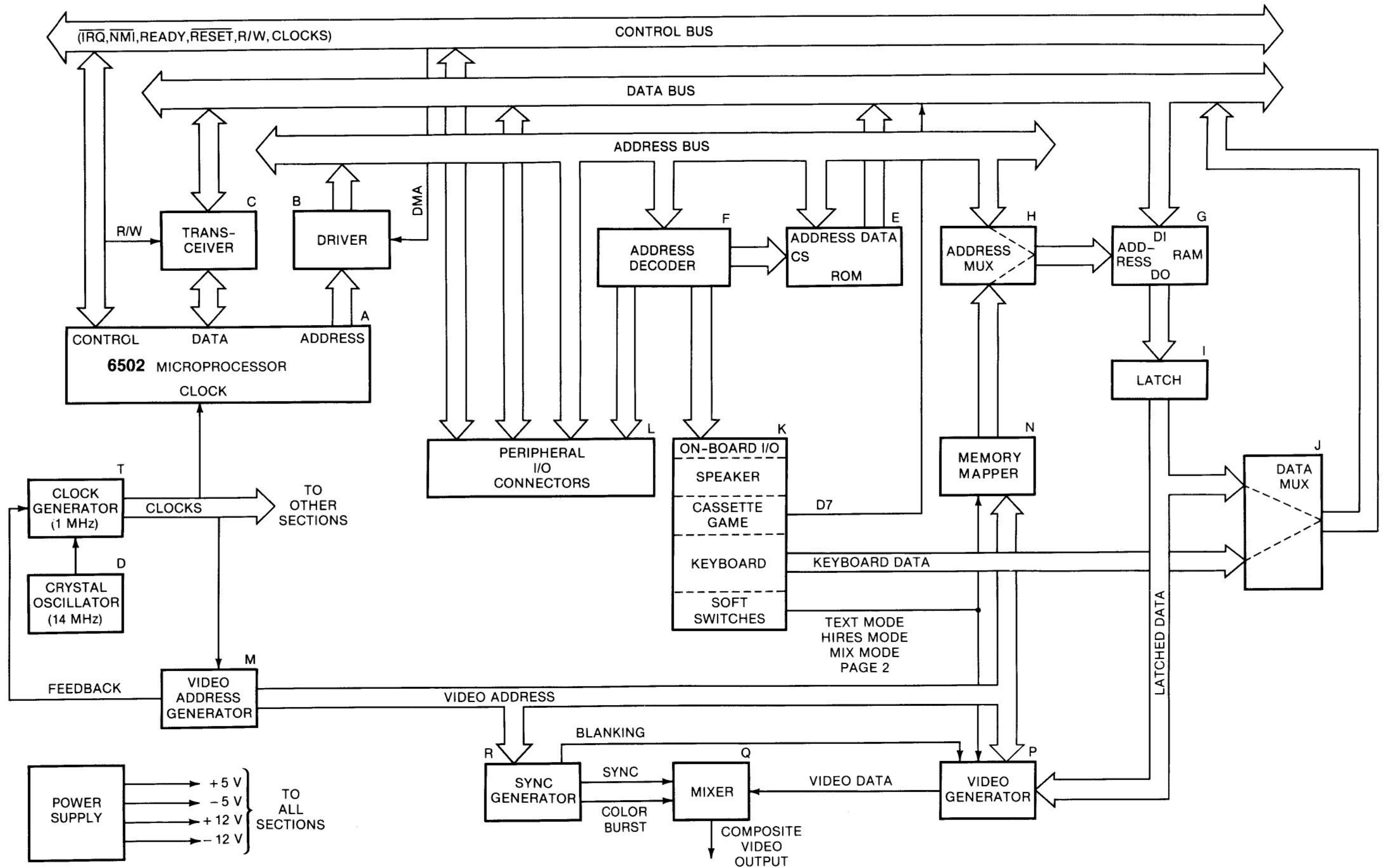


Fig. 2-1. Apple II block diagram.

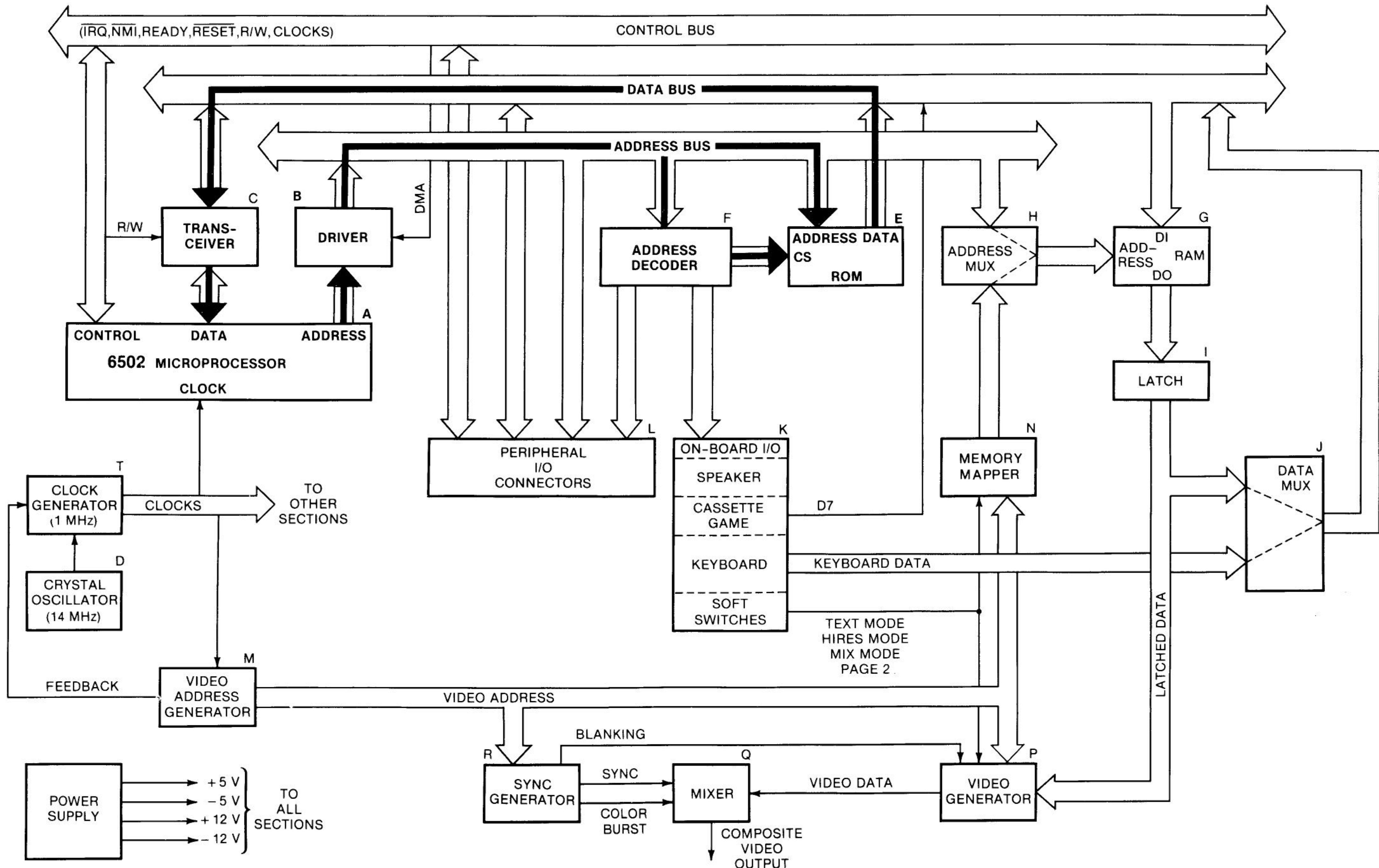


Fig. 2-2. ROM read-cycle path.

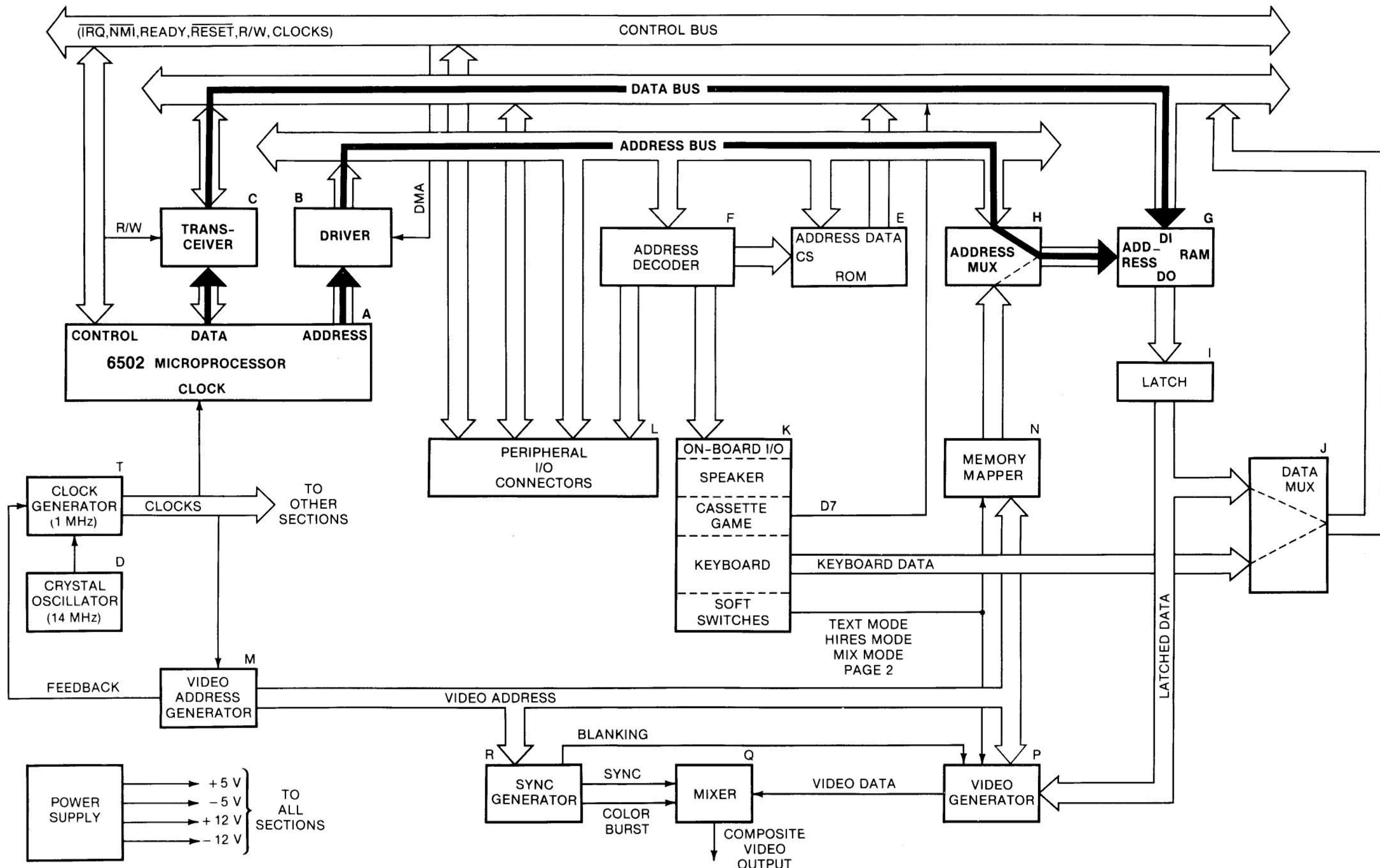


Fig. 2-3. RAM write-cycle path.

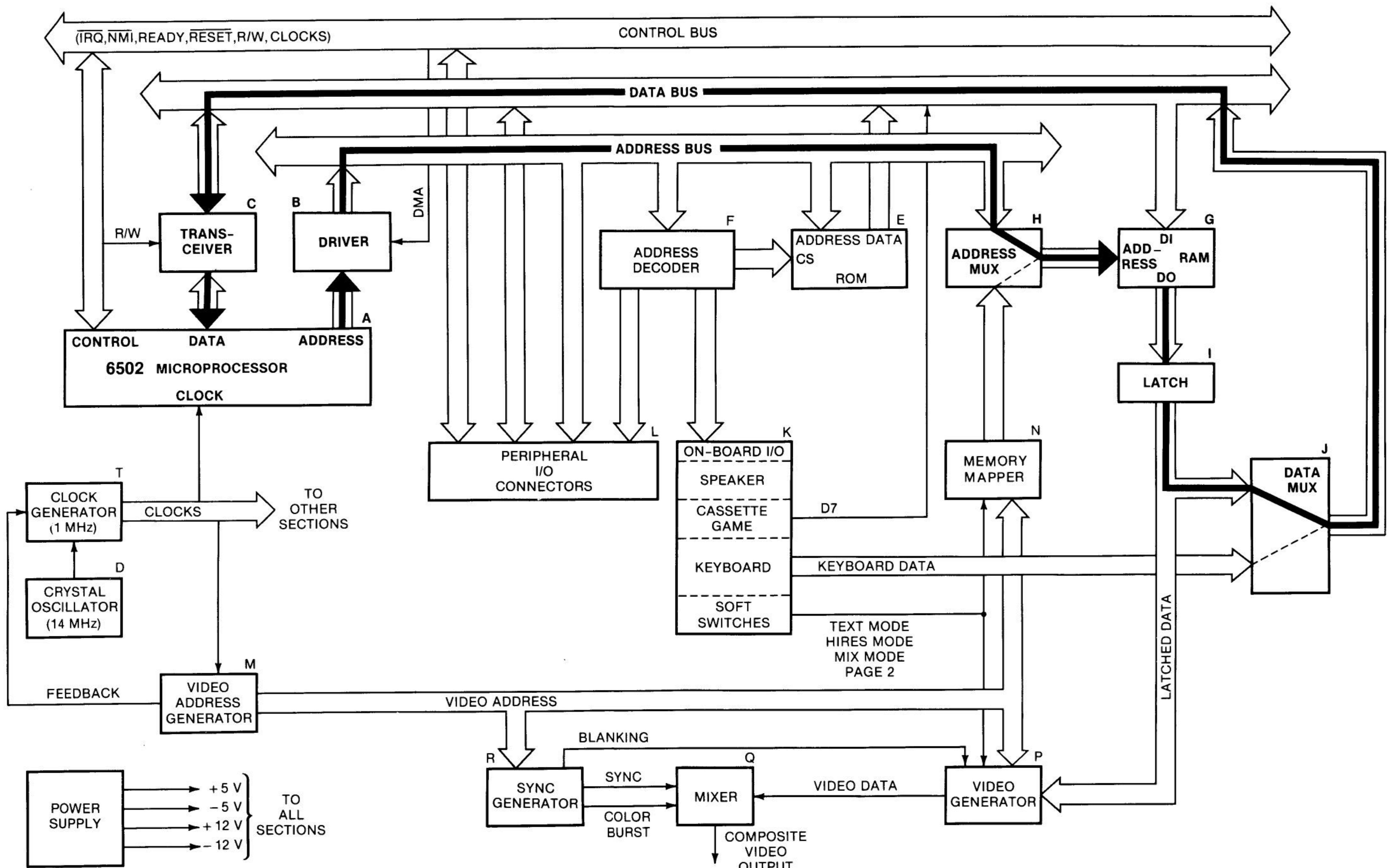


Fig. 2-4. RAM read-cycle path.

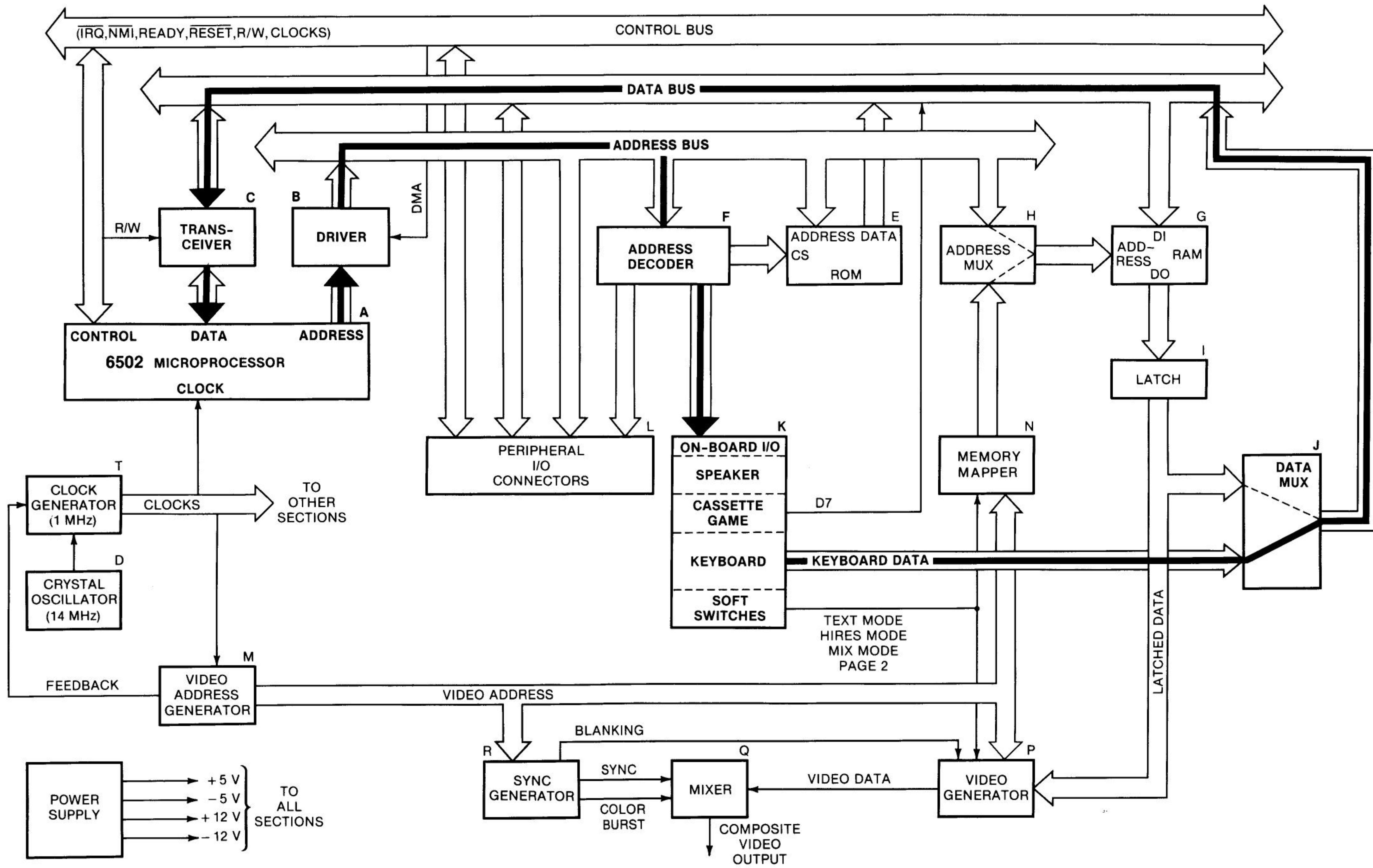


Fig. 2-5. Keyboard read-cycle path.

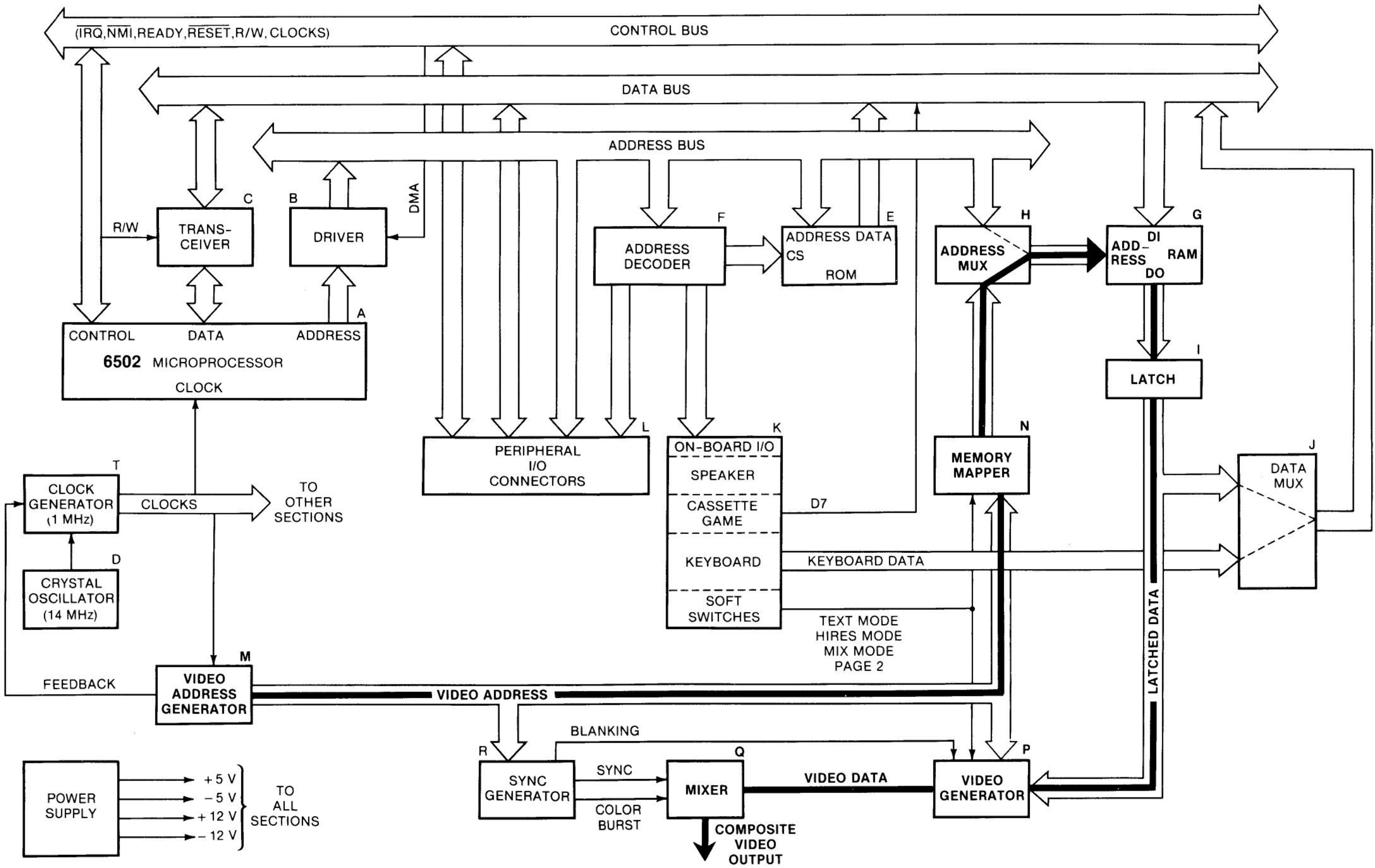


Fig. 2-6. Video-cycle path.

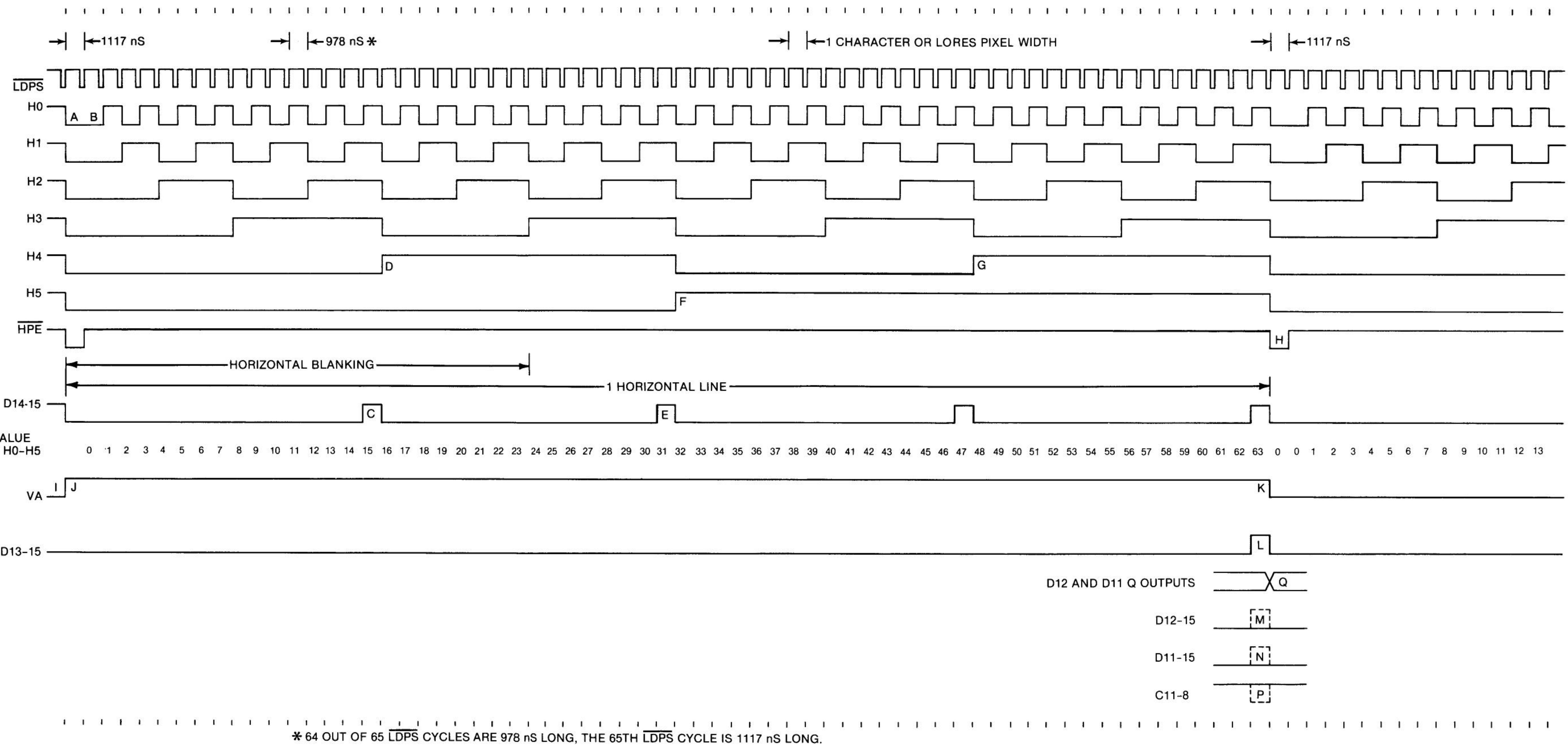


Fig. 3-4. Horizontal timing.

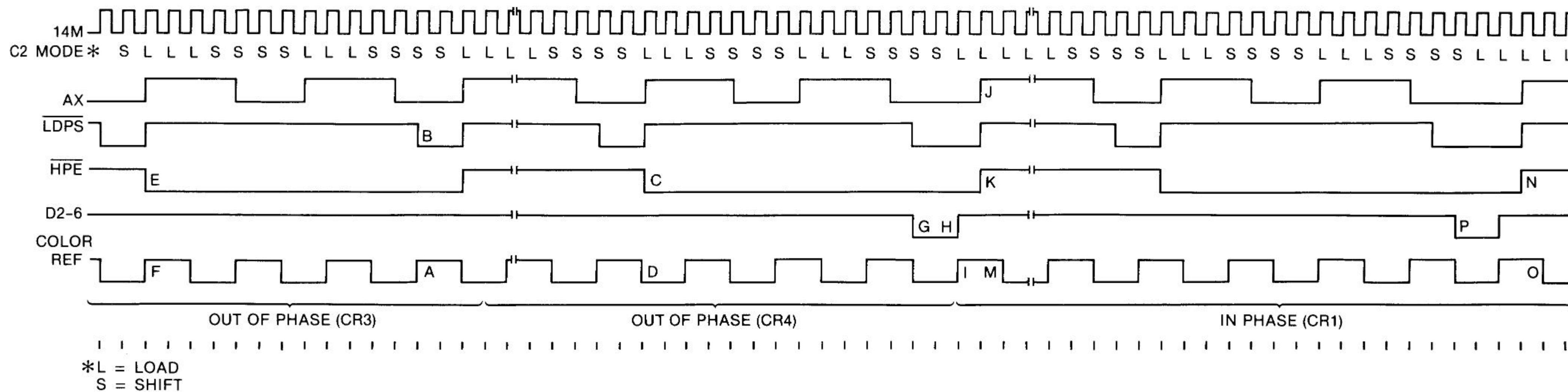


Fig. 3-7. Clock synchronization—CR3 and CR4.

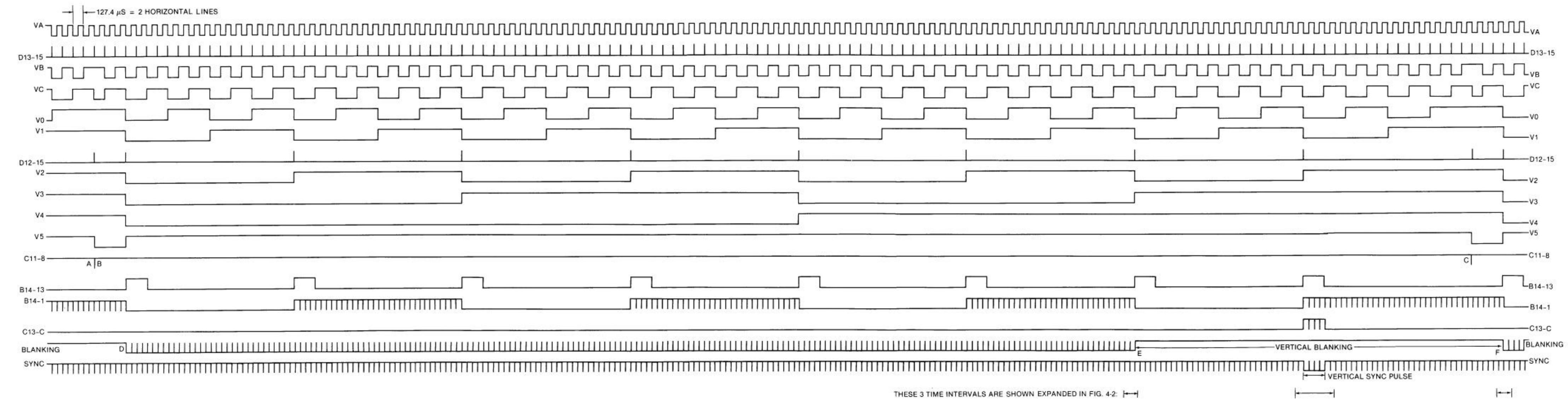


Fig. 4-1. Vertical timing.

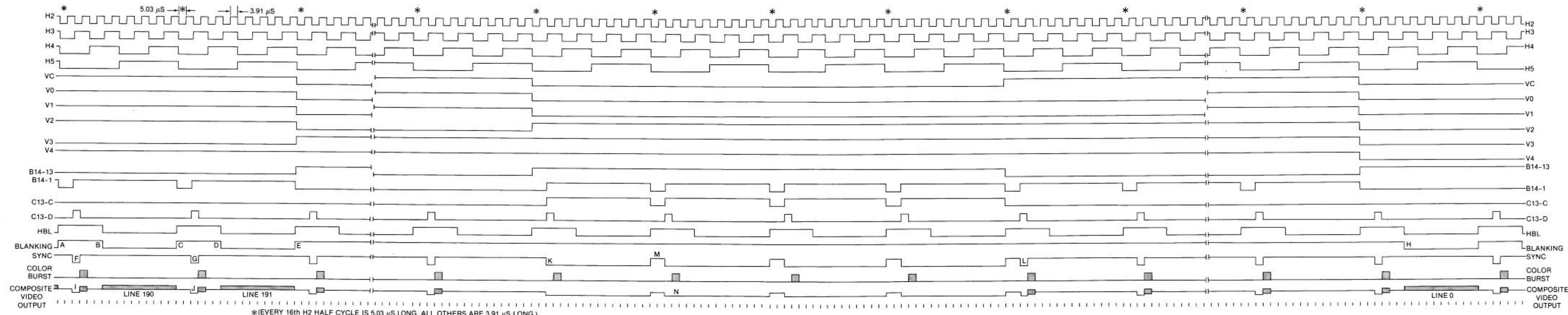


Fig. 4-2. Vertical retrace interval.

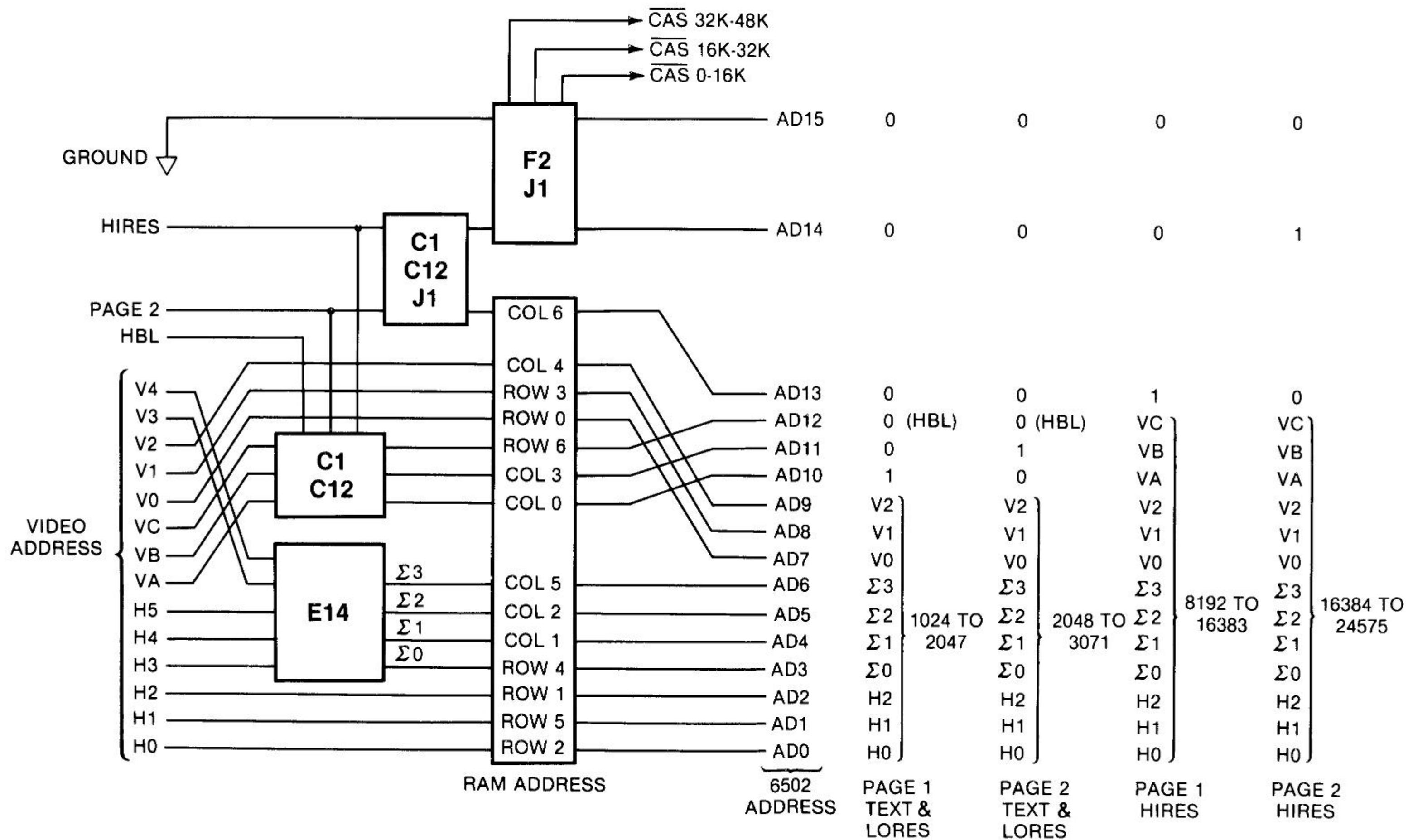
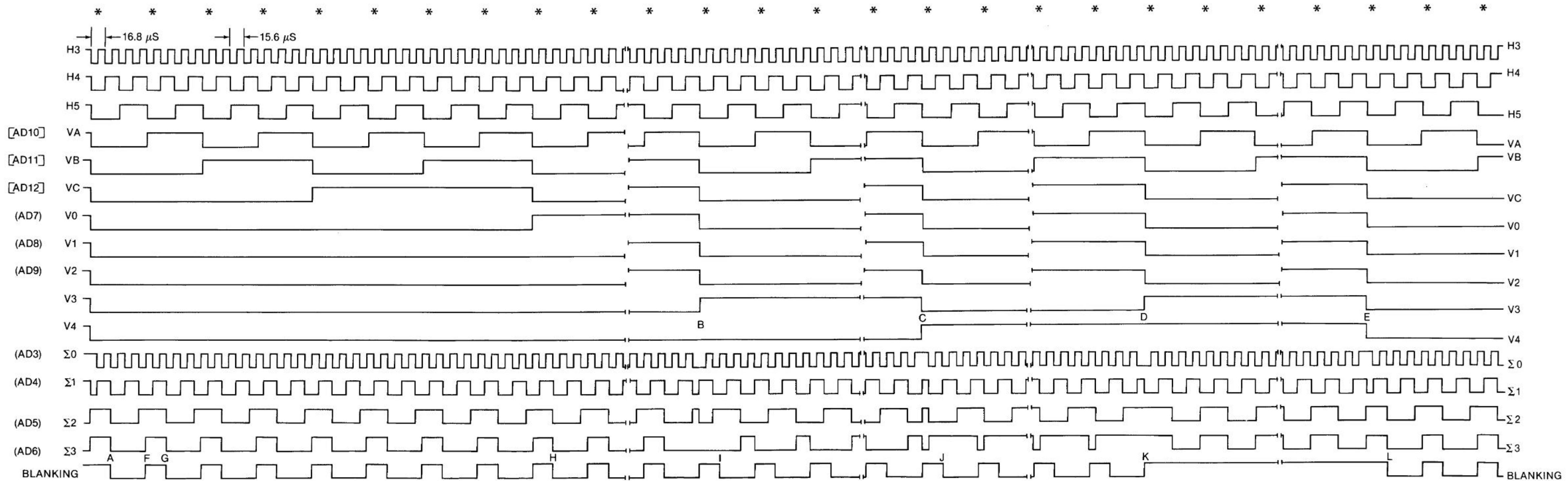


Fig. 5-7. Video mapping.



PAGE 1 TEXT  
DECIMAL ADDRESS

PAGE 1 HIRES  
DECIMAL ADDRESS

\*EVERY FOURTH H3...PERIOD IS 16.8  $\mu$ S LONG. ALL OTHERS ARE 15.6  $\mu$ S LONG.

Fig. 5-8. Video address signals.

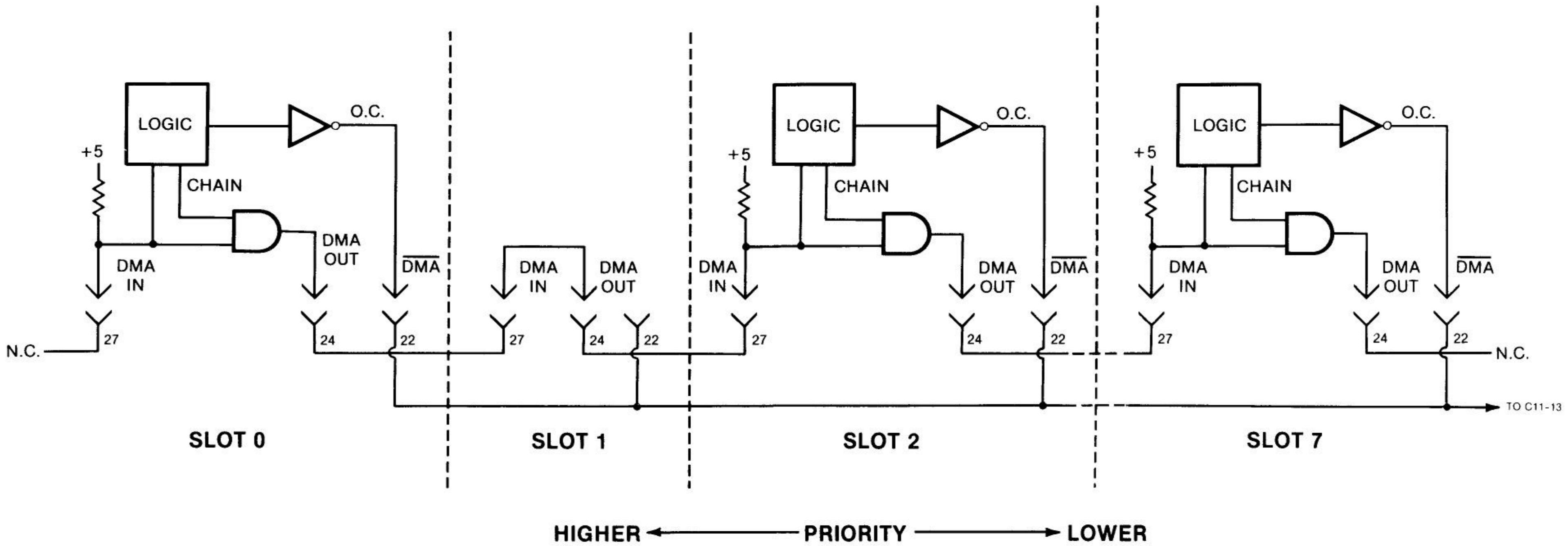


Fig. 6-11. DMA daisy chain.

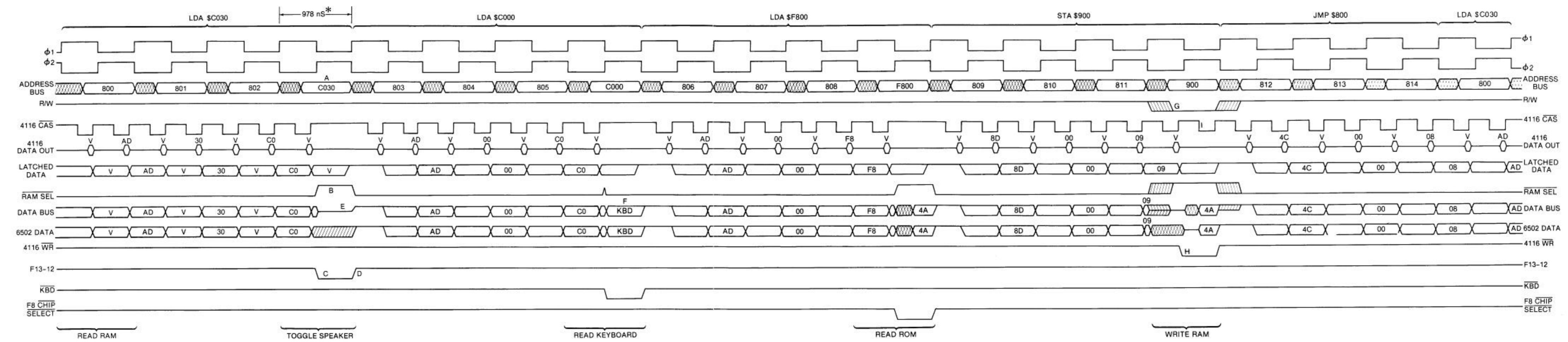
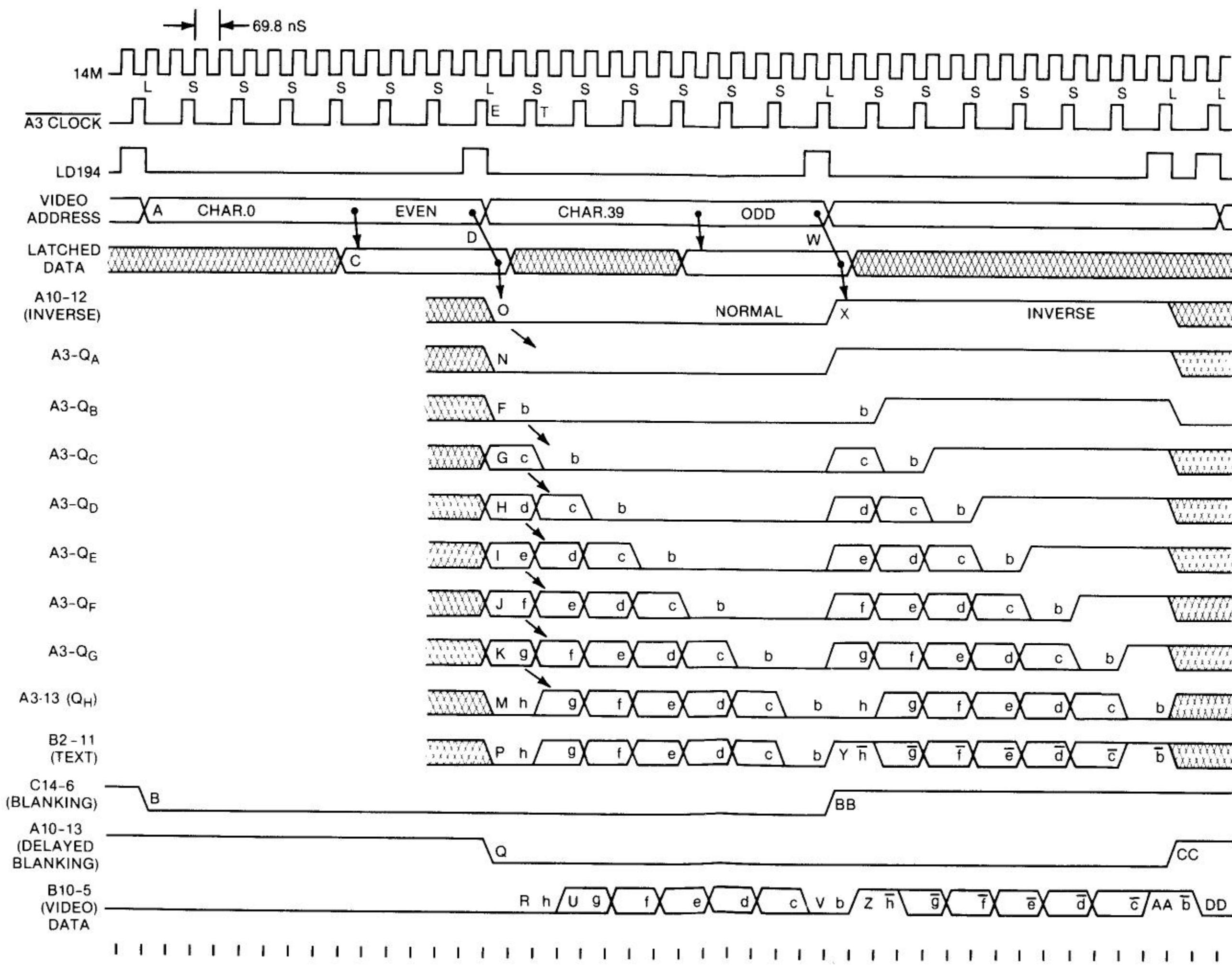


Fig. 6-16. 6502 scope loop.



**Fig. 8-26.** Text mode timing diagram.

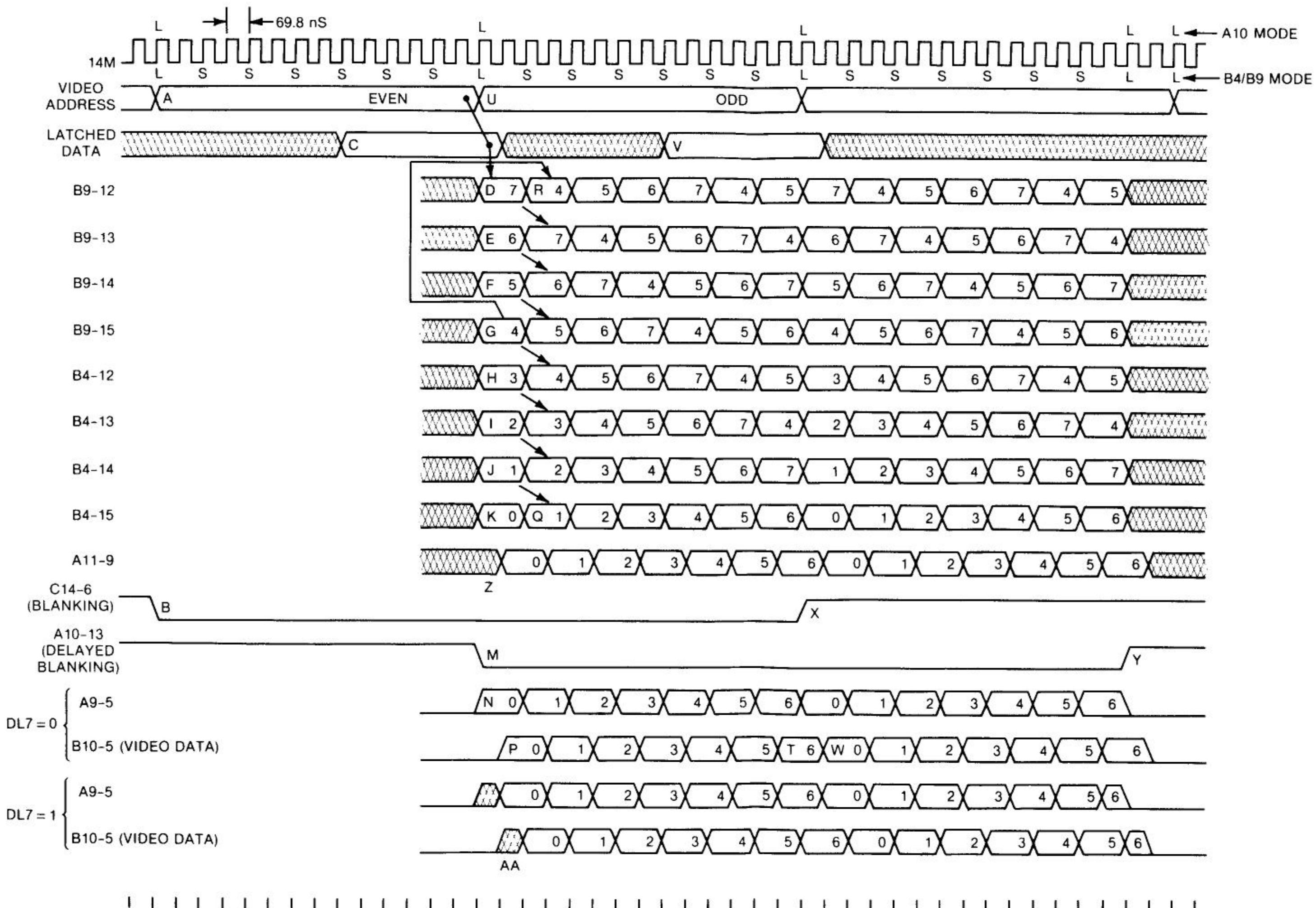


Fig. 8-28. HIRES-mode timing diagram.

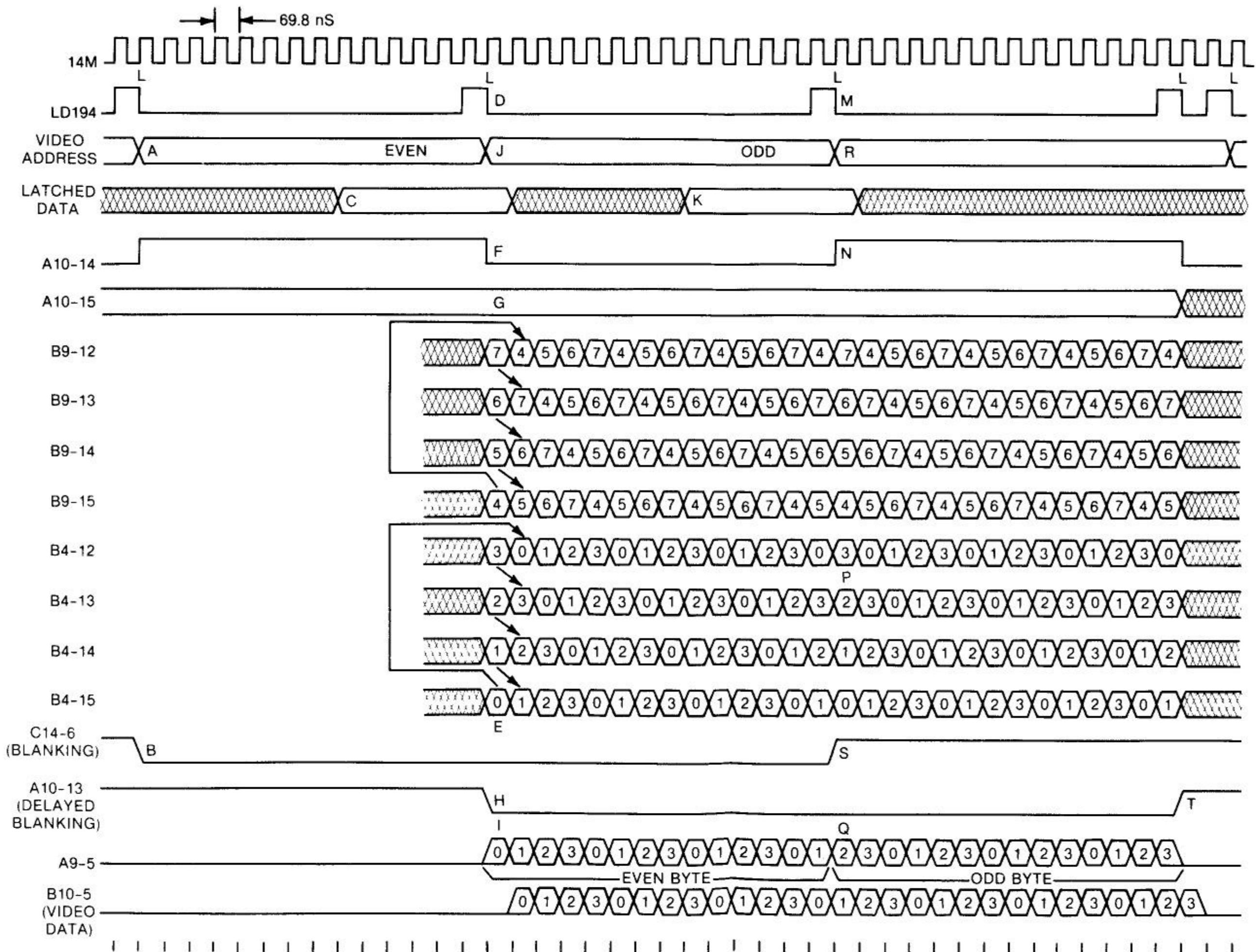
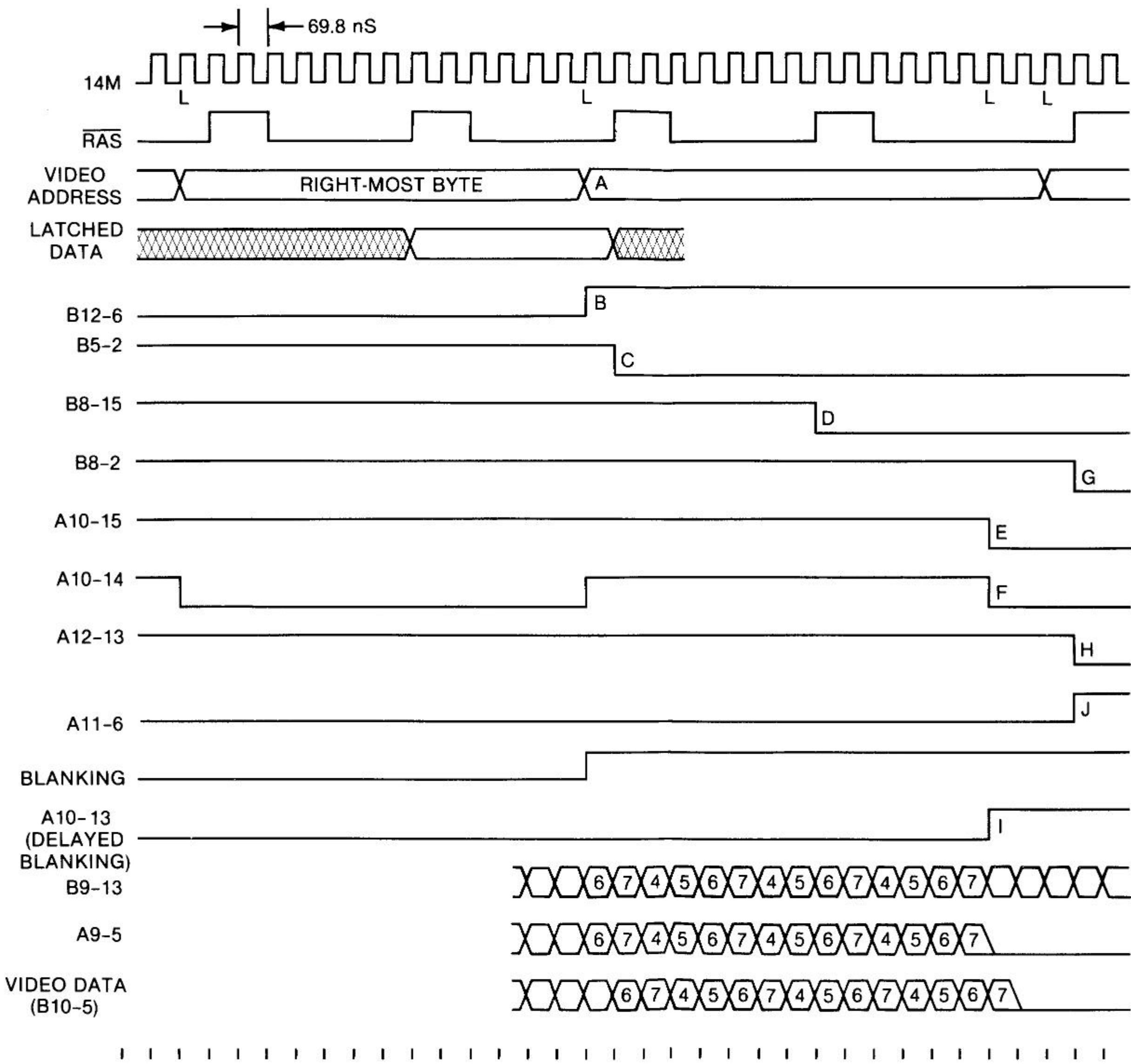
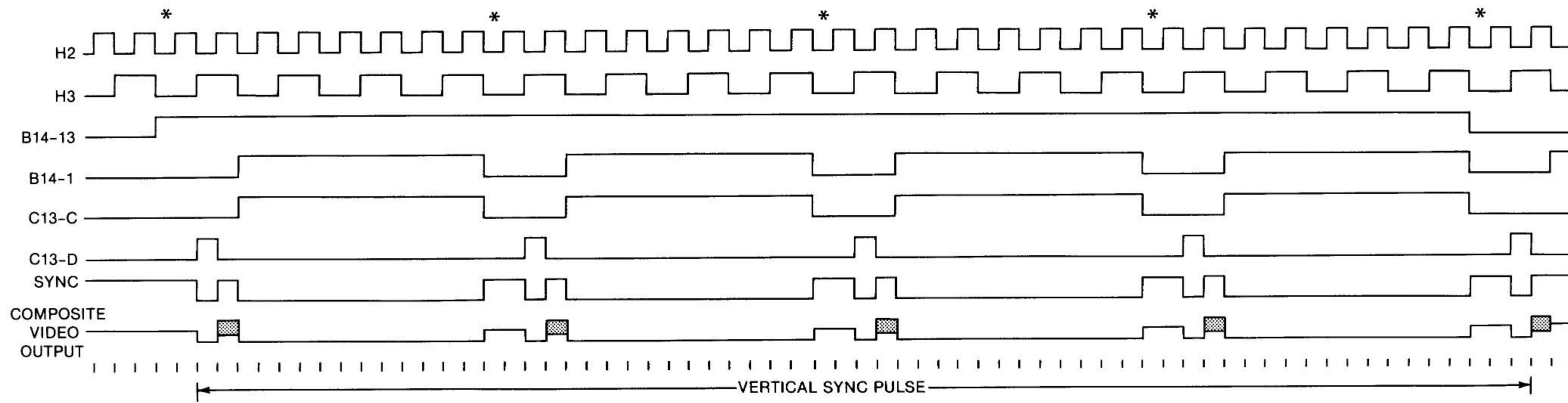


Fig. 8-31. LORES-mode timing diagram.

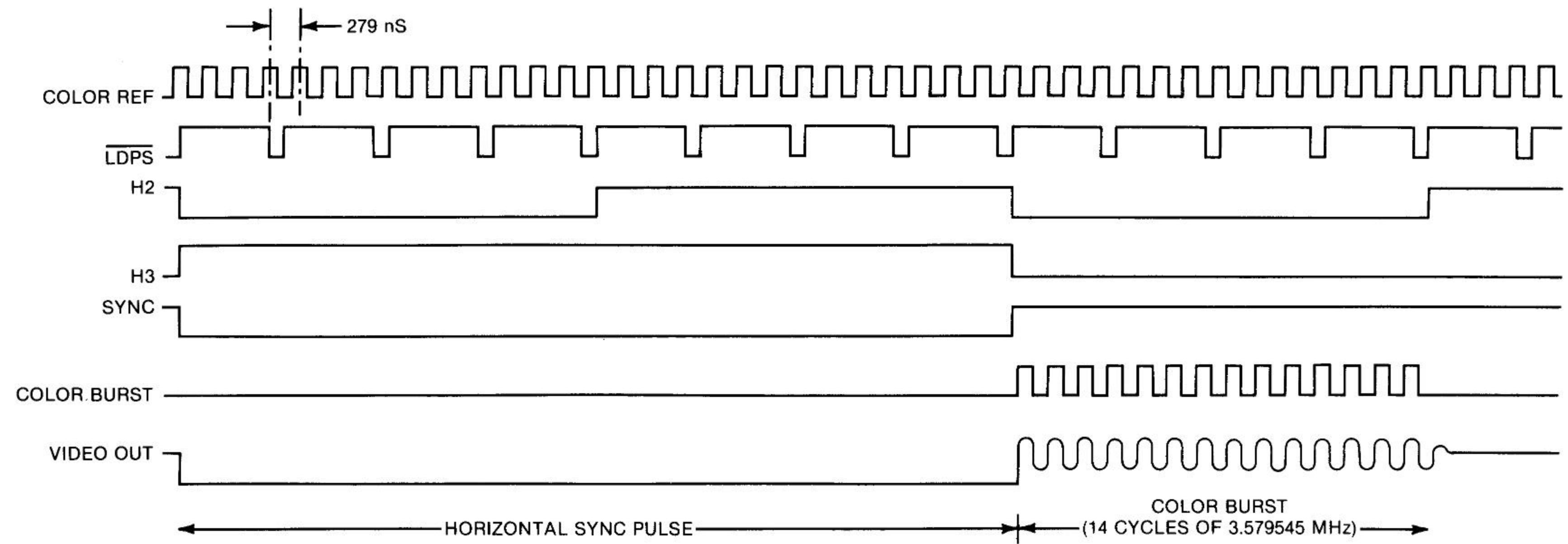


**Fig. 8-34.** Mixed LORES and text.

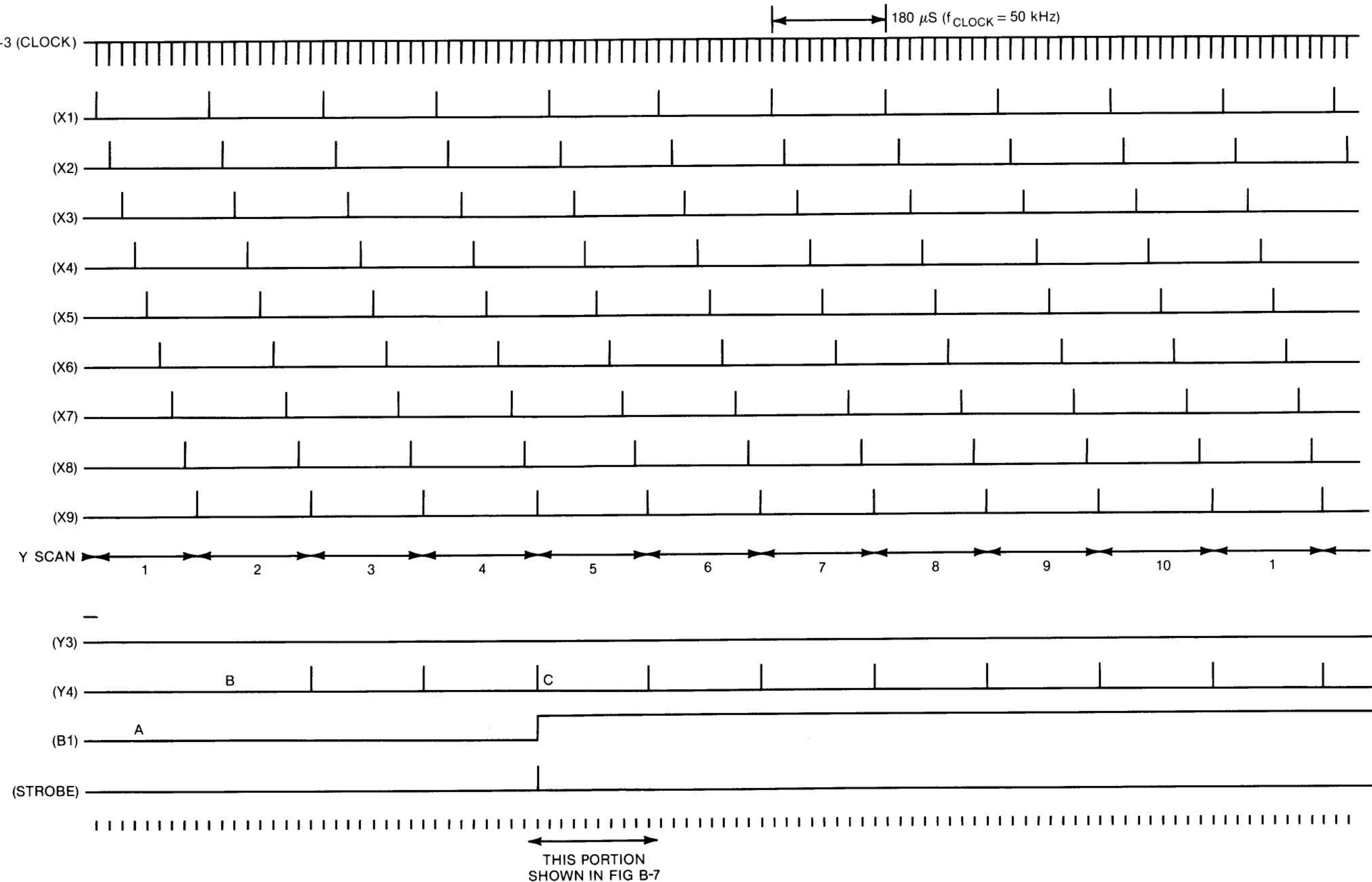


\*EVERY 16th H<sub>2</sub> HALF CYCLE IS 5.03  $\mu$ S LONG. ALL OTHERS  
ARE 3.91  $\mu$ S LONG.

Fig. B-2. Vertical sync—Rev. 7.



**Fig. B-4.** Color burst—Rev. 0 and 1.



**Fig. B-8.** Y scan—single-piece keyboard.

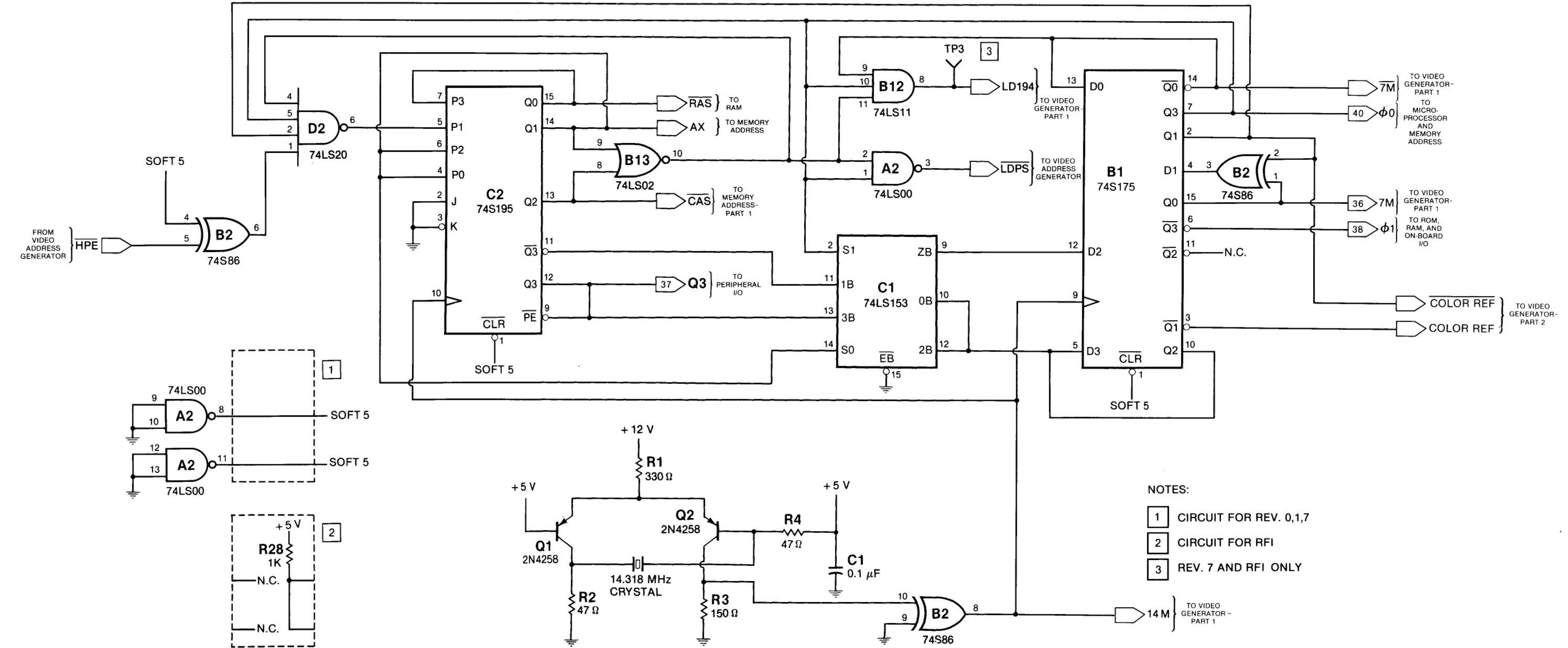


Fig. C-2. Clock generator (all revisions).

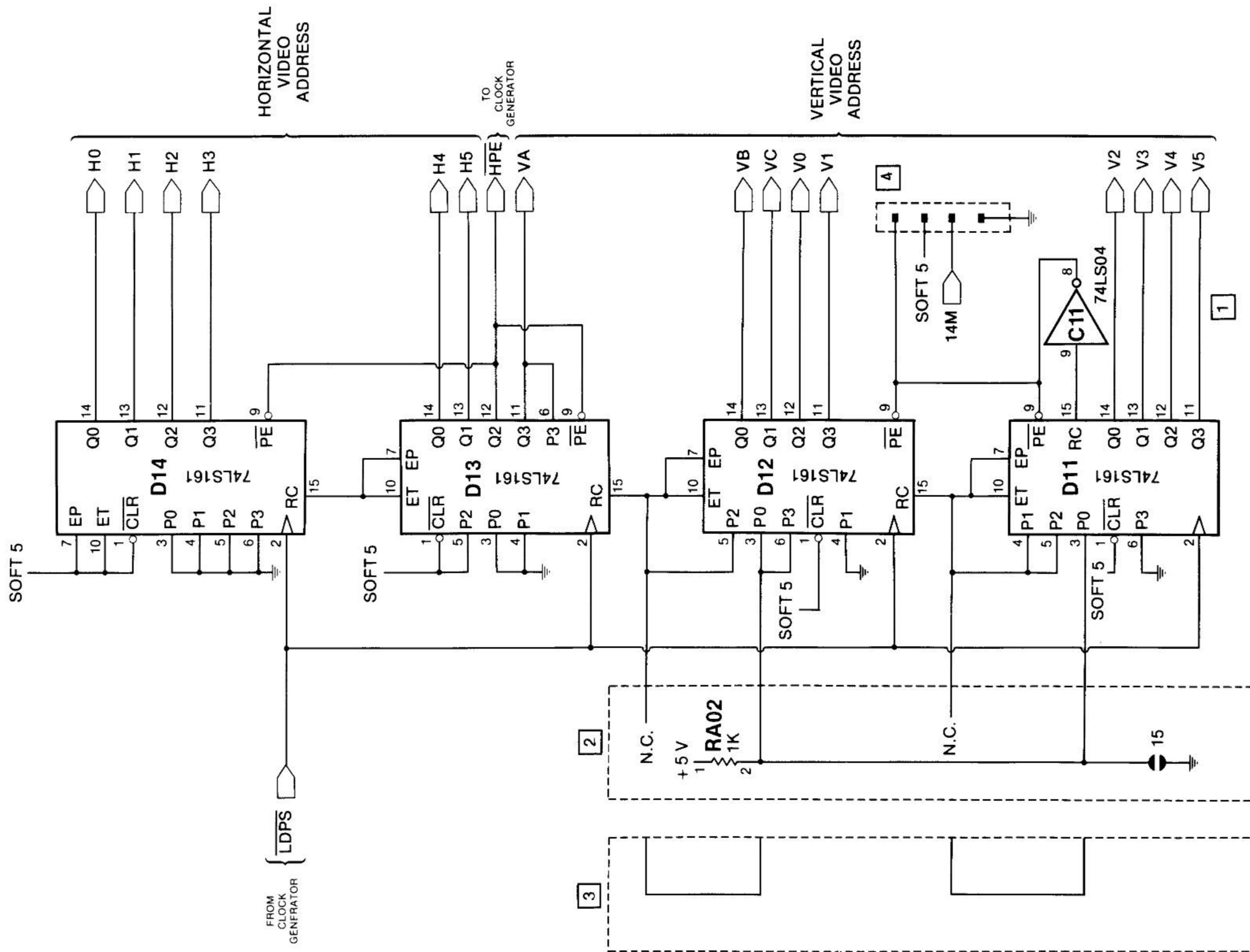


Fig. C-3. Video address generator (all revisions).

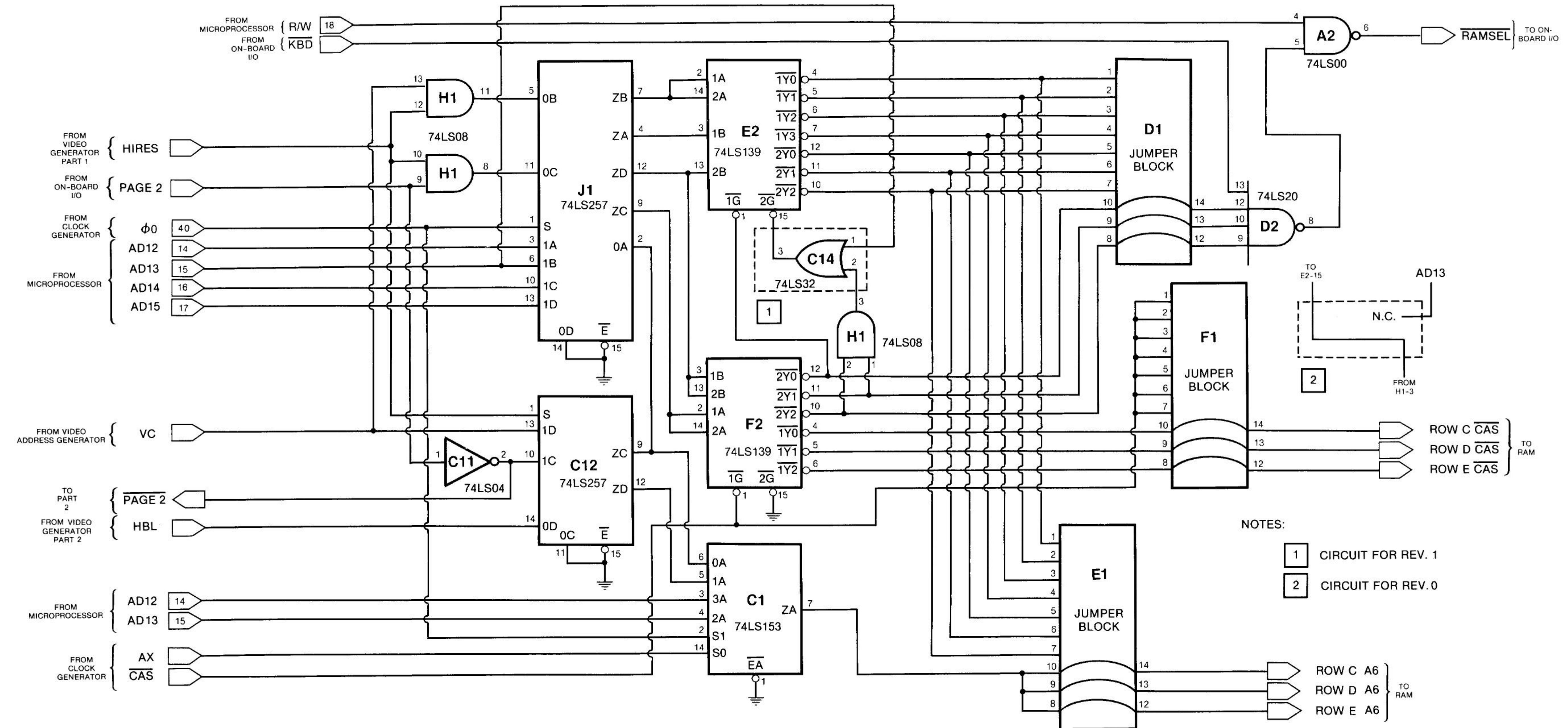


Fig. C-4. Memory address—part 1 (Rev. 0,1).

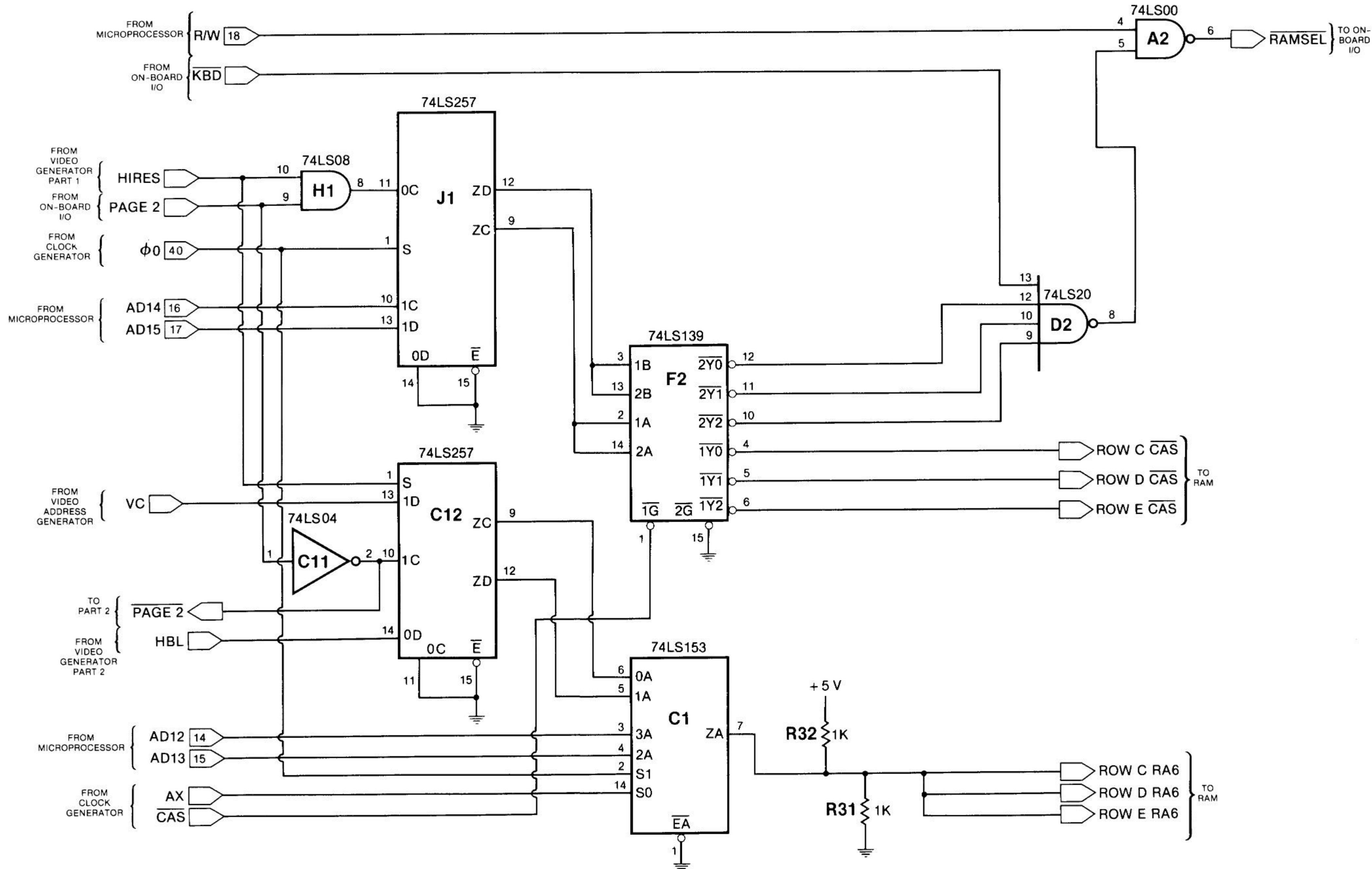


Fig. C-5. Memory address—part 1 (Rev. 7, RFI).

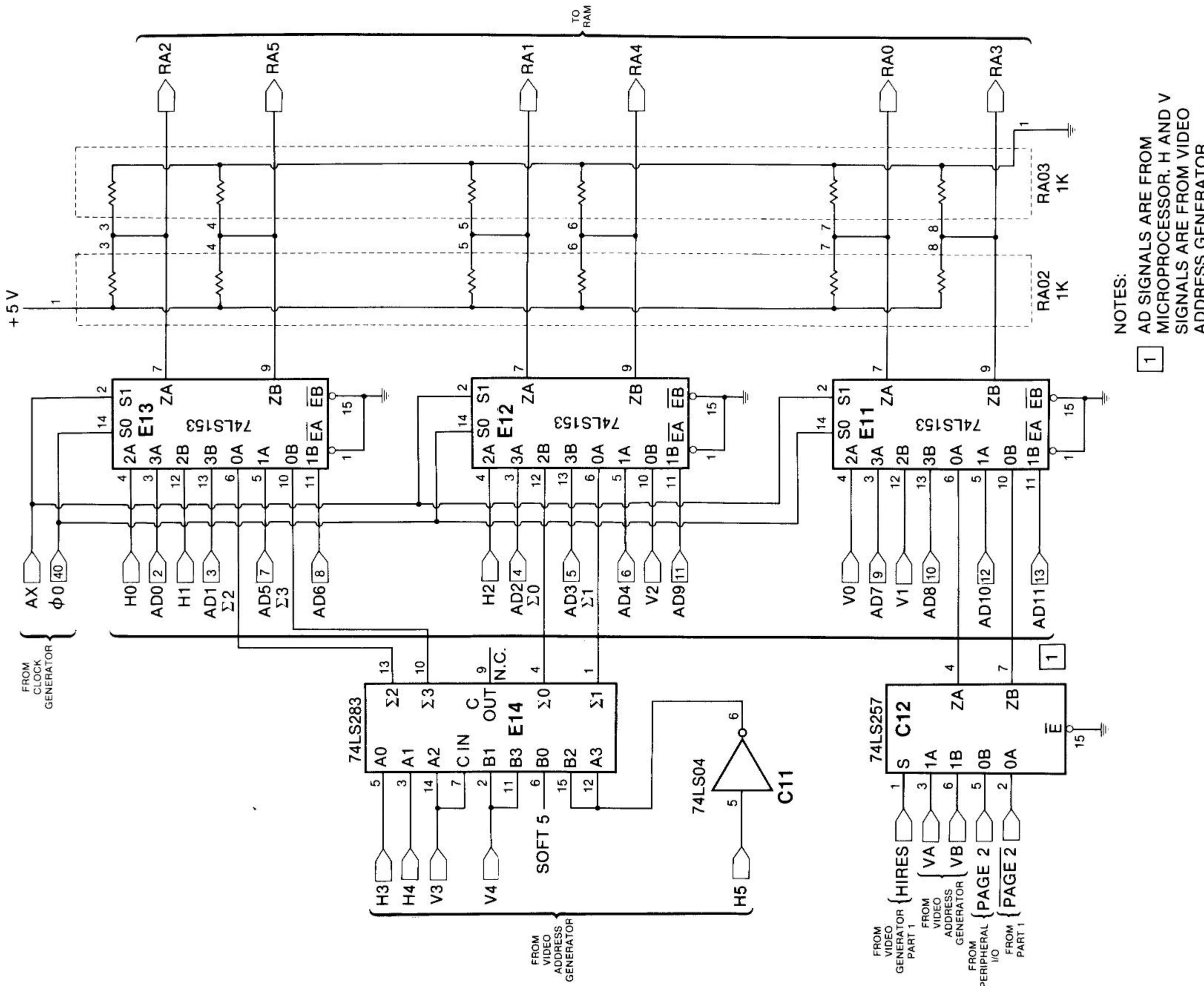


Fig. C-6. Memory address—part 2 (all revisions).

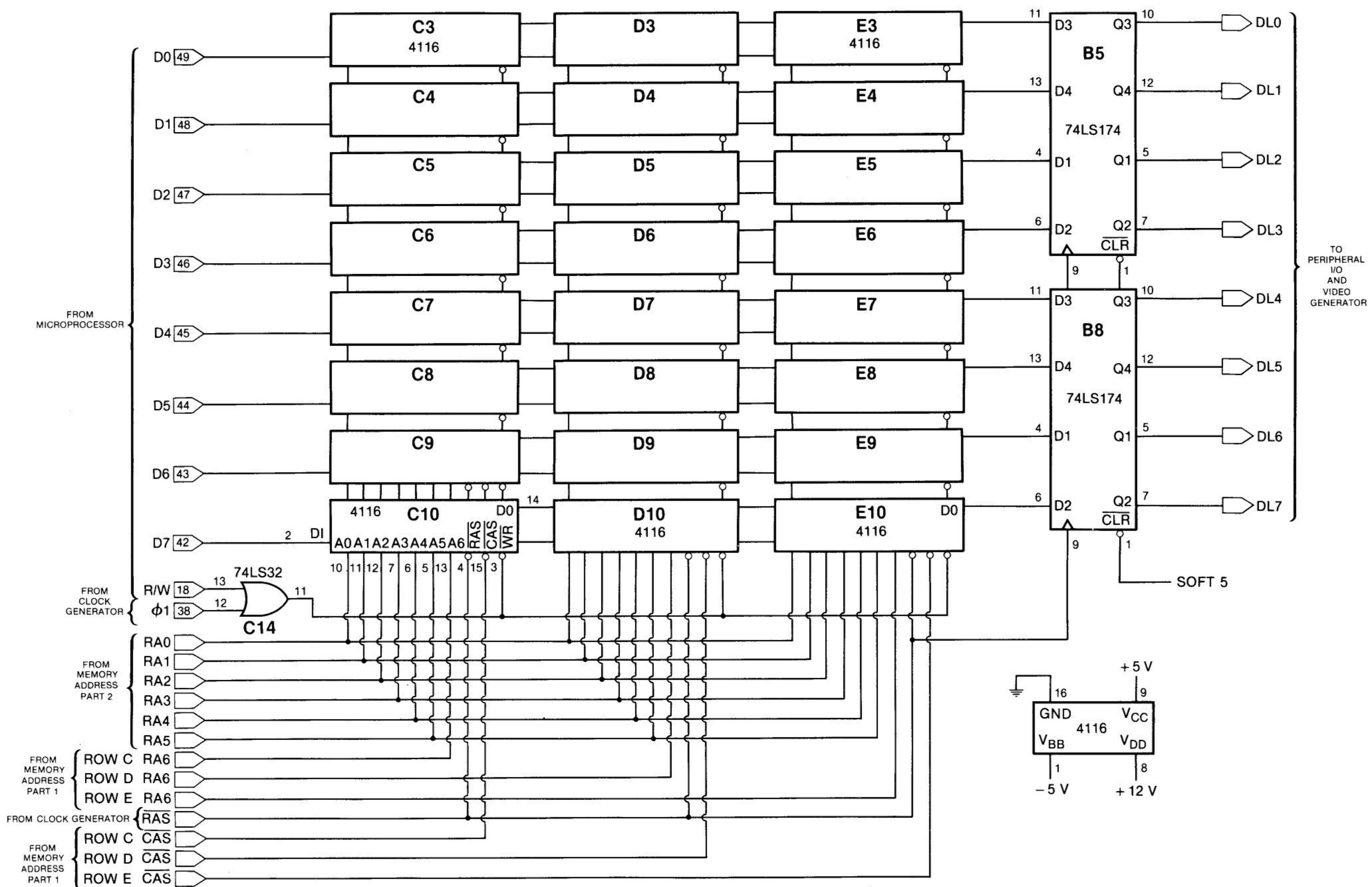
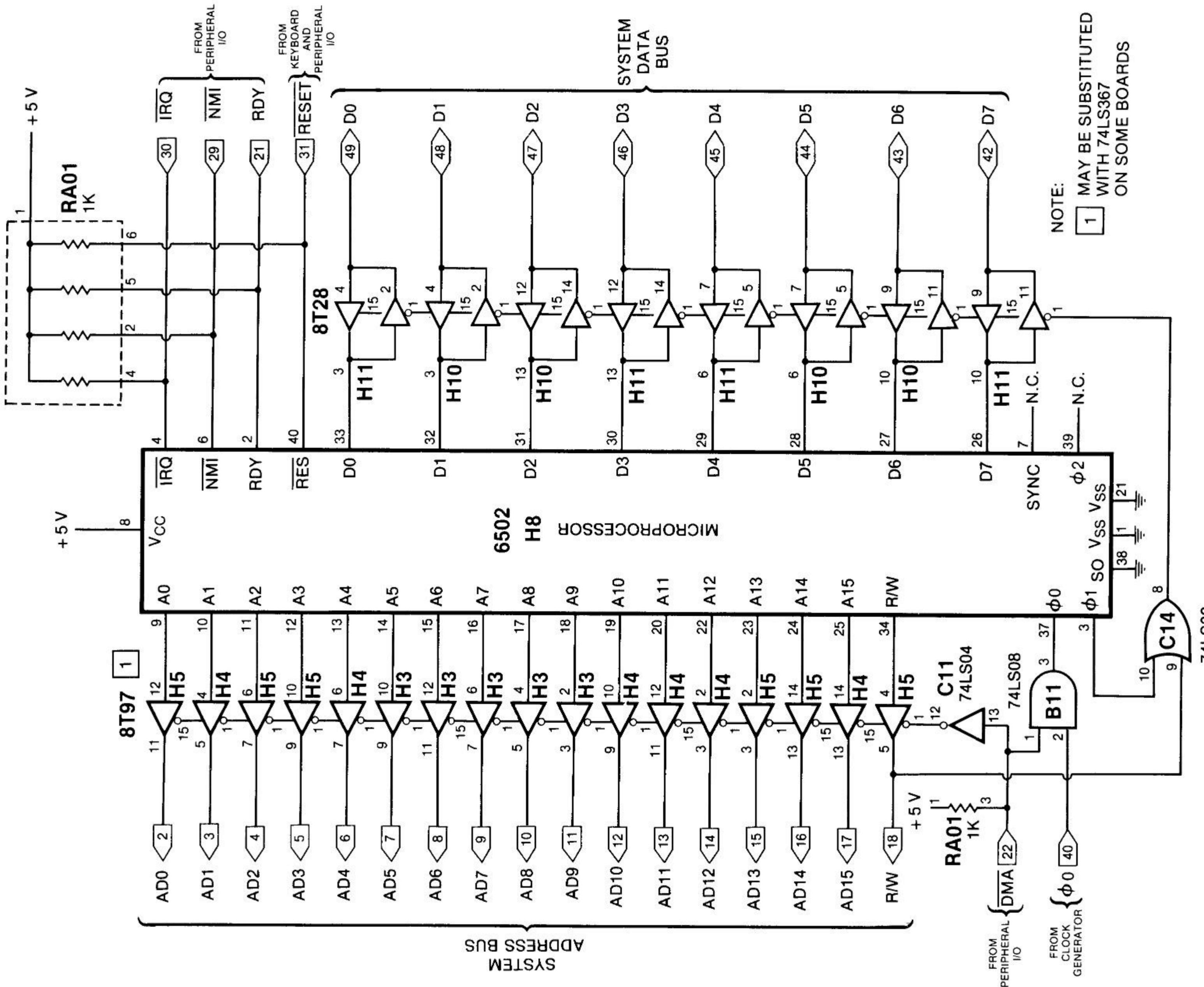
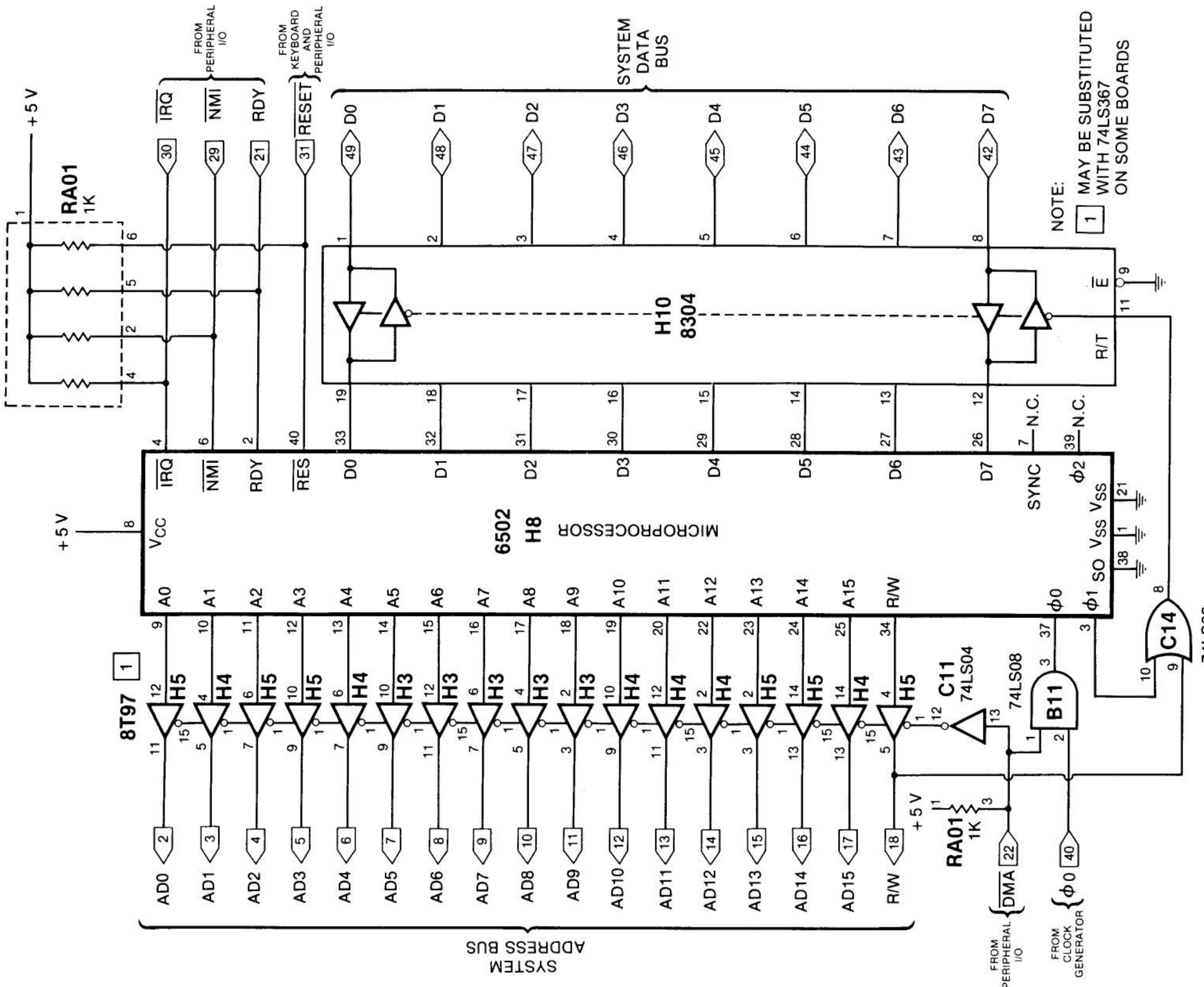


Fig. C-7. RAM (all revisions).



**Fig. C-8.** Microprocessor (Rev. 0,1,7).



**Fig. C-9.** Microprocessor (RFI).

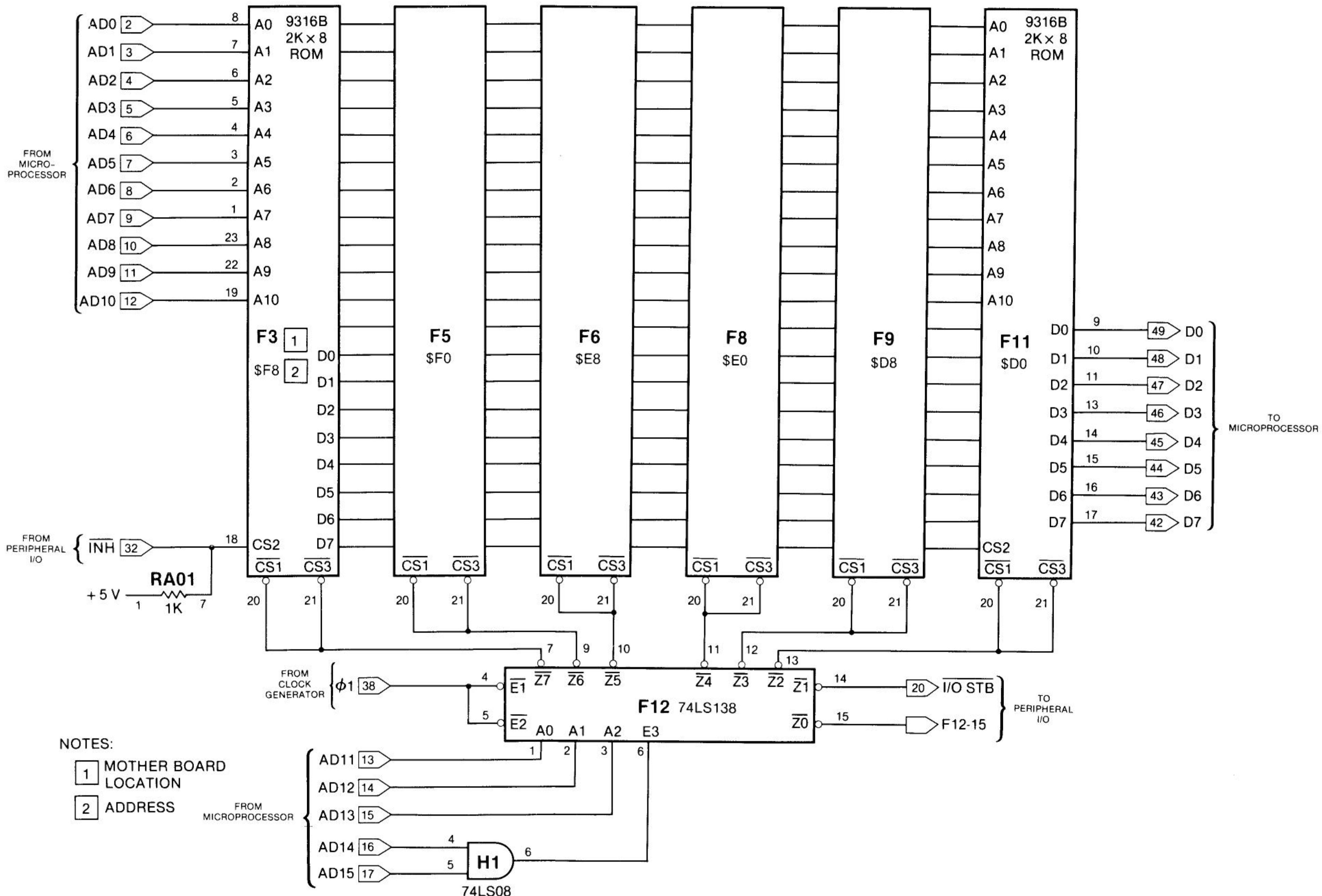


Fig. C-10. ROM (all revisions).

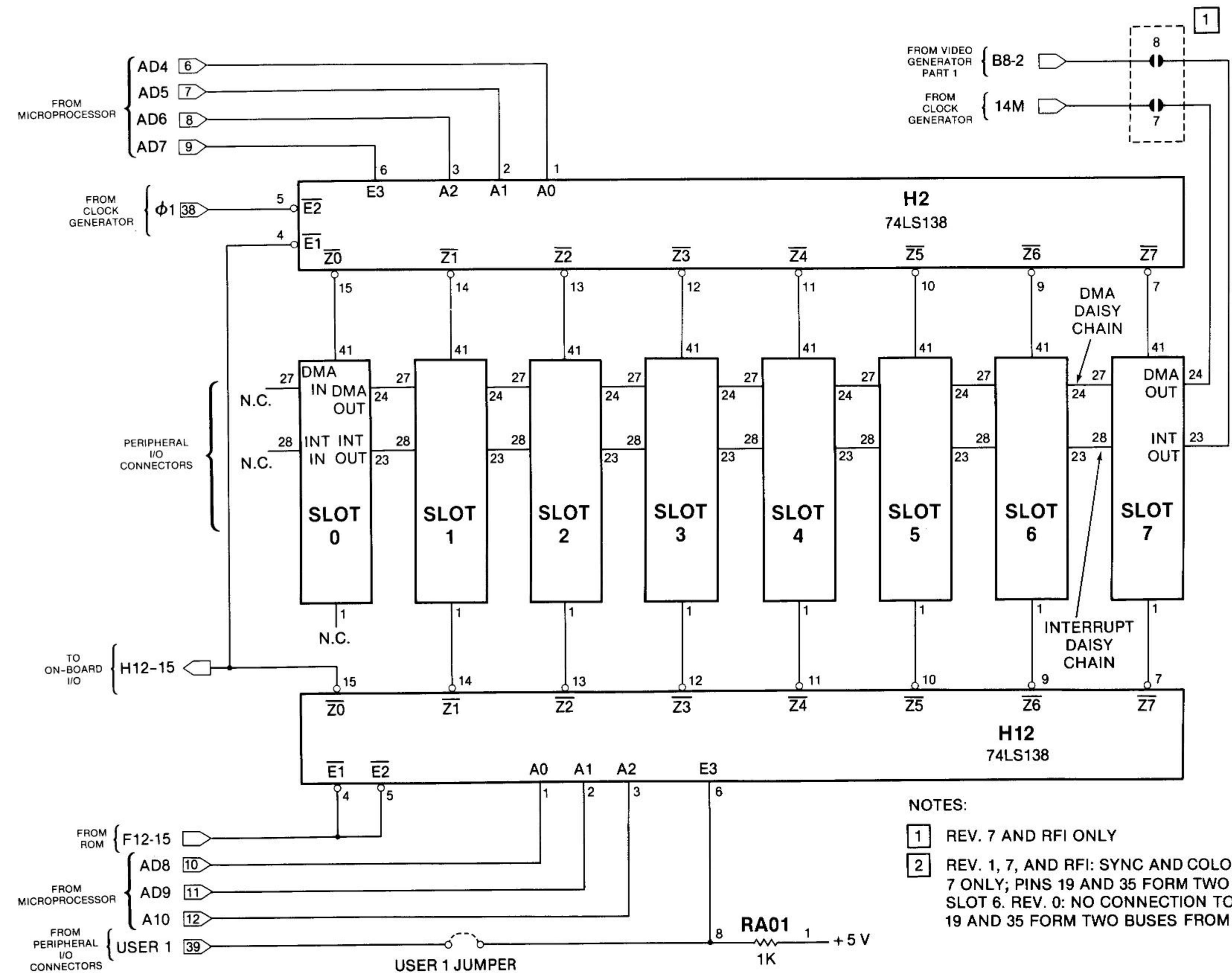


Fig. C-11. Peripheral I/O (all revisions).

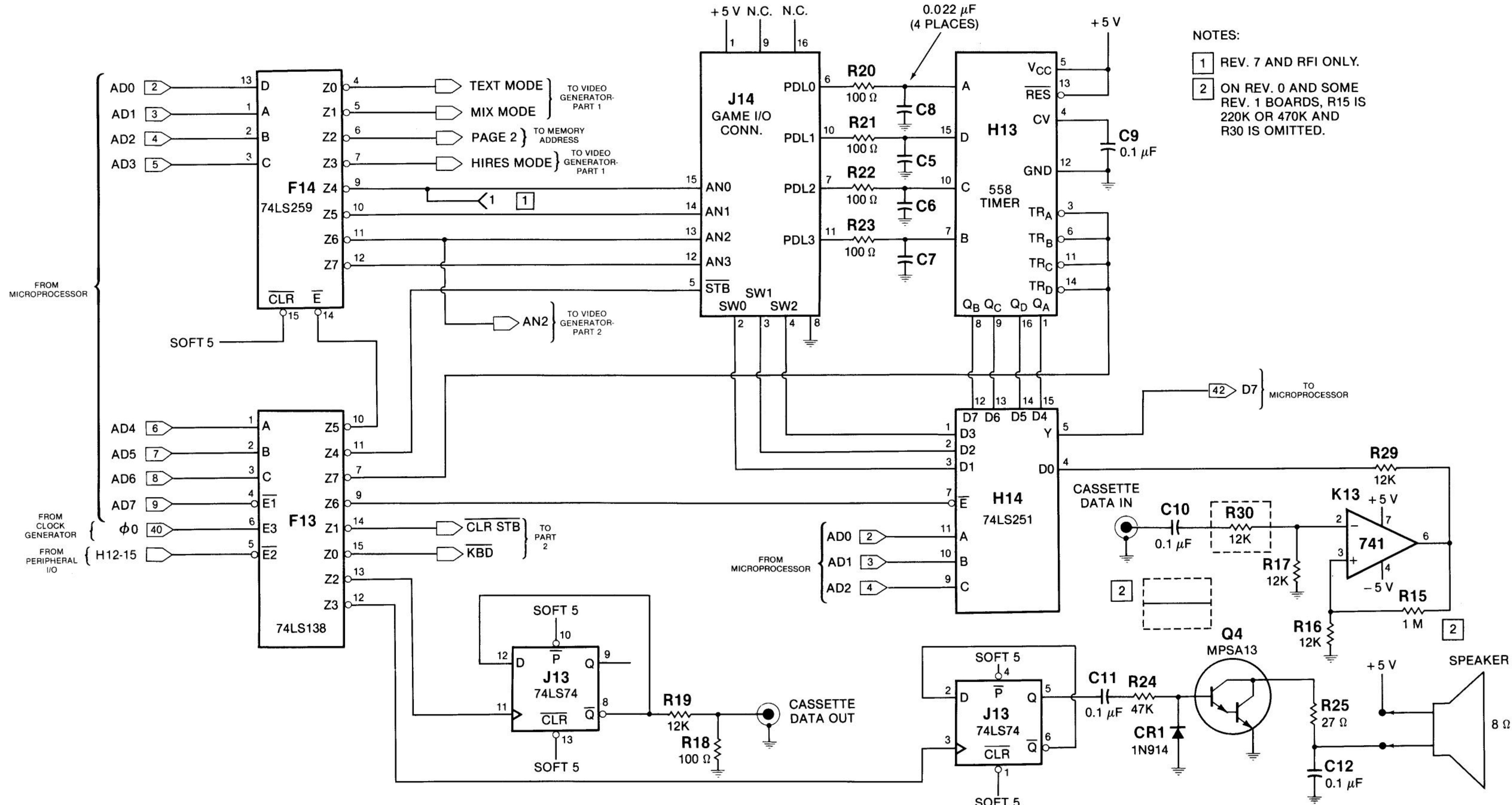


Fig. C-12. On-board I/O—part 1 (all revisions).

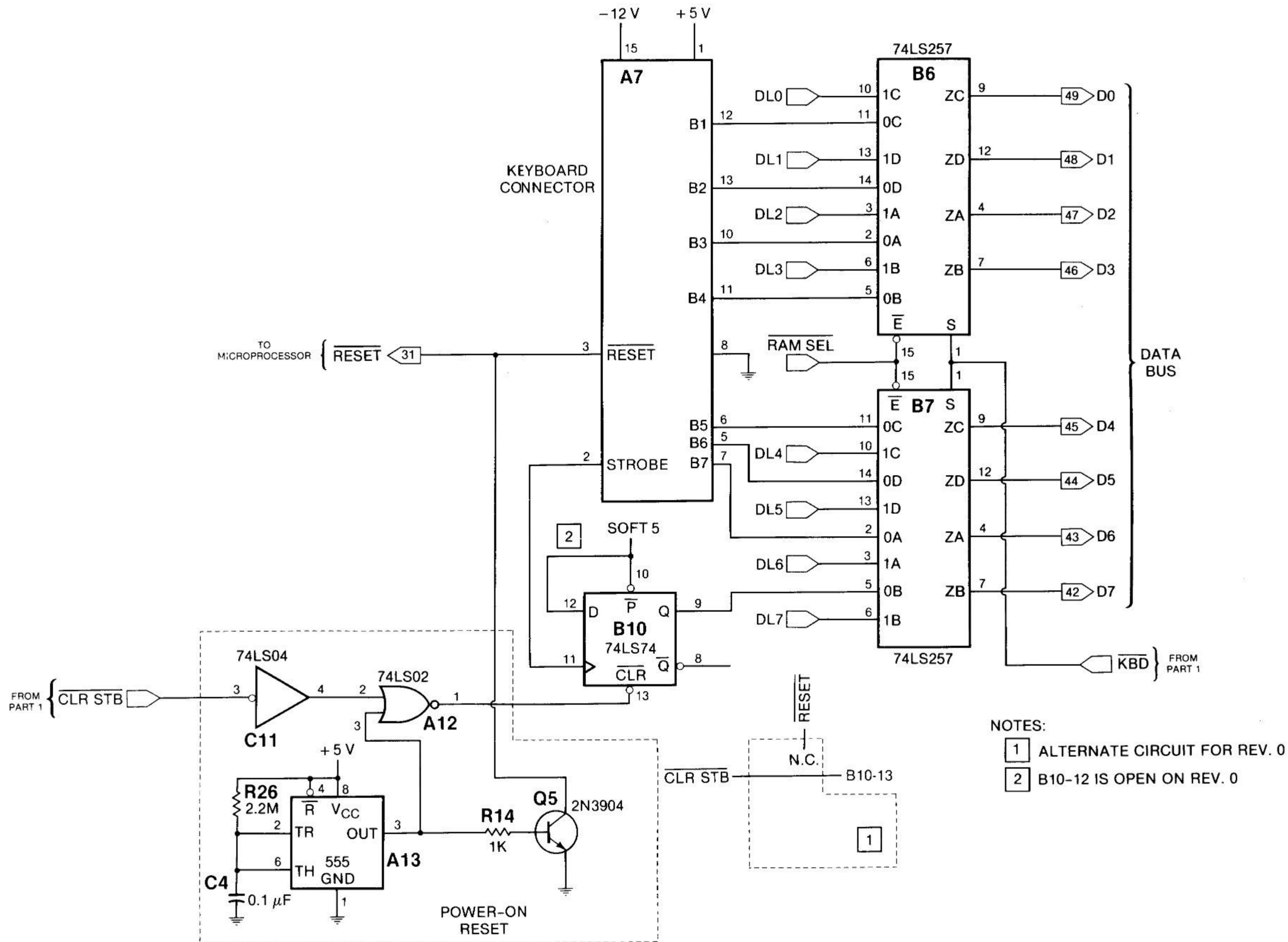


Fig. C-13. On-board I/O—part 2 (all revisions).

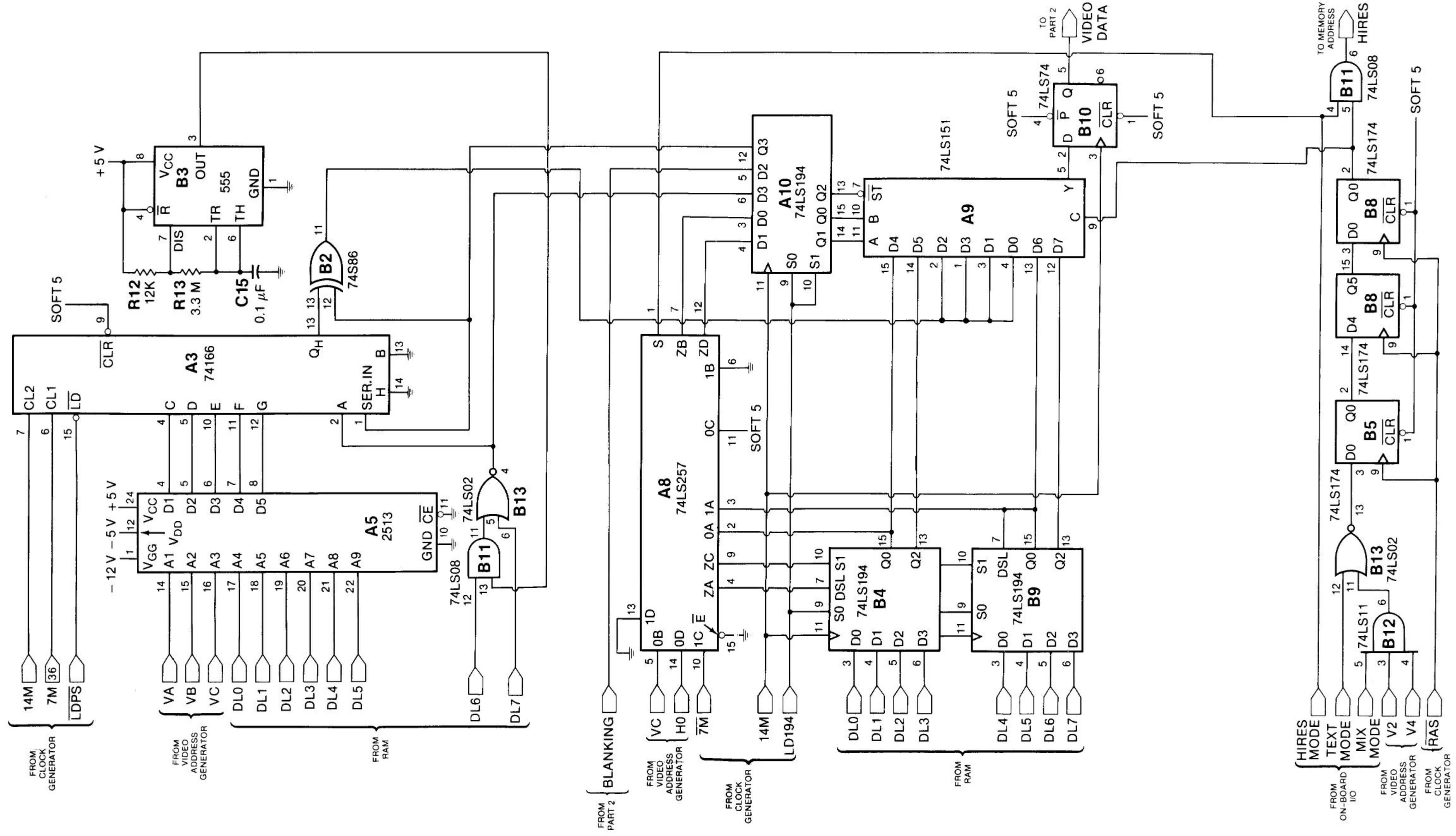


Fig. C-14. Video generator—part 1 (Rev. 0).

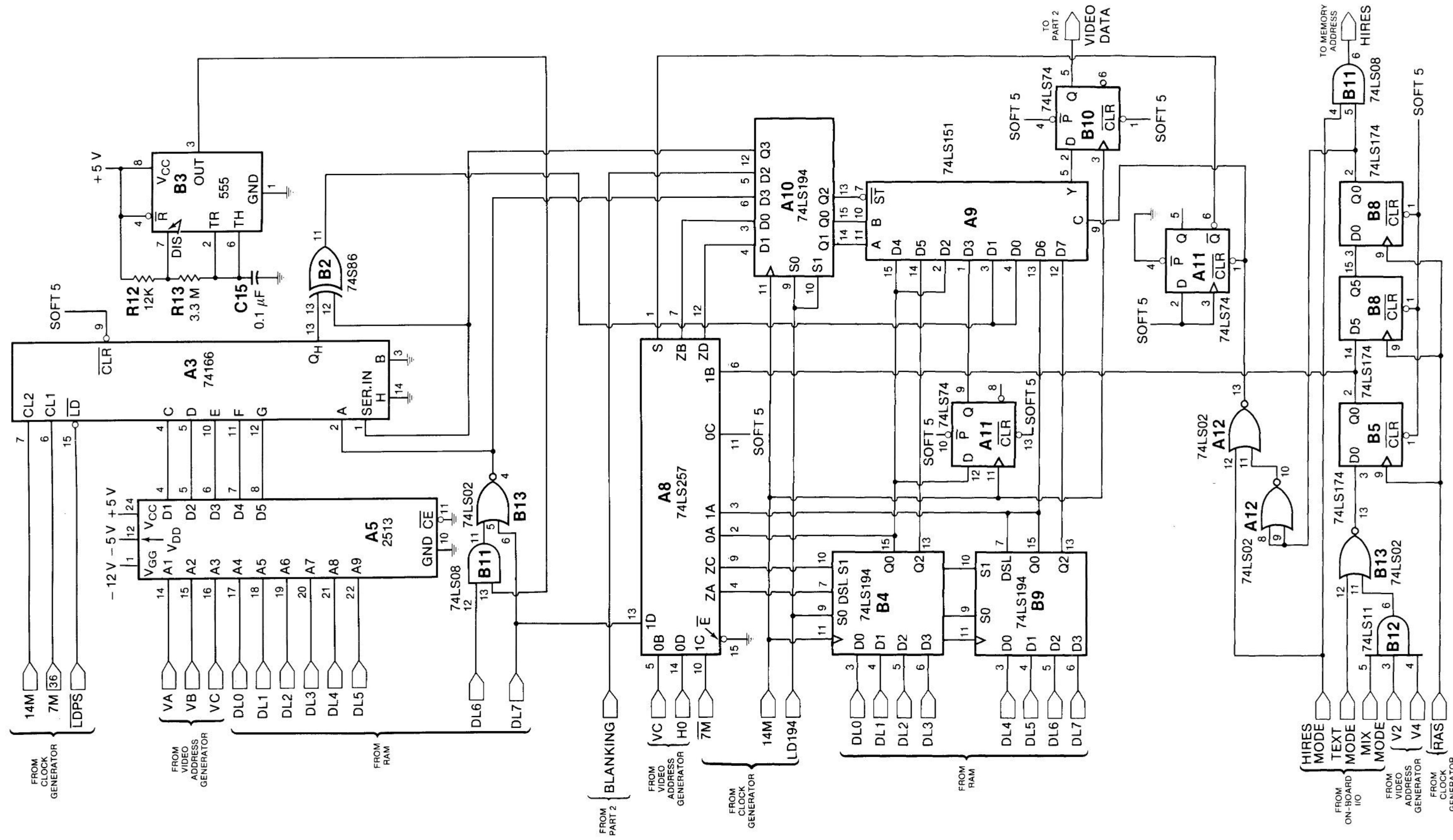
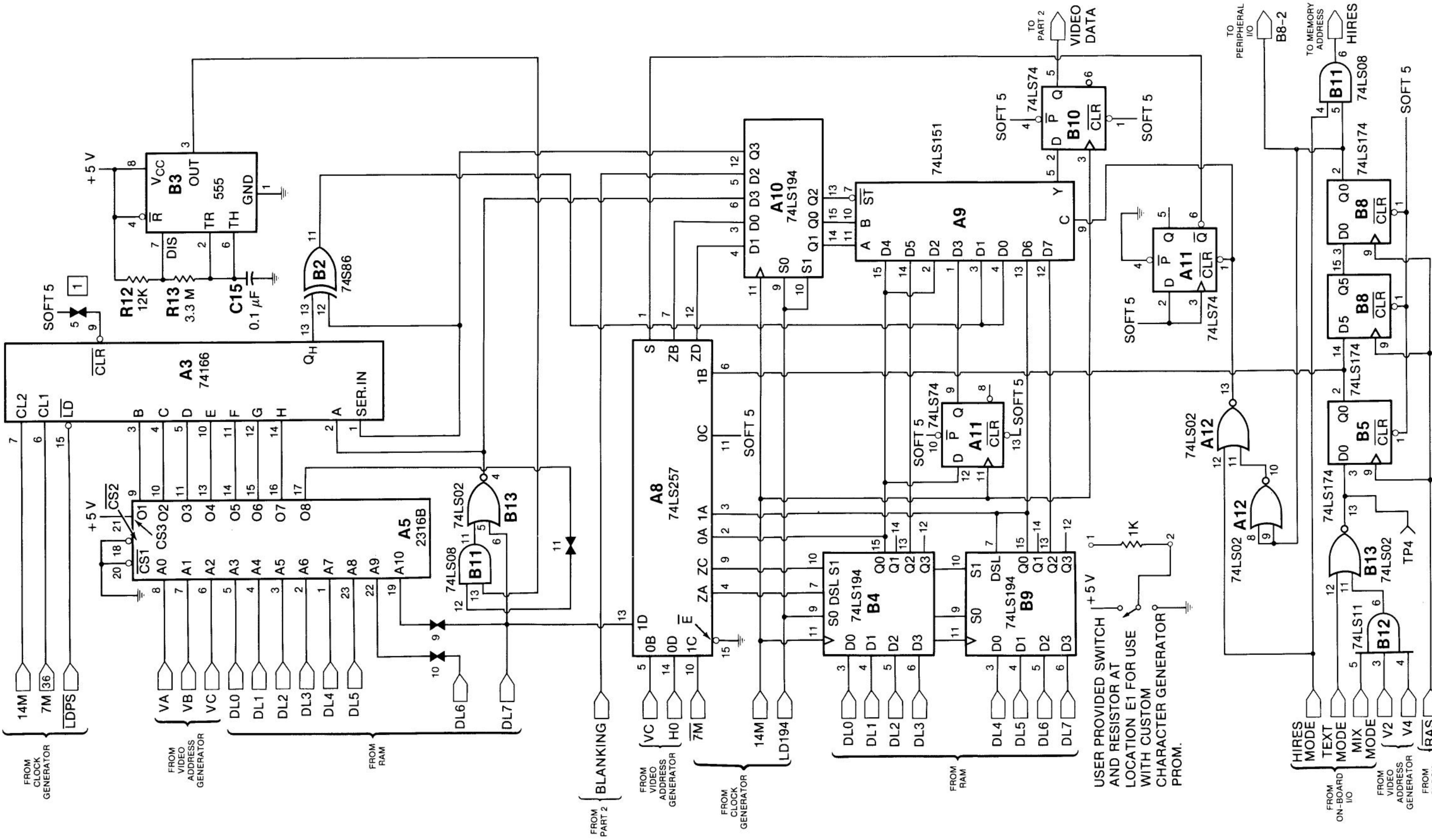


Fig. C-15. Video generator—part 1 (Rev. 1).



**Fig. C-16.** Video generator—part 1 (Rev. 7, RFI).

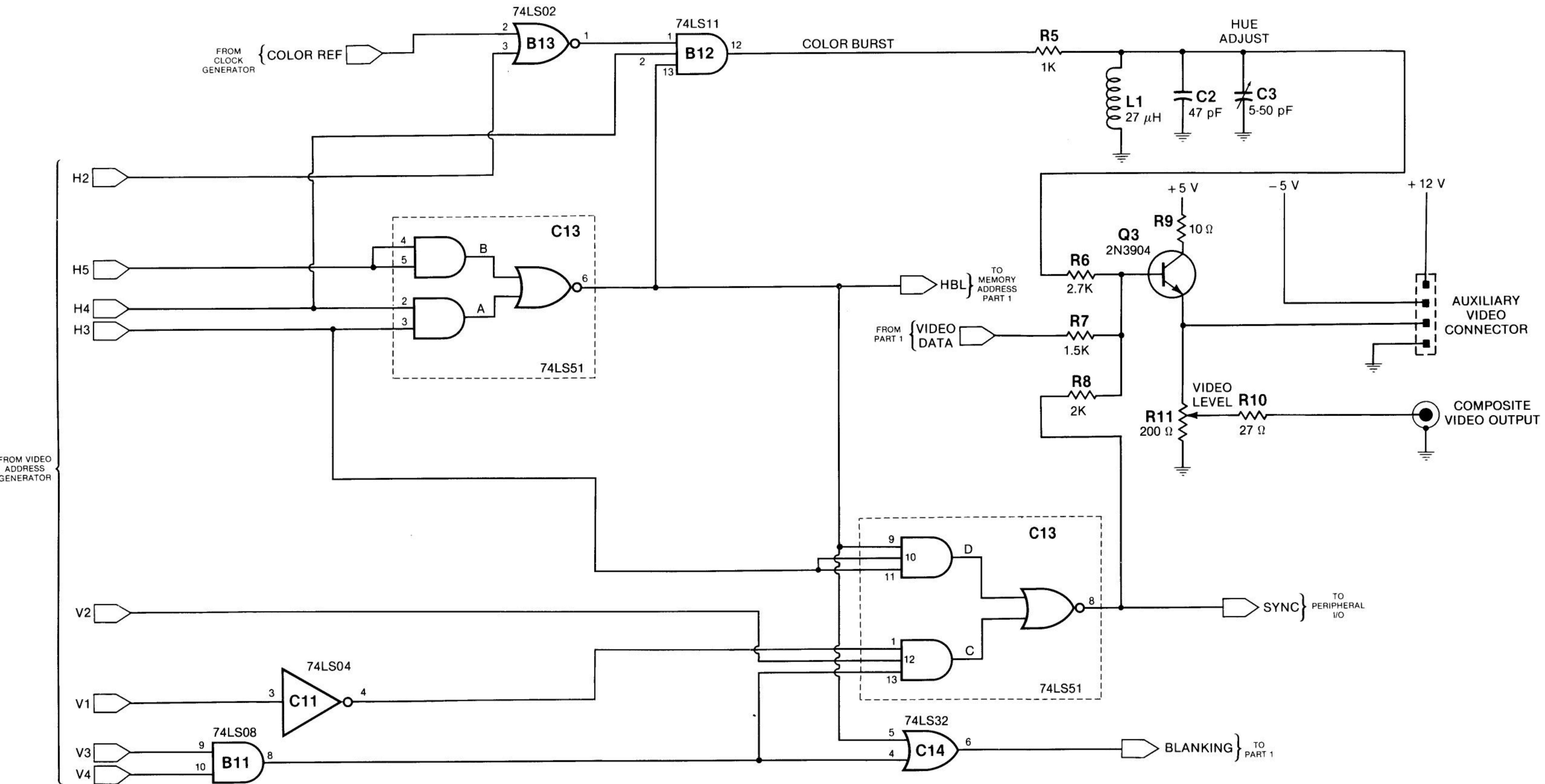


Fig. C-17. Video generator—part 2 (Rev. 0).

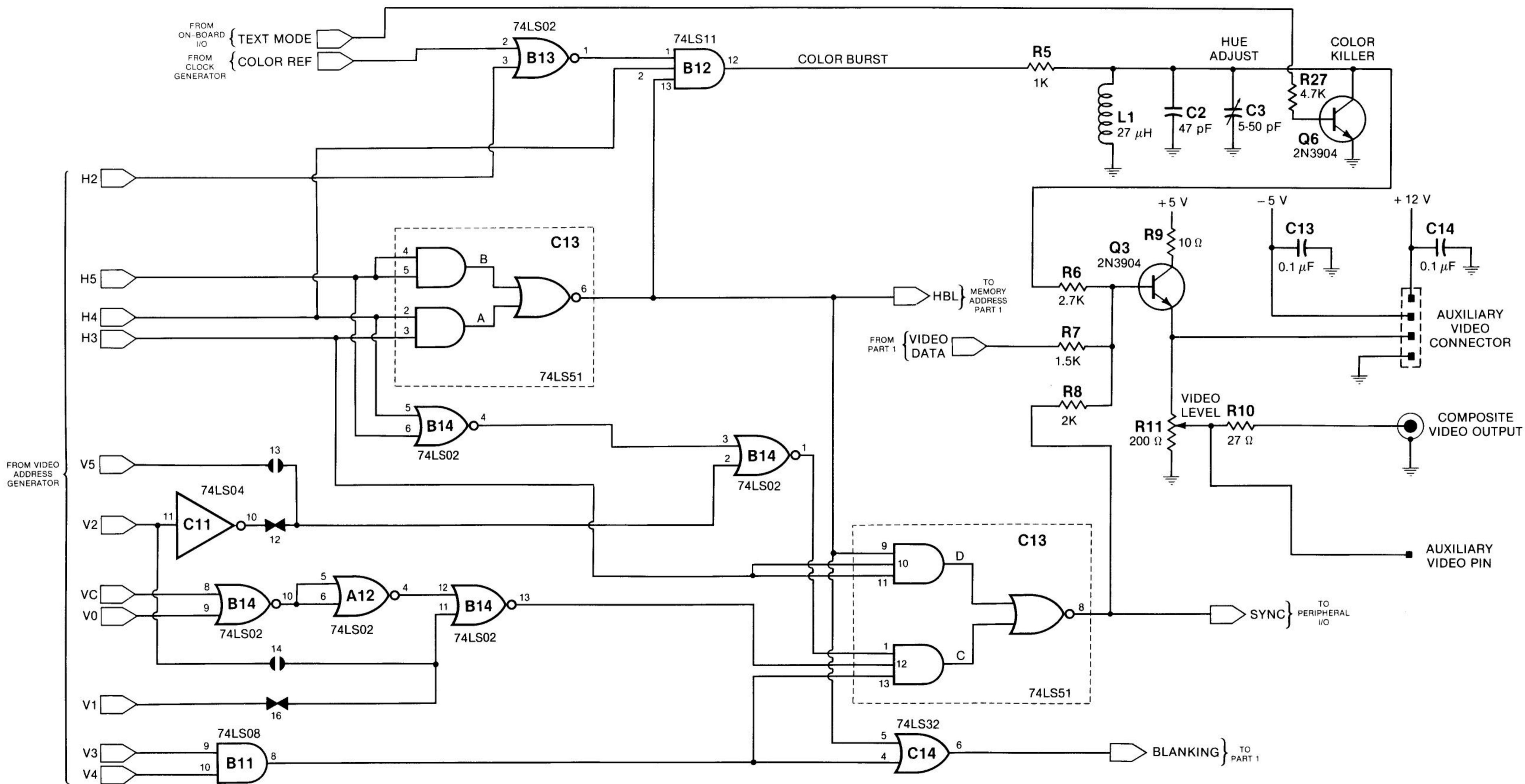


Fig. C-18. Video generator—part 2 (Rev. 1).

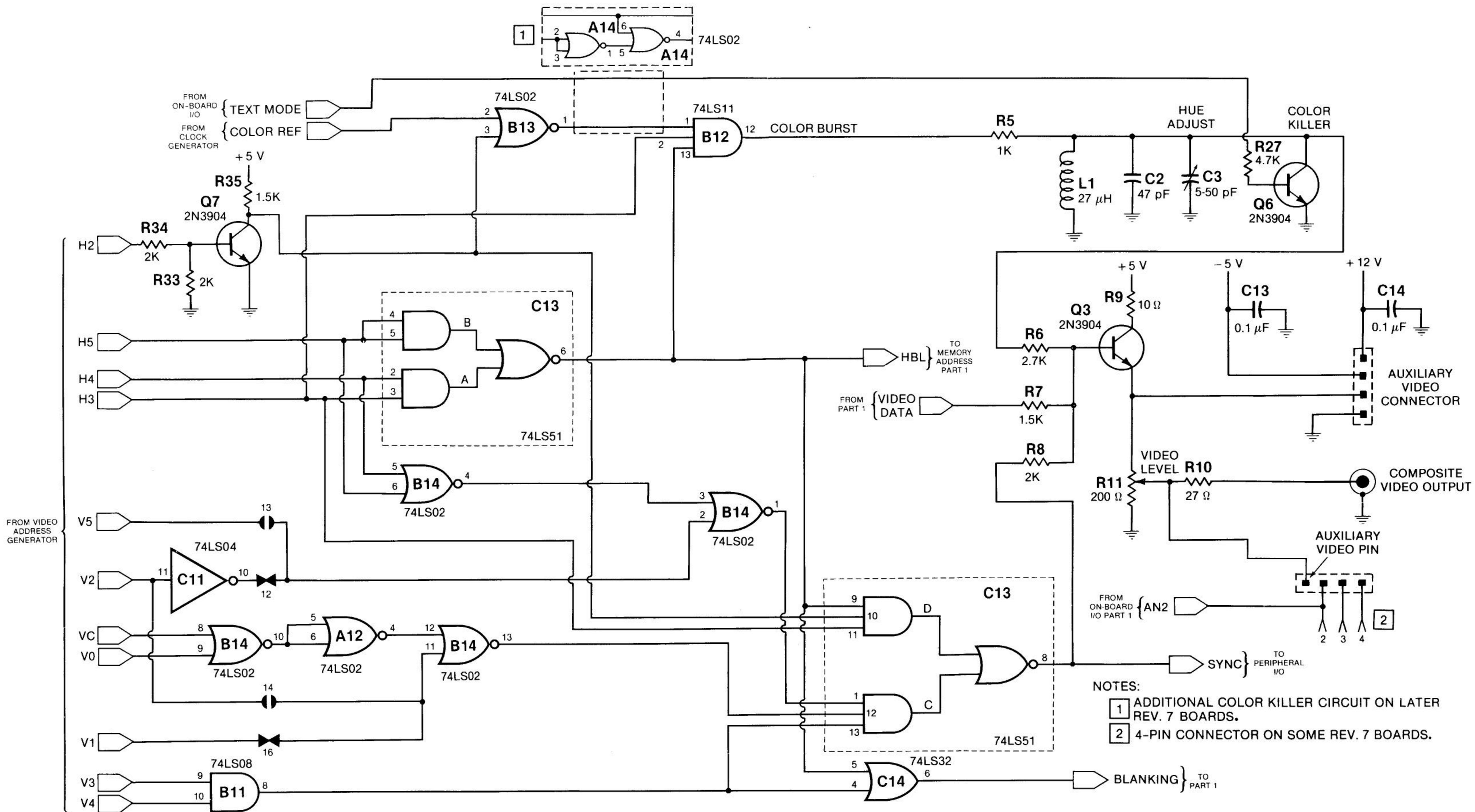


Fig. C-19. Video generator—part 2 (Rev. 7).

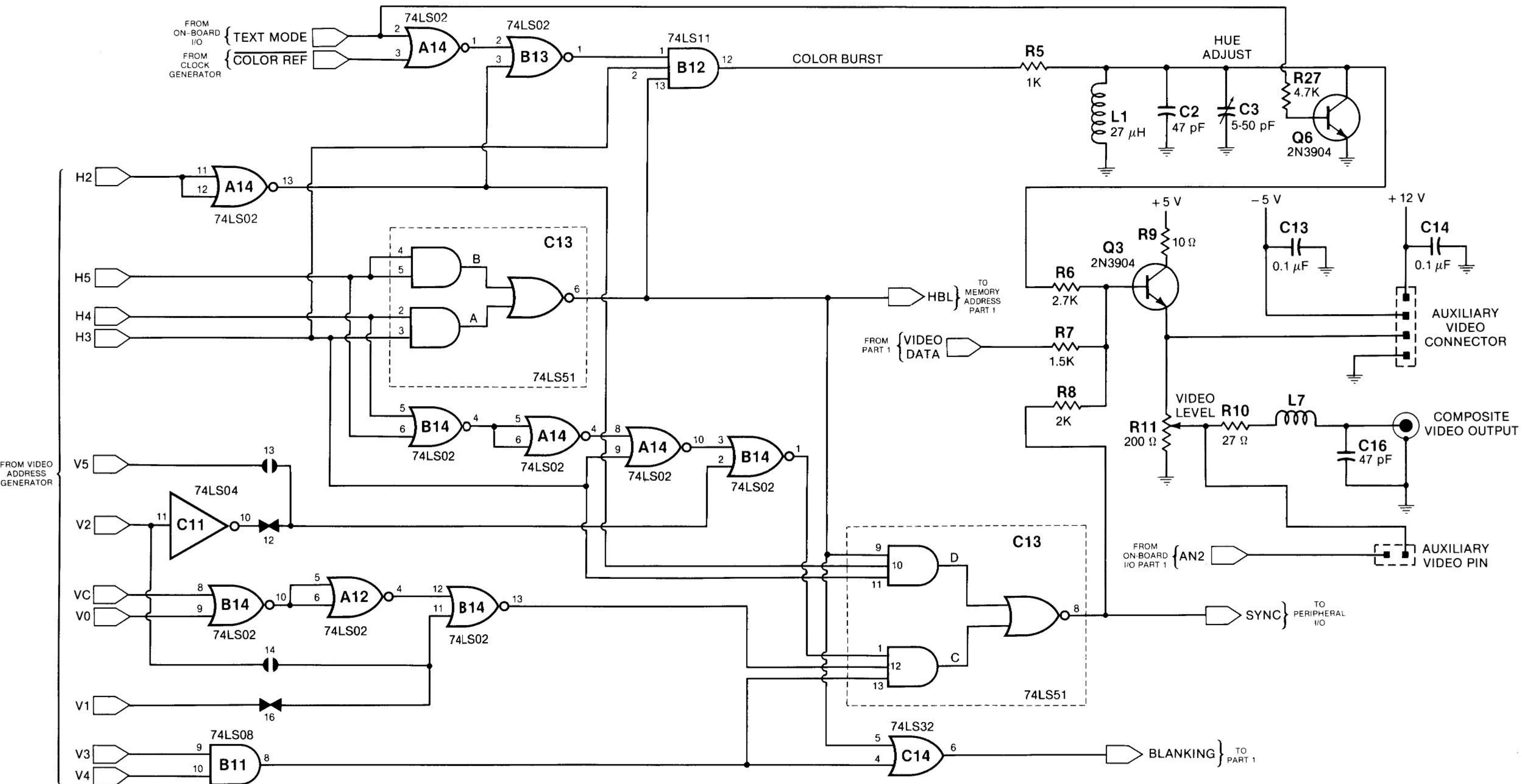


Fig. C-20. Video generator—part 2 (RFI).

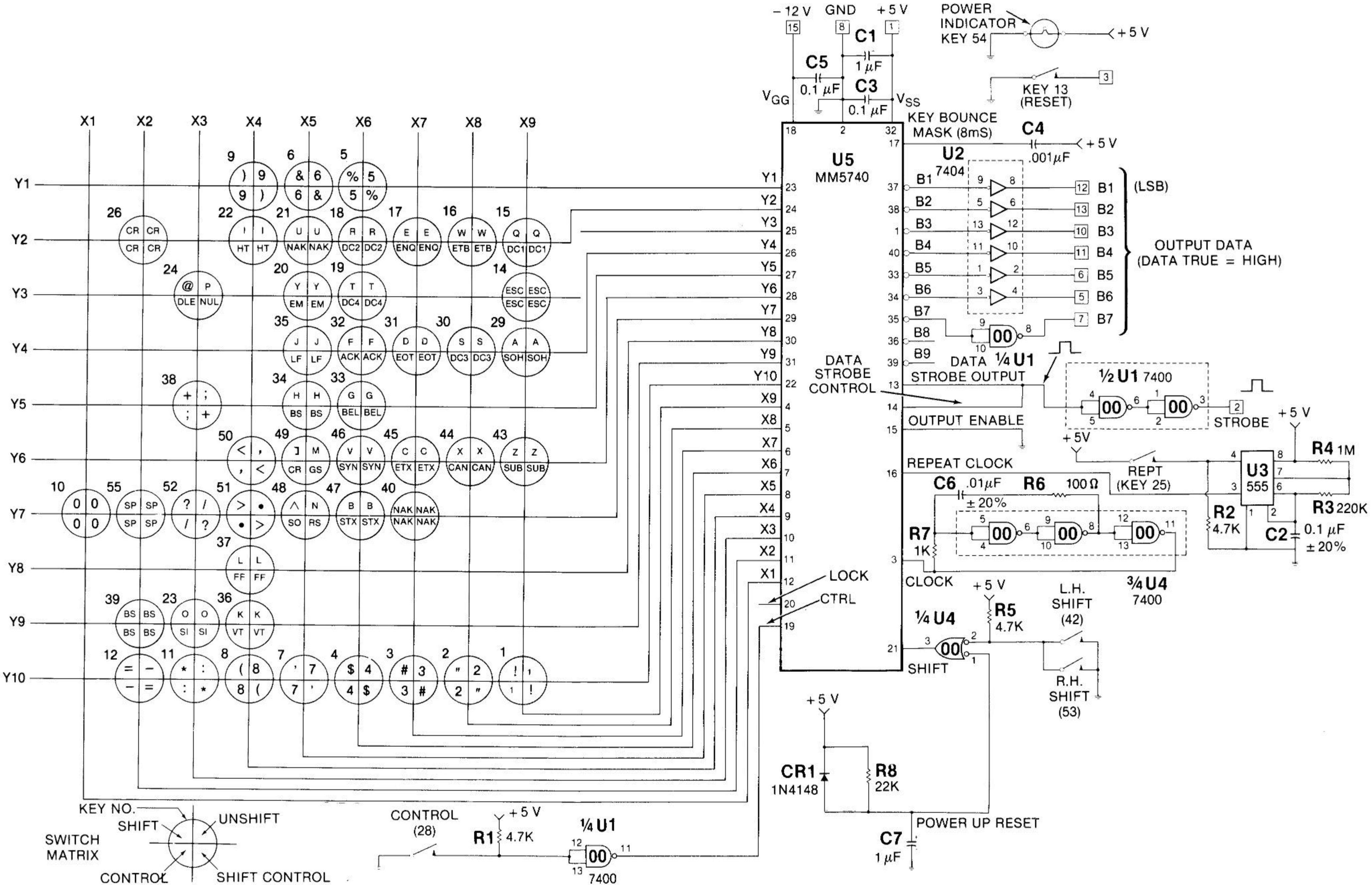


Fig. C-21. Single-piece keyboard.

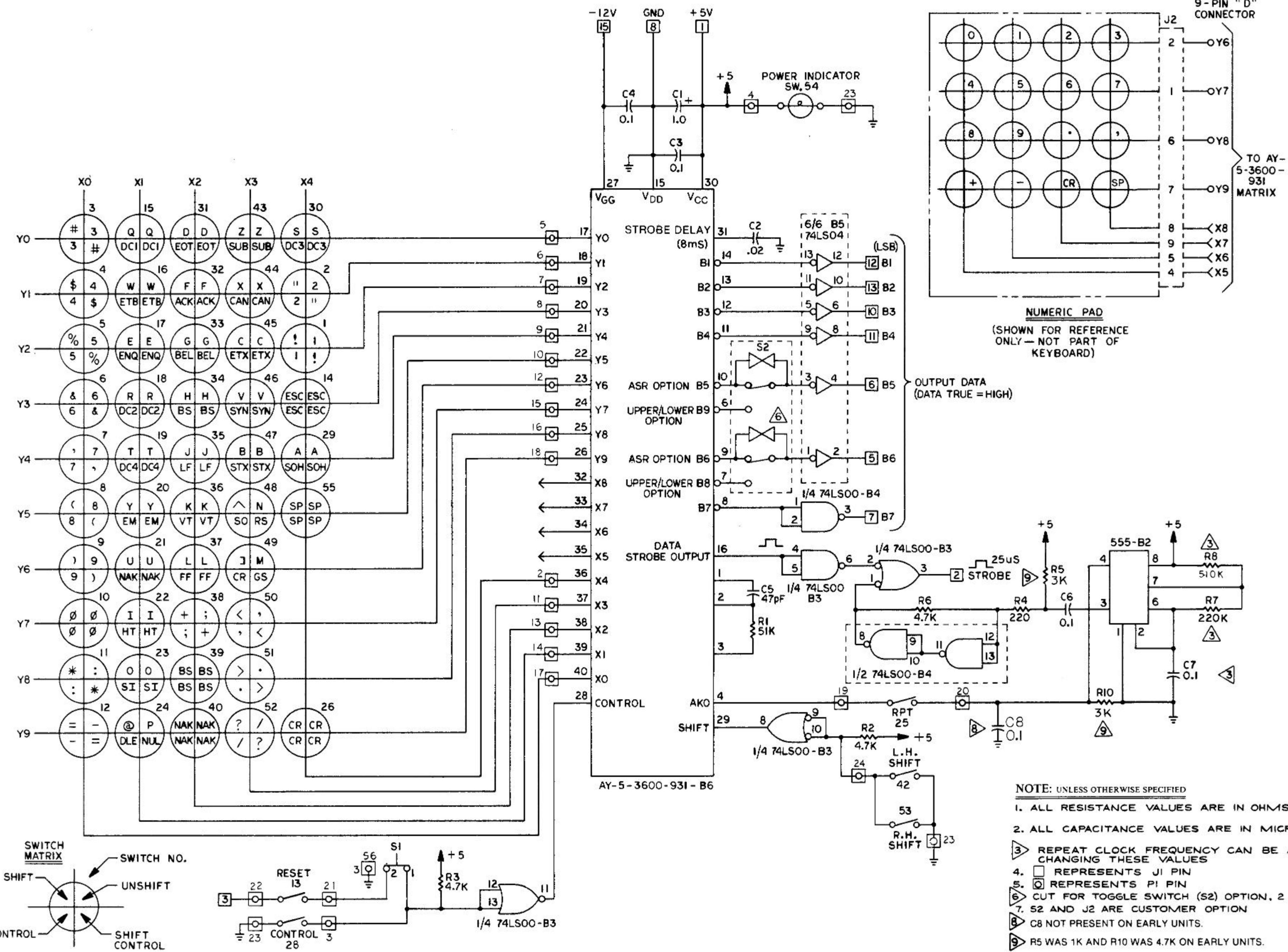


Fig. C-22. Two-piece keyboard.

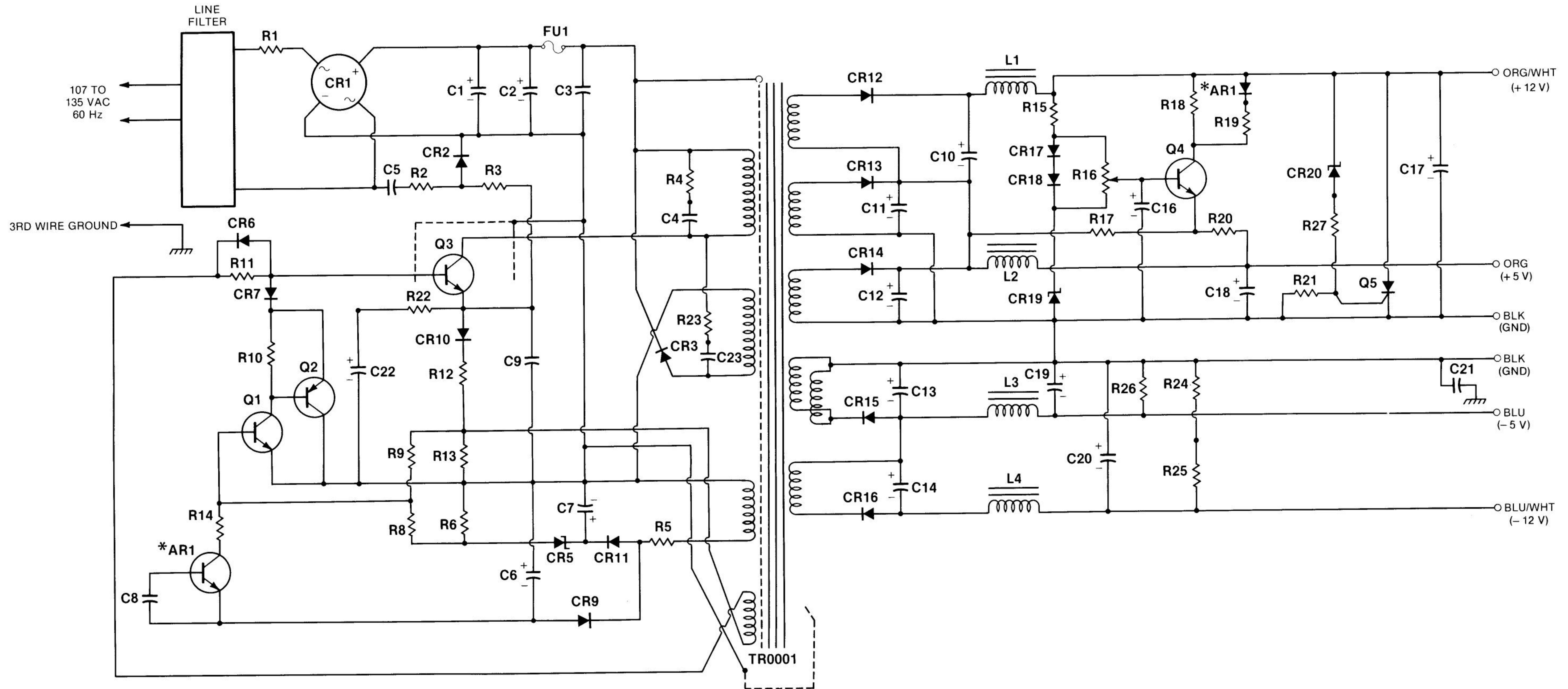


Fig. C-23. Power supply.