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TO FIX MEATSHAK TO NOTTAGE REGULATOR SCREW MAS AND NUT HECKGON WS ARE NOTE. EYELET CAN SUBSTITUTE. RACH, IT NS SULTABLE FOR 6556 REV. I AND 6567 REV. S. DO NOT USE FOR 6567 REV. 8 OR 6569 REV. 3. গ

CZOC, IT IS SUITABLE FOR MBITZA101. CROS, IT IS SUITABLE FOR 6569 REV.T. BUT WHEN USE ESTIBS (UTD ITEM 186.), DO NOT USE THIS CAPACITOR. 49

# PARTS LIST — PCB ASSEMBLY #250407-04

## **C** — Indicates Commodore Stocked Part Number

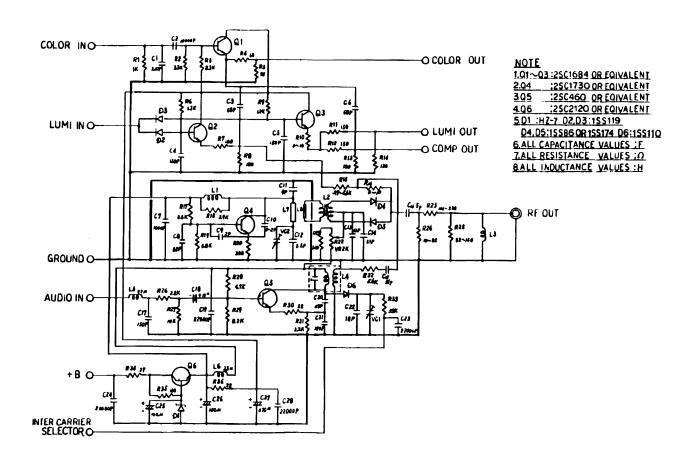
INTEGRATED CIRCUITS				RESISTORS (Continued)							
U1,U2	6526 CIA		C 906108-01	R26	Jumper Wire	$\prod$	R39		3	390	
U3	2364 Basic ROM		C 901226-01	R27	Pot 500Ω	• • • • • • • • • • • • • • • • • • • •		1	1	М	
U4	2364 Kernal ROM		C 901227-03	R28	1K		R4:	2	8	2	
U5	2332 Char ROM		C 901225-01	R29	1K		R4:			.3K	
U6	2114L-20 RAM		901453-01	R30	1K		R44			.3K	
U7	6510 μ Processor		C 906107-01	R31	180		R4!			.3K	
U8	7406		01522-06 sub:	R33	47K		R50			M	
	7416		901522-14	R34	47K		R51			.5K	
U9-U12	4164 (200 nS)		901505-01	R35	470K		1 1		3	00	
U13	74LS257		901521-57	R36	1K					90	
U14	74LS258		901521-58	R37	2.7K		R10			K	
U15	74LS139		901521-18	R38	1K		R10			2K	
U16	4066		901502-01			L		-			
U17	82S100 PL	Δ.	C 906114-01	RESISTOR PACKS							
U18	6581 SID		C 906112-01								
U19	6567 VIC II		C 906109-04	RP1,2	33Ω, 8 Pin (Bourns No.						
U20	LM556		901523-03	220	4308R-102-3						
U21-U24	4164 (200	nS)	901505-01	RP3	3.3KΩ, 8 Pin		urns	No.			
U25	74LS257		901521-57	224	4308R-101-3	-					
U26	74LS373		901521-29	RP4	3.3KΩ, 10 Pi	ın					
U27	74LS08		901521-03	CAPACIT	APACITORS						
U28	4066		901502-01								
U29	74LS74		901521-06	C1-7	Ceramic	.1	μF,	25V			
U30	74LS193		901521-26	C8	Electrolytic				- 50%	, –10%	
U31	74LS629		901521-68	C9	Ceramic			25V		•	
U32	MC4044		906128-01	C10,11	Ceramic		•	50V, 1	0%		
				C12	Ceramic	.1	μF,	25V			
TRANSISTORS					Electrolytic	10	μF,	25V, +	- 50%	, –10%	
Q1,2	2SC1815	C 90	02693-01 sub:	C16	Ceramic	.1		25V	=00/	4.00/	
03	TIP29 A		902653-01	C17	Electrolytic				- 50%	, –10%	
Q7,8	•		C 902693-01	C18	Ceramic			25V			
				C19	Electrolytic 2						
DIODES				C20,21	Film			100V,	20%		
			222122 22	C22	Ceramic			25V			
CR1	2.7V Zener		906103-02	C23	Ceramic			50V, 1		4.004	
CR2	7.5V Zener		900941-01	C24	Electrolytic		•		- 50%	, –10%	
CR4	Bridge S2VI		C 251026-01	C25-33	Ceramic			25V	<b></b> 00/	4.00/	
	DBA		C 251026-02	C34	Electrolytic		•		- 50%	, –10%	
005.0	DBA:		C 251026-03	C35	Ceramic		•	50V	.0/ 0:		
CR5,6	Rectifier IN4	FUU I	900750-01	C36	Ceramic		•	50V, 5			
RESISTORS — All values are in ohms- 1/4 W,			C37				50V, 1				
	5%, unless noted otherwise.			C38	Ceramic			50V, 5	7% SL		
<del> </del>	1	I	1	C39-47	Ceramic 1		•	25V	00/ D	,	
R1	3.3K	R6	1K	C48			•	50V, 1	U% B	•	
R2	1.5K	R7	10K	C49-54	Ceramic		•	25V			
R3	10K	R16	1K	C55	Ceramic			50V			
R4	1K	R17	2.7K	C56	Ceramic			25V	E00/	100/	
R5	560	R19	15K	C57	Electrolytic		•		50%	, –10%	
		l		C58	Ceramic	. !	μ٢,	50V			

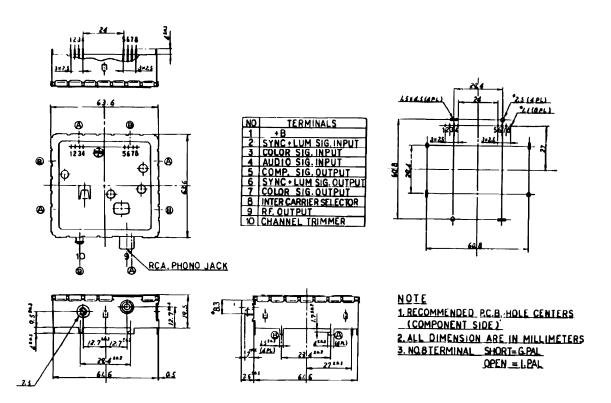
# PARTS LIST — PCB ASSEMBLY #250407-04 (Continued)

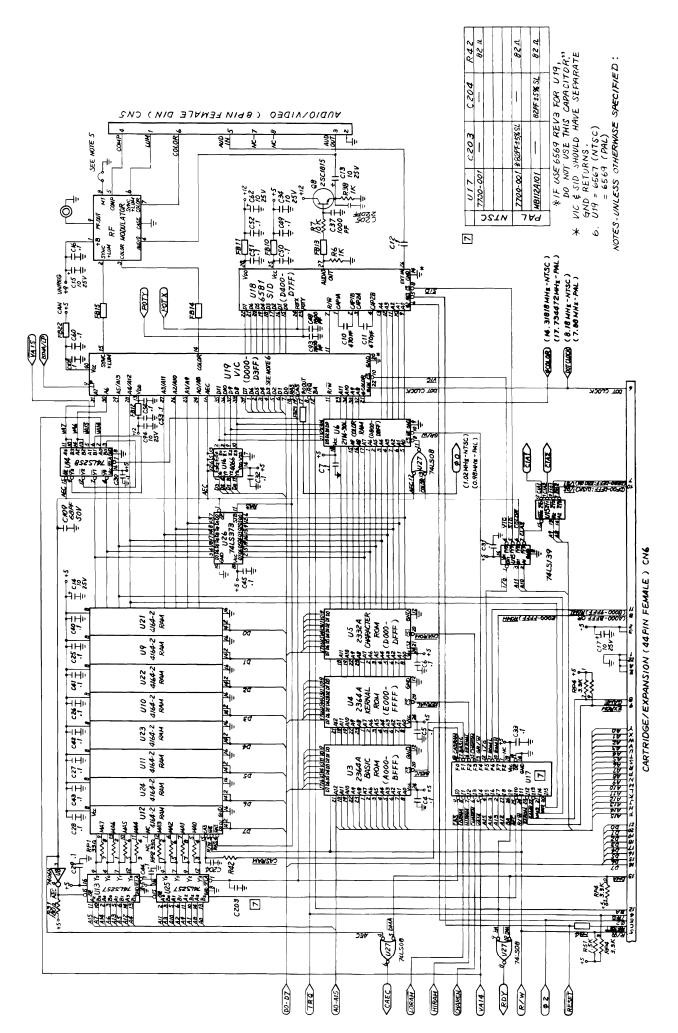
# **C** — Indicates Commodore Stocked Part Number

CAPACITORS (Continued)				CONNECTORS				
C59,60 C62,65	Ceramic Electrolytic	.1 μF, 25V 10 μF, 25V, - -10%	+ 50%,	CN1 CN4 CN5	Header Assy, 20 Pin 6 Pin Din 8 Pin Din	903331-20 C 903361-01 C 325573-01		
C66,67,68 C70 C74,82 C83	Film Ceramic Ceramic	.1 μF, 25V 16 pF, 5% .1 μF, 25V 82 pF, 5%		CN6 CN7 CN8,9 CN10	44 Pin Card Edge 7 Pin Din Plug Assy, 9 Pin MINID Header Assy, 3 Pin	C 251116-01		
C84 C85	Ceramic Ceramic	.1 μF, 25V .47 μF, 50V, 1	10%	MISCELLANEOUS				
C88 C89 C90 C91	Electrolytic Ceramic Electrolytic Electrolytic	1000 μF, 25V .1 μF, 25V 470 μF, 50V 100 μF, 16V, -1	+ 50%,	L2 L4 L5	Coil Inductor 2.2 μH Coil Inductor 1.2 μH Choke Coil	C 325559-02		
C92 C93 C94	Ceramic Ceramic Electrolytic	.1 μF, 25V		Y1 SW1	Crystal 14.31818 MHz Rocker Switch DPDT	C 900558-01 904500-01		
C95,96 C97	Ceramic Ceramic	-10% .1 μF, 25V .22 μF, 25V	0070,	VR1 VR2	Voltage Regulator MC7812CT Voltage Regulator	901527-01		
C98,99	Ceramic	.1 μF, 50V, - -20%	+80%,	VII.2	MC7805CT	901527-02		
C100 C101	Ceramic Ceramic	.22 μF, 25V .1 μF, 50V, -	+80%,	M1	Modulator	C 251080-01		
C102	Electrolytic Ceramic	-20% 10 μF, 25V, + -10% .1 μF, 25V	+ 50%,	F1 FB1-5 FB7-23	Fuse, Normal Blo, 250V, Ferrite Bead	903025-01		
C104 C105 C108 C200	Ceramic Electrolytic Ceramic	.1 μF, 25V 10 μF, 25V, 2 .1 μF, 25V	20%		Connector Panel (Power, ON, OFF) Cartridge Guide Shield Box Shield Cap	251095-01 326116-01 C 251023-01 C 251024-01		

# **MODULATOR SCHEMATIC #251025**







## U7 - 906107-016510 MICROPROCESSOR

01

**RDY** 

**NMI** 

**AEC** 

GND

02

RES

1

2

4

5

6

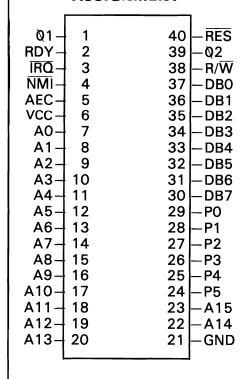
21

39

40

22,23

## PIN **ASSIGNMENT**



#### will cause the processor to halt. The current address line being fetched will be on the address bus. Can also be used to interface slower devices to the microprocessor. 3 IRQ

speeds.

Interrupt request input. When a low pulse is applied a jump to a location specified by the contents of FFFE and FFFF will occur to service the interrupt, if the interrupt mask flag is not set. This is a maskable interrupt.

Phase 1 clock input. This clock input is used to develop the internal overlapping

Single step operation input. A low applied

phase 2 clock. 1 MegHz or 2 MegHz

Non-maskable interrupt input. A low transition will cause a jump to a location specified by FFFA and FFFB to a subroutine which will service the interrupt. Address enable control input. A low ap-

plied to will cause the address bus to enter hi impedance state, so other devices can control the address bus.

ut.

6	VCC	5VDC inpu
7-20	A0-A15	Address bu

us outputs. Unidirectional bus used to address memory and I/O devices. The address bus can be disabled by con-

trolling the AEC input. Dc ground connection.

24-29 P0-P5 I/O bidirectional port. This port can be controlled via memory locations 0000 and 0001.

0001 = Output register

0000 = Data direction register

30-37 DB0-DB7 Bidirectional data bus. This is the bus that passes the data to or from any I/O device or memory. 38 R/W

Read/Write output. The processor generates a low level when writing, and a high level when reading. This signal is usually decoded for read or write operations to memory or I/O.

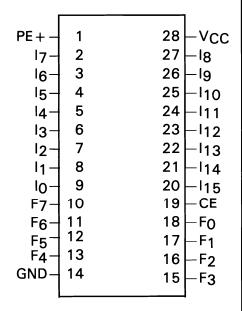
Phase 2 output. The processor generates this clock signal from the phase 1 clock applied. The two clock signals are 180 degrees out of phase. The phase 2 clock is used in decoding I/O and memory on the positive half cycle.

Reset input interrupt. A low pulse causes a jump to a subroutine specified by FFFC

and FFFD, which will initialize all processor controlled devices. This occurs during

a power up sequence.

### PIN ASSIGNMENT



U17 - 906114-01**PROGRAMMABLE** LOGIC ARRAY (PLA)

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