

TER REPORT

Hardware Performance Counters

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Abstract

Calmos le ramoloss, l'abstract c'est pas pour tout de suite

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1 Introduction

If you wish to explore the details of the work done for the project, the project's code is hosted on GitHub at <https://github.com/omelette-bio/projet-tutorat-s2-m1> Parler ici de ce que sont les compteurs matériels de performance Parler ici du but du projet

Part I

Checking Hardware Compatibility

In this part, we'll describe how to read precise informations about our CPUs, and go beyond the `cputime` linux command. We'll also cover how to find the events measurable by the CPU.

2 Checking CPU capabilities : the CPUID instruction

x86 architecture CPUs provide an instruction called **CPUID** that provides various informations on the CPU by reading special registers, for example, CPU name, memory address sizes, but also Hardware Performance Counters capacities.

The **CPUID** instruction is divided in **leafs** and **sub-leafs**, allowing to read multiple informations, stored statically in the CPU. These data are then stored in `eax`, `ebx`, `ecx`, and `edx` registers for the programmer to read.

For example, on intel, the leaf `0x80000008` stores in the `eax` register the physical address size and virtual address size of the CPU.

Intel and AMD manuals use a specific notation for this instruction which is the following : **CPUID[LEAF].REG** to more easily tell the leaf and register used for obtaining any information, with the previous exemple, such notation would give **CPUID[0x80000008].EAX**.

2.1 Using CPUID to find HPCs informations on INTEL CPUs

CPUID[0x0A].EAX gives us these informations

byte 1 [7:0]: version number of the Architectural Performance Monitoring

byte 2 [15:8]: number of general purpose PMC¹ per logical core

byte 3 [23:16]: bit size of the PMC registers

byte 4 [31:24]: number of architectural events

but, **CPUID[0x0A].EDX** gives us also the number of fixed PMC per logical core.

Here are the results on the Intel test machine :

Performance Monitoring Version : 5

Bit width of a PMC register

Number of general purpose PMC per logical core : 8

Number of fixed PMC per logical core : 4

Number of architectural events : 8

2.2 Using CPUID to find HPCs informations on AMD CPUs

On AMD, it's **CPUID[0x80000001].ECX** that gives us informations about HPCs.

bit 10 : support of IBS (specific to AMD, will be explained in part jsp combien)

bit 23 : support of 6 Core Performance Counters.

bit 24 : support of 4 NorthBridge Performance Counters.

bit 25 : support of 4 L2 Cache Performance Counters.

¹PMC : Performance Monitoring Counter

3 List measurable events

blablabla....

Part II

HPCs on x86 processors

4 Intel's Hardware Performance Monitoring

5 AMD's Hardware Performance Monitoring

Part III

Benchmarks

6 Using the perf linux command

7 Using the libpfm C-library

