# 1. Description

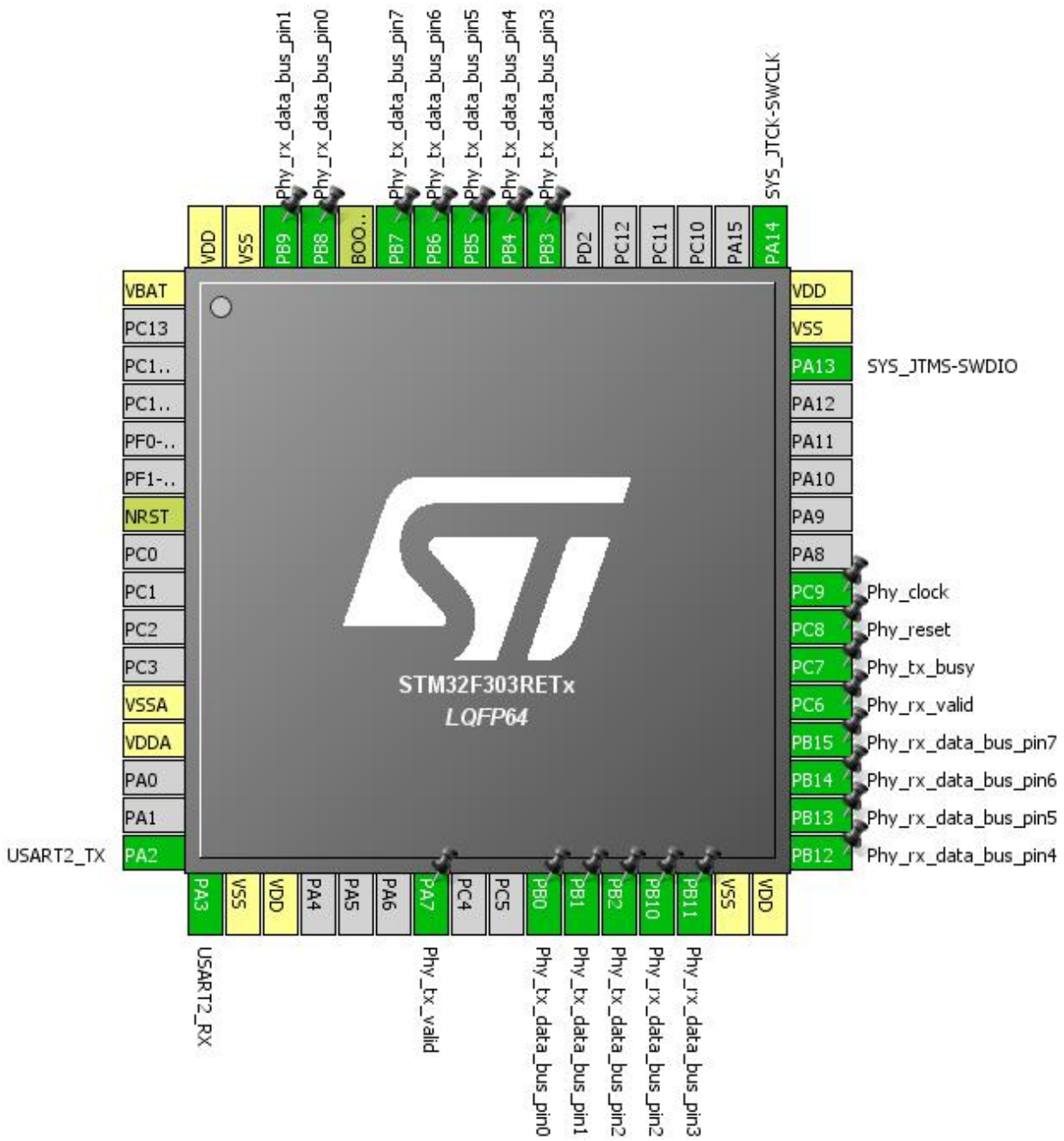
## 1.1. Project

| | |
|---|---|
| Project Name | DLL |
| Board Name | DLL |
| Generated with: | STM32CubeMX 4.21.0 |
| Date | 02/11/2019 |

## 1.2. MCU

| | |
|---|---|
| MCU Series | STM32F3 |
| MCU Line | STM32F303 |
| MCU name | STM32F303RETx |
| MCU Package | LQFP64 |
| MCU Pin number | 64 |

# 2. Pinout Configuration



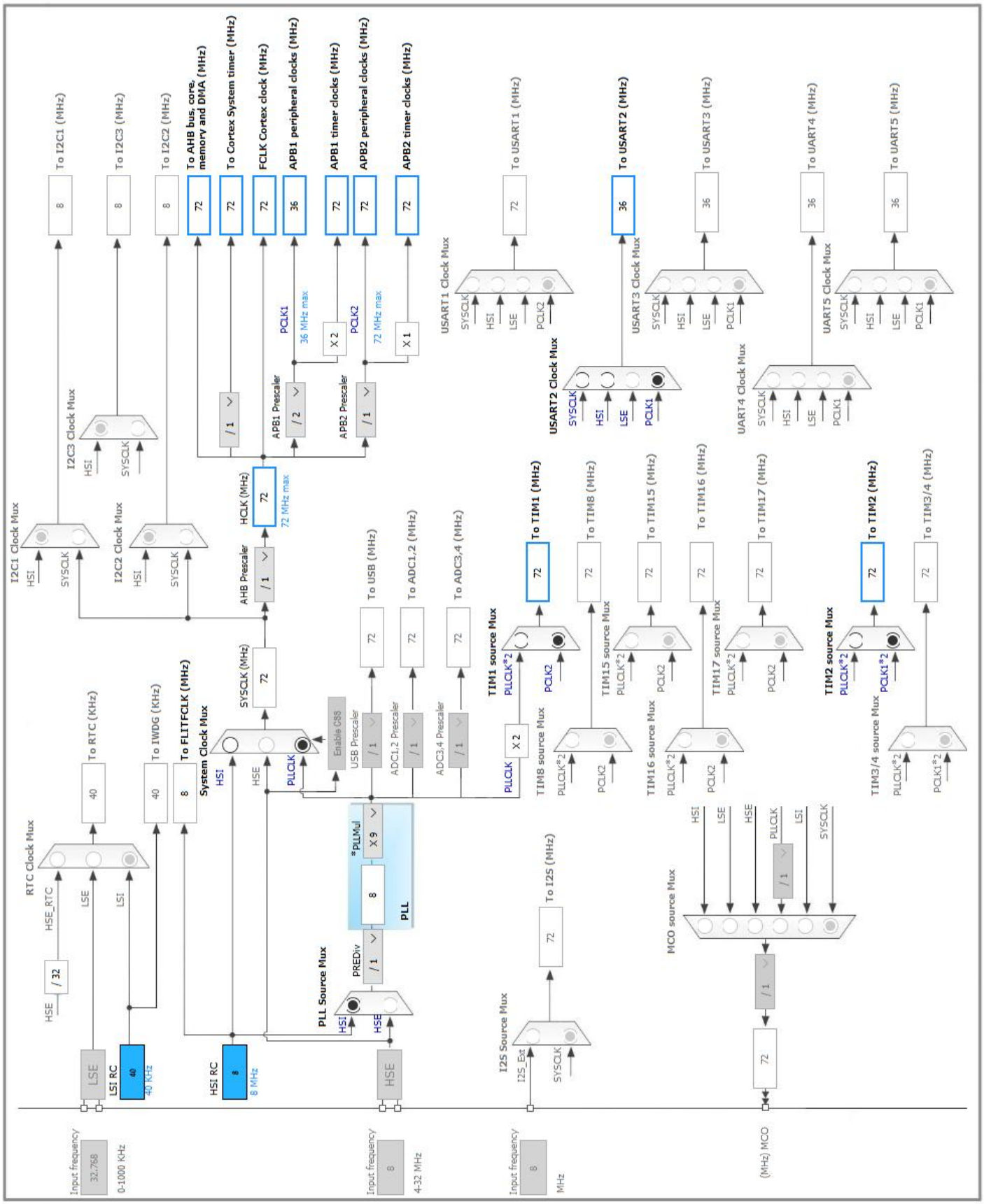
# 3. Pins Configuration

| Pin Number LQFP64 | Pin Name (function after reset) | Pin Type | Alternate Function(s) | Label |
|---|---|---|---|---|
| 1 | VBAT | Power | | |
| 7 | NRST | Reset | | |
| 12 | VSSA | Power | | |
| 13 | VDDA | Power | | |
| 16 | PA2 | I/O | USART2_TX | |
| 17 | PA3 | I/O | USART2_RX | |
| 18 | VSS | Power | | |
| 19 | VDD | Power | | |
| 23 | PA7 * | I/O | GPIO_Output | Phy_tx_valid |
| 26 | PB0 * | I/O | GPIO_Output | Phy_tx_data_bus_pin0 |
| 27 | PB1 * | I/O | GPIO_Output | Phy_tx_data_bus_pin1 |
| 28 | PB2 * | I/O | GPIO_Output | Phy_tx_data_bus_pin2 |
| 29 | PB10 * | I/O | GPIO_Input | Phy_rx_data_bus_pin2 |
| 30 | PB11 * | I/O | GPIO_Input | Phy_rx_data_bus_pin3 |
| 31 | VSS | Power | | |
| 32 | VDD | Power | | |
| 33 | PB12 * | I/O | GPIO_Input | Phy_rx_data_bus_pin4 |
| 34 | PB13 * | I/O | GPIO_Input | Phy_rx_data_bus_pin5 |
| 35 | PB14 * | I/O | GPIO_Input | Phy_rx_data_bus_pin6 |
| 36 | PB15 * | I/O | GPIO_Input | Phy_rx_data_bus_pin7 |
| 37 | PC6 * | I/O | GPIO_Input | Phy_rx_valid |
| 38 | PC7 * | I/O | GPIO_Input | Phy_tx_busy |
| 39 | PC8 * | I/O | GPIO_Input | Phy_reset |
| 40 | PC9 | I/O | GPIO_EXTI9 | Phy_clock |
| 46 | PA13 | I/O | SYS_JTMS-SWDIO | |
| 47 | VSS | Power | | |
| 48 | VDD | Power | | |
| 49 | PA14 | I/O | SYS_JTCK-SWCLK | |
| 55 | PB3 * | I/O | GPIO_Output | Phy_tx_data_bus_pin3 |
| 56 | PB4 * | I/O | GPIO_Output | Phy_tx_data_bus_pin4 |
| 57 | PB5 * | I/O | GPIO_Output | Phy_tx_data_bus_pin5 |
| 58 | PB6 * | I/O | GPIO_Output | Phy_tx_data_bus_pin6 |
| 59 | PB7 * | I/O | GPIO_Output | Phy_tx_data_bus_pin7 |
| 60 | BOOT0 | Boot | | |
| 61 | PB8 * | I/O | GPIO_Input | Phy_rx_data_bus_pin0 |
| 62 | PB9 * | I/O | GPIO_Input | Phy_rx_data_bus_pin1 |

| Pin Number LQFP64 | Pin Name (function after reset) | Pin Type | Alternate Function(s) | Label |
|---|---|---|---|---|
| 63 | VSS | Power | | |
| 64 | VDD | Power | | |

* The pin is affected with an I/O function

# 4. Clock Tree Configuration



# 5. IPs and Middleware Configuration

## 5.1. CRC

**mode: Activated**

### 5.1.1. Parameter Settings:

**Basic Parameters:**

| | |
|---|---|
| Default Polynomial State | Enable |
| Default Init Value State | Enable |

**Advanced Parameters:**

| | |
|---|---|
| Input Data Inversion Mode | None |
| Output Data Inversion Mode | Disable |
| Input Data Format | Bytes |

## 5.2. SYS

**Debug: Serial Wire**

**Timebase Source: SysTick**

## 5.3. TIM1

**Clock Source : Internal Clock**

### 5.3.1. Parameter Settings:

**Counter Settings:**

| | |
|---|---|
| Prescaler (PSC - 16 bits value) | **PSC_2KHZ *** |
| Counter Mode | Up |
| Counter Period (AutoReload Register - 16 bits value ) | **ARR_2HZ *** |
| Internal Clock Division (CKD) | No Division |
| Repetition Counter (RCR - 16 bits value) | 0 |
| auto-reload preload | Disable |

**Trigger Output (TRGO) Parameters:**

| | |
|---|---|
| Master/Slave Mode | Disable (no sync between this TIM (Master) and its Slaves |
| Trigger Event Selection TRGO | Reset (UG bit from TIMx_EGR) |
| Trigger Event Selection TRGO2 | Reset (UG bit from TIMx_EGR) |

## 5.4. TIM2

**Clock Source : Internal Clock**

### 5.4.1. Parameter Settings:

**Counter Settings:**

| | |
|---|---|
| Prescaler (PSC - 16 bits value) | **36000 *** |
| Counter Mode | Up |
| Counter Period (AutoReload Register - 32 bits value ) | **2000 *** |
| Internal Clock Division (CKD) | No Division |
| auto-reload preload | Disable |

**Trigger Output (TRGO) Parameters:**

| | |
|---|---|
| Master/Slave Mode | Disable (no sync between this TIM (Master) and its Slaves |
| Trigger Event Selection TRGO | Reset (UG bit from TIMx_EGR) |

## 5.5. USART2

**Mode: Asynchronous**

### 5.5.1. Parameter Settings:

**Basic Parameters:**

| | |
|---|---|
| Baud Rate | **9600 *** |
| Word Length | **8 Bits (including Parity) *** |
| Parity | None |
| Stop Bits | 1 |

**Advanced Parameters:**

| | |
|---|---|
| Data Direction | Receive and Transmit |
| Over Sampling | 16 Samples |
| Single Sample | Disable |

**Advanced Features:**

| | |
|---|---|
| Auto Baudrate | Disable |
| TX Pin Active Level Inversion | Disable |
| RX Pin Active Level Inversion | Disable |
| Data Inversion | Disable |
| TX and RX Pins Swapping | Disable |

| | |
|---|---|
| Overrun | Enable |
| DMA on RX Error | Enable |
| MSB First | Disable |

*** User modified value**

# 6. System Configuration

## 6.1. GPIO configuration

| IP | Pin | Signal | GPIO mode | GPIO pull/up pull down | Max Speed | User Label |
|---|---|---|---|---|---|---|
| SYS | PA13 | SYS_JTMS-SWDIO | n/a | n/a | n/a | |
| | PA14 | SYS_JTCK-SWCLK | n/a | n/a | n/a | |
| USART2 | PA2 | USART2_TX | Alternate Function Push Pull | Pull up | **High *** | |
| | PA3 | USART2_RX | Alternate Function Push Pull | Pull up | **High *** | |
| GPIO | PA7 | GPIO_Output | Output Push Pull | **Pull down *** | **High *** | Phy_tx_valid |
| | PB0 | GPIO_Output | Output Push Pull | **Pull down *** | **High *** | Phy_tx_data_bus_pin0 |
| | PB1 | GPIO_Output | Output Push Pull | **Pull down *** | **High *** | Phy_tx_data_bus_pin1 |
| | PB2 | GPIO_Output | Output Push Pull | **Pull down *** | **High *** | Phy_tx_data_bus_pin2 |
| | PB10 | GPIO_Input | Input mode | **Pull down *** | **n/a** | Phy_rx_data_bus_pin2 |
| | PB11 | GPIO_Input | Input mode | **Pull down *** | **n/a** | Phy_rx_data_bus_pin3 |
| | PB12 | GPIO_Input | Input mode | **Pull down *** | **n/a** | Phy_rx_data_bus_pin4 |
| | PB13 | GPIO_Input | Input mode | **Pull down *** | **n/a** | Phy_rx_data_bus_pin5 |
| | PB14 | GPIO_Input | Input mode | **Pull down *** | **n/a** | Phy_rx_data_bus_pin6 |
| | PB15 | GPIO_Input | Input mode | **Pull down *** | **n/a** | Phy_rx_data_bus_pin7 |
| | PC6 | GPIO_Input | Input mode | **Pull down *** | **n/a** | Phy_rx_valid |
| | PC7 | GPIO_Input | Input mode | **Pull down *** | **n/a** | Phy_tx_busy |
| | PC8 | GPIO_Input | Input mode | **Pull down *** | **n/a** | Phy_reset |
| | PC9 | GPIO_EXTI9 | **External Interrupt Mode with Rising/Falling edge** | **Pull down *** | **n/a** | Phy_clock |
| | PB3 | GPIO_Output | Output Push Pull | **Pull down *** | **High *** | Phy_tx_data_bus_pin3 |
| | PB4 | GPIO_Output | Output Push Pull | **Pull down *** | **High *** | Phy_tx_data_bus_pin4 |
| | PB5 | GPIO_Output | Output Push Pull | **Pull down *** | **High *** | Phy_tx_data_bus_pin5 |
| | PB6 | GPIO_Output | Output Push Pull | **Pull down *** | **High *** | Phy_tx_data_bus_pin6 |
| | PB7 | GPIO_Output | Output Push Pull | **Pull down *** | **High *** | Phy_tx_data_bus_pin7 |
| | PB8 | GPIO_Input | Input mode | **Pull down *** | **n/a** | Phy_rx_data_bus_pin0 |
| | PB9 | GPIO_Input | Input mode | **Pull down *** | **n/a** | Phy_rx_data_bus_pin1 |

## 6.2. DMA configuration

nothing configured in DMA service

## 6.3. NVIC configuration

| Interrupt Table | Enable | Preenmption Priority | SubPriority |
|---|---|---|---|
| Non maskable interrupt | true | 0 | 0 |
| Hard fault interrupt | true | 0 | 0 |
| Memory management fault | true | 0 | 0 |
| Pre-fetch fault, memory access fault | true | 0 | 0 |
| Undefined instruction or illegal state | true | 0 | 0 |
| System service call via SWI instruction | true | 0 | 0 |
| Debug monitor | true | 0 | 0 |
| Pendable request for system service | true | 0 | 0 |
| System tick timer | true | 0 | 0 |
| EXTI line[9:5] interrupts | true | 0 | 0 |
| TIM1 update and TIM16 interrupts | true | 0 | 0 |
| TIM2 global interrupt | true | 0 | 0 |
| USART2 global interrupt / USART2 wake-up interrupt through EXTI line 26 | true | 0 | 0 |
| PVD interrupt through EXTI line 16 | unused | | |
| Flash global interrupt | unused | | |
| RCC global interrupt | unused | | |
| TIM1 break and TIM15 interrupts | unused | | |
| TIM1 trigger, commutation and TIM17 interrupts | unused | | |
| TIM1 capture compare interrupt | unused | | |
| Floating point unit interrupt | unused | | |

*** User modified value**

# 7. Power Consumption Calculator report

7.1. Microcontroller Selection

| | |
|---|---|
| Series | STM32F3 |
| Line | STM32F303 |
| MCU | STM32F303RETx |
| Datasheet | 026415_Rev4 |

7.2. Parameter Selection

| | |
|---|---|
| Temperature | 25 |
| Vdd | 3.6 |

# 8. Software Project

## 8.1. Project Settings

| Name | Value |
|---|---|
| Project Name | DLL |
| Project Folder | D:\Dropbox\Network1Projects\working lubs\Lab6 Stop&Wait\DLL |
| Toolchain / IDE | MDK-ARM V5 |
| Firmware Package Name and Version | STM32Cube FW_F3 V1.8.0 |

## 8.2. Code Generation Settings

| Name | Value |
|---|---|
| STM32Cube Firmware Library Package | Copy all used libraries into the project folder |
| Generate peripheral initialization as a pair of '.c/.h' files | No |
| Backup previously generated files when re-generating | No |
| Delete previously generated files when not re-generated | Yes |
| Set all free pins as analog (to optimize the power consumption) | No |