Bilkent University
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EEE 313 Electronic Circuit Design Project Report

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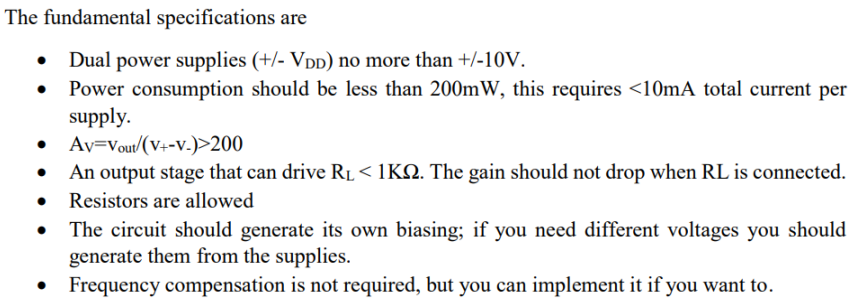
Table of Contents

1. Introduction

The purpose of this project is to design operational amplifier (OPAMP) design featuring self-biasing, differential input, and single-ended output capabilities. Unlike the integrated OPAMPs typically employed in laboratory environments, this design emphasizes core functionalities while satisfying specific performance criteria. The essential specifications entail the utilization of dual power supplies within the range of +/-10V, ensuring a power consumption of under 200mW (<10mA total current per supply), attaining a minimum voltage gain (AV) surpassing 200, incorporating an output stage capable of driving a load resistance (RL) below 1kΩ without compromising gain.



The fundamental specifications are

- Dual power supplies (+/- V_{DD}) no more than +/-10V.
- Power consumption should be less than 200mW, this requires <10mA total current per supply.
- $A_V=v_{out}/(v_+-v_-)>200$
- An output stage that can drive R_L < 1KΩ. The gain should not drop when RL is connected.
- Resistors are allowed
- The circuit should generate its own biasing; if you need different voltages you should generate them from the supplies.
- Frequency compensation is not required, but you can implement it if you want to.

Figure 1: Specifications given in the task

To fulfill these objectives, the central building block employed that we used in this design is a differential amplifier. The differential amplifier amplifies the voltage disparity between two input signals while effectively rejecting common-mode signals. After that, we used the gain stage to obtain the gain and level shift. Then, we used push-pull voltage buffer to get low output impedance.

The proposed circuit was assessed using a test setup where the positive terminal is grounded, R1 and R2 are both 5kΩ resistors, and the observed output voltage (Vout) will mirror the negative of the input voltage (Vin).

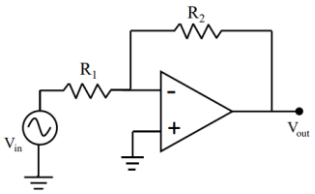


Figure 2: Opamp test circuit given in the task

By adhering to these design specifications, the aim is to develop a simplified yet functional operational amplifier that can be seamlessly applied in various real-world scenarios. The design first tested on the LTSpice simulation, then implemented on the breadboard. After that, using the DipTrace software we implemented our design in PCB.

2. Software Implementation and Analysis

In the software implementation part, the discrete OPAMP meets the given specifications designed. The design consists of three stages: differential amplifier, gain stage and the voltage buffer stage.

2.1. Stage 1: Differential Amplifier with Current Mirror on Top

In this stage, the differential amplifier is designed to remove the effects of common-mode signals and the noise. It also provides gain from voltage differences of the inputs, but the gain obtain in this stage is very small and the actual gain is obtained from the gain stage. The current mirror is designed using two pnp transistors to provide an active load current. This allows the currents passing through the transistors in the differential amplifier stage to be the same.

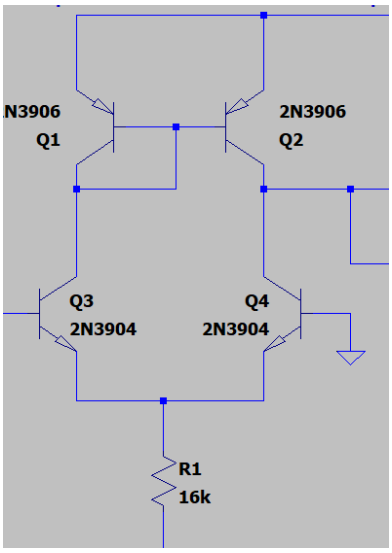


Figure 3: Software implementation of the first stage

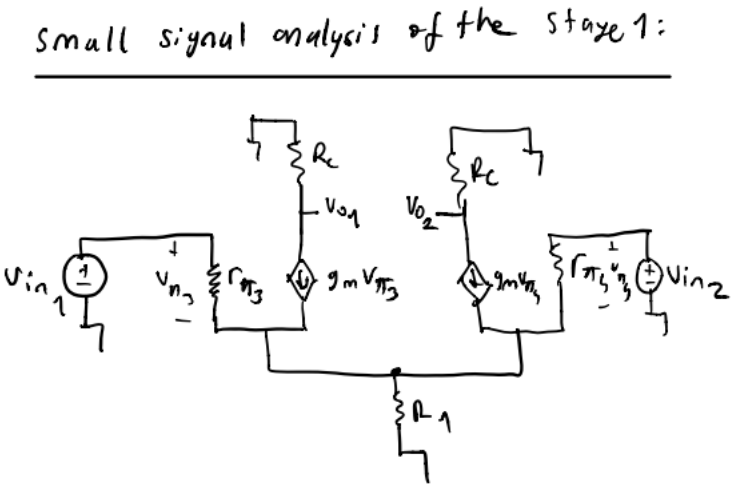


Figure 4: Small signal analysis of the first stage differential amplifier

Let Vin1 = Vcm + Vd/2 and Vin2 = Vcm – Vd/2, (eq. 1)

Use half circuits method to the differential gain:

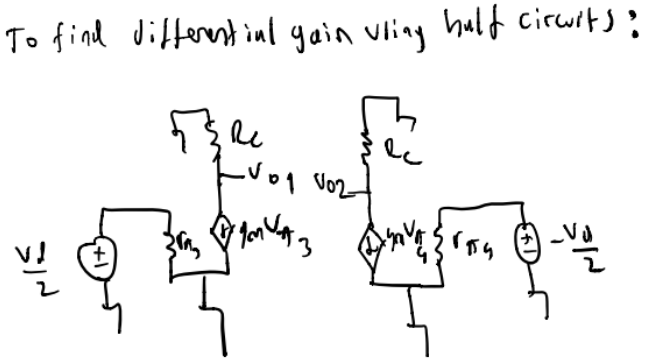


Figure 5: Analysis of the differential amplifier using half circuits

$$V_{o1} = -g_m V_{\pi 3} R_c \text{ (eq.2)}$$

$$V_{\pi 3} = Vd/2 \text{ (eq.3)}$$

$$\frac{V_{o1}}{Vd} = \frac{-g_m R_c}{2} \text{ (eq.4)}$$

From symmetry, $$\frac{V_{o2}}{Vd} = \frac{g_m R_c}{2} \text{ (eq. 5)}$$

Hence, the differential gain: $\frac{V_{o2} - V_{o1}}{Vd} = -g_m R_c$ (eq.6)

2.2 Stage 2: The Gain Stage (Common Emitter Amplifier)

In this stage, the common emitter amplifier is used to obtain the gain of the amplifier. Furthermore, this stage acts like a level shifter as well. The gain of the amplifier is adjusted to be more than 200 given in the specifications. The purpose of the capacitor is frequency compensation.

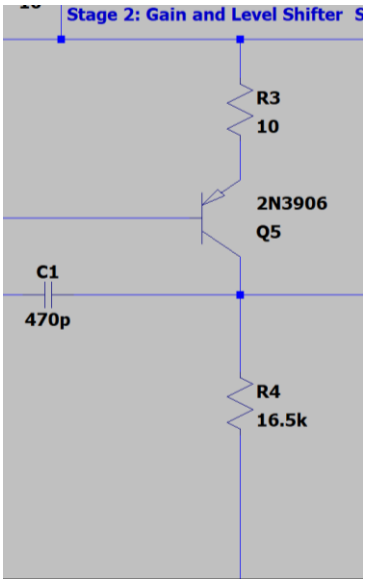


Figure 6: Software implementation of the second stage

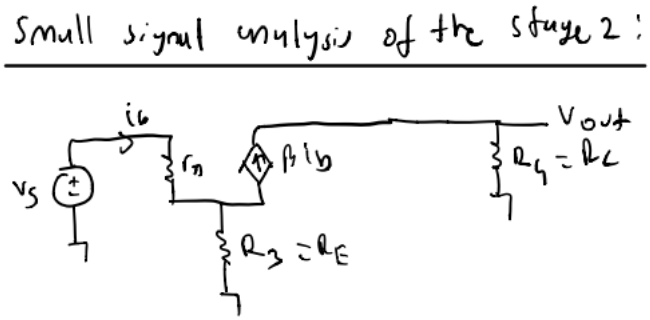


Figure 7: Small signal analysis of the stage 2

Assume Early voltage is infinite so the transistor output resistance (r_0) neglected.

$$V_{out} = \beta i_b R_4 \text{ (eq.7)}$$

$$V_s = \beta i_b r_\pi + (1+\beta) i_b R_3 \text{ (eq.8)}$$

$$\frac{V_{out}}{V_s} = \frac{\beta R_4}{r_\pi + (1+\beta)R_3} \; since \; (1+\beta)R_3 \gg r_\pi \text{ (eq.9)}$$

$$\frac{V_{out}}{V_s} = \frac{R_4}{R_3} \; approximately \text{ (eq. 10)}$$

2.3 Stage 3: Push-Pull Voltage Buffer

The purpose of the push-pull voltage buffer section is to transfer the gain with decreasing the output impedance. This stage creates a low impedance, which enables the circuit to use a wide range of load resistance. It helps the circuit to meet the specification "The gain should not drop when RL < 1k connected."

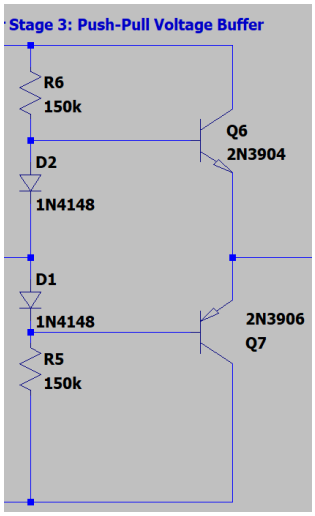


Figure 8: Software Implementation of the third stage

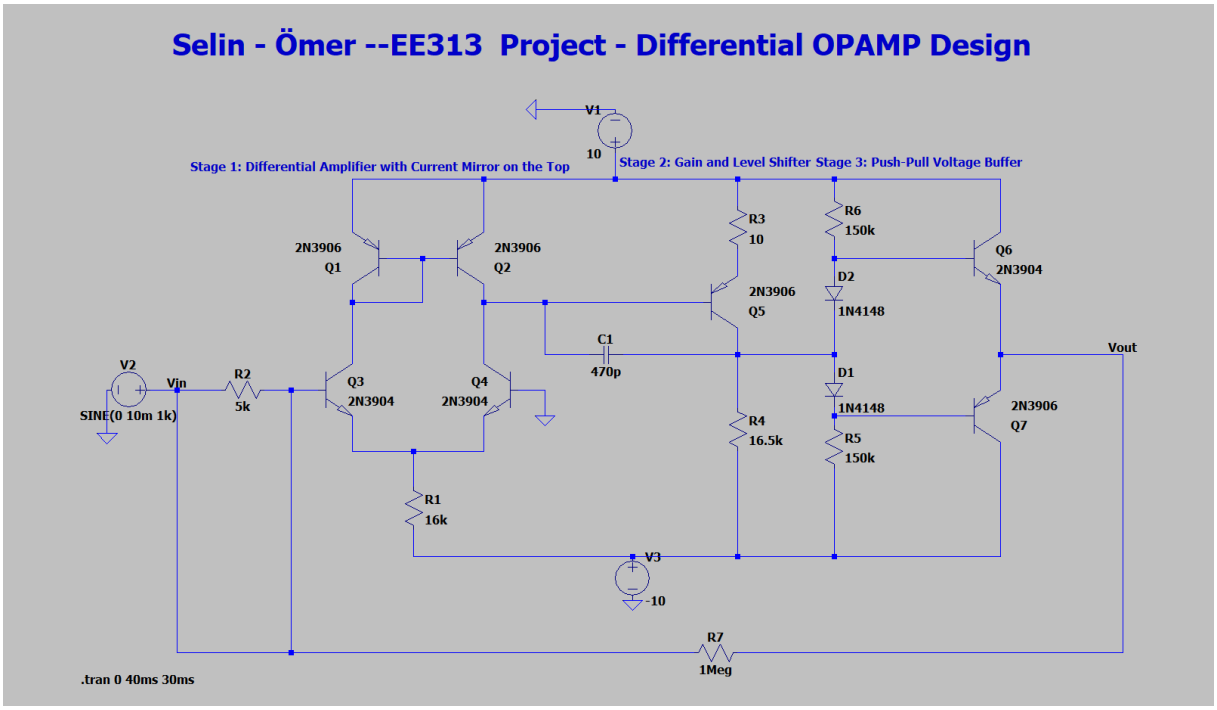


Figure 9: Software Implementation of the Open Loop Gain circuit

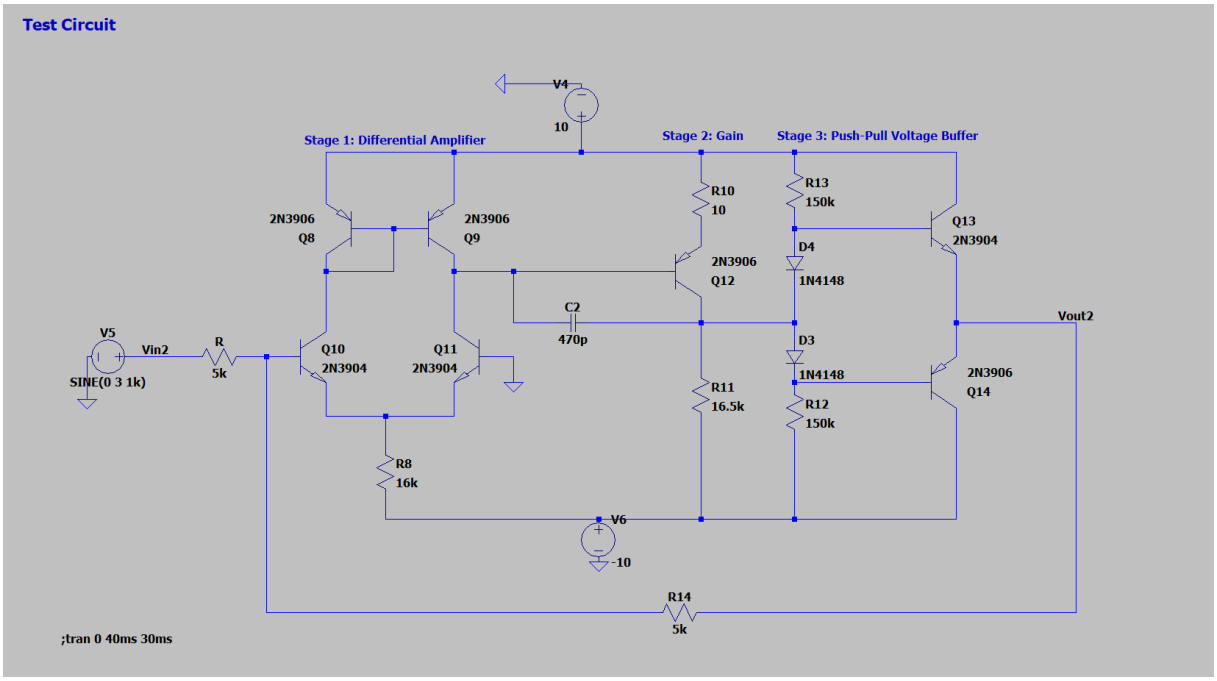


Figure 10: Software Implementation of the Test Circuit

The overall circuit design meets the specifications in the task. The differential amplifier has a very small gain found in equation 6, which appears to be around 2.8 and used to eliminate the common node noise. As stated above, the gain and the level shift are obtained from the stage 2 with the equation 10. Hence, the gain is found in this stage as 1650. The third stage provides low input impedance but decreases the gain around 0.8. Hence, we combine the gains from each stage and find the overall gain as 3696 and it is consistent with gain we measured at the simulation.

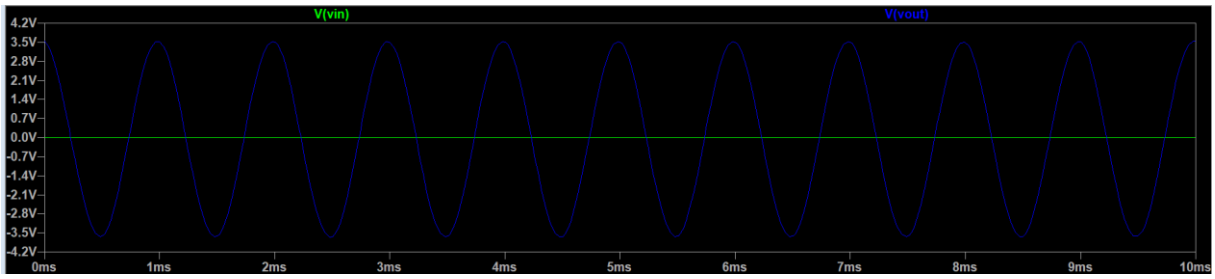


Figure 11: Output waveform when Vin = 1mV

The open loop gain is measured as 3500, which is larger than 200 given in the specifications.

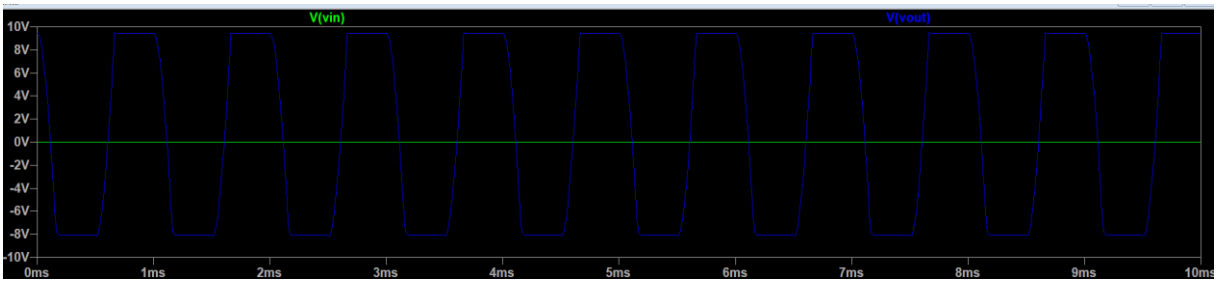


Figure 12: Output waveform when Vin = 10mV

We are feeding the OPAMP with +10V and -10V voltages, so output becomes saturated after +10V and -10V.

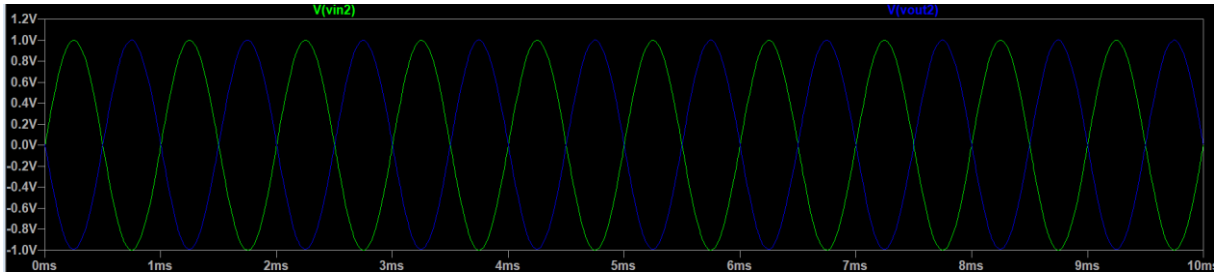


Figure 13: Output waveform of the test circuit when Vin = 1Vpp

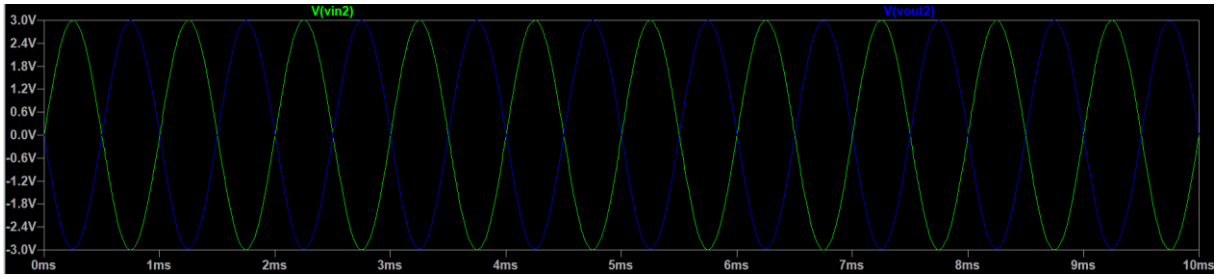


Figure 14: Output waveform of the test circuit when Vin = 3Vpp

The test circuit results with two different values shows that the OPAMP is working properly with providing -1 gain.

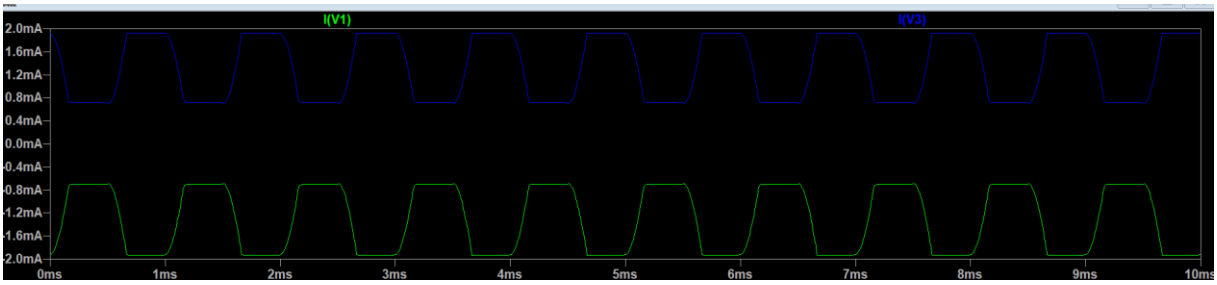


Figure 15: Current passes through voltage supplies

As stated in the task specifications, the current drawn from each supplies is smaller than 10mA.

3. Hardware Implementation and Analysis

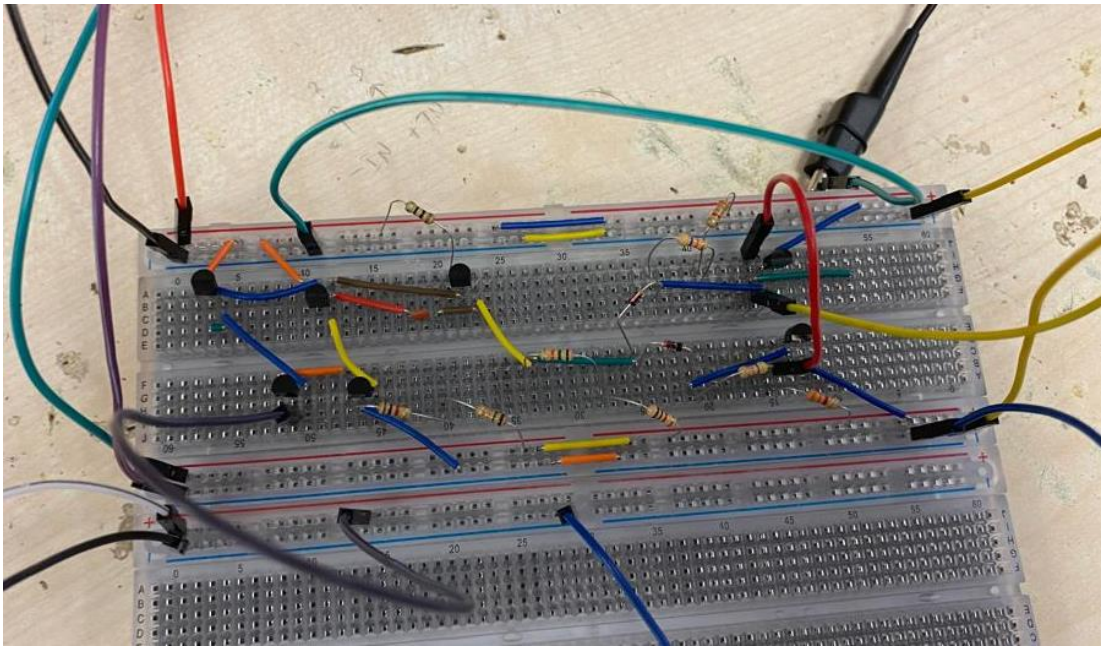


Figure 16: Breadboard implementation of the Open Loop Gain circuit

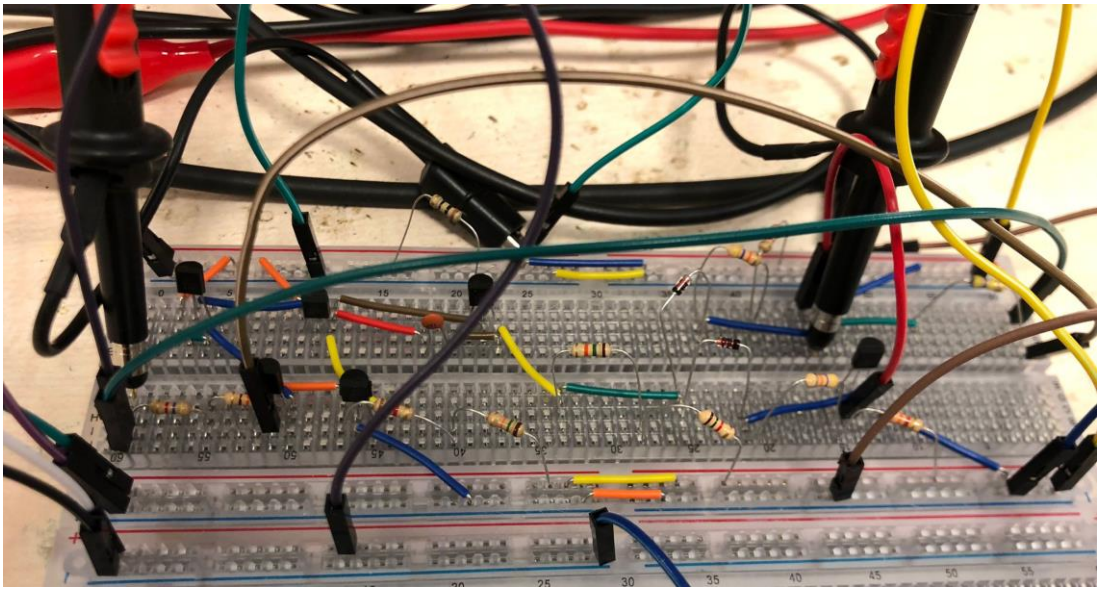


Figure 17: Breadboard implementation of the test circuit

We implemented our OPAMP design in breadboard to measure the open loop gain and the test circuit.

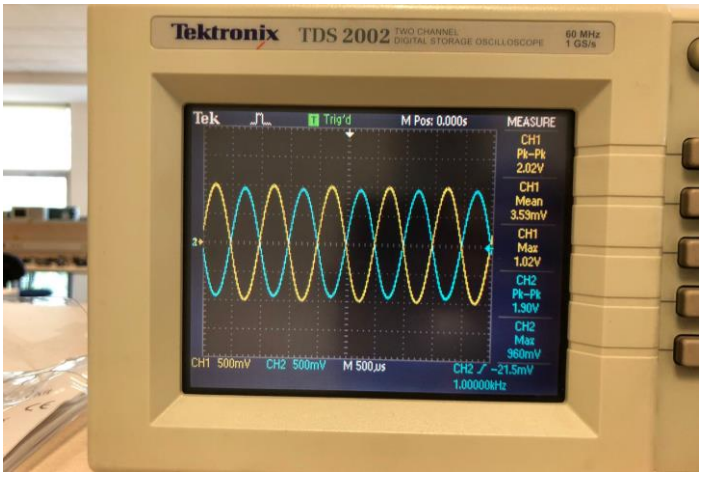


Figure 18: Output of the test circuit when Vin = 2Vpp

The test circuit provides -1 gain, shows that design working properly.

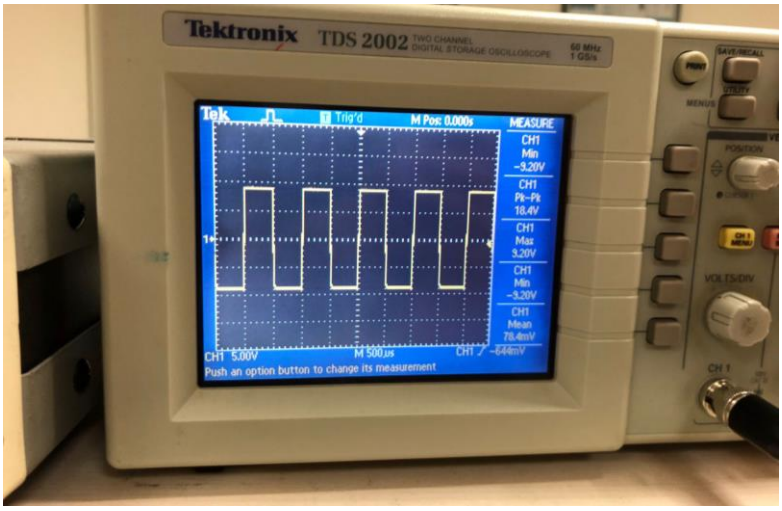


Figure 19: Output of the open loop gain when Vin = 10mVpp

The output gets saturated since it exceeds 10V and clipped above and below.

4. PCB Design and Implementation

First, the schematic of the design is created using the DipTrace schematic tool.

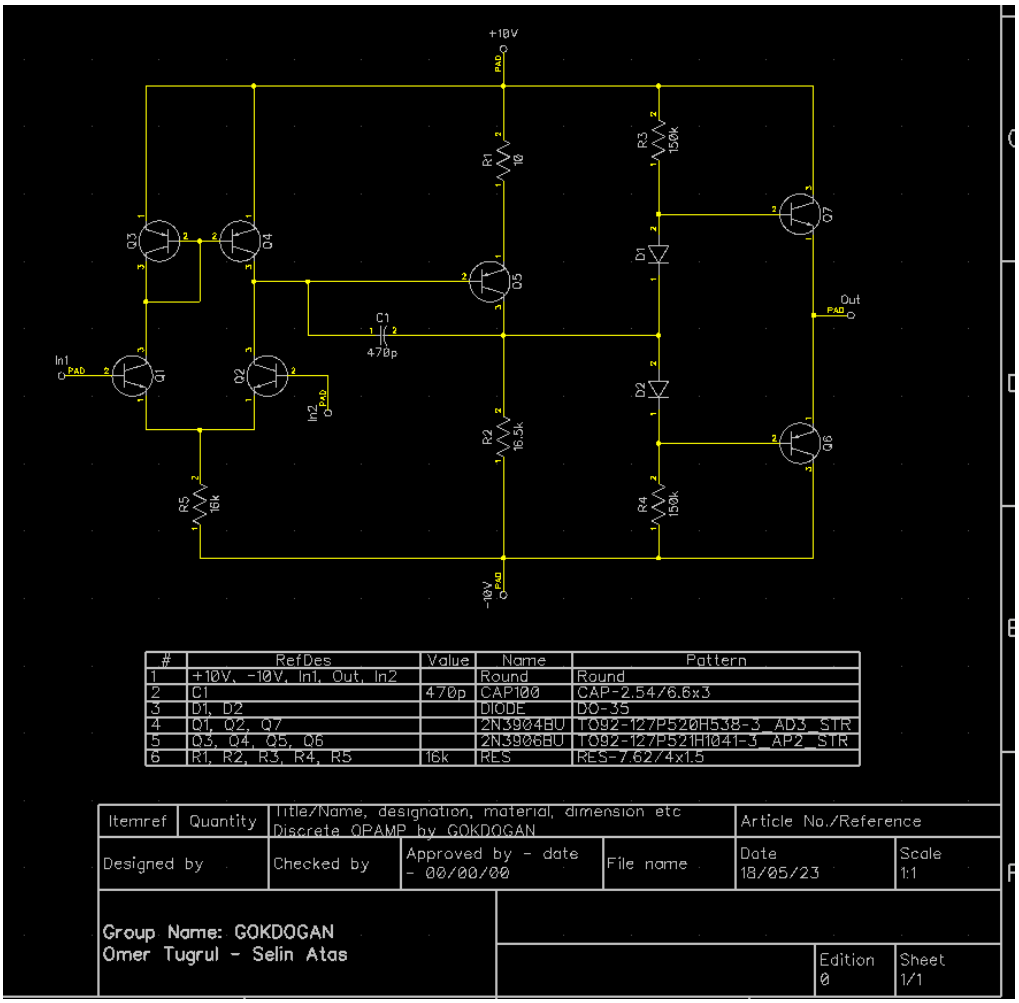


Figure 20: Schematic design using DipTrace software

Then, the PCB layout of the circuit is designed using the DipTrace PCB tool. After the design, the gerber files of the design are created and sent to the production.

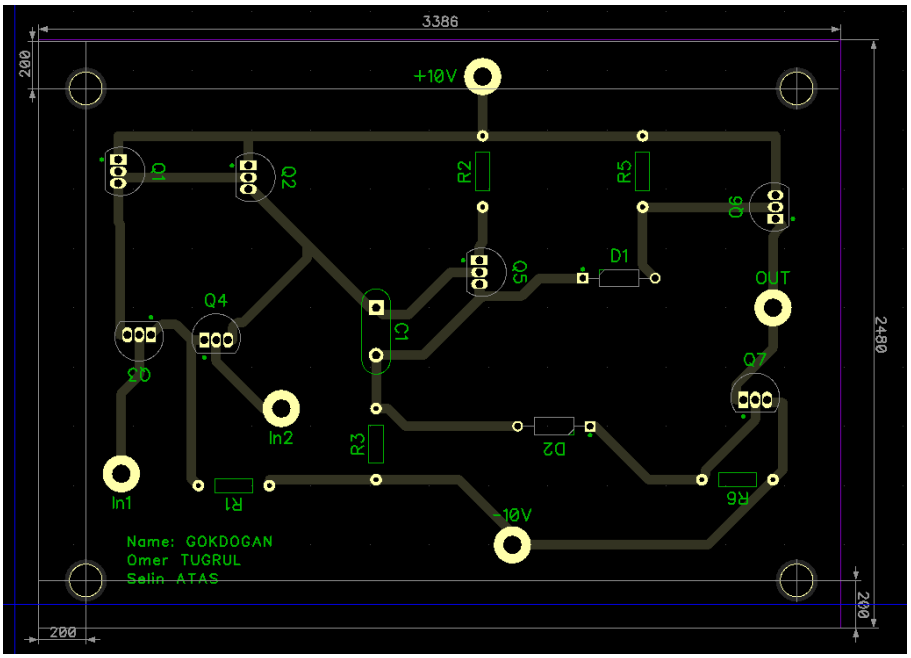


Figure 21: PCB layout design using DipTrace software

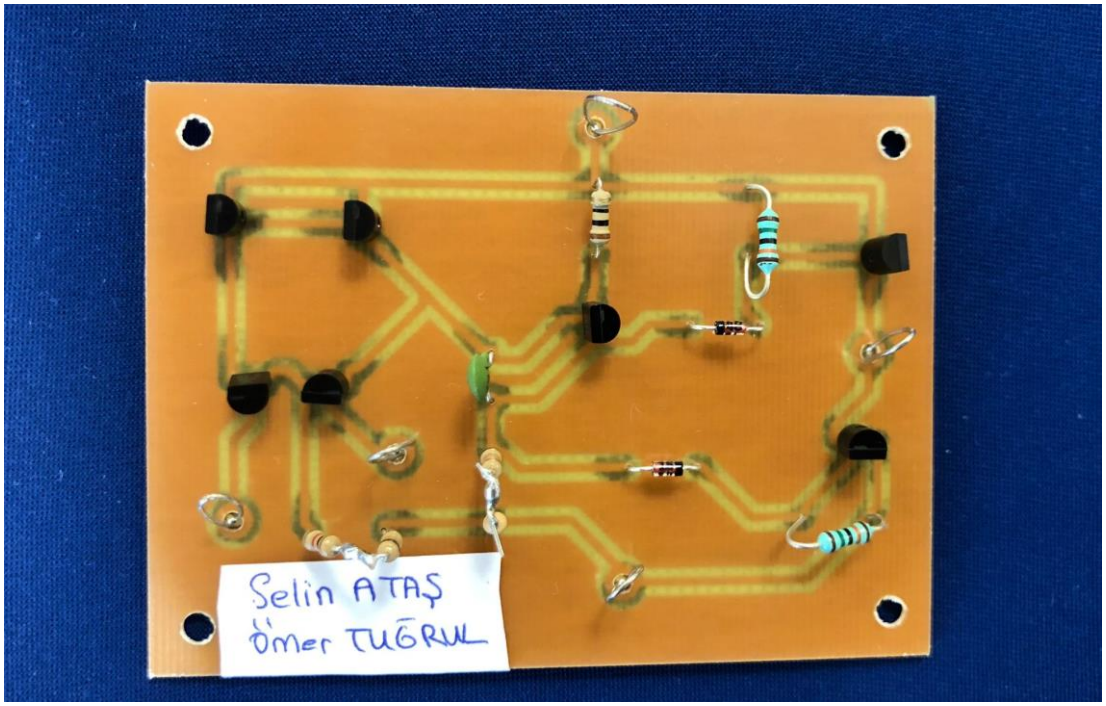


Figure 22: PCB implementation with the soldered components

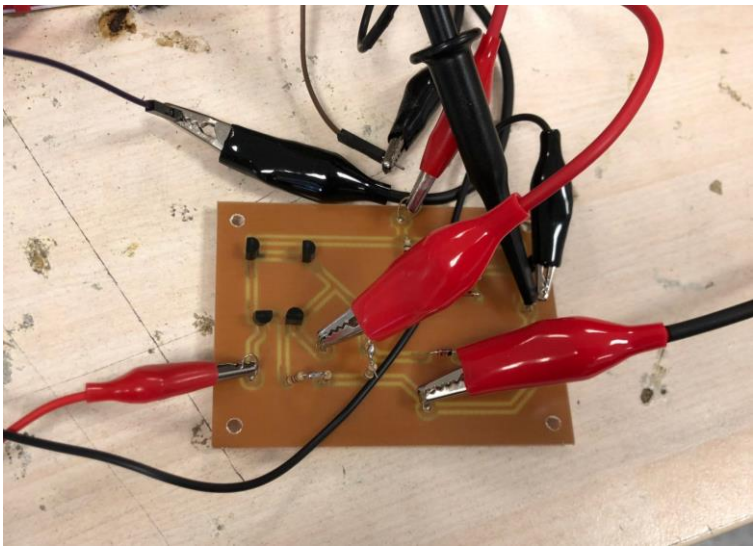


Figure 23: PCB implementation of the open loop gain circuit

The open loop gain is measured using the PCB board.

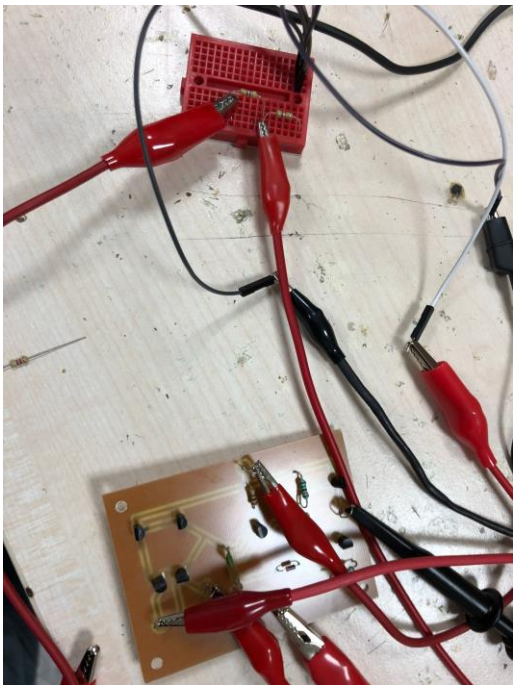


Figure 24: PCB implementation of the test circuit

The 5kΩ resistors are used to implement the test circuit.

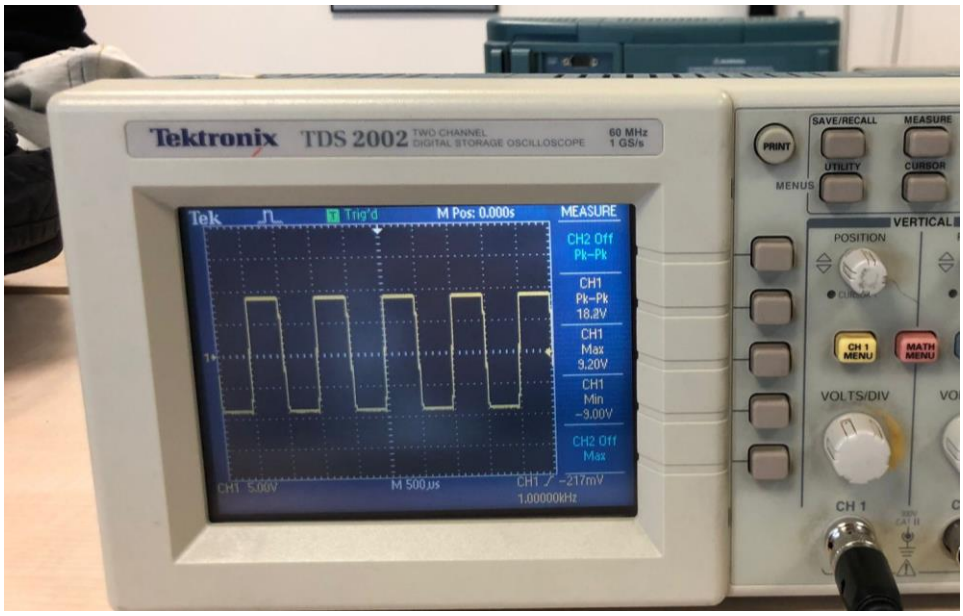


Figure 25: Output of the open loop gain circuit when Vin = 10mV

The open gain is measured, and the saturation is observed, since it exceeds 10V. Also, the perfect level shift is observed.

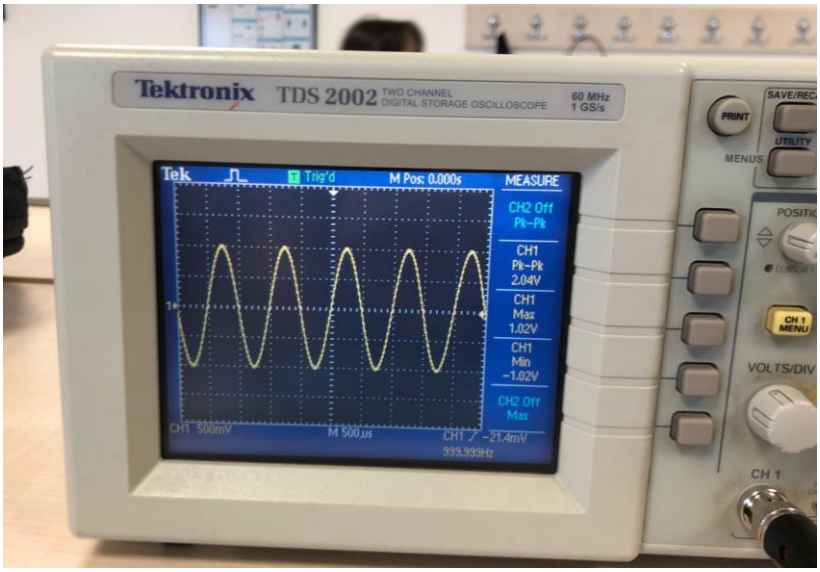


Figure 26: Output of the test circuit when Vin = 2Vpp

When we give 2Vpp to the test circuit, we observed 2Vpp at the output.

Figure 27: Current passess through voltage supply

The current through voltage supplies are measured and it is observed that it does not exceed 10mA.

Hence, the PCB implementation worked properly as expected.

5. Conclusion

In conclusion, we successfully designed and implemented a discrete operational amplifier (OPAMP) with self-biasing, differential input, and single-ended output capabilities. The design adhered to the given specifications, which included the utilization of dual power supplies within the range of +/-10V, a power consumption of less than 200mW (<10mA total current per supply), a minimum voltage gain (AV) exceeding 200, and an output stage capable of driving a load resistance (RL) below 1kΩ without compromising gain.

The design incorporated three key stages: a differential amplifier with a current mirror, a gain stage employing a common emitter amplifier, and a push-pull voltage buffer stage. Each stage contributed to achieving the desired functionality and performance. The differential amplifier provided noise rejection and a small gain, while the gain stage delivered the amplification and level shifting. The push-pull voltage buffer ensured a low output impedance and facilitated driving a wide range of load resistances.

LTSpice simulation, breadboard implementation, and PCB implementation were performed to validate the design. The simulation results exhibited a gain of 3500, surpassing the minimum requirement of 200. We cannot observe the 3500 gain in the breadboard and the PCB implementation, because we cannot give the 1mV input and the output exceeds the 10V and gets saturated. There were more errors in the breadboard implementation then the PCB implementation since it has connection issues arise from breadboard. However, the breadboard implementation and PCB implementation confirmed the successful operation of the design, with the output accurately reflecting the negative of the input voltage in the test circuit. The current drawn from each power supply remained below 10mA, aligning with the specified power consumption limit.

Overall, our designed discrete OPAMP fulfilled the project objectives.