(b) The results are shown in the following two tables; the first table corresponds direct mapping and the second two-way set-associative mapping. In each table, arrow connecting the same block numbers indicates that the corresponding acc takes more than one cycle due to read/write misses or bus contention. In any ca at most 3 cycles are required to complete an access in the case of a read/write m coupled with bus contention. The subscript associated with a block indicates t state of that block (R for read-only, and W for read-write.)

	cycle	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
	block trace	0 → 0		**0**	0	**1 → 1**		1	4 → 4		3 → 3		3	5	→	5	**5**	5
	frame 0	—	0_R	0_W	0_W	0_W	0_R	0_R	—	4_R	4_R	4_R	4_R	4_R	4_R	4_R	4_R	4_R
	frame 1	—	—	—	—	—	1_W	1_W	1_W	1_W	1_W	1_W	1_W	—	—	5_R	5_W	5_W
P1	frame 2	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	frame 3	—	—	—	—	—	—	—	—	—	—	3_R	3_R	3_R	3_R	3_R	3_R	3_R
	cache miss	*				*			*		*			*				
	bus in use	*		*		*			*		*			*	*		*	

	block trace	2	→	2	**2**	0	→	0	0	**7 → 7**		5 → 5		5	5	**7**	7	0
	frame 0	—	—	—	—	—	—	0_R	0_R	0_R	0_R	0_R	0_R	0_R	0_R	0_R	0_R	0_R
	frame 1	—	—	—	—	—	—	—	—	—	—	—	5_R	5_R	5_R	5_R	—	—
P2	frame 2	—	—	2_R	2_W	2_W	2_W	2_W	2_W	2_W	2_W	2_W	2_W	2_W	2_W	2_W	2_W	2_W
	frame 3	—	—	—	—	—	—	—	—	—	7_W	7_W	7_W	7_W	7_W	7_W	7_W	7_W
	cache miss	*				*				*		*						
	bus in use		*		*		*			*		*				*		

	cycle	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
	block trace	0 → 0		**0**	0	**1 → 1**		1	4 → 4		3 → 3		3	5	→	5	**5**	5
	frame 0	—	0_R	0_W	0_W	0_W	0_R	0_R	0_R	0_R	0_R	0_R	0_R	0_R	0_R	0_R	0_R	0_R
	frame 1	—	—	—	—	—	—	—	—	4_R	4_R	4_R	4_R	4_R	4_R	4_R	4_R	4_R
P1	frame 2	—	—	—	—	—	1_W	1_W	1_W	1_W	1_W	1_W	1_W	—	—	5_R	5_W	5_W
	frame 3	—	—	—	—	—	—	—	—	—	—	3_R	3_R	3_R	3_R	3_R	3_R	3_R
	cache miss	*				*			*		*			*				
	bus in use	*		*		*			*		*			*	*		*	

	block trace	2	→	2	**2**	0	→	0	0	**7 → 7**		5 → 5		5	5	**7**	7	0
	frame 0	—	—	2_R	2_W	2_W	2_W	2_W	2_W	2_W	2_W	2_W	2_W	2_W	2_W	2_W	2_W	2_W
	frame 1	—	—	—	—	—	—	0_R	0_R	0_R	0_R	0_R	0_R	0_R	0_R	0_R	0_R	0_R
P2	frame 2	—	—	—	—	—	—	—	—	—	7_W	7_W	7_W	7_W	7_W	7_W	7_W	7_W
	frame 3	—	—	—	—	—	—	—	—	—	—	—	5_R	5_R	5_R	5_R	—	—
	cache miss	*				*				*		*						
	bus in use		*		*		*			*		*				*		

For the given page reference patterns, the hit ratio is 6/11 for P1 and 7/11 for P2 with either cache organization. The major difference is the contents of block frames in the caches due to different ways of mapping between memory and cache. As can be seen, a memory block can possibly reside in more cache block frames with the set-associative organization, which generally improves hit ratio.