CSE 531
Homework-2

1. A $\sqrt{p} \times \sqrt{p}$ ***reconfigurable mesh*** consists of a $\sqrt{p} \times \sqrt{p}$ array of processors connected to a grid-shaped reconfigurable broadcast bus. A 4 x 4 re-configurable mesh is shown in Figure 1. Each processor has locally-controllable bus switches. The internal connections among the four ports, north (N), east (E), west (W), and south (S), of a processor can be configured during the execution of an algorithm. Note that there are 15 connection patterns. For example, {SW, EN} represents the configuration in which port S is connected to port W and port N is connected to port E. Each bit of the bus carries one of *1-signal* or *0-signal* at any time. The switches allow the broadcast bus to be divided into subbuses, providing smaller reconfigurable meshes. For a given set of switch settings, a ***subbus*** is a maximally-connected subset of the processors. Other than the buses and the switches, the reconfigurable mesh is similar to the standard two-dimensional mesh. Assume that only one processor is allowed to broadcast on a ***subbus*** shared by multiple processors at any time.

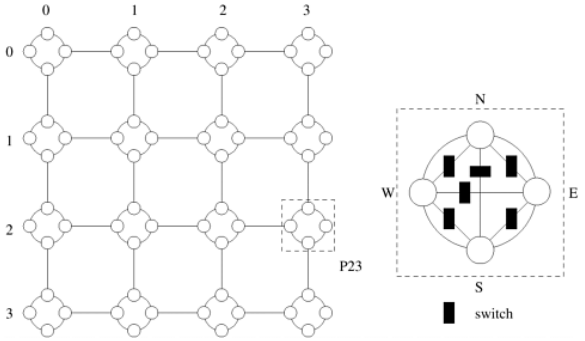

Figure 1. Switch connection patterns in a reconfigurable mesh.

Determine the bisection width, the diameter, and the number of switching elements and communication links for a reconfigurable mesh of $\sqrt{p} \times \sqrt{p}$ processors. What are the advantages and disadvantages of a reconfigurable mesh as compared to a wraparound mesh?

2. A ***mesh of trees*** is a network that imposes a tree interconnection on a grid of processors. A $\sqrt{p} \times \sqrt{p}$ mesh of trees is constructed as follows. Starting with a $\sqrt{p} \times \sqrt{p}$ grid of processors a complete binary tree is imposed on each row of the grid. Then a complete binary tree is imposed on each column of the grid. Figure 2 illustrates the construction of a 4 x 4 mesh of trees. Assume that the nodes at intermediate levels are switching elements. Determine the bisection width, diameter, and total number of switching elements in a $\sqrt{p} \times \sqrt{p}$ mesh of processors.

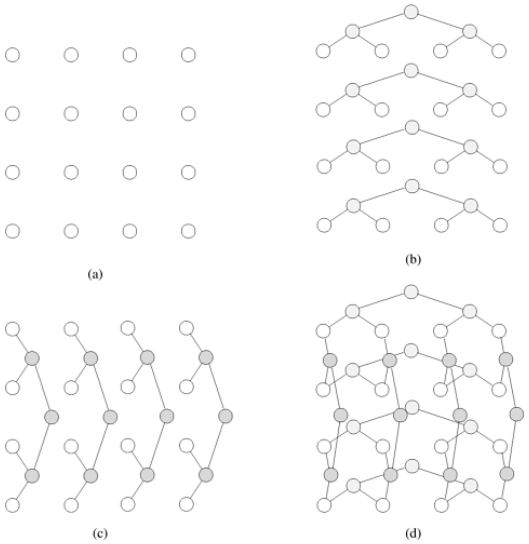

Figure 2. The construction of a 4 x 4 mesh of trees: (a) a 4 x 4 grid, (b) complete binary trees imposed over individual rows, (c) complete binary trees imposed over each column, and (d) the complete 4 x 4 mesh of trees.