1. Description:

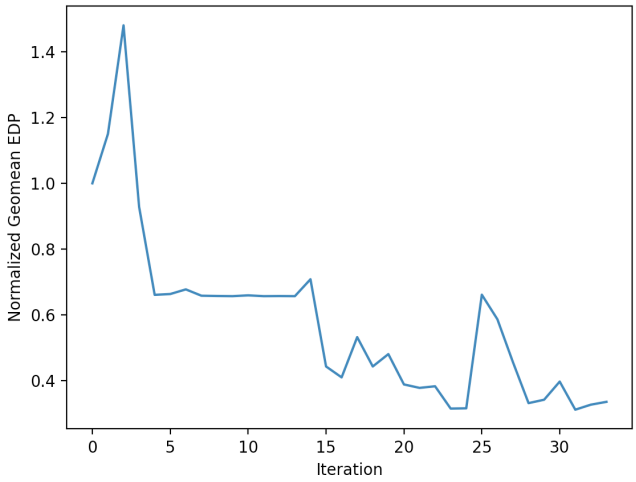
We are able to simulate different tasks on a simulator with different configurations of the hardware spanning multiple dimensions. Simulations on these different configurations allow us to do Design Space Exploration.

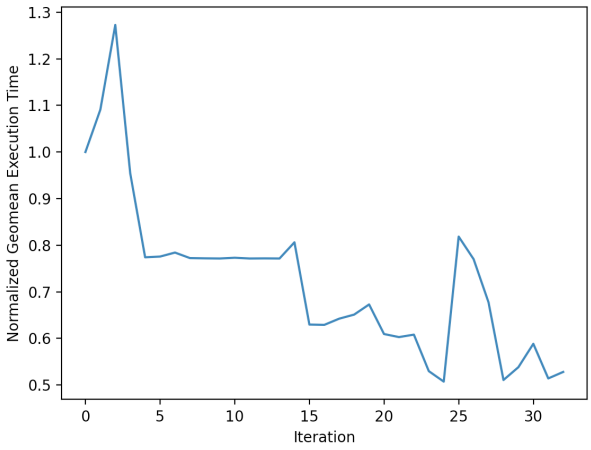
2. Efficiency: Iter # 32 config: 1 0 1 3 0 6 1 2 3 2 0 0 4 3 3 1 6 6
   Performance: Iter # 27 config: 2 0 2 2 0 6 0 2 3 1 0 1 1 2 0 1 5 4
3.

Param	EDP	Performance
Width	2 Energyis a balance of IP utilization.	4 The more we IP we have, the faster we are, but there are cache block_size limitations.
Scheduling	Inorder, Able to be more planned and energy efficient.	Inorder Quite surprising tbh
L1 block	16 Small-medium size is more power safe	32 Medium size is more performant without suffering from big block size.
dl1sets	256 Storing the data more saves power without cache misses.	128 Medium size cache makes it both fast and low missrate.
dl1assoc	1 Associativtiy is not helpful energy wise.	1 Associativtiy is not helpful performance wise.
il1sets	2KB This is the sweet spot both for energy and performance.	2KB This is the sweet spot both for energy and performance.
il1assoc	2 IL associtivity is more energy save	1 IL associativity is not performant.
ul2sets	1K This is the sweet spot both for performance and energy.	1K This is the sweet spot both for performance and energy.

ul2block	128 Bigger block size in L2 is good for both energy and performance.	128 Bigger block size in L2 is good for both energy and performance.
ul2assoc	4 Assoc is more helpful on L2, and it is more helpful to energy efficiency.	2 Assoc is more helpful on L2, and it is more helpful to energy efficiency.

4.





5. Testing each combination of connected/related dimensions. Ie. Cache dimensions. Using the current approach, we first decide on a BlockSize, after that we test other Cache dimensions for a fixed block size.
6. a. Dependence of hardware configurations
   b. Interesting heuristics on simulation