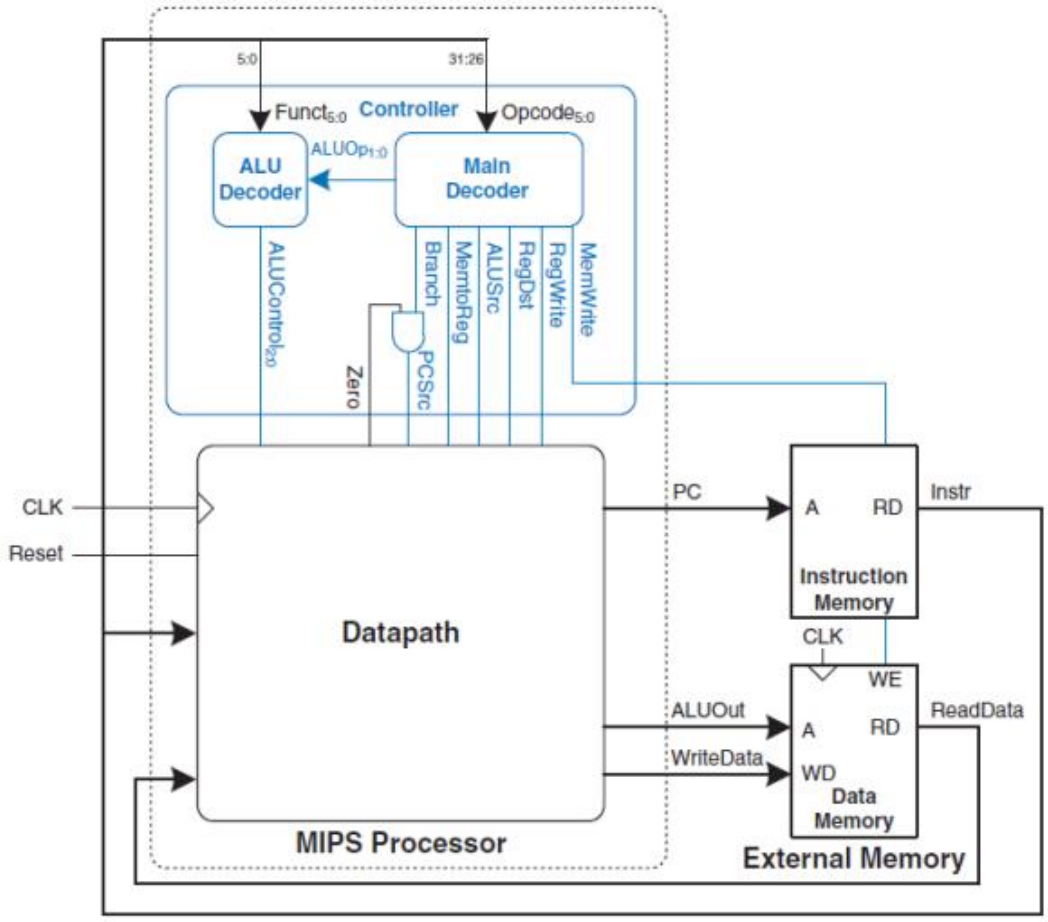
Lab 3(SCP datapath)

Deadline: 02.12.2023 – 23:59

In this lab, you will build datapaths of a MIPS single cycle processor (SCP) using system Verilog in Edaplayground or Modelsim. I recommend you to use EDAplayground which can be accessed from www. Edaplayground.com . You need to create an account to use it. It is all free. You can also view the systemverilog tutorial placed in LMS. Lets say a processor is supposed to support following instructions. addi, add, sub, and, or, lw, sw, beq, and j Write a system Verilog module for the datapath of MIPS SCP. The module MUST be named as “datapath”. The skeleton for required module containing the port list of the datapath, as shown in the figure below, is given in file named, “datapath.sv”. You are required to complete the module and submit it. After completing the datapath module you can run the testbench provided in file named “tbDataPath.sv”. HINT: systemVerilog modules for basic building blocks, needed for constructing the datapath, are given in the text book. You are supposed to study them on your own and use them as needed. Submitting your work: Place all your datapath.sv file in a SINGLE folder, name it as StudentName_ID_Lab3, compress it and upload to the LMS.


5:0
31:26
Funct5:0
Controller
Opcode5:0
ALU Decoder
ALUOp1:0
Main Decoder
ALUControl2:0
Branch
MemtoReg
ALUSrc
RegDst
RegWrite
MemWrite
Zero
PCSrc
CLK
Reset
Datapath
MIPS Processor
PC
A
RD
Instr
Instruction Memory
CLK
WE
ALUOut
A
RD
ReadData
WriteData
WD
Data Memory
External Memory