CSE3038 PROGRAMMING PROJECT 2
Due: 20 / 05 / 2024

In this project, you are required to extend the MIPS single-cycle implementation by implementing additional instructions. You will use ModelSim simulator [1] to develop and test your code. You are required to implement your assigned **6 instructions** (selected from following 22 instructions). *Note that your set of **6 instructions** will be emailed to you or your group member.*

R-format (6): brv, brnv, balrv, balrnv, jmxor, jmnor
I-format (13): nori, xori, andi, ori, nandi, bgtzal, bgezal, bltzal, blezal, jsp, jspal, jalpc, jrsal
J-format (3): baln, balz, balv

You must design the revised single-cycle datapath and revised control units which make a processor that executes your instructions as well as the instructions implemented already in the design. After designing the new enhanced processor, you will implement it in Verilog HDL.

Specifications of New Instructions

	Instr	Type	Code	Syntax	Meaning
1	brv	R-type	funct=20	brv $rs	if Status [V] = 1, branches to address found in register $rs.
2	brnv	R-type	funct=21	brnv $rs	if Status [V] = 0, branches to address found in register $rs.
3	balrv	R-type	funct=22	balrv $rs, $rd	if Status [V] = 1, branches to address found in register $rs, link address is stored in $rd (which defaults to 31)
4	balrnv	R-type	funct=23	balrnv $rs, $rd	if Status [V] = 0, branches to address found in register $rs, link address is stored in $rd (which defaults to 31)
5	jmxor	R-type	funct=34	jmxor $rs,$rt	jumps to address found in memory [$rs XOR $rt], link address is stored in $31
6	jmnor	R-type	funct=37	jmnor $rs,$rt	jumps to address found in memory [$rs NOR $rt], link address is stored in $31
7	nandi	I-type	opcode=16	nandi $rt, $rs, Label	Put the logical NAND of register $rs and the zero- extended immediate into register $rt.
8	xori	I-type	opcode=14	xori $rt, $rs, Label	Put the logical XOR of register $rs and the zero- extended immediate into register $rt.
9	andi	I-type	opcode=12	andi $rt, $rs, Label	Put the logical AND of register $rs and the zero- extended immediate into register $rt.
10	ori	I-type	opcode=13	ori $rt, $rs, Label	Put the logical OR of register $rs and the zero-extended immediate into register $rt.
11	nori	I-type	opcode=15	nori $rt, $rs, Label	Put the logical NOR of register $rs and the zero-extended immediate into register $rt.
12	bgtzal	I-type	opcode=33	bgtzal $rs, Label	if R[rs] >0, branch to PC-relative address (formed as beq & bne do), link address is stored in register 25.
13	bgezal	I-type	opcode=35	bgezal $rs, Label	if R[rs] >= 0, branch to PC-relative address (formed as beq & bne do), link address is stored in register 25.
14	bltzal	I-type	opcode=34	bltzal $rs, Label	if R[rs] < 0, branch to to PC-relative address (formed as beq & bne do), link address is stored in register 25.
15	blezal	I-type	opcode=36	blezal $rs, Label	if R[rs] <= 0, branch to to PC-relative address (formed as beq & bne do), link address is stored in register 25.
16	jsp	I-type	opcode=18	jsp	jumps to address found in memory where the memory address is written in register 29 ($sp).

17	jspal	I-type	opcode=19 jspal		jumps to address found in memory where the memory address is written in register 29 ($sp) and link address is stored in memory (DataMemory[Register[29]]).
18	jalpc	I-type	opcode=31	jalpc $rt, Target	jumps to PC-relative address (formed as beq and bne do), link address is stored in $rt
19	jrsal	I-type	opcode=17 jrsal	$rs	jumps to address found in memory where the memory address is written in register $rs and link address is stored in memory (DataMemory[$rs]).
20	baln	J-type	opcode=27 baln Target		if Status [N] = 1, branches to pseudo-direct address (formed as jal does), link address is stored in register 31
21	balz	J-type	opcode=26 balz Target		if Status [Z] = 1, branches to pseudo-direct address formed as jal does), link address is stored in register 31
22	balv	J-type	opcode=32	balv Target	if Status [V] = 1, branches to pseudo-direct address (formed as jal does), link address is stored in register 31

Status Register

Some of the conditional branches test the Z and N bits in the Status register. So the MIPS datapath will need to have a Status register, with the following 3 bits: Z (if the ALU result is zero) , N (if the ALU result is negative) or V (if the ALU result causes overflow). The Status register will be loaded with the ALU results each clock cycle.

Requirements

- You will implement only 6 instructions. The instructions are sent via email to your group members.
- Your design should support all your 6 instructions without corrupting other MIPS instructions.
- You can print out single-cycle datapath and start your design on a paper. Then you can continue with the Verilog implementation.
- A demo session will be scheduled in the following week of the submission. I request you to bring these design papers within you in demo sessions.
- **You have to prepare a simulation of your instructions for the demo (including *register file*, *data memory* and *instruction memory*)!**
- You have to do your projects in Verilog with using ModelSim simulator.
- You are allowed to use only the source codes in the attached. You cannot take any other implementations.
- You **will not** submit 6 different implementations. There should be only a single implementation supporting all 6 instructions that are assigned to your group.
- You are required to submit a minimum 2-pages report explaining implementation details of your project and commented code (via Canvas). Your report should include example runs for each instruction. Your implementation detail should be provided in the source code comment. All the files should be submitted as a single zip file. You should use your surnames as the name of the file: *surname1_surname2_surname3_surname4_project2.zip*

CSE 3038 – Computer Organization **Spring 2024**
Prof. Haluk Topcuoğlu

General Policies

- *You are allowed to work in groups of 3 or 4 members. Group members may get different grades.*
- *It is NOT acceptable to copy (or start your) solutions from Web. In case of any forms of cheating or copying, the penalties will be severe.* ***Both Giver and Receiver are equally culpable and suffer equal penalties.***
- There will be demo session for this assignment. If you cannot answer the questions about your project details in the demo section, even if you have done all the parts completely, you will not get points!
- ***No late submission will be accepted!***

[1] https://www.intel.com/content/www/us/en/software/programmable/quartus-prime/model-sim.html