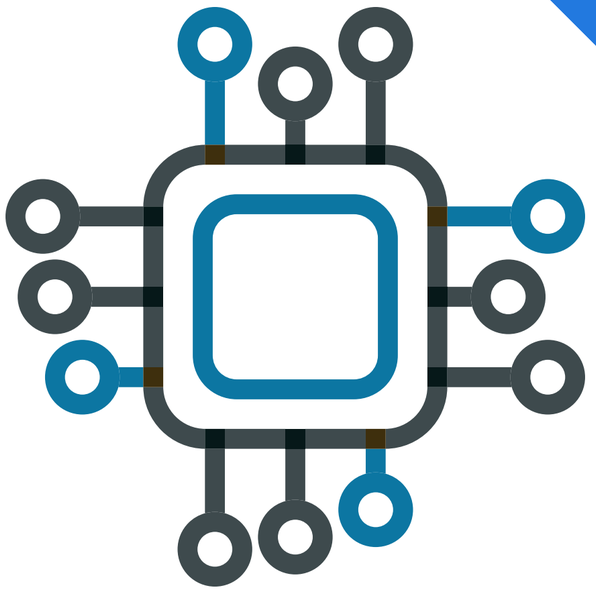
RISC ARCHITECTURE BASED 8 BITS COMPUTER DESIGN AND IMPLEMENTATION ON FPGA USING VHDL



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What Is The Aim?

to design a computer for low power and low cost application and to implement on a FPGA

- Based on 8 bit registers
- RISC ISA - 16 bit instruction - (37 Instructions)
- R-I-S-B-J Type Instruction Types

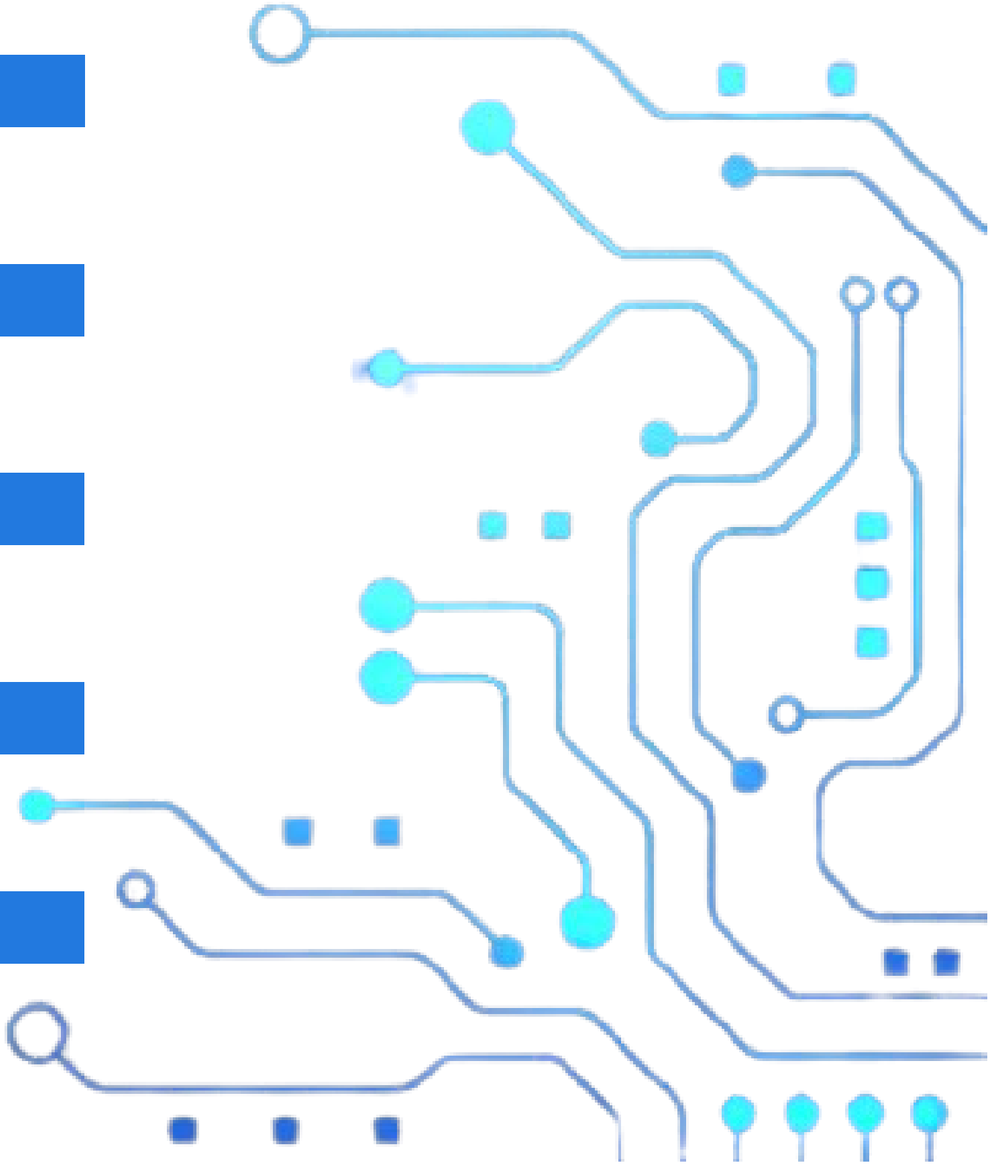
L1 Data Cache & Program Memory (ROM)

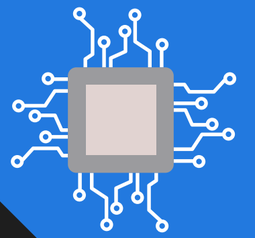
Customized ALU

Harward Architecture

2 Channel 2 Modes Timer x2

Interrupt Controller Unit





Usage Areas of This Computer System

Basic industrial application

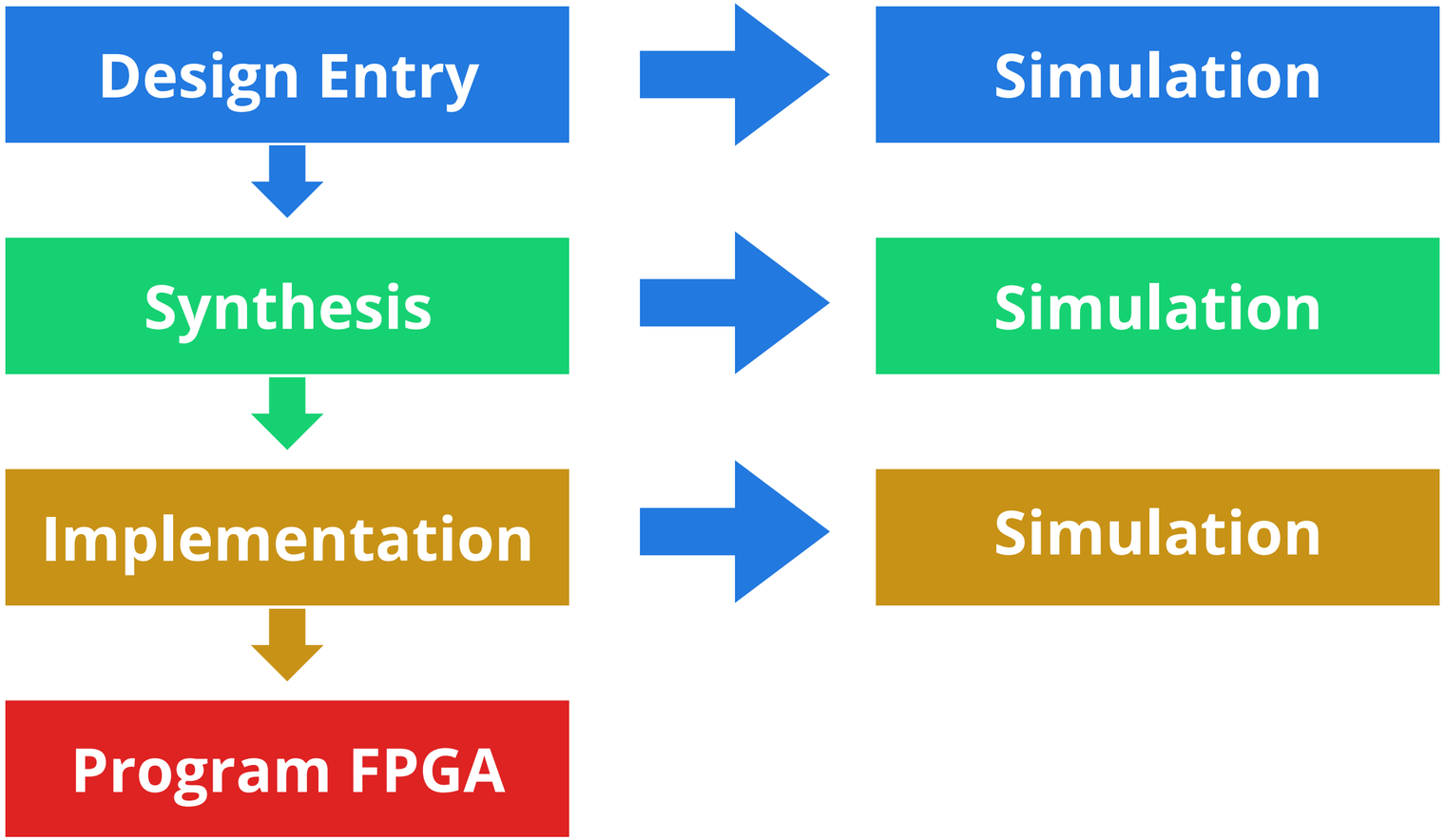
Basic communication system

Sensor control

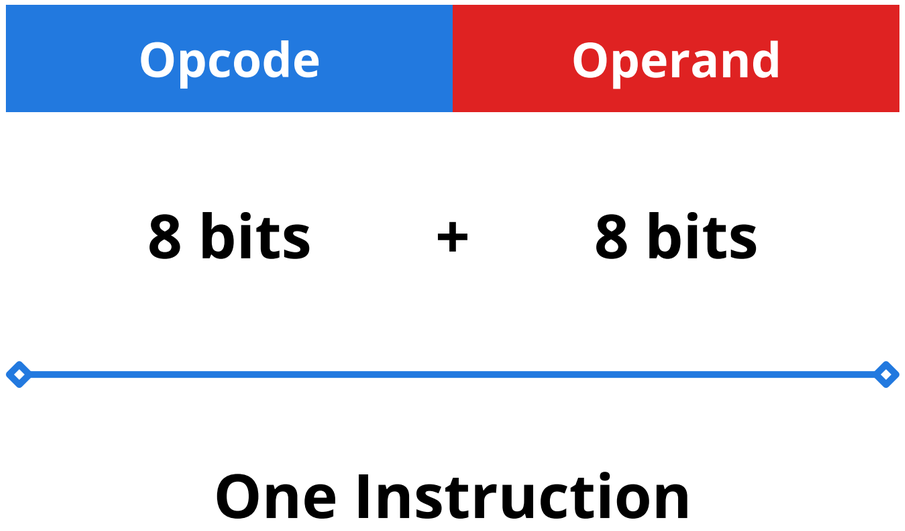
Low cost control system

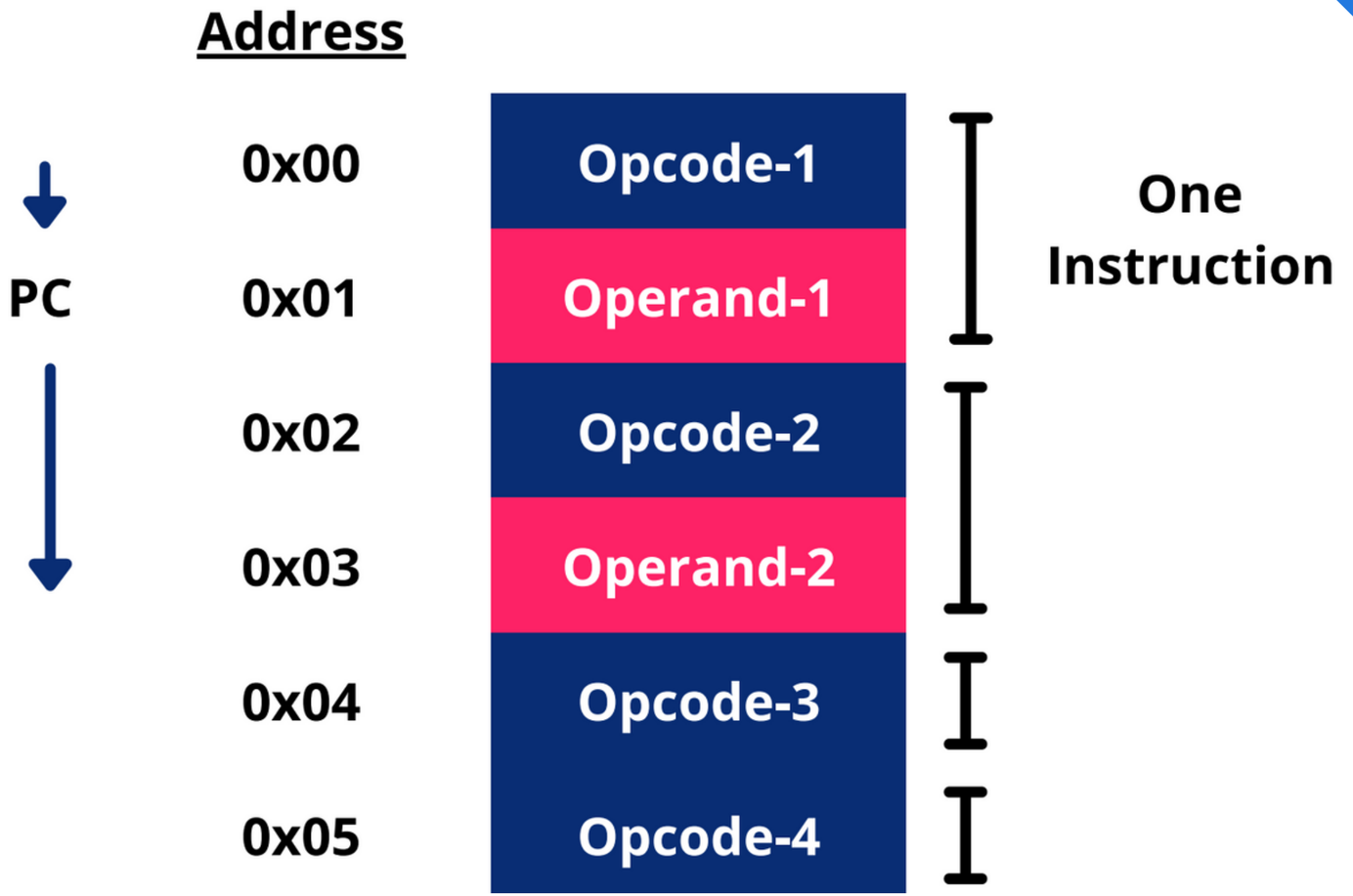
...

Design Flow

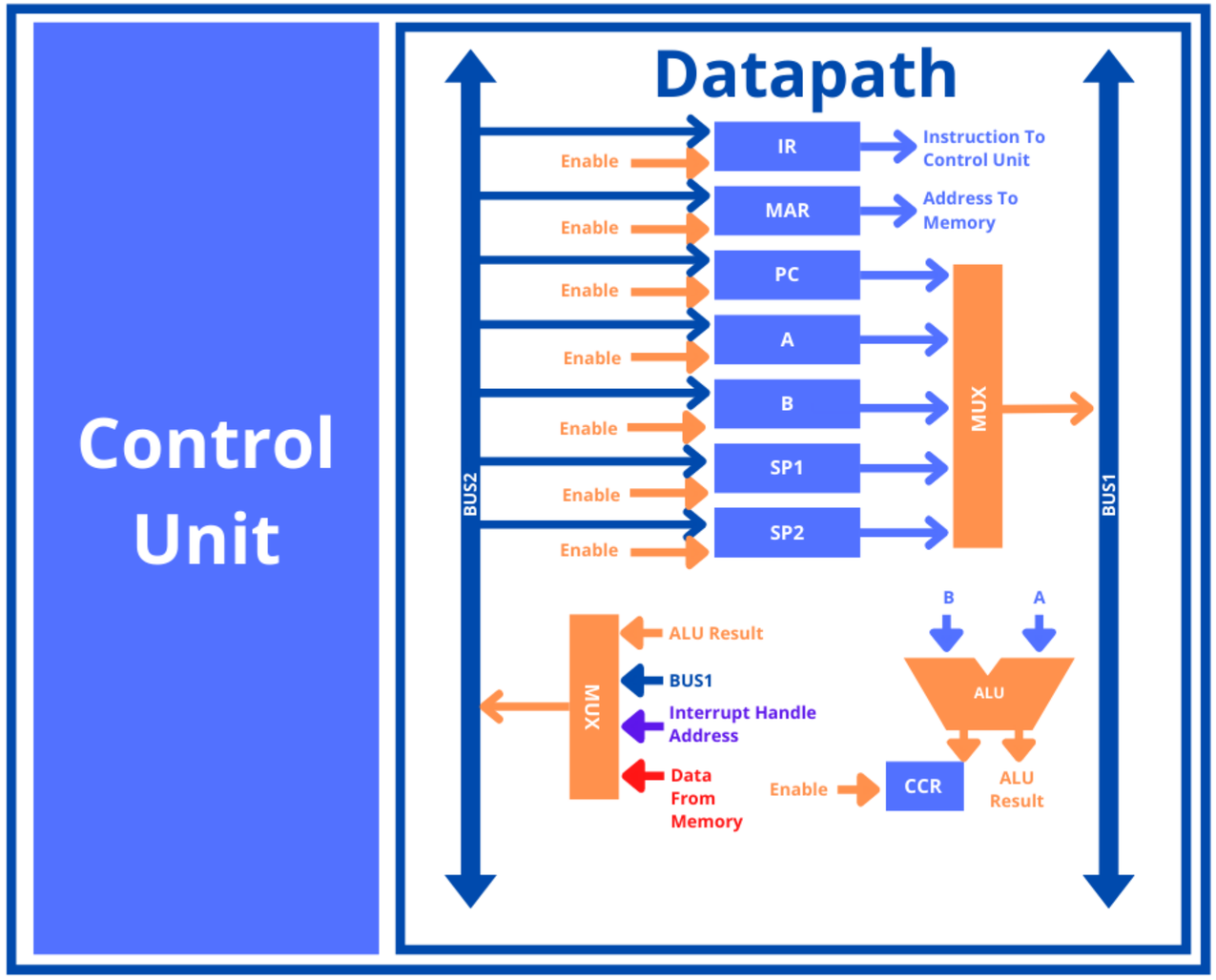

Design Entry
Simulation
Synthesis
Simulation
Implementation
Simulation
Program FPGA

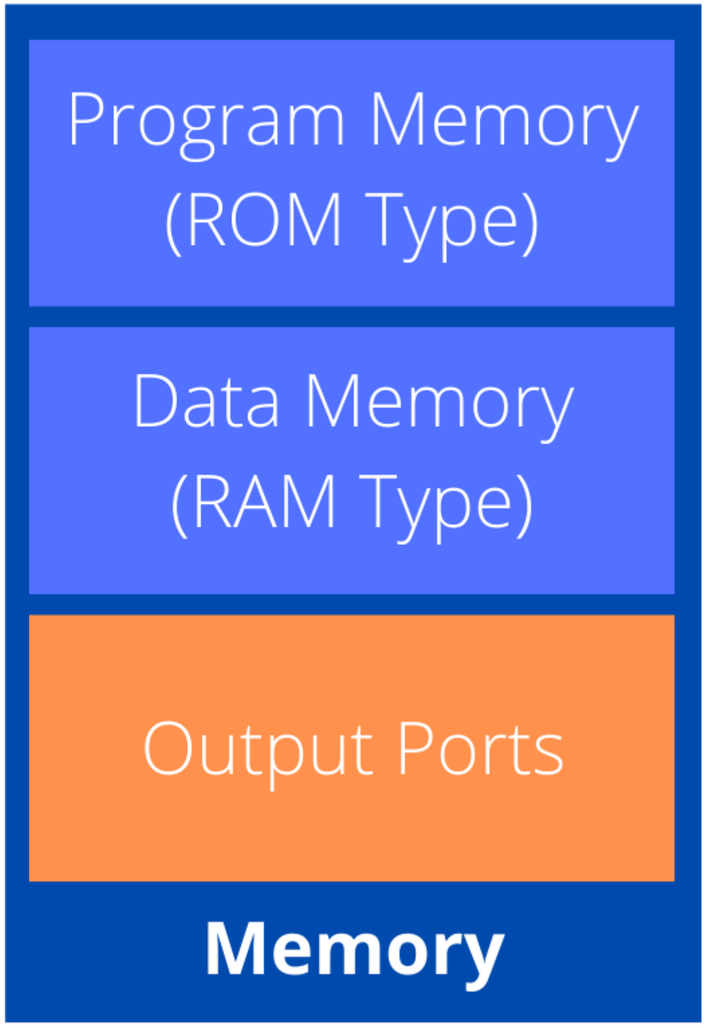
Instruction Structure





The Computer Design





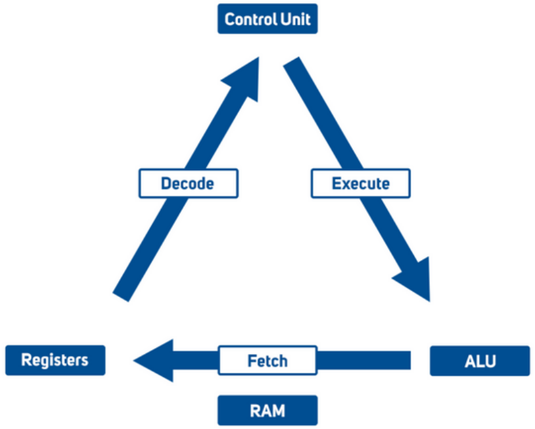
TIM1

TIM2

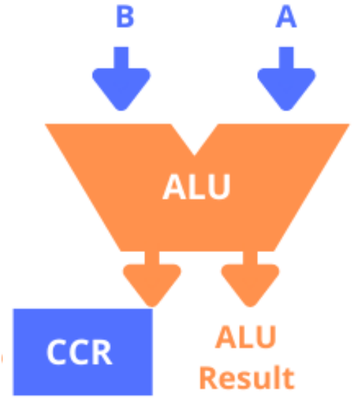
ICU

The computer is occured basically from CPU, Memory System and peripherals.

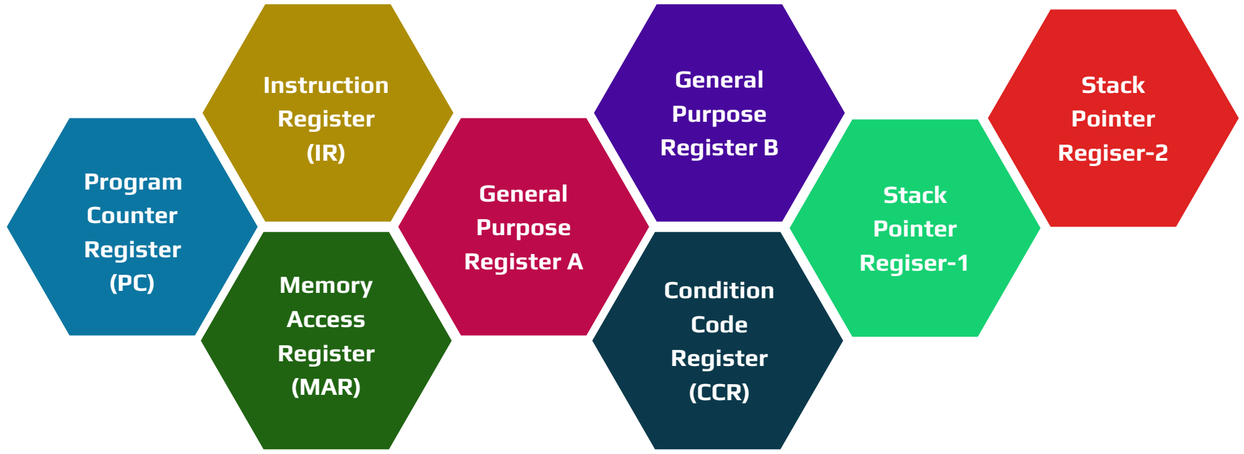
CPU has two main part:
a) Control Unit: Manages everything in the computer architecture.
b) Datapath: It processes instructions with fetch-decode-execution steps.
Datapath occured from three main parts:
Registers-ALU-BUS Structure



Fetch-Decode-Execute



ALU



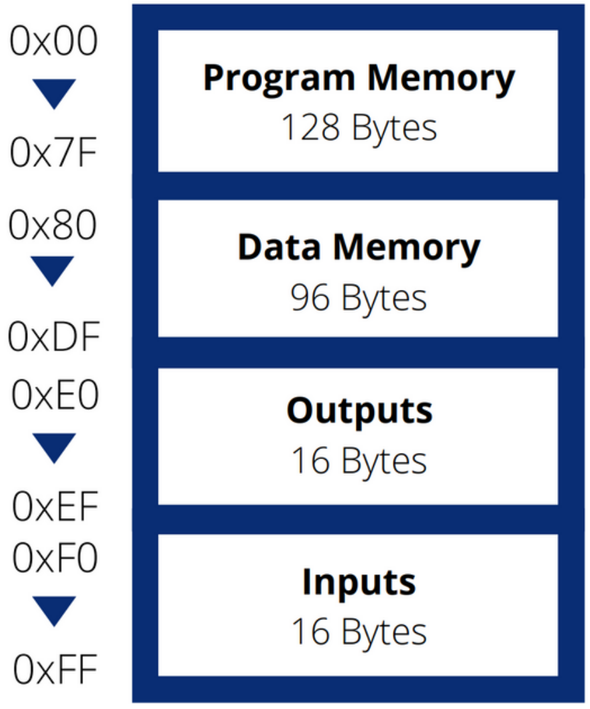
All Registers

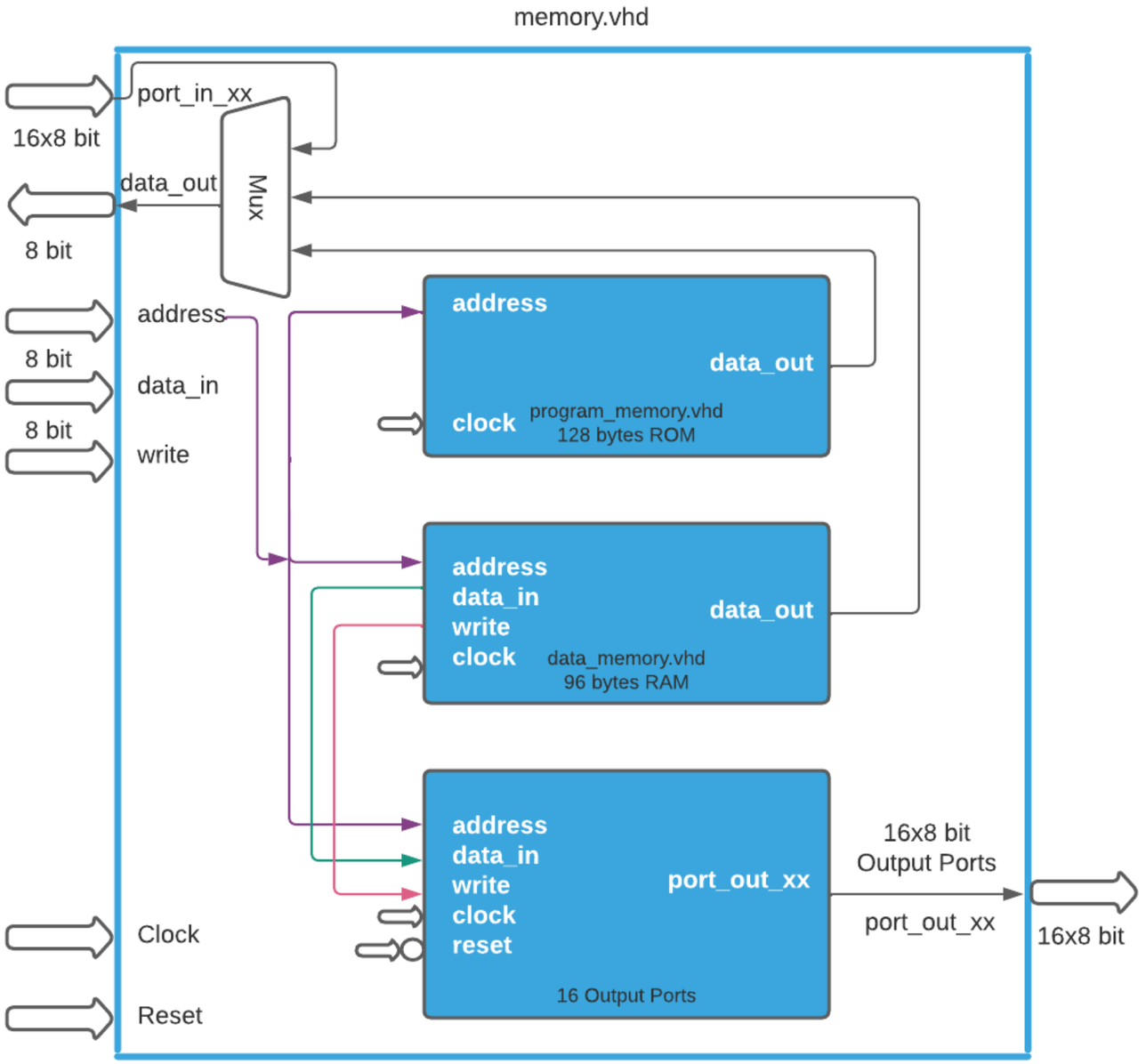
Memory System occured from three main part:

a) Program Memory (ROM Type)

b) L1 Data Cache (RAM Type)

c) Output Ports



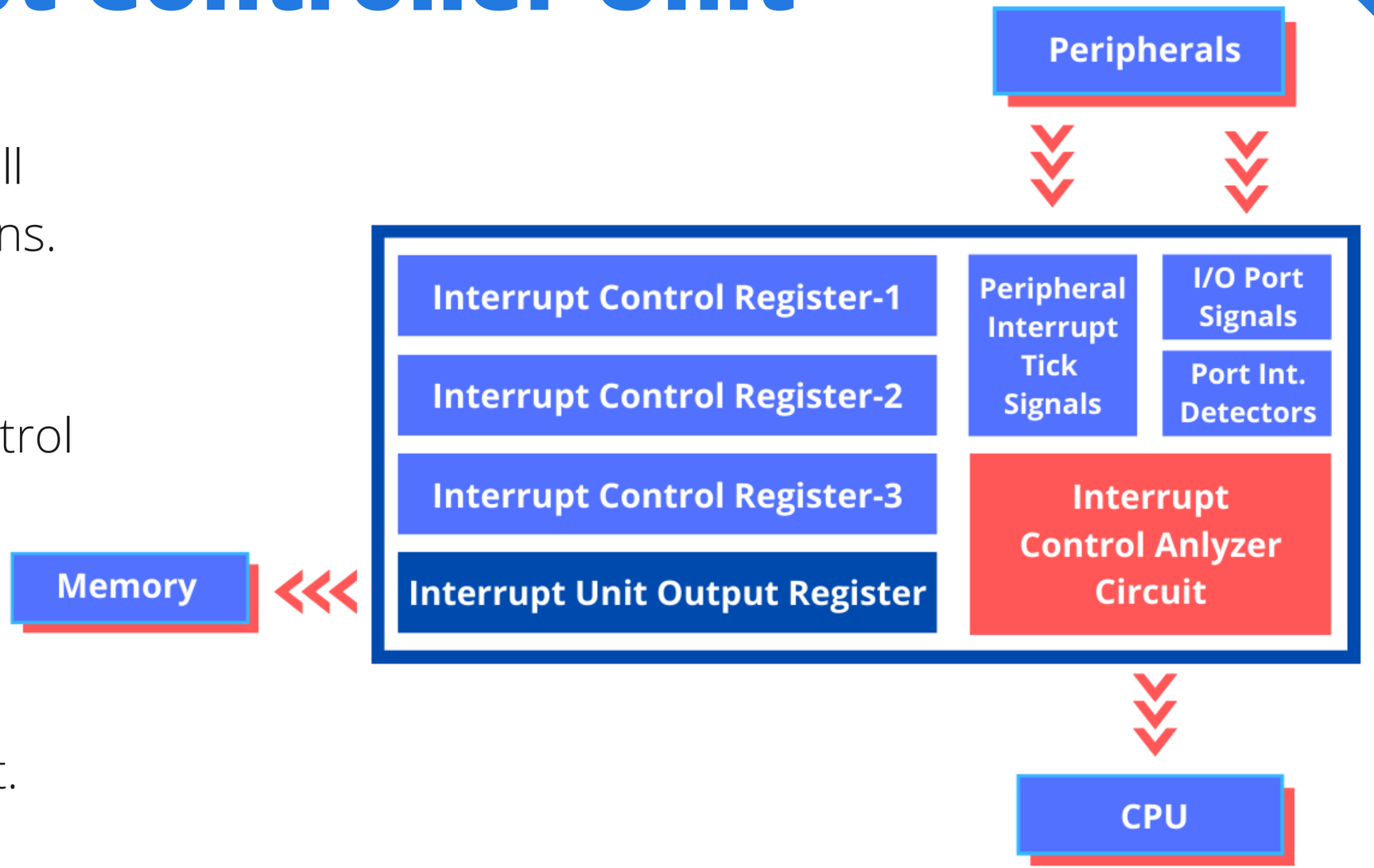


Interrupt Controller Unit

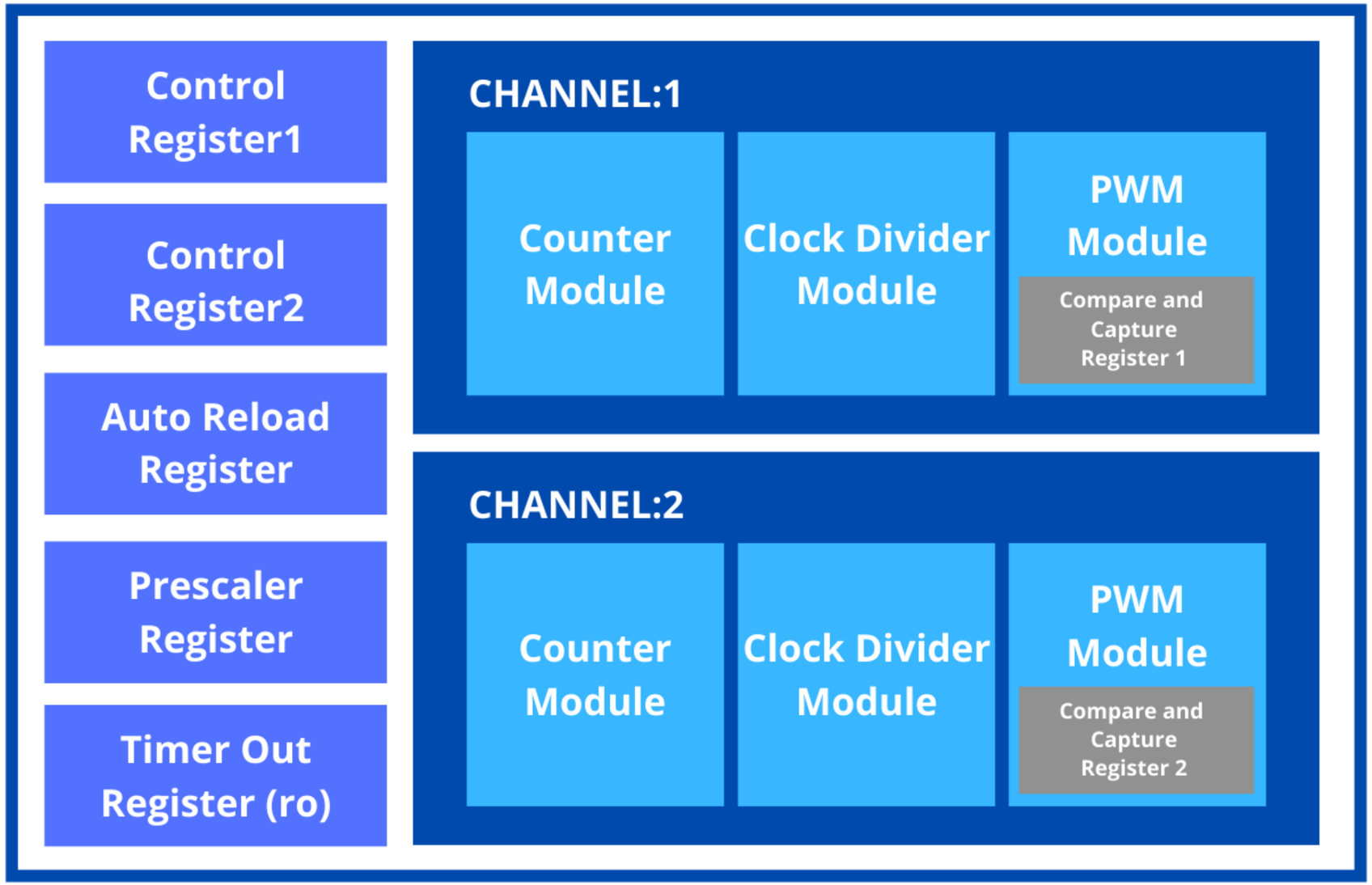
ICU controls the all interrupt conditions.

It is directly connected to Control Unit.

ICU can provides external and software interrupt.



TIMER Module Design

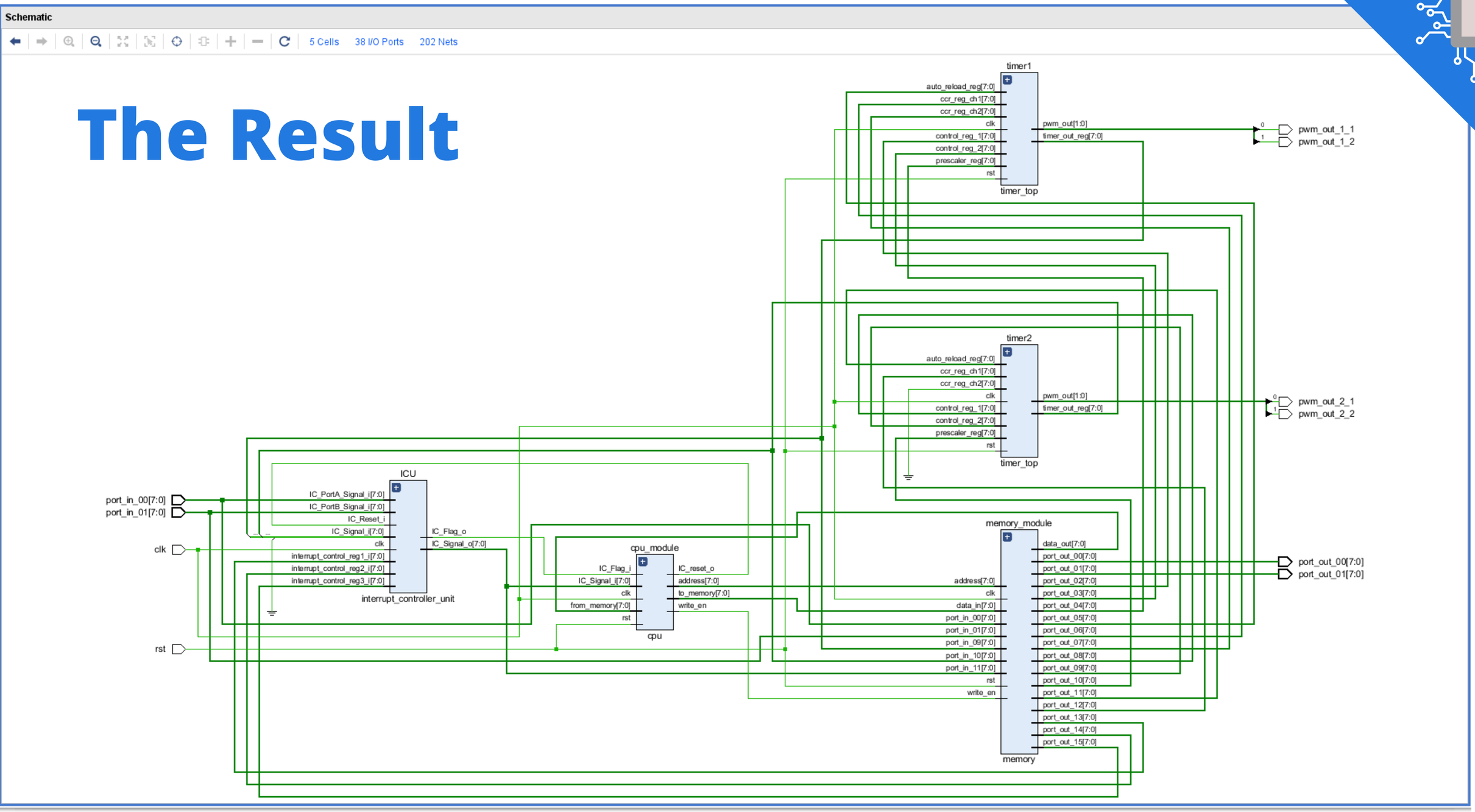


There are two channels in one timer module.

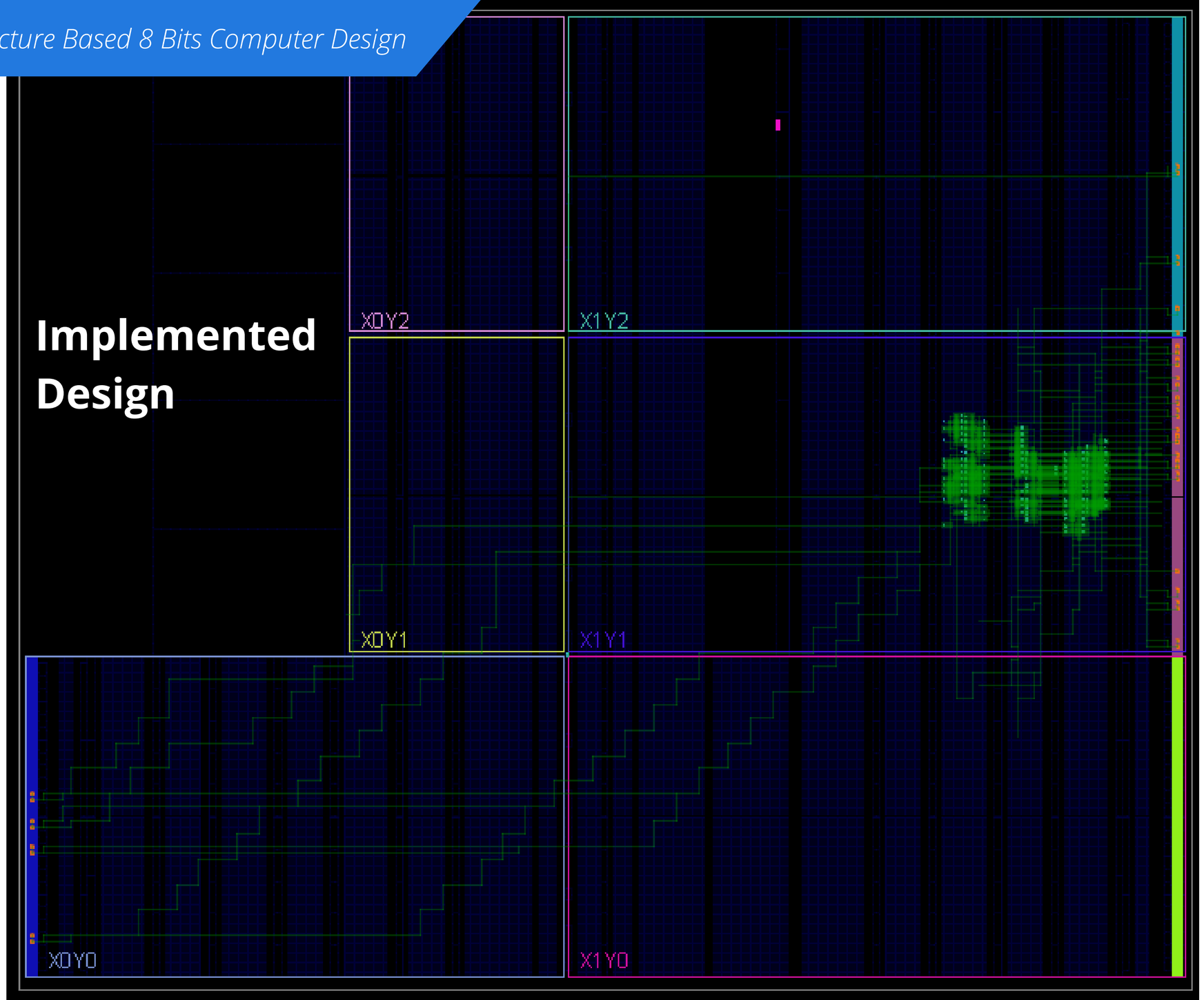
There are two modes:
a) Normal/Counter Mode
b) PWM Generation Mode

Also it has interrupt property.

The Result


Schematic
5 Cells
38 I/O Ports
202 Nets
timer1
auto_reload_reg[7:0]
ccr_reg_ch1[7:0]
ccr_reg_ch2[7:0]
clk
control_reg_1[7:0]
control_reg_2[7:0]
prescaler_reg[7:0]
rst
pwm_out[1:0]
timer_out_reg[7:0]
timer_top
pwm_out_1_1
pwm_out_1_2
timer2
pwm_out_2_1
pwm_out_2_2
ICU
IC_PortA_Signal_i[7:0]
IC_PortB_Signal_i[7:0]
IC_Reset_i
IC_Signal_i[7:0]
interrupt_control_reg1_i[7:0]
interrupt_control_reg2_i[7:0]
interrupt_control_reg3_i[7:0]
IC_Flag_o
IC_Signal_o[7:0]
interrupt_controller_unit
port_in_00[7:0]
port_in_01[7:0]
cpu_module
IC_Flag_i
IC_reset_o
address[7:0]
to_memory[7:0]
write_en
from_memory[7:0]
cpu
memory_module
data_out[7:0]
data_in[7:0]
port_in_09[7:0]
port_in_10[7:0]
port_in_11[7:0]
write_en
port_out_00[7:0]
port_out_01[7:0]
port_out_02[7:0]
port_out_03[7:0]
port_out_04[7:0]
port_out_05[7:0]
port_out_06[7:0]
port_out_07[7:0]
port_out_08[7:0]
port_out_09[7:0]
port_out_10[7:0]
port_out_11[7:0]
port_out_12[7:0]
port_out_13[7:0]
port_out_14[7:0]
port_out_15[7:0]
memory

Implemented Design



The system clock freq. set to 8 MHz (125ns period) with clock wizard.

Intra-Clock Paths - sys_clk

Statistics

Type	Worst Slack	Total Violation
Setup	114,897 ns	0,000 ns
Hold	0,137 ns	0,000 ns
Pulse Width	62,000 ns	0,000 ns

The critical path is about the memory system and takes time nearly 10.103ns.

Timing

Timing Checks - Setup

General Information
Settings
Timing Checks (40)
Setup (20)
Hold (20)

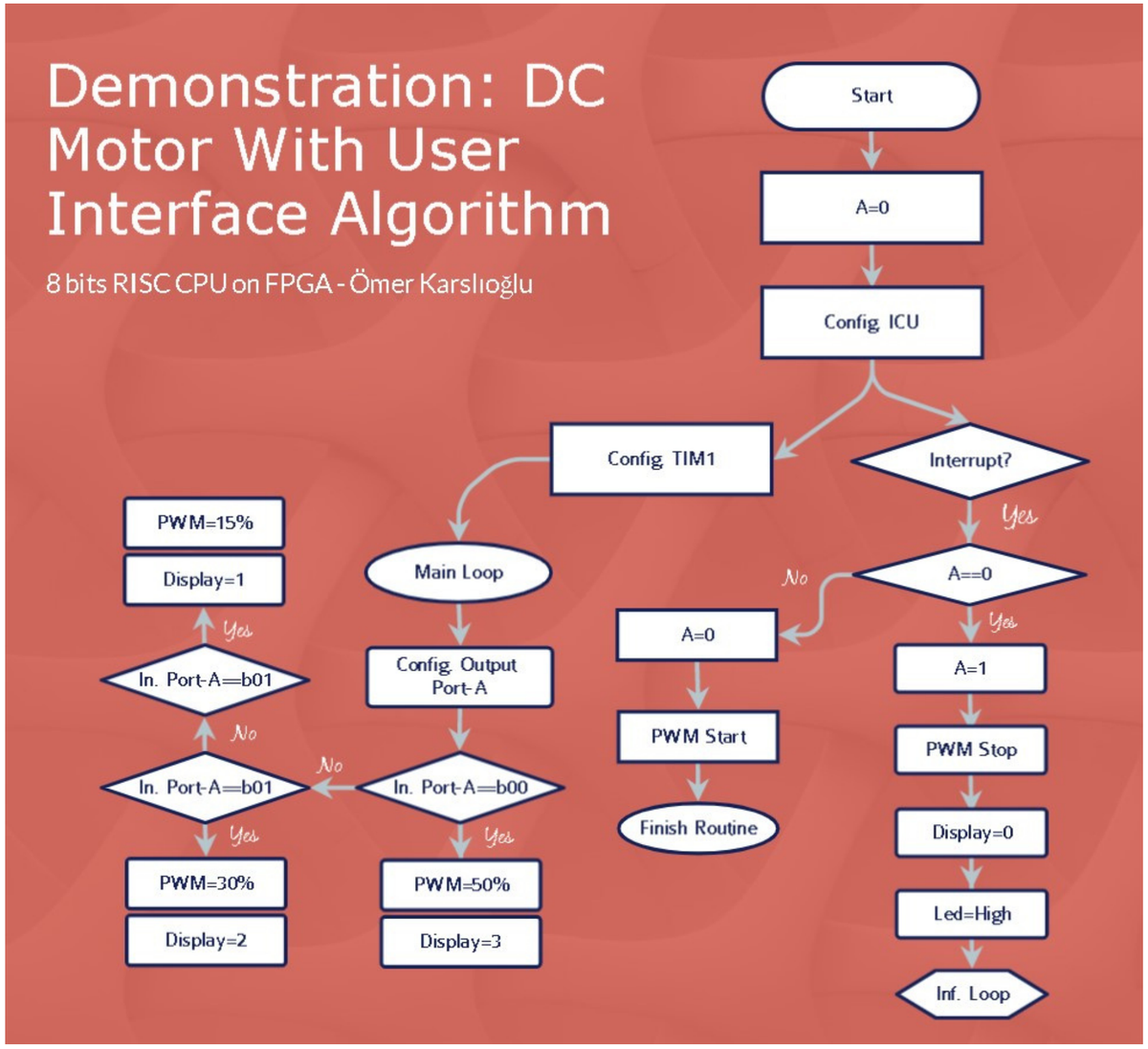
Name	Slack	...	...	...	From	To	Total...	Logi...	Net ...	Log...	Ne...	Requir...	Source Clock	Destinati...	...	Skew
Constrained Paths (2)																
sys_clk (10)																
Path 21	114.897	1	1	1	memory_module...t_00_reg[4]/C	port_o..._00[4]	5.108	4.308	0.800	84.3	15.7	125.000	sys_clk	sys_clk		-2.960
Path 22	114.909	1	1	1	memory_module...t_00_reg[5]/C	port_o..._00[5]	5.096	4.297	0.800	84.3	15.7	125.000	sys_clk	sys_clk		-2.960
Path 23	114.919	1	1	1	memory_module...t_00_reg[1]/C	port_o..._00[1]	5.086	4.287	0.800	84.3	15.7	125.000	sys_clk	sys_clk		-2.960
Path 24	114.920	1	1	1	timer1/pwm_mo..._signal_reg/C	pwm_o..._1_1	5.086	4.286	0.800	84.3	15.7	125.000	sys_clk	sys_clk		-2.960
Path 25	114.924	1	1	1	memory_module...t_01_reg[2]/C	port_o..._01[2]	5.081	4.281	0.800	84.3	15.7	125.000	sys_clk	sys_clk		-2.960
Path 26	114.927	1	1	1	memory_module...t_00_reg[7]/C	port_o..._00[7]	5.078	4.279	0.800	84.3	15.7	125.000	sys_clk	sys_clk		-2.960
Path 27	114.930	1	1	1	memory_module...t_01_reg[1]/C	port_o..._01[1]	5.075	4.275	0.800	84.2	15.8	125.000	sys_clk	sys_clk		-2.960
Path 28	114.931	1	1	1	memory_module...t_01_reg[0]/C	port_o..._01[0]	5.075	4.275	0.800	84.2	15.8	125.000	sys_clk	sys_clk		-2.960
Path 29	114.932	1	1	1	memory_module...t_01_reg[3]/C	port_o..._01[3]	5.074	4.274	0.800	84.2	15.8	125.000	sys_clk	sys_clk		-2.960
Path 30	114.933	1	1	1	memory_module...t_00_reg[6]/C	port_o..._00[6]	5.072	4.272	0.800	84.2	15.8	125.000	sys_clk	sys_clk		-2.960

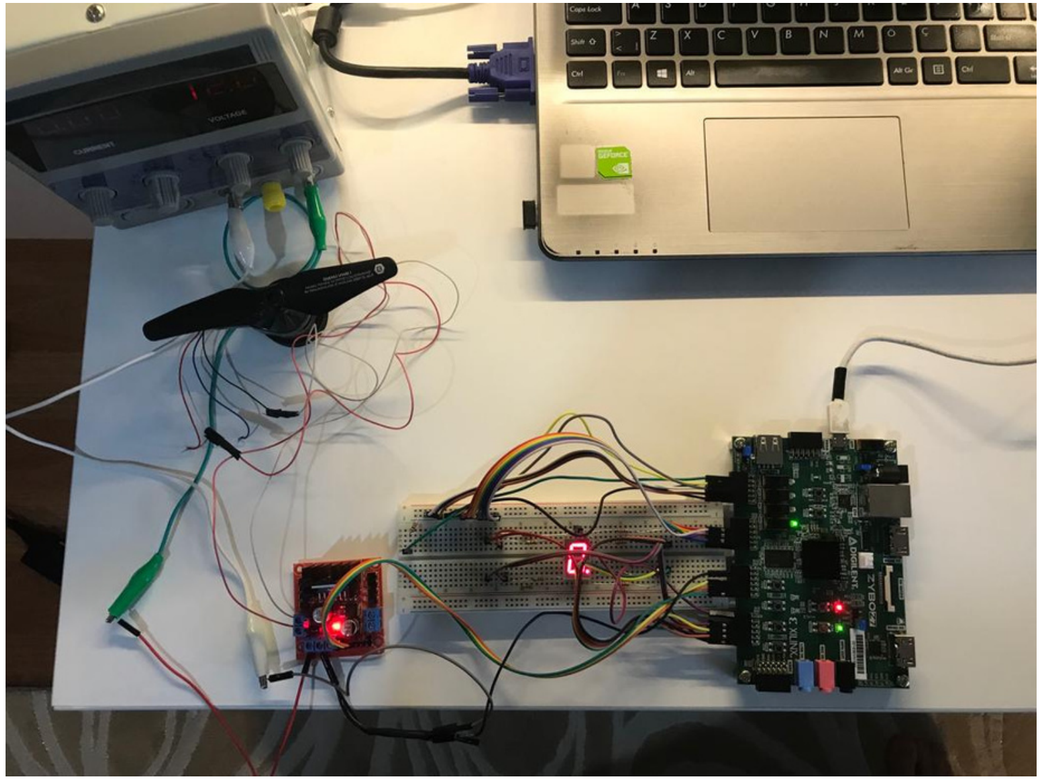
So store instructions may take more time than other instructions.

Tcl Console | Messages | Log | R

Name	Constraints	LUT	FF
synth_1	constrs_1	806	261
impl_1	constrs_1		
synth_2 (active)	**constrs_1**	**730**	**335**
impl_2 (active)	**constrs_1**	**720**	**337**

The Demonstration





A RISC ARCHITECTURE BASED 8 BITS COMPUTER DESIGN AND IMPLEMENTATION ON FPGA USING VHDL

Thanks for listening ...

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June, 2022

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