Digital Design 2 Project 1 Report Group 4 CloudX

Abdelhakim Badawy 900171087

Omer Moussa 900171920

Yahya Saad 900171786

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Contents

Chapter 1

Introduction

1.1 Project Description

This project is an implementation of a standard cell library that has the following low-level electronic logic functions: inverter, tristate inverter, 3 input NAND, 3 input NOR and $f = \overline{x.y + w.z}$. Each of these gates is implemented at 3 sizes: 1, 2 and 4. All the gates are simulated for all sizes and transistor widths are tuned to approach approximately 1:1 ratio for rise and fall delay sizes. All designs and implementations in this project follow standard cell design rules found in the scmos file attached with the project. All developed Schematics and Layouts were made sure to pass the DRC checker and the LVS checker. The widths of the layouts are all multiples of 4λ. Folding mechanism was used to minimize area waste. All cells at all sizes are tuned and folded. The software used in designing schematics and layouts is Electric VLSI. LTSpice is used to simulate electronic behavior of all the netlists and cell layouts in this project. A python script was developed to process the simulation results and compute the best fit plane for the curves. In this report, the methodology is discussed as well as the specifics of the design and implementation of each cell. Electronic behavior and data results is recorded and discussed in details.

1.2 Methodology

1.2.1 Area Waste Minimization and Folding Mechanism

To minimize cell height, transistor folding technique was used. The technique is based on splitting wide transistors in smaller ones and thus decrease cell height. This allows minimizing unused areas in cell layouts when designing a standard cell, as it decreases the differences between different cell heights. The concept of folding is dividing a transistor into smaller transistors whose widths add up to the width of the original transistors. After this, the drains and the sources of the smaller transistors should be shortened. The gate signal will be shared among resulting smaller transistors. This network of smaller transistor is then placed in the original circuit with the shortened drain connected in place of the original transistor and the shortened source connected in place of original source. Consider a transistor of width 18λ. It can be split into 3 transistors each of width 6λ. One of the nodes a, b will be chosen as a source of the network and the other will be the drain.

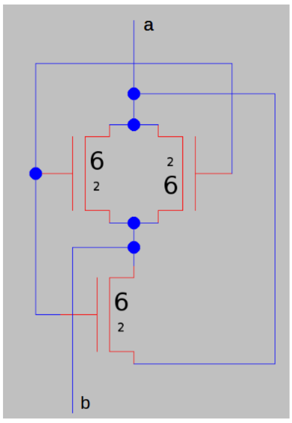


Figure 1.1: optimized split-up network for a 18λ width transistor.

Optimizing folding process is based on minimizing the maximum width of a transistor in the folded network. The technique was applied on all cells and sizes. Layout heights were compared before tuning, after tuning and after folding tuned transistors. Moreover, maximum width of a transistor is calculated before tuning, after tuning and after folding tuned transistors. Figures 1.2 and 1.3 show the cell heights and transistor maximum widths respectively. Observing the data shows that the maximum cell height after tuning and folding will be that of 3 input NAND gate at size 2. Its height is 63λ. Therefore, any cell whose height is less that 63λ , its height will be extended to 63λ.

Cell	Size	Max width of NMOS before tuning	Max width of PMOS before tuning	Max width of NMOS after tuning	Max width of PMOS after tuning	Max width of NMOS after tuning and folding	Max width of PMOS after tuning and folding
Inverter	1	5	12	4	10	4	10
	2	10	24	10	24	5	12
	4	20	48	20	47	5	12
3x1 NAND	1	15	12	14	15	7	15
	2	30	24	29	34	6	17
	4	60	48	46	55	6	14
3x1 NOR	1	5	36	5	36	5	12
	2	10	72	10	72	5	12
	4	20	144	22	142	6	17
Complex f	1	10	24	13	24	7	12
	2	20	48	26	48	6	12
	4	40	96	52	96	6	12
Tristate inverter	1	10	24	10	28	5	12
	2	20	48	20	56	5	12
	4	40	96	40	112	5	12

Figure 1.2: Widths Table

Cell	Size	Height before tuning	Height after tuning	Estimated Height after tuning and folding
Inverter	1	55 λ	55 λ	55 λ
	2	74 λ	74 λ	57 λ
	4	108 λ	107 λ	57 λ
3x1 NAND	1	67 λ	69 λ	62 λ
	2	94 λ	103 λ	63 λ
	4	148 λ	141 λ	60 λ
3x1 NOR	1	81 λ	81 λ	57 λ
	2	122 λ	122 λ	57 λ
	4	204 λ	204 λ	63 λ
Complex f	1	74 λ	77 λ	59 λ
	2	108 λ	114 λ	58 λ
	4	176 λ	188 λ	58 λ
Tristate inverter	1	74 λ	78 λ	57 λ
	2	108 λ	116 λ	57 λ
	4	176 λ	194 λ	57 λ

Figure 1.3: Heights Table

1.2.2 Electronic Behavior simulation and data representation

For each cell the schematic and the layout electronic behavior is simulated using LTSpice. This data is recorded and tabulated and saved in a .csv file to allow further computations and analysis using the python script that was specifically designed for the sake of this project. The python script is used to plot and derive the best fit plane for the t_{pdf} and t_{pdr} data. It uses Matplotlib Library for plotting the data, pandas for reading excel sheets files, and Sci Kit Learn to get the parameters of the plane that fits the data best. The script takes the path of the data files, then it plots t_{pdf} and t_{pdr} in two ways. First, the 2D plot where multiple lines are drawn, one for each transition times. The X-axis is the capacitance load, and the y-axis is the delay in picoseconds. Second, the 3D graph graphs the data in 3D space for better visualization. Then the 3D data are passed to a Sci Kit Learn function used in Machine learning to find the parameters (K1 ,K2, and K3) of the linaer model by fitting the data using the minimum square error.

Chapter 2

Inverter

2.1 Schematics

2.1.1 Size 1

Original Sizes: NMOS 5λ , PMOS 12λ
Tuned Sizes: NMOS 5λ , PMOS 10λ

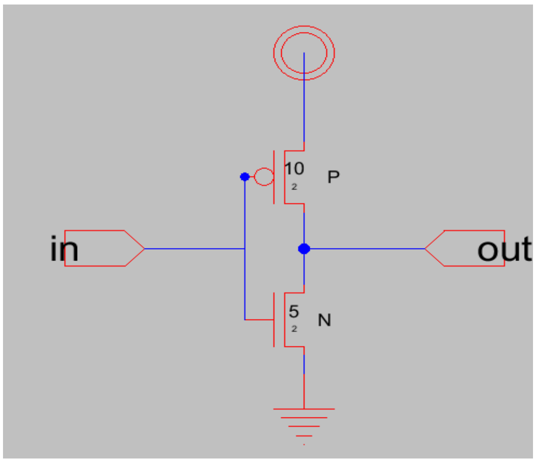
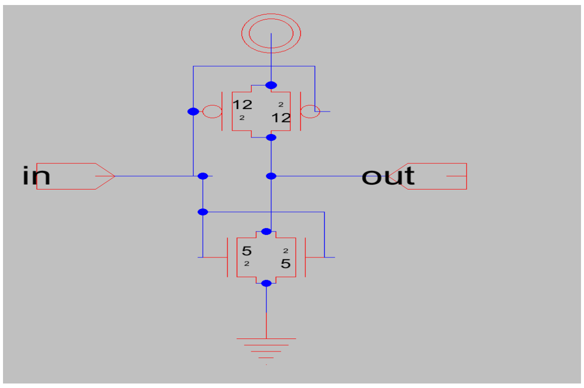


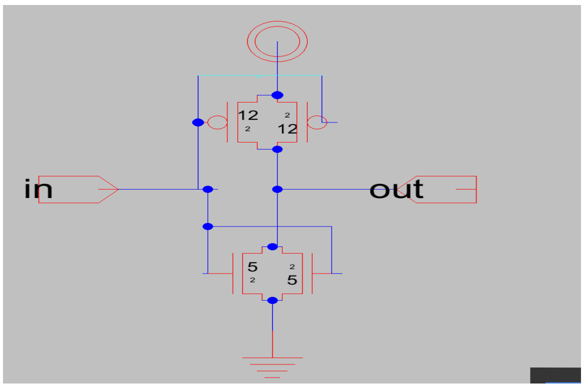
Figure 2.1: Inv 1

2.1.2 Size 2

Original Sizes: NMOS 10λ , PMOS 24λ
Tuned Sizes: NMOS 10λ , PMOS 24λ



(a) inv 2

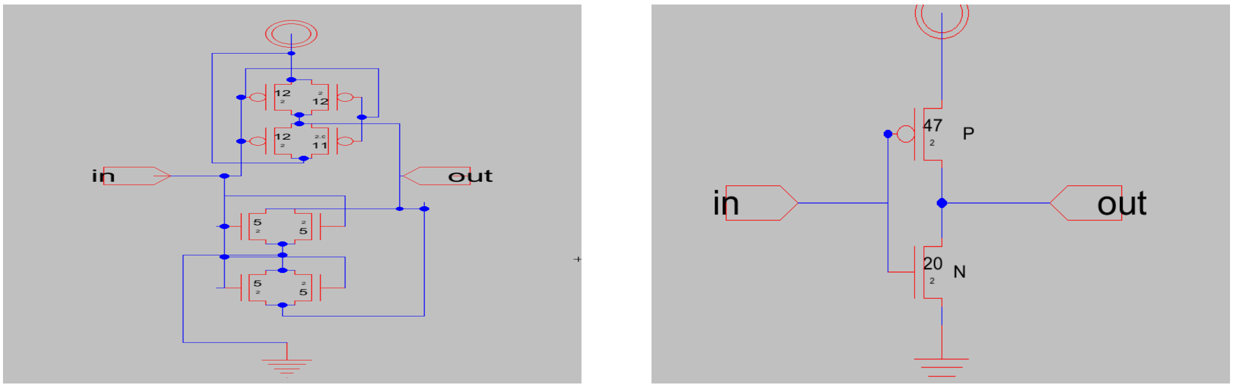


(b) inv 2 folded

Figure 2.2: Inv size 2 Schematics

2.1.3 Size 4

Original Sizes: NMOS 20λ , PMOS 48λ
Tuned Sizes: NMOS 20λ , PMOS 47λ



(a) inv 4

(b) inv 4 folded

Figure 2.3: Inv size 4 Schematics

2.2 Stick Diagrams

The stick diagram of the inverter is the same for all sizes.

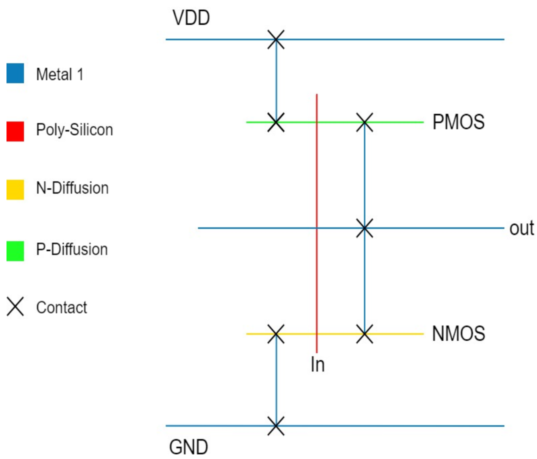


Figure 2.4: Inv Diagram

2.3 Layouts

The figure below provides the Layout of Size 1 Inverter. The dimensions of it is 32 width by 60 height.

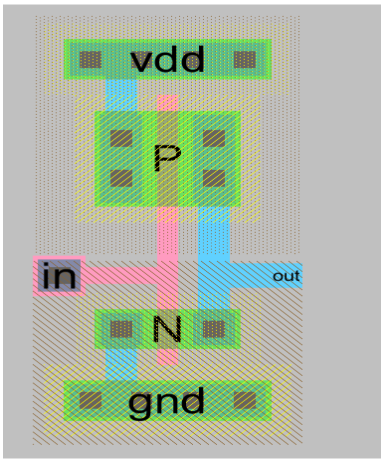


Figure 2.5: Inv Layout

2.4 Data Collection

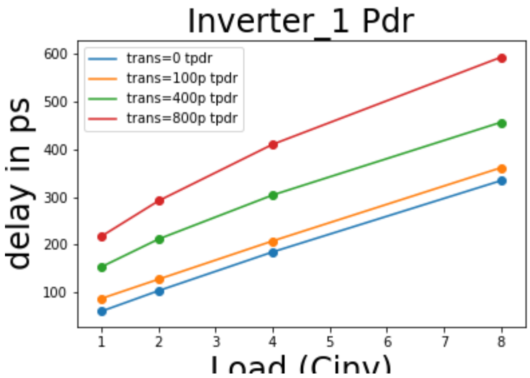
The simulation were run for every Cload and Transition times for all sizes; the linear model was derived for t_{pdr} and t_{pdf} individually.

2.4.1 Size 1

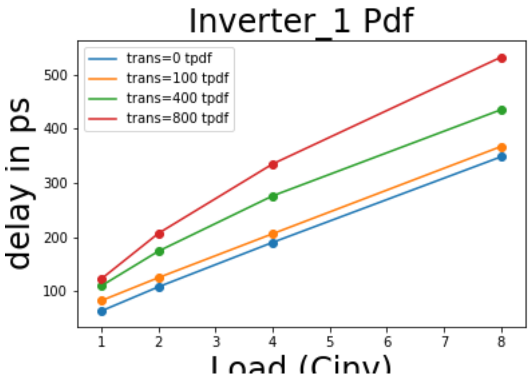
Load (Cinv)	trans=0 tpdr	trans=0 tpdf	trans=100p tpdr	trans=100 tpdf	trans=400p tpdr	trans=400 tpdf	trans=800p tpdr	trans=800 tpdf
1	6.11E-11	6.35E-11	8.78E-11	8.26E-11	1.54E-10	1.10E-10	2.18E-10	1.23E-10
2	1.04E-10	1.08E-10	1.28E-10	1.25E-10	2.12E-10	1.74E-10	2.92E-10	2.07E-10
4	1.85E-10	1.90E-10	2.08E-10	2.06E-10	3.04E-10	2.76E-10	4.10E-10	3.35E-10
8	3.34E-10	3.48E-10	3.61E-10	3.67E-10	4.56E-10	4.35E-10	5.92E-10	5.32E-10

Figure 2.6: size 1 Data

The best fit planes for both t_{pdr} and t_{pdf} respectively gives the following Linear models.
Linear Model for Pdr is
delay= 43.165435 (K1)*Cload + 0.260476 (K2)*Transition + 10.156232 (K3)
Linear Model for Pdf is
delay= 45.941087 (K1)*Cload + 0.152889 (K2)*Transition + 8.163343 (K3)

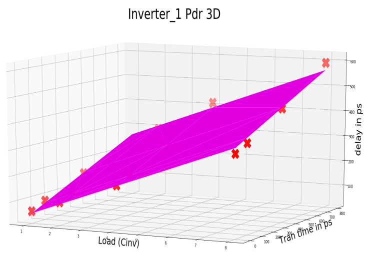


(a) inv 1 Pdr

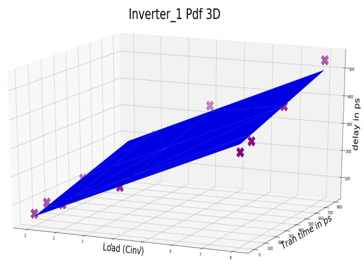


(b) inv 1 Pdf

Figure 2.7: Invertr 1 Data



(a) inv 1 Pdr 3D



(b) inv 1 Pdf 3D

Figure 2.8: Invertr 1 Data

2.4.2 Size 2 and 4

The Data for Size for is found below. The graphs for them can be found in the plots folder. They generally follow the same trend as size 1.

Load (Cinv)	trans=0 tpdr	trans=0 tpdf	trans=100p tpdr	trans=100 tpdf	trans=400p tpdr	trans=400 tpdf	trans=800p tpdr	trans=800 tpdf
1	3.13E-11	3.14E-11	6.28E-11	5.51E-11	1.13E-10	6.77E-11	1.61E-10	6.94E-11
2	5.53E-11	5.58E-11	8.34E-11	7.68E-11	1.47E-10	1.03E-10	2.07E-10	1.13E-10
4	9.45E-11	9.50E-11	1.18E-10	1.12E-10	2.00E-10	1.59E-10	2.74E-10	1.84E-10
8	1.65E-10	1.65E-10	1.89E-10	1.82E-10	2.83E-10	2.48E-10	3.83E-10	2.98E-10

Figure 2.9: size 2 Data

The best fit planes for both t_{pdr} and t_{pdf} respectively gives the following Linear models.
For size 2 Linear Model for Pdr is
delay= 22.888043 (K1)*Cload + 0.211708 (K2)*Transition + 5.820966 (K3)
Linear Model for Pdf is
delay= 23.546087 (K1)*Cload + 0.096935 (K2)*Transition + 6.148142 (K3) For size 4 Linear Model for Pdr is

Load (Cinv)	trans=0 tpdr	trans=0 tpdf	trans=100p tpdr	trans=100 tpdf	trans=400p tpdr	trans=400 tpdf	trans=800p tpdr	trans=800 tpdf
1	2.01E-11	1.99E-11	5.09E-11	4.23E-11	9.22E-11	4.75E-11	1.34E-10	4.20E-11
2	3.27E-11	3.21E-11	6.38E-11	5.59E-11	1.15E-10	6.99E-11	1.62E-10	7.17E-11
4	5.71E-11	5.71E-11	8.47E-11	7.77E-11	1.49E-10	1.06E-10	2.09E-10	1.15E-10
8	9.68E-11	9.59E-11	1.21E-10	1.13E-10	2.02E-10	1.62E-10	2.78E-10	1.90E-10

Figure 2.10: size 4 Data

delay= 14.084130 (K1)*Cload + 0.177111 (K2)*Transition + 6.392092 (K3)
Linear Model for Pdf is
delay= 14.380870 (K1)*Cload + 0.062039 (K2)*Transition + 7.034158 (K3)

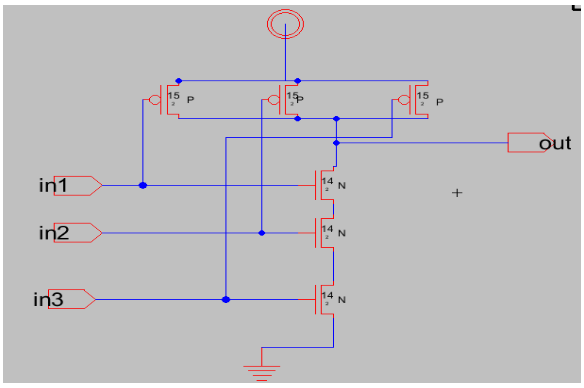
Chapter 3

Three Input NAND

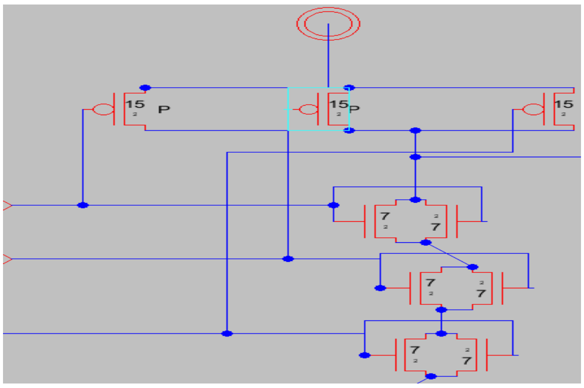
3.1 Schematics

3.1.1 Size 1

Original Sizes: NMOS 15λ , PMOS 12λ
Tuned Sizes: NMOS 15λ , PMOS 14λ



(a) NAND 1

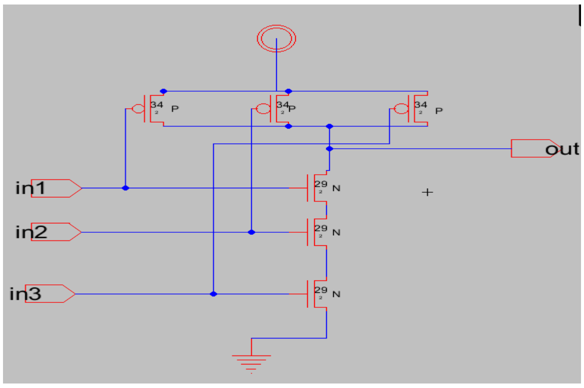


(b) NAND 1 folded

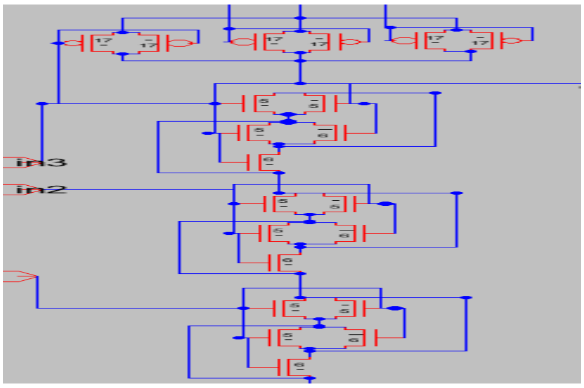
Figure 3.1: NAND size 1 Schematics

3.1.2 Size 2

Original Sizes: NMOS 30λ , PMOS 24λ
Tuned Sizes: NMOS 29λ , PMOS 34λ



(a) NAND 2

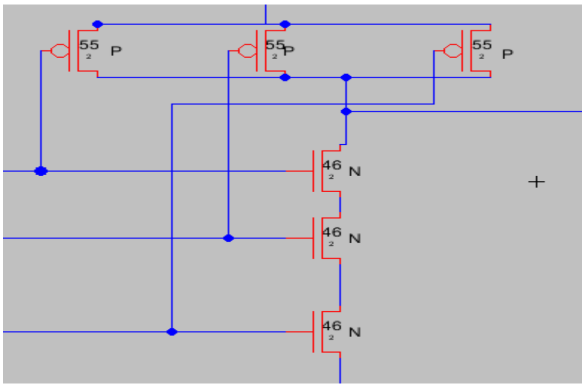


(b) NAND 2 folded

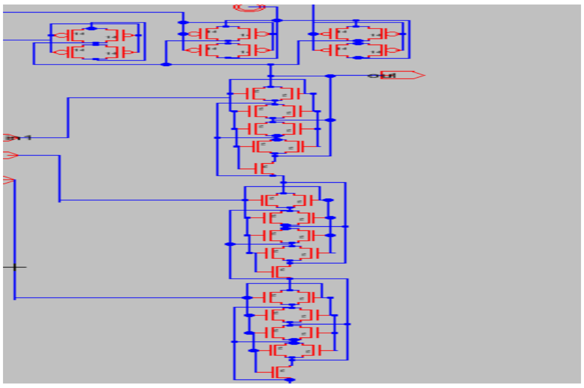
Figure 3.2: NAND Size 2 Schematics

3.1.3 Size 4

Original Sizes: NMOS 60λ , PMOS 40λ
Tuned Sizes: NMOS 55λ , PMOS 46λ



(a) NAND 4



(b) NAND 4 folded

Figure 3.3: NAND size 4 Schematics

3.2 Stick Diagrams

The stick diagram of the three input NAND is the same for all sizes.

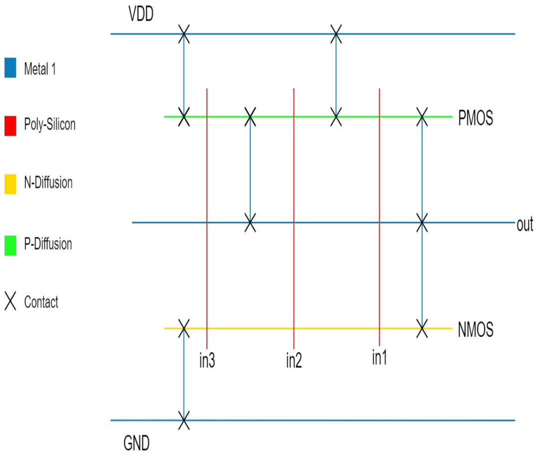


Figure 3.4: NAND Diagram

3.3 Layouts

The figure below provides the Layout of Size 1 3NAND. The dimensions of it is 48 width by 80 height.

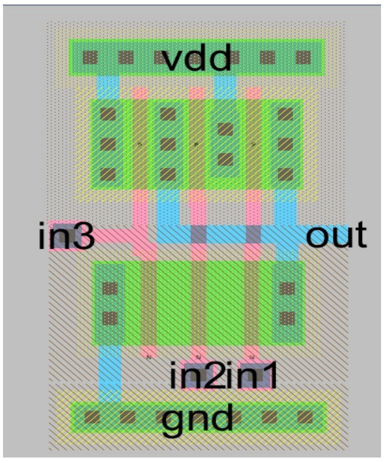


Figure 3.5: NAND Layout

3.4 Data Collection

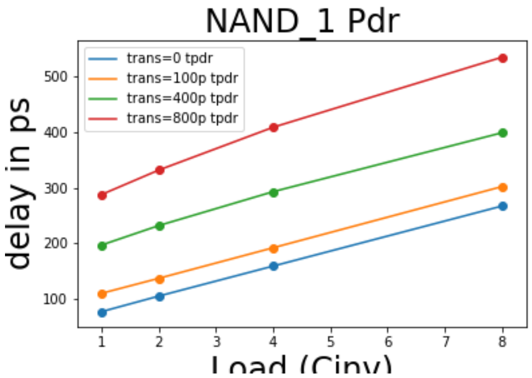
The simulation were run for every Cload and Transition times for all sizes; the linear model was derived for t_{pdr} and t_{pdf} individually.

3.4.1 Size 1

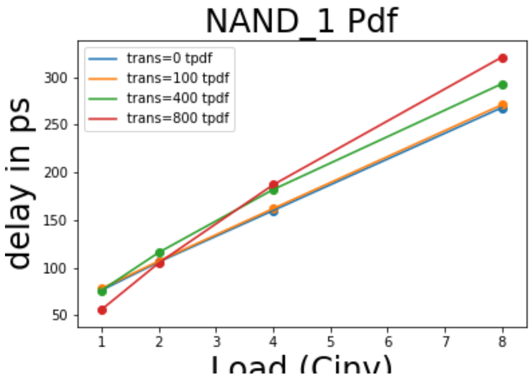
Load (Cinv)	trans=0 tpdr	trans=0 tpdf	trans=100p tpdr	trans=100 tpdf	trans=400p tpdr	trans=400 tpdf	trans=800p tpdr	trans=800 tpdf
1	7.70E-11	7.63E-11	1.10E-10	7.81E-11	1.97E-10	7.62E-11	2.88E-10	5.61E-11
2	1.05E-10	1.06E-10	1.37E-10	1.07E-10	2.32E-10	1.16E-10	3.32E-10	1.05E-10
4	1.59E-10	1.60E-10	1.92E-10	1.62E-10	2.93E-10	1.82E-10	4.09E-10	1.87E-10
8	2.67E-10	2.68E-10	3.02E-10	2.71E-10	3.99E-10	2.93E-10	5.35E-10	3.21E-10

Figure 3.6: size 1 Data

The best fit planes for both t_{pdr} and t_{pdf} respectively gives the following Linear models.
Linear Model for Pdr is
delay= 29.500000 (K1)*Cload + 0.298484 (K2)*Transition + 44.492742 (K3)
Linear Model for Pdf is
delay= 30.652826 (K1)*Cload + 0.019640 (K2)*Transition + 38.962547 (K3)

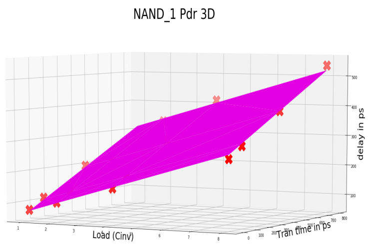


(a) NAND 1 Pdr

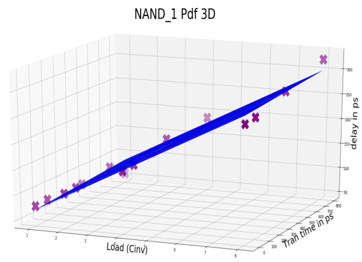


(b) NAND 1 Pdf

Figure 3.7: NAND 1 Plots



(a) NAND 1 Pdr 3D



(b) NAND 1 Pdf 3D

Figure 3.8: NAND 1 Plots

3.4.2 Size 2 and 4

The Data for Size for is found below. The graphs for them can be found in the plots folder. They generally follow the same trend as size 1.

Load (Cinv)	trans= 0 tpdr	trans= 0 tpdf	trans=100 p tpdr	trans=100 tpdf	trans=400 p tpdr	trans=400 tpdf	trans=800 p tpdr	trans=800 tpdf
1	6.00E-11	5.97E-11	9.25E-11	6.43E-11	1.68E-10	6.09E-11	2.47E-10	4.33E-11
2	7.35E-11	7.73E-11	1.05E-10	7.98E-11	1.87E-10	8.29E-11	2.69E-10	6.99E-11
4	9.89E-11	1.07E-10	1.31E-10	1.08E-10	2.20E-10	1.20E-10	3.15E-10	1.17E-10
8	1.48E-10	1.59E-10	1.80E-10	1.62E-10	2.78E-10	1.84E-10	3.84E-10	1.96E-10

Figure 3.9: size 2 Data

The best fit planes for both t_{pdr} and t_{pdf} respectively gives the following Linear models.
For size 2 Linear Model for Pdr is

delay= 15.023696 (K1)*Cload + 0.260037 (K2)*Transition + 43.955335 (K3)

Linear Model for Pdf is

delay= 16.716304 (K1)*Cload + 0.007666 (K2)*Transition + 40.516117 (K3)

For size 4 Linear Model for Pdr is

Load (Cinv)	trans=0 tpdr	trans=0 tpdf	trans=100p tpdr	trans=100 tpdf	trans=400p tpdr	trans=400 tpdf	trans=800p tpdr	trans=800 tpdf
1	5.36E-11	5.38E-11	8.72E-11	5.85E-11	1.59E-10	5.43E-11	2.34E-10	3.65E-11
2	6.39E-11	6.50E-11	9.51E-11	6.90E-11	1.71E-10	6.89E-11	2.48E-10	5.50E-11
4	7.97E-11	8.73E-11	1.11E-10	8.85E-11	1.94E-10	9.54E-11	2.78E-10	8.70E-11
8	1.10E-10	1.21E-10	1.43E-10	1.24E-10	2.34E-10	1.40E-10	3.28E-10	1.43E-10

Figure 3.10: size 4 Data

delay= 9.999783 (K1)*Cload + 0.242350 (K2)*Transition + 45.580815 (K3)
Linear Model for Pdf is
delay= 11.510435 (K1)*Cload + -0.002065 (K2)*Transition + 41.706837 (K3)

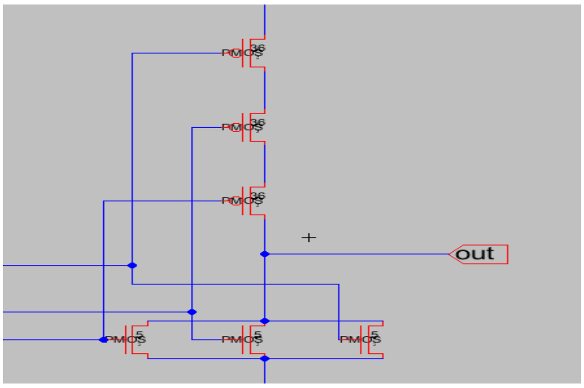
Chapter 4

Three Input NOR

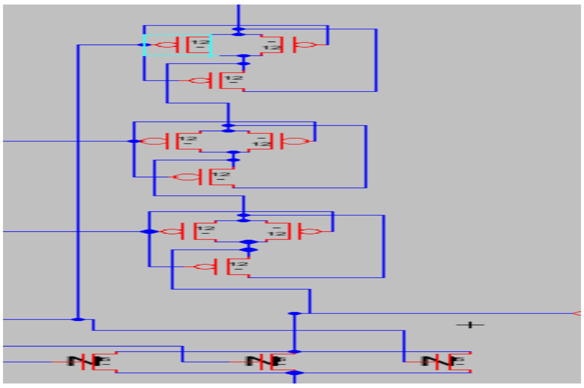
4.1 Schematics

4.1.1 Size 1

Original Sizes: NMOS 5λ , PMOS 36λ
Tuned Sizes: NMOS 5λ , PMOS 36λ



(a) NOR 1

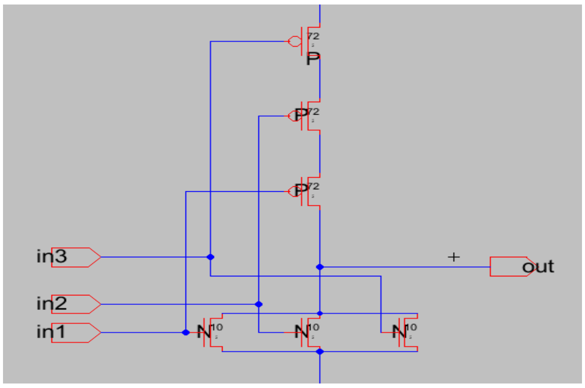


(b) NOR 1 folded

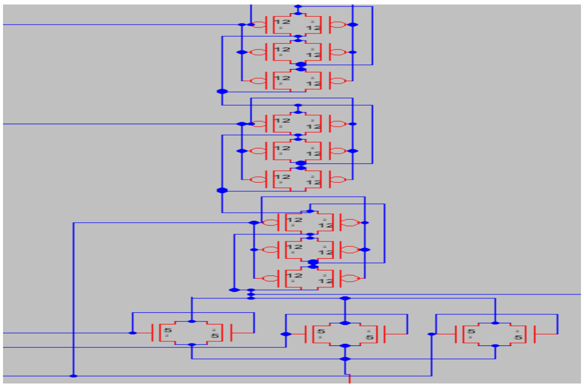
Figure 4.1: NOR size 1 Schematics

4.1.2 Size 2

Original Sizes: NMOS 10λ , PMOS 72λ
Tuned Sizes: NMOS 10λ , PMOS 72λ



(a) NOR 2

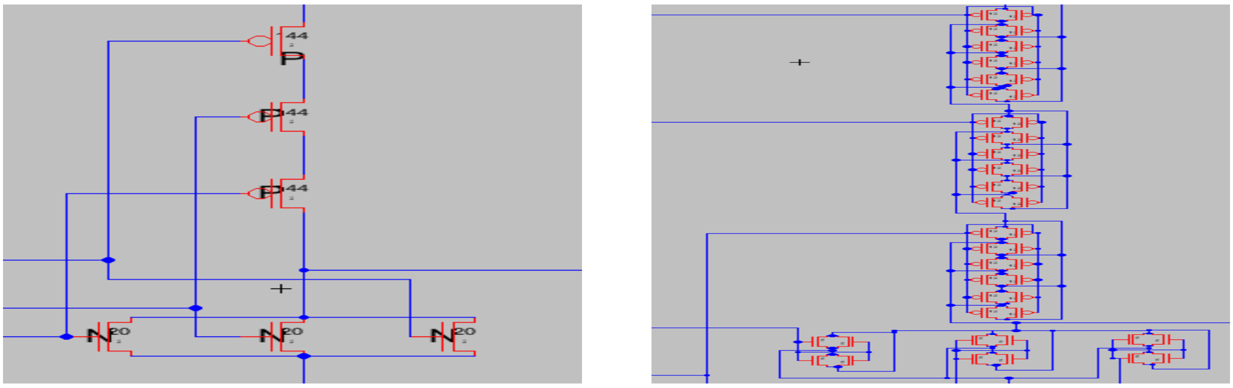


(b) NOR 2 folded

Figure 4.2: NOR size 2 Schematics

4.1.3 Size 4

Original Sizes: NMOS 20λ , PMOS 144λ
Tuned Sizes: NMOS 20λ , PMOS 144λ



(a) NOR 4 (b) NOR 4 folded

Figure 4.3: NOR size 4 Schematics

4.2 Stick Diagrams

The stick diagram of the three input NOR is the same for all sizes.

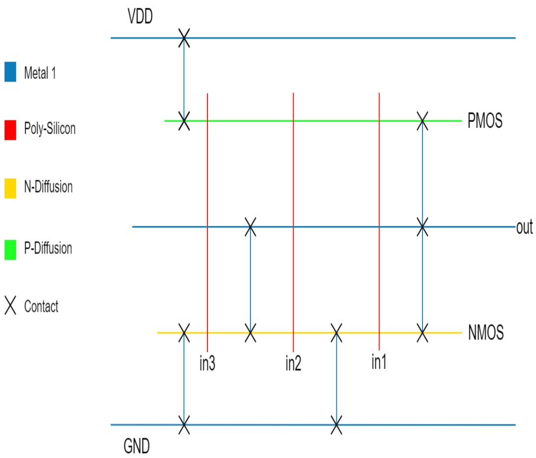


Figure 4.4: NOR Diagram

4.3 Layouts

The figure below provides the Layout of Size 1 3NOR. The dimensions of it is 52 width by 88 height.

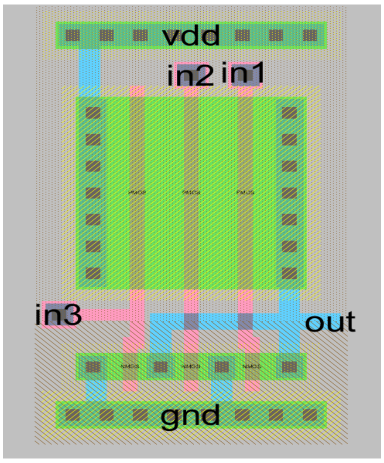


Figure 4.5: NOR Layout

4.4 Data Collection

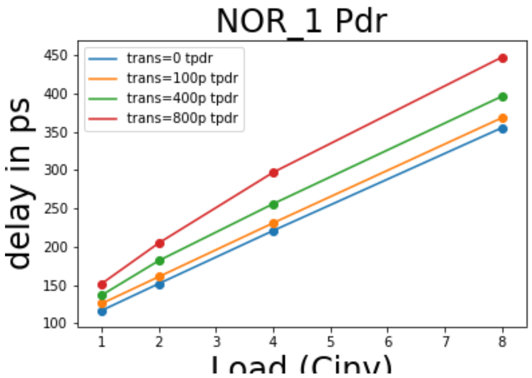
The simulation were run for every Cload and Transition times for all sizes; the linear model was derived for t_{pdr} and t_{pdf} individually.

4.4.1 Size 1

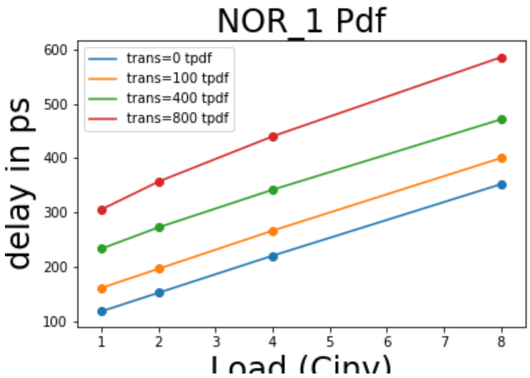
Load (Cinv)	trans=0 tpdr	trans=0 tpdf	trans=100p tpdr	trans=100 tpdf	trans=400p tpdr	trans=400 tpdf	trans=800p tpdr	trans=800 tpdf
1	1.17E-10	1.19E-10	1.26E-10	1.62E-10	1.37E-10	2.34E-10	1.52E-10	3.06E-10
2	1.52E-10	1.53E-10	1.61E-10	1.97E-10	1.82E-10	2.73E-10	2.05E-10	3.57E-10
4	2.21E-10	2.21E-10	2.31E-10	2.67E-10	2.56E-10	3.42E-10	2.97E-10	4.40E-10
8	3.55E-10	3.52E-10	3.68E-10	4.00E-10	3.96E-10	4.71E-10	4.47E-10	5.85E-10

Figure 4.6: size 1 Data

The best fit planes for both t_{pdr} and t_{pdf} respectively gives the following Linear models.
Linear Model for Pdr is
delay= 36.684783 (K1)*Cload + 0.078597 (K2)*Transition + 74.575614 (K3))
Linear Model for Pdf is
= 35.032609 (K1)*Cload + 0.255048 (K2)*Transition + 90.674492 (K3)

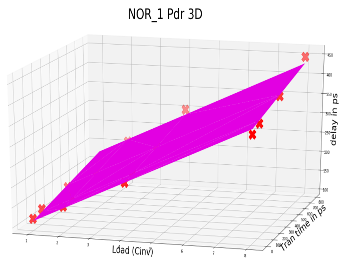


(a) NOR 1 Pdr

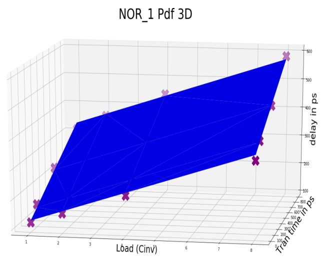


(b) NOR 1 Pdf

Figure 4.7: NOR 1 Plots



(a) NOR 1 Pdr 3D



(b) NOR 1 Pdf 3D

Figure 4.8: NOR 1 Plots

4.4.2 Size 2 and 4

The Data for Size for is found below. The graphs for them can be found in the plots folder. They generally follow the same trend as size 1.

Load (Cinv)	trans=0 tpdr	trans=0 tpdf	trans=100p tpdr	trans=100 tpdf	trans=400p tpdr	trans=400 tpdf	trans=800p tpdr	trans=800 tpdf
1	9.91E-11	1.06E-10	1.07E-10	1.48E-10	1.10E-10	2.19E-10	1.16E-10	2.90E-10
2	1.18E-10	1.24E-10	1.27E-10	1.67E-10	1.36E-10	2.40E-10	1.48E-10	3.19E-10
4	1.54E-10	1.59E-10	1.63E-10	2.04E-10	1.81E-10	2.81E-10	2.03E-10	3.66E-10
8	2.21E-10	2.29E-10	2.34E-10	2.75E-10	2.57E-10	3.51E-10	2.94E-10	4.53E-10

Figure 4.9: size 2 Data

The best fit planes for both t_{pdr} and t_{pdf} respectively gives the following Linear models.
For size 2 Linear Model for Pdr is

delay= 20.319348 (K1)*Cload + 0.050560 (K2)*Transition + 74.126800 (K3)

Linear Model for Pdf is

delay= 19.354348 (K1)*Cload + 0.245565 (K2)*Transition + 93.300228 (K3

For size 4: Linear Model for Pdr is

Load (Cinv)	trans=0 tpdr	trans=0 tpdf	trans=100p tpdr	trans=100 tpdf	trans=400p tpdr	trans=400 tpdf	trans=800p tpdr	trans=800 tpdf
1	8.84E-11	8.96E-11	9.70E-11	1.29E-10	1.01E-10	1.94E-10	1.10E-10	2.50E-10
2	1.01E-10	9.81E-11	1.08E-10	1.38E-10	1.15E-10	2.04E-10	1.28E-10	2.64E-10
4	1.21E-10	1.15E-10	1.29E-10	1.56E-10	1.41E-10	2.26E-10	1.59E-10	2.96E-10
8	1.57E-10	1.47E-10	1.66E-10	1.90E-10	1.86E-10	2.65E-10	2.13E-10	3.41E-10

Figure 4.10: size 4 Data

delay= 11.520870 (K1)*Cload + 0.042626 (K2)*Transition + 75.468352 (K3)
Linear Model for Pdf is
delay= 10.014565 (K1)*Cload + 0.212466 (K2)*Transition + 87.312638 (K3)

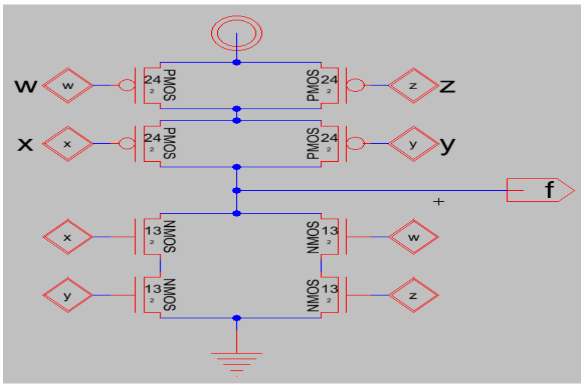
Chapter 5

Complex Function

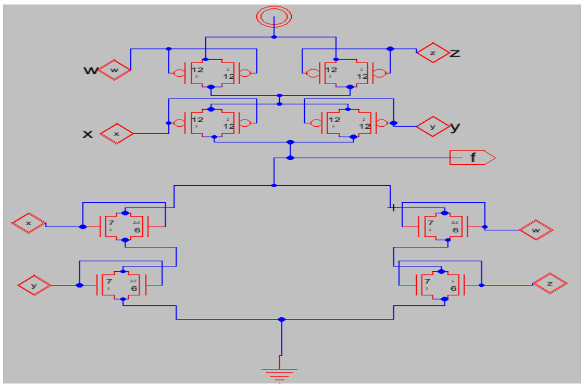
5.1 Schematics

5.1.1 Size 1

Original Sizes: NMOS 10λ , PMOS 24λ
Tuned Sizes: NMOS 13λ , PMOS 24λ



(a) Complex Function 1

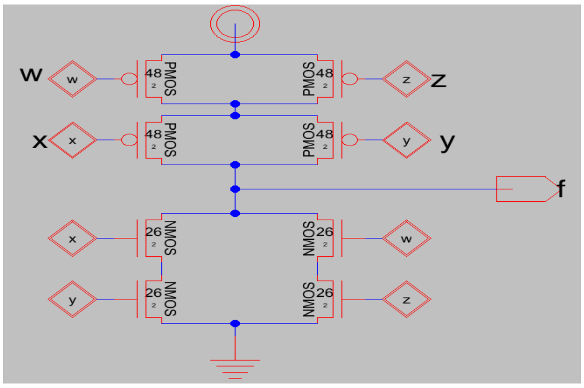


(b) Complex Function 1 folded

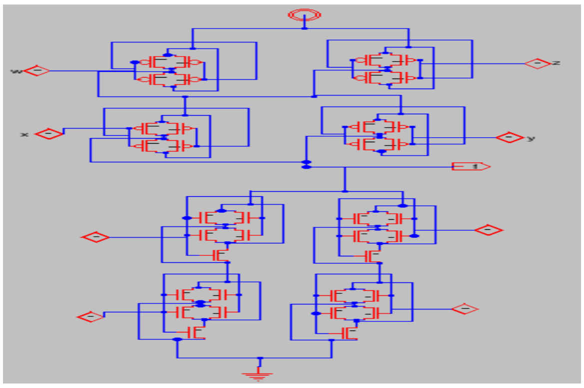
Figure 5.1: Complex Function size 1 Schematics

5.1.2 Size 2

Original Sizes: NMOS 20λ , PMOS 48λ
Tuned Sizes: NMOS 26λ , PMOS 48λ



(a) Complex Function 2

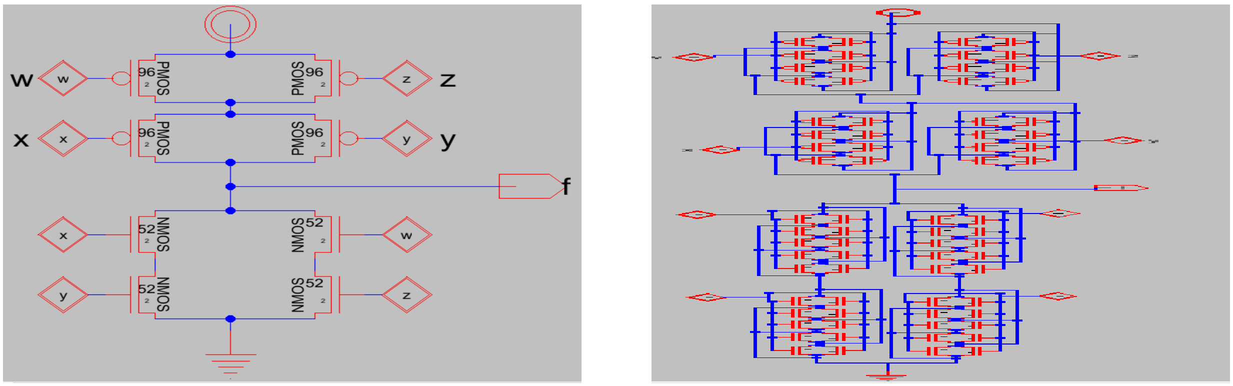


(b) Complex Function 2 folded

Figure 5.2: Complex Function Size 2 Schematics

5.1.3 Size 4

Original Sizes: NMOS 40λ , PMOS 96λ
Tuned Sizes: NMOS 52λ , PMOS 96λ



(a) Complex Function 4

(b) Complex Function 4 folded

Figure 5.3: Complex Function size 4 Schematics

5.2 Stick Diagrams

The stick diagram of the Complex Function is the same for all sizes.

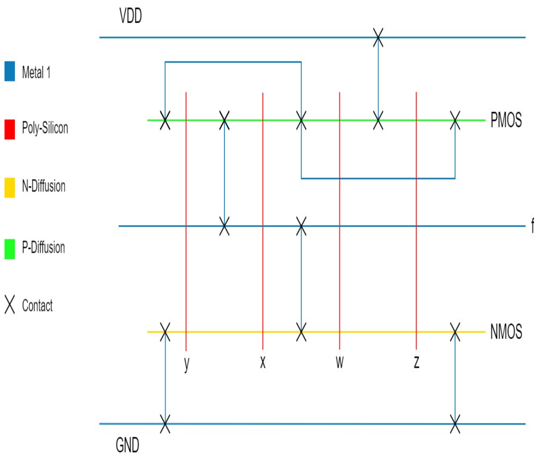


Figure 5.4: Complex Function Stick Diagram

5.3 Layouts

The figure below provides the Layout of the size 1 Complex Function. The dimensions of it is 56 width by 100 height. Note that those dimensions are of the minimized layout of the cell, before applying folding and making all cells match in height.

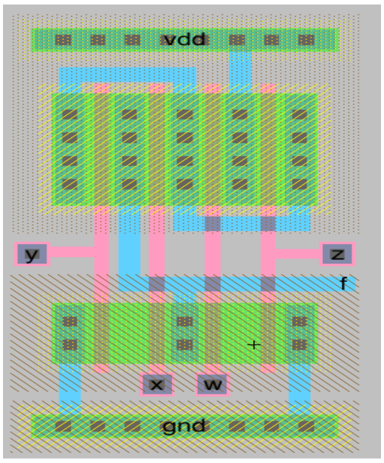


Figure 5.5: Complex Function Layout

5.4 Data Collection

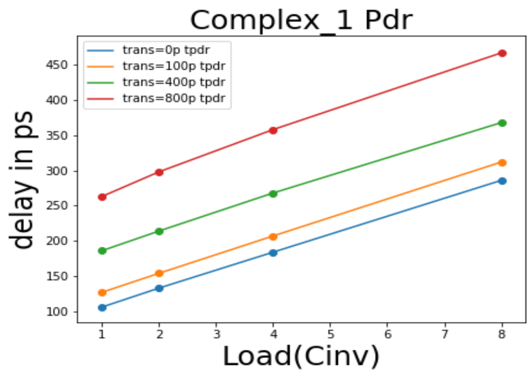
The simulations were run for every required Cload and Transition time for all sizes; the linear model was derived for t_{pdr} and t_{pdf} individually.

5.4.1 Size 1

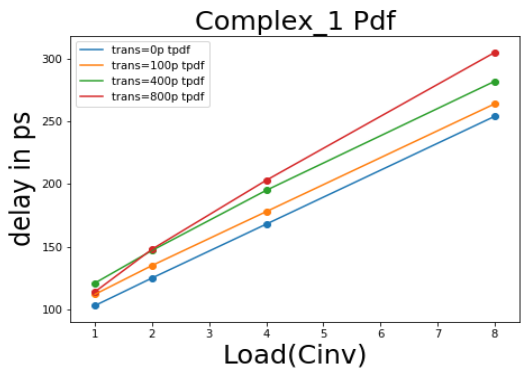
Load (Cinv)	trans = 0p tpdr	trans = 0p tpdf	trans = 100p tpdr	trans = 100p tpdf	trans = 400p tpdr	trans = 400p tpdf	trans = 800p tpdr	trans = 800p tpdf
1	1.06E-10	1.03E-10	1.27E-10	1.12E-10	1.86E-10	1.21E-10	2.63E-10	1.14E-10
2	1.33E-10	1.25E-10	1.54E-10	1.35E-10	2.14E-10	1.47E-10	2.98E-10	1.48E-10
4	1.84E-10	1.68E-10	2.07E-10	1.78E-10	2.68E-10	1.95E-10	3.58E-10	2.03E-10
8	2.86E-10	2.54E-10	3.12E-10	2.64E-10	3.68E-10	2.82E-10	4.67E-10	3.05E-10

Figure 5.6: Size 1 Data

The best fit planes for both t_{pdr} and t_{pdf} respectively gives the following Linear models.
Linear Model for t_{pdr} is
delay= 26.702174 (K1)*C_{load} + 0.210081 (K2)*Transition + 77.278138 (K3)
Linear Model for Pdf is
delay= 23.247826 (K1)*C_{load} + 0.035710 (K2)*Transition + 79.590007 (K3)

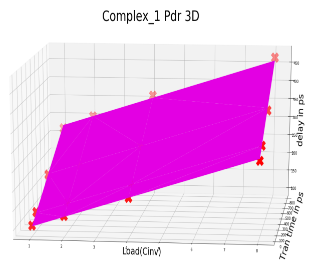


(a) Complex Function 1 t_{pdr}

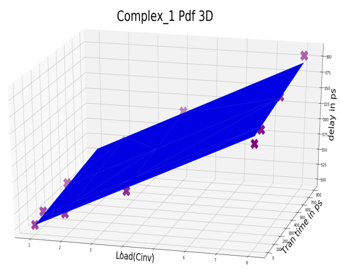


(b) Complex Function 1 t_{pdf}

Figure 5.7: Complex Function Size 1 Plots



(a) Complex Function 1 t_{pdr} 3D



(b) Complex Function 1 t_{pdf} 3D

Figure 5.8: Complex Function Size 1 best fit Plots

5.4.2 Sizes 2 and 4

The Data for Sizes 2 and 4 is found below. The graphs for them can be found in the plots folder. They generally follow the same trend as size 1.

Load (Cinv)	trans = 0p tpdr	trans = 0p tpdf	trans = 100p tpdr	trans = 100p tpdf	trans = 400p tpdr	trans = 400p tpdf	trans = 800p tpdr	trans = 800p tpdf
1	9.49E-11	9.30E-11	1.15E-10	1.02E-10	1.69E-10	1.09E-10	2.42E-10	1.01E-10
2	1.08E-10	1.04E-10	1.28E-10	1.14E-10	1.86E-10	1.24E-10	2.61E-10	1.17E-10
4	1.35E-10	1.27E-10	1.56E-10	1.37E-10	2.15E-10	1.50E-10	2.96E-10	1.49E-10
8	1.87E-10	1.70E-10	2.10E-10	1.81E-10	2.70E-10	1.99E-10	3.58E-10	2.10E-10

Figure 5.9: Complex Function Size 2 Data

The best fit planes for both t_{pdr} and t_{pdf} respectively gives the following Linear models.
For size 2:
Linear Model for t_{pdr} is
delay= 14.382826 (K1)*C_{load} + 0.196747 (K2)*Transition + 77.802951 (K3)
Linear Model for t_{pdf} is
delay= 12.641304 (K1)*C_{load} + 0.023887 (K2)*Transition + 81.519302 (K3)

Load (Cinv)	trans = 0p tpdr	trans = 0p tpdf	trans = 100p tpdr	trans = 100p tpdf	trans = 400p tpdr	trans = 400p tpdf	trans = 800p tpdr	trans = 800p tpdf
1	8.80E-11	8.80E-11	1.07E-10	9.70E-11	1.61E-10	1.03E-10	2.30E-10	9.52E-11
2	9.52E-11	9.39E-11	1.15E-10	1.03E-10	1.69E-10	1.10E-10	2.41E-10	1.04E-10
4	1.09E-10	1.05E-10	1.29E-10	1.15E-10	1.85E-10	1.25E-10	2.60E-10	1.21E-10
8	1.35E-10	1.28E-10	1.56E-10	1.38E-10	2.15E-10	1.52E-10	2.95E-10	1.53E-10

Figure 5.10: Complex Function Size 4 Data

For size 4:
Linear Model for t_{pdr} is
delay= 7.636087 (K1)*C_{load} + 0.186571 (K2)*Transition + 78.866609 (K3)
Linear Model for t_{pdf} is
delay= 6.698913 (K1)*C_{load} + 0.015969 (K2)*Transition + 84.132786 (K3)

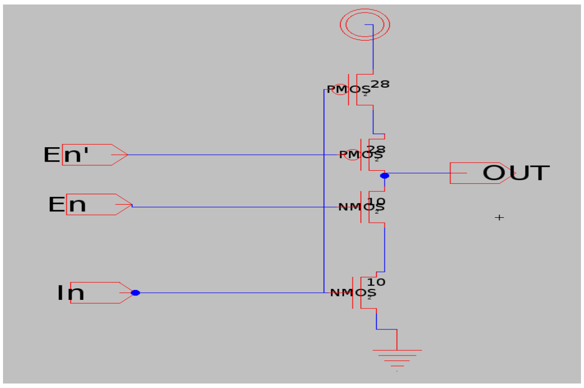
Chapter 6

Tristate Inverter

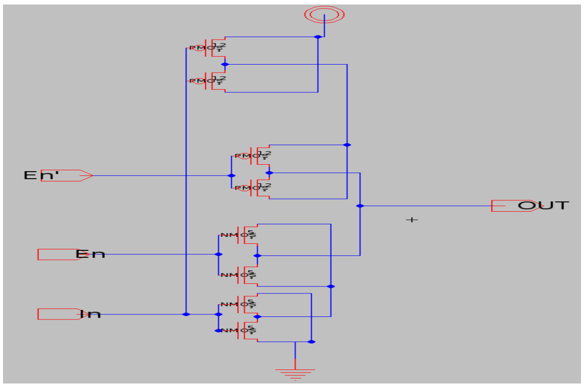
6.1 Schematics

6.1.1 Size 1

Original Sizes: NMOS 10λ , PMOS 24λ
Tuned Sizes: NMOS 13λ , PMOS 28λ



(a) Tristate Inverter 1

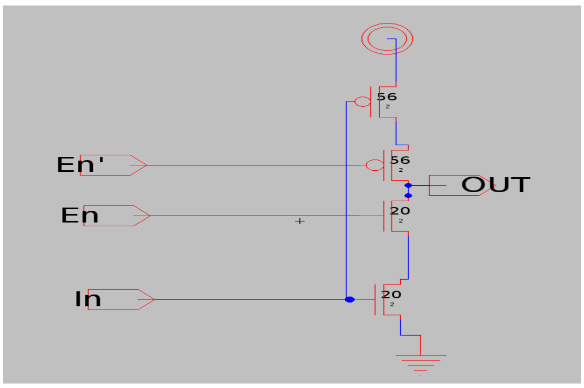


(b) Tris

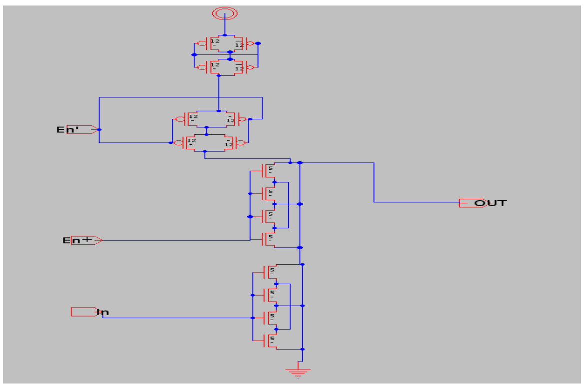
Figure 6.1: Tristate Inverter Size 1 Schematics

6.1.2 Size 2

Original Sizes: NMOS 20λ , PMOS 48λ
Tuned Sizes: NMOS 20λ , PMOS 56λ



(a) Tristate inverter 2

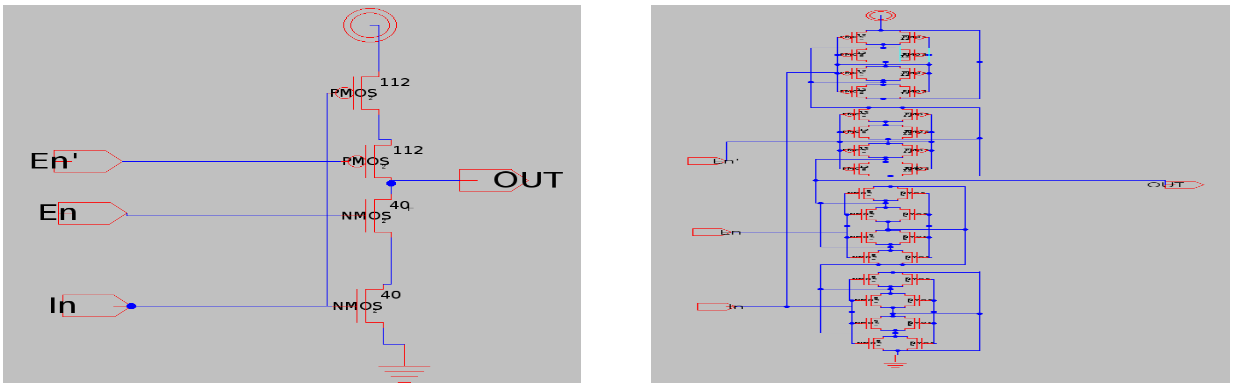


(b) Tristate inverter size 2 folded

Figure 6.2: Tristate inverter Size 2 Schematics

6.1.3 Size 4

Original Sizes: NMOS 40λ , PMOS 96λ
Tuned Sizes: NMOS 40λ , PMOS 112λ



(a) Tristate Inverter 4

(b) Tristate In 4 folded

Figure 6.3: Complex Function size 4 Schematics

6.2 Stick Diagrams

The stick diagram of the Complex Function is the same for all sizes.

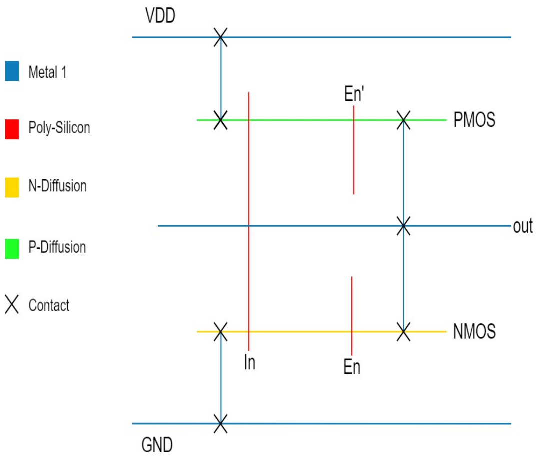


Figure 6.4: Tristate stick diagram

6.3 Layouts

The figure below provides the Layout of the size 1 Complex Function. The dimensions of it is 56 width by 100 height. Note that those dimensions are of the minimized layout of the cell, before applying folding and making all cells match in height.

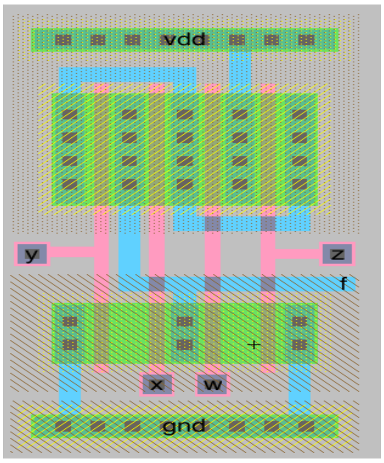


Figure 6.5: Complex Function Layout

6.4 Data Collection

The simulations were run for every required Cload and Transition time for all sizes; the linear model was derived for t_{pdr} and t_{pdf} individually.

6.4.1 Size 1

Load (Cinv)	trans = 0p tpdr	trans = 0p tpdf	trans = 100p tpdr	trans = 100p tpdf	trans = 400p tpdr	trans = 400p tpdf	trans = 800p tpdr	trans = 800p tpdf
1	1.06E-10	1.03E-10	1.27E-10	1.12E-10	1.86E-10	1.21E-10	2.63E-10	1.14E-10
2	1.33E-10	1.25E-10	1.54E-10	1.35E-10	2.14E-10	1.47E-10	2.98E-10	1.48E-10
4	1.84E-10	1.68E-10	2.07E-10	1.78E-10	2.68E-10	1.95E-10	3.58E-10	2.03E-10
8	2.86E-10	2.54E-10	3.12E-10	2.64E-10	3.68E-10	2.82E-10	4.67E-10	3.05E-10

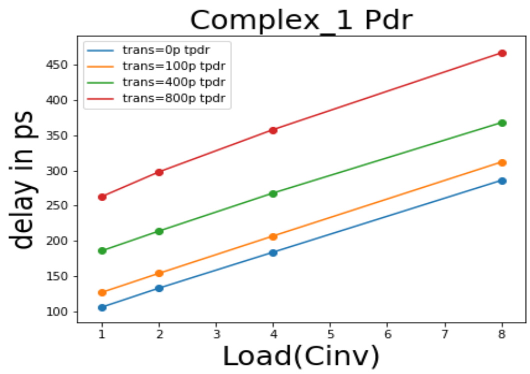
Figure 6.6: Size 1 Data

The best fit planes for both t_{pdr} and t_{pdf} respectively gives the following Linear models.
Linear Model for t_{pdr} is

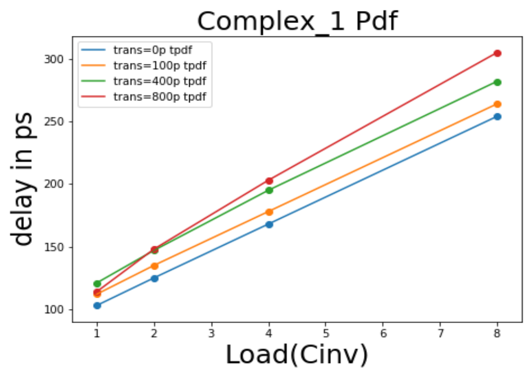
delay= 26.702174 (K1)*C_{load} + 0.210081 (K2)*Transition + 77.278138 (K3)

Linear Model for Pdf is

delay= 23.247826 (K1)*C_{load} + 0.035710 (K2)*Transition + 79.590007 (K3)

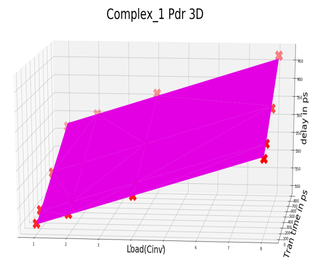


(a) Complex Function 1 t_{pdr}

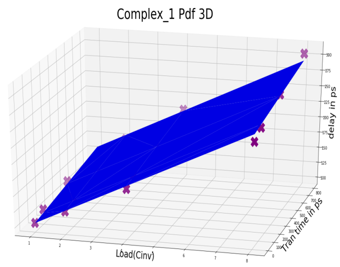


(b) Complex Function 1 t_{pdf}

Figure 6.7: Complex Function Size 1 Plots



(a) Complex Function 1 t_{pdr} 3D



(b) Complex Function 1 t_{pdf} 3D

Figure 6.8: Complex Function Size 1 best fit Plots

6.4.2 Sizes 2 and 4

The Data for Sizes 2 and 4 is found below. The graphs for them can be found in the plots folder. They generally follow the same trend as size 1.

Load (Cinv)	trans = 0p tpdr	trans = 0p tpdf	trans = 100p tpdr	trans = 100p tpdf	trans = 400p tpdr	trans = 400p tpdf	trans = 800p tpdr	trans = 800p tpdf
1	9.49E-11	9.30E-11	1.15E-10	1.02E-10	1.69E-10	1.09E-10	2.42E-10	1.01E-10
2	1.08E-10	1.04E-10	1.28E-10	1.14E-10	1.86E-10	1.24E-10	2.61E-10	1.17E-10
4	1.35E-10	1.27E-10	1.56E-10	1.37E-10	2.15E-10	1.50E-10	2.96E-10	1.49E-10
8	1.87E-10	1.70E-10	2.10E-10	1.81E-10	2.70E-10	1.99E-10	3.58E-10	2.10E-10

Figure 6.9: Complex Function Size 2 Data

The best fit planes for both t_{pdr} and t_{pdf} respectively gives the following Linear models.
For size 2 Linear Model for t_{pdr} is
delay= 14.382826 (K1)*C_{load} + 0.196747 (K2)*Transition + 77.802951 (K3)
Linear Model for t_{pdf} is
delay= 23.247826 (K1)*C_{load} + 0.035710 (K2)*Transition + 79.590007 (K3)
For size 4: Linear Model for Pdr is

Load (Cinv)	trans=0 tpdr	trans=0 tpdf	trans=100p tpdr	trans=100 tpdf	trans=400p tpdr	trans=400 tpdf	trans=800p tpdr	trans=800 tpdf
1	8.84E-11	8.96E-11	9.70E-11	1.29E-10	1.01E-10	1.94E-10	1.10E-10	2.50E-10
2	1.01E-10	9.81E-11	1.08E-10	1.38E-10	1.15E-10	2.04E-10	1.28E-10	2.64E-10
4	1.21E-10	1.15E-10	1.29E-10	1.56E-10	1.41E-10	2.26E-10	1.59E-10	2.96E-10
8	1.57E-10	1.47E-10	1.66E-10	1.90E-10	1.86E-10	2.65E-10	2.13E-10	3.41E-10

Figure 6.10: size 4 Data

delay= 11.520870 (K1)*Cload + 0.042626 (K2)*Transition + 75.468352 (K3)
Linear Model for Pdf is
delay= 10.014565 (K1)*Cload + 0.212466 (K2)*Transition + 87.312638 (K3)