Design and Implementation of an 8-Bit SAR ADC

A Project Report of

ECE 703 VLSI DATA CONVERTERS

Under the Guidance of

Dr. Kalpana Bhat

Authors:

Anush (201EC108)
Omkar Kamath (201EC140)
Aniket Uppin (201EC169)

April 15, 2024

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
NATIONAL INSTITUTE OF TECHNOLOGY KARNATAKA
SURATHKAL, MANGALORE - 575025

Contents

1 Introduction

In an ever-growing digital world, the vast majority of computers and devices work in the digital domain since it is easier to manipulate, store and display data. The devices responsible for this processing are the data-acquisition-systems (DAS), in which analog-to-digital converters (ADCs) play a fundamental role.
Analog-to-Digital Converters (ADCs) are essential components in modern electronic systems, bridging the gap between the analog and digital domains. They play a crucial role in a wide range of applications, including communication systems, signal processing, medical instrumentation, and consumer electronics. Among the various ADC architectures, the Successive Approximation Register (SAR) ADC has emerged as a popular choice due to its simplicity, low power consumption, and high-resolution capabilities.

The need for high-performance, low-power ADCs has been steadily increasing, driven by the growing demand for digital processing and the integration of analog and digital components on a single chip. SAR ADCs, with their efficient architecture and flexible design, have become a preferred solution for many applications that require moderate sampling rates and high resolution, such as audio processing, sensor interfaces, and data acquisition systems.

1.1 Objective

The main objectives of this project are:

- To design and implement an 8-bit SAR ADC with a sampling rate of 1 MSPS and a reference voltage of 2V using a 0.25 um technology process.
- To optimize the design parameters, such as the reference voltage, input range, and power consumption, to meet the desired performance specifications.
- To simulate and analyze the performance of the designed SAR ADC, including the calculation of key metrics such as Differential Non-Linearity (DNL), Integral Non-Linearity (INL), Signal-to-Noise and Distortion Ratio (SNDR), and Effective Number of Bits (ENOB).

2 Architecture Design

The architectural design of the 8-bit SAR ADC consists of Sample and Hold block, a Binary-weighted split-capacitive DAC, a comparator and a SAR logic generator.

The comparator was designed to have a high gain and low input-referred noise, allowing it to detect voltage differences as small as 1/2 * VLSB (Voltage Least Significant Bit).

2.1 Sample-and-Hold

In the tracking mode, when the sampling signal is high and the switch is connected, the analog input signal is tracked. The captured value is then held when the sampling signal turns to low in the hold mode. In this case, sample and hold provides a constant voltage at the input of the ADC during conversion. The designed simple and hold circuit is shown in Figure 1.

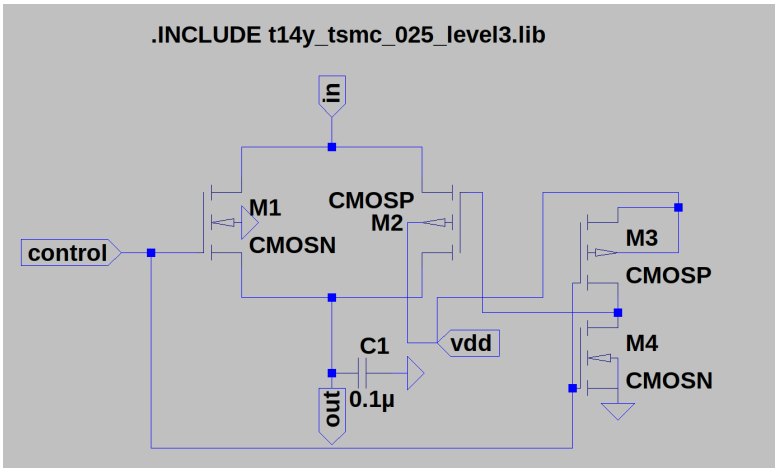

Figure 1: A graph of something.

Transmission gate is used to implement a switch. The clock signal is provided as control input to the switch. The output response of the switch to the input sine wave of 50KHz, is shown in Figure 2.

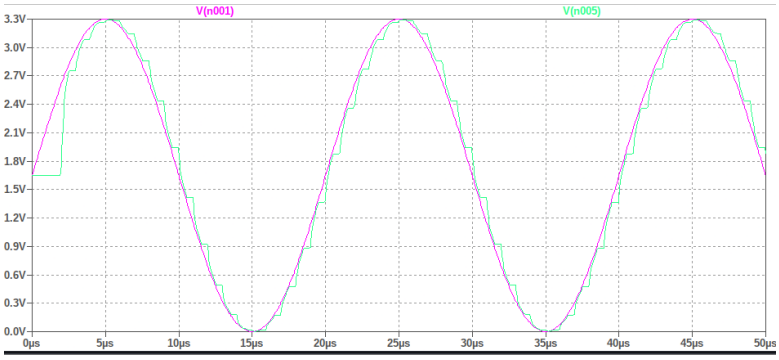

Figure 2: A graph of something.

2.2 DAC

The digital to analog converter (DAC) converts the digital word at the output of the SAR logic to an analog value. Then in the comparator, this value is compared to the input signal. Charge redistribution DACs are the commonly used as they can be fabricated easily. They consume less power and induce less mismatch errors compared to the resistive based DAC.

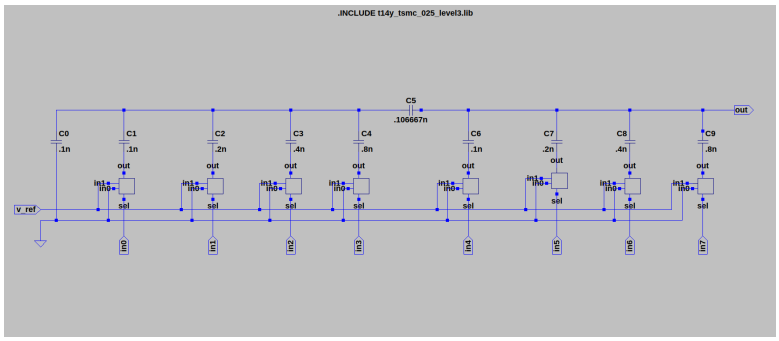

Figure 3: A graph of something.

Figure 3 shows the 8-bit split capacitive DAC that we have implemented. The split capacitive array helps mitigate the large capacitance sizes as in the 8-bit Binary weighted DAC. The DAC was tested

by feeding an up counting sequence starting from 0 to 255. The output of the DAC rises from 0 to (255/256)*vlsb as evident in Figure 4.

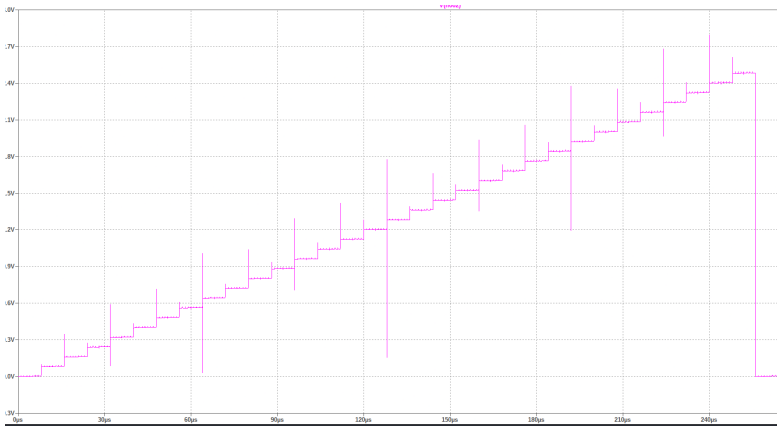

Figure 4: A graph of something.

2.3 Comparator

The comparator block receives input signals input voltage value and accumulated voltage value from the SAR logic block. It compares the 2 signal values and in turn outputs a single bit depicting the comparison of the 2 input signals. This output is then fed to the SAR logic block as an input for the next clock cycle. The comparator was designed to have a high gain and low input-referred noise, allowing it to detect voltage differences as small as $\frac{V_{lsb}}{2}$

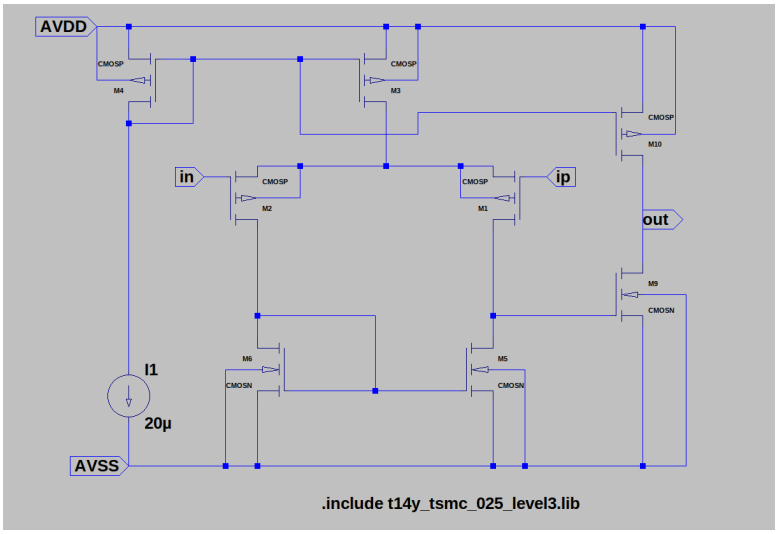

Figure 5: Comparator Circuit

We can correctly see the working of the comparator through the help of the given images. For the given differential input voltage (figure 6), we observe the following output (figure 7).

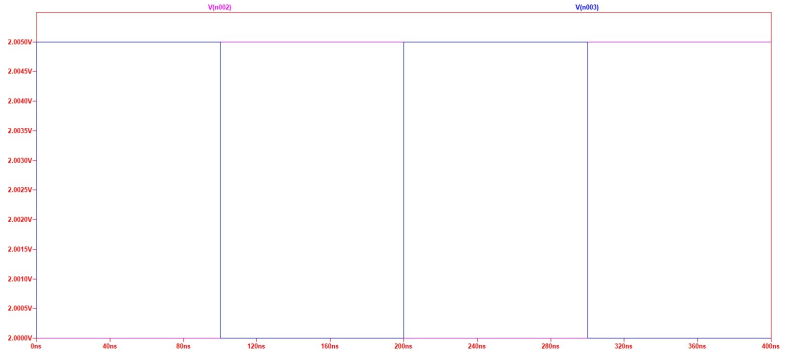

Figure 6: Differential Input Voltage

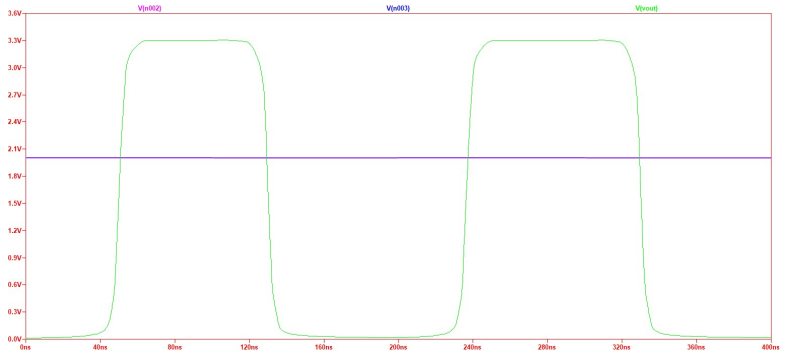

Figure 7: Output observed of the Comparator

We also calculated the frequency response of the comparator which is depicted in the image given below (figure 8).

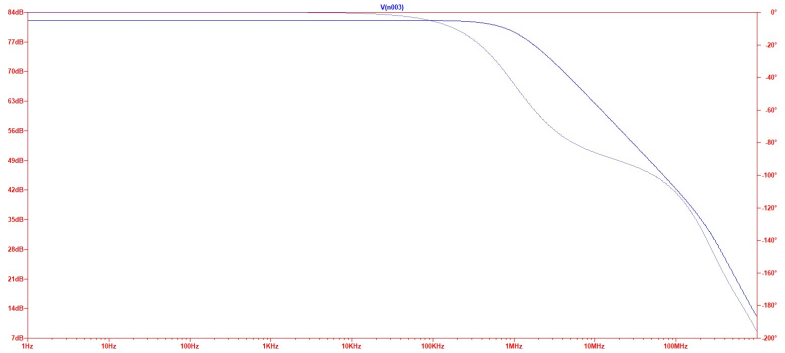

Figure 8: Frequency Response of the Comparator circuit

2.4 SAR Logic

SAR control logic implements the binary search algorithm and determines the value of bits sequentially based on the result of the comparator. The proposed design of the SAR logic is shown in Figure 9.

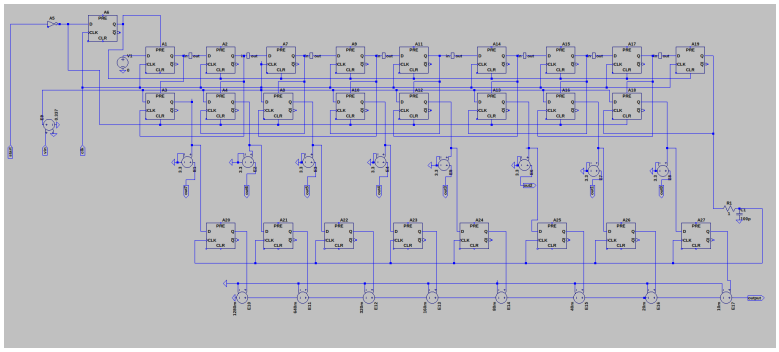

Figure 9: A graph of something.

The SAR logic begins by setting the most-significant bit(MSB) to 1, when start signal goes high and sets all the other bits to 0.Then, if the feedback value of the DAC is greater than the reference, the proposed change is accepted, increasing the feedback value by $V_{ref}/2^{N+1-k}$, where k is the bit number, and the bit remains set un- til the next conversion of the input. Otherwise, the SAR refuses the change, and the bit is reset again to 0, decreasing the feedback value by $V_{ref}/2^{N+1-k}$. The above process is continued for 8 clock cycles until the least-significant bit(lsb) is checked. The last cycle is used for storing the results of the complete conversion. The above functionality is illustrated in Figure 10.

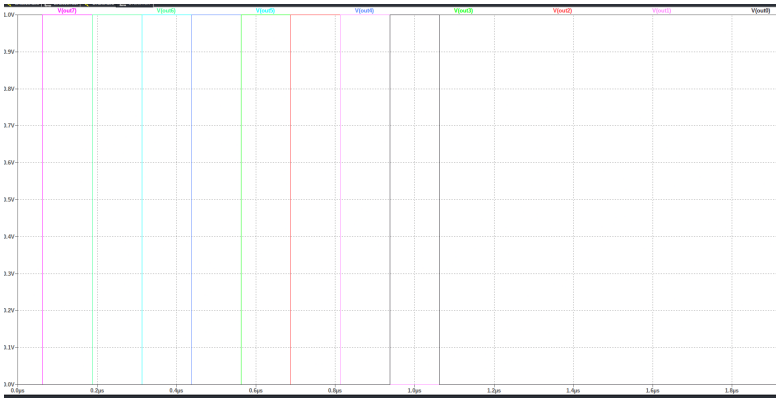

Figure 10: A graph of something.

3 Experimental Setup

The individual subcircuits were then integrated into a complete SAR ADC system as shown in Figure 11.

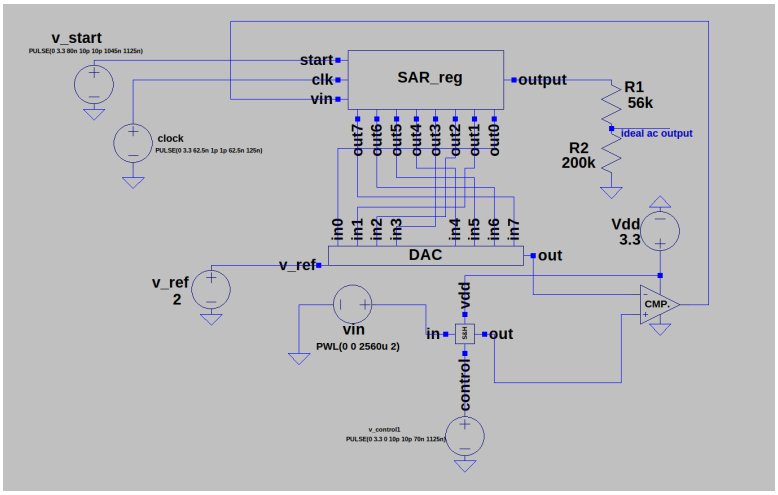

Figure 11: A graph of something.

The interconnections between the sub-blocks were carefully designed to ensure proper timing and signal integrity. The complete SAR ADC system was simulated using LTspice to verify its functionality and performance. The ADC was tested by applying a ramp signal as input, with each code subjected to 10 hits. This means that the slope of the signal is determined by

$$slope = \frac{V_{lsb}}{10 * t_s}$$

where V_{lsb} represents voltage value that corresponds to the least significant bit, and t_s represents samplting time. The below Figure 12 illustrates the output of the SAR ADC.

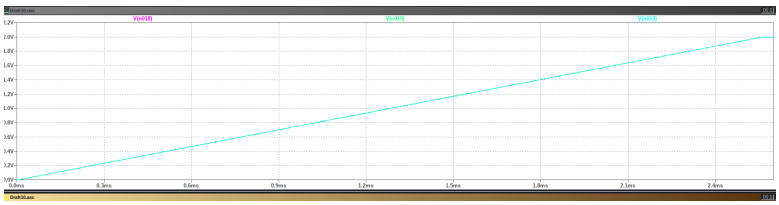

Figure 12: A graph of something.

As seen in Figure 12, the offset error is 0 and the gain error is also negligible. The plot shows voltages at three nodes, the pink plot shows the input signal, the green plot shows the held input voltage, and the cyan colored plot shows the output from the SAR register, reconstructed by the ideal DAC.

4 Results

The input and the output values were captured at each time step and written into a text file. For measuring INL and DNL a ramp signal was fed as an input signal with a slope of $V_{lsb}/(10 * t_s)$, where 10 represents the number of hits. We then prepared a python file to extract the output reconstructed by the ideal DAC and calculated the INL and DNL values for each of the 256 digital codes, and are shown in Figure 13 and Figure 14 respectively.

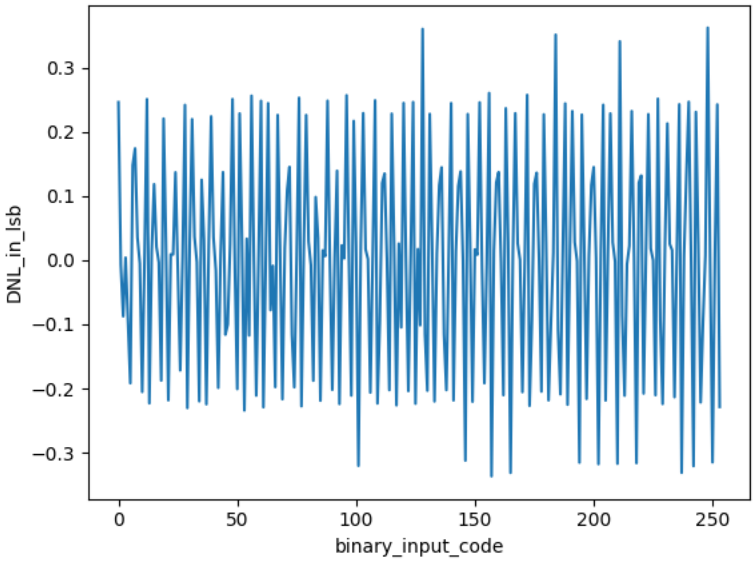

Figure 13: A graph of something.

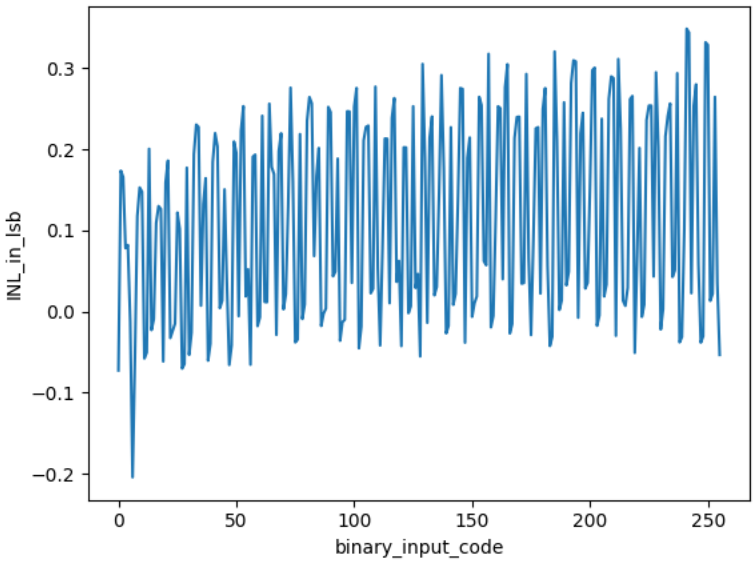

Figure 14: A graph of something.

As shown above, we have successfully achieved the INL and DNL values less than $\frac{V_{lsb}}{2}$. For obtaining SNDR and ENOB, we gave a sine wave input excitation to the ADC with a full scale voltage of 2V.The output of the ADC is shown in Figure 15.

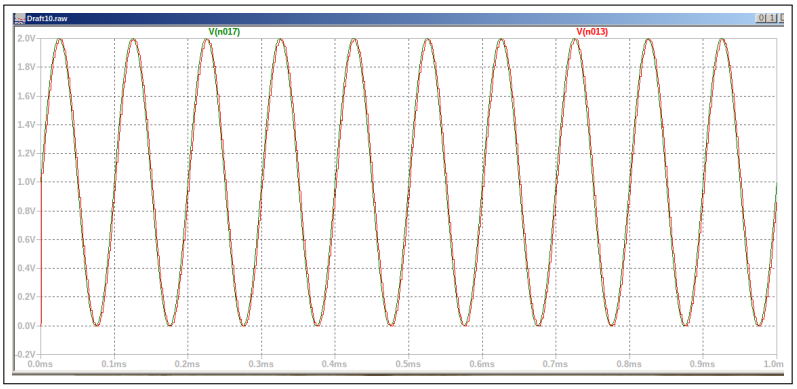

Figure 15: Output for sine wave excitation.

We captured the signal as well as noise amplitudes from the Fast Fourier Transform plot which is shown in Figure 16.

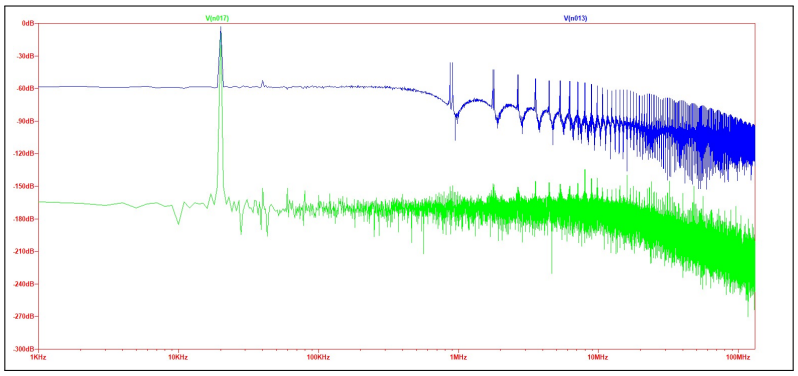

Figure 16: A graph of something.

The input frequency is swept from 10Khz to 320KHz by doubling the previous frequency. The captured data is then processed by a python file to extract signal power,noise and the distortion power. The SNDR values is then calculated and is shown in Figure 17 and Figure 18

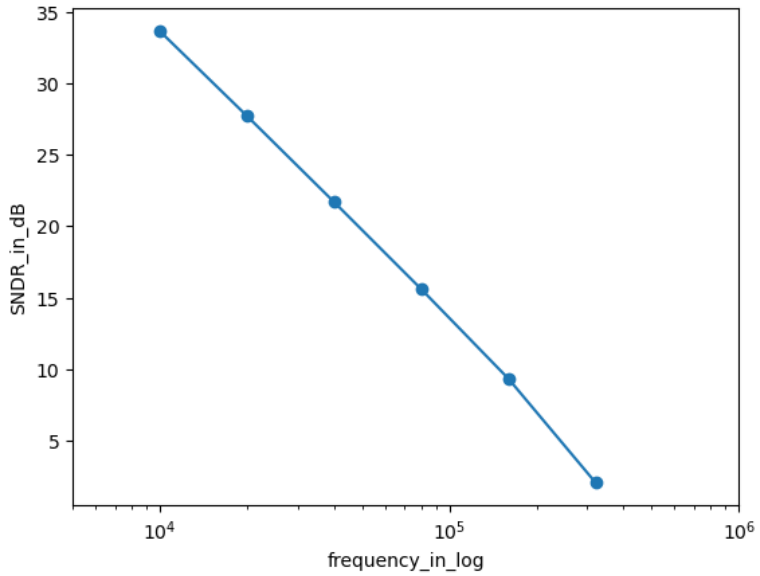

Figure 17: SNDR vs log frequency plot.

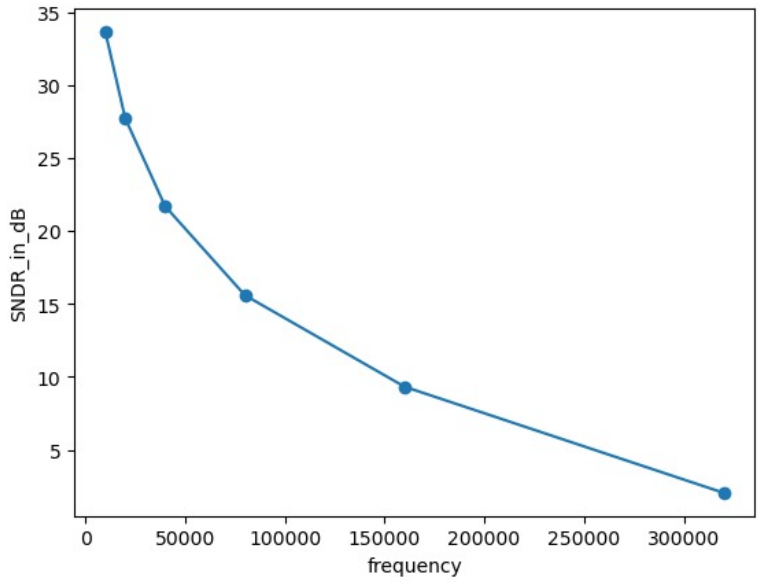

Figure 18: SNDR vs frequency plot.

The Effective number of bits(ENOB) value can be calculated as $ENOB = (SNDR - 1.76)/6.02$ For our design the ENOB value at 10KHz comes out to be 5.3.

5 Conclusion

We successfully designed and simulated an 8-bit SAR ADC in 250nm technology. The ADC achieved a sampling rate of 1 Msps and a reference voltage of 2 V. We verified sub-block designs and functionality through LTspice simulations. The implemented ADC demonstrated successful conversion of ramp and sine wave inputs. Performance analysis confirmed good linearity with INL and DNL values below $V_{lsb}/2$. The simulated SNDR plot and ENOB value met the design objectives. Overall, this project demonstrates the feasibility of designing a high-performance SAR ADC using the described approach.

Notes:

The link for the ppt is pasted below:
https://drive.google.com/drive/folders/12HyN3ESouniTBNpZioV4Rm2ToJDAl6FN?usp=sharing

Contributions:
Anush: Primary focus on designing the Comparator.
Aniket: Primary focus on designing the SAR logic and Sample and Hold block.
Omkar: Primary focus on designing the DAC.
Rest of the work is done by everybody.

6 References

1. Akkinapally, Sesha Smuruti, "Design and Implementation of 8 Bit Successive Approximation ADC at1MHZ" (2006). Open Access Master's Theses. Paper 1001. https://digitalcommons.uri.edu/theses/1001

2. Ahmed S, Kakkar V. Modeling and simulation of an eight-bit auto-configurable successive approximation register analog-to-digital converter for cardiac and neural implants. SIMULATION. 2018;94(1):11-29. doi:10.1177/0037549717716537

3. W. Pengyu, G. Bo, Q. Zheng, G. Min and T. Ping, "An 8-Bit High Speed Successive Approximation Analog-to-Digital Converter," 2018 IEEE Asia Pacific Conference on Postgraduate Research in Microelectronics and Electronics (PrimeAsia), Chengdu, China, 2018, pp. 5-8, doi: 10.1109/PRIMEASIA.2018.8597951.

4. V. P. Singh, G. K. Sharma and A. Shukla, "Power efficient SAR ADC designed in 90 nm CMOS technology," 2017 2nd International Conference on Telecommunication and Networks (TEL-NET), Noida, India, 2017, pp. 1-5, doi: 10.1109/TEL-NET.2017.8343542.