

# Specification Document

Omkar Girish Kamath

November 19, 2022

## Contents

<b>1</b>	<b>Processor</b>	<b>2</b>
1.1	Instruction Set . . . . .	2
1.2	Input Output Interface . . . . .	3
1.3	Timing Diagrams . . . . .	3
<b>2</b>	<b>Memory</b>	<b>3</b>
2.1	Description . . . . .	3
2.2	I/O of the Memory device . . . . .	4

# 1 Processor

## 1.1 Instruction Set

In this instruction syntax X=Not used, K=Constant, A=Instruction Address, P=Data Address

Table 1: Instruction Set of the Simple CPU

Opcode	Instruction	RTL
Load ACC kk	0000 XXXX KKKKKKKK	ACC <- KK
Add ACC kk	0100 XXXX KKKKKKKK	ACC <- ACC + KK
And ACC kk	0001 XXXX KKKKKKKK	ACC <- ACC & KK
Sub ACC kk	0110 XXXX KKKKKKKK	ACC <- ACC - KK
Input ACC pp	1010 XXXX PPPPPPPP	ACC <- M[PP]
Output ACC pp	1110 XXXX PPPPPPPP	M[PP] <- ACC
Jump U aa	1000 XXXX AAAAAAAAAA	PC <- AA
Jump Z aa	1001 00XX AAAAAAAAAA	IF Z=1 PC <- AA ELSE PC <- PC + 1
Jump C aa	1001 10XX AAAAAAAAAA	IF C=1 PC <- AA ELSE PC <- PC + 1
Jump NZ aa	1001 01XX AAAAAAAAAA	IF Z=0 PC <- AA ELSE PC <- PC + 1
Jump NC aa	1001 11XX AAAAAAAAAA	IF C=0 PC <- AA ELSE PC <- PC + 1

Here '>' indicates updated with .

The processor has an extra cycle to save on hardware which would have been required for incrementing the PC . So the processor follows **fetch-decode-execute-increment** cycle .

## 1.2 Input Output Interface

Table 2: I/O interface of the processor

Signals	Type	Size	Active	Description
clk	input	1 bit	-	square wave used to maintain synchronosity in the device
c_e	input	1 bit	High	enables the chip for input data
rst	input	1 bit	Low	resets the chip to a pre decided state
[15:0] d_in	input	16 bits	-	the instruction sent from memory
[7:0] adrs	output	8 bits	-	the address of the required instruction sent to memory
rw	output	1 bit	-	read write control signal sent to memory
[7:0] d_out	output	8 bits	-	output data from the processor

## 1.3 Timing Diagrams

# 2 Memory

## 2.1 Description

**Size of RAM -> 4 Kilobytes**

RAM used is DDR5 Synchronous Dynamic RAM .

Instruction length is *16 bit* , maximum number of instructions and data than can be stored is **256** (address 0 to 255). Address length required is 8 bits.

## 2.2 I/O of the Memory device

Table 3: I/O of the Memory device

Signals	Type	Size	Active	Description
clk	input	1 bit	-	square wave used to maintain synchronosity in the device
c_e	input	1 bit	High	enables the memory functioning
rst	input	1 bit	Low	resets the memory to a pre decided state
[15:0] mem_in	input	16 bits	-	the data sent by chip
[7:0] adrs	input	8 bits	-	the address of the required instruction
rw	input	1 bit	-	read write control signal sent to memory
[15:0] mem_out	output	16 bits	-	output data/instruction from the memory