Specification Document

Omkar Girish Kamath

November 18, 2022

Contents

1 Processor

1.1 Instruction Set

In this instruction syntax X=Not used, K=Constant, A=Instruction Address, P=Data Address

Table 1: Instruction Set of the Simple CPU

Opcode	Instruction	RTL
Load ACC kk	0000 XXXX KKKKKKKK	ACC <- KK
Add ACC kk	0100 XXXX KKKKKKKK	ACC <- ACC + KK
And ACC kk	0001 XXXX KKKKKKKK	ACC <- ACC & KK
Sub ACC kk	0110 XXXX KKKKKKKK	ACC <- ACC - KK
Input ACC pp	1010 XXXX PPPPPPPP	ACC <- M[PP]
Output ACC pp	1110 XXXX PPPPPPPP	M[PP] <- ACC
Jump U aa	1000 XXXX AAAAAAAA	PC <- AA
Jump Z aa	1001 00XX AAAAAAAA	IF Z=1 PC <- AA ELSE PC <- PC + 1

continued on next page

Table 1: (*continued from previous page)*

Opcode	Instruction	RTL
Jump C aa	1001 10XX AAAAAAAA	IF C=1 PC <- AA ELSE PC <- PC + 1
Jump NZ aa	1001 01XX AAAAAAAA	IF Z=0 PC <- AA ELSE PC <- PC + 1
Jump NC aa	1001 11XX AAAAAAAA	IF C=0 PC <- AA ELSE PC <- PC + 1

Here '->' indicates updated with .

The processor has an extra cycle to save on hardware which would have been required for incrementing the PC . So the processor follows **fetch-decode-execute-increment** cycle .

1.2 Input Output Interface

Table 2: I/O signals

Signals	type	size	description

2 Memory

2.1 Description

Size of RAM -> 4 Kilobytes
RAM used is DDR5 Synchronous Dynamic RAM .
Instruction length is *16 bit* , maximum instructions and data than can be stored is **256**. Address length required is 8 bits.

2.2 I/O of RAM