Specification Document

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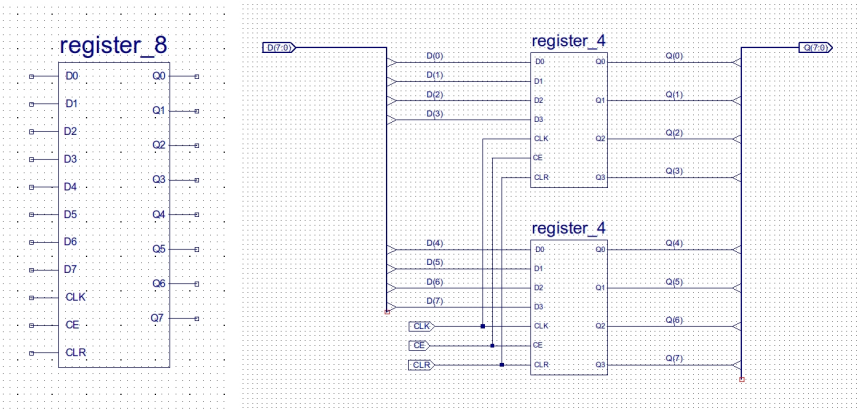


Figure 1:

8 bit register used to store the address **current** instruction being executed. It is incremented after every *fetch-decode-execute-increment* cycle .

1.2.2 Interface

```
module pc (
d,
clk,
ce,
clr,
q
);

input [7:0] d ;
input clk ;
input ce ;
input clr ;
```

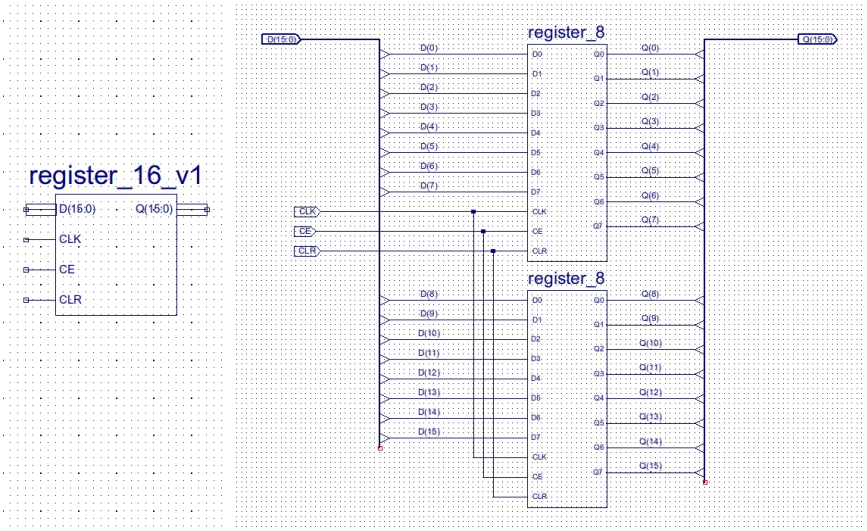
output [7:0]q;

signal name	type	size
d	input	8 bits
clk	input	1 bit
ce	input	1 bit
clr	input	1 bit
q	output	8 bits

1.3 Instruction Register

1.3.1 Theory

Instruction Register (IR) : **16** bit register, updated at the end of the fetch phase with the instruction to be processed (decoded and executed).



1.3.2 Interface

module ir (
d,
clk,
ce,
clr,
q

);

```
input [15:0] d ;
input clk ;
input ce ;
input clr ;
output [15:0] q ;
```

signal name	type	size
d	input	16 bits
clk	input	1 bit
ce	input	1 bit
clr	input	1 bit
q	output	16 bits

1.4 Decoder

1.4.1 Theory

1.4.2 Interface

Name	size	function	type
mux_a	1	ALU A input MUX control	output
mux_b	1	ALU B input MUX control	output
mux_c	1	address MUX control, selecting PC or IR	output
en_{da}	1	accumulator (ACC) register update control	output
en_{pc}	1	program counter (PC) register update control	output
en_{ir}	1	instruction register (IR) update control	output
ram_{we}	1	memory write enable control	output
alu_c	5	ALU control line	output
ir	8	high byte of instruction register, contains opcode	input
zero	1	connected to ALU output, if 1 indicates result is zero	output
clk	1	system clock	input
ce	1	clock enable, normally set to 1, if set to 0 processor will HALT	input
clr	1	system reset, if pulsed high system will be reset	input

MUX_A : output, ALU A input MUX control

MUX_B : output, ALU B input MUX control

MUX_C : output, address MUX control, selecting PC or IR

EN_{DA} : output, accumulator (ACC) register update control

EN_{PC} : output, program counter (PC) register update control

EN_{IR} : output, instruction register (IR) update control

RAM_{WE} : output, memory write enable control

ALU_{S0} : output, ALU control line

ALU_{S1} : output, ALU control line

ALU_{S2} : output, ALU control line

ALU_{S3} : output, ALU control line

ALU_{S4} : output, ALU control line (**combining all the ALU control lines we get a 5 bit out alu_c signal**)

IR : input bus, 8bits, high byte of instruction register, contains opcode

ZERO : input, driven by 8bit NOR gate connected to ALU output, if 1 indicates result is zero

CARRY : input, driven by carry out (Cout) of ALU

CLK : input, system clock

CE : input, clock enable, normally set to 1, if set to 0 processor will HALT

CLR : input, system reset, if pulsed high system will be reset

1.5 Accumulator

1.5.1 Theory

Accumulator (ACC) : *8* bit register, a general purpose data register, providing data (operand) to be processed by the ALU and used to **store** any result produced. Note, we can only store one 8 bit value at a time on the processor, other data values will need to be buffered in external memory.

1.5.2 Interface

module pc (
d,
clk,
ce,
clr,

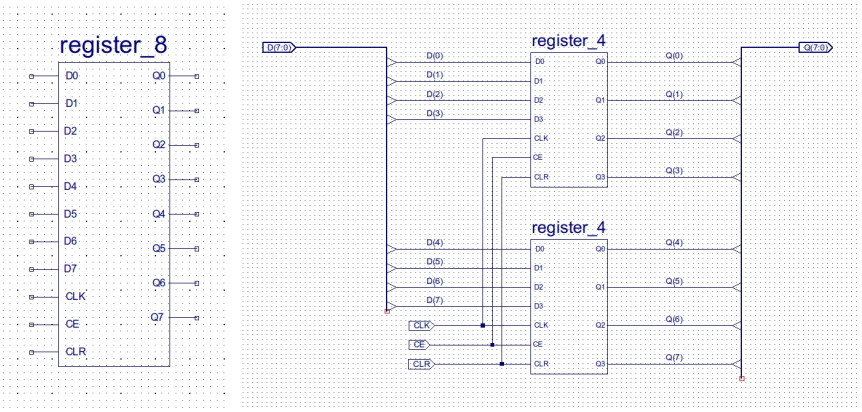


Figure 2:

q
);

input [7:0] d ;
input clk ;
input ce ;
input clr ;
output [7:0]q;

signal name	type	size
d	input	8 bits
clk	input	1 bit
ce	input	1 bit
clr	input	1 bit
q	output	8 bits

1.6 ALU

1.6.1 Theory

1.6.2 Interface

1.7 MUX

1.7.1 $\text{MUX}_{\text{IR to ALU}}$

1.7.2 $\text{MUX}_{\text{PC to ALU}}$

1.7.3 $\text{MUX}_{\text{Address in RAM}}$