Specification

Synchronous FIFO

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1 Operation

The high-level operation of a synchronous FIFO can be modeled by a circular buffer as shown:

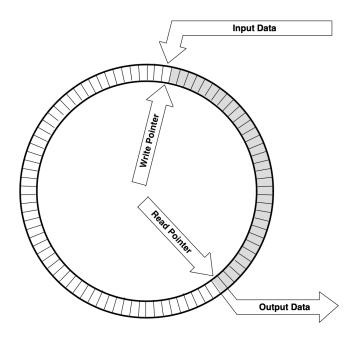


Figure 1: Circular buffer modelling a FIFO.

Two operations are defined: reading and writing to the FIFO. Writing input data involves:

- Copying the input data to the location write pointer points to.
- Incrementing write pointer.

Reading data involves:

- Reading out the data at location read pointer.
- Incrementing read pointer.

"Synchronous" refers to the fact that there is a single common free-running clock for both reading and writing. When to read and write is given by two signals: a read enable and a write enable. Our FIFO has 64 addresses and each location stores an 8-bit word (one byte).

2 Interface

2.1 Description

Signal Name	Width	Type	Description	Drive
rst	1	Input	Reset device	Active low
clk	1	Input	Free running clock	Square wave
w_en	1	Input	Write enable	Active high
din	8	Input	Input for WRITE operation.	Active high
r_en	1	Input	Read enable	Active high
dout	8	Output	Output of READ operation.	Active high
full	1	Output	Raised when FIFO is full.	Active high
empty	1	Output	Raised when FIFO is empty/on reset.	Active high
overflow	1	Output	Raised if write is attempted when full.	Active high
underflow	1	Output	Raised if read is attempted when empty.	Active high

2.2 Verilog

```
module sfifo
  (rst,
    clk,
    w_en,
    din,
    r_en,
    dout,
    full,
    empty,
    overflow,
    underflow
);
```

```
input
                rst;
input
                clk;
input
                w_en;
input
       [7:0]
                din;
input
                r_en;
output [7:0]
                dout;
output
                full;
output
                empty;
output
                overflow;
output
                underflow;
```

endmodule

3 Timing Diagrams

