# CA80C85B

## HIGH PERFORMANCE 8-BIT CMOS MICROPROCESSOR

- **Enhanced, high performance CA80C85B microprocessor features pin and functional compatibility with industry standard 8085 and 8085A**
- **Very low power consumption achieved with proven CMOS implementation**
- **TTL compatible input/output voltages**
- **Fast - Available in 8 MHz, 6 MHz, 5 MHz and 3 MHz speed versions**
- **Full support of extended instruction set, and standard 8080 and 8085/8085A instruction sets**
- **Runs over 10,000 CP/M® programs**
- **On-chip clock generator (using external crystal, LC or RC network)**
- **Direct addressing to 64K bytes**
- **Four Interrupt inputs (one non-maskable)**
- **One of the multi-sourced, Calmos™ 8000 series products**

The CA80C85B is an 8-bit microprocessor having complete pin and functional compatibility with industry standard 8085s and 8085As. In addition, it supports the special 8085 extended instruction set. The CA80C85B includes an on-board system controller, clock generator, serial I/O port and direct addressing capability to 64K bytes of memory. The device also utilizes a multiplexed data bus, with 16-bit addresses split between an 8-bit address bus and an 8-bit data bus.

The CA80C85B is manufactured in CMOS and supplied in a PDIP package configuration suitable for commercial and industrial applications.

The CA80C85B provides the systems designer with single component CPU functionality, thereby reducing the parts count. Its low power consumption and TTL I/O compatibility make the CA80C85B particularly well suited to portable or standby type applications.

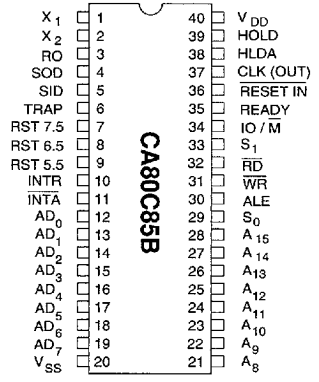



**Figure 2-1: PDIP in Configurations**

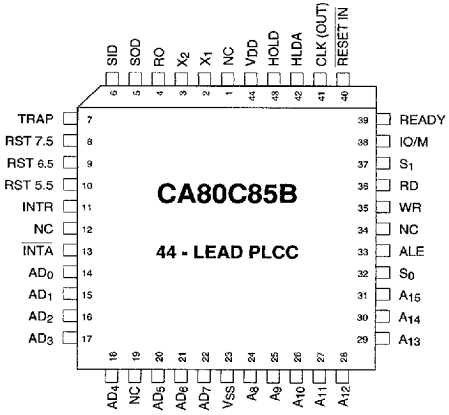



**Figure 2-2: PLCC Pin Configurations**

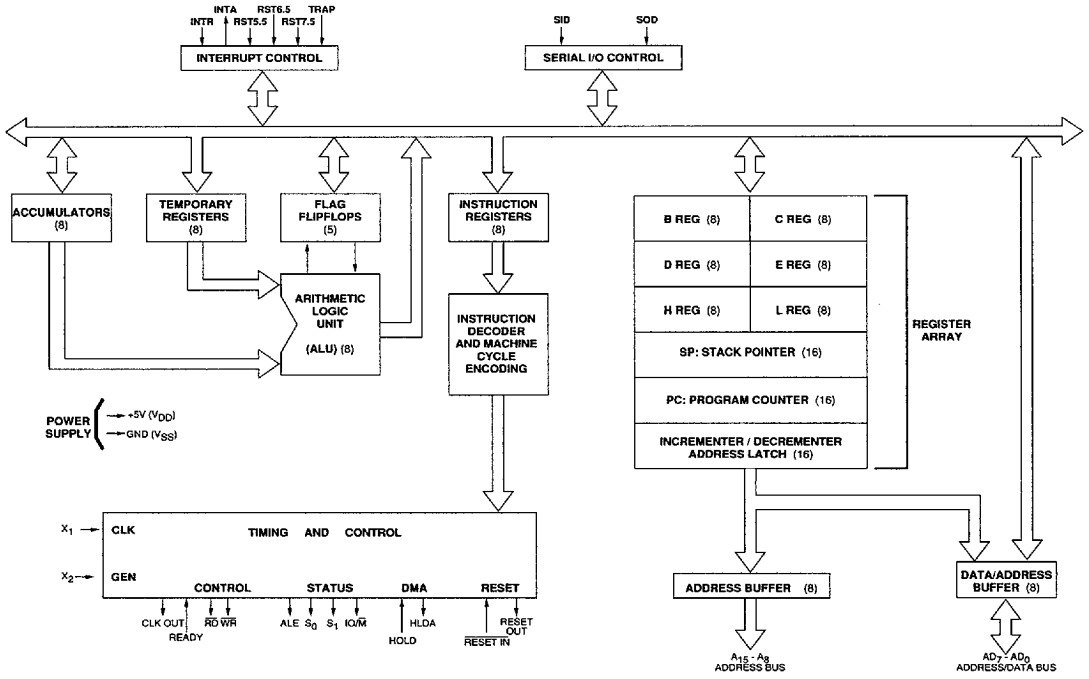



**Figure 2-3: CA80C85B Block Diagram**

## Table 2-1: Pin Descriptions

| Symbol PDIP | Pin | Type | Name and Function |
|---|---|---|---|
| $A_8$ - $A_{15}$ | 21 - 28 | O | **High Address Bus**: the most significant 8 bits of the memory address. |
| $AD_0$ - $AD_7$ | 12 - 19 | I/O | **Low Address and Data Bus**: the least significant 8 bits of the memory address multiplexed with an 8-bit data bus. |
| ALE | 30 | O | **Address Latch Enable Out**: This signal occurs during the first clock state of a machine cycle. The falling edge of the ALE may be used to strobe the status information. |
| CLK | 37 | O | **Clock**: This signal can be used as a system clock. The period of CLK is twice the period of the $X_1$, $X_2$ input. |
| HLDA | 38 | O | **Hold Acknowledge**: Indicates that the CPU has received the HOLD request and that the bus will be relinquished in the next clock cycle. |
| HOLD | 39 | I | **Hold Request**: Is used to indicate that another master is requesting the use of the address and data buses. When HOLD is acknowledged (HLDA), the Address, Data, $\overline{RD}$, $\overline{WR}$ and IO/$\overline{M}$ lines are set to the high impedance state. Note that the CPU can regain control of the bus only after the HOLD is removed. |
| $\overline{INTA}$ | 11 | O | **Interrupt Acknowledge**: This active low signal indicates that the interrupt request input (INTR) has been recognized and acknowledged. |
| INTR | 10 | O | **Interrupt Request**: This is a general purpose interrupt. When INTR goes HIGH, it will inhibit the Program Counter, generate an interrupt acknowledge ($\overline{INTA}$) signal, and sample the data bus for a RESTART or CALL instruction. |
| IO/$\overline{M}$ | 34 | O | **Machine Cycle Status**: See $S_0$ and $S_1$ status bits for further details. |
| $\overline{RD}$ | 32 | O | **Read Control**: Active low signal is used to indicate that selected memory or I/O device is to be read with the data bus available for the data transfer. $\overline{RD}$ is set to a high impedance state during HOLD, HALT and RESET modes. |
| READY | 35 | I | **Ready**: This signal is set to HIGH during read or write cycles to indicate that the selected memory or I/O device is ready to send or receive data. |
| $\overline{RESET\ IN}$ | 36 | I | **Reset In**: Active low signal sets the Program Counter to zero, and resets the interrupt enable (INTE) and HLDA flipflop. Note that so long as $\overline{RESET\ IN}$ is held low, the CPU is held in a reset condition. |
| RO | 3 | O | **Reset Out**: Indicates that the CPU is being reset. This signal can be used as a system RESET. |
| RST7.5<br>RST6.5<br>RST5.5 | 7, 8, 9 | I | **Restart Interrupts**: These inputs provide three maskable interrupts which invoke an automatic internal restart. RST7.5 is the highest relative priority, followed by RST6.5 and RST5.5. All three interrupts have a higher priority than INTR. |
| $S_0$ - $S_1$<br>IO/$\overline{M}$ | 29, 33, 34 | O | **Status Outputs**: These signals provide an indication of the machine status during any given cycle. All become valid at the beginning of a machine cycle, and remain stable for the duration of that cycle. The status may be latched by the falling edge of the ALE signal. |
| SID | 5 | I | **Serial Input Data**: Data on SID is loaded into accumulator bit 7 when a RIM instruction is executed. |
| SOD | 4 | O | **Serial Output Data**: This signal is set or reset by the SIM instruction. |
| TRAP | 6 | I | **Trap Interrupt**: Is a non-maskable restart interrupt. It is the highest priority interrupt, and is unaffected by an interrupt enable (INTE). |
| $V_{DD}$ | 40 | – | **Power**: +5V supply |
| $V_{SS}$ | 20 | – | **Ground**: Ground reference. |
| $\overline{WR}$ | 31 | O | **Write Control**: This active low signal is used to indicate that selected memory or I/O device is to be written to, with the data bus available for the data transfer. WR is set to a high impedance state during HOLD, HALT, and RESET modes. |
| $X_1$, $X_2$ | 1,2 | I | **$X_1$, $X_2$**: These two inputs are connected to clock source which is used to drive the internal clock generator. The clock source may be a crystal, LC or RC network. An external clock cal also be connected directly to $X_1$, to produce an internal processor clock frequency of one half of the input frequency. |

## FUNCTIONAL DESIGN

The CA80C85B utilizes a stack architecture to enable any part of the external memory to be employed as a Last In/First Out (LIFO) memory stack. A 16-bit stack pointer controls the addressing of this stack. The arrangement allows extensive subroutine nesting and multiple level interrupts to be handled without losing the system status. In addition, the device accepts serial input data and provides serial output data, functions which are controlled by the interrupt mask instructions.

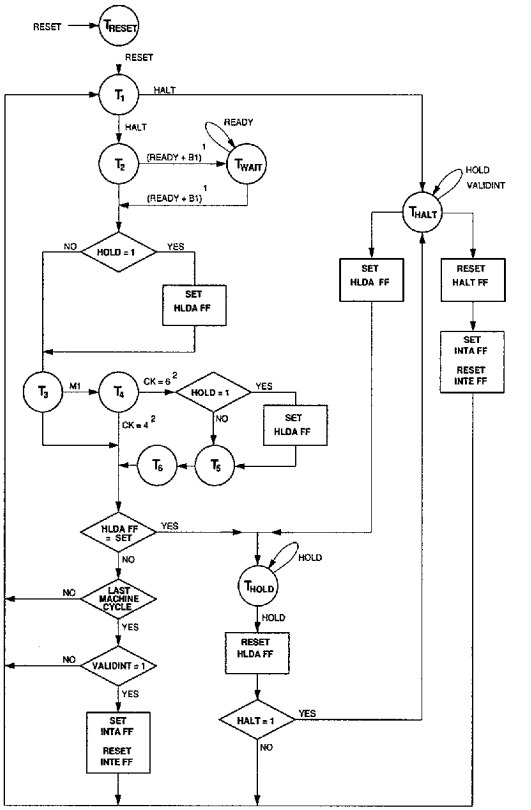
The CA80C85B provides 16-bit arithmetic operation with immediate operators and decimal capability. An 8-bit accumulator, four user accessible flag bits, an 8-bit parallel binary arithmetic unit and six 8-bit data registers, all shown in the block diagram of Figure 2-3, are also provided. CA80C85B timing signals are supplied by an internal clock generator (which can be used with either crystal or RC timing circuits), or by an external clock input signal. Status outputs convey memory I/O instruction and Read/Write timing indications.

For typical, single function type configurations, the CA80C85B is supplied in a 40-pin package, the low pin count a result of multiplexing the Address and Data Bus lines. Pin functions are described in Table 2-1, with the 40-pin DIP pin configuration illustrated in Figure 2-1. The lower processor pin count of this device can be reflected throughout a system design by similar pin count reductions in peripheral chips. Further, this optimization can be achieved without incurring complex or critical timing problems.

The CA80C85B has five levels of interrupts, including three maskable restart interrupts, one non-maskable TRAP interrupt and a bus vectored interrupt, INTR. Bus control is provided by the $\overline{RD}$, $\overline{WR}$, $S_0$, $S_1$, IO/$\overline{M}$ and $\overline{INTA}$ interrupt acknowledge signals. When a HOLD control input signal is received, both Address and Data Bus are set to a high-impedance state, and an HLDA output signal acknowledges that microprocessor operation is stopped, and that the buses are available for use by other devices. Note that HOLD and all other interrupt signals are synchronized with the processor's internal clock. This is illustrated in the processor state transition diagram of Figure 2-4.

In addition to the Data Bus, a simple serial interface is provided by the Serial Input Data (SID) and Serial Output Data (SOD) lines.

At the software level, the CA80C85B supports the full extended instruction set, offering 10 additional instructions for the production of more efficient code. The five existing condition code flags have also been enhanced with two additional flag bits, one of which indicates a 2s complement overflow.




Notes:
1. *BI* indicates that the bus is idle during this machine cycle, though the processor itself is active
2. *CK* indicates the number of clock cycles in this machine cycle.

**Figure 2-4: State Transition Diagram**

## Table 2-2: 3 MHz AC Characteristics

**$T_A$ = –40° to +85°C, $V_{DD}$ = +5v + 10%, $t_{CYC}$ = 320 ns, $C_L$ = 150 pF**

| Symbol | Parameter | Limits | | Units |
|---|---|---|---|---|
| | | Min | Max | |
| $t_1$ | CLK Low Time | 80 | - | ns |
| $t_2$ | CLK High Time | 120 | - | ns |
| $t_{AC}$ | $A_8$ - $A_{15}$ Valid to Leading Edge of Control (Note 1) | 270 | - | ns |
| $t_{ACL}$ | $A_0$ - $A_7$ Valid to Leading Edge of Control | 240 | - | ns |
| $t_{AD}$ | A0 - A15 Valid to Valid Data In | - | 575 | ns |
| $t_{AFR}$ | Address Float After Leading Edge of $\overline{RD}$, $\overline{INTA}$ | - | 0 | ns |
| $t_{AL}$ | $A_8$ - $A_{15}$ Valid Before Trailing Edge of ALE (Note 1) | 115 | - | ns |
| $t_{ALL}$ | $A_0$ - $A_7$ Valid Before Trailing Edge of ALE | 90 | - | ns |
| $t_{ARY}$ | READY Valid from Address Valid | - | 220 | ns |
| $t_{CA}$ | Address ($A_8$ - $A_{15}$) Valid After Control | 120 | - | ns |
| $t_{CC}$ | Width of Control Low ($\overline{RD}$, $\overline{WR}$, $\overline{INTA}$) | 400 | - | ns |
| $t_{CL}$ | Trailing Edge of Control to Leading Edge of ALE | 50 | - | ns |
| $t_{CYC}$ | CLK Cycle Period | 320 | 2000 | ns |
| $t_{DW}$ | Data Valid to Trailing Edge of $\overline{WR}$ | 420 | - | ns |
| $t_f$ | CLK Fall Time | - | 30 | ns |
| $t_{HABE}$ | HLDA to Bus Enable | - | 210 | ns |
| $t_{HABF}$ | Bus Float After HLDA | - | 210 | ns |
| $t_{HACK}$ | HLDA Valid to Trailing Edge of CLK | 110 | - | ns |
| $t_{HDH}$ | HOLD Hold Time | 0 | - | ns |
| $t_{HDS}$ | HOLD Setup Time to Trailing Edge of CLK | 170 | - | ns |
| $t_{INH}$ | INTR Hold Time | 0 | - | ns |
| $t_{INS}$ | INTR RST and TRAP Setup Time to Falling Edge of CLK | 160 | - | ns |
| $t_{LA}$ | Address Hold Time After ALE | 100 | - | ns |
| $t_{LC}$ | Trailing Edge of ALE to Leading Edge of Control | 130 | - | ns |
| $t_{LCK}$ | ALE Low During CLK High | 100 | - | ns |
| $t_{LDR}$ | ALE to Valid Data During Read | - | 460 | ns |
| $t_{LDW}$ | ALE to Valid Data During Write | - | 200 | ns |
| $t_{LL}$ | ALE Width | 140 | - | ns |
| $t_{LRY}$ | ALE to Ready Stable | - | 110 | ns |
| $t_r$ | CLK Rise Time | - | 30 | ns |
| $t_{RAE}$ | Trailing Edge of RD to re-Enabling of Address | 150 | - | ns |
| $t_{RD}$ | $\overline{RD}$ (or $\overline{INTA}$) to Valid Data | - | 300 | ns |
| $t_{RDH}$ | Data Hold Time After $\overline{RD}$, $\overline{INTA}$ | 0 | - | ns |
| $t_{RV}$ | Control Trailing Edge to Leading Edge of Next Control | 400 | - | ns |
| $t_{RYH}$ | READY Hold Time | 0 | - | ns |
| $t_{RYS}$ | READY Setup Time to Leading Edge of CLK | 110 | - | ns |
| $t_{WD}$ | Data Valid After Trailing Edge of $\overline{WR}$ | 100 | - | ns |
| $t_{WDL}$ | Leading Edge of $\overline{WR}$ to Data Valid | - | 40 | ns |
| $t_{XKF}$ | $X_1$ Rising to CLK Falling | 20 | 150 | ns |
| $t_{XKR}$ | $X_1$ Rising to CLK Rising | 20 | 120 | ns |

Note: 1. $A_8$ - $A_{15}$ Address Specs apply to IO/$\overline{M}$, S0 and S1. Except $A_8$ - $A_{15}$ are undefined during $T_4$ - $T_6$ of cycle whereas IO/$\overline{M}$, $S_0$ and $S_1$ are stable.

**Table 2-3: 5 MHz AC Characteristics**

**$T_A$ = –40° to +85°C, $V_{DD}$ = +5v + 10%, $t_{CYC}$ = 200 ns, $C_L$ = 150 pF**

| Symbol | Parameter | Limits | | Units |
|---|---|---|---|---|
| | | Min | Max | |
| $t_1$ | CLK Low Time | 40 | - | ns |
| $t_2$ | CLK High Time | 70 | - | ns |
| $t_{AC}$ | $A_8$ - $A_{15}$ Valid to Leading Edge of Control (Note 1) | 115 | - | ns |
| $t_{ACL}$ | $A_0$ - $A_7$ Valid to Leading Edge of Control | 115 | - | ns |
| $t_{AD}$ | $A_0$ - $A_{15}$ Valid to Valid Data In | - | 330 | ns |
| $t_{AFR}$ | Address Float After Leading Edge of $\overline{RD}$, $\overline{INTA}$ | - | 0 | ns |
| $t_{AL}$ | $A_8$ - $A_{15}$ Valid Before Trailing Edge of ALE (Note 1) | 50 | - | ns |
| $t_{ALL}$ | $A_0$ - $A_7$ Valid Before Trailing Edge of ALE | 50 | - | ns |
| $t_{ARY}$ | READY Valid from Address Valid | - | 100 | ns |
| $t_{CA}$ | Address ($A_8$ - $A_{15}$) Valid After Control | 60 | - | ns |
| $t_{CC}$ | Width of Control Low ($\overline{RD}$, $\overline{WR}$, $\overline{INTA}$) | 230 | - | ns |
| $t_{CL}$ | Trailing Edge of Control to Leading Edge of ALE | 25 | - | ns |
| $t_{CYC}$ | CLK Cycle Period | 200 | 2000 | ns |
| $t_{DW}$ | Data Valid to Trailing Edge of $\overline{WR}$ | 230 | - | ns |
| $t_f$ | CLK Fall Time | - | 30 | ns |
| $t_{HABE}$ | HLDA to Bus Enable | - | 150 | ns |
| $t_{HABF}$ | Bus Float After HLDA | - | 150 | ns |
| $t_{HACK}$ | HLDA Valid to Trailing Edge of CLK | 40 | - | ns |
| $t_{HDH}$ | HOLD Hold Time | 0 | - | ns |
| $t_{HDS}$ | HOLD Setup Time to Trailing Edge of CLK | 120 | - | ns |
| $t_{INH}$ | INTR Hold Time | 0 | - | ns |
| $t_{INS}$ | INTR RST and TRAP Setup Time to Falling Edge of CLK | 150 | - | ns |
| $t_{LA}$ | Address Hold Time After ALE | 50 | - | ns |
| $t_{LC}$ | Trailing Edge of ALE to Leading Edge of Control | 60 | - | ns |
| $t_{LCK}$ | ALE Low During CLK High | 50 | - | ns |
| $t_{LDR}$ | ALE to Valid Data During Read | - | 250 | ns |
| $t_{LDW}$ | ALE to Valid Data During Write | - | 140 | ns |
| $t_{LL}$ | ALE Width | 80 | - | ns |
| $t_{LRY}$ | ALE to Ready Stable | - | 30 | ns |
| $t_r$ | CLK Rise Time | - | 30 | ns |
| $t_{RAE}$ | Trailing Edge of RD to re-Enabling of Address | 85 | - | ns |
| $t_{RD}$ | $\overline{RD}$ (or $\overline{INTA}$) to Valid Data | - | 150 | ns |
| $t_{RDH}$ | Data Hold Time After $\overline{RD}$, $\overline{INTA}$ | 0 | - | ns |
| $t_{RV}$ | Control Trailing Edge to Leading Edge of Next Control | 220 | - | ns |
| $t_{RYH}$ | READY Hold Time | 0 | - | ns |
| $t_{RYS}$ | READY Setup Time to Leading Edge of CLK | 100 | - | ns |
| $t_{WD}$ | Data Valid After Trailing Edge of $\overline{WR}$ | 60 | - | ns |
| $t_{WDL}$ | Leading Edge of $\overline{WR}$ to Data Valid | - | 20 | ns |
| $t_{XKF}$ | $X_1$ Rising to CLK Falling | 20 | 110 | ns |
| $t_{XKR}$ | $X_1$ Rising to CLK Rising | 20 | 100 | ns |

Note: 1. $A_8$ - $A_{15}$ Address Specs apply to IO/$\overline{M}$, S0 and S1. Except $A_8$ - $A_{15}$ are undefined during $T_4$ - $T_6$ of cycle whereas IO/$\overline{M}$, $S_0$ and $S_1$ are stable.

## Table 2-4: 6 MHz AC Characteristics

**$T_A$ = –40° to +85°C, $V_{DD}$ = +5v + 5%, $t_{CYC}$ = 167 ns, $C_L$ = 150 pF**

| Symbol | Parameter | Limits | | Units |
|---|---|---|---|---|
| | | Min | Max | |
| $t_1$ | CLK Low Time | 34 | - | ns |
| $t_2$ | CLK High Time | 59 | - | ns |
| $t_{AC}$ | $A_8$ - $A_{15}$ Valid to Leading Edge of Control (Note 1) | 96 | - | ns |
| $t_{ACL}$ | $A_0$ - $A_7$ Valid to Leading Edge of Control | 96 | - | ns |
| $t_{AD}$ | $A_0$ - $A_{15}$ Valid to Valid Data In | - | 292 | ns |
| $t_{AFR}$ | Address Float After Leading Edge of $\overline{RD}$, $\overline{INTA}$ | - | 0 | ns |
| $t_{AL}$ | $A_8$ - $A_{15}$ Valid Before Trailing Edge of ALE (Note 1) | 42 | - | ns |
| $t_{ALL}$ | $A_0$ - $A_7$ Valid Before Trailing Edge of ALE | 42 | - | ns |
| $t_{ARY}$ | READY Valid from Address Valid | - | 83 | ns |
| $t_{CA}$ | Address ($A_8$ - $A_{15}$) Valid After Control | 50 | - | ns |
| $t_{CC}$ | Width of Control Low ($\overline{RD}$, $\overline{WR}$, $\overline{INTA}$) | 192 | - | ns |
| $t_{CL}$ | Trailing Edge of Control to Leading Edge of ALE | 20 | - | ns |
| $t_{CYC}$ | CLK Cycle Period | 167 | 2000 | ns |
| $t_{DW}$ | Data Valid to Trailing Edge of $\overline{WR}$ | 192 | - | ns |
| $t_f$ | CLK Fall Time | - | 25 | ns |
| $t_{HABE}$ | HLDA to Bus Enable | - | 125 | ns |
| $t_{HABF}$ | Bus Float After HLDA | - | 125 | ns |
| $t_{HACK}$ | HLDA Valid to Trailing Edge of CLK | 33 | - | ns |
| $t_{HDH}$ | HOLD Hold Time | 0 | - | ns |
| $t_{HDS}$ | HOLD Setup Time to Trailing Edge of CLK | 100 | - | ns |
| $t_{INH}$ | INTR Hold Time | 0 | - | ns |
| $t_{INS}$ | INTR RST and TRAP Setup Time to Falling Edge of CLK | 125 | - | ns |
| $t_{LA}$ | Address Hold Time After ALE | 42 | - | ns |
| $t_{LC}$ | Trailing Edge of ALE to Leading Edge of Control | 50 | - | ns |
| $t_{LCK}$ | ALE Low During CLK High | 42 | - | ns |
| $t_{LDR}$ | ALE to Valid Data During Read | - | 225 | ns |
| $t_{LDW}$ | ALE to Valid Data During Write | - | 100 | ns |
| $t_{LL}$ | ALE Width | 67 | - | ns |
| $t_{LRY}$ | ALE to Ready Stable | - | 25 | ns |
| $t_r$ | CLK Rise Time | - | 25 | ns |
| $t_{RAE}$ | Trailing Edge of RD to Re-enabling of Address | 65 | - | ns |
| $t_{RD}$ | $\overline{RD}$ (or $\overline{INTA}$) to Valid Data | - | 125 | ns |
| $t_{RDH}$ | Data Hold Time After $\overline{RD}$, $\overline{INTA}$ | 0 | - | ns |
| $t_{RV}$ | Control Trailing Edge to Leading Edge of Next Control | 183 | - | ns |
| $t_{RYH}$ | READY Hold Time | 0 | - | ns |
| $t_{RYS}$ | READY Setup Time to Leading Edge of CLK | 84 | - | ns |
| $t_{WD}$ | Data Valid After Trailing Edge of $\overline{WR}$ | 50 | - | ns |
| $t_{WDL}$ | Leading Edge of $\overline{WR}$ to Data Valid | - | 16 | ns |
| $t_{XKF}$ | $X_1$ Rising to CLK Falling | 20 | 110 | ns |
| $t_{XKR}$ | $X_1$ Rising to CLK Rising | 20 | 100 | ns |

Note: 1. $A_8$ - $A_{15}$ Address Specs apply to IO/$\overline{M}$, S0 and S1. Except $A_8$ - $A_{15}$ are undefined during $T_4$ - $T_6$ of cycle whereas IO/$\overline{M}$, $S_0$ and $S_1$ are stable.

**Table 2-5: 8 MHz AC Characteristics**

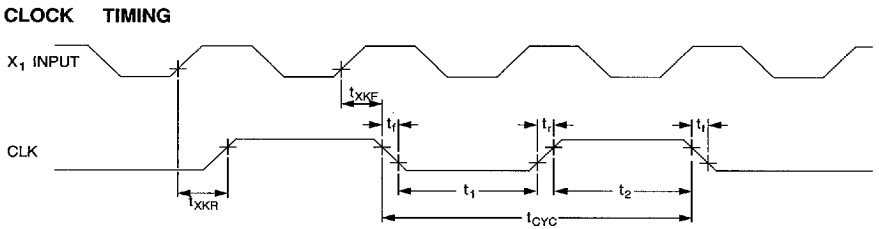
**$T_A$ = –40° to +85°C, $V_{DD}$ = +5v + 5%, $t_{CYC}$ = 125 ns, $C_L$ = 150 pF**

| Symbol | Parameter | Limits | | Units |
|---|---|---|---|---|
| | | Min | Max | |
| $t_1$ | CLK Low Time | 25 | - | ns |
| $t_2$ | CLK High Time | 44 | - | ns |
| $t_{AC}$ | $A_8$ - $A_{15}$ Valid to Leading Edge of Control (Note 1) | 72 | - | ns |
| $t_{ACL}$ | $A_0$ - $A_7$ Valid to Leading Edge of Control | 72 | - | ns |
| $t_{AD}$ | $A_0$ - $A_{15}$ Valid to Valid Data In | - | 220 | ns |
| $t_{AFR}$ | Address Float After Leading Edge of $\overline{RD}$, $\overline{INTA}$ | - | 0 | ns |
| $t_{AL}$ | $A_8$ - $A_{15}$ Valid Before Trailing Edge of ALE (Note 1) | 31 | - | ns |
| $t_{ALL}$ | $A_0$ - $A_7$ Valid Before Trailing Edge of ALE | 31 | - | ns |
| $t_{ARY}$ | READY Valid from Address Valid | - | 63 | ns |
| $t_{CA}$ | Address ($A_8$ - $A_{15}$) Valid After Control | 37 | - | ns |
| $t_{CC}$ | Width of Control Low ($\overline{RD}$, $\overline{WR}$, $\overline{INTA}$) | 144 | - | ns |
| $t_{CL}$ | Trailing Edge of Control to Leading Edge of ALE | 15 | - | ns |
| $t_{CYC}$ | CLK Cycle Period | 125 | 2000 | ns |
| $t_{DW}$ | Data Valid to Trailing Edge of $\overline{WR}$ | 144 | - | ns |
| $t_f$ | CLK Fall Time | - | 25 | ns |
| $t_{HABE}$ | HLDA to Bus Enable | - | 94 | ns |
| $t_{HABF}$ | Bus Float After HLDA | - | 94 | ns |
| $t_{HACK}$ | HLDA Valid to Trailing Edge of CLK | 25 | - | ns |
| $t_{HDH}$ | HOLD Hold Time | 0 | - | ns |
| $t_{HDS}$ | HOLD Setup Time to Trailing Edge of CLK | 78 | - | ns |
| $t_{INH}$ | INTR Hold Time | 0 | - | ns |
| $t_{INS}$ | INTR RST and TRAP Setup Time to Falling Edge of CLK | 94 | - | ns |
| $t_{LA}$ | Address Hold Time After ALE | 32 | - | ns |
| $t_{LC}$ | Trailing Edge of ALE to Leading Edge of Control | 38 | - | ns |
| $t_{LCK}$ | ALE Low During CLK High | 32 | - | ns |
| $t_{LDR}$ | ALE to Valid Data During Read | - | 168 | ns |
| $t_{LDW}$ | ALE to Valid Data During Write | - | 75 | ns |
| $t_{LL}$ | ALE Width | 50 | - | ns |
| $t_{LRY}$ | ALE to Ready Stable | - | 25 | ns |
| $t_r$ | CLK Rise Time | - | 25 | ns |
| $t_{RAE}$ | Trailing Edge of $\overline{RD}$ to Re-enabling of Address | 45 | - | ns |
| $t_{RD}$ | $\overline{RD}$ (or $\overline{INTA}$) to Valid Data | - | 94 | ns |
| $t_{RDH}$ | Data Hold Time After $\overline{RD}$, $\overline{INTA}$ | 0 | - | ns |
| $t_{RV}$ | Control Trailing Edge to Leading Edge of Next Control | 138 | - | ns |
| $t_{RYH}$ | READY Hold Time | 0 | - | ns |
| $t_{RYS}$ | READY Setup Time to Leading Edge of CLK | 63 | - | ns |
| $t_{WD}$ | Data Valid After Trailing Edge of $\overline{WR}$ | 34 | - | ns |
| $t_{WDL}$ | Leading Edge of $\overline{WR}$ to Data Valid | - | 16 | ns |
| $t_{XKF}$ | $X_1$ Rising to CLK Falling | 20 | 69 | ns |
| $t_{XKR}$ | $X_1$ Rising to CLK Rising | 20 | 63 | ns |

Note: 1. $A_8$ - $A_{15}$ Address Specs apply to IO/$\overline{M}$, S0 and S1. Except $A_8$ - $A_{15}$ are undefined during $T_4$ - $T_6$ of cycle whereas IO/$\overline{M}$, $S_0$ and $S_1$ are stable.

**Figure 2-5: Timing Diagrams**

**a) Clock Timing**




**b) Read Operation**

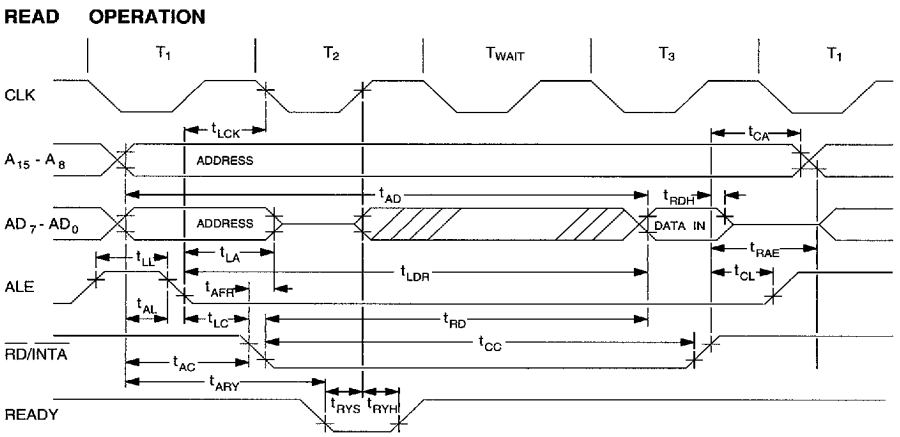
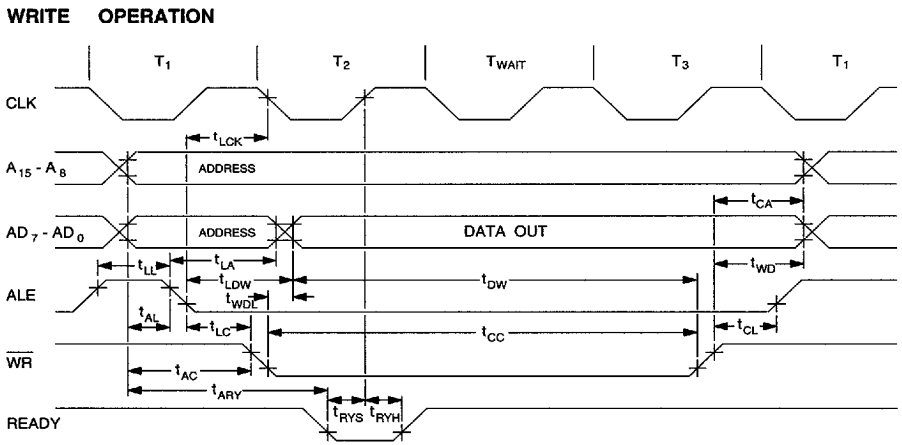


**Figure 4: Timing Diagrams con't**

**c) Write Operation**




**d) Hold Operation**

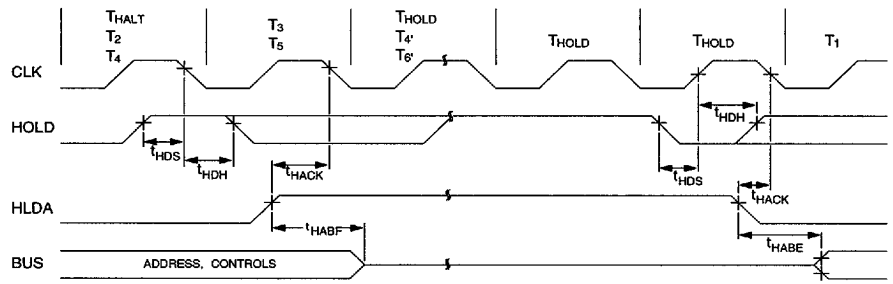
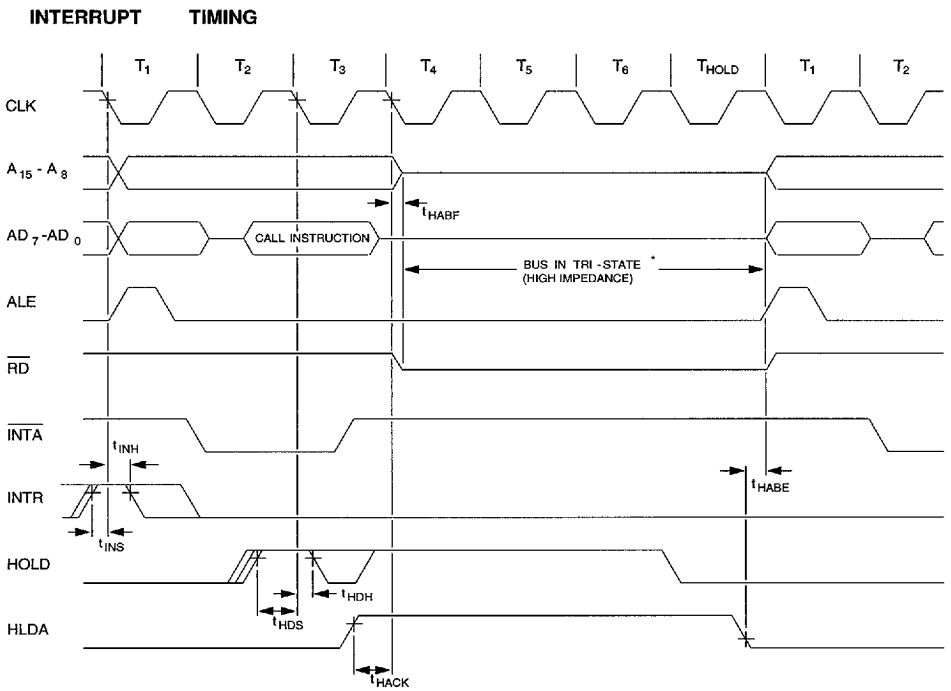


**Figure 4: Timing Diagrams con't**

**e) Interrupt Timing**




*NOTE: IO/M is also floating in a high-impedance state during this time

**Table 2-6: DC Characteristics (Commercial and Industrial Temperature Range Devices)**

**$T_A$ = –40° to +85°C, $V_{DD}$ = +5v + 10%, $t_{CYC}$ = 320 ns (except as noted)**

| Symbol | Parameter | Test Condition | Limits | | Units |
|---|---|---|---|---|---|
| | | | Min | Max | |
| $I_{DD1}$ | Power Supply Current | $t_{CYC}$ = 320 ns, $T_A$ = –40 °C | | 24 | mA |
| | | $t_{CYC}$ = 320 ns, $T_A$ = +25 °C | | 17 | mA |
| $I_{DD2}$ | Power Supply Current | $t_{CYC}$ = 200 ns, $T_A$ = –40 °C | | 29 | mA |
| | | $t_{CYC}$ = 200 ns, $T_A$ = +25 °C | | 21 | mA |
| $I_{IL}$ | Input Leakage Current | $V_{IN} = V_{DD}$ and $V_{IN} = 0$ | -10 | 10 | µA |
| $I_{OL}$ | Output Leakage Current | $0v \le V_{OUT} \le V_{DD}$ | -10 | 10 | µA |
| $V_{HY}$ | Hysteresis, RESET | | 0.25 | | V |
| $V_{IH}$ | Input High Voltage | | 2.2 | $V_{DD}$+0.3 | V |
| $V_{IHR}$ | Input High Level, RESET | | 2.4 | $V_{DD}$+0.3 | V |
| $V_{IL}$ | Input Low Voltage | | –0.3 | +0.8 | V |
| $V_{ILR}$ | Input Low Level, RESET | | –0.3 | +0.8 | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 2 mA | | 0.45 | V |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = –400 µA | 2.4 | | V |
| | | $I_{OH}$ = –40 µA | 4.2 | | V |

**Table 2-7: Absolute Maximum Ratings**

| | |
|---|---|
| Storage Temperature | –65°C to +160°C |
| Voltage On Any Pin with respect to Ground | –0.3 to VDD +0.3 Volts |
| Output Currents | 100mA |
| Power Dissipation | 1 Watt |
| Lead Temperature (Soldering: 10 seconds) | 300°C |

Note: Stresses beyond those listed above may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## Clock Inputs

Clock inputs to the CA80C85B are supplied via the two inputs $X_1$ and $X_2$. The $X_1$ input can be driven either from an external clock, or used with the $X_2$ input and a crystal to produce an oscillator function. The minimum input

frequency required in both cases is 1 MHz. The actual internal microprocessor clock frequency is one half of the frequency applied or generated externally. For example, a 6 MHz crystal or external clock waveform is required for 3 MHz operation, and a 12 MHz clock source is required for 6 MHz operation.

The $X_1/X_2$ circuitry is intended to be used with a crystal cut for parallel resonance at the required clock frequency. Such crystals require closely controlled load capacitance in order to resonate at the specified frequency. The CA80C85B has an equivalent parallel capacitance of between 10 and 20 pF. Since most crystals will require higher values of capacitance to resonate at precisely their specified frequency, additional capacitance must be added as shown in Figure 2-6(a).

When the $X_1$ input is driven from an external clock, $X_2$ is left open. In this case, $X_1$ should be driven with a CMOS driver or a TTL device with a pull-up resistor, as shown in Figure 2-6(b). The clock low time must be greater than 80 ns for the 3 MHz device and 30 ns for the 6 MHz.

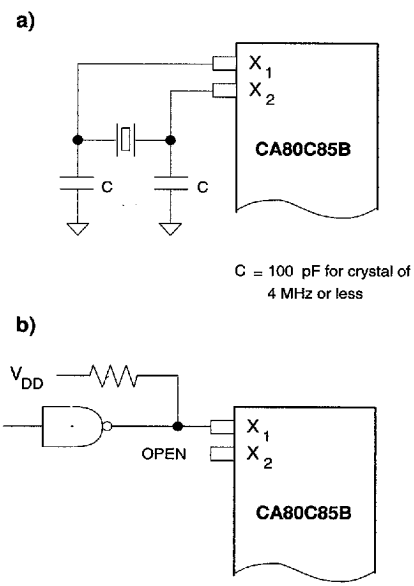



**Figure 2-6: External Clock Circuits**

### Serial I/O

The Set Interrupt Mask (SIM) and Read Interrupt Mask (RIM) instructions provide several functions related to serial port I/O and interrupt mask operations. The SIM instruction is used to output serial data, and to program the interrupt mask register. The output signal, SOD, is set or reset as specified by the SIM instruction, with the accumulator contents constructed as shown in Figure 2-7.

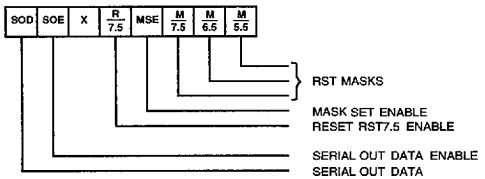



**Figure 2-7: SIM Instruction Data Byte**

The RIM instruction is used to read the serial input data (SID), as well as the interrupt mask. The accumulator contents after a RIM instruction has been executed are as shown in Figure 2-8.

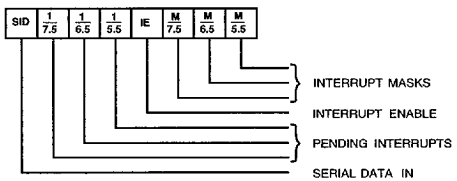



**Figure 2-8: RIM Instruction Data Byte**

### Interrupts

The five interrupt levels provided by the CA80C85B are listed by descending order of priority in Table 2-8. TRAP and RSTx.5 are RESTART interrupts. When acknowledged, these four interrupts cause the processor to save the program counter (PC) on the stack, then branch to the restart address specified in the table.

The TRAP interrupt is non-maskable. It is set with a rising edge (low to high) followed by a stable high level until sampled by the processor. To reactivate the TRAP interrupt, the input signal must first go low, then high.

To preserve the status of the Interrupt Enable (IE) flag after a TRAP interrupt has occurred, the interrupt mask must be read and saved immediately after the interrupt has been acknowledged (refer to RIM instruction).

The RST7.5 is a maskable interrupt, set on a rising edge only, and then latched.

The RST6.5 and RST5.5 are maskable interrupts, set with a high level applied to their respective inputs. The status of the three RST interrupt masks can only be affected by the SIM instruction and $\overline{\text{RESET IN}}$.

The INTR interrupt is also set by a high level applied to the input pin. It is similar in operation to the 8080 INT interrupt in that the action of the processor is dependent on the instruction placed on the bus during the $\overline{\text{INTA}}$.

Note that the servicing of any of the five interrupts disables all future interrupts (except TRAPS) until an EI instruction is executed. Of course, an interrupt of higher priority may interrupt a previous interrupt in process if the interrupts have been re-enabled within the interrupt service routine.

**Table 2-8: Interrupt Restart Address**

| Interrupt | Restart Address (HEX) |
|---|---|
| TRAP | 24H |
| RST7.5 | 3CH |
| RST6.5 | 34H |
| RST5.5 | 2CH |
| INTR | Dependent upon the instruction received on the bus during an INTA |

### Status Outputs

The status of the CA80C85B can be determined from the combination of $S_0$, $S_1$ and IO/$\overline{M}$ output signals. These signals are latched on the falling edge of an ALE signal, and are valid while ALE is low. Table 2-9 lists the seven possible types of machine cycles as defined by $S_0$, $S_1$ and IO/$\overline{M}$. Note in the Figure 2-5 timing diagrams that the $\overline{RD}$ and $\overline{WR}$ control lines become active after the status signals, when the transfer of data is to take place.

**Table 2-9: Machine Cycle Status Conditions**

| $S_0$ | $S_1$ | IO/M | Status |
|---|---|---|---|
| 1 | 0 | 0 | Memory Write |
| 0 | 1 | 0 | Memory Read |
| 1 | 0 | 1 | I/O Write |
| 0 | 1 | 1 | I/O Read |
| 1 | 1 | 0 | Opcode Fetch |
| 1 | 1 | 1 | Interrupt Acknowledge |
| Z | 0 | 0 | Halt |
| Z | X | X | Hold |
| Z | X | X | Reset |

Z - High impedance state
X - Don't care condition

### Extended Instructions and Condition Codes

The CA80C85B Flag Register features two additional condition code flags, for a total of seven. These are illustrated in Figure 2-9. The ten opcodes which comprise the extended instruction set of the CA80C85B microprocessor are described in Table 2-10.

| S | Z | V | AC | 0 | P | UI | C | FLAG |
|---|---|---|---|---|---|---|---|---|
| 7 | 6 | | 4 | 3 | 2 | | 0 | BIT |

V - 2's complement overflow for both 8 and 16-bit arithmetic operations

UI - Underflow indicator (DCX instruction)
or
Overflow indicator (INX instruction)

UI = 01 x 02 + 01 x R + 02 x R

where:
01 = sign of operand 1
02 = sign of operand 2
R = sign of result

For subtraction and comparisons, replace 02 with 02

**Figure 2-9: Extended Condition Codes**

**Table 2-10: CA80C85B Extended Instruction Set**

| Name | Opcodes | Flags | Cycles | States | Description |
|---|---|---|---|---|---|
| ARHL | 00010000<br>Addressing:<br>Register | CY | 2 | 7 | **Arithmetic Shift of H and L to the Right:**<br>The contents of registers H and L are shifted right one bit is shifted into the carry bit. The result is saved in registers H and L.<br>H7=H7; Hn-1=Hn; L7=H0; Ln-1=Ln; CY=L0 |
| DSUB | 00001000<br>Addressing:<br>Register | Z, S, P, CY, | 3 | 10 | **Double Subtraction:**<br>The contents of registers B and Care subtracted from the contents of registers H and L. The result is saved in registers H and L.<br>(H) (L)=(H) (L) - (B) (C) |
| JNUI | 11011101<br>low-order address<br>high-order address<br>Addressing:<br>Immediate | none | 2 or 3 | 7 or 10 | **Jump on NOT UI Flag:**<br>Control is transferred to the instruction address specified in bytes 2 and 3 of the current instruction. The result is saved in registers H and L.<br>(H) (L)=(H) (L) - (B) (C) |
| JUI | 11111101<br>low-order address<br>high-order address<br>Addressing:<br>Immediate | none | 2 or 3 | 7 or 10 | **Jump on UI Flag:**<br>Control is transferred to the instruction address specified in bytes 2 and 3 of the current instruction. if the Unsigned Indicator Flag (UI) is set. Otherwise control continues sequentially.<br>(H) (L)=(H) (L) - (B) (C) |
| LDHI | 00101000<br>data<br>Addressing:<br>Immediate Register | none | 3 | 10 | **Load D and E with L Plus Immediate Byte:**<br>The immediate byte is added to the contents of registers H and L, and the result is saved in registers D and E.<br>(D) (E) = (H) (L) + (byte 2) |
| LDSI | 00111000<br>data<br>Addressing:<br>Immediate Register | none | 3 | 10 | **Load D and E with SP Plus Immediate Byte:**<br>The 2 bytes of register SP are added to the immediate byte, and the result is saved in registers D and E.<br>(D) (E) = (SPH) (SPL) + (byte 2) |
| LHLX | 11101101<br>data<br>Addressing:<br>Register Indirect | none | 3 | 10 | **Load H and L Indirect Through D and E:**<br>The contents of the memory location given by registers D and E are moved to register L. The contents of the next location are moved to register H<br>L=((D) (E)); H=((D)(E) + 1) |
| RDEL | 00011000<br>Addressing:<br>Register | CY, V | 3 | 10 | **Rotate D and E Left Through Carry:**<br>The contents of the registers D and E are rotated one bit left through the carry flag. The low-order bit is set equal to the CY flag and the CY flag is set to the value shifted out of the high-order bit<br>Dn+1=Dn; D0; E7; CY=D7; En+1=En; E0=CY |
| RSTV | 11001011<br>Addressing:<br>Register Indirect | none | 1 or 3 | 6 or 12 | **Restart on Overflow:**<br>If overflow flag V is set, then the actions below are performed. Otherwise, control continues sequentially.<br>If (V): SP - 1=PCH; SP - 2=PCL; SP=SP - 2; PC=40HEX |
| SHLX | 11011001<br>Addressing: | none | 3 | 10 | **Store H and L Indirect Through D and E:**<br>The contents of register L are moved to the memory location given by registers D and E. The contents of register H are |