

# Cache Revive: Exploiting Volatility of STT-RAM Caches for Enhanced Performance in CMPs.

Anonymous MICRO submission

Paper ID 761

## Abstract

*Spin-Transfer Torque RAM (STT-RAM) is a CMOS compatible emerging non-volatile memory (NVM) technology that has the potential to replace the conventional on-chip SRAM caches for designing a more efficient memory hierarchy for future multicore architectures. However, its high write latency and dynamic write energy are major obstacles for being competitive with the SRAM-based cache hierarchy. On the other hand, STT-RAM technology has another adaptable feature that it is possible to reduce its write latency by reducing its retention time, thereby making it volatile. In this paper, we exploit this volatile property of the STT-RAM for designing an efficient L2 cache architecture. The paper addresses several critical design issues such as how do we decide a suitable retention time for last level cache, what is the relationship between retention time and write latency, and how do we architect the cache hierarchy with a volatile STT-RAM. Through an extensive execution driven analysis of the inter-write time revivetime of several PARSEC and SPEC 2006 benchmarks, we observe that retention time in the order of 10s of ms is a good design point to handle most of the writes. Then for the rest of the cache blocks that have a higher revive time than the STT-RAM retention time, we propose an architectural solution to identify these blocks with a per block 2 bit counter, temporarily save a limited number of MRU blocks in a buffer, and writeback the rest of the dirty blocks to avoid any data loss. Our experiments with 4*

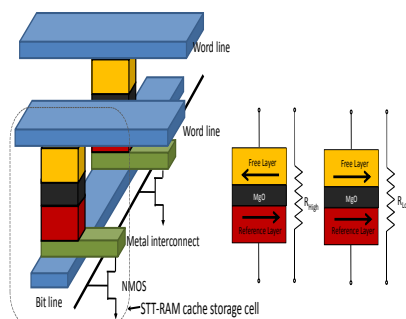


Figure 1. Caption.

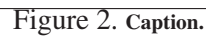
and 8-core architectures with an SRAM-based L1 cache and STT-RAM-based L2 cache indicate that not only we can eliminate the high write overhead of an NVM STT-RAM, but can provide on an average 10-12% improvement in IPC compared to the traditional SRAM-based design, while reducing the energy consumption significantly.

## 1. Introduction

## 2. Motivation

The ABSTRACT is to be in fully-justified italicized text. Use the word “Abstract” as the title, in 14-point Times, boldface type, centered relative to the column, initially capitalized. The abstract is to be in 12-point, single-spaced type. Leave two blank lines after the Abstract, then begin the main text. Look at previous MICRO abstracts to get a feel for style and length. referring Fig 1 here.

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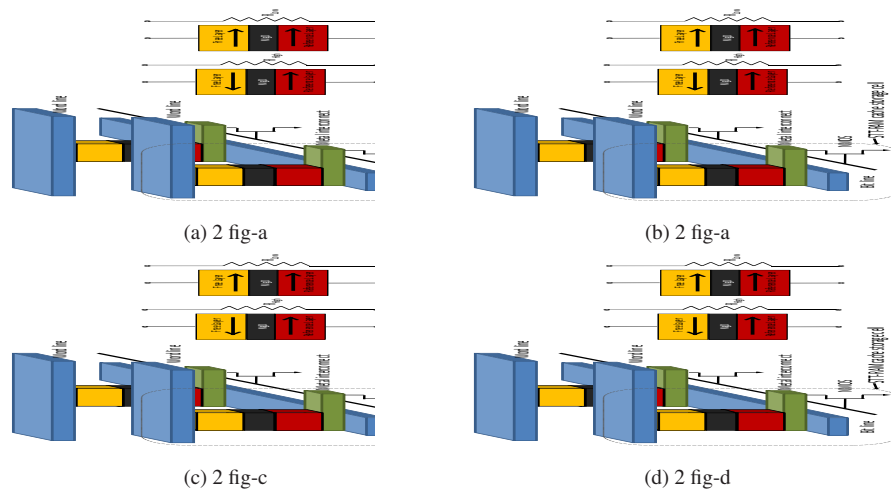


Figure 3. Caption.

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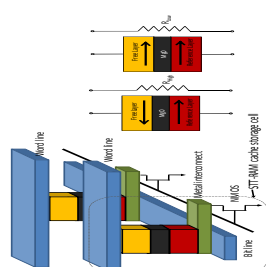


Figure 4. Caption.

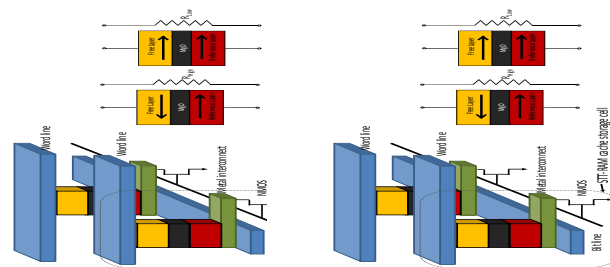


Figure 5. Caption.

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### 3. STT-RAM Design

### 4. Architecting Volatile STT-RAM

### 5. Experimental Evaluation

### 6. Results

### 7. Prior Work

### 8. Conclusions

Sample bibliography [1]”.

### References

[1] Authors. Frobnication tutorial, 2011. Supplied as additional material `tr.pdf`. 8