

# ECE 532 FINAL PROJECT: VOLTAGE REGULATOR

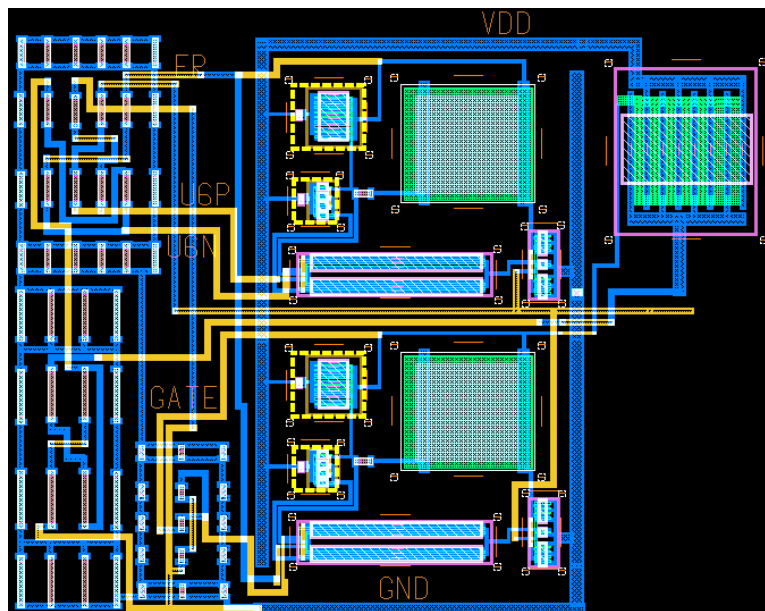
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## 1. INTRODUCTION

In this report I will detail the design of a linear regulator that takes a 5 volt input and outputs 1.0 - 4.0 volts on the output. I can control it by tuning the feedback amplifiers. I fine tune the final amplifier that will be fabricated to output 2.5V. I learned a lot in this project, from how to design a negative feedback controller to the design tradeoffs involved in analog circuits. Almost every decision I made had a pro and a con (such as more current vs. using more area). The layout showed me how important it is to plan ahead and think of a project modularly.

This report is divided into the following sections:

- (1) Design Goals
- (2) Design Challenges
- (3) Schematics
- (4) Simulations
- (5) Layout



## 2. DESIGN GOALS

There are several types of linear regulators. Note that drop out depends on a variety of factors, not just the topology (as I show later). My design will use only one power element, and thus falls under the LDO category with a minimum drop of 1 Volt.

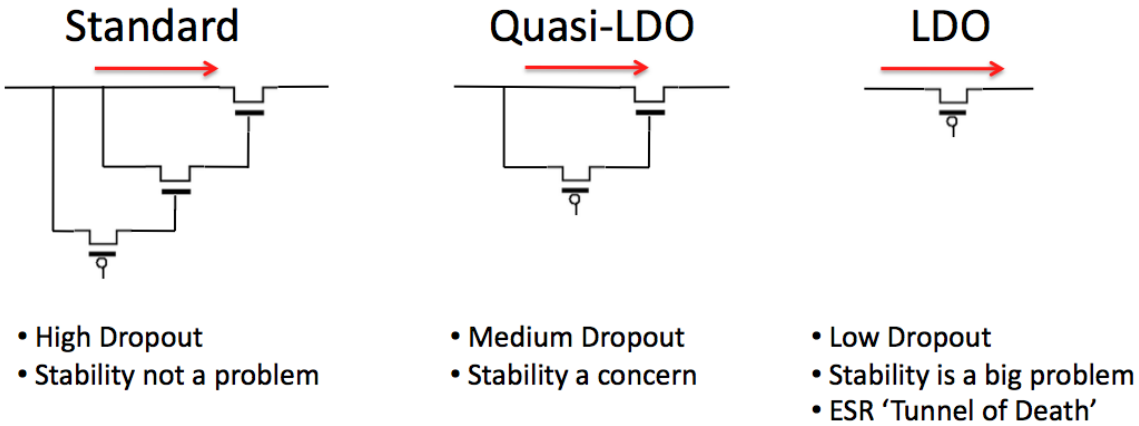


FIGURE 1. Comparison of linear regulator topologies

I have cut down significantly on the amount of I/O, external power, and references needed from my earlier, more complicated designs. Here is a black box I/O diagram of my final design:

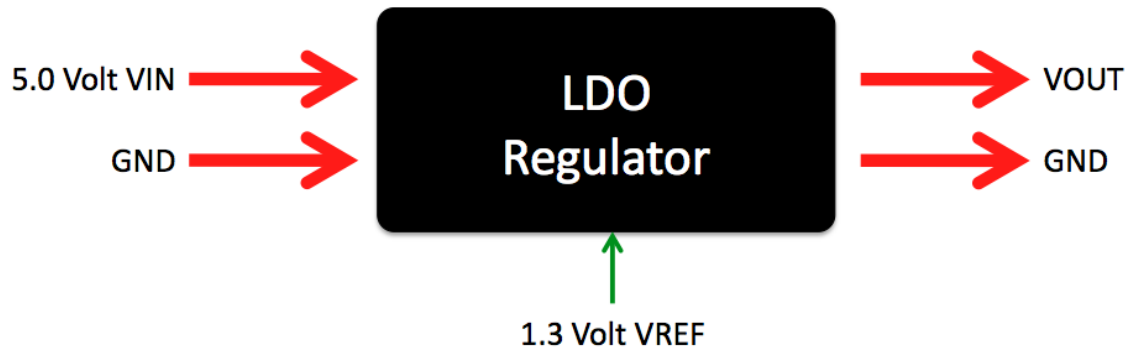


FIGURE 2. I/O Diagram

Following are the specifications I am designing to. For comparison, I am using the Texas Instruments TLV1171 which is a highly optimized linear regulator that claims 500x lower quiescent power draw over most commercial regulators.

	My LDO      Texas Instruments TLV1171		
✖	Minimum Drop Out	1.0 V	0.455 V
✔	Required Capacitance	1 pF	1 μF
✔	Pos. Settling Time	10 nano sec	~ 5 μ sec
✔	Neg. Settling Time	8 nano sec	~ 5 μ sec
✔	Pos. Slew Rate	100 V / μ sec	5V / μ sec
✔	Neg. Slew Rate	166 V / μ sec	5V / μ sec
✖	Quiescent PWR Loss	2.5 mW	0.2 mW
✔	Area	0.33 mm <sup>2</sup>	>> 1.0 mm <sup>2</sup>
✖	Max. Input	5.3 Volts	5.5 Volts
✖	Min. Input	4.7 Volts	2 Volts
✖	Max Output Current	8 mA	1.0 A
✖	Temperature Range for Vout ±200 mV	10°C to 45°C	-55°C to 150°C

FIGURE 3. I/O Diagram. Specs from Texas Instruments's part I am able to match or beat are highlighted with green; specs I am not able to match are marked with red.

### 3. DESIGN CHALLENGES

There are a few key challenges I must work around to design this linear regulator. These include a physical limitation with the power MOSFET and process limitations (limited voltage range).

**3.1. Power MOSFET Limitations.** The rule of thumb for analog amplifier design is:

$$(1) \quad \text{Max } I_{DS} = \frac{1\text{mA}}{1\mu\text{m}}$$

This suggests that I find the ideal  $\frac{W}{L}$  ratio and then scale it up to the current I need. However, there is a problem. As  $\frac{W}{L}$  decreases, the  $V_{DS}$  of the mosfet becomes a bigger factor. In order to have an efficient regulator, I need a very high  $\frac{W}{L}$ , which costs a lot of area that I do not have. On the flip side, a larger ratio decreases the size of the controllable linear region, which makes the regulator harder to control. The best compromise, is  $L = 8\mu$ ,  $W = 420 \mu$  as shown in Figure 4.

I want to find a linearization point for my feedback circuit with a large linear region. The middle graph is ideal for this. So my power MOSFET pass element will have  $\frac{W}{L} = \frac{420}{8} = \frac{52.5}{1}$  which will allow up to 8mA of output current.

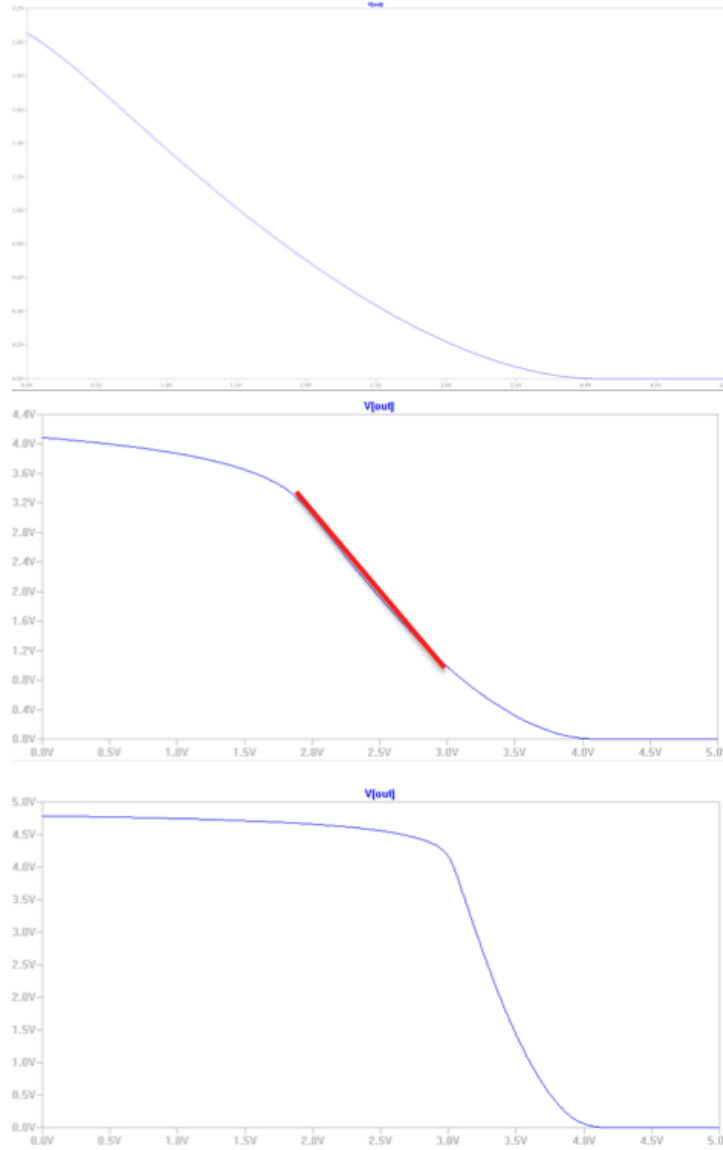


FIGURE 4.  $L = 8\mu$  for all. Top:  $W = 100\mu$ , Middle:  $W = 420\mu$ , Bottom:  $W = 1000\mu$ .  $V_{DS}$  vs  $V_{GS}$  for a single MOSFET using our technology. This is an important graph because  $V_{DS}$  determines the output voltage and  $V_{GS}$  is what I use to control it. Note the nice linear region in the middle one.

**3.2. Process Limitation: No Negative Voltage.** Use of the negative voltage rail allows a PID controller to be directly implemented in the feedback path. A negative voltage allows me to create an op amp differentiator around a zero point, so that a  $V_{out}$  that is too high can directly cause a gate voltage to compensate. My initial design assumed I had access to this negative voltage, so my controller looked like Figure 5:

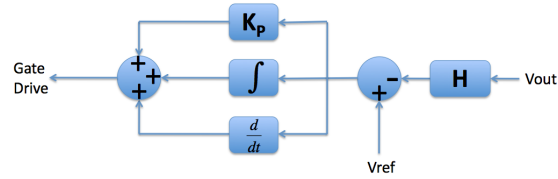


FIGURE 5. The initial PID controller I designed.

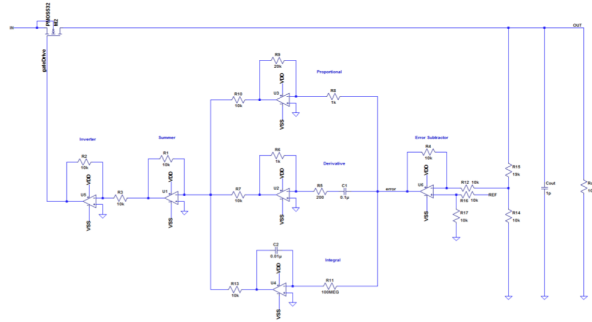


FIGURE 6. Using this, I can precisely control the output.

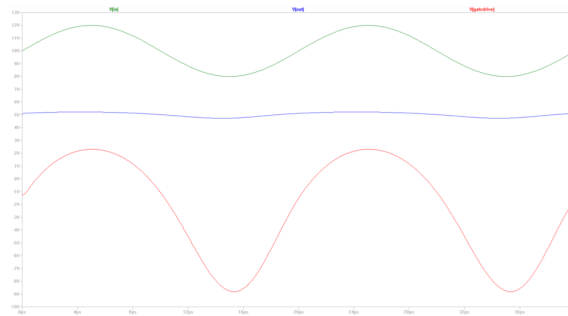
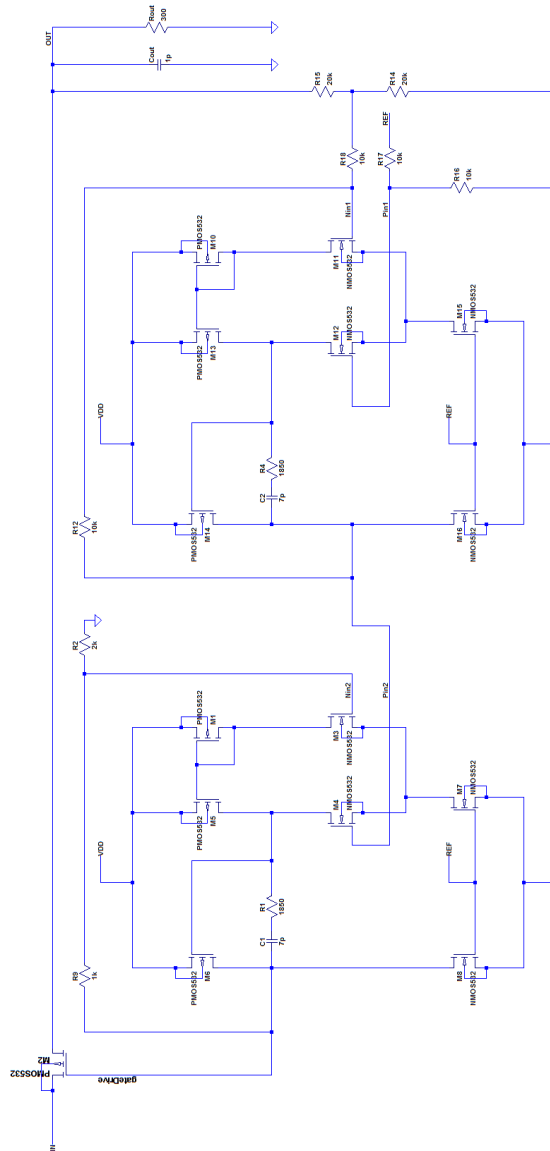


FIGURE 7. PID controlled output voltage (blue) with a 4V sinusoidal input (green) and the PID controller output (red) to precisely control the blue output and keep it constant.

My solution is to reduce the feedback path to a proportional-only controller, and then use the same reference as I am already using for the op-amps, which is 1.3 Volts. With a 2 Volt output, I then have  $V_{error} = 0.3$  which drives my gate to give a 2.0 Volt output. I can tune this to provide a 4.0 Volt output and anything in between or down to 1.0 V as well. These are shown later in the simulations.



Here is the final design:



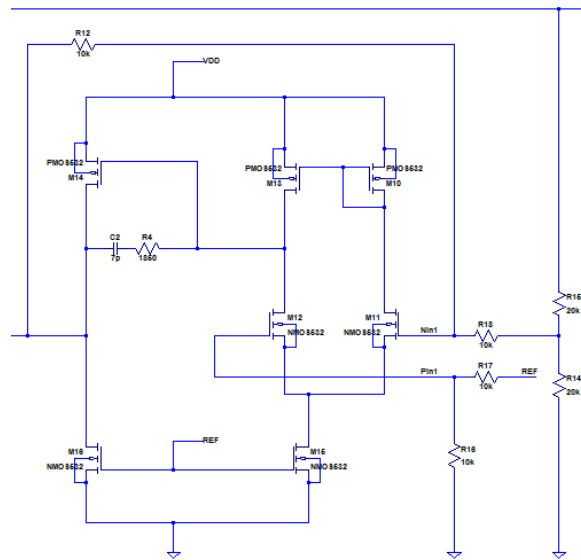


FIGURE 9. Close up of differential amplifier.

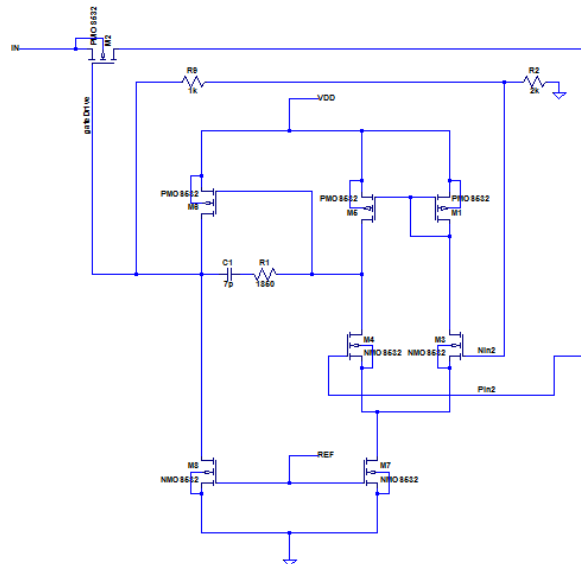


FIGURE 10. Close up of gain amplifier and gate driver.



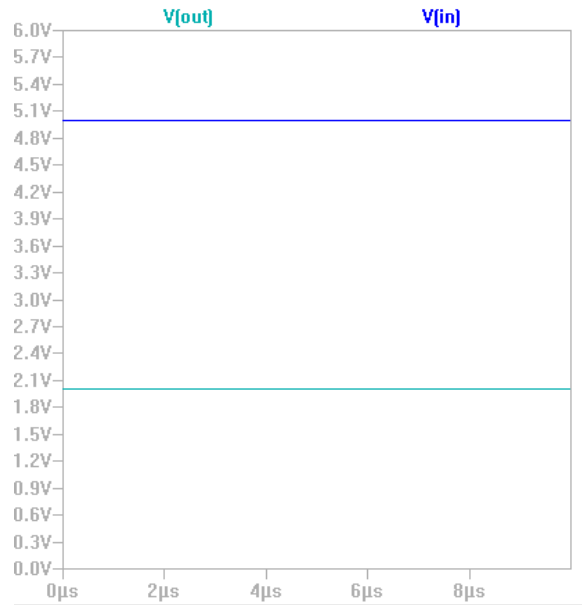


FIGURE 11. Steady State Output. Showing the amplifier tuned for  $V_{out} = 2.00$ .

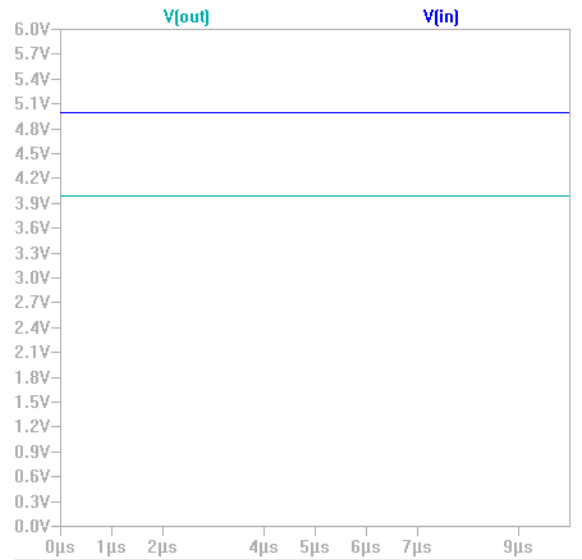
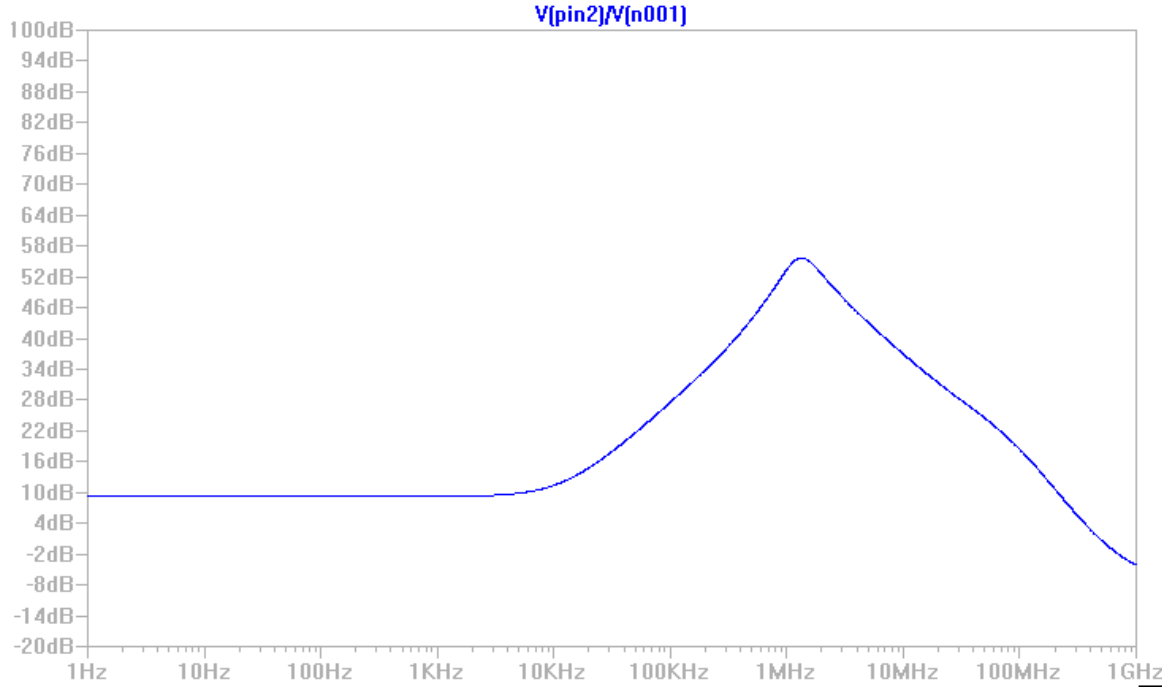


FIGURE 12. Steady State Output. Showing the amplifier tuned for  $V_{out} = 4.00$ .

## 5. SIMULATIONS

Both are accurate in steady state to within 2%.

FIGURE 13. Loop Gain,  $T(s)$ .

The loop gain,  $T(s)$  is between 10 dB and 60 dB. Note in my previous designs the loop gain was about -20 dB. I have greatly improved it here. This is very import because for a negative feedback voltage regulator we have:

- Voltage noise on the input is rejected in proportion to  $\frac{1}{1+T(s)}$ , which is  $\approx 0$  if  $T(s)$  is very high.
- Voltage disturbances on the load are rejected in proportion to  $\frac{1}{1+T(s)}$ , which is  $\approx 0$  if  $T(s)$  is very high.
- The reference voltage is followed in proportion to  $\frac{T(s)}{1+T(s)}$ , which is  $\approx 1$  if  $T(s)$  is very high.

Therefore, since my loop gain,  $T(s)$  is sufficiently high, voltage and current disturbances should be rejected well as they are multiplied by a very small number, and the reference voltage should be followed well as it is multiplied by something close to unity.

Note that the above is the idea case; several non-idealities as well as the fact my error amplifier cannot realize the entire negative range will hamper the affect of the feedback circuit to actively compensate.

The regulator maintains stability even with a sine wave of just under 1 V. The hypothetical noise rejection from the loop gain is not realized, but regulator maintains stability under load.

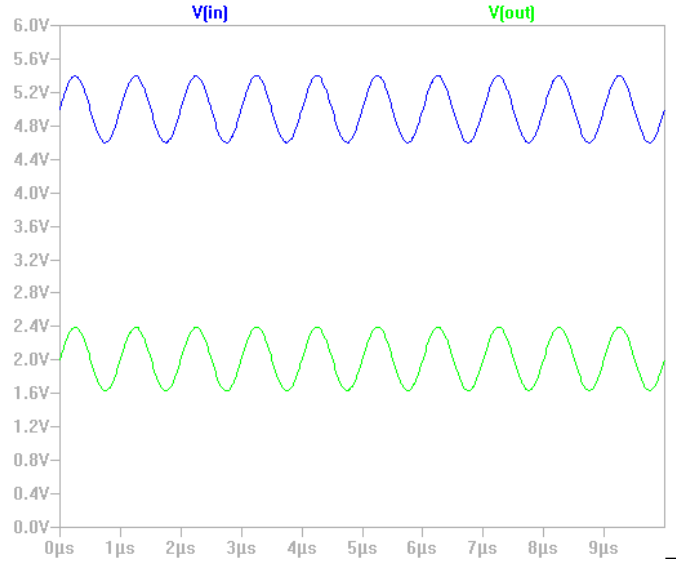


FIGURE 14.  $V_{out}$  vs  $V_{in}$  with a sine wave on the input.

Here is the steady state current draw and power loss across the control circuitry:

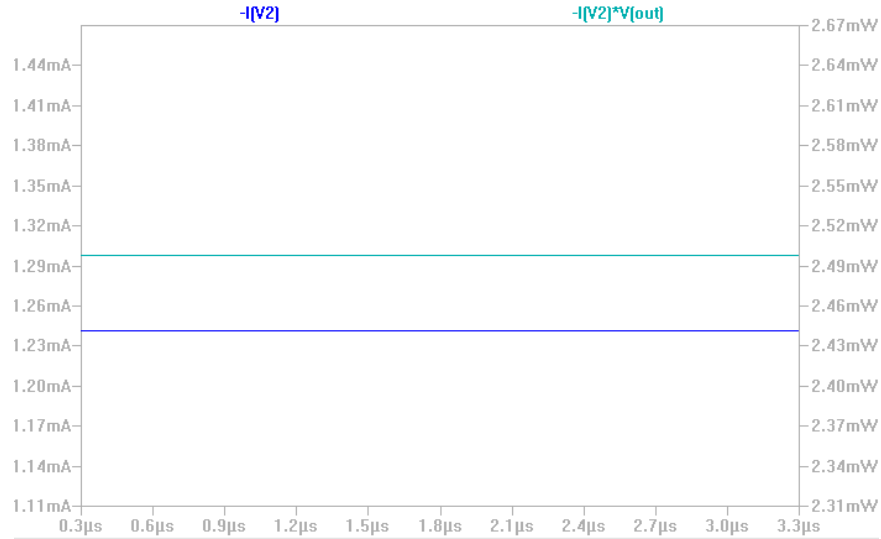
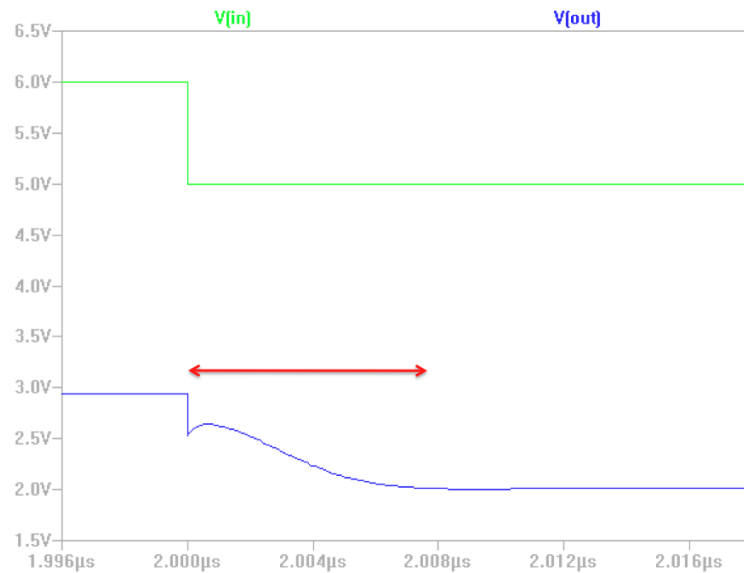
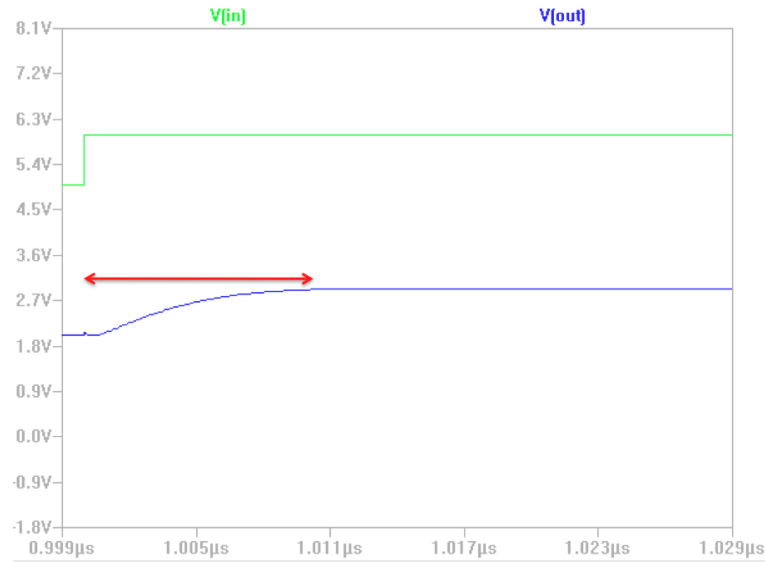


FIGURE 15. Steady state current draw and steady state power loss through control circuitry. The quiescent power loss is 2.5 mW.

The positive settling time is 10 nano seconds. The negative settling time is 8 nano seconds. From the linear section of the same graphs, I also get the slew rates:

$$\text{Positive slew rate} = \frac{100 \text{ Volts}}{\mu \text{ sec}}$$

$$\text{Negative slew rate} = \frac{166 \text{ Volts}}{\mu \text{ sec}}$$



Here is a temperature sweep of my regulator over a 35 degree Celsius range from 10 degrees Celcius to 45 degrees Celcius. It keeps the output without a 200 mV range of optimal. Outside of these temperatures performance is adversely affected.

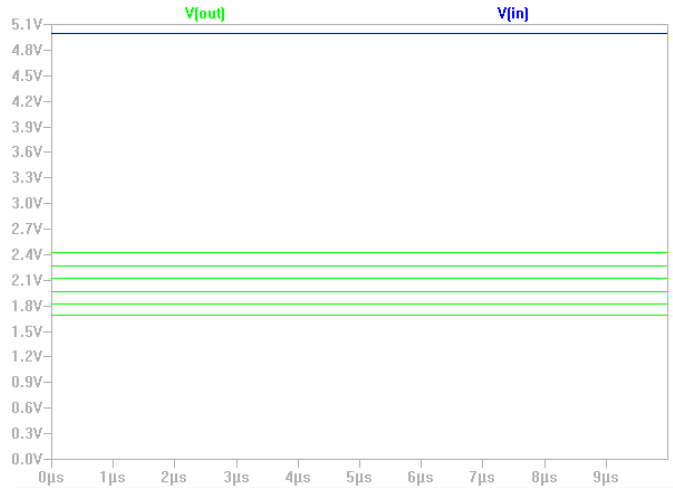
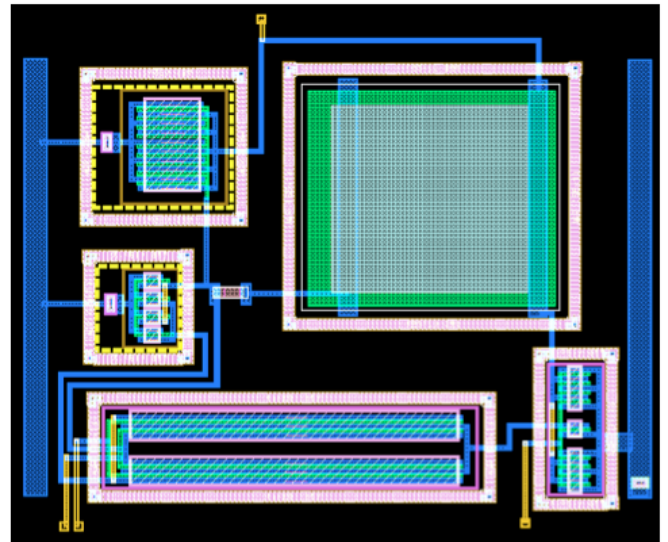
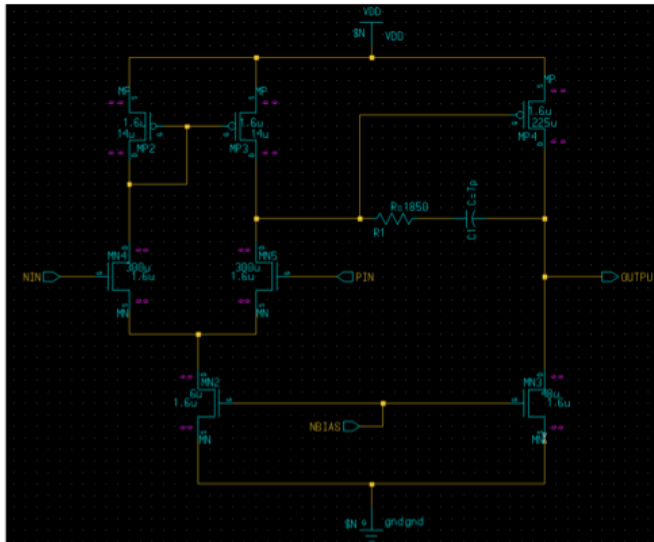


FIGURE 16. Regulator operation from 10 degrees C (top) to 45 degrees C (bottom) in 5 degree increments.

## 6. LAYOUT

I improved my op amp from homework 4 for this project. Here is my new op amp (the one I used above in simulations) as a schematic and also the layout for it.



For the rest of my design, I have several resistors that I need to common centroid. Here is my common centroid scheme:

Op Amps	Inverting Amplifier	Differential Amplifier	Feedback Divider
Common centroid already completed in homework 4	R1: 1 kΩ R2: 2 kΩ  Unit Resistor for common centroid: 1 kΩ	R1: 10 kΩ R2: 10 kΩ R3: 10 kΩ R4: 10 kΩ  Unit Resistor for common centroid: 5 kΩ	R1: 20 kΩ R2: 20 kΩ  Unit Resistor for common centroid: 10 kΩ

FIGURE 17. My common centroid scheme.

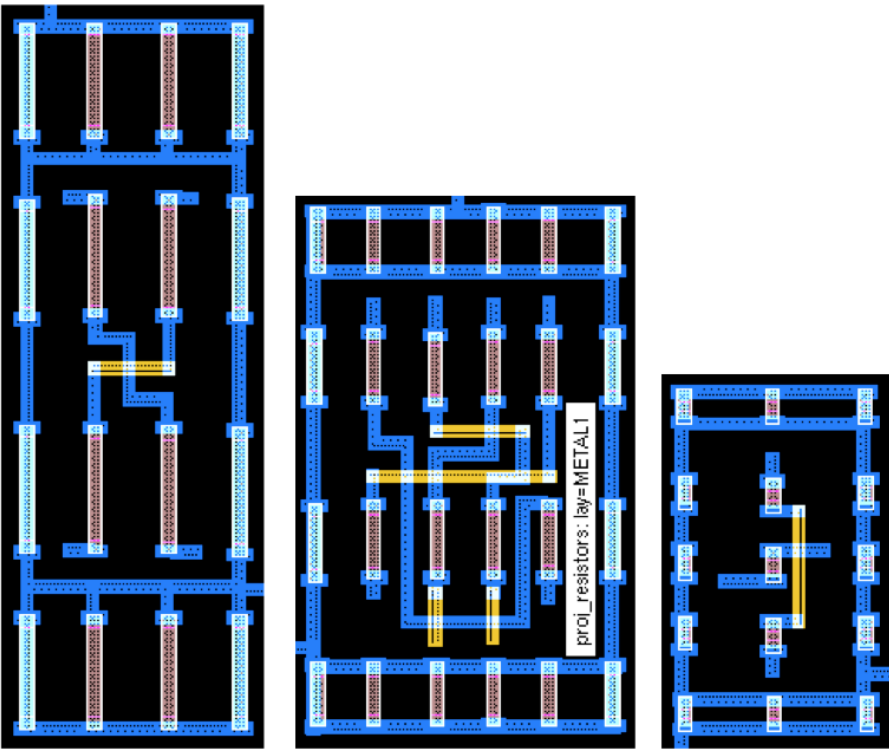


FIGURE 18. Common centroid resistors with dummy resistors added around the outside.

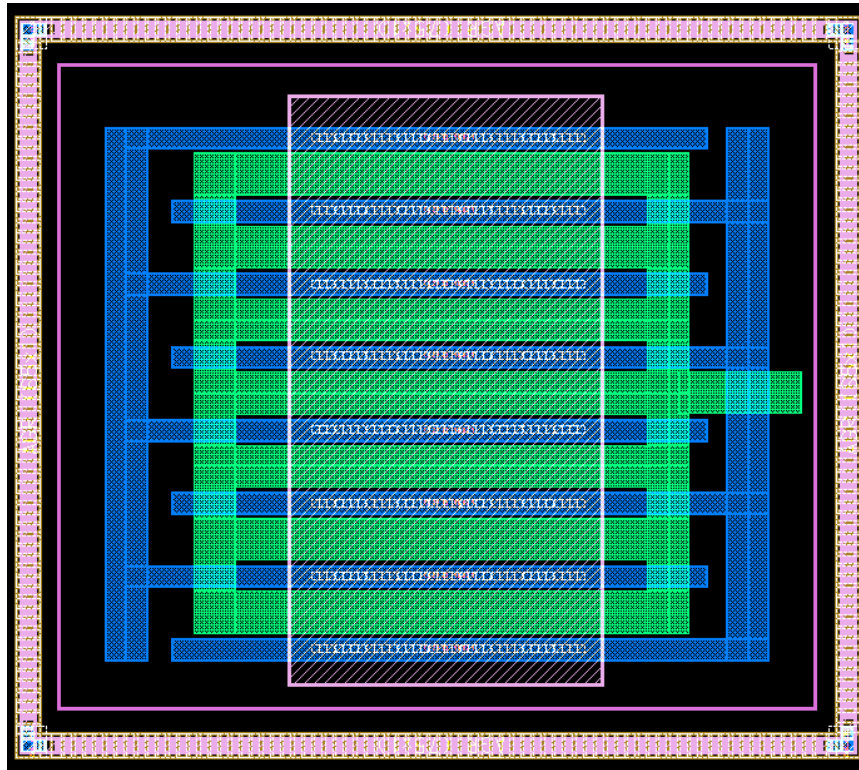


FIGURE 19. Power MOSFET. This is the pass element that controls power flow through the regulator.

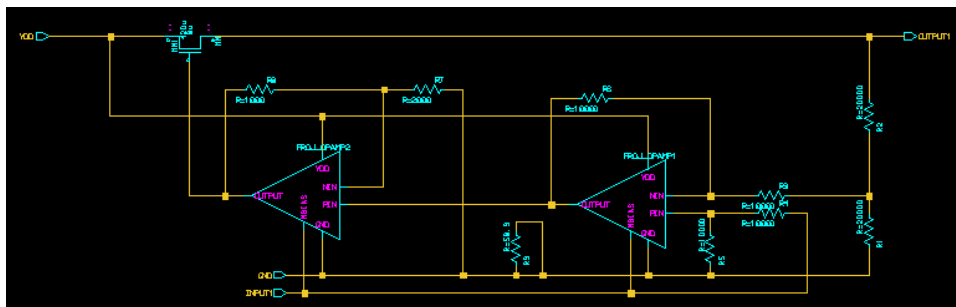


FIGURE 20. Final design in Design Architect.

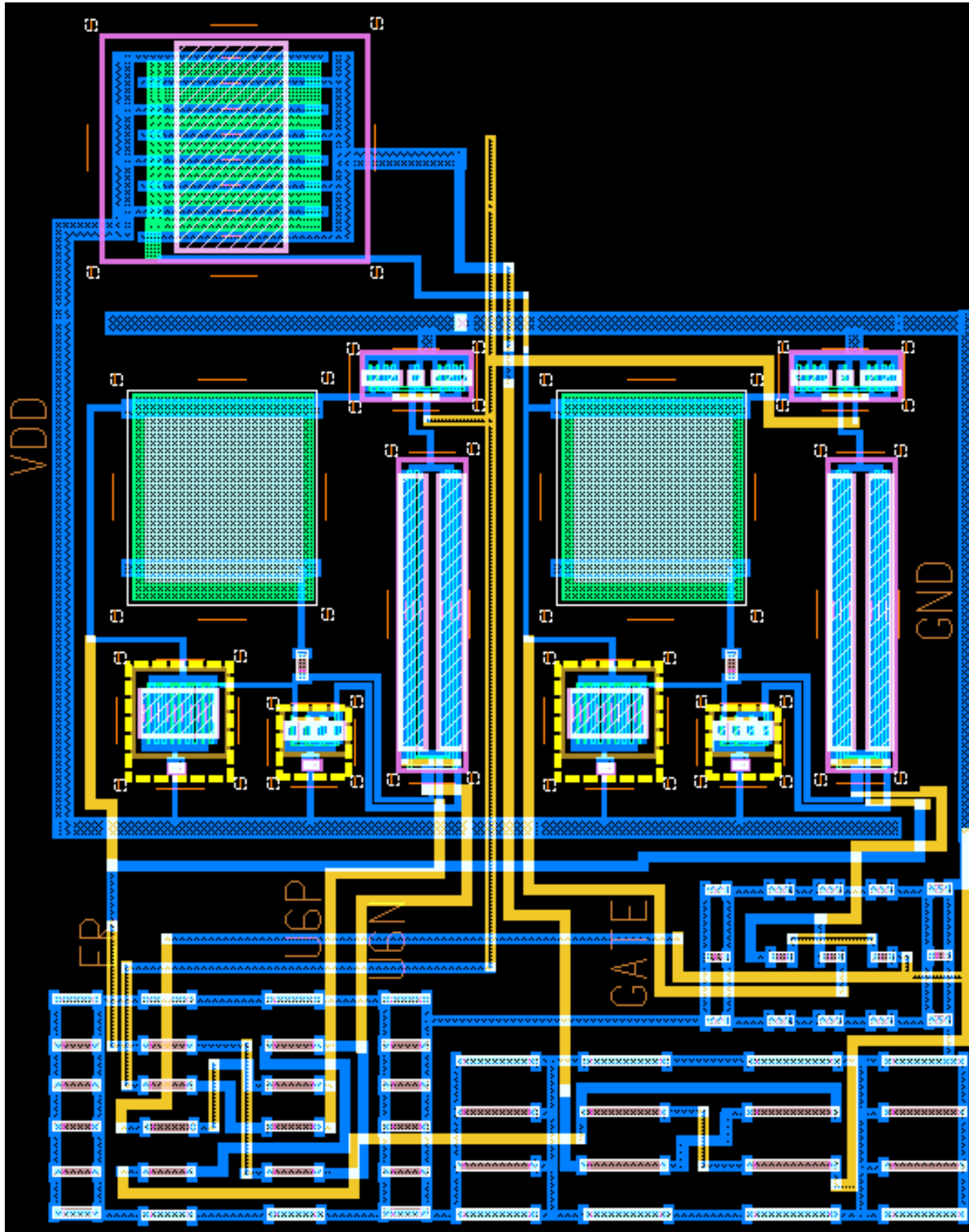


FIGURE 21. Final Layout.



Note: DRC completed. Total RuleChecks: 120; Total Results: 0; Total Original Geometries: 9521; CPU Time: 0.08, REAL Time: 0.113497.

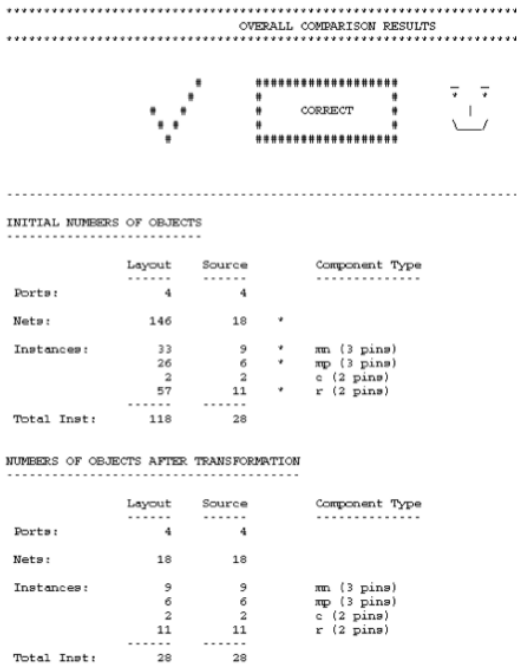


FIGURE 22. The design is DRC (top) and LVS (bottom) clean.

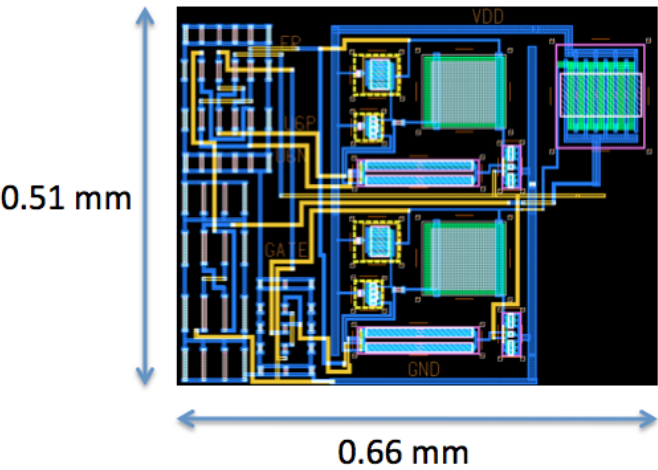


FIGURE 23. The area is 0.33 mm<sup>2</sup>.