ECE 532 FINAL PROJECT: VOLTAGE REGULATOR

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1. Introduction

In this report I will detail the design of a linear regulator that takes a 5 volt input and outputs 1.5 volts on the output.

This report is divided into the following sections:

(1) Design Goals
(2) Design Challenges
(3) Schematics
(4) Simulations
(5) Layout
(6) Fabrication

2. Design Goals

There are several types of linear regulators. Note that drop out depends on a variety of factors, not just the topology (as I show later). My design will use only one power element, and thus falls under the LDO category (even though I am going to optimize it to output 2.5 volts).

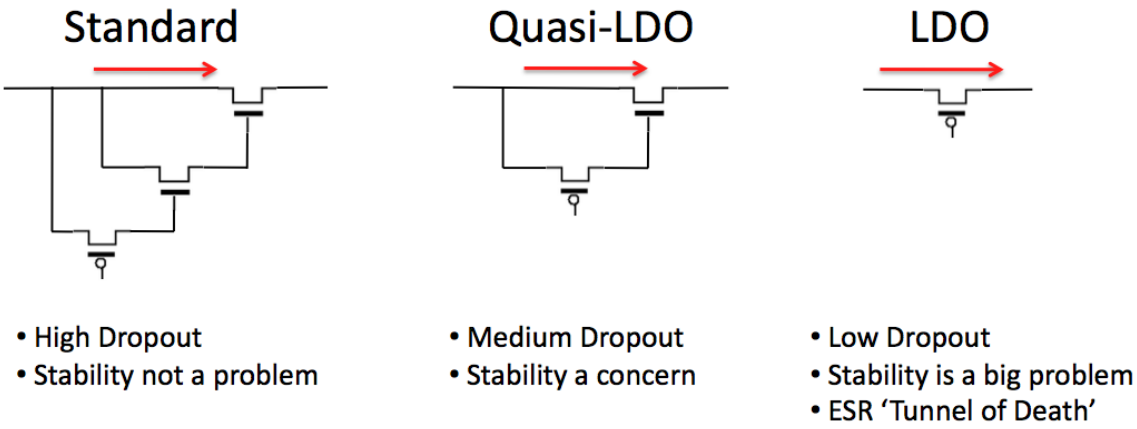


Figure 1. Comparison of linear regulator topologies

I have cut down significantly on the amount of I/O, external power, and references needed from my earlier, more complicated designs. Here is a black box I/O diagram of my final design:

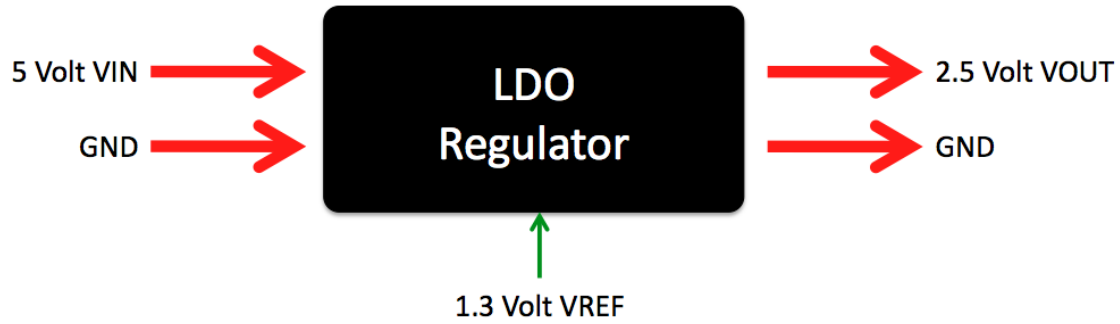


Figure 2. I/O Diagram

Following are the specifications I am designing to. For comparison, I am using the Texas Instruments TLV1171 which is a highly optimized linear regulator that claims 500x lower quiescent power draw over most commercial regulators. Note the TI part outputs 2V, mine will output 2.5 Volts.

	My LDO	Texas Instruments TLV1171
Minimum Drop Out	0.5 V	0.455 V
Required Capacitance	1 pF	1 µF
Pos. Settling Time	16 nano sec	~ 5 µ sec
Neg. Settling Time	25 nano sec	~ 5 µ sec
Pos. Slew Rate	5 V / µ sec	5V / µ sec
Neg. Slew Rate	66 V / µ sec	5V / µ sec
Quiescent PWR Loss	2.4 mW	0.2 mW
Area		>> 1.0 mm^2
Max. Input (+200 mV)	5.3 Volts	5.5 Volts
Min. Input (-200 mV)	4.7 Volts	2 Volts
Max Output Current	8 mA	1.0 A
Temperature Range for Vout ±200 mV	0°C to 50°C	-55°C to 150°C

FIGURE 3. I/O Diagram. Specs I am able to match or beat are highlighted with green; specs I am not able to match are in red.

3. Design Challenges

There are a few key challenges I must work around to design this linear regulator. These include a physical limitation with the power MOSFET and process limitations (limited voltage range).

3.1. Power MOSFET Limitations.

The rule of thumb for analog amplifier design is:

$$\text{Max } I_{DS} = \frac{1\text{mA}}{1\mu m} \tag{1}$$

This suggests that I find the ideal $\frac{W}{L}$ ratio and then scale it up to the current I need. However, there is a problem. As $\frac{W}{L}$, decreases, the V_{DS} of the mosfet becomes a bigger factor. In order to have an efficient regulator, I need a very high $\frac{W}{L}$, which costs a lot of area that I do not have. On the flip side, a larger ratio decreases the size of the controllable linear region, which makes the regulator harder to control.

I want to be able to control my output around 2.5 volts. Therefore, I need to have the linear region be centered around 2.5 volts. Furthermore, I want to be able to push through several mA, so I will choose L = 8u. See the plots to see how I chose my ideal W, which will be 420.

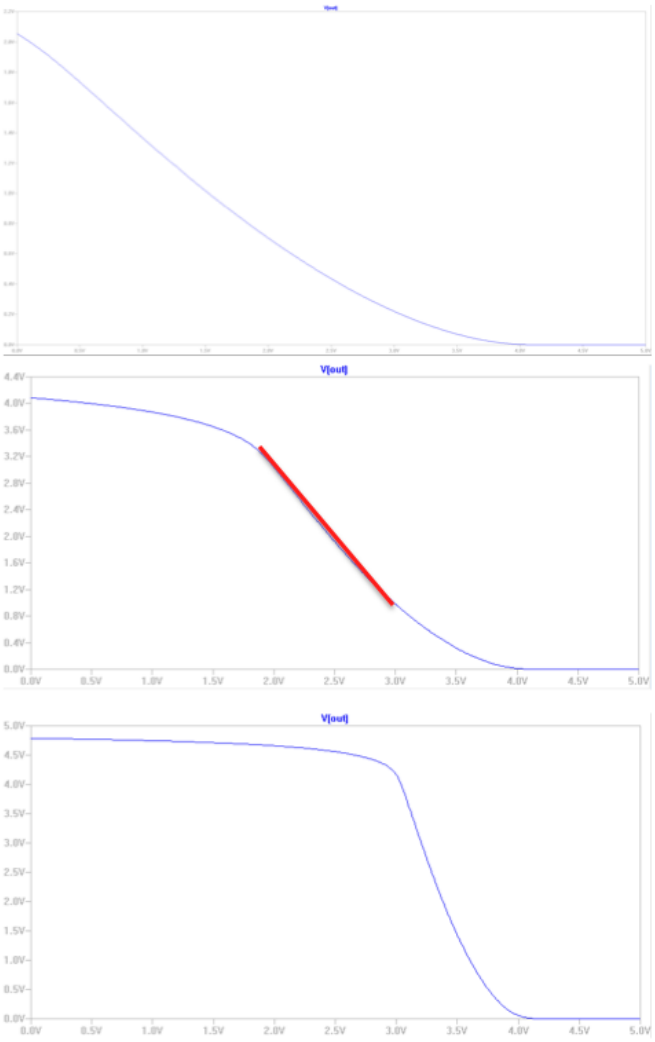


FIGURE 4. Top: W = 100, Middle: W = 420, Bottom: W = 1000. V_{DS} vs V_{GS} for a single MOSFET using our technology. This is an important graph because V_{DS} determines the output voltage and V_{GS} is what I use to control it. Note the nice linear region around 2.5V for my L = 8u, W = 420u.

3.2. **Process Limitation: No Negative Voltage.** Use of the negative voltage rail allows a PID controller to be directly implemented in the feedback path. A negative voltage allows me to create an op amp differentiator around a zero point, so that a V_{out} that is too high can directly cause a

gate voltage to compensate. My initial design assumed I had access to this negative voltage, so my controller looked like Figure 5:

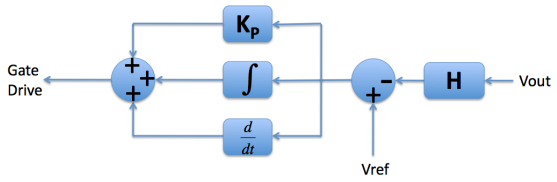


FIGURE 5. The initial PID controller I designed.

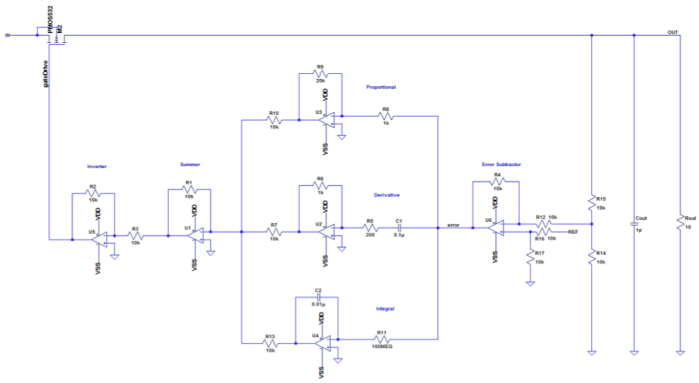


FIGURE 6. Using this, I can precisely control the output.

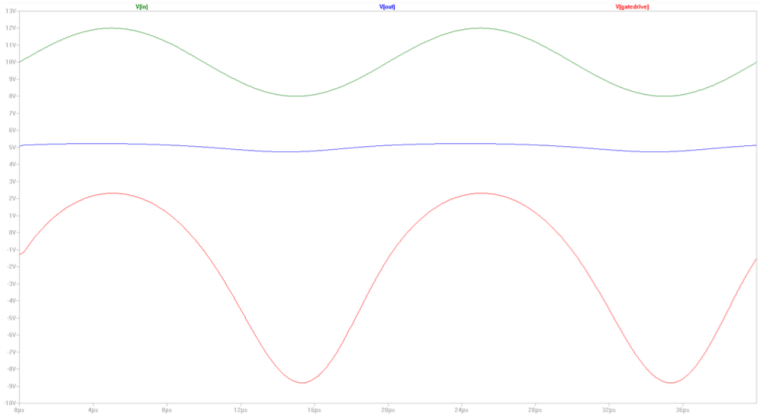


FIGURE 7. PID controlled output voltage (blue) with a 4V sinusoidal input (green) and the PID controller output (red) to precisely control the blue output and keep it constant.

However, to fabricate my design I will need to have a maximum voltage differential on chip of 5V. Therefore, I do not have access to this negative voltage rail, and I will have to improvise. To solve this I will design a negative feedback proportional-only controller that uses a differential amplifier that does not output a negative voltage. My solution is to output a voltage, 2.5V that can be output without any voltage initialization and also without the gate being needed to be driven negative. The other alternative is a complicated series of circuits and references to step the operating point up, perform the operations, and then step it back down again. Chip manufacturers do this with several hundred transistors, but I will simplify things to complete this project.

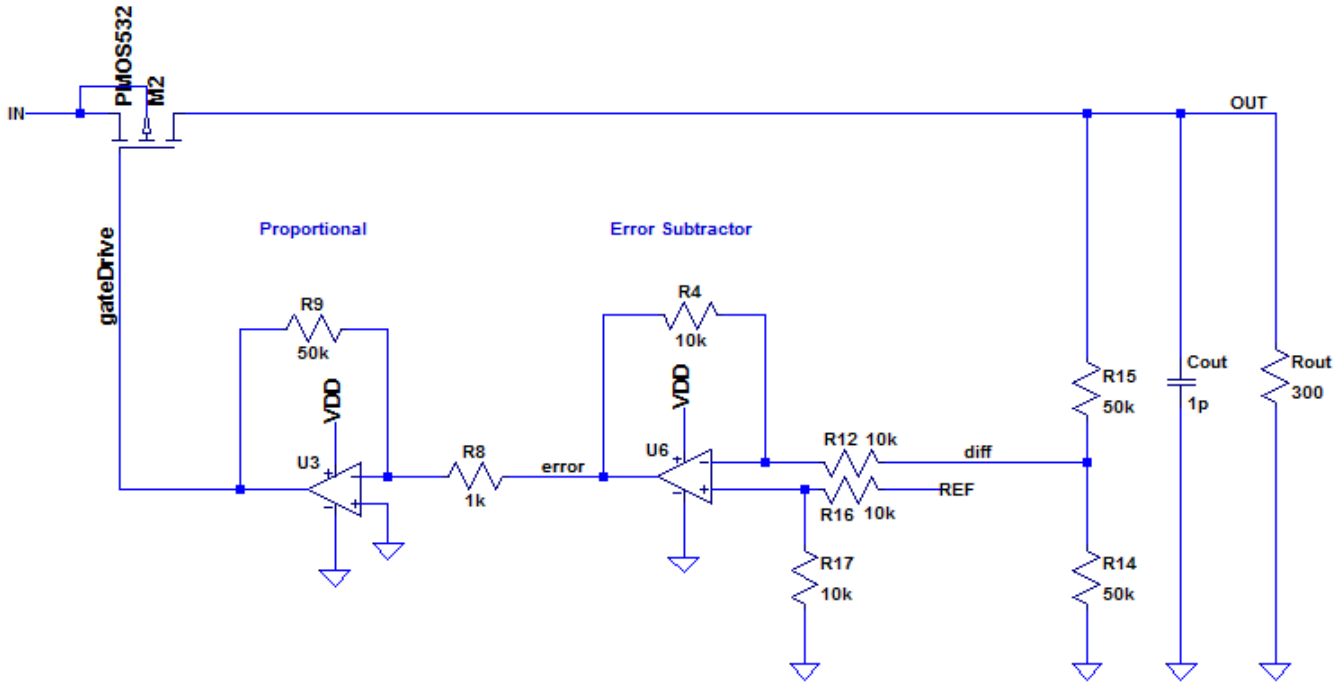
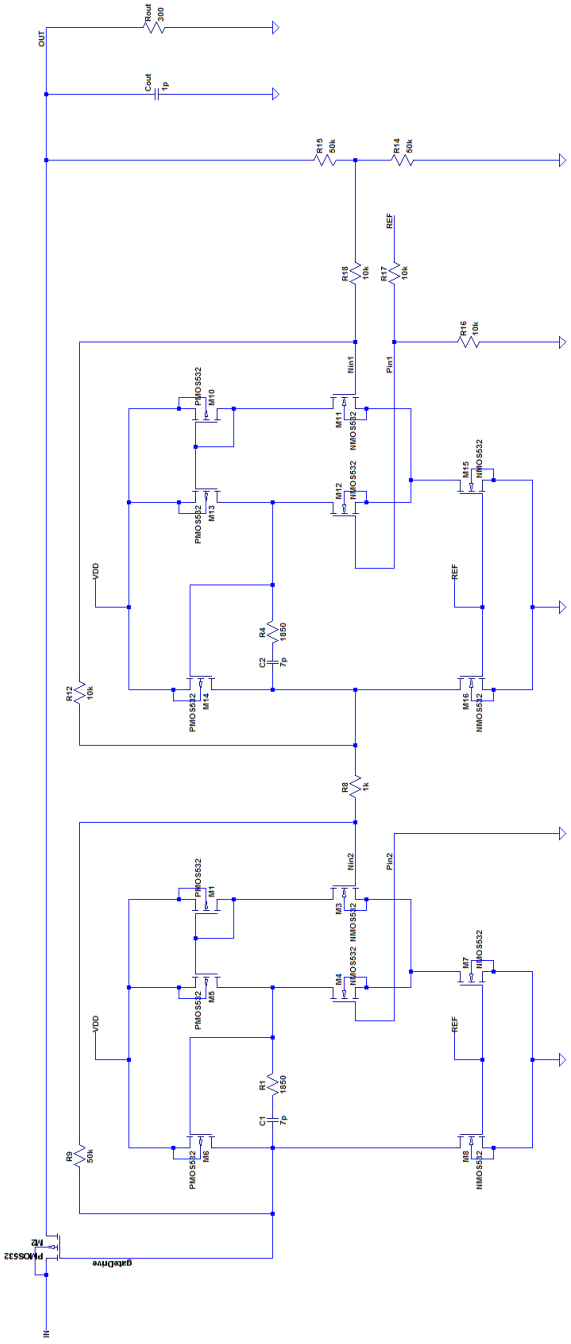


FIGURE 8. A high level view of my final design. Transistor level shown on next page.

4. Schematics

Here is the final design:



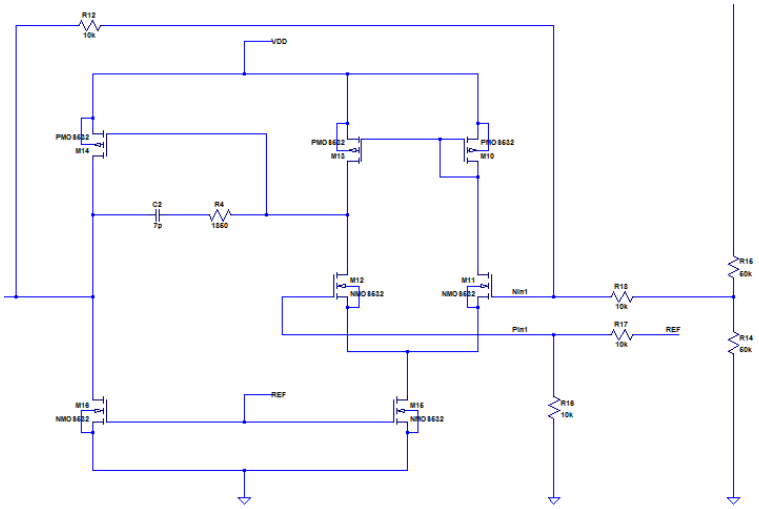


FIGURE 9. Close up of error amplifier.

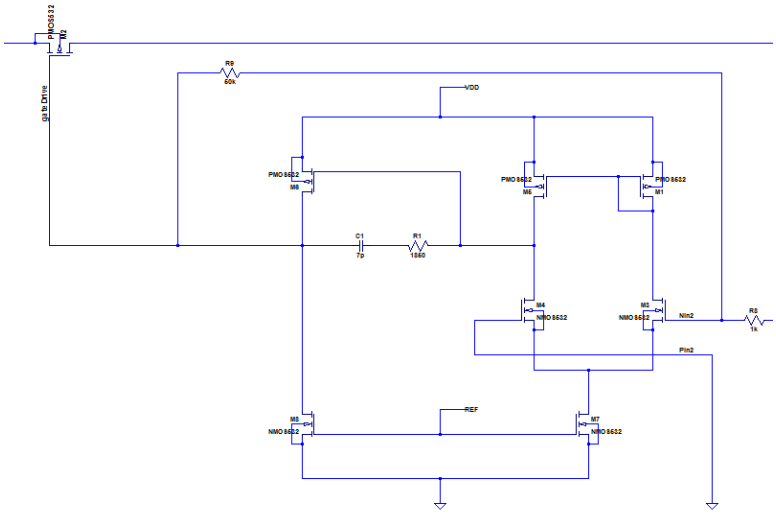


FIGURE 10. Close up of inverting amplifier and gate driver.

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5. Simulations

Figure 11. Steady State Output. V_{out} is 2.5V with the 5V input.

The output is correct to within 0.02 Volts.

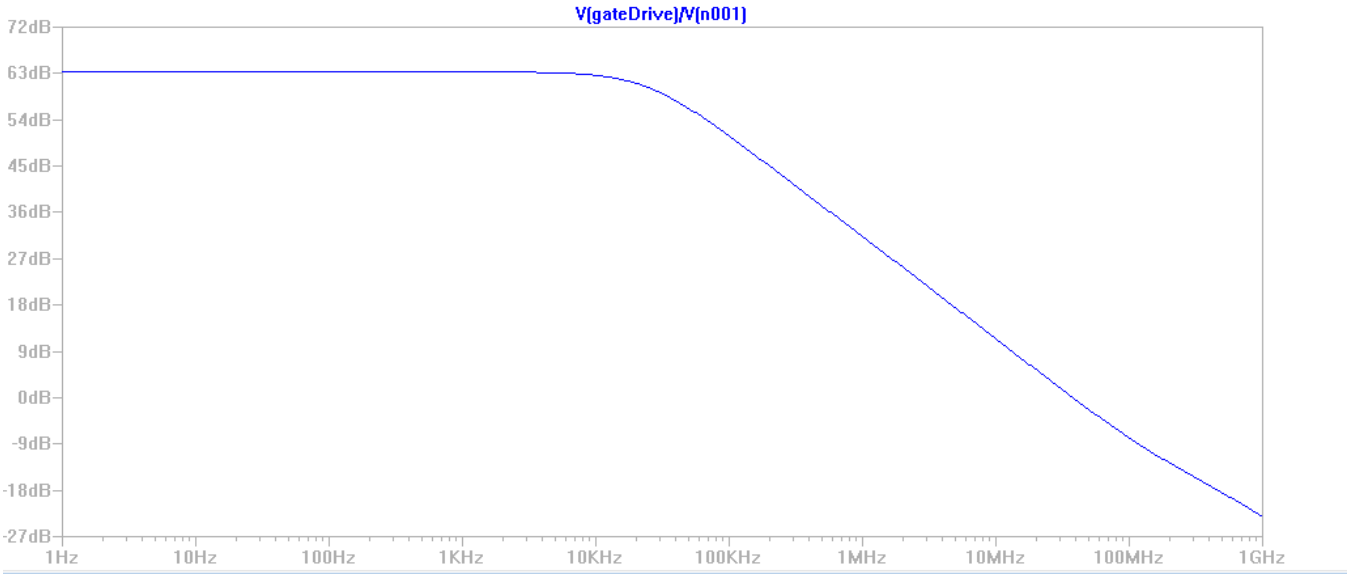

FIGURE 12. Loop Gain, $T(s)$.

The loop gain, $T(s)$ is very high, 63 dB. Note in my previous designs the loop gain was about -20 dB. I have greatly improved it here, by over 80 dB. For a negative feedback voltage regulator:

Voltage noise on the input is rejected in proportion to $\frac{1}{1+T(s)} \approx 0$.

Voltage disturbances on the load are rejected in proportion to $\frac{1}{1+T(s)} \approx 0$.

The reference voltage is followed in proportion to $\frac{T(s)}{1+T(s)} \approx 1$.

Therefore, since my loop gain, $T(s)$ is very high, voltage and current disturbances should be rejected very well as they are multiplied by 0, and the reference voltage should be followed well as it is multiplied by unity.

Note that the above is in the ideal case. I modified my error amplifier to work without a negative rail so I do not actually see nearly the ideal rejection.

Output with a sinusoidal input:

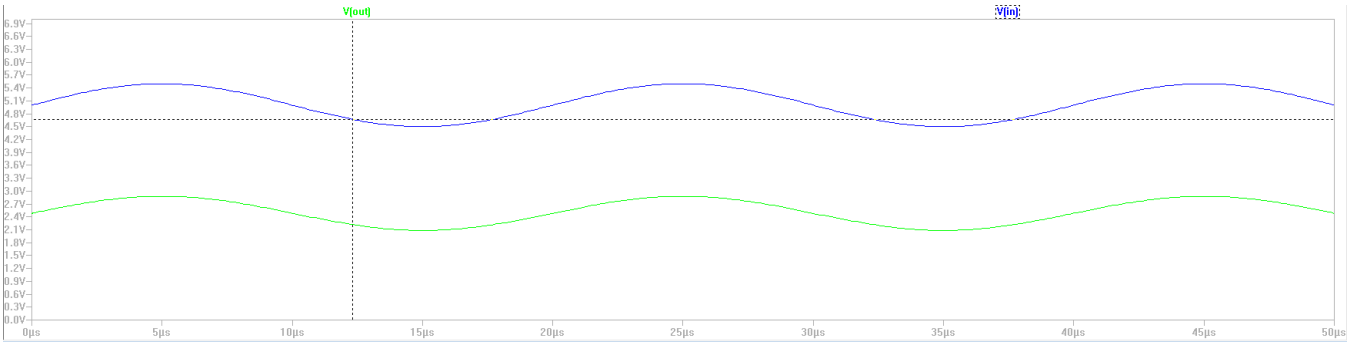

FIGURE 13. V_{out} vs V_{in} with a 1V sine wave on the input.

Here is the steady state power loss across the control circuitry:

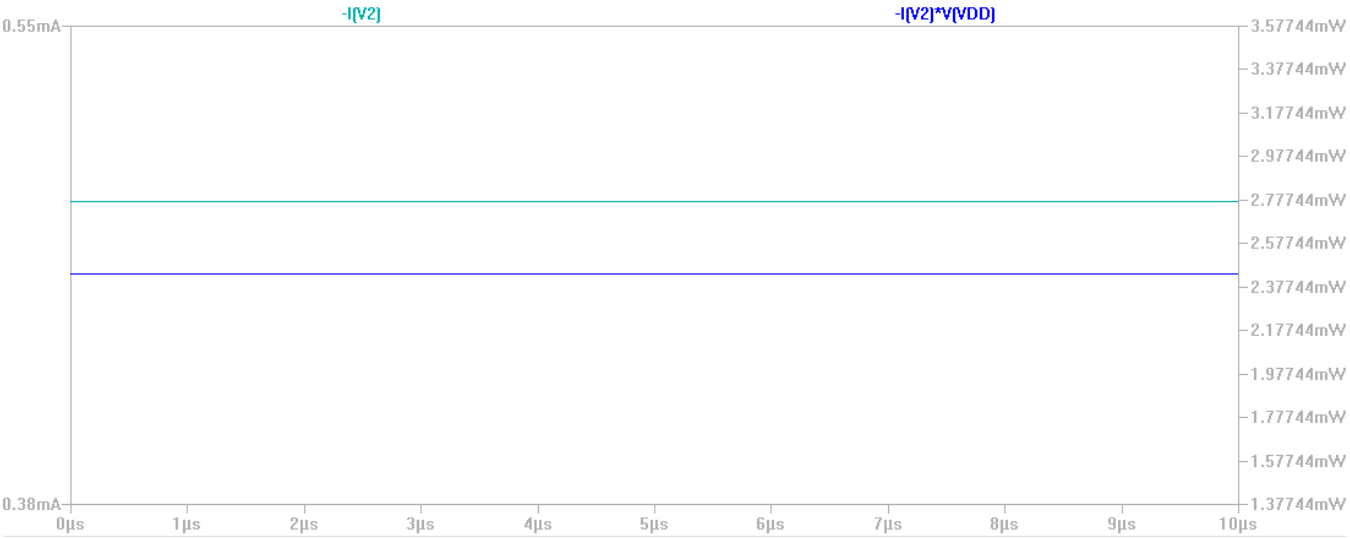

FIGURE 14. Steady state current draw and steady state power loss through control circuitry. The quiescent power loss is 2.4 mW.

The positive settling time is 16 nano seconds.

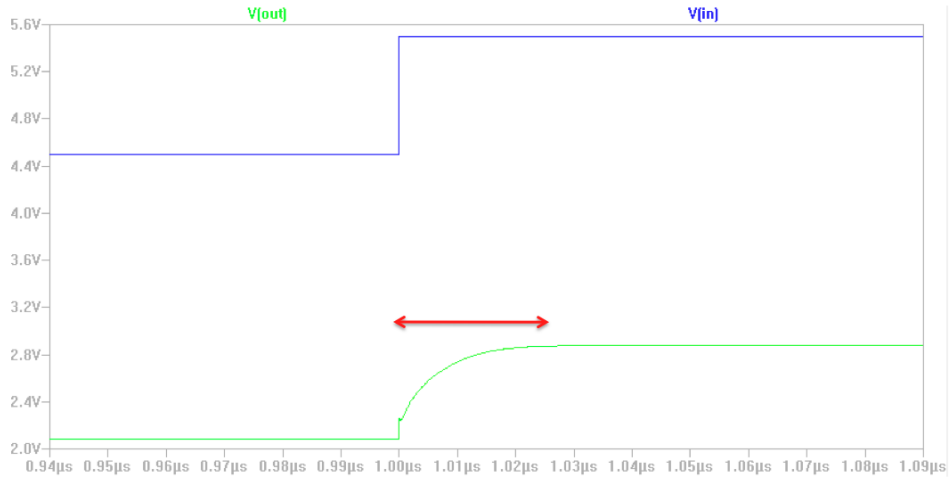

FIGURE 15. Positive settling time = 16 ns

The negative settling time is 25 nano seconds

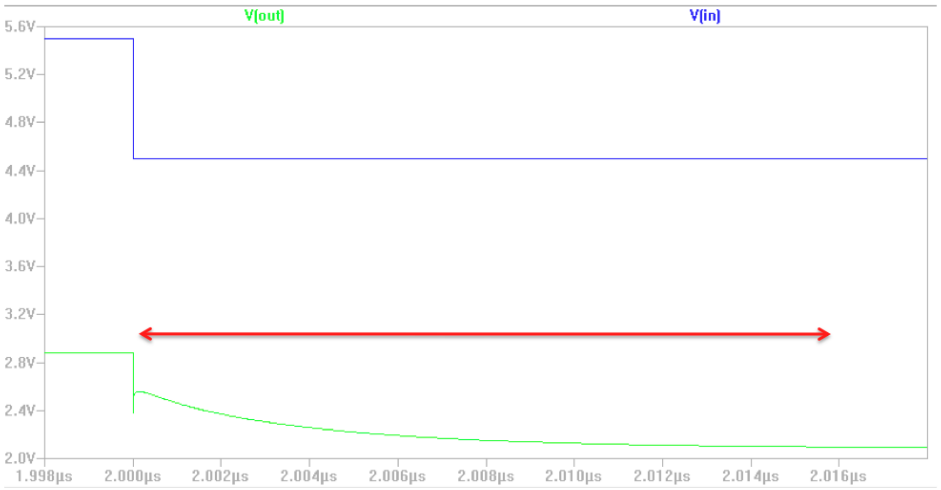

FIGURE 16. Negative settling time = 25 ns.

From the same graphs, I also get the slew rates:

$$\text{Positive slew rate} = \frac{5 \text{ Volts}}{\mu \text{ sec}}$$

$$\text{Negative slew rate} = \frac{66 \text{ Volts}}{\mu \text{ sec}}$$

Here is a temperature sweep of my regulator over a 50 degree Celsius range from 25 degrees below ambient to 25 degrees above ambient (0-50). It keeps the output without a 200 mV range of optimal.

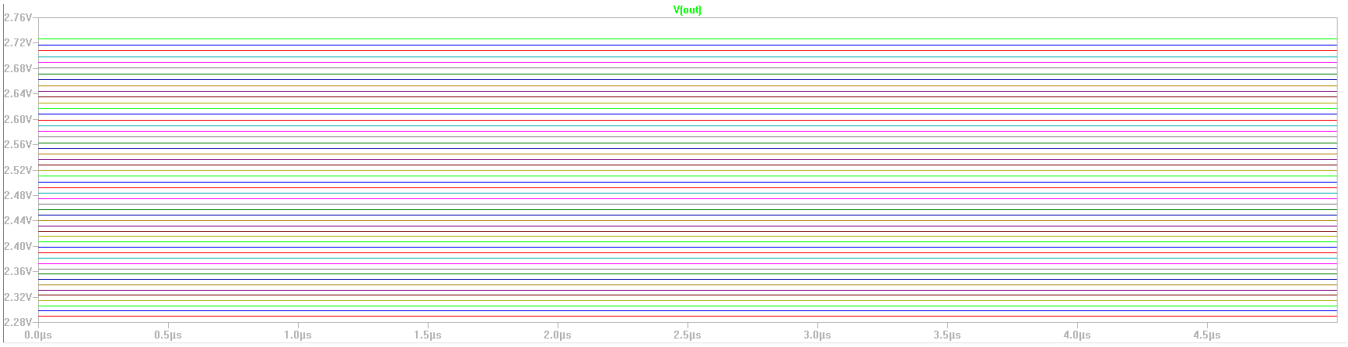

FIGURE 17. Regulator operation over a range from 0 to 50 degrees Celcius.

6. LAYOUT

I improved my op amp from homework 4 for this project. Here is my new op amp (the one I used above in simulations) as a schematic and also the layout for it.

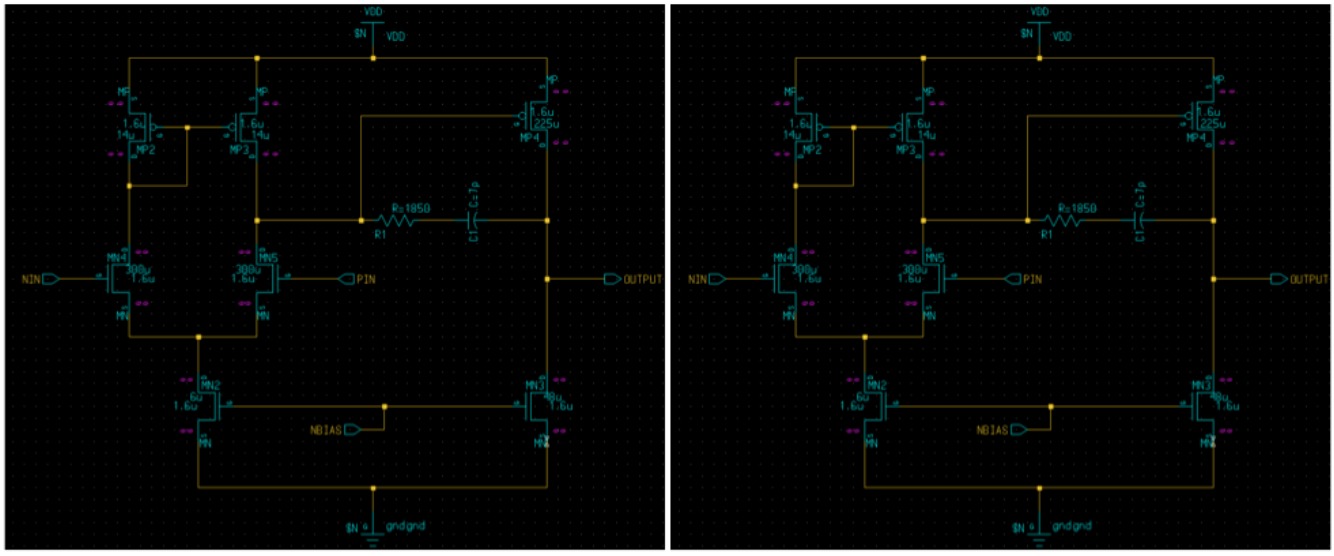

FIGURE 18. My improved op amp.

For the rest of my design, I have several resistors that I need to common centroid. Here is my common centroid scheme:

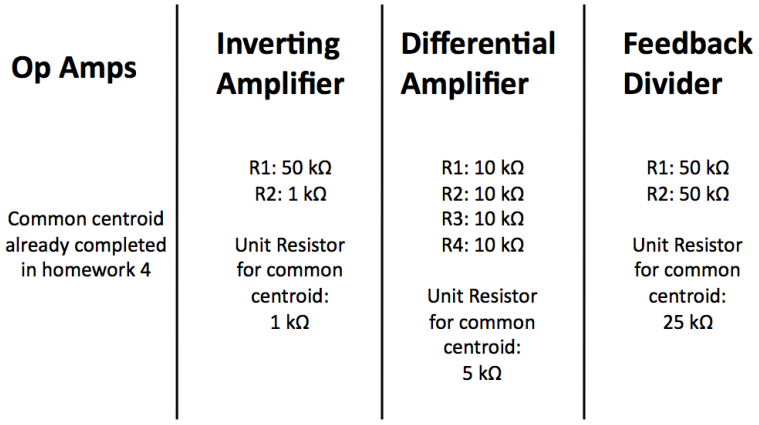

FIGURE 19. My common centroid scheme.

7. FABRICATION

I am fabricating my project, which is why I have added the extra pads at the top level. I will test the project next semester in the fall when it comes back.

8. CONCLUSION

I built a full linear regulator in this project. I learned a lot, from how to design a negative feedback controller to the design tradeoffs involved in analog circuits. Almost every decision I made had a pro and a con (such as more current vs more accurate control). The layout showed me how important it is to plan ahead and think of a project modularly.