ECE 532 FINAL PROJECT: VOLTAGE REGULATOR

JOHN O'HOLLAREN

1. Introduction

In this report I will detail the design of a linear regulator that takes a 5 volt input and outputs 1.0 - 4.0 volts on the output. I can control it by tuning the feedback amplifiers. I fine tune the final amplifier that will be fabricated to output 2.5V. I learned a lot in this project, from how to design a negative feedback controller to the design tradeoffs involved in analog circuits. Almost every decision I made had a pro and a con (such as more current vs. using more area). The layout showed me how important it is to plan ahead and think of a project modularly.

This report is divided into the following sections:

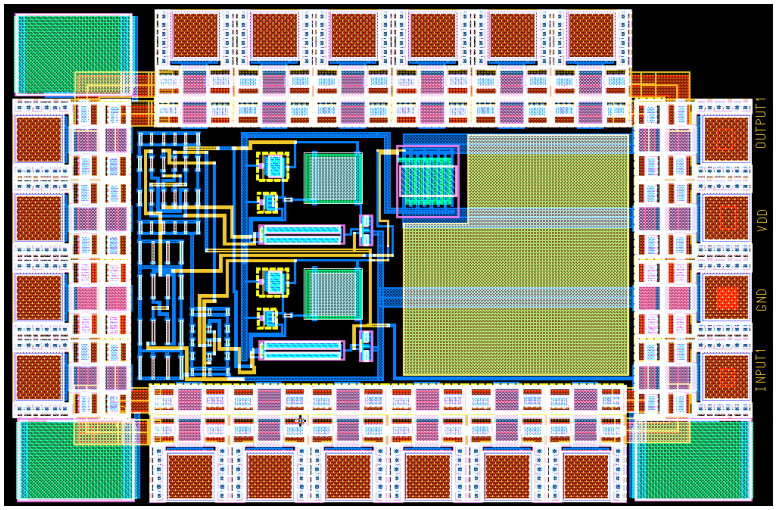
(1) Design Goals

(2) Design Challenges

(3) Schematics

(4) Simulations

(5) Layout



2. Design Goals

There are several types of linear regulators. Note that drop out depends on a variety of factors, not just the topology (as I show later). My design will use only one power element, and thus falls under the LDO category with a minimum drop of 1 Volt.

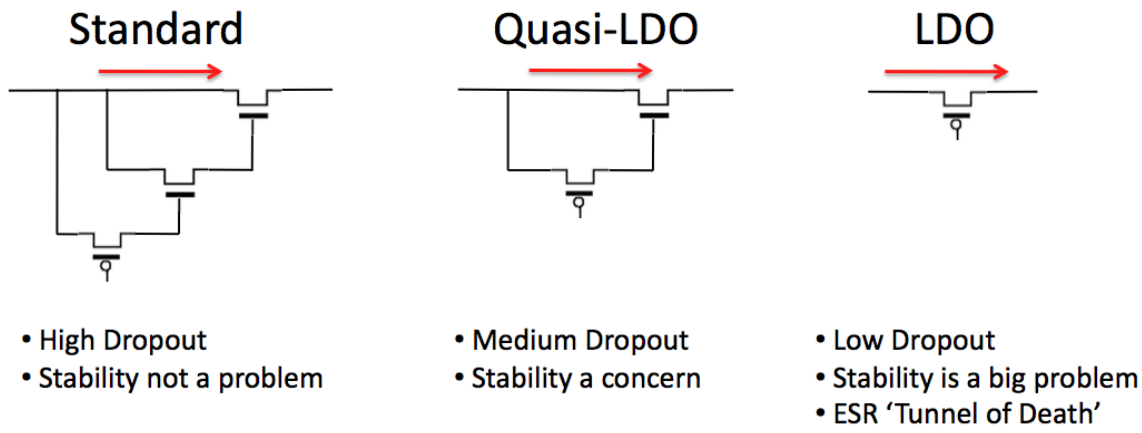


Figure 1. Comparison of linear regulator topologies

I have cut down significantly on the amount of I/O, external power, and references needed from my earlier, more complicated designs. Here is a black box I/O diagram of my final design:

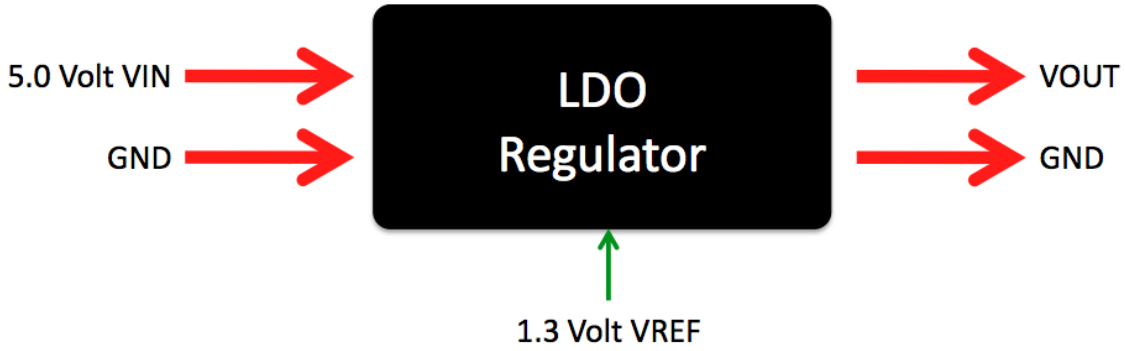


Figure 2. I/O Diagram

Following are the specifications I am designing to. For comparison, I am using the Texas Instruments TLV1171 which is a highly optimized linear regulator that claims 500x lower quiescent power draw over most commercial regulators.

	My LDO	Texas Instruments TLV1171
Minimum Drop Out	1.0 V	0.455 V
Required Capacitance	1 pF	1 µF
Pos. Settling Time	10 nano sec	~ 5 µ sec
Neg. Settling Time	8 nano sec	~ 5 µ sec
Pos. Slew Rate	100 V / µ sec	5V / µ sec
Neg. Slew Rate	166 V / µ sec	5V / µ sec
Quiescent PWR Loss	2.5 mW	0.2 mW
Area	0.33 mm^2	>> 1.0 mm^2
Max. Input	5.3 Volts	5.5 Volts
Min. Input	4.7 Volts	2 Volts
Max Output Current	8 mA	1.0 A
Temperature Range for Vout ±200 mV	10°C to 45°C	-55°C to 150°C

FIGURE 3. I/O Diagram. Specs from Texas Instruments's part I am able to match or beat are highlighted with green; specs I am not able to match are marked with red.

3. Design Challenges

There are a few key challenges I must work around to design this linear regulator. These include a physical limitation with the power MOSFET and process limitations (limited voltage range).

3.1. Power MOSFET Limitations.

The rule of thumb for analog amplifier design is:

$$\text{Max } I_{DS} = \frac{1\text{mA}}{1\mu m} \tag{1}$$

This suggests that I find the ideal $\frac{W}{L}$ ratio and then scale it up to the current I need. However, there is a problem. As $\frac{W}{L}$, decreases, the V_{DS} of the mosfet becomes a bigger factor. In order to have an efficient regulator, I need a very high $\frac{W}{L}$, which costs a lot of area that I do not have. On the flip side, a larger ratio decreases the size of the controllable linear region, which makes the regulator harder to control. The best compromise, is L = 8u, W = 420 u as shown in Figure 4.

I want to find a linearization point for my feedback circuit with a large linear region. The middle graph is ideal for this. So my power MOSFET pass element will have $\frac{W}{L} = \frac{420}{8} = \frac{52.5}{1}$ which will allow up to 8mA of output current.

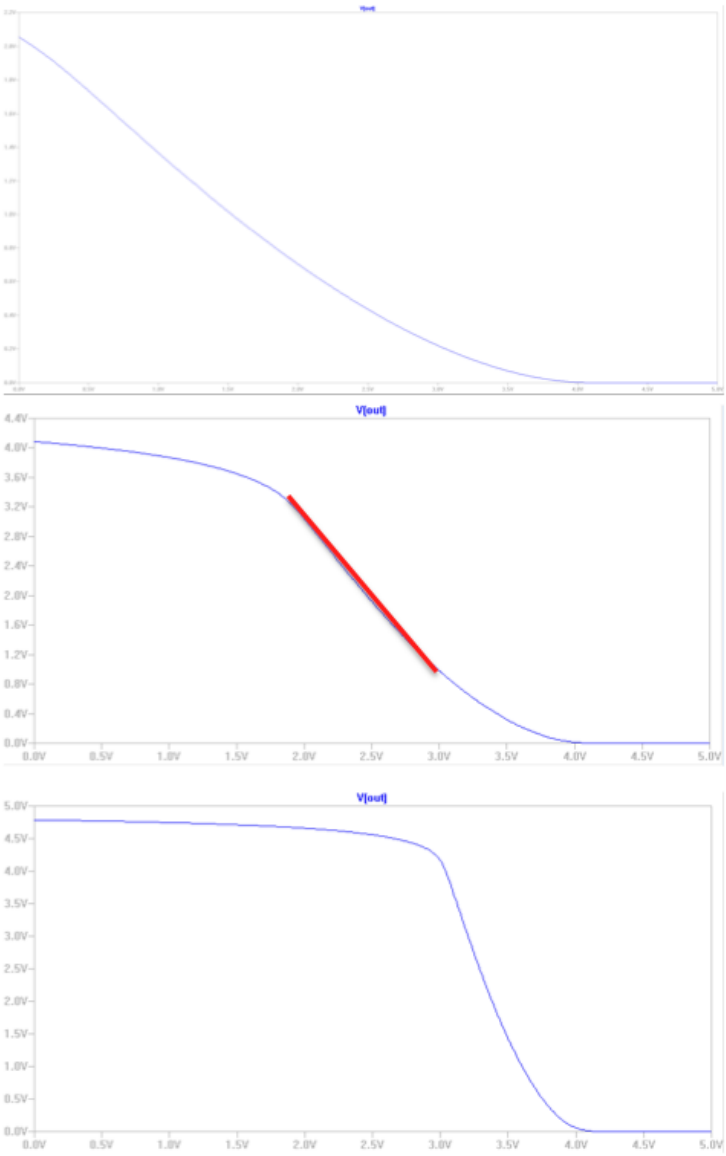


FIGURE 4. L = 8u for all. Top: W = 100u, Middle: W = 420u, Bottom: W = 1000u. V_{DS} vs V_{GS} for a single MOSFET using our technology. This is an important graph because V_{DS} determines the output voltage and V_{GS} is what I use to control it. Note the nice linear region in the middle one.

3.2. **Process Limitation: No Negative Voltage.** Use of the negative voltage rail allows a PID controller to be directly implemented in the feedback path. A negative voltage allows me to create an op amp differentiator around a zero point, so that a V_{out} that is too high can directly cause a gate voltage to compensate. My initial design assumed I had access to this negative voltage, so my controller looked like Figure 5:

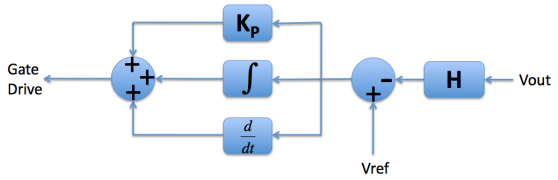


FIGURE 5. The initial PID controller I designed.

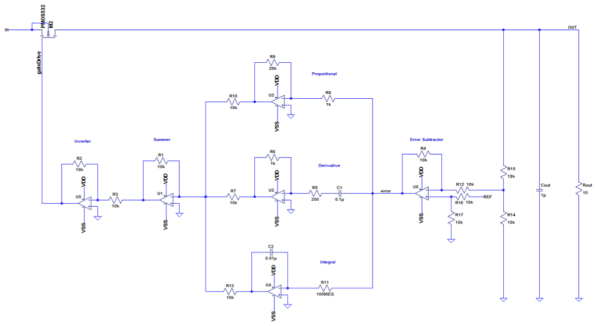


FIGURE 6. Using this, I can precisely control the output.

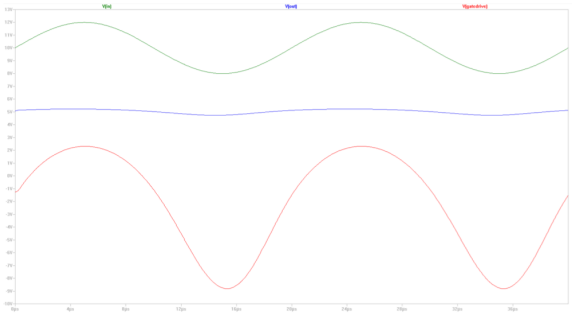


FIGURE 7. PID controlled output voltage (blue) with a 4V sinusoidal input (green) and the PID controller output (red) to precisely control the blue output and keep it constant.

However, to fabricate my design I will need to have a maximum voltage differential on chip of 5V. Therefore, I do not have access to this negative voltage rail, and I will have to improvise with a negative feedback differential amplifier that never pushes the error signal below 0.

My solution is to reduce the feedback path to a porportional-only controller, and then use the same reference as I am already using for the op-amps, which is 1.3 Volts. With a 2 Volt output, I then have $V_{error} = 0.3$ which drives my gate to give a 2.0 Volt output. I can tune this to provide a 4.0 Volt output and anything in between or down to 1.0 V as well. These are shown later in the simulations.

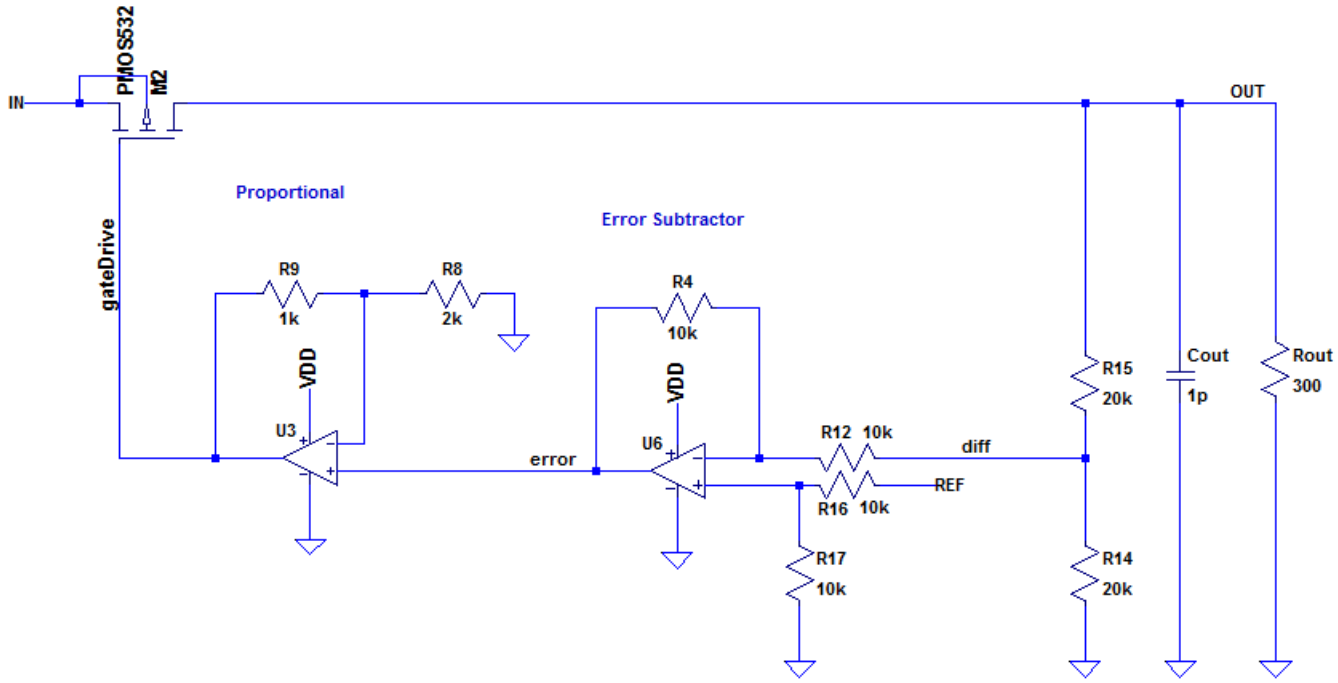
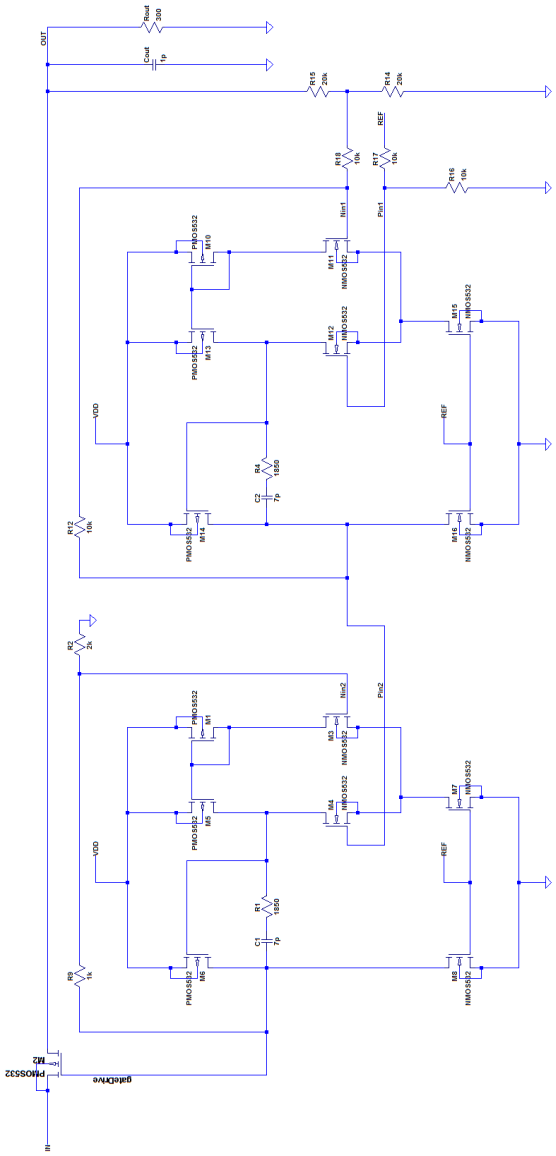


FIGURE 8. A high level view of my final design. Transistor level shown on next page.

4. Schematics

Here is the final design:



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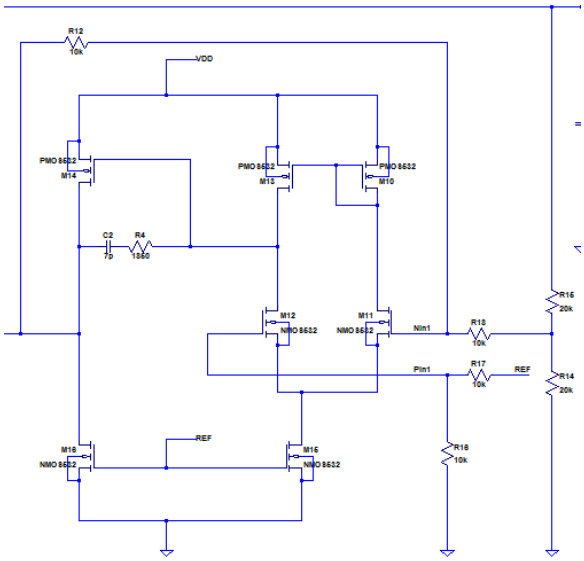

FIGURE 9. Close up of differential amplifier.

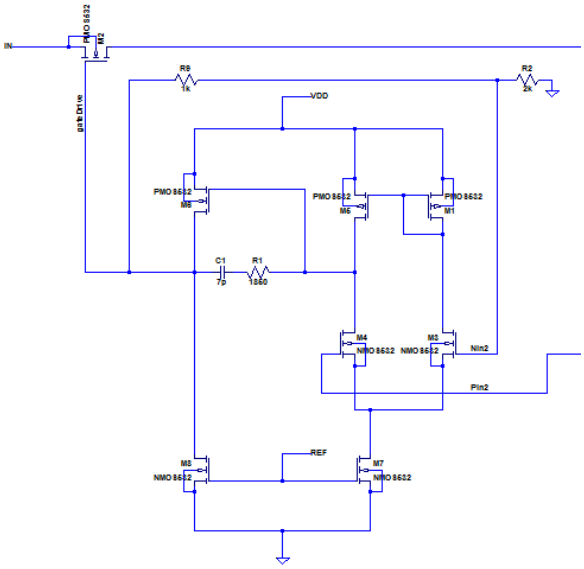

FIGURE 10. Close up of gain amplifier and gate driver.

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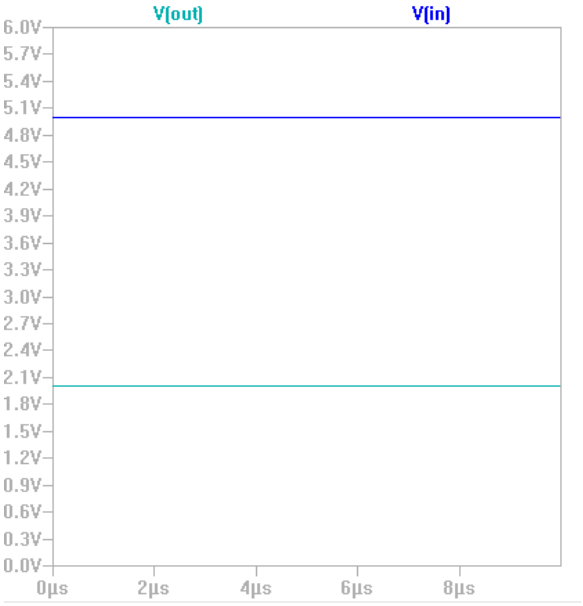


FIGURE 11. Steady State Output. Showing the amplifier tuned for $V_{out} = 2.00$.

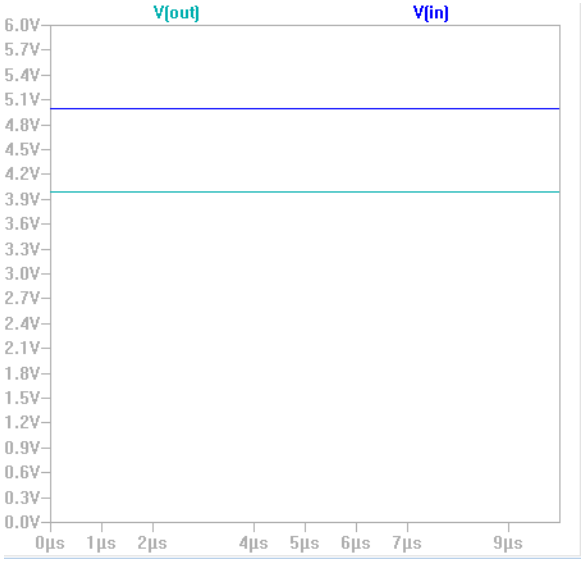


FIGURE 12. Steady State Output. Showing the amplifier tuned for $V_{out} = 4.00$.

5. SIMULATIONS

Both are accurate in steady state to within 2%.

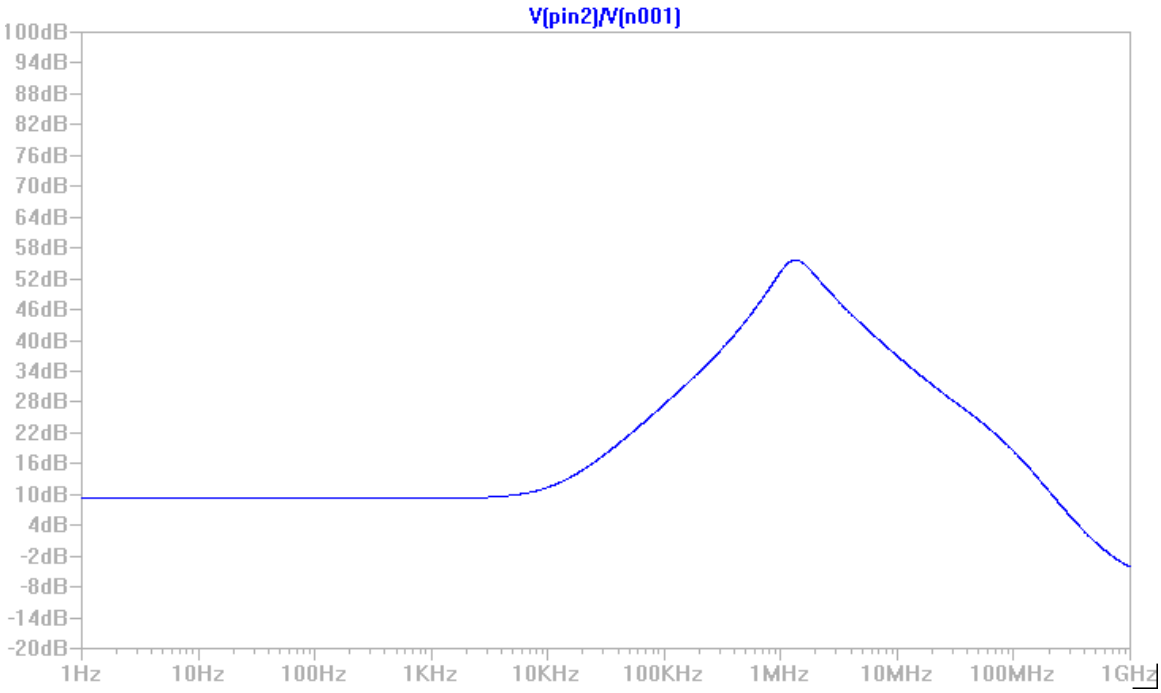


FIGURE 13. Loop Gain, $T(s)$.

The loop gain, $T(s)$ is between 10 dB and 60 dB. Note in my previous designs the loop gain was about -20 dB. I have greatly improved it here. This is very import because for a negative feedback voltage regulator we have:

- Voltage noise on the input is rejected in proportion to $\frac{1}{1+T(s)}$, which is ≈ 0 if $T(s)$ is very high.
- Voltage disturbances on the load are rejected in proportion to $\frac{1}{1+T(s)}$, which is ≈ 0 if $T(s)$ is very high.
- The reference voltage is followed in proportion to $\frac{T(s)}{1+T(s)}$, which is ≈ 1 if $T(s)$ is very high.

Therefore, since my loop gain, $T(s)$ is sufficiently high, voltage and current disturbances should be rejected well as they are multiplied by a very small number, and the reference voltage should be followed well as it is multiplied by something close to unity.

Note that the above is the idea case; several non-idealities as well as the fact my error amplifier cannot realize the entire negative range will hamper the affect of the feedback circuit to actively compensate.

The regulator maintains stability even with a sine wave of just under 1 V. The hypothetical noise rejection from the loop gain is not realized, but regulator maintains stability under load.

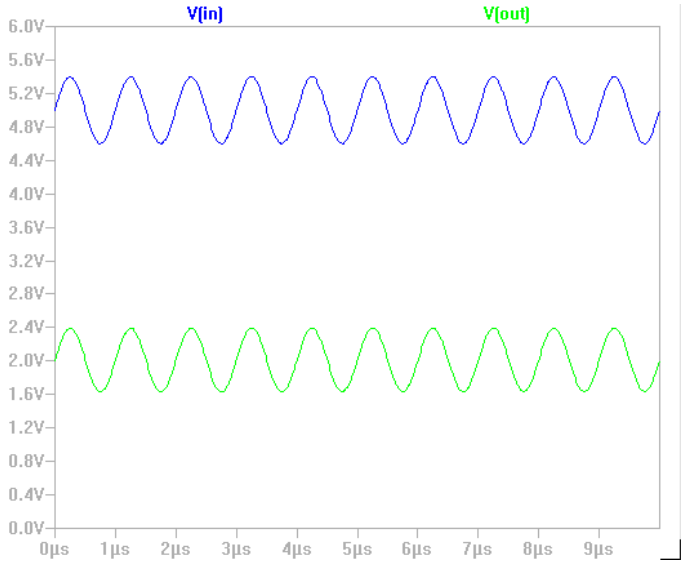


FIGURE 14. V_{out} vs V_{in} with a sine wave on the input.

Here is the steady state current draw and power loss across the control circuitry:

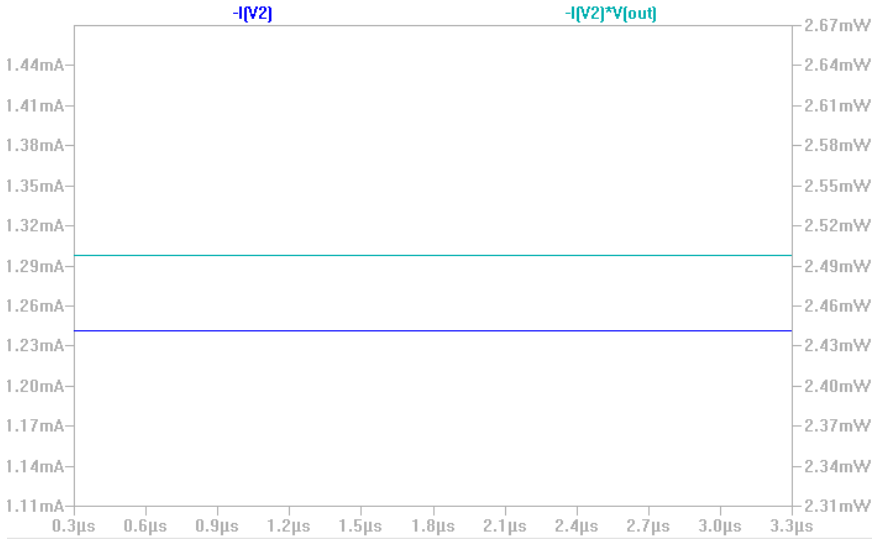
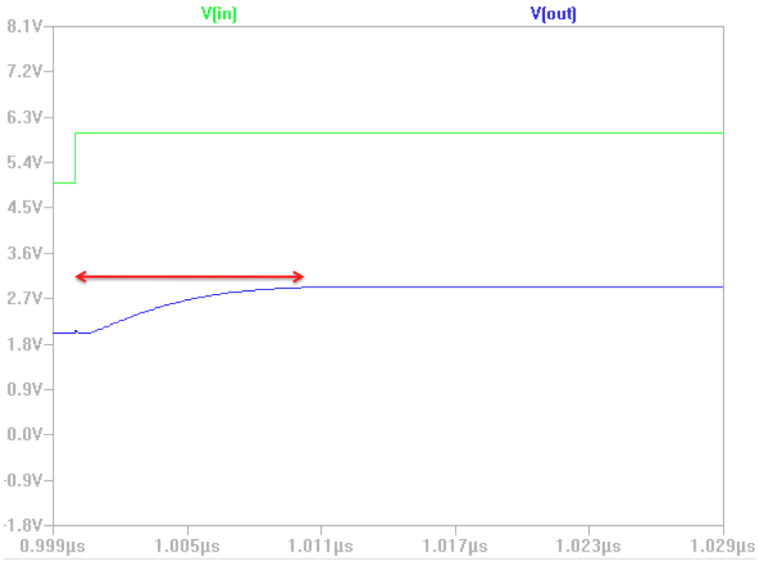


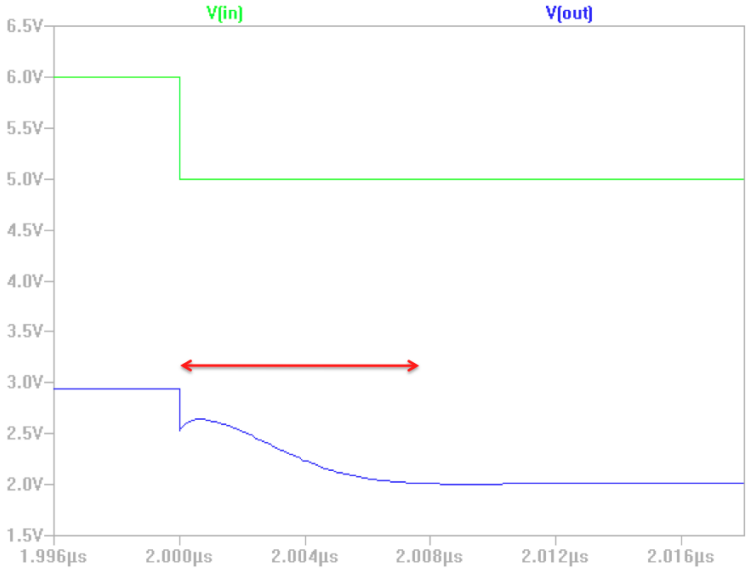
FIGURE 15. Steady state current draw and steady state power loss through control circuitry. The quiescent power loss is 2.5 mW.

The positive settling time is 10 nano seconds. The negative settling time is 8 nano seconds. From the linear section of the same graphs, I also get the slew rates:

$$\text{Positive slew rate} = \frac{100 \text{ Volts}}{\mu \text{ sec}}$$

$$\text{Negative slew rate} = \frac{166 \text{ Volts}}{\mu \text{ sec}}$$





Here is a temperature sweep of my regulator over a 35 degree Celsius range from 10 degrees Celcius to 45 degrees Celcius. It keeps the output without a 200 mV range of optimal. Outside of these temperatures performance is adversely affected.

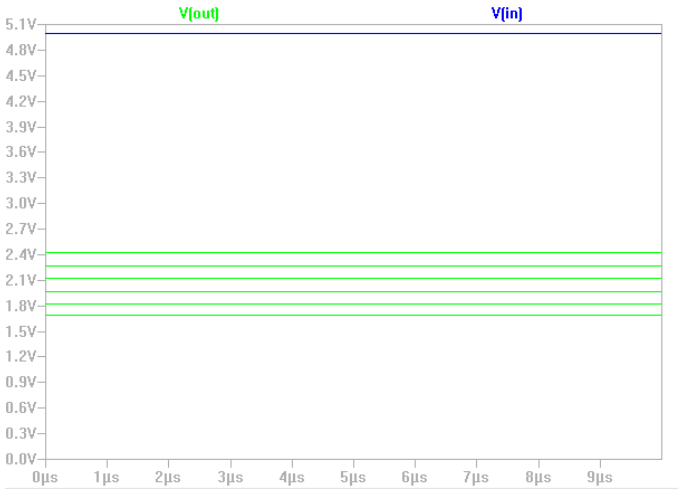
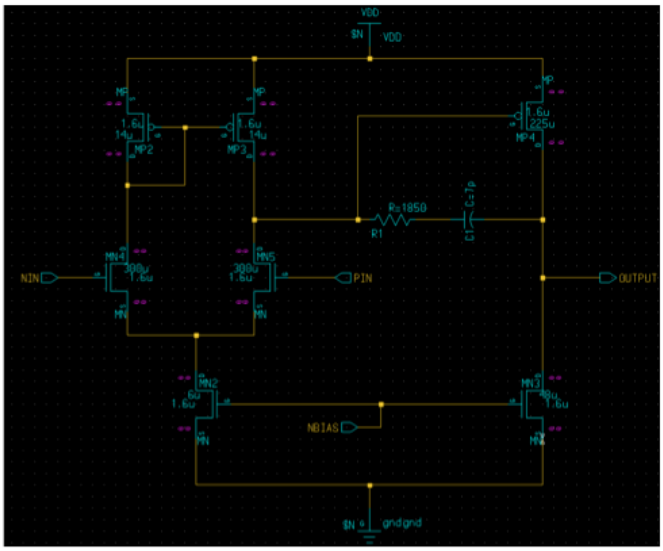
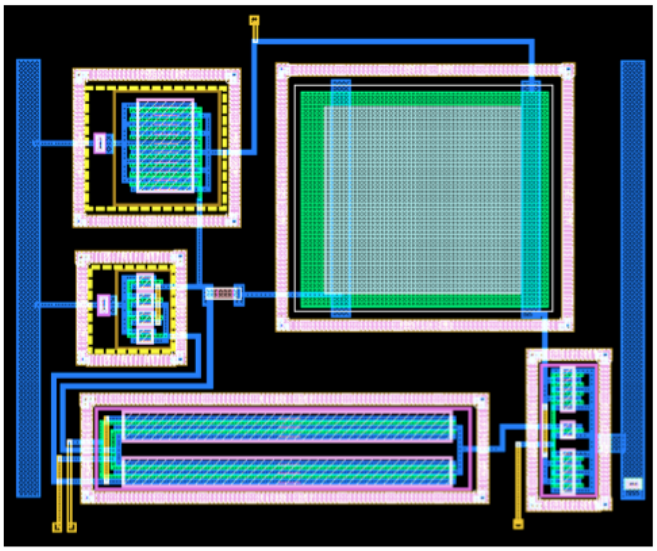


FIGURE 16. Regulator operation from 10 degrees C (top) to 45 degrees C (bottom) in 5 degree increments.

6. LAYOUT

I improved my op amp from homework 4 for this project. Here is my new op amp (the one I used above in simulations) as a schematic and also the layout for it.





For the rest of my design, I have several resistors that I need to common centroid. Here is my common centroid scheme:

Op Amps	Inverting Amplifier	Differential Amplifier	Feedback Divider
Common centroid already completed in homework 4	R1: 1 kΩ R2: 2 kΩ Unit Resistor for common centroid: 1 kΩ	R1: 10 kΩ R2: 10 kΩ R3: 10 kΩ R4: 10 kΩ Unit Resistor for common centroid: 5 kΩ	R1: 20 kΩ R2: 20 kΩ Unit Resistor for common centroid: 10 kΩ

FIGURE 17. My common centroid scheme.

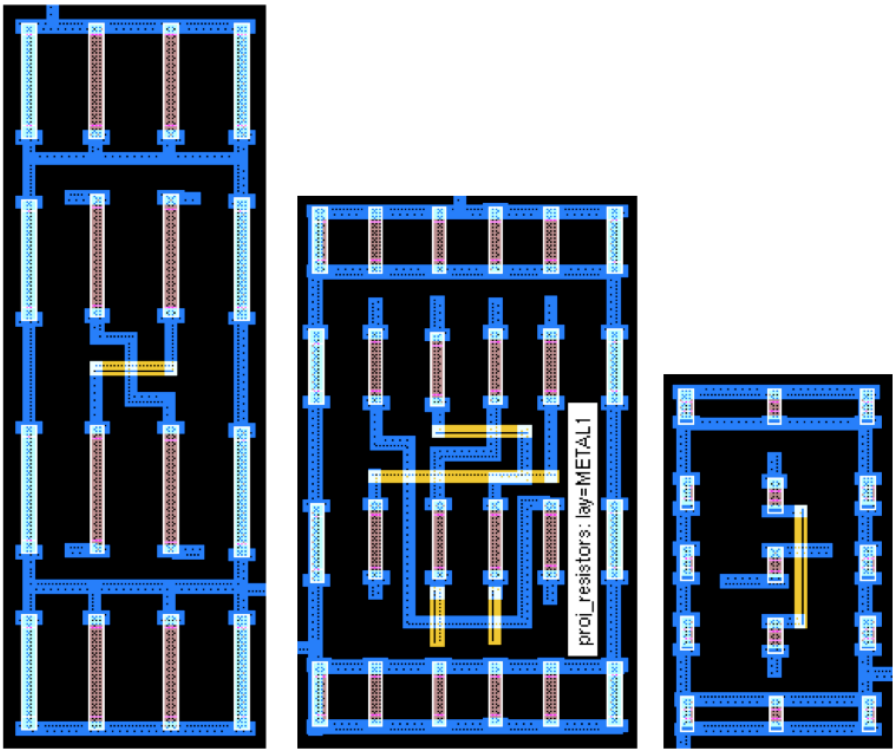


FIGURE 18. Common centroid resistors with dummy resistors added around the outside.

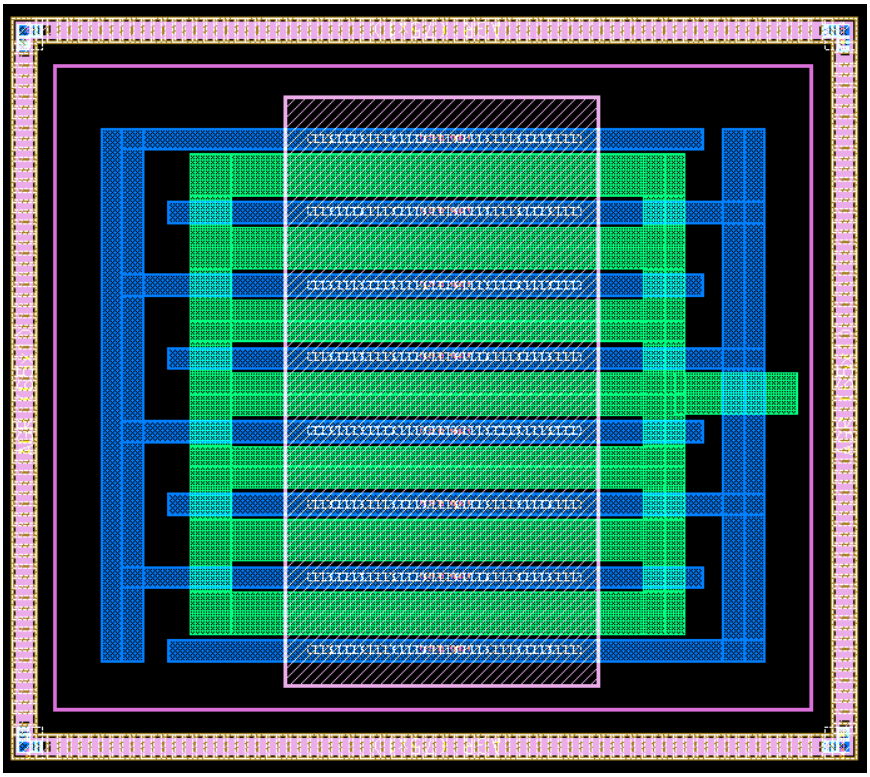


FIGURE 19. Power MOSFET. This is the pass element that controls power flow through the regulator.

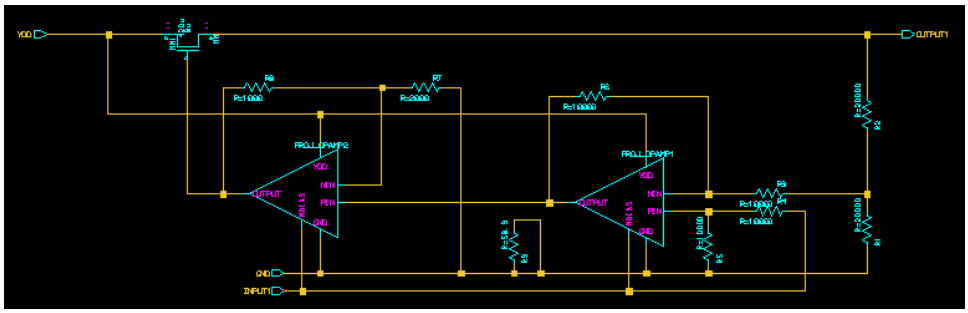


FIGURE 20. Final design in Design Architect.

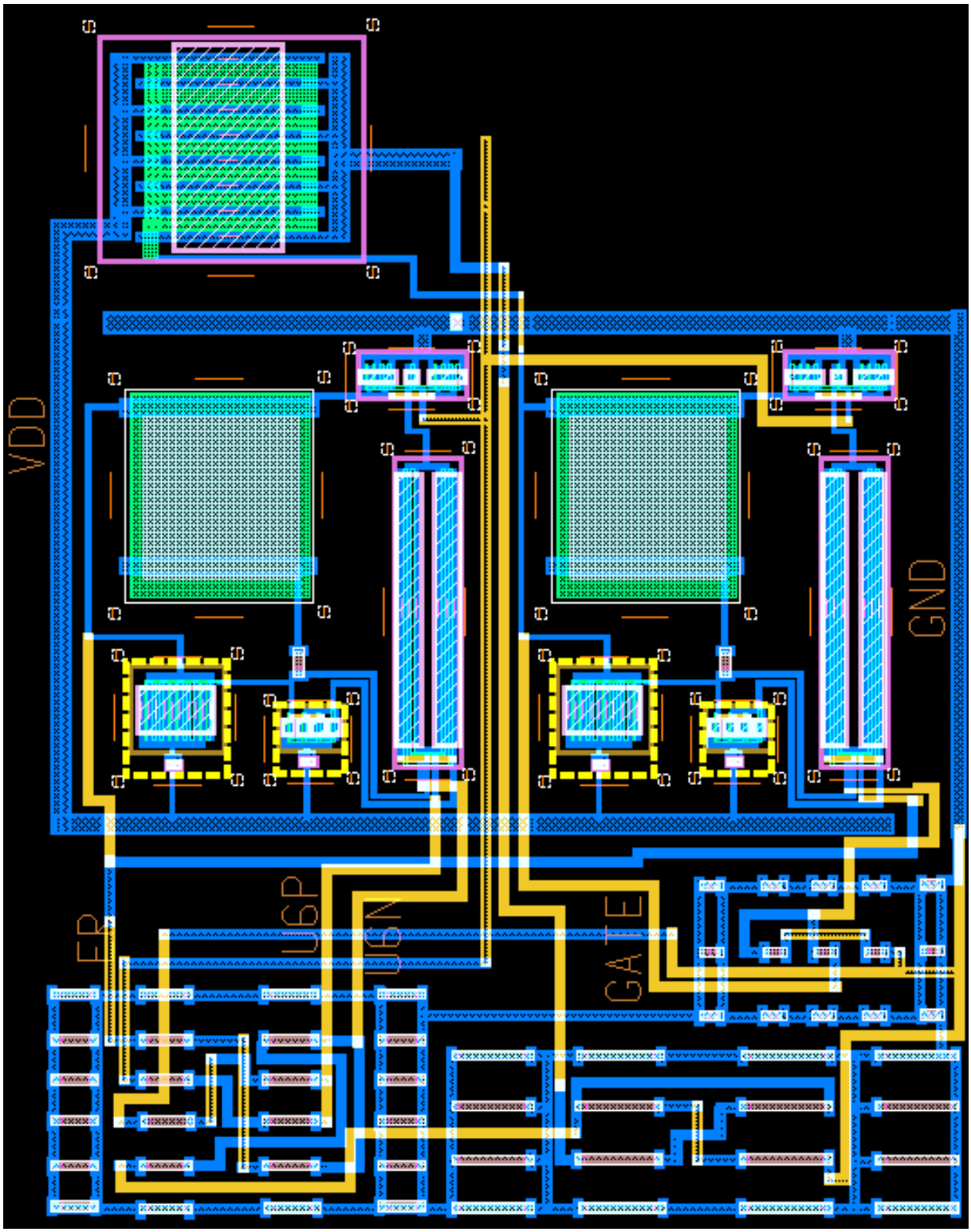


FIGURE 21. Everything put together.

```
Note: DRC completed. Total RuleChecks: 120; Total Results: 0; Total Original Geometries: 9521; CPU Time: 0.08, REAL Time: 0.113497.
```

```
*******************************************************************
                    OVERALL COMPARISON RESULTS
*******************************************************************

                    ###################
                    #                 #
                    #     CORRECT     #
                    #                 #
                    ###################

-------------------------------------------------------------------

INITIAL NUMBERS OF OBJECTS
--------------------------

                Layout     Source          Component Type
                ------     ------          --------------
Ports:               4          4
Nets:              146         18    *
Instances:          33          9    *    nn (3 pins)
                    26          6    *    pp (3 pins)
                     2          2         c (2 pins)
                    57         11    *    r (2 pins)
                ------     ------
Total Inst:        118         28

NUMBERS OF OBJECTS AFTER TRANSFORMATION
---------------------------------------

                Layout     Source          Component Type
                ------     ------          --------------
Ports:               4          4
Nets:               18         18
Instances:           9          9         nn (3 pins)
                     6          6         pp (3 pins)
                     2          2         c (2 pins)
                    11         11         r (2 pins)
                ------     ------
Total Inst:         28         28
```

FIGURE 22. The design is DRC (top) and LVS (bottom) clean.

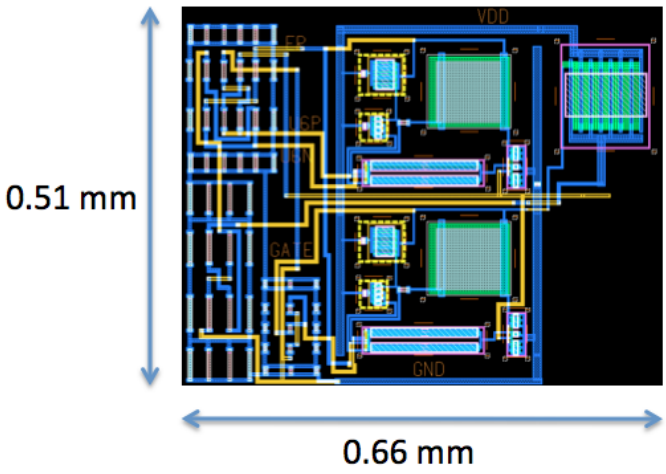


FIGURE 23. The area is 0.33 mm^2.

```
.OPTIONS ACCT POST ACOUT=0 ACCURATE=1 UNWRAP LIST

.OP
.TRAN 0.1u 1u
.GLOBAL VDD GND

V1 VDD GND DC 5.0
V2 2 GND DC 1.3
R1 3 GND 300
C1 3 GND 1p

.PRINT TRAN V(VDD) V(2) V(3)

.DC sweep V1 4.0 6.0 0.1

.subckt proj_v3 GND INPUT1 OUTPUT1 VDD
* devices:
m0 VDD 14 14 PMOS l=1.6u w=7u ad=18.2p as=18.9p pd=19.2u ps=19.4u nrd=0.142857
+ nrs=0.128571
m1 VDD 14 16 PMOS l=1.6u w=7u ad=19.6p as=18.9p pd=19.6u ps=19.4u nrd=0.142857
+ nrs=0.128571
m2 VDD 14 14 PMOS l=1.6u w=7u ad=19.6p as=18.9p pd=19.6u ps=19.4u nrd=0.142857
+ nrs=0.128571
m3 VDD 14 16 PMOS l=1.6u w=7u ad=19.6p as=18.9p pd=19.6u ps=19.4u nrd=0.142857
+ nrs=0.128571
m4 VDD 15 15 PMOS l=1.6u w=7u ad=18.2p as=18.9p pd=19.2u ps=19.4u nrd=0.142857
+ nrs=0.128571
m5 VDD 15 17 PMOS l=1.6u w=7u ad=19.6p as=18.9p pd=19.6u ps=19.4u nrd=0.142857
+ nrs=0.128571
m6 VDD 15 15 PMOS l=1.6u w=7u ad=19.6p as=18.9p pd=19.6u ps=19.4u nrd=0.142857
+ nrs=0.128571
m7 VDD 15 17 PMOS l=1.6u w=7u ad=19.6p as=18.9p pd=19.6u ps=19.4u nrd=0.142857
+ nrs=0.128571
m8 VDD 16 11 PMOS l=1.6u w=25u ad=33.75p as=67.5p pd=27.7u ps=55.4u nrd=0.04
+ nrs=0.036
m9 VDD 16 11 PMOS l=1.6u w=25u ad=33.75p as=32.5p pd=27.7u ps=27.6u nrd=0.04
+ nrs=0.04
m10 VDD 16 11 PMOS l=1.6u w=25u ad=33.75p as=32.5p pd=27.7u ps=27.6u nrd=0.04
+ nrs=0.036
m11 11 16 VDD PMOS l=1.6u w=25u ad=32.5p as=33.75p pd=27.6u ps=27.7u nrd=0.036
+ nrs=0.04
m12 11 16 VDD PMOS l=1.6u w=25u ad=32.5p as=33.75p pd=27.6u ps=27.7u nrd=0.04
+ nrs=0.04
m13 11 16 VDD PMOS l=1.6u w=25u ad=32.5p as=33.75p pd=27.6u ps=27.7u nrd=0.04
+ nrs=0.04
m14 VDD 16 11 PMOS l=1.6u w=25u ad=33.75p as=32.5p pd=27.7u ps=27.6u nrd=0.04
+ nrs=0.036
m15 VDD 16 11 PMOS l=1.6u w=25u ad=33.75p as=32.5p pd=27.7u ps=27.6u nrd=0.04
+ nrs=0.04
m16 VDD 16 11 PMOS l=1.6u w=25u ad=92.5p as=32.5p pd=57.4u ps=27.6u nrd=0.04
+ nrs=0.036
m17 VDD 17 10 PMOS l=1.6u w=25u ad=33.75p as=67.5p pd=27.7u ps=55.4u nrd=0.04
```

```
m21 10 17 VDD PMOS l=1.6u w=25u ad=32.5p as=33.75p pd=27.6u ps=27.7u nrd=0.04
+ nrs=0.04
m22 10 17 VDD PMOS l=1.6u w=25u ad=32.5p as=33.75p pd=27.6u ps=27.7u nrd=0.04
+ nrs=0.04
m23 VDD 17 10 PMOS l=1.6u w=25u ad=33.75p as=32.5p pd=27.7u ps=27.6u nrd=0.04
+ nrs=0.036
m24 VDD 17 10 PMOS l=1.6u w=25u ad=33.75p as=32.5p pd=27.7u ps=27.6u nrd=0.04
+ nrs=0.04
m25 VDD 17 10 PMOS l=1.6u w=25u ad=92.5p as=32.5p pd=57.4u ps=27.6u nrd=0.04
+ nrs=0.036
m26 35 13 14 NMOS l=1.6u w=150u ad=187.5p as=540p pd=152.5u ps=307.2u nrd=0.006
+ nrs=0.006
m27 16 10 35 NMOS l=1.6u w=150u ad=570p as=187.5p pd=307.6u ps=152.5u nrd=0.006
+ nrs=0.006
m28 35 10 16 NMOS l=1.6u w=150u ad=187.5p as=540p pd=152.5u ps=307.2u nrd=0.006
+ nrs=0.006
m29 14 13 35 NMOS l=1.6u w=150u ad=570p as=187.5p pd=307.6u ps=152.5u nrd=0.006
+ nrs=0.006
m30 36 9 15 NMOS l=1.6u w=150u ad=187.5p as=540p pd=152.5u ps=307.2u nrd=0.006
+ nrs=0.006
m31 17 6 36 NMOS l=1.6u w=150u ad=570p as=187.5p pd=307.6u ps=152.5u nrd=0.006
+ nrs=0.006
m32 36 6 17 NMOS l=1.6u w=150u ad=187.5p as=540p pd=152.5u ps=307.2u nrd=0.006
+ nrs=0.006
m33 15 9 36 NMOS l=1.6u w=150u ad=570p as=187.5p pd=307.6u ps=152.5u nrd=0.006
+ nrs=0.006
m34 11 INPUT1 GND NMOS l=1.6u w=6u ad=7.8p as=17.4p pd=8.6u ps=17.8u
+ nrd=0.166667 nrs=0.15
m35 GND INPUT1 11 NMOS l=1.6u w=6u ad=7.8p as=7.8p pd=8.6u ps=8.6u nrd=0.166667
+ nrs=0.15
m36 11 INPUT1 GND NMOS l=1.6u w=6u ad=7.8p as=7.8p pd=8.6u ps=8.6u nrd=0.166667
+ nrs=0.15
m37 11 INPUT1 GND NMOS l=1.6u w=6u ad=7.8p as=16.8p pd=8.6u ps=17.6u nrd=0.15
+ nrs=0.15
m38 GND INPUT1 35 NMOS l=1.6u w=6u ad=16.2p as=16.8p pd=17.4u ps=17.6u nrd=0.15
+ nrs=0.15
m39 11 INPUT1 GND NMOS l=1.6u w=6u ad=7.8p as=17.4p pd=8.6u ps=17.8u
+ nrd=0.166667 nrs=0.15
m40 GND INPUT1 11 NMOS l=1.6u w=6u ad=7.8p as=7.8p pd=8.6u ps=8.6u nrd=0.166667
+ nrs=0.15
m41 11 INPUT1 GND NMOS l=1.6u w=6u ad=7.8p as=7.8p pd=8.6u ps=8.6u nrd=0.166667
+ nrs=0.15
m42 11 INPUT1 GND NMOS l=1.6u w=6u ad=7.8p as=16.8p pd=8.6u ps=17.6u nrd=0.15
+ nrs=0.15
m43 10 INPUT1 GND NMOS l=1.6u w=6u ad=7.8p as=17.4p pd=8.6u ps=17.8u
+ nrd=0.166667 nrs=0.15
m44 GND INPUT1 10 NMOS l=1.6u w=6u ad=7.8p as=7.8p pd=8.6u ps=8.6u nrd=0.166667
+ nrs=0.15
m45 10 INPUT1 GND NMOS l=1.6u w=6u ad=7.8p as=7.8p pd=8.6u ps=8.6u nrd=0.166667
+ nrs=0.15
m46 10 INPUT1 GND NMOS l=1.6u w=6u ad=7.8p as=16.8p pd=8.6u ps=17.6u nrd=0.15
+ nrs=0.15
m47 GND INPUT1 36 NMOS l=1.6u w=6u ad=16.2p as=16.8p pd=17.4u ps=17.6u nrd=0.15
```

```
m48 10 INPUT1 GND NMOS l=1.6u w=6u ad=7.8p as=17.4p pd=8.6u ps=17.8u
+ nrd=0.166667 nrs=0.15
m49 GND INPUT1 10 NMOS l=1.6u w=6u ad=7.8p as=7.8p pd=8.6u ps=8.6u nrd=0.166667
+ nrs=0.15
m50 10 INPUT1 GND NMOS l=1.6u w=6u ad=7.8p as=7.8p pd=8.6u ps=8.6u nrd=0.166667
+ nrs=0.15
m51 10 INPUT1 GND NMOS l=1.6u w=6u ad=7.8p as=16.8p pd=8.6u ps=17.6u nrd=0.15
+ nrs=0.15
m52 VDD 11 OUTPUT1 NMOS l=8u w=60u ad=180p as=660p pd=66u ps=142u nrd=0.0433333
+ nrs=0.0433333
m53 OUTPUT1 11 VDD NMOS l=8u w=60u ad=180p as=180p pd=66u ps=66u nrd=0.0466667
+ nrs=0.045
m54 VDD 11 OUTPUT1 NMOS l=8u w=60u ad=180p as=180p pd=66u ps=66u nrd=0.04
+ nrs=0.0416667
m55 OUTPUT1 11 VDD NMOS l=8u w=60u ad=180p as=180p pd=66u ps=66u nrd=0.045
+ nrs=0.0483333
m56 VDD 11 OUTPUT1 NMOS l=8u w=60u ad=180p as=180p pd=66u ps=66u nrd=0.045
+ nrs=0.0433333
m57 OUTPUT1 11 VDD NMOS l=8u w=60u ad=180p as=180p pd=66u ps=66u nrd=0.0433333
+ nrs=0.0433333
m58 VDD 11 OUTPUT1 NMOS l=8u w=60u ad=594p as=180p pd=139.8u ps=66u
+ nrd=0.0433333 nrs=0.045
c59 11 45 7.04035p
c60 10 46 7.04035p
r61 GND GND 4.775k
r62 GND GND 5.2k
r63 GND GND 8.95k
r64 GND GND 10.225k
r65 GND GND 9.525k
r66 GND GND 8.95k
r67 GND GND 3.85k
r68 GND GND 3.85k
r69 GND GND 3.85k
r70 9 2 5.2k
r71 19 3 4.775k
r72 GND GND 3.85k
r73 GND GND 8.95k
r74 GND GND 8.95k
r75 GND 5 10.175k
r76 20 OUTPUT1 9.625k
r77 7 GND 4.775k
r78 GND GND 3.85k
r79 6 21 5.2k
r80 GND GND 3.85k
r81 GND GND 8.95k
r82 3 20 10.175k
r83 5 3 9.625k
r84 GND GND 8.95k
r85 GND GND 3.85k
r86 6 7 5.2k
r87 21 INPUT1 4.775k
r88 GND GND 3.85k
r89 GND GND 8.95k
```

```
**** voltage sources

subckt
element  0:v1        0:v2
 volts       5.0000      1.3000
 current    -1.9234m   -65.1629u
 power       9.6171m    84.7118u

    total voltage source power dissipation=    9.7018m       watts
```

FIGURE 24. Extracted Spice Netlist.

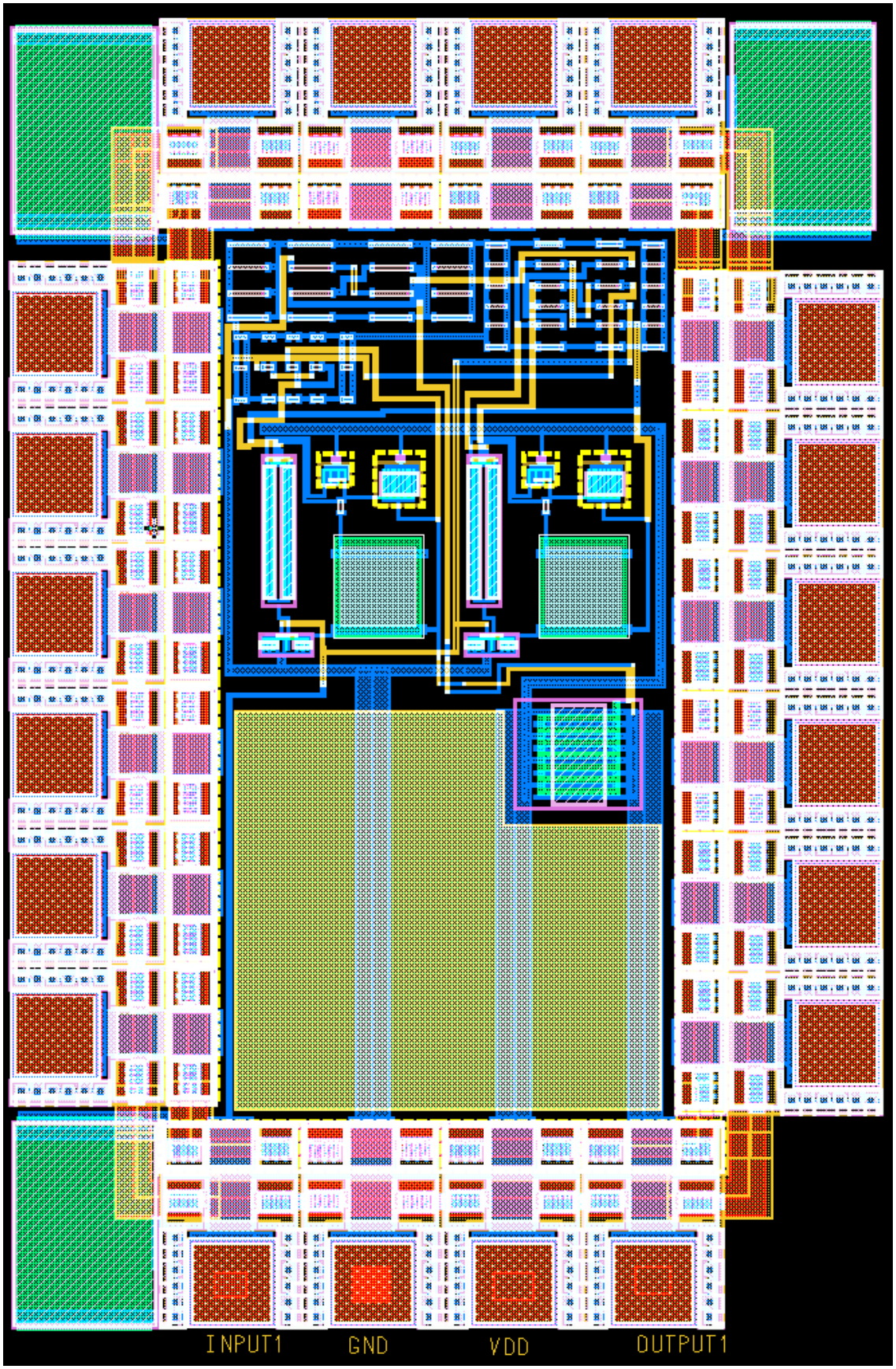


FIGURE 25. Layout inside template.