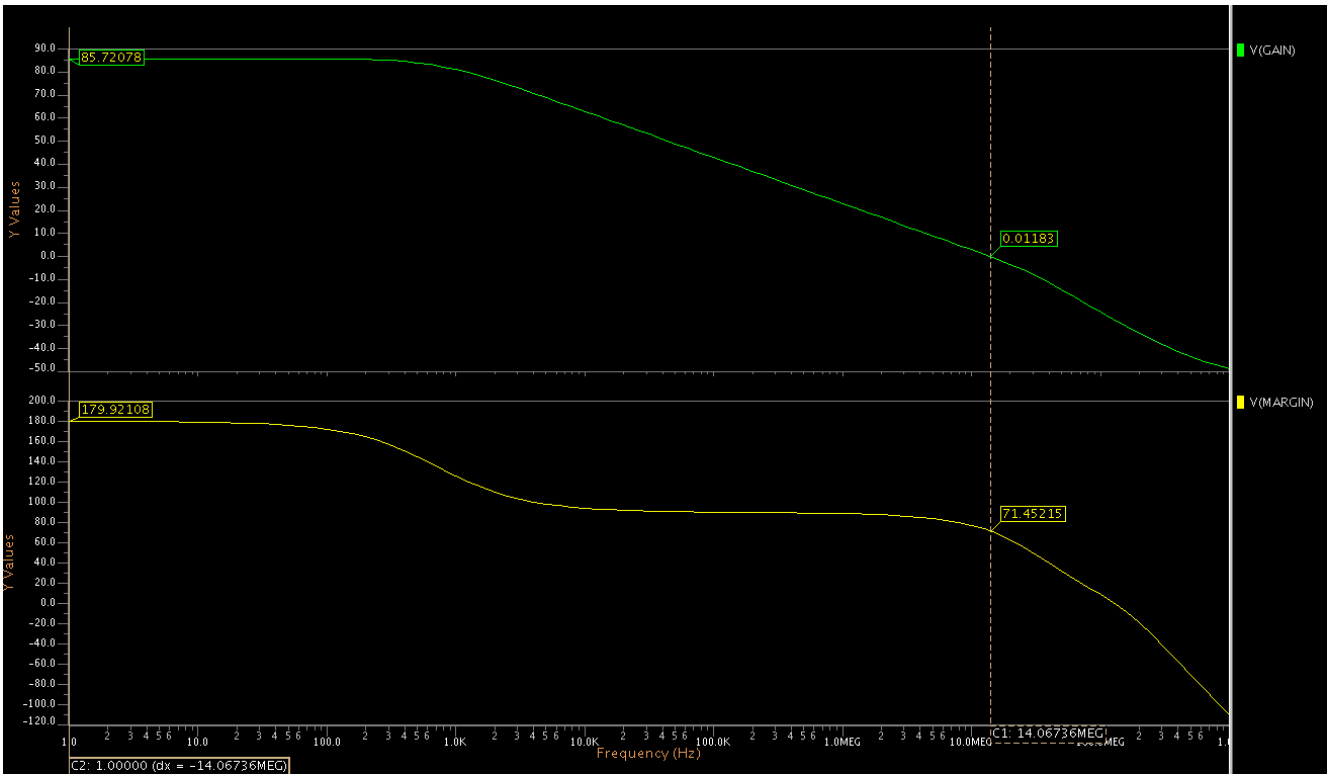
John O’Hollaren
ECE 532
Homework 4

Problem 1

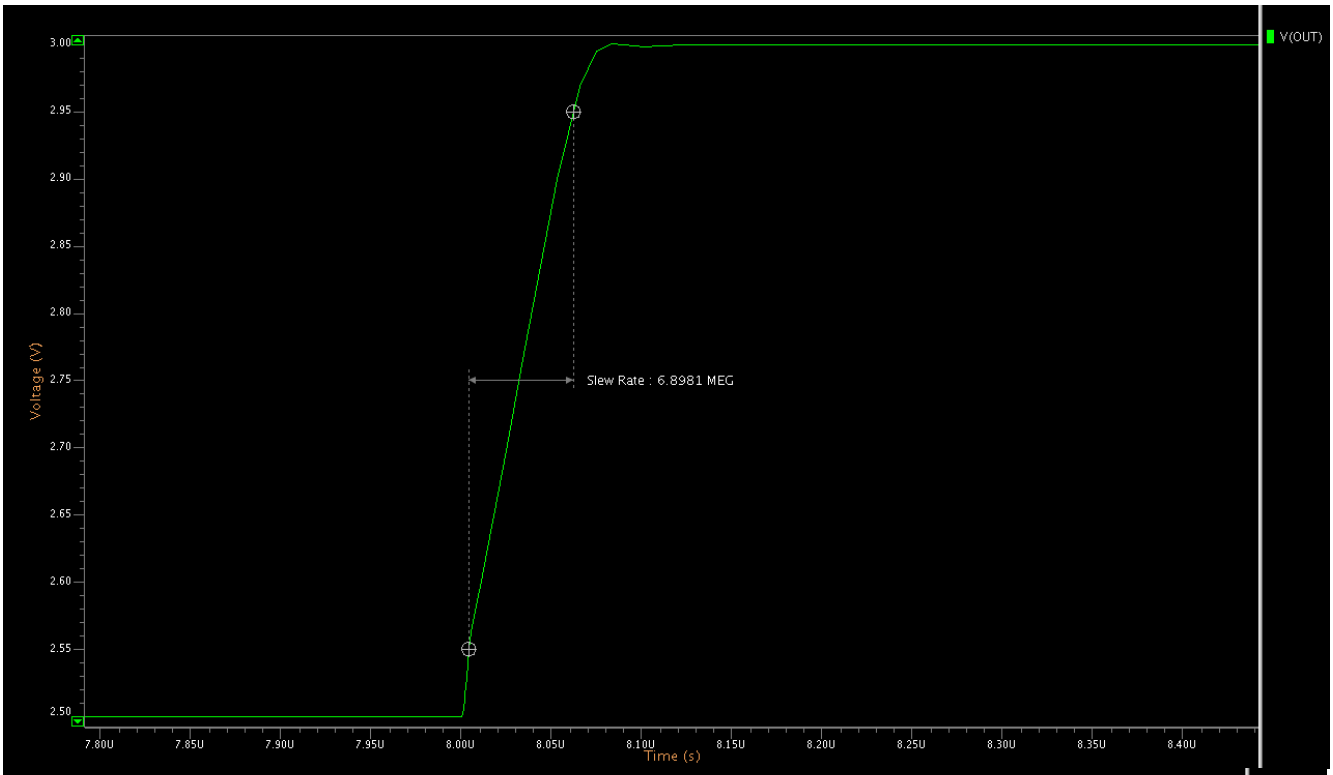
All my mosfets are in saturation:

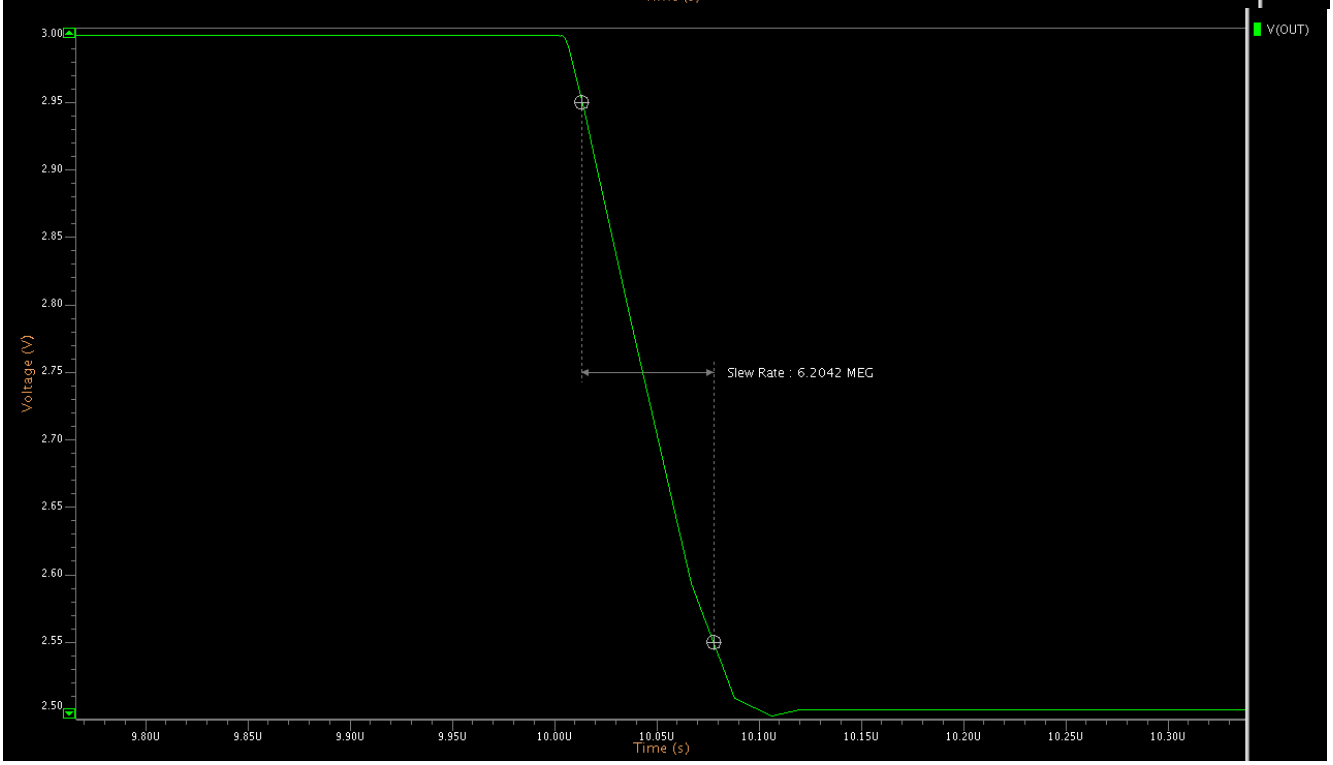
```
**** mosfets


subckt    xi_1744     xi_1744     xi_1744     xi_1744     xi_1744     xi_1744
element   1:mpout     1:mout_bia  1:m_pload1  1:m_pload2  1:mndif1    1:mndif2
model     0:pmos      0:nmos      0:pmos      0:pmos      0:nmos      0:nmos
region      Saturati    Saturati    Saturati    Saturati    Saturati    Saturati
 id       -546.9372u   546.9372u  -26.5047u   -26.5424u    26.5047u    26.5424u
 ibs         0.          0.          0.          0.          0.          0.
 ibd         0.          0.          0.          0.          0.          0.
 vgs        -1.3584      1.3000     -1.3244     -1.3244      1.1431      1.1433
 vds        -2.1002      2.8998     -1.3244     -1.3584      1.9189      1.8849
 vbs         0.          0.          0.          0.         -1.7567     -1.7567
 vth      -931.6127m   705.4324m  -934.3134m  -934.3073m    1.1040      1.1040
 vdsat    -381.0867m   464.7962m  -346.7111m  -346.7156m   68.2302m    68.2976m
 vod      -426.8324m   594.5676m  -390.0573m  -390.0633m   39.1125m    39.2726m
 beta        6.0715m     3.4999m   362.2543u   362.2547u   24.0693m    24.0691m
 gam eff   552.7278m   942.2269m   552.3894m   552.3894m    1.0496      1.0496
 gm          2.2819m     1.6677m   121.2678u   121.4370u   640.4451u   641.4333u
 gds        15.2761u     6.5678u     1.1206u     1.0948u     2.3504u     2.3602u
 gmb       700.3670u    540.6890u    37.2317u    37.2832u    99.9588u   100.1212u
 cdtot     330.2508f     58.6748f    23.6065f    23.4739f   377.8985f   378.4989f
 cgtot     728.2836f    139.7924f    44.6302f    44.6295f   787.9299f   788.4404f
 cstot     939.5933f    165.5626f    58.1177f    58.1178f   803.0338f   803.4611f
 cbtot     958.7790f    182.9262f    64.6104f    64.4780f   927.4508f   928.0655f
 cgs       631.7747f    106.9759f    37.6330f    37.6330f   565.5406f   566.1348f
 cgd        50.3697f     8.9090f     2.9852f     2.9848f    61.5135f    61.5133f


subckt    xi_1744
element   1:m_tailbi
model     0:nmos
region      Saturati
 id        53.0470u
 ibs        0.
 ibd        0.
 vgs        1.3000
 vds        1.7567
 vbs        0.
 vth      756.9269m
 vdsat    407.1742m
 vod      543.0731m
 beta     432.0001u
 gam eff  943.3232m
 gm       180.6818u
 gds        1.0457u
 gmb       60.3357u
 cdtot      9.7126f
 cgtot     19.1217f
 cstot     23.0314f
 cbtot     28.5552f
 cgs       14.0851f
 cgd        1.1095f
```

```
*HSpice File
*.OPTIONS ACCT POST PROBE
.OPTIONS ACCT POST ACOUT=0 DCON=1 ACCURATE=1 UNWRAP LIST
.OP
*.TRAN 200n 2.5m sweep  BIAS .9v 1.7v .1v
*.TRAN 1u .3m
*.TRAN 1u 3ms  sweep biasvalue 0 1.8 .1
*.TRAN 1u 50ms sweep cvalue 0 4p .5p
*.TRAN .001u .001ms   sweep sfreq 5e6 20e6 2e6
*.TRAN 10n 200us

* Do this sweep so we can see right where we want to be biased
* This will be helpful for AC Analysis, could use this for ACGND etc?
*.DC SWEEP biasvalue  1.3995v 1.4005v .00001v

*.DC sweep bias .5v 2.0v .25v width .5u 50u .4u
*.DC sweep vbias .5v 2.0v .25v
*.DC
    .GLOBAL vdd gnd
.PARAM VDD=5.0

.AC  dec 10 1 1GHz
**.AC  dec 10 1 1GHz sweep offset 1.5 3.5 .1
**.AC  dec 10 1 1GHz sweep cvalue 0 2.0p .1p

* Use this for AC Analysis
* builds off ACGND
Vp1 INP ACGND   AC=1e-4

**VSRC INP gnd 1.25 AC 1 sin(.0001 0 1)
*vp1 INP 0 sin (.9 .0005 3000)
*vinp INP 0  sin (2.2  .130 sfreq)
*vinp INP 0 .9v
*vinn INN 0 2.9v
*vbias outbias 0  sin (offset .4 1e3)
*vbias outbias 0  sin (3.8 .01 5e4)
*vinp P1 0  sin (1.25 .001 1000)
*vbias outbias 0 outbias
 *VPOS INP 0 2.0v

* for AC analysis we have to set up these inputs

*vp1 INP 0 biasvalue
*vinn N_1237 0 1.4
*Small Amp SLew Test
*vinn INP gnd  pulse 2.499 2.501 2n .1n .1n 1000n 2000n
*Larger Amp SLew Test
*vinp INP 0 0  pulse 2.49 2.51 2n .1n .1n 1600n 3200n

* this is for measuring slew rate and settling time
* comment this out for AC, only for DC
*Vp1 INP 0 0  pulse 2.5 3.0 2n 2n 1n 1600n 3200n

*vinp INP 0 0  pulse 2.499 2.501 2n 0.1n 0.1n 40u 80u
*vinp INP 0 0  pulse 2.1 2.9 2n 0.1n 0.1n 40u 80u
*Vp1 INP 0 0  pulse .9070v .893v 2n 0.1n 0.1n 40u 80u
*Vinp INP 0 0  pulse 1.v 1.8v 2n 0.1n 0.1n 5u 10u
*vinp INN 0 .9v
*vinp P1 0 0  pulse 2.3 2.7 2n 0.1n 0.1n 40u 80u

*Input Range Test (INN = INP with slow ramp; open loop))
*vinp INP 0 0  pulse 1.3 1.4 2n 30u 30u 2u 84u
*vinn INN 0 0  pulse 1.2 3.5  2n 30u 30u 2u 84u

* Power supply definitions
vdd vdd gnd 5.0v
vacgnd ACGND gnd 2.9v
*vgainctln gainctln  gnd 0
*vgainctlp gainctlp  gnd vdd
*vbias bias 0 1.25
vnbias NBIAS 0 1.3

* these are floating nodes used for debugging
*vpc PC 0  3.0
*vnc NC 0 2.7

.subckt HIGHBWN  OUTPUT NIN NBIAS PIN VDD GROUND

    C2 N$653 OUTPUT  C=7p
    R3 N$229 N$653  R=1850
    MPOUT OUTPUT N$229 VDD VDD PMOS L=1.6e-6 W=225e-6 M=1
    MOUT_BIAS OUTPUT NBIAS GROUND GROUND NMOS L=1.6e-6 W=48e-
6 M=1

            * load devices / resistors for diff pair
    M_PLOAD1 N$239 N$239 VDD VDD PMOS L=1.6e-6 W=14e-6 M=1
    M_PLOAD2 N$229 N$239 VDD VDD PMOS L=1.6e-6 W=14e-6 M=1

    * this is the diff pair
    MNDIF1 N$239 NIN N$228 GROUND NMOS L=1.6e-6 W=300e-6 M=1
    MNDIF2 N$229 PIN N$228 GROUND NMOS L=1.6e-6 W=300e-6 M=1

    * tail current
    M_TAILBIAS N$228 NBIAS GROUND GROUND NMOS L=1.6e-6 W=6e-6
M=1

.ends HIGHBWN

* spice command to initialize a node, this is an intial condition
* might need to use this
*.IC v(N_1237) 1.4

* ACGND BIAS GAINCTLN GAINCTLP OUTPUT P1
XI_1744  OUT INN NBIAS INP VDD GND  HIGHBWN
*.subckt BOOKAMPPIP GND INN INP OUT pipbias VDD
*XI_1744  GND  INN INP OUTPUT BIAS VDD BOOKAMPPIP
* GAIN 4 or 12 dB is 45000
*RFeed INN OUT 45000

* for open loop gain we comment these out

* gain should be 2 with this setup, these are resistors around the subcircuit
*RFeed INN OUT 20000  ROpen INN OUT 100G COpen INN GND 1u
* ACGND is a bias at 2.9V. this is the common mode center. AC GND
* could be at 0 v, but that would load down output, we want it at common
mode
* if ACGND is at 0V, we would get more offset
*Rgnd INN ACGND 20000
*Rgnd INN GND 20000
*MXBIAS VDD BIAS BIAS VDD PMOS L=4u W=30u
*RBIAS BIAS GND 850k
**XI_1744  BIAS OUTPUT INP OUTPUT opampip
**MXM4 N_1235 GAINCTLP N_1237 VDD PMOS L=.7u W=5u
**RXR4 OUTPUT N_1236 133333
***RXRS N_1236 N_1235 1
**RXRS OUTPUT N_1237 1386666
*RXRS OUTPUT N_1237 1386666
**RXRS OUTPUT N_1237 700000
***MXM1 N_1235 GAINCTLN N_1236 gnd NMOS L=.7u W=50u
**RXR2 N_1235 N_1237 133333
*RXR3 N_1237 ACGND  7923
*Cload OUTPUT gnd 3.5p

* small load capacitor
Cload OUT GND 20p

.probe ac vdb(OUT) vp(OUT)
.probe ac gain=par('20*log10(vm(OUT)/vm(INP))')
.probe ac phase=par('vp(OUT)-vp(INP,INN)')
.probe ac margin=par('vp(OUT)-vp(INP,INN)+180')

* .INCLUDE '/ece/digital/share/saturn/hspice/opampjim/pip/pip.sp.pex'
.INCLUDE 'spice_models/ami.5um.typmodels'

.END
```



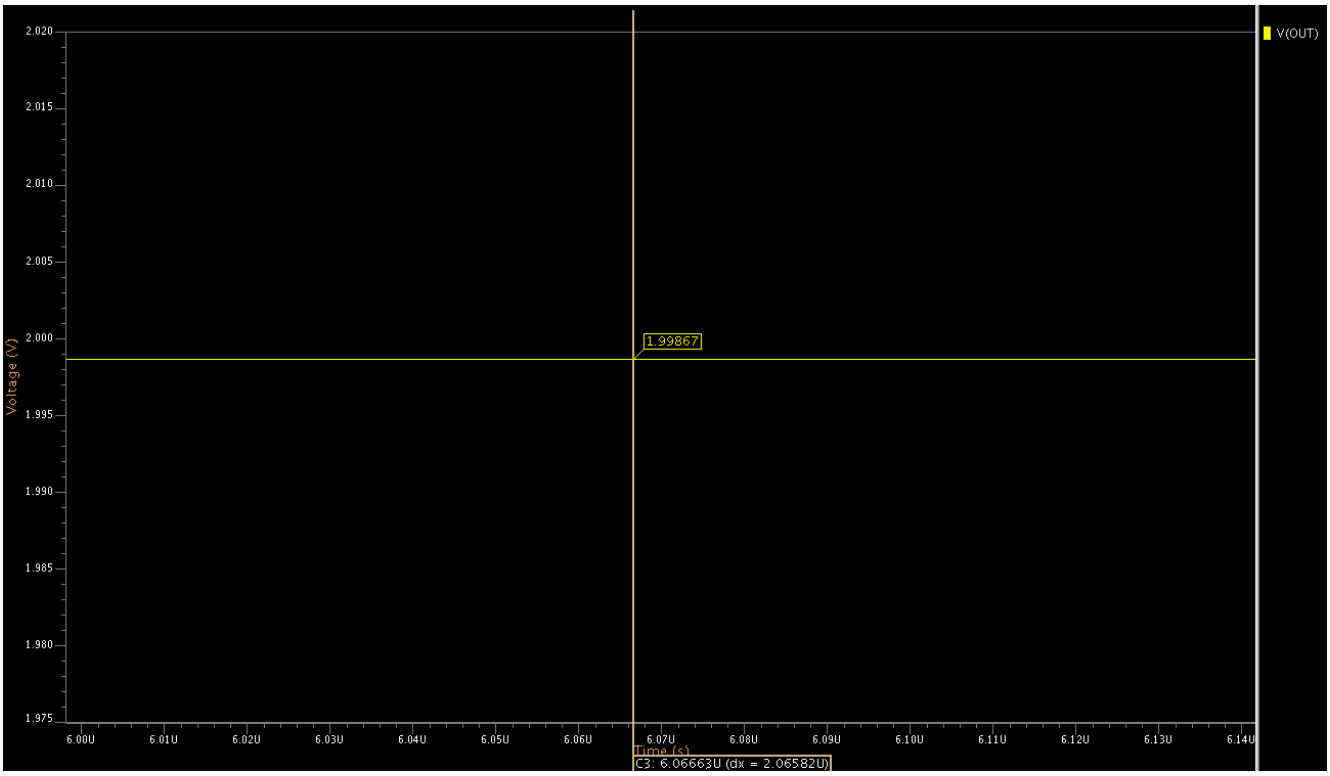
85 dB gain
14 MHz BW
71 degrees Phase Margin

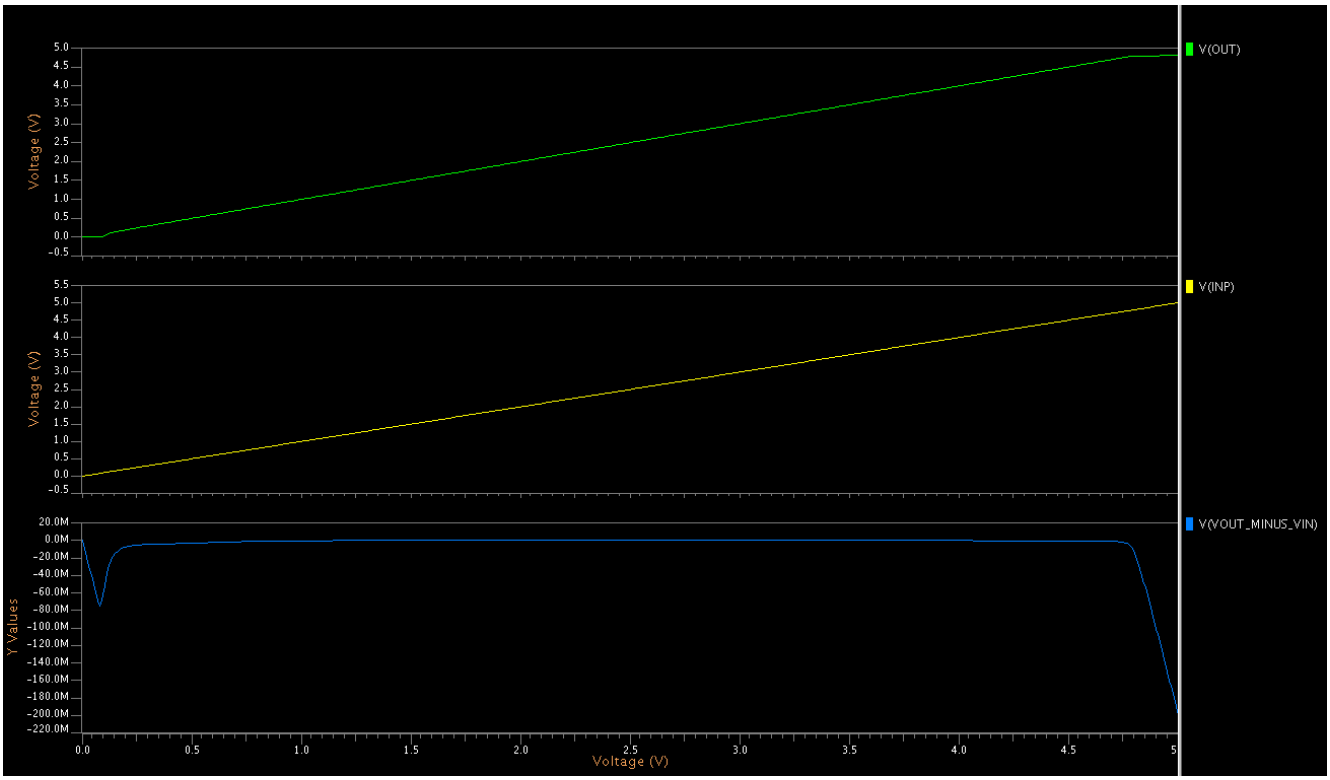




Positive Slew: 6.9 V / us
Negative Slew: 6.2 V / us

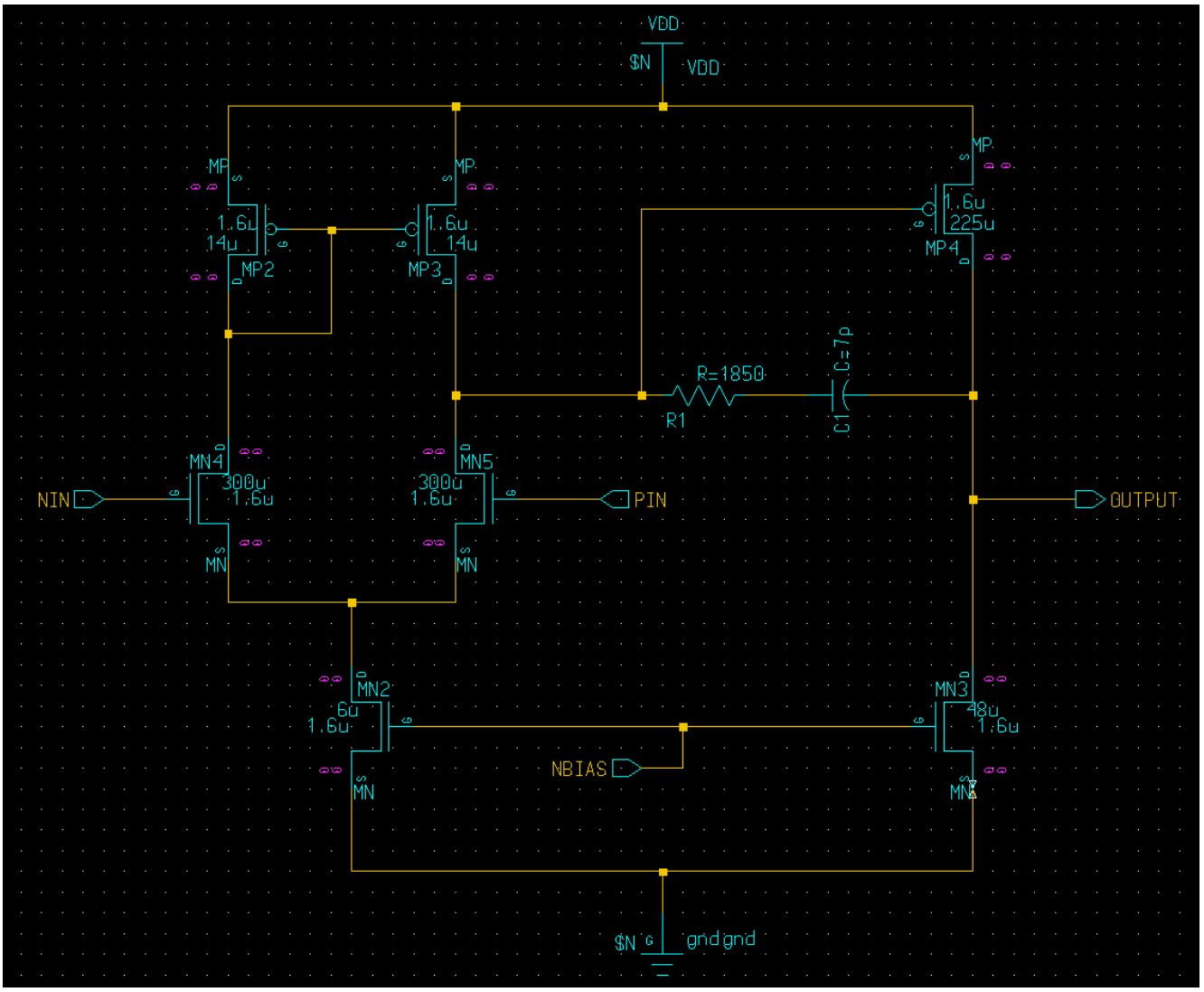
I used the typical ideal models, so offset is almost non existent and op amp is very accurate, for example here is the output for a non-inverting gain 2 amplifier to double a 1V input, the offset is only 1.4 mV

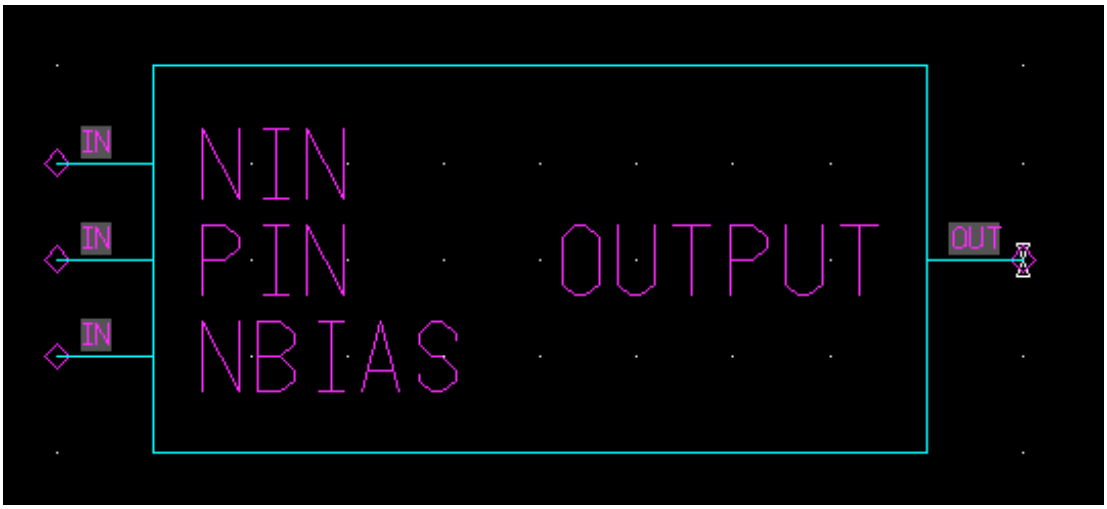




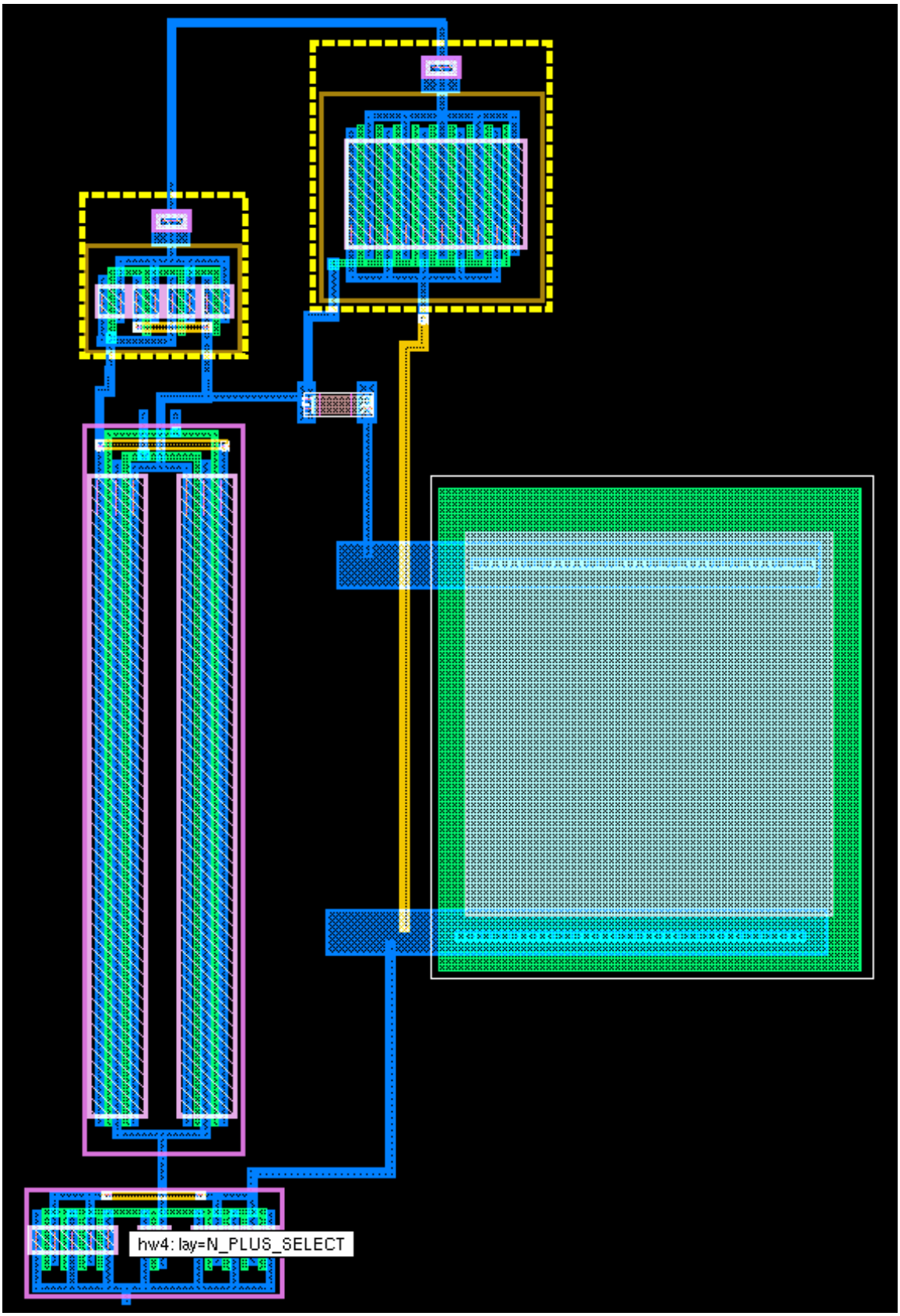
Common mode range is approximately 0.5 to 4.5 V

Here is my circuit schematic with all W/L ratios and component values:

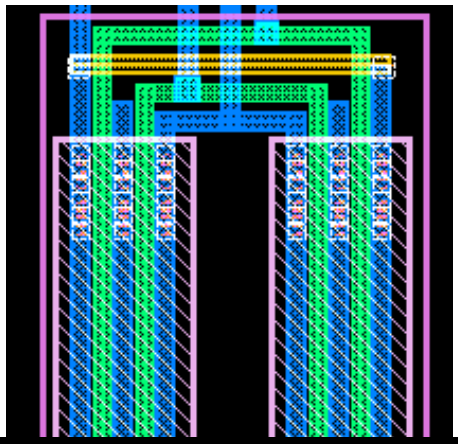


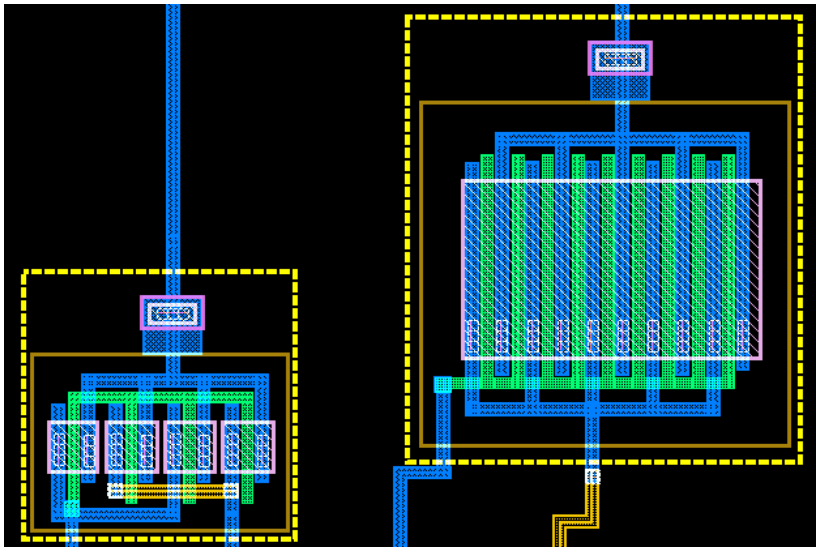


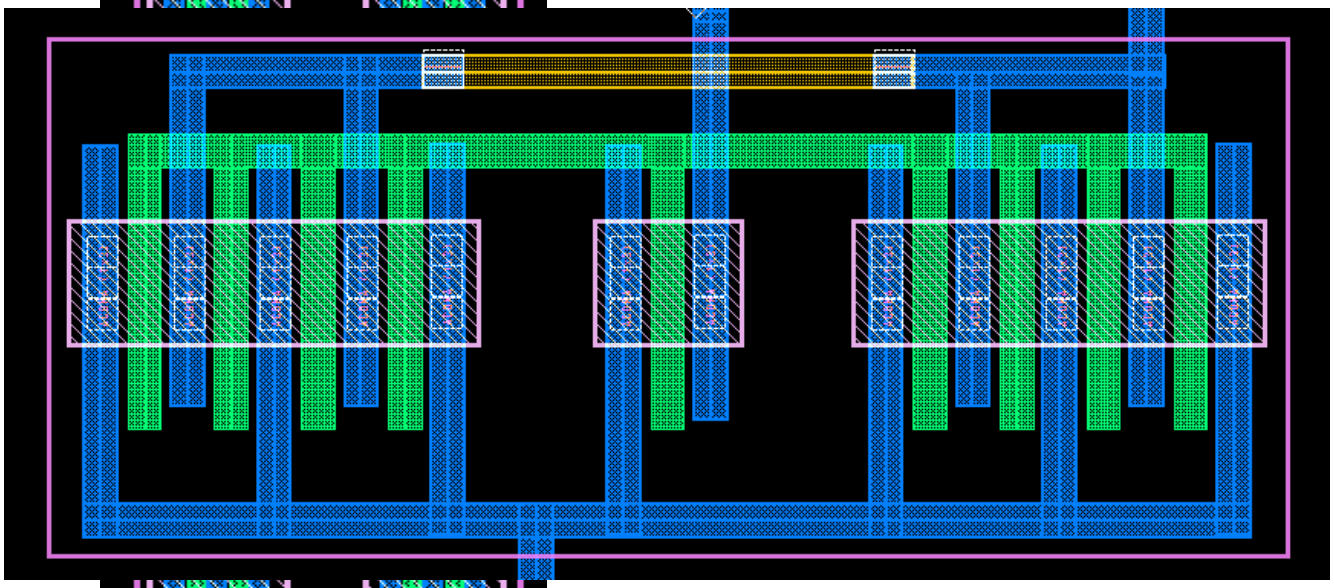
Here is my layout:

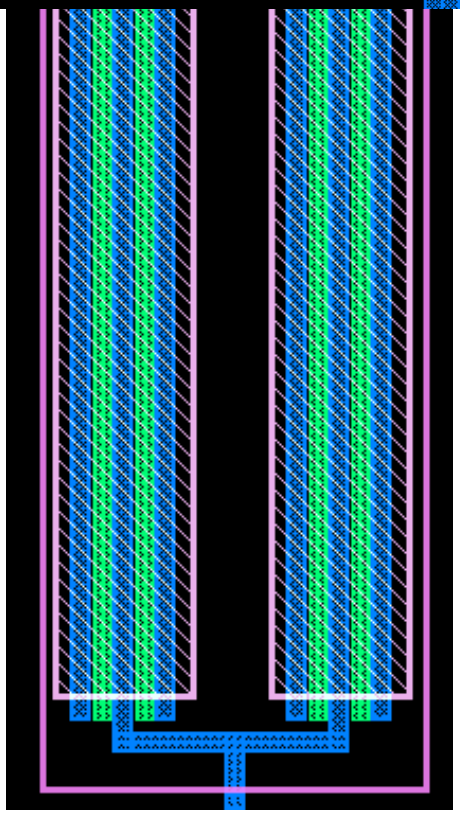


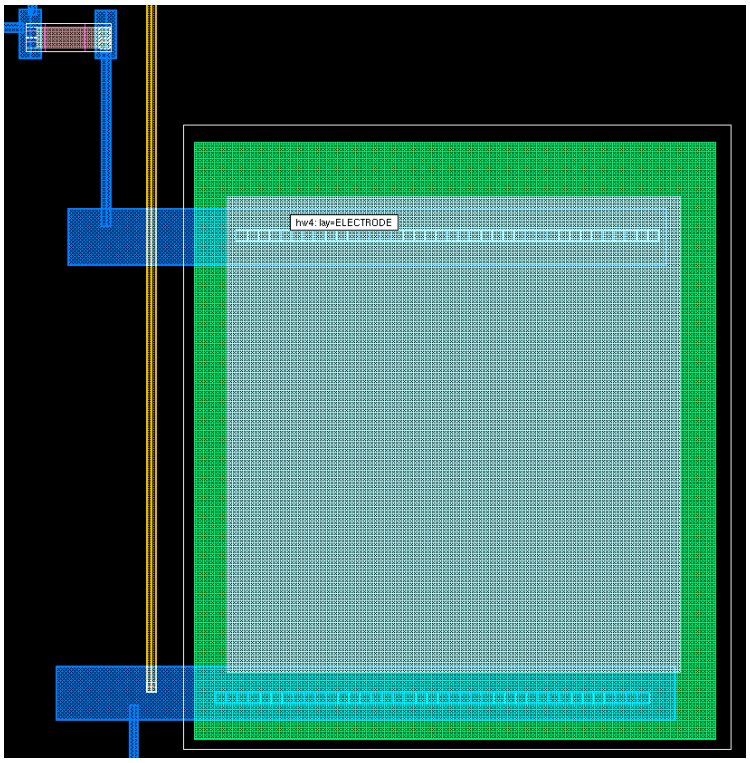
Here are close ups:







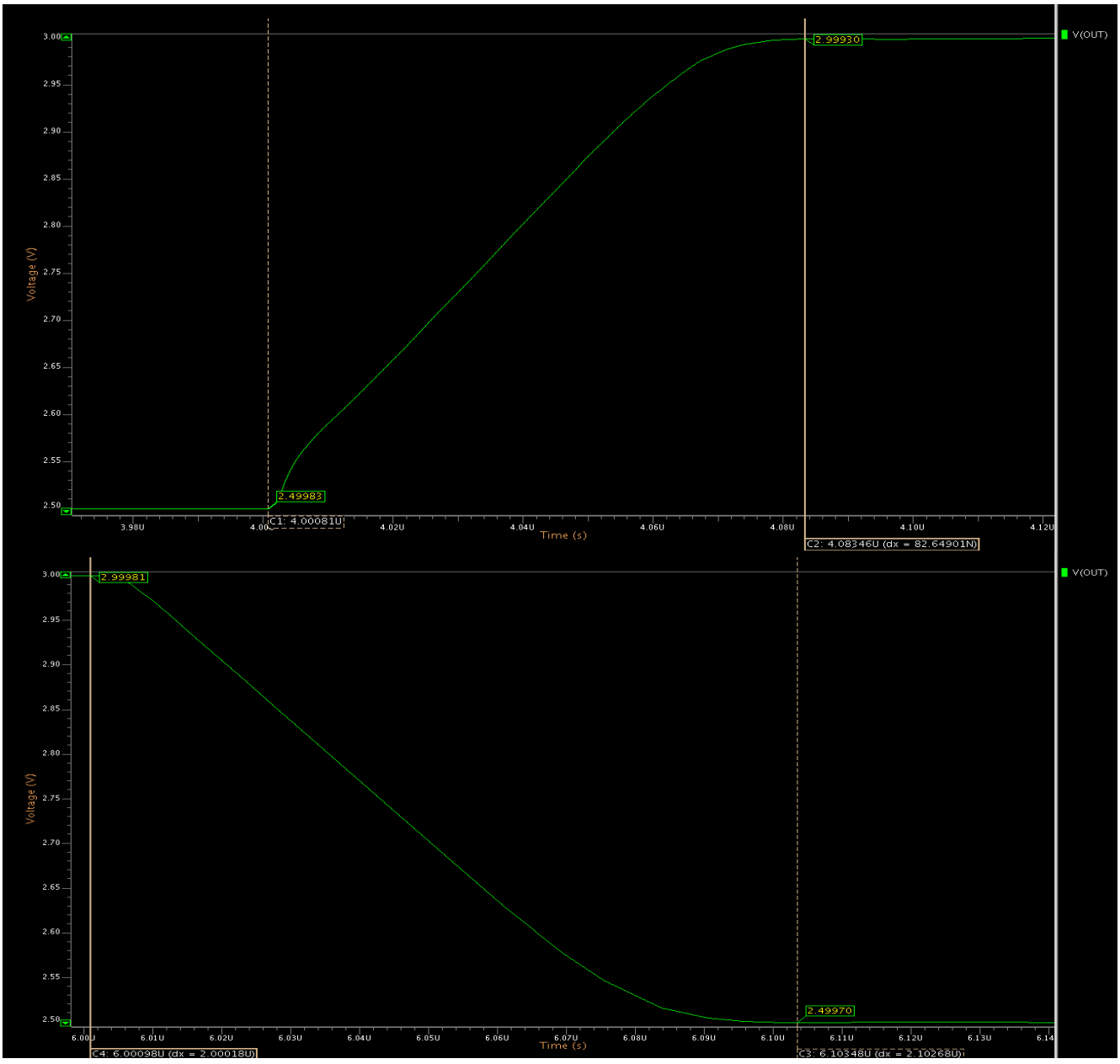




```
                ################################################
                ##                                            ##
                ##        C A L I B R E   S Y S T E M         ##
                ##                                            ##
                ##            L V S   R E P O R T             ##
                ##                                            ##
                ################################################


REPORT FILE NAME:         /home/software/ece532/jpo4/mentor/lvs.rep
LAYOUT NAME:              $JPO4LAY/hw4
SOURCE NAME:              $JPO4NETS/hw4/viewictrace
RULE FILE:                /opt/digital/share/mgc_hep/technology/ic/ami.5um.rules.3term
LVS MODE:                 Mask
RULE FILE NAME:           /opt/digital/share/mgc_hep/technology/ic/ami.5um.rules.3term
CREATION TIME:            Tue Apr  2 23:37:58 2013
CURRENT DIRECTORY:        /home/software/ece532/jpo4/mentor
USER NAME:                jpo4

*****************************************************************************************************************
                          OVERALL COMPARISON RESULTS
*****************************************************************************************************************

                     #       ###################       _   _
                    #        #                 #       *   *
                  #   #      #     CORRECT     #         |
                   # #       #                 #       \___/
                    #        ###################


-----------------------------------------------------------------------------------------------------------------

INITIAL NUMBERS OF OBJECTS
--------------------------

                Layout    Source          Component Type
                ------    ------          --------------
 Ports:              6         6

 Nets:              49        10    *

 Instances:         13         4    *    mn (3 pins)
                    13         3    *    mp (3 pins)
                     1         1         c (2 pins)
                     1         1         r (2 pins)
                ------    ------
 Total Inst:        28         9


NUMBERS OF OBJECTS AFTER TRANSFORMATION
---------------------------------------

                Layout    Source          Component Type
                ------    ------          --------------
 Ports:              6         6

 Nets:              10        10

 Instances:          4         4         mn (3 pins)
                     3         3         mp (3 pins)
                     1         1         c (2 pins)
                     1         1         r (2 pins)
                ------    ------
 Total Inst:         9         9


       * = Number of objects in layout different from number in source.
```

Number 2

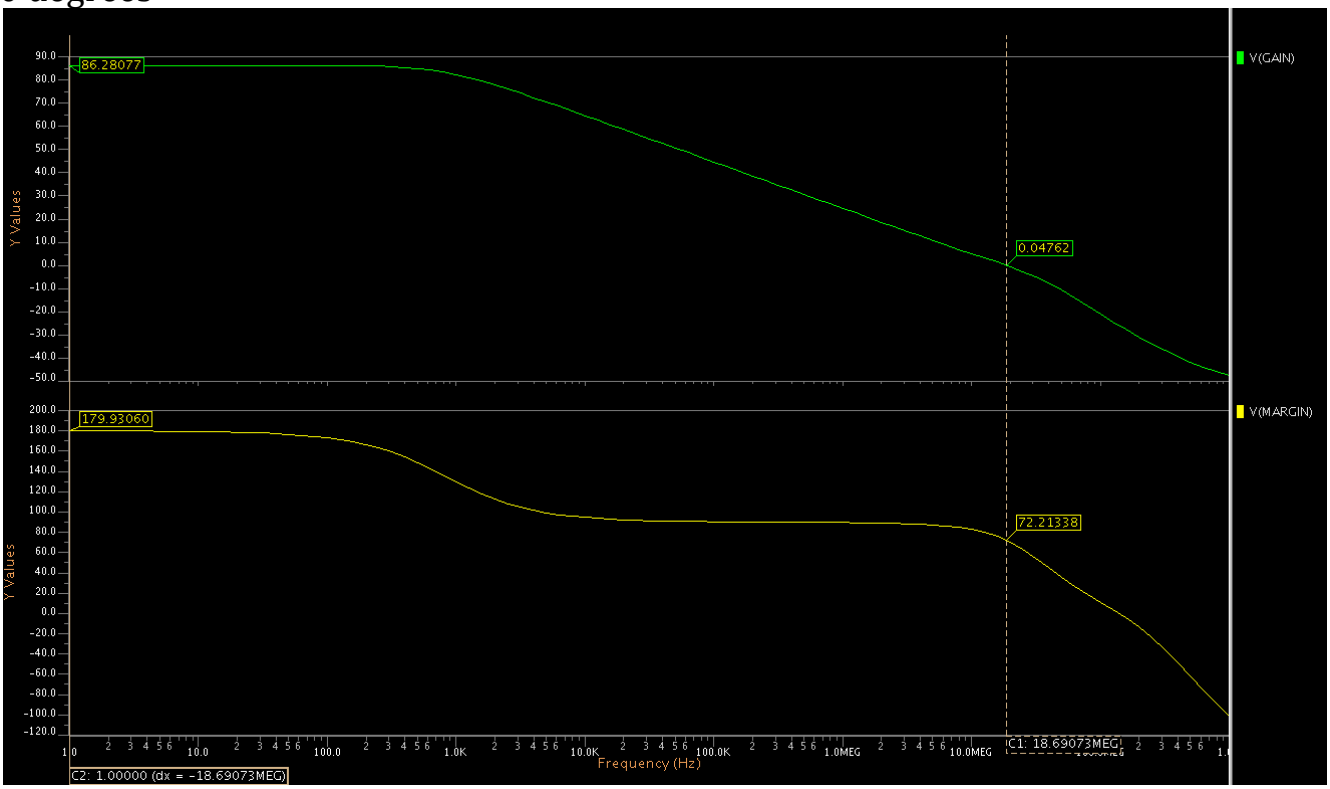
With this 50 mV step, the amplifier is near to critically damped, which makes sense considering the 70 degrees of phase margin; although it is just slightly over damped. (70 degrees is just slightly overdamped).



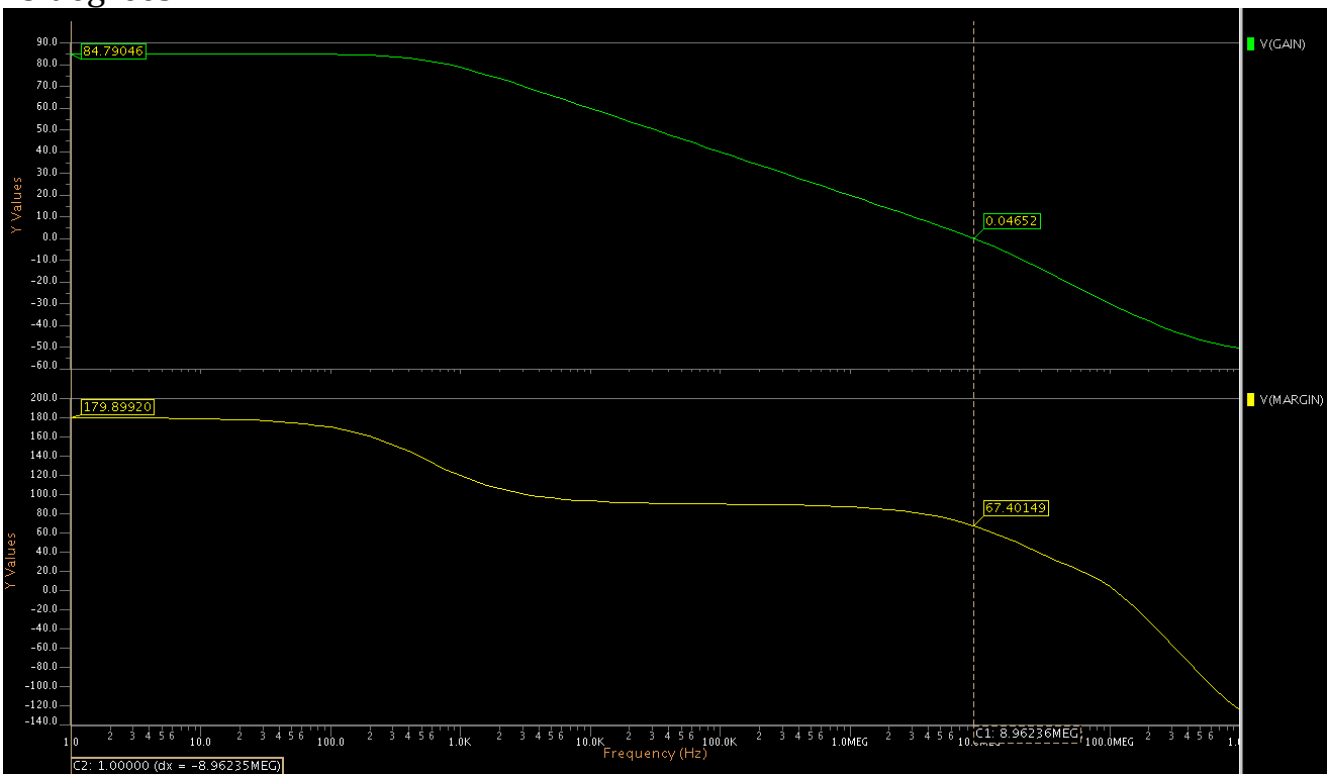
The positive settling time is 0.8 us
The negative settling time is 1.0 us

Number 3

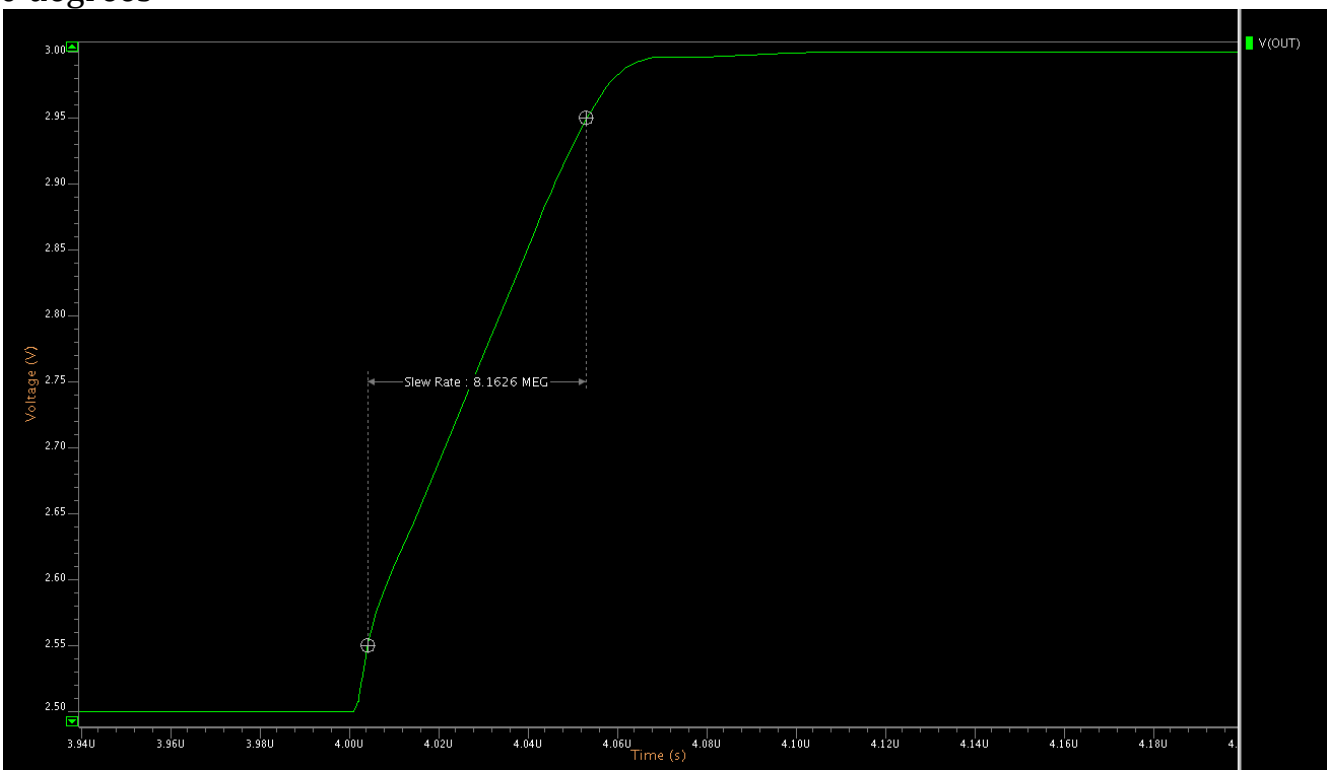
0 degrees



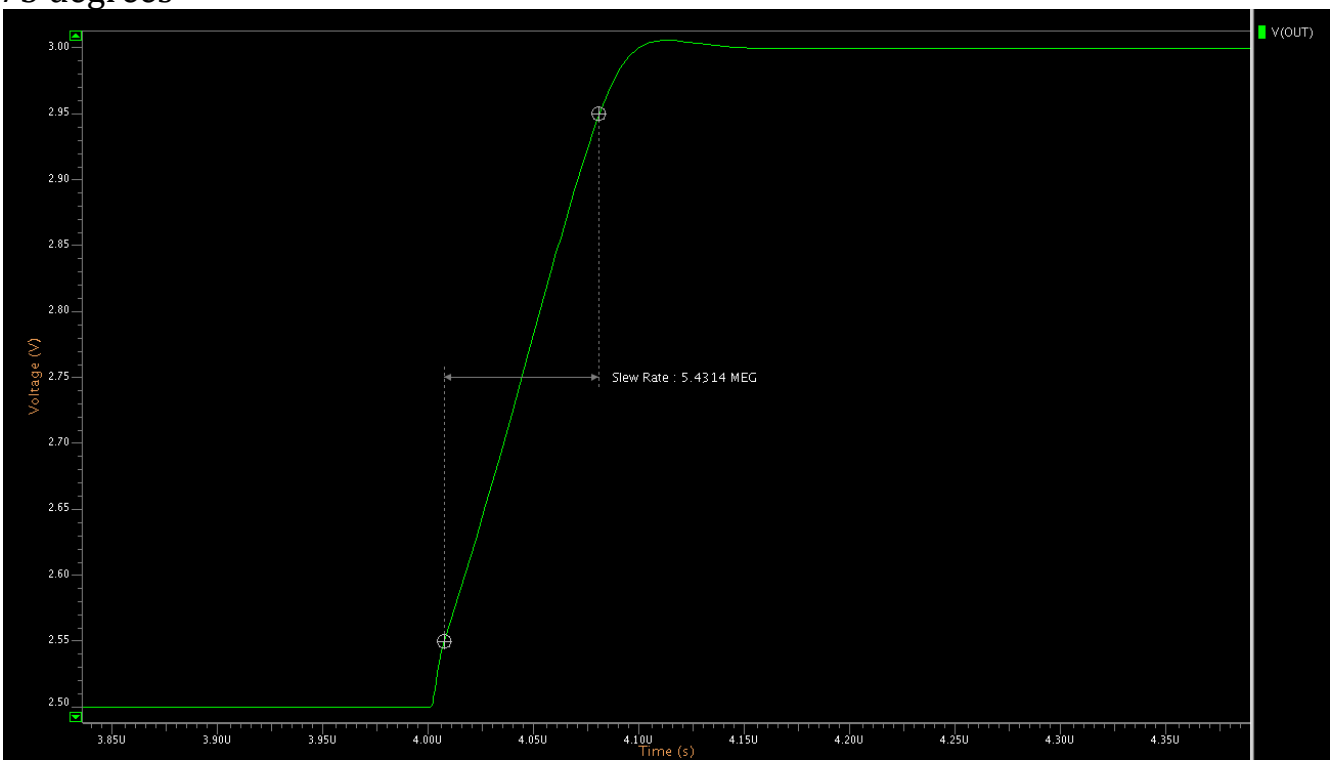
75 degrees



0 degrees



75 degrees



At 0 degrees C the BW, gain and phase margin are all improved.
At 75 degrees C they are all worse.

At 0 degrees C the slew rate improves (positive shown on previous page, negative is the same), at 75 degrees C it gets worse.

The common mode input range does not noticeably change.

Note that in the entire temperature range 0 – 75, my op amp still meets all the requirements.