Design Framework for Reliable, Energy Efficient Cross-Point based Resistive Memory

***Abstract*—Since the conventional memory technologies approaching their scaling limit, the non-volatile memory technologies, such as Phase Change RAM (PCRAM), Magnetoresistive RAM (STT-RAM) and Resistive Memory (ReRAM) have attracted considerable attention because their non-volatility, high access speed, low power consumption and good scalability. Among these emerging memory technologies, the ReRAM has shown great potentials a one of the most promising candidates for future universal memory, due to its simple structure, small cell size and potential for 3D stacking. Besides, the unique non-linearity of ReRAM provides the possibility to build a cross-point structure based ReRAM without CMOS access device, with the smallest cell size of $4F^2$. However, the cross-point structure also suffers from its inherent disadvantages and brings in extra design challenges. In this work, the design challenges of cross-point structure based ReRAM are comprehensively analyzed. In addition to the cell-level analysis, different programming schemes are also discussed in detail. A precise mathematical model is built to perform a comprehensive analysis on the issues of reliability, energy consumption and the area overhead. Based on the study, a detailed design methodology is proposed. With the proposed methodology, designers can explore the most energy/area efficient ReRAM design with different design constraints.**

I. Introduction

The scaling of traditional memory technologies, such as SRAM and DRAM, is approaching its technological and physical limit. In order to effectively follow the Moore's Law [1] in the near further, new memory technologies are desired. In the past few years, the non-volatile technologies, including Phase Change RAM (PCRAM), Magnetoresistive RAM (STT-RAM) and Resistive Memory (ReRAM) have been widely accepted as the candidates for next generation memory to meet the need of higher density, faster access time, and lower power consumption. Among all of these emerging memory technologies, ReRAM has many unique characteristics, including simple structure, non-linearity and high resistance ratio, making it be considered as the most promising technology. Researchers have shown that the state-of-art single-level-cell ReRAM can achieve sub-8ns random access time for both read and write operation with resistance ratio larger than 100 [2]. Also, HP labs and Hynix have already announced that they are going to commercialize the memristor-based ReRAM and predicted that ReRAM could eventually replace the traditional memory technologies [3].

Different from other non-volatile memory technologies, ReRAM can be implemented in a cross-point style structure without any access devices. Generally speaking, in a nano cross-point array, the bistable ReRAM cell is sandwiched by two layers, orthogonal nanowires, without access devices. In this case, the cell size of ReRAM can be further reduced to $4F^2$ per bit. However, the simplicity of the access device free, cross-point structure cell also brings in additional challenges on the peripheral circuit design as well as the memory organization. There are many literatures that analyzed the design challenges of the cross-point ReRAM array [4] [5] [6] [7]. Nevertheless, all of these researches focus on the cross-point memory array itself but do not take into account the overhead of peripheral circuitry and different programming methods. Besides, the analysis of area and energy consumption is also lacking. In this work, we carefully analyzed the design challenges of cross-point structure based ReRAM. A precise mathematical model is built to evaluate the reliability, energy consumption and area of different design schemes and various cell parameters. Based on the study, a detailed design framework is proposed. With the proposed methodology, designers can explore the most energy/area efficient ReRAM design with different design constraints and cell parameters at the very beginning of the design stage. On the other hand, the system designers can also leverage the proposed framework to provide valuable feedback to device researchers to adjust their experiments and offer more useful ReRAM cell. We believe that this kind of two-way communications will be very helpful to accelerate speed-to-market of ReRAM memory.

The rest of this paper is organized as follows. In Section II, the preliminaries of ReRAM technology and cross-point architecture are introduced. Section III discusses the mathematical model built in this paper and detailed the edge conditions for different write and read schemes. Section IV analysis different design constraints of the write and read operation on the cross-point based ReRAM array. Then in Section V, the design methodology for the ReRAM array is proposed based on our mathematical model and simulation results. Finally, the conclusion is presented in Section VI.

II. Preliminaries

This section provides some preliminaries on ReRAM technology and cross-point architecture. Then the limitations of cross-point architecture are discussed, which motivates the work in this paper.

A. Background of ReRAM technology

Table. I compares the state-of-art non-volatile memory technologies. Obviously, the ReRAM and STT-RAM are the most promising technologies because they have faster access time than PCM and FeRAM with reasonable endurance. However, although the STT-RAM shows the fastest read/write latency among all non-volatile memory technologies, the structure of the memory cell is complex and it has large cell size. On the other hand, the ReRAM has very simple cell structure and can be implemented as a cross-point structure, which can work without access devices. The easy structure provides the possibility of high density integration and 3-D stackability to ReRAM based memory. Besides, the ReRAM also has much higher ON-OFF resistance ratio than STT-RAM. Therefore, with all of these advantages, ReRAM based memory is a highly competitive technology compared to all of the emerging non-volatile memory technologies.

As implied by the name, the ReRAM uses its resistance to represent the stored information. The resistance of a ReRAM cell can be switched between high resistance state (HRS) and low resistance state (LRS) by applying an external voltage across the cell. The resistance switching behavior has been noticed for several years and attracted

great research interest recently for the potential application as next generation non-volatile memory technology. Generally, the ReRAM memory cell is usually built on a Metal-Insulator-Metal (MIM) structure. The resistance switching behaviors have been observed in many MIM nanodevice with different metal oxide materials. For example, a TiO_2 based MIM structure ReRAM was proposed by HP Labs in 2008 [8]. The proposed ReRAM is considered as the first experimental realization and a theoretical model of the fourth fundamental circuit elements, which is predicted by Chua [9] about 40 years ago. The memristor-based ReRAM has a very small cell size of $50\times50nm^2$ with access time less than 50ns. Another HfO_2-based bipolar ReRAM is implemented by ITRI this year with as small as 7.2ns access time [2].

Although there are several different ReRAM proposed by researchers, all of them can be classified into two types: the unipolar ReRAM and the bipolar ReRAM. For a unipolar ReRAM cell, the resistance switching behaviors do not depend on the polarity of the voltage input across the cell and only relate to magnitude and latency of the voltage input. However, for a bipolar ReRAM, the voltage polarity for a ON-to-OFF switching (RESET operation) is different from a OFF-to-ON switching (SET operation). A unipolar ReRAM can be easily stacked on top of a diode to built a one diode one resistor (1D1R) ReRAM. However, as mentioned, the its SET and RESET operations have different latencies and therefore the performance is mainly determined by the longer voltage pulse. Besides, the control of SET, RESET and read operations without any disturbance is another crucial design challenge, especially in the high speed ReRAM design. Therefore, the reported state-of-art high performance ReRAM technologies are dominated by bipolar ReRAM [**? Added reference here**].

B. Cross-Point Architecture

There are two possible memory structures for ReRAM implementation: the traditional MOSFET-accessed structure and the cross-point structure. In the MOS-accessed memory array, the conventional memory cell is substituted by the ReRAM cell where the access device remains to be the MOSFET. In this structure, each ReRAM cell has to be accompanied with a MOSFET access device, whose size is much larger than the ReRAM cell. In this case, the area of the memory array is mainly dominated by MOSFET access device rather than the actual ReRAM cell. Therefore, the ReRAM's advantage of ultra small cell size will be eliminated.

On the contrary, the cross-point structure is more area-efficient for the ReRAM based memory array [10]. A schematic view of a typical cross-point memory array is shown in Figure. 1(a). It can be seen that in the cross-point array, the only item at each crossing point is the ReRAM cell. Therefore, the area of the array is significantly reduced since the large MOSFET access part is removed. Figure. 1(b) shows that the cell size of the cross-point memory can achieve $4F^2$, the theoretical minimum size for a single layer single level memory cell. Besides, as aforementioned, the good stackability and the high resistance ratio provide the capability of building multi-layer multi-level cross-point ReRAM array, which can further increase the area efficiency of the ReRAM array [2] [11].

TABLE I
COMPARISON OF NON-VOLATILE MEMORY TECHNOLOGIES

Metric	STT-RAM	PCM	FeRAM	ReRAM
Cell Size(F^2)	$6-20$	$4-8$	15	4
Read Latency(ns)	1-10	20-50	20-80	5-50
Write Latency(ns)	2-20	150	100	5-50
Endurance	10^{15}	10^{8}	10^{12}	10^{8-10}

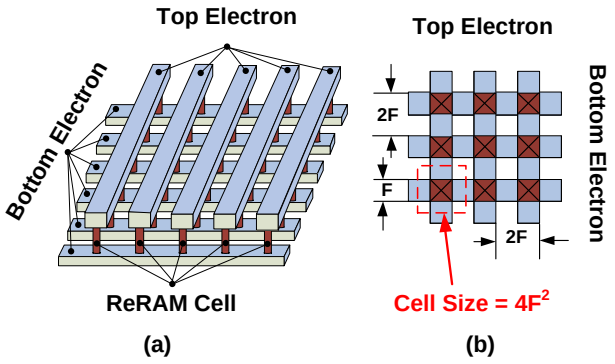


Fig. 1. A schematic view of typical cross-point architecture.

For the cross-point structure, the write operation can either write one bit per time or write several bits at the same word line at the same time. Although the second scheme is more efficient, it required a two-step writing methodology to prevent the unintended writing, which will reduce the write speed. Besides, the unselected word line and bit line can be either left floating or half biased. In read operation, two ways are exhibited for preventing a read failure: the first is to supply the same voltage to the unselected row and selected column. In this way, only the data on the select row is read from the selected column. The disadvantage of this method is the voltage drop on the crossing points of the unselected row and the selected column may not be ideal zero because of the resistance of interconnect wires, and this imposes a limitation on the array size. The second way is a two-step read operation. The disturbance current of the partial selected cell on there selected column will be read out beforehand as a background current. Later the total current, comprised of both partial selected cell and full selected cell, will be read out. The state of the selected cell can then be determined by computing the difference between the total current and background current. Since there are different read/write schemes as well as the array size can be chosen for the cross-point array, it is not a easy way to figure out how to design a workable memory array with the minimum area and energy consumption overhead. Thus, following sections will proposed a worst case based methodology to help designer make the choice at the early step of the design.

C. Limitations of Cross-Point Architecture

III. MODELING OF THE CROSS-POINT MEMORY

In this section, a detailed mathematical model of cross-point memory array is built. By using the proposed model with specific parameters and boundary conditions, different read/write schemes can be easily evaluated at the very early stage of the design.

A. Basic model of Cross-Point Memory

Figure. 2 shows the circuit model of the M by N cross-point ReRAM array. The horizontal lines are word lines and vertical lines represent the bit lines. The ReRAM cells are located at each cross point of one word line and one bit line. The resistance of the ReRAM cell at the cross point of the i^{th} word line and j^{th} bit line is indicated as $R_{i,j}$. We assume the resistance of the interconnect nanowires between two adjacent cross point has the same value of R_{line}. The input resistance of each word line and bit line is R_v and the resistance of sense amplifier is R_s. In order to set up the Kirchhoff's Current Law (KCL) equations, the voltage at each cross point is indicated as $V_{i,j}$ for word line and $V'_{i,j}$ for bit line. A detailed cross point is also shown in Figure. 2. Besides, the input voltage for the i^{th} word line

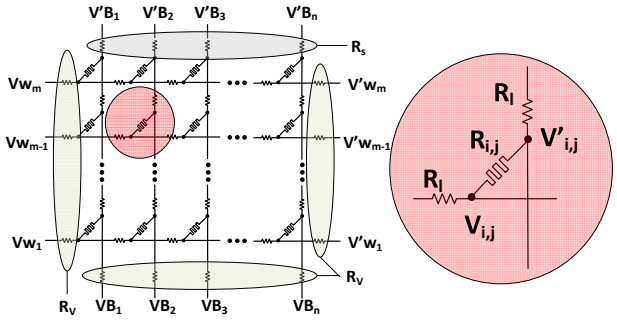


Fig. 2. The basic model of typical cross-point array.

is V_{Wi} and for the i^{th} bit line is V_{Bi}. In the case of two side voltage input of word line, the voltage at the other end of the i^{th} word line is denoted as V_{W1}. Finally, the voltage at the sense amplifier is V'_{Bi} during the read operation.

B. Mathematical Model of the Cross-Point Array

Based on the circuit model, the current equation for each cross point can be built following the KCL:

$$\Sigma_{I=1}^{k} I_k = 0. \tag{1}$$

All of the cross points have similar structure with no more than three current injection and therefore it is easy to set up the KCL equation for each cross point. However, we should treat the cross points at the edges of the array seriously because there are different conditions for different write/read schemes. For example, the unselected word line for write operation can be either half biased or left floating. Thus, the edge conditions should be adjusted according to each write/read schemes. However, even consider the different conditions of at the edge of the array, all of the cross points can be classified into three major categories: Normal point, Activated point and Floating point.

The normal points located inside the memory array. In other words, for all of the nodes with $1 < i < m$ and $1 < j < n$, the KCL equations take the form of

$$R_l^{-1}V_{i,j-1} - (2R_l^{-1} + R_{i,j}^{-1})V_{i,j} + R_l^{-1}V_{i,j+1} + R_{i,j}^{-1}V'_{i,j} = 0, \tag{2}$$

for the node at word line layer and

$$R_l^{-1}V'_{i-1,j} - (2R_l^{-1} + R_{i,j}^{-1})V'_{i,j} + R_l^{-1}V'_{i+1,j} + R_{i,j}^{-1}V_{i,j} = 0, \tag{3}$$

for the node at bit line layer.

The activated point and floating point represent the node at the edge of cross point array with different conditions: an edge point, which have been directly connected to the voltage input or the ground, can be considered as a activated point. Otherwise, it is a floating point. Take the point located at the intersection of i^{th} word line and 1^{st} bit line for example. If the i^{th} word line is activated by a voltage input of V_{Wi}, then this cross point is an activated point, and the KCL equation for this point is:

$$-(R_v^{-1}+R_l^{-1}+R_{i,1}^{-1})V_{i,1}+R_l^{-1}V_{i,2}+R_{i,1}^{-1}V'_{i,1} = -R_v^{-1}V_{Wi}, \tag{4}$$

otherwise, it is left floating and has the KCL equation take the form of

$$-(R_l^{-1} + R_{i,1}^{-1})V_{i,1} + R_l^{-1}V_{i,2} + R_{i,1}^{-1}V'_{i,1} = 0. \tag{5}$$

For the reasons of clarity, a vector $V_{2mn\times 1}$ is used to represent all of the variables in the KCL equations:

$$V = [{V_1}^T, {V_2}^T ... {V_m}^T, {V'_1}^T, {V'_2}^T ... {V'_m}^T]^T, \tag{6}$$

where,

$$V_i = [V_{i,1}, V_{i,2} ... V_{i,n}]^T, \tag{7}$$

$$V'_i = [V'_{i,1}, V'_{i,2} ... V'_{i,n}]^T. \tag{8}$$

Then the KCL equations can be considered as a system of linear equations and has the form of

$$A_{2mn\times 2mn} \cdot V_{2mn\times 1} = C_{2mn\times 1}, \tag{9}$$

where A is the coefficient matrix which is determined by Equation(2)-(5) and C contained the constant terms of these equations. As shown, the KCL equations for each node have very simple structure and are very similar to each other. Therefore, the system of linear equations has a relatively fixed format and simple structure, which will be very easy to establish the equations and to adjust the coefficients according to different design schemes. The characteristics of the linear system can be summarized as:

1) As shown in Equation (10), coefficient matrix A can be further partitioned into 4 smaller subblocks :

$$\mathbf{A} = \begin{bmatrix} A1 & A2 \\ A3 & A4 \end{bmatrix}. \tag{10}$$

All of these subblocks have the same size of $m \times n$. $A2$ and $A3$ are diagonal matrixes and have the value of: $A2_{i,i} = A3_{i,i} = R_{i,i}^{-1}$. Besides, $A2$ and $A3$ do not change their values with different schemas. $A1$ and $A4$ are a little bit more complex than $A2$ and $A3$. $A1$ is a tridiagonal matrix and only has nonzero elements at the location in the main diagonal, and the first line below and above diagonal. Similarly, the A_4 is a special tridiagonal matrix, which has nonzero elements in the main diagonal, the n^{th} line below and above diagonal, where n is the number of bit line in the cross point model. The value of the elements in $A1$ and $A4$ can be easily derived from Equation (2) and (3). However, as mentioned, the edge condition varies with different program schemes. Therefore, the coefficients related to the edge condition should be update according to the program schemes. Clearly, the four edges shown in Figure. 2 correspond to different coefficients in $A1$ and $A4$. Due to the space limitations, we take the nodes at the left edge of the array for example. Coefficients of other edge nodes can be initiated by the same way. The coefficients of nodes at the left edge of the array ($V_{i,1}$) can be set as:

$$A1(k,k) = \begin{cases} -(R_l^{-1} + R_{i,1}^{-1}) & \text{if } floating \\ -(R_v^{-1} + R_l^{-1} + R_{i,1}^{-1}) & \text{if } activated \end{cases} \tag{11}$$

where $k = (n-1)i + 1$ for $i = 1, 2...m$.

2) The constant terms C is a $2mn\times 1$ vector. Equation(2)-(5) show that only KCL equations of the activated points have the constant term. Therefore, only the following elements in C may have non-zero value: $C((i-1)n+1)$, $C(in)$, $C(mn+i)$ and $C((2m-1)n+i)$ for $i = 1, 2...m$, correspond to the nodes at the four edges respectively. Likewise, we take nodes $V_{i,1}$ for example. The constant correspond to these node can be defined as:

$$C((i-1)n+1) = \begin{cases} 0 & \text{if } floating \\ -R_v^{-1}V_{Wi} & \text{if } activated \end{cases} \tag{12}$$

for $i = 1, 2...m$.

Therefore, by given all of the required parameters, including the resistance of ReRAM cell, interconnect wires, program voltage and

write/read schemes, the voltage at each point of the cross point array can be obtained by solving the Equation (9) with simple matrix computations. With the voltage map, $V_{2mn\times 1}$, we can analyzed the array at a very fine granularity. Also, these information can be very useful to evaluate the reliability, energy consumption, driven current density and area overhead of the cross point array.

IV. Analysis of Design Constraints

A. Overview

As shown in Figure. 2, in order to write or read the cross-point array, the external voltages should be applied at the end of the word line and the bit line. Although there are several potential read/write schemes can be used to program the memory array, it is difficult to point out which schemes is the most proper choice under given design constraints of area/energy/reliability. Therefore, in this section, studies on different operation schemes and present are conducted. The results of this study can be very useful to guide the design of the cross-point array. Since it is impossible to consider all of the data pattern stored in the array, in this work, the best and worst cases are studied.

Table II shows the circuit parameter of our baseline design. The data is consistent to the recently published studies on ReRAM [7] [10]. In this section, the reliability, energy consumption and area overhead for the four write schemes are detailed. Then the sensitivities of these schemes to the data pattern of HRS and LRS ReRAM cells, and interconnect wires are studied.

Considering that program schemes for write and read operation are different and the the requirement for write and read are also dissimilar, in the following section we carefully study the write and read operation separately. And then the results are combined together to provide a design methodology for the cross-point array.

B. Write Operation

To write a ReRAM cell, a external voltage is required to applied across the cell for a certain duration. Intuitively, there are four possible schemes for the write operation:

1) According the location of the target cell, activate one word line and one bit line and leave all of the other lines floating (FWFB shemes).
2) Activate the targeted word line and bit line. Left all the other word line floating and half bias the other bit line (FWHB shemes).
3) In contrast with the scheme 2, activate the targeted word line and bit line. Left all the other bit line floating and half bias the other wold line (HWFB shemes).

TABLE II
Parameters of the baseline Cross-Point Array

Metric	Description	Values
S_{cell}	Cell Size	$4F^2$
R_l	Interconnection Resistance	1.25Ω
R_s	Resistance of SA	100Ω
V_{RESET}	Threshold voltage for RESET	$2.0V$
V_{SET}	Threshold voltage for SET	$-2.0V$
V_{READ}	Read Voltage of Cell	$0.5V$
R_{off}	HRS Resistance	$500K\Omega$
R_{on}	LRS Resistance	$10K\Omega$
$V_W(R)$	Word Line Voltage during Read	$\pm 1V$???
$V_W(W)$	Word Line Voltage during Write	$0/2V$
$V_W(H)$	Half Selected Word Line Voltage	$1V$
$V_B(R)$	Bit Line Voltage during Read	$10K\Omega$????
$V_B(W)$	Bit Line Voltage during Write	$0/2V$
$V_B(H)$	Half Selected Bit Line Voltage	$1V$
M	Number of Word Line	64
N	Number of Bit Line	64

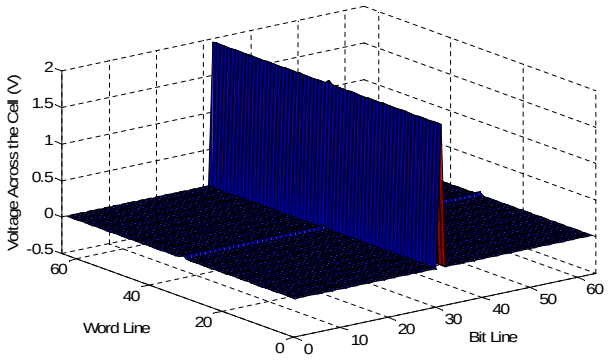


Fig. 3. Write Disturbance for FWFB Schemes. ($V_{W32} = 2V$, $V_{B32} = 0V$. $R_{x,32}$ at HRS, others at LRS.)

4) Activate the targeted word line and bit line. Half bias all of the other bit line (HWHB shemes).

Since the reliability, energy consumption and area overhead for these schemes are different from each other. We will address these problem separately and then combine all of the constraints to provide a design guideline for write operation.

Reliable Write Operation.

The most important issue for the write operation is the reliability concern. In the ideal condition, the resistances of interconnect wires and the sneak currents at unselected cells are negligible. Therefore, all of these four schemes can provide enough voltage drop across the specified cell. However, the realistic circuit is not perfect and the electronic behavior of the array will deviate from the ideal scenario with different data pattern stored. A reliable write operation can be defined as: switching the selected cells into required states without disturbing the states of unselected cells. Therefore, there exist two potential write errors: **write failure**, an unsuccessful write on selected cell, and **write disturbance**, an undesirable write on unselected cell. All of the write schemes should at least meet the reliability requirement at the worst case. On the other word, the designer should make sure there is not any write failure and write disturbance even in the worst case.

First of all, we will discuss the inherent problem of FWFB scheme, which may result in severs write disturbance. A worse case scenario for FWFB write disturbance can be defined as: all of unselected cells in the activated word line (or all of unselected cells in the activated bit line) are at HRS and other cells are in LRS. In this case, the voltage drop at unselected cells are mainly applied at the HRS cells at the word line (or bit line). Figure. 3 shows an example of this case for a 64×64 cross-point array. It clearly that all of the unselected cells at the activated bit line will be disturbed. This inherent problem exists at all of the FWFB schemes and becomes very serious with the large On-OFF resistance ratio. Considering that the reported On-OFF resistance ratio of ReRAM cell is always > 50 [12]–[17], it is impossible to build a cross-point structure ReRAM with the FWFB scheme. Therefore, in the following discussion, we only compare the results of FWHB, HWFB and HWHB schemes. For each of these three schemes, we can either write one word line at the same time or only write one bit per access and separate the write operation to several arrays. In the following discussion, we start from one bit per access write operation. And then the results of one word line per access method are compared.

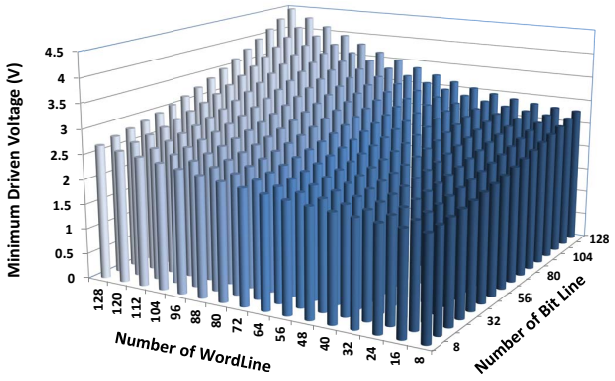


Fig. 4. Write Voltage Requirement (Threshold Voltage = 2V).

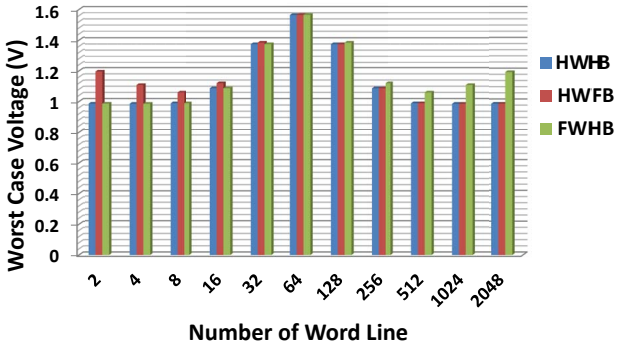


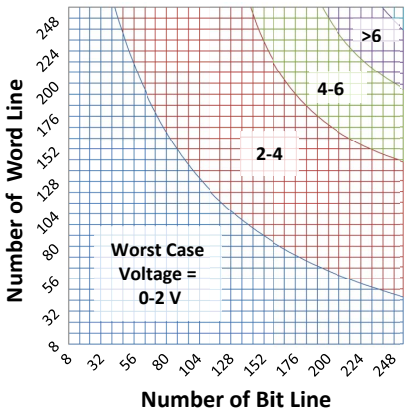
Fig. 5. Write Voltage Requirement with Different Memory Shape. (Array Capacity = 4Kbits, Activated Word Line Voltage = 2V, Activated Bit Line Voltage = 0V.)

The write failure results from the voltage drop at the interconnect wires along the word line and bit line It has been shown that, for one bit per access write operation, the worst case of voltage drop is:

$$\begin{cases} R_{i,j} = R_{on} \\ V_{WM} = V_W(W) \\ V_{BN} = V_B(W). \end{cases} \tag{13}$$

In order to avoid the **write failure** and successful program the selected ReRAM cell, the driven voltage should be increased to a higher level, making sure the voltage across the cell exceed the threshold voltage at the worst case. Figure. 4 shows the lower bound of the driven voltage for different size of cross-point array. The minimum word/bit line voltage increases from 2.01 V for a 8×8 array to 4.47 V for a 128×128 cross-point array. Besides, for a given memory capability, the cross-point can be organized with different number of word line and bit line. For example, a 4K bits cross-point array can be implemented either by a 64×64 array or by a 32×128 array. In the latter case, the voltage drops along the word line and bit line are different with each other. Therefore, Figure. 5 exams the voltage requirement for different array organization. The results show that from the reliability point of view, the cross-point array with same numbers of word line and bit line is the best choice.

However, in the other hand, the increasing of the driven voltage also increases the voltage applied at the unselected cell. Therefore, a **write disturbance** will occur when the voltage applied at the unselected cell exceeds the threshold voltage for SET or RESET operation. Figure. 6 shows the worst case (maximum) voltage applied at unselected cells with the minimum driven voltage shown in



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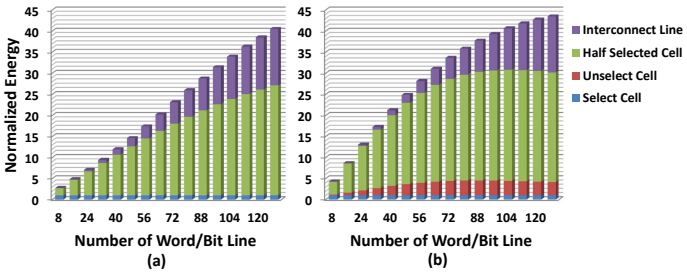


Fig. 7. The Normalized Energy Consumption. (a): HWHB scheme (b): FWHB and HBFW Schemes.

Figure 4. Since the threshold voltage of the cell is 2V, all of the word/bit line combinations at the region with worst case voltage more than 2V are unreliable and can not avoid write failure and write disturbance at the same time. Thus, Figure. 6 provides the hard constraint of array size, and all of the following energy and area tradeoffs should be bounded by this constraint.

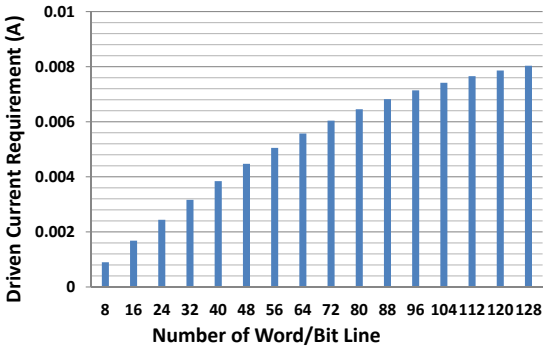
Energy Consumption of Write Operation.

The energy consumption of a write operation for a cross-point array can be calculated as:

$$E_{write} = E_{select} + E_{unselect} + E_{halfselect} + E_{line}, \tag{14}$$

where the E_{select} is the energy consumed to change the state of the selected cell, the $E_{unselect}$ and $E_{halfselect}$ are the undesired energy wasted at the half selected and unselected cells. The energy consumed by the interconnect lines are represented by E_{line}. Figure. 7 shows each part's energy consumption for the cross-point array. Firstly, the E_{line} and $E_{halfselect}$ take a large amount of the total energy consumption. Besides, the energy wasted during the write operation is much larger than the energy required to program the ReRAM cell. For example, the energy consumption for writing a 64×64 array is about 20 30 times larger than the $E_{selected}$. We also notice that, since the impact of sneak paths for floating schemes (FWHB and HWFB) is much serious, the energy consumed at unselected cells for the floating schemes are much larger than the half-biased scheme, resulting the total energy consumptions for FWHB and HWFB schemes are larger than HWHB scheme.

Area cost of Write Operation.



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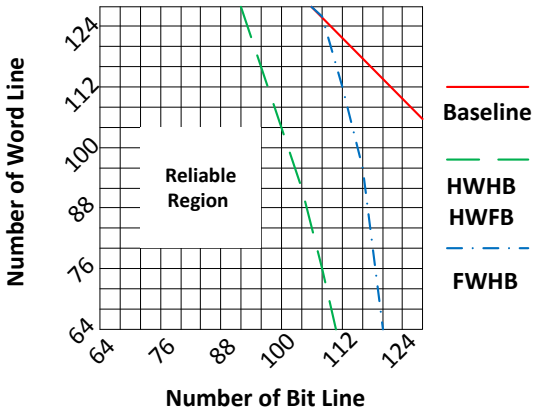

Fig. 9. The

The write operation requires $m+n$ access device for a $m \times n$ array. Therefore, the average number of ReRAM cells per access device can be calculated as $mn/(m+n)$. By given a array capacity C_{array}, it is easy to find that the optimal array organization can be achieved when $m = n = \sqrt{C_{array}}$ and the maximum number of cells per access device is: $\sqrt{C_{array}}/2$. However, the area overhead of the access device also related to the driven current. Figure ?? shows the required driven current for different

Multi-Bits Write Operation.

Non-linearity of the ReRAM Cell.

C. Read Operation

D. Discussion on Non-linearity of the ReRAM

An

V. Framework

A. Experimental Results

VI. Conclusion

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