Design Framework for Reliable, Energy Efficient Cross-Point based Resistive Memory

***Abstract*—Since the conventional memory technologies approaching their scaling limit, the non-volatile memory technologies, such as Phase Change RAM (PCRAM), Magnetoresistive RAM (STT-RAM) and Resistive Memory (ReRAM) have attached much attention because their non-volatility, high speed, low power consumption and good scalability. Among these emerging memory technologies, the ReRAM has shown great potentials a one of the most promising candidates for future universal memory is the ReRAM, due to its simple structure, small cell size and potential for 3D stacking. Besides, the unique non-linearity of ReRAM provides the possibility to build a cross-point structure based ReRAM with out CMOS access device, with the smallest cell size of $4F^2$. However, the cross-point structure also suffers from its inherent disadvantages and brings in extra design challenges. In this work, the design challenges of cross-point structure based ReRAM are comprehensively analyzed. In addition to the cell-level analysis, ??????????????. A precise mathematical model is built to perform ..... Based on the study, a detailed design methodology is developed. With the proposed methodology, designers can explore the most energy/area efficient ReRAM design with different design constraints.**

I. Introduction

The scaling of traditional memory technologies, such as SRAM and DRAM, is approaching a technological and physical limit. In order to effectively follow the Moore's Law [1] in the near further, new memory technologies are desired. In the past few years, the non-volatile technologies, including Phase Change RAM (PCRAM), Magnetoresistive RAM (STT-RAM) and Resistive Memory (ReRAM) have been widely accepted as the candidates for next generation memory to meet the need of higher density, faster access time, and lower power consumption. Among all of these emerging memory technologies, ReRAM has many unique characteristics, including simple structure, non-linearity and high resistance ratio, making it be considered as the most promising technology. Researchers has shown that the state-of-art single-level-cell ReRAM can achieve sub-8ns random access time for both read and write operation with resistance ratio > 100 [2]. Also, HP labs and Hynix have already announced that they are going to commercialize the memristor-based ReRAM and predicted that ReRAM could eventually replace the traditional memory technologies [3].

Different from other non-volatile memory technologies, ReRAM can be implemented in a cross-point style structure. Generally speaking, in a nano cross-point array, the bistable ReRAM cell is sandwiched by two layers, orthogonal nanowires, without any access device. Therefore, the cell size of ReRAM can be further reduced to $4F^2$ per bit. However, the simplicity of cross-point structure with out access cell also bring in additional challenges on the peripheral circuit design as well as memory organization. There are many literatures that analyzed the design challenges of the cross-point ReRAM array. Nevertheless, all of these researches focus on the cross-point memory array itself but do not take into account the peripheral circuity and different programming methods. Besides, the analysis of energy consumption is also lacking. In this work, we carefully analyzed the design challenges of cross-point structure based ReRAM. A precise mathematical model is built to evaluate the reliability, energy consumption and area of different design schemes and various cell parameters. Based on the study, a detailed design framework is developed. With the proposed methodology, designers can explore the most energy/area efficient ReRAM design with different design constraints and cell parameters at the very beginning of the design stage. On the other hand, the system designers can also leverage the proposed framework to provide valuable feedback to device researchers to adjust their experiments and offer more useful ReRAM cell. We believe that this kind of two-way communications will be very helpful to accelerate speed-to-market of ReRAM memory.

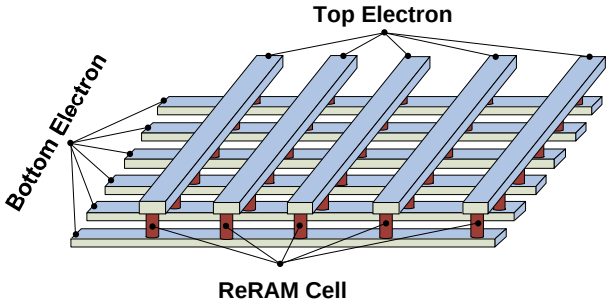

Fig. 1. A schematic view of typical cross point architecture.

The rest of this paper is organized as follows. In Section **??**, the memristor based memory and the basic concept of ECC are introduced. Section **??** discusses the mathematical model used in this paper and evaluates various ECC designs for memristor-based ReRAM architecture. Section **??** shows results of the experiment conducted in this study. Finally, the conclusion is presented in Section **??**.

II. Preliminaries and Motivations

This section provides some preliminaries on ReRAM technology and cross-point architecture. Then the limitations of cross-point architecture are demonstrated by a series of simple example, which motivates the work in this paper.

A. ReRAM technology and Cross-Point Architecture

b State of Art ReRAM technologies.
Memristor based ReRAM.
Cross-Point Architecture.
Sneak Path.

B. Motivations

As aforementioned, although the cross-point structure can provide the fabricate simplicity and area efficiency, it also incur lots of design challenges. Following cases show some examples to demonstrate the disadvantages of the cross-point structure, which motivates the work in this paper.

1) **Reliable Write Operation**
In order to

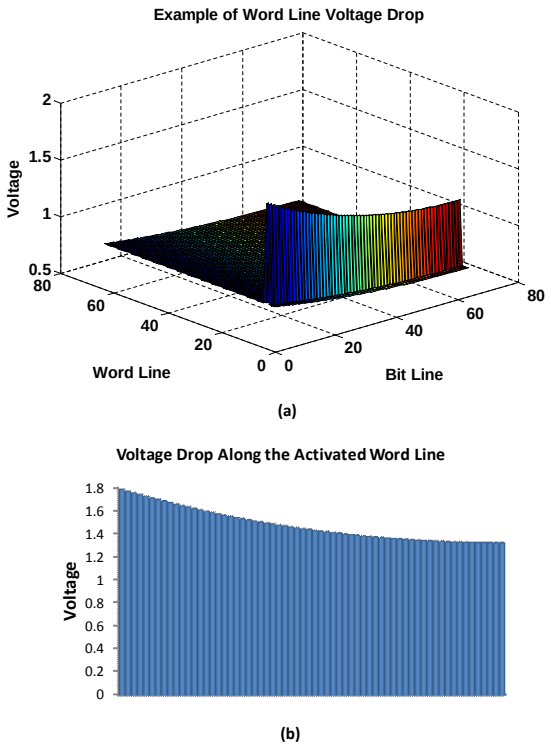

Fig. 2. Case 1: Voltage Drop Along the Word Line during Write Operation.

2) **Read Margin Disturbance**
123

3) **Energy Waste Due to Sneak Pass**
123

[4] [5] [1]

III. Related Work

IV. Modeling of the Cross-Point Memory

In this section, a detailed mathematical model of cross-point memory array is built. By using the proposed model with specific parameters and boundary conditions, different read/write schemes can be easily evaluated at the very early stage of the design.

A. Basic model of Cross-Point Memory

Figure. 3 shows the circuit model of the M by N cross point ReRAM array. The horizontal lines are word line and vertical lines represent the bit line. The ReRAM cells are located at each cross point of one word line and one bit line. The resistance of the ReRAM cell at the cross point of the i^{th} word line and j^{th} bit line is indicated as $R_{i,j}$. We assume the resistance of the interconnect nanowires between two adjacent cross point has the same value of R_{line}. The input resistance of each word line and bit line is R_v and the resistance of sense amplifier is R_s. In order to set up the Kirchhoff's Current Law (KCL) equations, the voltage at each cross point is indicated as $V_{i,j}$ for word line and $V'_{i,j}$ for bit line. A detailed cross point is also shown in Figure. 3. Besides, the input voltage for the i^{th} word line is V_{Wi} and for the i^{th} bit line is V_{Bi}. In the case of two side voltage input of word line, the voltage at the other end of the i^{th} word line is denoted as V_{W1}. Finally, the voltage at the sense amplifier is V'_{Bi} during the read operation.

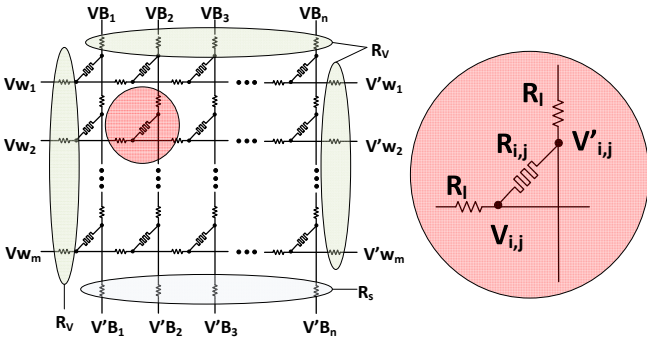

Fig. 3. The basic model of typical cross point array.

B. Edge Conditions for Different Write/Read Schemes

Based on the circuit model, the current equation for each cross point can be built following the KCL:

$$\Sigma_{I=1}^{k} I_k = 0. \quad (1)$$

All of the cross points have similar structure and therefore it is easy to set up the KCL equation for each cross point. However, the cross point at the edge of the array may have different condition for different write/read schemes. For example, the unselected word line for write operation can be either half biased or left floating. Thus, the edge conditions should be carefully considered for each write/read schemes. However, generally speaking, all of the cross points can be classified into three major categories: Normal point, Activated point and Floating point.

The normal point located insides the memory array. In other words, for all of the nodes with $1 < i < m$ and $1 < j < n$, the KCL equations take the form of

$$R_l^{-1}V_{i,j-1} - (2R_l^{-1} + R_{i,j}^{-1})V_{i,j} + R_l^{-1}V_{i,j+1} + R_{i,j}^{-1}V'_{i,j} = 0, \quad (2)$$

for the node at word line layer and

$$R_l^{-1}V'_{i-1,j} - (2R_l^{-1} + R_{i,j}^{-1})V'_{i,j} + R_l^{-1}V'_{i,j+1} + R_{i,j}^{-1}V_{i,j} = 0, \quad (3)$$

for the node at bit line layer.

Besides, the activated point and floating point represent the node at the edge of cross point array with different condition: a point, which have been directly connected to the voltage input or the ground, can be considered as a activated mode. Take the cross point connected to word line voltage

C. Analysis of the Computing Complexity

V. Analysis of Design Constraints

A. Overview

B. Write Operation

1. Only consider the one-side scheme Consider 1/2 1/3 and floating? Energy Issue? Define Energy Efficient Parameter? Reliable Issue: Any possibility of write disturbance

2. Present the voltage drop problem Reliability Issue

3. Two Way Scheme

C. Read Operation

D. Framework

E. Experimental Results

F. Conclusion

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