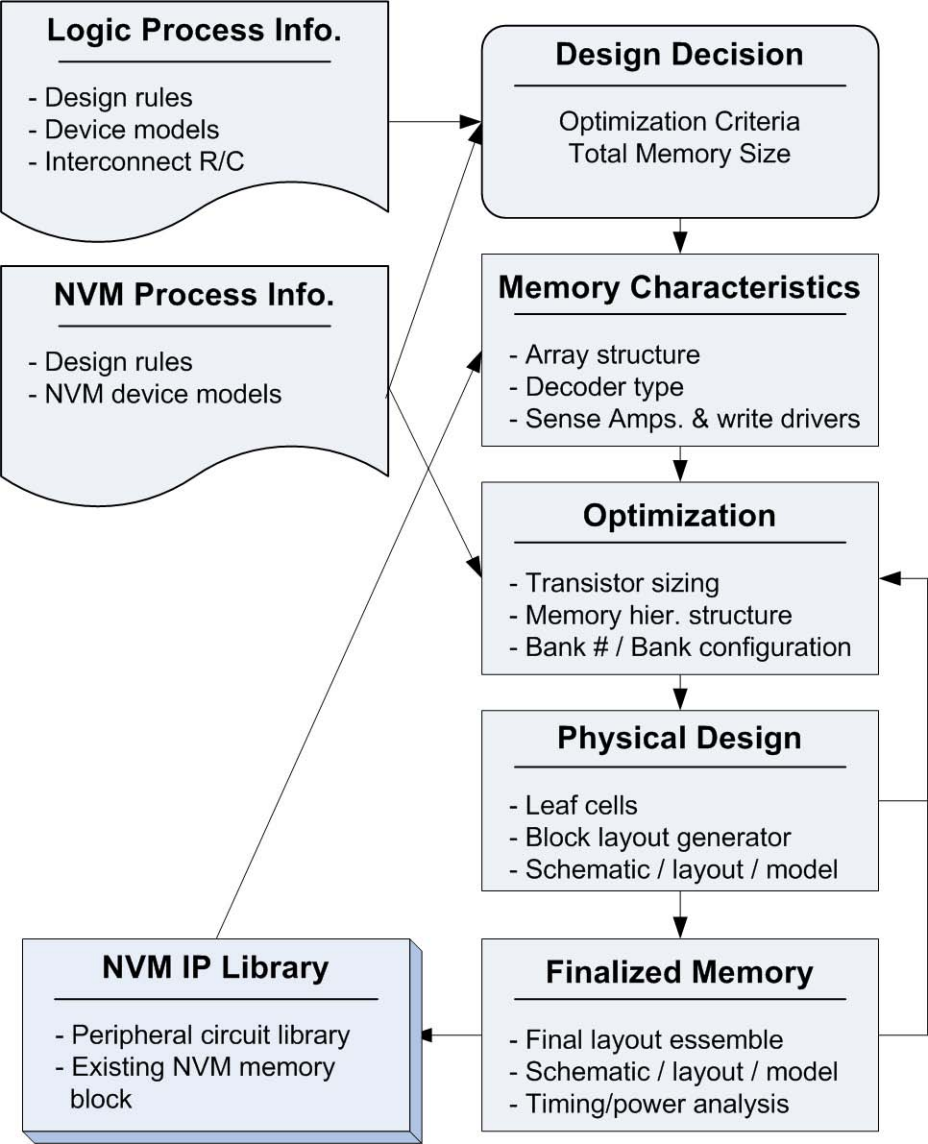
Logic Process Info.
- Design rules
- Device models
- Interconnect R/C
NVM Process Info.
- Design rules
- NVM device models
Design Decision
Optimization Criteria
Total Memory Size
Memory Characteristics
- Array structure
- Decoder type
- Sense Amps. & write drivers
Optimization
- Transistor sizing
- Memory hier. structure
- Bank # / Bank configuration
Physical Design
- Leaf cells
- Block layout generator
- Schematic / layout / model
Finalized Memory
- Final layout essemble
- Schematic / layout / model
- Timing/power analysis
NVM IP Library
- Peripheral circuit library
- Existing NVM memory block