Circuit Techniques and System Applications for Emerging Non-Volatile Memory in Hybrid Computing Systems

Project Description

1 Introduction

In modern computer architecture design, the storage of instruction and data follows a hierarchical arrangement called **memory hierarchy**, which takes advantage of the access locality and the performance-capacity trade-offs of diverse memory technologies. The importance of the memory hierarchy increases with the advances in microprocessor performance [1]. Figure 1 illustrates a typical memory hierarchy. The closer the memory is placed to microprocessor, the faster latency and higher bandwidth are required, with the penalty of the smaller capacity. Different memory technologies, such as SRAM, DRAM, and magnetic hard disk drives (HDD) are the common memory embodiments at the different levels in the memory hierarchy, respectively. With the improvements in speed, density, and cost of Flash memory, solid-state drives (SSD) have gained the momentum as the replacements of the traditional magnetic HDD (Figure 1).

Besides increasing leakage power dissipation, technology scaling also significantly degrades the reliability of SRAM and DRAM. In recent years, we have seen a lot of efforts have been made to address the research and development of some **emerging non-volatile memory (NVM) technologies**, e.g., *Phase-Change RAM (PCRAM)*, *Magnetic RAM (MRAM)*, *Resistive RAM (RRAM)*, and *Memristor*. By combing the speed of SRAM, the density of DRAM, and the non-volatility of Flash memory, these emerging memory technologies demonstrated a great potential to be the candidates of the future universal memories.

In order to enable the massive production and to accelerate the commercialization of the emerging memory technologies, it is important for designers to understand their physical mechanisms, investigate new circuitries, and look for new applications for better utilizing them to improve the performance/power/reliability of future computing systems. To be more specific, we are trying to answer the questions as follows.

Here, we propose a three-year project. The main objective of the proposal is to study design techniques and system applications for such emerging memory technologies ini future computer systems. The proposed program makes the following major contributions.

- **Developing device models for emerging non-volatile memories (NVMs):** The device models for emerging non-volatile memories (NVMs) will be developed to fill the gap between process development and circuit design society.
- **Proposing novel circuits techniques:** Based on the unique device characteristics of NVMs, the proposed circuit design techniques could make up the shortfalls of NVMs and even utilize its advantages.
- **Exploring novel applications on system:** The novel application of the emerging NVM in computing systems will be exploited. The corresponding circuit support and architecture implementation will be investigated too.
- **Integrated educational plan:** The educational plan will enhance the existing standard curricula by integrating new course modules on emerging non-volatile memories to complement and upgrade the core computer architecture courses, and bring the awareness of emerging memory technologies into the circuit design and computer architecture community through tutorials and workshops.

Figure 1 illustrates the overview of the proposed project. The proposed work will initiate a novel research direction in high-performance system design and investigate the impact of emerging

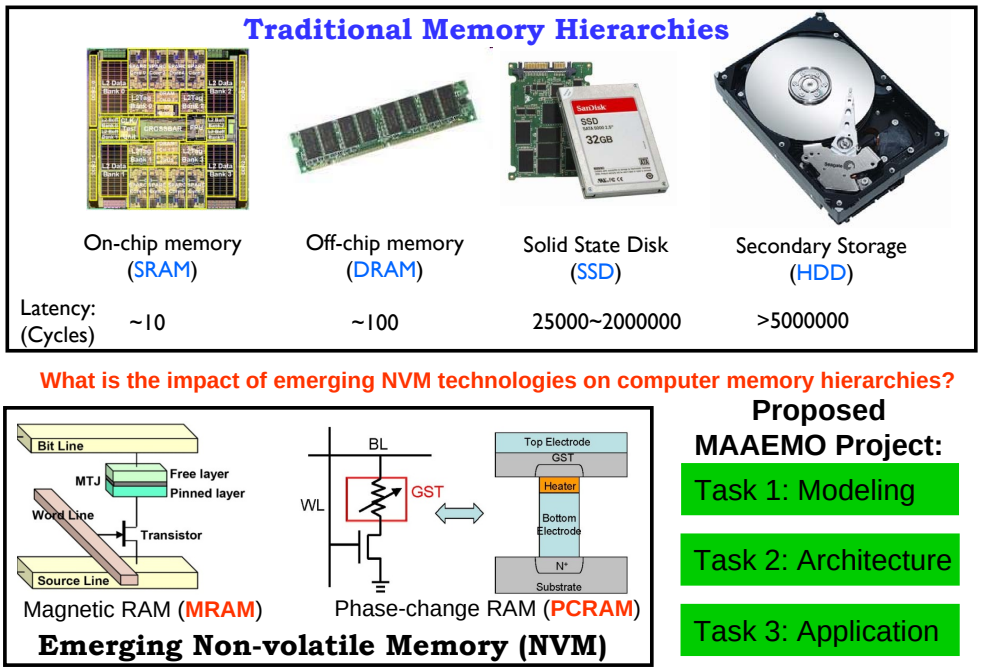

Figure 1: **Project Overview.** Top: Traditional memory hierarchies consist of SRAM, DRAM, SSD, and HDD; Bottom: MRAM and PCRAM are the most promising emerging memory technologies. Research Goal: Study the impact of emerging nonvolatile memory technologies on computer architecture design, with 3 proposed tasks in NVM modeling, architectures, and applications.

memory technologies on future computing systems. This work will support the deployment of modern microprocessor designs that use emerging nonvolatile memory technologies. The proposed research will provide a complementary perspective to the existing computing system research.

2 Background

In recent years, significant efforts and resources have been put on the researches and developments of emerging memory technologies that combine attractive features such as scalability, fast read/write, negligible leakage, and non-volatility. Multiple promising candidates, such as Phase-Change RAM (PCRAM) and Magnetic RAM (MRAM), Resistive RAM (RRAM), and Memristor, have gained substantial attentions and are being actively pursued by industry [2]. In this section we will briefly describe the fundamentals of the two most promising emerging memory technologies to be investigated in our project, namely, the Magnetic RAM (MRAM) based on Spin-Torque Transfer RAM(STT-RAM), and the Phase-Change RAM (PCRAM).

MRAM based on Spin-Torque Transfer RAM (STT-RAM) technology. STT-RAM is a new type of Magnetic RAM (MRAM) [**?**,**?**,**?**,1,3], which features non-volatility, fast writing/reading speed (<10ns), high programming endurance ($>10^{15}$cycles) and zero standby power [1]. The storage capability or programmability of MRAM arises from magnetic tunneling junction (MTJ), in which a thin tunneling dielectric, e.g., MgO., is sandwiched by two ferromagnetic layers, as shown in Figure 1. One ferromagnetic layer ("pinned layer") is designed to have its magnetization pinned, while the magnetization of the other layer ("free layer") can be flipped by a write event. An MTJ has a low (high) resistance if the magnetizations of the free layer and the pinned layer are parallel (anti-parallel). In first-generation MRAM design, the magnetization of free layer is changed by the current-induced magnetic field [4, 5]. In STT-RAM, a new write mechanism called "polarization-current-induced magnetization switching" is introduced – the magnetization of free layer is flipped

by the electrical current directly. Because the current required to switch an MTJ resistance state is proportional to the MTJ cell area, STT-RAM is believed to have a better scaling property [**?**, 3, 6] than the first-generation MRAM. Prototyping STT-RAM chips have been demonstrated recently by various companies and research groups [3, 4, 6–9]. Commercial MRAM products have been launched by companies like Everspin (which is a spin-off from Freescale to expedite the technology commercialization in 2008) and NEC.

Phase-Change RAM (PCRAM). PCRAM technology is based on a chalcogenide alloy (typically, Ge_2–Sb_2–Te_5, GST) material, which is similar to those commonly used in optical storage means (compact discs and digital versatile discs) [10]. The data storage capability is achieved from the resistance differences between an amorphous (high-resistance) and a crystalline (low-resistance) phase of the chalcogenide-based material. In SET operation, the phase change material is crystallized by applying an electrical pulse that heats a significant portion of the cell above its crystallization temperature. In RESET operation, a larger electrical current is applied and then abruptly cut off in order to melt and then quench the material, leaving it in the amorphous state [2]. PCRAM has shown to offer compatible integration with CMOS technology [11], fast speed [12], high endurance [13], and inherent scaling of the phase-change process at 22-nm technology node and beyond [14]. Compared to STT-RAM, PCRAM is even denser with an approximate cell area of $6 \sim 12F^2$ [1], where F is the feature size. In addition, phase change material has a key advantage of the excellent scalability within current CMOS fabrication methodology [12, 15–18], with continuous density improvement [19–21]. Many PCRAM prototypes have been demonstrated in the past years by companies like Hitachi [22], Samsung [23], STMicroelectronics [24, 25], and Numonyx [26].

Resistive RAM (RRAM). RRAM can generally denote all the memory technologies that rely on the resistance change to store the data. Based on the storage mechanisms, RRAM materials can be cataloged as space-charge-limited-current (SCLC), filament, programmable-metallization-cell (PMC), Schottky contact and traps (SCT), *etc.* Among them, filament-based RRAM has been wided investigated because of the potentials on high-speed, high-endurance, and better scalability. The nsulating material between two electrodes can be made conducting through a hopping or tunneling conduction path after the application of a sufficiently high voltage, a process called electro-forming. The data storage could be achieved by break ("reset") or reconnect ("set") the conducting path. Such switching mechanism can in fact be explained with the fourth circuit element, i.e., the memristor or the memory resistor [27–29]. Indeed, HP Labs plan to unveil RRAM prototype chips based on memristors with crossbar arrays soon.

Memristor. Memristor, the fourth fundamental passive circuit element, was predicted by Professor Chua in 1971 [27], based on the completeness of circuit theory. Different from other electrical parameters resistance (R), capacitance (C) and inductance (L), memristance (M) is a function of charge (q), which depends upon the historic behavior of the current (or voltage) profile [30]. In 2008, 37 years after memristor was predicted in theory, the researchers at HP reported the first real device of a memristor. The memristive effect was achieved in a solid-state thin film two-terminal device by moving the doping front along the device [28]. Afterwards, magnetic technology provides the other possible methods to build a memristive system [31, 32]. Due to its unique historic characteristic, memristor has very broad application including nonvolatile memory, signal processing, control and learning system etc [33].

Summary. Figure 2 illustrates the comparison of two emerging memory technologies – PCRAM and MRAM (STT-RAM) – against the traditional main-stream SRAM, DRAM, and NAND-based Flash memory [1]. Note that both CMOS-compatible embedded MRAM (NEC) [**?**] and embedded PCRAM (Hitachi and STMicro) [**?**, **?**] have been demonstrated, paving the way of integrating these

	SRAM	DRAM	NAND Flash	PCRAM	MRAM (STT-RAM)
Data Retention	N	N	Y	Y	Y
Memory Cell Factor (F^2)	50-120	6-10	2-5	6-12	4-20
Read Time (ns)	1	30	50	20-50	2-20
Write /Erase Time (ns)	1	50	106-10^5	50-120	2-20
Number of Rewrites	10^{16}	10^{16}	10^5	10^{10}	10^{15}
Power Read/Write	Low	Low	High	Low	Low
Power (Other than R/W)	Leakage Current	Refresh Power	None	None	None

Figure 2: The comparison of various memory technologies [1].

NVMs to the traditional memory hierarchies. In addition, the emerging 3D integration technologies [**?**, **?**] enables cost-effective integration of these NVMs with CMOS logic circuits. With all the NVM technology advances in recent years, it is anticipated that the emerging NVM technologies will break important ground and move closer to market in the near future ("Non-volatile memory goes commercial", EEtimes, 12/02/2009).

3 Research Overview

To enable the massive production and commercialization of the emerging memory technologies, there are many critical technical issues to be solved. For example, how to introduce the novel devices into the existing design flow? How to minimize the process variation impacts? How to relieve the effect of the poor endurance and improve life time? In this project, we start with the modeling and analysis methodologies for emerging non-volatile memories (NVMs); Next, novel circuitry schemes will be proposed for each emerging NVMs based on their physical characteristics or issues; Finally, we explore novel applications that are enabled by the unique features of emerging NVM technologies. Our proposed research takes a holistic design perspective with close collaboration between two PIs with complementary expertise, aiming at accelerating the adoption of emerging NVMs for future computer architecture design.

4 Task 1: Device Modeling and Design Flow

HL: Need to be modified. To help the architectural level and system-level design of the SRAM-based or DRAM-based cache and memory, various modeling tools have been developed during the last decade. For example, CACTI [**?**, **?**, **?**, **?**] and DRAMsim [34] have become widely used in the computer architecture community to estimate the speed, power, and area parameters of SRAM and DRAM caches and main memory. Similarly, to explore new design opportunities that these emerging memory technologies can bring to the designers at architecture and system levels, it is imperative to have a high-level model for caches and memories built with emerging NVMs, such as MRAM/PCRAM. The model needs to provide the extraction of all important parameters, including access latency, dynamic access power, leakage power, die area, and I/O bandwidth *etc.*, to facilitate architecture and system-level analysis and to bridge the gap between the abundant research activities at process and device levels and the lack of a high-level cache and memory model for emerging NVMs.

4.1 NVM Device Modeling

Not like SRAM which is based on traditional CMOS technology, new materials are introduced in the emerging NVM technologies. For example, MRAM arises from magnetic tunneling junction (MTJ), and PCRAM technology is based on Ge_2–Sb_2–Te_5. Due to the lack of knowledge on material

physics of these NVM devices, most of research works on circuit, architecture and system levels nowadays are based on highly-simplified characteristics of the emerging devices. This methodology can cause a large design overhead, increase the production cost, and reduce the design margin, especially in the highly scaled technology with large process variations. For example, the data storage element MTJ at a certain resistance state is usually modeled as a constant resistor by ignoring the dependency of the MTJ resistance on the magnitude of the read/write current driven by the NMOS selection transistor in an MRAM cell. Our previous work [35] showed that after adopting a dynamic MTJ model that can take into account the time-varying electrical inputs in MRAM design flow, the design pessimism can be dramatically minimized and the memory array area can be reduced by more than 40%. Therefore, one of the important tasks of our proposal is to build device models of the emerging NVM technologies for circuit design. Both dedicated device model and simplified behavioral model will be developed.

The dedicated device models, which will be built based on physical mechanism and corroborated by device measurements, need to satisfy three requirements: (1) These models should provide not only the accurate static characteristics (i.e., I-V relationship and high/low resistances), but also the reasonable dynamic behaviors, for example, what is the relationship between write current amplitude and write current pulse width and frequency in PCRAM design? How does MTJ resistance change during the magnetic direction transition of ferromagnetic layer? (2) The device parameter fluctuations induced by process variations, such as line-edge roughnesses (LERs), oxide thickness fluctuations (OTFs), and random discrete dopants (RDDs), will be also analyzed and integrated into the dedicated device model; and (3) the models should have reasonable runtime and be compatible to commercial EDA tools, i.e., HSPICE from Synopsys [36] and Spectre from Cadence. Hence, Verilog-A or C language could be used to implement these models. The dedicated model will be used for memory optimization and timing/power analysis.

On top of it, the simplified behavioral models will be extracted. High-level languages, i.e. VHDL/Verilog or C will be used. The highly simplified conceptual model will be used for logic and functionality analysis.

4.2 Circuit Design Flow

Another important task of our proposal is to build a design environment that can be seamlessly integrated with the existing CMOS logic design flow. **HL: Modify figure**. Figure 3 illustrates the proposed scope of device modeling and circuit analysis methodology for the emerging NVMs. In Stage I, we will develop the dedicated device models be based on physical mechanism. On top of it, the simplified behavior models will be extracted. In Stage II, we will build an emerging memory design flow, which can realize the creation and optimization of novel hierarchal memory array structure and peripheral circuitry. The accuracy of the corresponding device model will determine the cred-

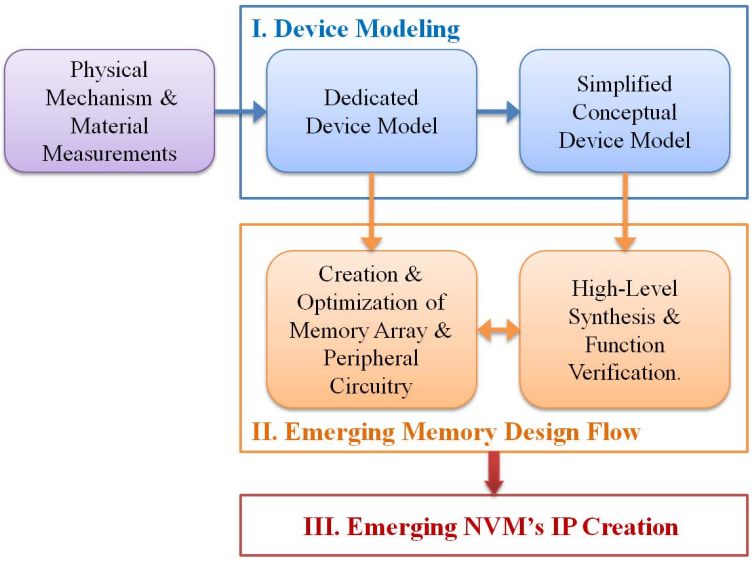

Figure 3: The proposed scope of device modeling and circuit analysis methodology for the emerging NVMs.

ibility of the design, such as critical timing/power simulation and corner analysis. Therefore, the dedicated device model will be used in this step. High-level synthesis and function verification will also be an important part in Stage II. The simplified conceptual model is expected to provide sufficient accuracy and can be easily integrated in the commercial EDA tools and design methodologies such as *Primetime* and *Timemill* from Synopsys [36] for more thoroughly analysis, *i.e.*, the critical path timing at design corners. In Stage III, we will build IP's (Intelligence Properties) for emerging NVM technologies with the aid of the proposed design flow in Stage II. The IP's will provide the extracted parameters of memory array cell including area, dynamic and leakage power, access latency, *etc.*, the recommendable memory array structures and the corresponding trade-offs, as well as the optimized peripheral circuitry design, *i.e.*, sense amplifier and write drivers. Those IP's will be used in the researches at architectural and system levels.

The whole methodology and the corresponding outcomes, including device models, memory design flow, and IP's, will be distributed to the architecture and system design community. Our project will build a channel and provide a friendly interface among material development, device fabrication and architecture design.

4.3 Architectural Modeling

Based on the device/circuit-level modeling and analysis methodologies described in Task 1-A, we will develop a PCRAM/MRAM simulator, which can be easily integrated with architecture simulators including Simplescalar-based single core simulator [**?**, **?**], and multi-core simulators such as M5 [**?**],GEMS [**?**] or PTLsim [**?**].

Note that tools such as CACTI [**?**,**?**,**?**,**?**] and DRAMsim [34] have been widely used in the computer architecture community to estimate the speed, power, and area parameters of the traditional caches and main memory. However, these existing tools were initiated and built based on the cache and memory modelings of SRAM/DRAM. The architectural modeling for PCRAM/MRAM raises unique research issues and challenges on building such simulators. First, some circuitry modules in PCRAM/MRAM have different requirements from those originally designed for SRAM/DRAM. For example, the existing sense amplifier model in CACTI [**?**,**?**,**?**,**?**] and DRAMsim [34] is voltage-mode sensing, while PCRAM data reading usually uses a current-mode sense amplifier. Second, due to the unique device mechanisms, the models of PCRAM/MRAM need specialized circuits to properly handle their operations. We can still take PCRAM as an example. The specific pulse shapes are required to heat up GST material quickly and to cool it down gradually during the RESET and especially SET operations. Hence, a model of the slow quench pulse shaper need to be created. Finally, the most obvious and important difference between PCRAM/MRAM and SRAM/DRAM is their distinct memory cell structure. PCRAM and MRAM typically use a simple "1T1R" (one-transistor-one-resistor) or "1D1R" (one-diode-one-resistor) structure, while SRAM and DRAM cell has a conventional "6T" structure and "1T1C" (one-transistor-one-capacitor) structure, respectively. The difference of cell structures directly leads to different cell sizes and array structures.

In addition, where to place these NVM memories in the traditional memory hierarchy also influences the modeling methodologies. For example, the emerging NVMs could be used as a replacement for on-chip cache or for off-chip DIMM (dual in-line memory module). Obviously, the performance/power of on-chip cache and off-chip DIMM would be quite different: When a NVM is integrated with logics on the same die, there is no off-chip pin limitation so that the interface between NVM and logic can be re-designed to provide a much higher bandwidth. Furthermore, off-chip memory is not affected by the thermal profile of the microprocessor core while the on-chip cache is affected by the heat dissipation from the hot cores. While higher on-chip temperature has a negative impact on SRAM/DRAM memory, it actually has a positive influence on PCRAM because the heat can facilitate the write operations of PCRAM cell. The performance estima-

tion of PCRAM becomes much more complicated in such a case. Moreover, building an accurate PCRAM/MRAM simulator needs close collaborations with the industry (see collaboration letters from HP, IBM, IMEC, and Seagate) to understand physics and circuit details, as well as architectural level requirements such as the interface/interconnect with the multi-core CPUs.

4.4 Preliminary Result and Collaborations:

The PI Li has built a combined magnetic and circuit design analysis and optimization methodology for MRAM, which has been proved to improve design efficiency significantly [35] by test-chip design and fabrication at Seagate. We are also one of the first researchers to propose spintronic memristor structures [32], which was interviewed by IEEE Spectrum [37]. The corresponding compact model and corner analysis [33] have also been developed. In this project, we will further extend this methodology to other emerging NVMs, such as PCRAM.

The PSU PI Xie has developed a stacked SRAM cache simulator called 3DCacti [**?**, **?**], which has been widely downloaded and used by other researchers. The PI and co-PI have collaborated together when the PI Li was in Seagate, to develop a preliminary version of MRAM simulator for cache stacking [**?**, **?**]. Xie also collaborated with Dr. Norm Jouppi from HP Labs, developed a preliminary version of PCRAM simulator [**?**]. We will extend our tools to support architectural exploration in Task 2, especially for hybrid memory systems with an emphasis on multi-core architecture (for example, interface design and coherency modeling) and with Non-Uniform Cache Architecture(NUCA) model (for large memory). Dr. Norm Jouppi from HP Labs, with his expertise in memory architecture modeling, will keep a close collaboration with us for the development of the architectural models for NVMs (see supporting letter from Dr. Jouppi), and we will integrate our models to HP Labs' CACTI tool [**?**], which is an integrated cache and memory model that is widely used in computer architecture community for design space exploration.

5 Task 2: Explore novel circuit techniques for NVM

The advent of novel materials and devices have introduced a number of new design issues. On one hand, all types of emerging NVM technologies are facing to the common requirements – fast speed, high density, affordable yield, low power, etc. On the other hand, the primary concern and effective solution could be quite different for each NVM technique because of the specific device characteristic and process integration difficulty. Our task here is to investigate the common design issues and to exploit distinctive circuit techniques for each individual emerging NVM technology. More specifically, we will focus on three main issues in memory design – yield, reliability, and density.

5.1 Write Endurance Improvement

Write endurance is one of the biggest obstacles that prevent the emerging NVMs from massive production and wide application, although the physical mechanisms behind for various emerging NVMs are different. For PCRAM, writing is the primary wear mechanism: when injecting current into a volume of phase change material, thermal expansion and contraction degrades the electrode-storage contact [38]. While in MRAM, the cell damage during write operations mainly is triggered by particles and pin-holes introduced in process integration. Write endurance is usually measured as the number of writes performed before the cell cannot be programmed reliably. SRAM and DRAM both have endurance of about 10^{16} programming cycles [1], which are sufficient for use even in high-performance processing. The best reported write endurance for PCRAM, however, is only 10^9 based on a survey of PCRAM device and circuit prototypes published within the last five years [38]. And the best endurance test result of STT-RAM is less than 4×10^{12} programming cycles [39].

Besides the improvements on device material and process development, the most straightforward and effective approach is to reduce the time period that writing current applied on the memory cell. Some architectural level solutions have been proposed previously, such as early write termination [40] or partial writes [38]. Circuit design can also help out in many ways. For example, An accurate self-timing control scheme is necessary, which can stop providing writing current to memory cells once detecting successful set/reset operations. Because the damage on NVM material has an exponential relationship with the current/energy applied on it, one possible solution is smoothing the driving current during write operation and avoiding overshot on NVM materials. Here, how to design a write driver to provide a sleek but fast ramp-up curve is the tricky part. Another interesting alternative could be lowering the voltage on memory device to meet only the minimal current requirements. Then, how to overcome process variation and even utilize it to control driving current are two key challenges. Furthermore, for some applications that non-volatility is not a requirement (i.e. directly replace SRAM with PCRAM), we can even trade data retention with endurance by further reducing the energy pulse. Of course, the statically or dynamically fixing by using redundancy and ECC will keep useful. However, will the more complex ECC algorithms or bit-level redundancy be needed? This project will investigate these solutions and give convincing answers.

Multi-level cell (MLC) can effectively improve the integration density of memory by storing more than one bit information in a single memory device: n bits are represented by 2^n states of a storage device. MLC technology has achieved significant commercial success in NAND flash memory [41] and it has been explored in PCRAM [10,18], STT-RAM [42], and RRAM [43]. It can effectively improve the integration density of memory. However, the write endurance is also degraded due to the smaller resistance gap between two adjacent states.

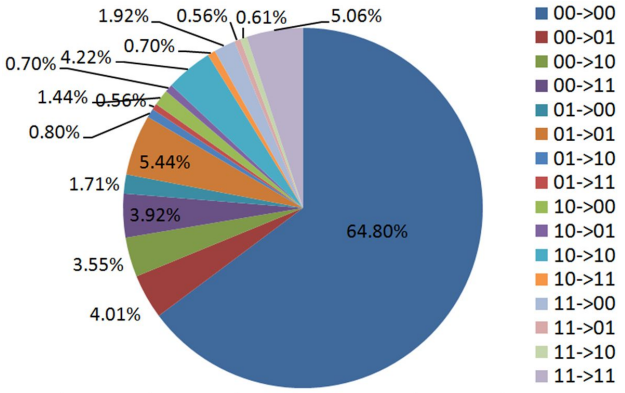

Figure 4: The transition distribution between the different values of MLC MRAM bit

Figure 4 shows the transition distribution between the different logic values of 2-bit MLC in an in-order microarchitecture. We noticed that most of transitions occur between the same values, and hence, there is no need to change resistance state at all. Therefore, "write-after-read" scheme, which conducts only the necessary transitions based on the values of the new data being written and the original data stored in the MLC bit, could be the most efficient way for energy saving and lifetime improvement. Furthermore, we observe that the resistance switching in MLC need follow specific sequence. For example, the free layer of the MTJ in an MLC MRAM has two magnetic domains whose magnetization directions can be switched separately. The magnetization direction of *soft domain* can be switched alone by a small current, while that of *hard domain* can be switched by only a large current which is always associated with the magnetization direction switching of soft domain. Corresponding to the four resistance states – $R00$, $R01$, $R10$, and $R11$ from low to high, an MLC MRAM cell may have total of $4! = 24$ encoding schemes for its four logic states – $L00$, $L01$, $L10$, and $L11$. As we stated above that the probability of MTJ breakdown has an exponential relationship with the current amplitude through it, the hard domain switching can induce more damage on MTJ material than the soft domain switching. Properly selecting the encoding scheme of logic vs. physical states to reduce the hard domain switches based on the transition distributions can further improve the write endurance and lifetime of MLC MRAM.

5.2 Process Variation-Tolerant Design

As the process technology scales, device parameter fluctuations induced by process variations such as line-edge roughnesses (LERs) and oxide thickness fluctuations (OTFs) have become critical issues in affecting the performance of devices [44]. Similar to any other memory manufactured in the scaled technologies, emerging nonvolatile memories also suffer from the large process variation. For example, MTJ resistance increases exponentially with the thickness of oxide barrier between two magnetic layers. It was reported in [45] that MTJ resistance increases by 8% when the thickness of oxide barrier changes from $14\mathring{A}$ to $14.1\mathring{A}$. Moreover, the MTJ resistance variation will be aggravated by the further reduction of oxide barrier thickness in scaled technologies. Besides oxide barrier thickness, MTJ resistance is also significantly affected by the large MTJ geometry variations.

5.2.1 Read Failure

Most of the emerging NVM technologies, e.g., MRAM and PCRAM, use device resistance as the data storage media. **Figure xxx(a)** illustrates a conventional voltage sensing scheme: Comparing the bit line voltage V_{BL} generated by the selected memory cell with a reference signal V_{REF} produced by the dummy cell. Ideally the resistance of the dummy cell should be set in the middle of the high and low resistance states (R_H and R_L) of the selected memory cell. When V_{BL} is higher than V_{REF}, the data storage device in the memory cell is in R_H state, and vice versa. Usually a dummy cell is shared by multiple memory bits to reduce overhead. In reality, process variation incurs the resistance distribution of data storage device in memory cell as well as the dummy cell. As illustrated **Figure xxx(b)**, when the resistance variation σ_R is large, the tails of R_H or/and R_L could be overlapped with R_{dummy} and lead to the false detection of the stored value. We called it as ***Read Failure***.

Read failure is a severe problem in STT-RAM design for two main constraints. (1) The difference between two resistance states of MTJ is fairly small: $\Delta R = R_H - R_L \approx 1000\Omega$ at 45nm technology node [46]; and (2) the MTJ resistance variation σ_R is relatively high because it is extremely difficult to control oxide barrier thickness within a small range of variation, i.e. $0.5\mathring{A}$ [47]. Besides the regular yield improvement techniques, such as redundant column/row and ECC (Error Correction Code), a self-reference read-out scheme could be another effective way to fix read-failure problem.

The basic idea of a self-reference reading is to compare the stored data in a memory cell with a reference value written to the same cell. By limiting the comparison within one single STT-RAM cell, the impact of bit-to-bit variation of MTJ resistance can be avoided. Previously some self-reference schemes were used in toggle-mode MRAM design [47,48]. We also successfully utilized it in STT-RAM design [49]. These schemes are all "destructive" because the original value in memory cell is wiped out when writing the reference value into MTJ, and has to be recovered at the end of the read operation. Obviously it prolongs read latency and introduces reliability issue.

In this project, we will work on a ***non-destructive self-reference*** methodology, which does not disturb the original data during read operations. The approach comes from the special R-I characteristic of MgO-based MTJ. As we can see in Figure 5, the MTJ current dependence of the high and the low resistance states are quite different: the current roll-off slope of high resistance is much steeper than that of low resistance. Therefore, we can sample the stored value of an MTJ twice by using two read currents I_{R1} and I_{R2} and compare the resistance difference $\Delta R = R1 - R2$. Obviously ΔR_H is pretty big, while ΔR_L is

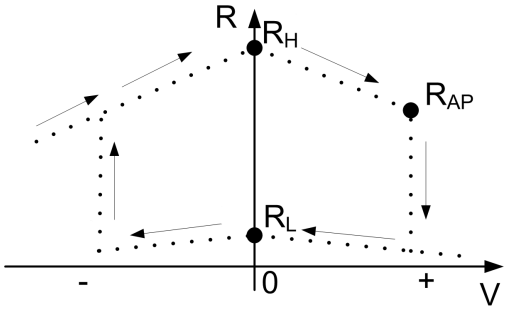

Figure 5: The static R-I curve of MgO-based MTJ. **HL: Modify Figure.**

close to '0'.

However, there are some uncertainties to realize this
approach. For example, how much is the sensing margin in the new read-out scheme after considering process variations? What type of sensing circuitry is more optimal? Will a new sense-amplifier (SA) design be necessary? How does it impact memory array structure? How much yield improvement can be achieved with the new scheme? Will this scheme be still valid when technology further scales down? In this proposal we will investigate these issues and exploring the solutions. Our target is to minimize the effect of process variation and to improve read speed.

5.2.2 dopant drifting in Memristor, read window change???

HL: Add new section here. Process has more impacts on memristor-based design, especially when memristor is used for a continuous data storage and detection.

5.3 Density Enhancement

Memory density is directly related to its capacity, and hence, reducing memory cell size and increasing density becomes an ultimate goal. In the past, technology scaling is always the biggest driving force to reduce single memory cell size by decreasing the pattern on chip. Process development plays an important role as well. For example, the charge storage materials of NAND Flash have gone through several generations to continue its scalability: from standard double polysilicon gate, to Silicon-Oxide-Nitride-Oxide-Silicon (SONOS), to bandgap engineered SONOS, and to $TaN/Al_2O_3/SiN/SiO_2$ (TaNOS) [50]. The emerge of new NVMs is another good example to show the power of technology. On top of it, we should note that cell structure and circuit design technique can also constraint or boost memory density.

5.3.1 MRAM and PCRAM

In a random access memory cell, usually an NMOS transistor is used as selection device (e.g. DRAM, MRAM and PCRAM) by connecting it in series with the data storage element. Such a cell structure needs three sets of terminals – word line (WL), bit line (BL) and source line (SL). The routing requirement and design rules determine that the minimal possible cell size is $12F^2$ [46]. Here, F represents the technology feature size.

The real memory size is also determined by ... The real cell size could grow when the storage device cannot fit into it or the select transistor need serve as driving device too.

5.3.2 RRAM and Memristor

Theoretically, the smallest memory cell is $4F^2$, which has only two terminals – one is horizonal (WL) and another is vertical (BL). The storage element is built at the cross-point of two metal wires, so it is called cross-point structure. RRAM can support data access in this structure by properly controlling the voltages applied on WL's and BL's. Moreover, the cross-point structure can grow in third dimension and forms an intra-die stacking structure. The memory storage cell is located in between any two adjacent metal layers which are used as interconnects. Within the same die size, the multiple memory layers further improve the memory density. Hence, RRAM is expected to replace NAND Flash memory as main storage in near future [1].

From design point of view, RRAM technologies can be divided into two operation types: unipolar switching and bipolar switching. Unipolar operation executes the programming/erasing by using short and long pulse, or by using high and low voltage with the same voltage polarity. Usually a diode is served as selection device (1D1R). The data in bipolar switching RRAM can be changed by short voltage/current pulses with opposite voltage polarity. For such memory structures, non-ohmic device (NOD) [51] is used to provide two-direction driving current as well as support process integration of cross-point structure. We call it as 1NOD-1R (See Figure 6).

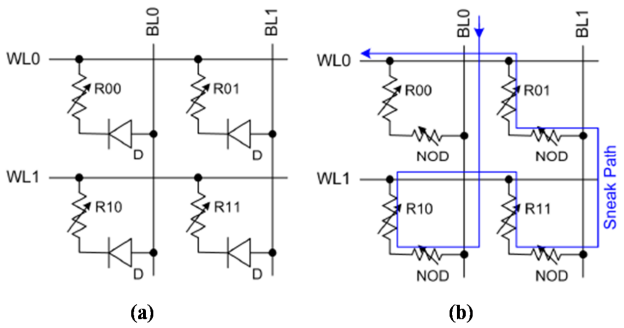

Figure 6: RRAM memory cell scheme. (a) 1D1R; (b) 1NOD-1R.

However, 1D1R and 1NOD-1R cell structures are facing on some design difficulties due to process limitation. Conceptually, NOD can be understood as two parallel connected diodes. Ideally, it turns on only when the voltage drop between the two terminals exceeds its threshold. However, the I-V characteristic curve of real device could be quite different. This results in sneak path which has three or more cells in series as shown in Figure 6(b). The sneak current can introduce disturbance on unintended cells during read, write and erase operations. Therefore, diode (P-N or Schottky) is more favorable as a selective element for RRAM array and intra-die stacking. However, it is extremely difficult to achieve the high quality diode with large I_{on}/I_{off} ratio (large forward current I_{on} and extremely small reverse current I_{off}) by using temperature limited BEOL (back end of line) process ($< 400°C$) [52].

Using bipolar PMC as the selective element. We propose to bipolar resistive switching devices as the selection device. Programmable-metallization-cell (PMC) could be a good candidate. PMC [53] is a promising bipolar RRAM technology, which is composed of two solid metal electrodes – relatively, one is inert and the other is electrochemically active. Between the two electrodes locates a thin electrolyte film. When a negative bias is applied to the inert electrode in programming operation (SET), metal ions in the electrolyte together with those flew from the positive active electrode can be reduced by the inert electrode. As a result, the metal ions form a small metallic "nanowire" between the two electrodes, which produces a low resistance. In erasing operation (RESET), a positive bias is applied on the inert electrode. Metal ions migrate back into the electrolyte and eventually to the negatively-charged active electrode. The "nanowire" is broken and the resistance increase back. The I-V curve is illustrated in Figure **??**(a). A higher voltage is required in RESET operation (V_r) than the one in SET operation (V_s).

Compared to diode or NOD, PMC based switch has two advantages – bipolar switching and large I_{on}/I_{off} ratio. Hence, the proposed scheme could be used in bipolar switching RRAM design with minimized sneak current. Although we have investigate the feasibility based on theoretical analysis, there are still a lot of unsolved issues. For example, how to control timing and applied voltage? What kind of peripheral circuitry floorplan will be optimal for the proposed RRAM design? And again, how will process variations affect the proposed RRAM scheme? In this project, we will address these circuit issues from both device and circuit point of views and explore the solutions.

5.4 Preliminary results and Collaborations:

Previously, we have already successfully utilized the destructive self-reference scheme in STT-RAM design [49]. The feasibility of the non-destructive self-reference scheme has been also discussed and analyzed in theory [54]. Add experience on SRAM design??

6 Task 3: Novel Applications

6.1 Memristor as novel sensing scheme

The device structure for temperature sensor is in Fig. 3a. It consists of a long spin-valve strip which includes two ferromagnetic layers: reference layer and free layer. The magnetization direction of reference layer is fixed by coupling to a pinned magnetic reference layer. The free layer is divided by a domain-wall into two segments that have opposite magnetization directions to each other. The device time domain resistance depends upon domain wall position as: , where and are the high and low resistance of the spin valve. is the spin valve length and is the domain wall position.

Domain wall velocity at finite temperature depends upon both spin torque excitation strength and thermal fluctuation magnitude. Fig. 4 shows the normalized domain wall velocity as a function of the normalized current density for different normalized thermal fluctuation magnitudes. Domain wall velocity increases as temperature increases. Temperature sensitive and insensitive regions can be observed. Curves with kneeling shapes are around critical current density, where the domain wall velocity is sensitive to thermal fluctuation magnitude. For temperature sensing, a biasing voltage pulse with constant magnitude is applied to the device. Resistance difference before and after voltage pulse is measured. This resistance difference is calibrated to sense temperature. Higher temperature results a bigger resistance dropping as shown in Figure 5.

The temperature sensing memristor is operated at a region where its electric behavior is sensitive to temperature change. This is achieved through a combination of temperature dependent domain wall mobility and the positive feedback between resistance and driving strength in memristor. The positive feedback between resistance and driving strength is a unique property of the memrisor. Memristor's resistance depends upon the integration of current/voltage excitation. For a constant voltage pulse driving, higher temperature results an increased domain wall moving distance. The increased domain wall moving distance results a smaller resistance. The smaller resistance results a higher driving current density, thus providing positive feedback to further increase domain wall distance. This positive feedback accelerates domain wall speed and reduces device resistance further for a constant voltage pulse driving. Solid curves on the Fig. 5 are the resistance changes for the proposed spintronic memristor at different temperatures. Dash lines are the resistance dropping for a non-memristive device without positive feedback between resistance and the integration of driving strength. The dash lines are equivalent to simulations with fixed driving current strength. It can be seen that positive feed back between resistance and driving strength in memristor significantly increases the temperature sensing margin.

6.2 Reconfigurable System

6.3 : Hybrid system with other emerging devices.

7 Related Work

In recently years, there have been active efforts on emerging NVM technologies. However, most of efforts were at process and device levels. Relatively, the architecture and system level analysis is less due to the lack of a high-level cache and memory model for emerging NVMs.

PCRAM. Compared to STT-RAM, PCM is even denser with an approximate cell area of $6 \sim 12F^2$ [1], where F is the feature size. In addition, phase change material has a key advantage of the excellent scalability within current CMOS fabrication methodology [12, 15–18]. Continue density improvement is the most important task for PCRAM process development. 2 and 4-bit MLC PCRAM material and the correponding write strategies were demonstrated by Nirshl et al. [19]. New process integration techniques, such as ultra-small lithography independent contact area [20] and unified 7.5nm dash-type confined cell [21], could also help enhance density. Reliability is the

major challenge in PCRAM process, which severely limits its applications. Researches on different angles have been done: Lacaita et al. discussed projected its impact on scaling [55], Shih et al described the mechanisms of retention loss in GST material [56], and Lavizzari et al presented the impact of transient effects [57]. Accordingly, many device models were built from reliability [58], low-frequency noise [59], statistical analysis [60] point of views. Those models mainly were dedicated to process and device, which cannot be borrowed by computer community.

Many PCRAM prototypes have been demonstrated in the past years. In 2007, a 1.5V 512KB embedded PCRAM in a 0.13μm CMOS by Hitachi [22] and a 512b diode-switch PCRAM in a 90nm CMOS by Samsung [23]. A year later, a 256Mb MLC PCRAM in a 90nm technology by STMicroelectronics [24]. Accordingly, a multi-level programming algorithm was developed and embedded into the chip, demonstrating 2b/cell feasibility. Very recently, a 45nm 1Gb 1.8V single-level cell (SLC) PCRAM was designed with 85ns random-access time and 9MB/s program throughput was demonstrated by Numonyx [26], and A 90nm 4Mb embedded PCRAM with 1.2V 12ns read access time and 1MB/s write throughput was made by STMicroelectronics [25]. In addition, The peripheral circuit design for high density diode-switch PCRAM was discussed in ISQED 2009 [46]. Diode-switch PCRAM was demonstrated in VLSI Symposium 2007 [61]

Discussions on endurance limitation were recently brought up to off-ship memories. Lee et al. proposed techniques to reduce the write accesses to PCM-based main memory to improve its endurance [**?**]. One of the techniques utilizes the dirty bits in L2 at the word granularity to check if a word has been updated since it was last fetched on-chip. A technique along a similar line for PCM memory at bit level was proposed by Zhou et al. [**?**]. In this technique, a memory row is first read out, then compared with the new data, and finally written back for those changed values. This technique can significantly save performance and energy by avoiding pre-write operations. These technologies, however, all incurred significant access performance degradation and cannot be directly used in on-chip cache structure.

MRAM. MRAM features non-volatility, fast access speed, zero standby power and high programming endurance [3,39]. The research on MRAM material and device mainly devoted on spin-torque based MTJ due to its better performance, higher density, and better scalability compared to the conventional MRAM [6,62–64]. Certainly, the yield improvement is an important topic in nanoscale devices. Miura et al. presented a SPRAM with synthetic ferrimagnetic free layer, which has high immunity to read disturbance and sufficient margin between read and write currents [65]. The MTJ structure with synthetic ferrimagnetic free layer can achieve a lower critical current density without degrading the thermal stability [66]. Very recently, a 2-bit MLC (Multi-level cell) MTJ device was reported in [42] for further density enhancement. Two-digit information – 00, 01, 10, and 11, are represented by four MTJ resistance states. The transitions between different MTJ resistance states can be realized by passing the spin-polarized currents with different amplitudes and/or directions.

A 4Kb STT-RAM using tailored MTJ design was fabricated by Sony in 0.18μm technology in 2005 [3]. The test chip demonstrated that STT-RAM is a prominent candidate for the next generation memory because of its high speed, low power and high scalability. In 2007, Kawahara et al. prototyped a larger 2Mb STT-RAM in 0.2μm technology [6]. This chip improves memory access latency by featuring an array scheme with bit-by-bit bidirectional current write and a prallelizing-direction current read. Recently, a even larger capacity – 32Mb MRAM prototype in 90nm technology was demonstrated by NEC [7]. A cell structure with 2 transistors and 1 magnetic tunneling junction (2T1MTJ) was adopted to improve access time to 12ns. Besides the SRAM-like array [4, 8, 9], other memory structures are also investigated by using MRAM/STT-RAM technology. In [67], Wang et. al. described a CAM structure based on conventional MRAM technology. In [68], Wu et. al. propsoed a novel STT-RAM read scheme with high sensing margin and illus-

trates a new CAM design. The possibility of applying STT-RAM in reconfigurable logic block for 3D-stacked reconfigurable spin processor was investigated [69].

A write disturbance fault (WDF) model for conventional MRAM was proposed by Su et al. [70]. The fault affects the data stored in MRAM cells due to excessive magnetic filed during a write operation. This should not be a problem to STT-RAM since it uses spin-polarized current to flip data. We have proposed a dynamic MTJ model with more accurate (transient) description for MTJ resistance switching [35]. Compared to highly conceptual fixed resistance used in traditional STT-RAM design flow, the dynamic model can help to reduce 20% pessimism in write time at TSMC $0.13\mu m$. The failure probability of STT-RAM cells due to parameter variations was considered and discussed in [46]. A model was proposed to predict memory yield and design optimization to minimize memory failures.

At architecture level, there are several recent efforts in using STT-RAM as an on-chip last level cache. Desikan et. al. conducted an architectural evaluation of on-chip conventional MRAM cache in a single micro-processor [71]. Dong et al. developed a delay and energy model for MRAM-based cache and conducted a detailed comparison between the cache with SRAM and STT-RAM technologies in terms of area, performance and energy in the context of 3D stacking [**?**]. Sun et al. extended the application of STT-RAM based cache to Chip Multiprocessor (CMP) and proposed new techniques to improve latency and to reduce write energy [72].

8 Education Plan

An academic job is not only to create knowledge but also to disseminate that knowledge to others both at the graduate and undergraduate levels. Education is an integral part of the PI's career development plan and is a supportive and inseparable part of the PI's research. It is the PI's belief that research and academic activities should be inextricably linked in a healthy academic environment. The PI envisions that students play an important role in the research program. Successful teaching and other forms of interaction with students will attract them to the research area, excite them to learn more about the ongoing research, and eventually contribute to the PI's research program. The interaction between academia and industry is also very important. The following sections present the objectives of the proposed educational plan.

8.1 Course Development and Teaching

- **Course module development**

  As computer engineering educators, we should not only preserve the historical domain of our discipline, but also expand it. Current standard curricula on VLSI design/computer architecture/embedded system design are still mainly oriented to *deterministic design paradigm*, giving none or little emphasis on the non-deterministic behaviors introduced by technology scaling or novel device. In stead of introducing a new course, **the major goal of the PI is to develop and disseminate course modules that complement or upgrade existing core courses, by introducing new development and challenges in the forthcoming probabilistic design paradigm**. These class modules (overheads, labs, and notes) on process variations and probabilistic design techniques, will easily upgrade and complement a variety of courses, including embedded system designs, computer architecture, VLSI circuits and systems, and design automation tools/methodologies. The course modules and class projects related to PVT variations will be developed to provide students with hands-on experience on statistical timing analysis and statistical optimization techniques. Some of the modules will be incorporated into undergraduate engineering courses and others will be more suitable for graduate-level courses:

- *Undergraduate courses.* The PI plans to revamp a senior-level course (CSE 477: VLSI Digital Circuits) by introducing new course modules, such as circuit-level process variation, new labs on SPICE simulation of process variation, and gate-level statistical timing analysis tools. The PI also plans to incorporate variation-aware micro-architecture design concepts, such as the Razor architecture [**?**], into a senior-level computer architecture course (CSE 431: Computer Organization and Design).
- *Graduate courses.* The PI introduced a new graduate level course (CSE 598C: Design of Reliable Power Efficient Systems) in his first semester on the faculty at Penn State. The new course already included the reliability issues caused by temperature variation and power supply noise variation. Another graduate-level course that the PI co-teaches is a research seminar course (CSE597D: Embedded System Design). The PI plans to develop and incorporate new modules on process variation as well as the new research outcomes from the CAREER research program for these courses, and make them available to other academic institutions through the WWW or CDs, so that they can be easily integrated into a variety of courses. In fact, some of the modules from the PI's course have been adopted by University of Minnesota (Prof. Antonia Zhai) and University of Connecticut (Prof. Yunsi Fei). The PI believes that the new modules will continue to benefit his colleagues at Penn State and other institutions.

- **Fostering Interaction with Industry**

  In teaching computer engineering courses, the PI believes in the clear need to present real-life example products and applications, so that students can understand the significance of what they are learning. For instance, in the past, the PI infused his industrial design experience into the classroom and discussed the real problems he encountered when working as a designer. In this education plan, the PI plans to invite his industry contacts, who are the experts in process variation (Dr. Kerry Bernstein from IBM and Dr. Tanay Karnik from Intel), to give guest lectures on how complex chips are designed and what biggest challenges the industry faces in the probabilistic design paradigm.
- **Bringing Research into the Classroom**.

  The PI views research and teaching as complementary and promotes this view in all the classes he teaches. For example, some projects from his graduate course involve both theory and implementation on new topics, and have led to conference quality papers [**?**, **?**, **?**]. The PI will propose related research topics as possible projects and the tools developed via the research plan will also be used in the classroom.

  The semiconductor industry is a fast growing and swiftly changing area. The PI believes that it is extremely important to keep the advanced-level graduate courses up-to-date with latest research papers and novel ideas. When the PI was at IBM, the company had a tradition of giving a review seminar to all employees after a major conference (such as DAC or ISSCC). The PI plans to borrow this idea and develop a graduate seminar course, in which the students will review the latest major design automation conferences and real-time embedded system conferences, such as DAC, ICCAD, and RTSS. The PI will guide the students to review the most significant papers from each conference, encouraging students to explore their interesting topics and discover potential research topics.
- **Striving for Teaching Excellence**

  The PI has worked very hard to improve his teaching effectiveness rapidly. He has consulted senior professors with numerous questions about teaching and signed up for the teaching seminars organized by the Penn State's graduate school. These efforts have been successful; for the first 3 years of teaching at Penn State, the PI received an average 6.03/7 rating for his teaching evaluation, which was higher than the departmental and college average (5.17/7 and 5.28/7,

respectively). The PI will keep using all resource available at PennState to improve his teaching. In particular, he will keep participating all activities provided by PennState's Schreyer Institute for Teaching Excellence (www.schreyerinstitute.psu.edu), including teaching luncheon, seminars, and workshops.

8.2 Multidisciplinary/Multi-institution/International Education Collaboration

The PI plans to investigate *collaborative teaching experiments* that can then be adopted by other universities. In fact, The PI has **already** made a plan with Carnegie Mellon University and University of Pittsburgh: The PI will work with *Prof. Rob Rutenbar* from CMU and *Prof. Alex Jones* from UPitt to organize a graduate-level course on design automation tools and algorithms in Fall 2006 (CSE 578: CAD Tools). This course will span design automation flow from high-level synthesis to physical synthesis. The course will be simultaneously offered at Penn State, CMU, and University of Pittsburgh through online course delivery system (WebEx). Lectures will originate from the different schools based on the topics to be covered.

Based on the experience and assessment from this design automation course, the PI plans to organize another graduate-level course on probabilistic design flow for MPSoC embedded system design, which complements the CAREER research plan. The course will involve Princeton University (Prof. Wayne Wolf on conventional embedded MPSoC design), North Carolina State University (Prof. Frank Mueller on embedded software and compiler design), and Northwestern University (Prof. Hai Zhou on statistical timing analysis and optimization). The PI will incorporate the latest research outcomes from this project. Students at PSU/Princeton/Northwestern/NCSU will also experiment with the tools developed as a part of this research.

This multi-institution education plan will not only provide a unique opportunity for students to learn from experts in other universities/areas but also promote collaborations among students in different schools by working together on course projects. Such remote collaboration is a critical skill in today's global economy, where many companies have offices throughout the world.

The PI also believes that the success of universities in the United States stems from their willingness to leverage the best talent around the world. The PI plans to foster the connections between PennState and other top universities in the world. In fact, the PI will spend 7 weeks during the summer of 2006 visiting top universities in Asia. He will spend 4 weeks at Tsinghua University in Beijing to teach a short course on embedded system design. He will then spend 2 weeks and 1 week at National Taiwan University and Hong Kong University of Science and Technology, respectively, to give seminars and explore research collaborations with these universities. He also plans to conduct an international teaching experiment with Tsinghua University by offering his graduate level course on embedded system designs to Tsinghua University's graduate curriculum.

8.3 Outreach and Broader Impact

Tutorials and Workshops: The PI also believes that it is important to share research findings with experts in related areas. Such activities can spawn inter-disciplinary and inter-university research collaborations. The PI has a good track record of presenting tutorials on his latest research outcome, together with other experts in the field. For example, **he has presented tutorials** in ASPLOS 2004 [**?**], ASPDAC 2005 [**?**], ISCA 2005 [**?**], ASICON 2005 [**?**], and will present in MICRO 2006 [**?**]. From past offerings of tutorials, the PI has found these tutorials to serve as a spark plug for drawing more researchers to start working on a particular research area by creating awareness of the problem's importance and by introducing tools to facilitate in solving the problem. The PI will continue this tradition in this program, and prepare **tutorials for the future embedded**

system conferences such as EMSOFT, ISSS+CODES, RTSS, or CASES, based on the new outcomes from this research. The PI has served as the tutorial chair for **EMSOFT 2005** and helped organized the conference. He also served in the **CASES 2006** program committee. In the future, the PI plans to organize a **workshop on probabilistic embedded system design**, since a workshop is a great aid to attract other researchers to exchange ideas in this important area.

Industrial Courses: University and industry interactions are very important and benefit each other. On the one hand, the class materials in university education need to be infused with the latest developments in the industry; on the other hand, professional engineers need continuing education and training to develop new specialized skills and keep up with the rapid changes in the industry. Penn State is part of the University-Industry-Government partnership called *The Technology Collaborative (TTC)* (www.techcollaborative.org), which focuses on research, training, and education issues related with system design. The PI is actively involved with their education programs and has offered courses to the local industry in the past through TTC. Based on his graduate level course (Design of Reliable Power Efficient Systems), the PI has developed a two-day short course on designing reliable power efficient systems for industrial engineers. The course was delivered twice (in Jan 2004 and May 2004) to industrial engineers in companies like IBM, Seagate, and ADC, via an online course delivery system (Webex) as well as local attendance. He was also invited by Synopsys Inc. to give a five-day short course to industrial engineers on designing reliable power efficient circuits. The PI plans to maintain a close relationship with industry and disseminate findings of the proposed research to industry practitioners, who in turn can incorporate these into real Embedded SoC designs.

8.4 Student Advising

- **Advice Webpage**. Currently the PI has four Ph.D. advisees and co-advisees, including one female student. The PI has created an advice webpage (www.cse.psu.edu/ỹuanxie/advice.htm), which is a collection of more than 100 useful links categorized as follows: (1) Ph.D. dissertation/research advice; (2) presentation advice; (3) technical writing advice; (4) technical reviewing advice; (5) Job hunting advice; and (6) English learning advice. These advice links were collected by the PI when he was a graduate student at Princeton University and was extremely helpful for the smooth completion of his Ph.D. study. The PI's advisees have found them very useful when they start their graduate study. The webpage has also benefited other faculty members' advisees and the PI has received much positive feedback.
- **Advising Under-represented Groups and Undergraduate Research**
  The Computer Science and Engineering disciplines have exhibited a growing gender gap [**?**, **?**]. Working close together with his mentor Dr. Mary Jane Irwin, who is very active in CRA-W and ACM-W, the PI has strived for the promotion of women and minority in engineering. Currently he has one female Ph.D. student, who has been involved in the preliminary work proposed in this program [**?**], and will be supported by this program if it is funded. The PI has encouraged her to participate PennState Women in Engineering Program (WEP), to attend CRA-W (Women in Computing Research Association)'s computer architecture summer school in 2006, and to attend DAC 2006 with ACM-W scholarship. He plans to recruit two minority undergraduate students through the Penn State WISER (Women in Science and Engineering Research) and MURE (Minority Undergraduate Research Experience) programs, with funding provided by Penn State. These two students can help develop software for this program. PennState's WEP program also organizes Engineering Camp for Girls and Girl Scout Saturdays every year. The PI plans to participate and design small projects for these students, to promote computer engineering among high school female students.

8.5 Outreach and Broader Impact

Tutorials and Workshops: Li believes that the communication between academia and industry is very important. In NANOARCH 2009, she organized a panel on **Emerging Technologies**, which brought industrial voices into emerging NVM research. She also gave a tutorial in Tsinghua University in 2008. Li will continue her effort, and prepare tutorials for the future device and circuit conferences such as DATE, ISQED, or DAC based on the new outcomes from this research.

9 Project Management and Industry Collaborations

The research team poses complementary skills required for the project. The PIs are well qualified for the proposed research with significant prior experience in various areas. The PI Prof. Li has 5-years industrial experience related to device modeling and circuit design with focus on emerging non-volatile memories, and just recently joined NYU-Poly as an assistant professor. The co-PI Prof. Xie's expertise span areas of VLSI and architecture, with extensive experience in architectures with emerging technologies, such as 3D architecture. The PIs will work in close coordination on different parts of this project. The integration of all these research components and tool will be a coordinated effort by all the investigators. The project is a three-year effort involving multiple PhD students. Li will lead the effort in the first year with 2 PhD students from NYU working with 1 PhD student from PSU on the circuit and architectural modeling in Task 1. In the second year, Xie will lead the effort in Task 2, with 2 PhD students from PSU and 1 student from NYU, to study architectural techniques using NVM technologies. In the final year, both PIs will work together with 1 PhD from each institute to study novel applications that leverage NVM technologies. Detailed project milestones are given in Figure 7.

	Year 1	Year 2	Year3
Task 1 (GRA1 & 2 & 3)	Modeling		
Task 2 (GRA 3 & 4 & 1)		Architecture	
Task 3 (GRA 3 & 4)			Application
# of Students	NYU: 2	NYU: 1	NYU:1
	PSU: 1	PSU: 2	PSU: 1

GRA1 and 2: NYU students, GRA3 &4: Penn State students

Figure 7: Project Management (The first student in each task would be the lead).

The PIs have a well-established collaboration in the past years, when the PI was still in Seagate, and published preliminary results on NVM architectures in DAC 2008 and HPCA 2009 [**?**, **?**]. The existing collaboration and preliminary results will allow rapid ramp-up for the proposed research. The two teams will coordinate with each other via weekly teleconferences and regular mutual visits (with only 4-hour driving between two institutes).

Industry Collaborations. By leveraging both PI's past industry experience and successful collaborations with companies, the project will be carried out in close collaboration with industrial partners from IBM, HP, Intel, Qualcomm, Seagate, ITRI, as well as with a partner from IMEC in Belgium (see attached supporting letters). The industrial collaborators will play important roles in the proposed project by enabling the acquisition of realistic data, discussion of the practicality of ideas, placement of students in internships and permanent positions, and eventually the transfer of the technologies. By working closely with researchers in industry, the PIs will be able to ensure that the proposed methodologies and tools are practical and have a real impact on industry.

10 Results from Prior NSF Support

Hai (Helen) Li recently just joined NYU-Poly as an assistant professor, after 5-years industrial experience in Qualcomm, Intel, and Seagate. She doesn't have any NSF grant yet.

Yuan Xie: The most related prior NSF grant is CCF-0903432 (ADAM: Architecture and Design Automation for 3D Multi-core Systems; 08/2009-07/2012; $480K). This project aims at developing architectural design techniques and design automation tools for future 3D multi-core architectures. Xie actively collaborates with industry in 3D IC design research (IBM, Qualcomm, Honda, and Seagate). He has published extensively in the 3D IC design and 3D architecture areas, covering various aspects, including 3D architecture [?,?,?,?,?,?,?,?,?,?] and 3D EDA tools [?,?,?,?,?,?,?,?].

One of the benefits for 3D integration technologies is the capability of enabling cost-effective heterogeneous integration, which makes it much more practical to integrate emerging NVM with CMOS logic circuits. Consequently, the research plan described in this proposal will complement and be synergistic with the ongoing project.

REFERENCES CITED

References

[1] International Technology Roadmap for Semiconductor, 2007.

[2] G. W. Burr, B. N. Kurdi, J. C. Scott, C. H. Lam, K. Gopalakrishnan, and R. S. Shenoty. Overview of candidate device technologies for storage-class memory. In *IBM Journal Research and Device*, volume 52, pages 449 – 464, 2008.

[3] M. Hosomi, H. Yamagishi, T. Yamamoto, K. Bessho, Y. Higo, K. Yamane, H. Yamada, M. Shoji, H. Hachino, C. Fukumoto, H. Nagao, and H. Kano. A novel nonvolatile memory with spin torque transfer magnetization switching: spin-ram. In *Proc. International Electron Device Meeting Tech. Dig.*, pages 459 – 462, 2005.

[4] M. Motoyoshi, I. Yamamura, W. Ohtsuka, M. Shouji, H. Yamagishi, M. Nakamura, H. Yamada, K. Tai, T. Kikutani, T. Sagara, K. Moriyama, H. Mori, C. Fukamoto, M. Watanabe, R. Hachino, H. Kano, K. Bessho, H. Narisawa, M. Hosomi, and N. Okazaki. A study for 0.18um high-density mram. In *IEEE VLSI Symposium on Technology*, pages 22 – 23, 2004.

[5] Y.K. Ha, J.E. Lee, H.-J. Kim, J.S. Bae, S.C. Oh, K.T. Nam, S.O. Park, N.I. Lee, H.K. Kang, U.-I. Chung, and J.T. Moon. Mram with novel shaped cell using synthetic anti-ferromagnetic free layer. In *VLSI Symposium on Technology*, pages 24 – 25, 2004.

[6] T. Kawahara et al. 2mb spin-transfer torque ram (spram) with bit-by-bit bidirectional current write and parallelizing-direction current read. In *Proc. IEEE International Solid-State Circuits Conference, Tech. Dig*, pages 480 – 617, 2007.

[7] H. Honjo S. Saito Y. Ito S. Miura Y. Kato K. Mori Y. Ozaki Y. Kobayashi N. Ohshima K. Kinoshita T. Suzuki K. Nagahara N. Ishiwata K. Suemitsu S. Fukami H. Hada T. Sugibayashi R. Nebashi, N. Sakimura and N. Kasai. A 90nm 12ns 32mb 2t1mtj mram. In *IEEE International Solid-State Circuits Conference (ISSCC)*, pages 462–463, 2009.

[8] T. W. Andre, J. J. Nahas, C. K. Subramanian, B. J. Garni, H. S. Lin, A. Omair, and Jr. W. L. Martino. A 4-Mb 0.18-μm 1T1MTJ toggle MRAM with balanced three input sensing scheme and locally mirrored unidirectional write drivers. *IEEE Jour. Of Solid-State Circuits*, 40(1):301–309, 2005.

[9] T. Kawahara, R. Takemura, K. Miura, J. Hayakawa, S. Ikeda, Y. M. Lee, R. Sasaki, Y. Goto, K. Ito, T. Meguro, F. Matsukura, H. Takahashi, H. Matsuoka, and H. Ohno. 2 Mb SPRAM (SPin-transfer torque RAM) with bit-by-bit bi-directional current write and parallelizing-direction current read. *IEEE Jour. of Solid-State Circuits*, 43(1):109–120, 2008.

[10] Ferdinando Bedeschi, Rich Fackenthal, Claudio Resta, Enzo Michele Donzand Meenatchi Jagasivamani, Egidio Cassiodoro Buda, Fabio Pellizzer, David W. Chow, Alessandro Cabrini, Giacomo Matteo Angelo Calvi, Roberto Faravelli, Andrea Fantini, Guido Torelli, Duane Mills, Roberto Gastaldi, and Giulio Casagrande. A Bipolar-Selected Phase Change Memory Featuring Multi-Level Cell Storage. *IEEE Journal of Solid-State Circuits*, 44(1):217–227, 2009.

[11] J. H. Oh, J. H. Park, Y. S. Lim, H. S. Lim, Y. T. Oh, J. S. Kim, J. M. Shin, and et al. Full integration of highly manufacturable 512mb pram based on 90nm technology. In *Proceedings of the IEEE International Electron Devices Meeting*, pages 2.6.1–2.6.4, 2006.

[12] A. Pirovano, A. L. Lacaita, A. Benvenuti, F. Pellizzer, S. Hudgens, , and R. Bez. Scaling analysis of phase-change memory technology. In *Proceedings of the IEEE International Electron Devices Meeting*, pages 29.6.1–29.6.4, 2003.

[13] S. Lai. Current status of the phase change memory and its future. In *Proceedings of the IEEE International Electron Devices Meeting*, pages 10.1.1–10.1.4, 2003.

[14] Y. C. Chen, C. T. Rettner, S. Raoux, G. W. Burr, S. H. Chen, R. M. Shelby, M. Salinga, and et al. Ultra-thin phase-change bridge memory device using gesb. In *Proceedings of the IEEE International Electron Devices Meeting*, pages 30.3.1–30.3.4, 2006.

[15] S.L. Cho et al. Highly scalable on-axis confined cell structure for high density pram beyond 256mb. In *Symposium on VLSI Technology Digest of Technical Papers*, pages 96–97, 2005.

[16] H.-S. P. Wong S. Kim. Generalized phase change memory scaling rule analysis. In *Non-Volatile Semiconductor Memory Workshop*, 2006.

[17] T. Lowrey S. Lai. Oum - a 180nm nonvolatile memory cell element technology for standalone and embedded applications. In *IEEE International Electron Devices Meeting (IEDM)*, pages 36.5.1–36.5.4, 2001.

[18] S. Raoux, G. W. Burr, M. J. Breitwisch, C. T. Rettner, Y.-C.Chen, R. M. Shelby, M. Salinga, and et al. Phase-change random access memory: A scalable technology. In *IBM Journal Research and Device*, volume 52, 2008.

[19] T. D. Happ G. W. Burr B. Rajendran M. H. Lee A. Schrott M. Yang M. Breitwisch C. F. Chen E. Joseph M. Lamorey R. Cheek S. H. Chen S. Zaidi S. Raoux Y. C. Chen Y. Zhu R. Bergmann H. L. Lung T. Nirschl, J. B. Phipp and C. Lam. Write strategies for 2 and 4-bit multi-level phase-change memory. In *IEEE International Electron Devices Meeting (IEDM)*, pages 461–464, 2007.

[20] D. S. Chao Y. C. Chen F. Chen C. W. Chen R. Yen M. J. Chen W. H. Wang T. C. Hsiao J. T. Yeh S. H. Chiou M. Y. Liu T. C. Wang L. L. Chein C. Huang N. T. Shih L. S. Tu D. Huang T. H. Yu M. J. Kao W. S. Chen, C. Lee and M. J. Tsai. A novel cross-spacer phase change memory with ultra-small lithography independent contact area. In *IEEE International Electron Devices Meeting (IEDM)*, pages 319–322, 2007.

[21] S. L. Cho H. G. An D. H. Kim I. S. Kim H. Park D. H. Ahn H. Horii S. O. Park U. I. Chung D. H. Im, J. I. Lee and J. T. Moon. A unified 7.5nm dash-type confined cell for high performance pram device. In *IEEE International Electron Devices Meeting (IEDM)*, pages 1–4, 2008.

[22] K. Osada A. Kotabe Y. Matsui N. Matsuzaki N. Takaura M. Moniwa T. Kawahara S. Hanzawa, N. Kitai. A 512kb embedded pram with 416kbs write throughput at 100μa cell write current. In *IEEE International Solid-State Circuits Conference (ISSCC)*, page 26.2, 2007.

[23] W-Y. Cho S. Kang B-G. Choi H-R. Oh C-S. Lee H-J. Kim J-M. Park Q. Wang M-H. Park Y-H. Ro J-Y. Choi K-S. Kim Y-R. Kim W-R. Chung H-K. Cho K-W. Lim C-H. Choi I-C. Shin D-E. Kim K-S. Yu C-K. Kwak C-H. Kim K-J. Lee, B. Cho. A 90nm 1.8v 512mb diode-switch pram with 266mb/s read throughput. In *IEEE International Solid-State Circuits Conference (ISSCC)*, page 26.1, 2007.

[24] C. Resta-E. Donze M. Jagasivamani E. Buda F. Pellizzer-D. Chow A. Fantini A. Calibrini-G. Calvi R. Faravelli G. Torelli D. Mills-R. Gastaldi G. Casagrande F. Bedeschi, R. Fackenthal. A multi-level-cell bipolar-selected phase-change memory. In *IEEE International Solid-State Circuits Conference (ISSCC)*, page 23.5, 2008.

[25] A. Pirola L. Marmonier M. Pasotti M. Borghi P. Mattavelli P. Zuliani1 L. Scotti G. Mastracchio F. Bedeschi R. Gastaldi R. Bez G. De Sandre, L. Bettini. A 90nm 4mb embedded phase-change memory with 1.2v 12ns read access time and 1mb/s write throughput. In *IEEE International Solid-State Circuits Conference (ISSCC)*, page 14.7, 2010.

[26] G. Barkley H. Giduturi S. Schippers D. Vimercati C. Villa, D. Mills. A 45nm 1gb 1.8v phase-change memory. In *IEEE International Solid-State Circuits Conference (ISSCC)*, page 14.8, 2010.

[27] L. O. Chua. Memristor - the missing circuit element. In *IEEE Trans. Circuit Theory*, volume CT-18, pages 507–519, 1971.

[28] J. M. Tour and T. He. The fourth element. In *Nature*, volume 453, pages 42–43, 2008.

[29] Dmitri B. Strukov, Gregory S. Snider, Duncan R. Stewart, and R. StanleyWilliams. The missing memristor found. In *Nature*, volume 453, pages 80–83, 2008.

[30] L. O. Chua. Memristive devices and systems. In *Proc. IEEE*, volume 64, pages 209–223, 1976.

[31] Yu. V. Pershin and M. Di Ventra. Spin memristive systems: Spin memory effects in semiconductor spintronics. In *Phys. Rev. B, Condens. Matter*, volume 78, page 113309, 2008.

[32] X. Wang et al. Spin memristor through spin-torque-induced magnetization motion. In *IEEE Electron Device Lett.*, volume 30, pages 294–297, 2009.

[33] Y. Chen and X. Wang. Compact modeling and corner analysis of spintronic memristor. In *IEEE/ACM International Symposium on Nanoscale Architectures 2009 (Nanoarch09)*, pages 7–12, 2009.

[34] David Wang, Brinda Ganesh, Nuengwong Tuaycharoen, Katie Baynes, Aamer Jaleel, and Bruce Jacob. DRAMsim: A memory-system simulator. *SIGARCH Computer Architecture News*, 33(4):100–107, 2005.

[35] Y. Chen, X. Wang, H. Li, H. Liu, and D. Dimitrov. Design margin exploration of spin-torque transfer ram (spram). In *International Symposium on Quality Electronic Design*, pages 684–690, 2008.

[36] http://www.synopsys.com.

[37] Spintronic memristors, http://www.spectrum.ieee.org/semiconductors/devices/spintronic-memristors/0.

[38] Benjamin Lee, Engin Ipek, Onur Mutlu, and Doug Burger. Architecting phase change memory as a scalable DRAM alternative. In *The 36th International Symposium on Computer Architecture (ISCA)*, 2009.

[39] Z. Diao, Z. Li, S. Wang, Y. Ding, A. Panchula, E. Chen, L.-C. Wang, and Y. Huai. Spin-transfer torque switching in magnetic tunnel junctions and spin-transfer torque random access memory. *Journal of Physics: Condensed matter*, 19(16):165209, 2007.

[40] Ping Zhou, Bo Zhao, Jun Yang, and Youtao Zhang. A durable and energy efficient main memory using phase change memory technology. In *The 36th International Symposium on Computer Architecture*, 2009.

[41] Jong-Ho Park, Sung-Hoi Hur, Joon-Hee Leex, Jin-Taek Park, Jong-Sun Sel, Jong-Won Kim, Sang-Bin Song, Jung-Young Lee, Ji-Hwon Lee, Suk-Joon Son, Yong-Seok Kim, Min-Cheol Park, Soo-Jin Chai, Jung-Dal Choi, U. In Chung, Joo-Tae Moon, Kyeong-Tae Kim, Kinam Kim, and Byung-Il Ryu. 8 Gb MLC (multi-level cell) NAND flash memory using 63 nm process technology. In *IEEE International Electron Devices Meeting (IEDM)*, pages 876 – 876, 2004.

[42] X. Lou, Z. Gao, D. V. Dimitrov, and M. X. Tang. Demonstration of multilevel cell spin transfer switching in mgo magnetic tunnel junctions. *Applied Physics Letter*, 93:242502, 2008.

[43] I.G. Baek, D.C. Kim, M.J. Lee, H.J. Kim, E.K. Yim, M.S. Lee, J.E. Lee, S.E. Ahn, S. Seo, J.H. Lee, J.C. Park, Y.K. Cha, S.O. Park, H.S. Kim, I.K. Yoo, U.In Chung, J.T. Moon, and B.I. Ryu. Multi-layer cross-point binary oxide resistive memory (OxRRAM) for post-NAND storage application. In *IEEE International Electron Devices Meeting (IEDM)*, pages 750 – 753, 2005.

[44] A. Asenov, S. Kaya, and A.R. Brown. Intrinsic parameter fluctuations in decananometer mosfets introduced by gate line edge roughness. *IEEE Transactions on Electron Devices*, 50:1254 – 1260, 2003.

[45] S. Tehrani et al. Recent developments in magnetic tunnel junction mram. In *IEEE Trans. Magn.*, volume 36, pages 2752–2757, 2000.

[46] H. Li and Y. Chen. An overview of nonvolatile memory technology and the implication for tools and architectures. In *Design, Automation and Test in Europe Conference and Exhibition*, pages 731–736, 2009.

[47] Gitae Jeong, Wooyoung Cho, S. Ahn, Hongsik Jeong, Gwanhyeob Koh, Youngnam Hwang, and K. Kim. A 0.24μm 2.0-V 1T1MTJ 16-kb nonvolatile magnetoresistance RAM with self-reference sensing scheme. In *IEEE Jour. of Solid-State Circuits*, volume 38, pages 1906–1910, 2003.

[48] H. Tanizaki. A high-density and high-speed 1t-4mtj mram with voltage offset self-reference sensing scheme. In *Proc. IEEE Asian Solid-State Circuits Conference*, pages 303 – 306, 2006.

[49] Spin-transfer torque memory self-reference read scheme.

[50] Chih-Yuan Lu, Kuang-Yeu Hsieh, and Rich Liu. Future challenges of flash memory technologies. *Microelectronic Engineering*, 86(3):283–286, 2009.

[51] Non-ohmic device using tio2.

[52] Magic pmc switch fabrication method and its application as selective element for high density cross bar memory arrays.

[53] M.N. Kozicki, M. Balakrishnan, C. Gopalan, C. Ratnakumar, and Mitkova. Programmable metallization cell memory based on ag-ge-s and cu-ge-s solid electrolytes. In *Non-Volatile Memory Technology Symp.*, pages 83–89, 2005.

[54] Spin-transfer torque memory non-destructive self-reference read.

[55] A. L. Lacaita and D. Ielmini. Reliability issues and scaling projections for phase change non volatile memories. In *IEEE International Electron Devices Meeting (IEDM)*, pages 157–160, 2007.

[56] B. Rajendran M. H. Lee R. Cheek M. Lamorey M. Breitwisch Y. Zhu E. K. Lai C. F. Chen E. Stinzianni A. Schrott E. Joseph R. Dasaka S. Raoux H. L. Lung Y. H. Shih, J. Y. Wu and C. Lam. Mechanisms of retention loss in ge¡inf¿2¡/inf¿sb¡inf¿2¡/inf¿te¡inf¿5¡/inf¿-based phase-change memory. In *IEEE International Electron Devices Meeting (IEDM)*, pages 1–4, 2008.

[57] D. Sharma S. Lavizzari, D. Ielmini and A. L. Lacaita. Transient effects of delay, switching and recovery in phase change memory (pcm) devices. In *IEEE International Electron Devices Meeting (IEDM)*, pages 1–4, 2008.

[58] D. Sharma D. Ielmini, S. Lavizzari and A. L. Lacaita. Physical interpretation, modeling and impact on phase change memory (pcm) reliability of resistance drift due to chalcogenide structural relaxation. In *IEEE International Electron Devices Meeting (IEDM)*, pages 939–942, 2007.

[59] A. Calderoni L. Larcher P. Pavan P. Fantini, G. Betti Beneventi and F. Pellizzer. Characterization and modelling of low-frequency noise in pcm devices. In *IEEE International Electron Devices Meeting (IEDM)*, pages 1–4, 2008.

[60] E. Varesi A. Pirovano D. Mantegazza, D. Ielmini and A. L. Lacaita. Statistical analysis and modeling of programming and retention in pcm arrays. In *IEEE International Electron Devices Meeting (IEDM)*, pages 311–314, 2007.

[61] Y. Zhang et al. An intergrated phase change memory cell with ge nanowire diode for cross-point memory. In *Proc. of Symposium on VLSI Technology Digest of Technical Papers*, 2007.

[62] P. Srivastava S. Salahuddin, D. Datta and S. Datta. Quantum transport simulation of tunneling based spin torque transfer (stt) devices: Design trade offs and torque efficiency. In *IEEE International Electron Devices Meeting (IEDM)*, pages 121–124, 2007.

[63] C. Horng Q. Chen P. Sherman S. Le S. Young K. Yang H. Yu X. Lu W. Kula T. Zhong R. Xiao A. Zhong G. Liu J. Kan J. Yuan J. Chen R. Tong J. Chien-T. Torng D. Tang P. Wang-M. Chen S. Assefa M. Qazi-J. DeBrosse M. Gaidis S. Kanakasabapathy-Y. Lu J. Nowak E. O'Sullivan-T. Maffitt J. Z. Sun R. Beach, T. Min and W. J. Gallagher. A statistical study of magnetic tunnel junctions for high-density spin torque transfer-mram (stt-mram). In *IEEE International Electron Devices Meeting (IEDM)*, pages 1–4, 2008.

[64] T. Kai T. Nagase E. Kitagawa M. Yoshikawa K. Nishiyama T. Daibou M. Nagamine M. Amano S. Takahashi M. Nakayama N. Shimomura H. Aikawa S. Ikegawa S. Yuasa K. Yakushiji H. Kubota A. Fukushima M. Oogane-T. Miyazaki T. Kishi, H. Yoda and K. Ando. Lower-current and fast switching of a perpendicular tmr for high speed and high density spin-transfer-torque mram. In *IEEE International Electron Devices Meeting (IEDM)*, pages 1–4, 2008.

[65] K. Miura, T. Kawahara, R. Takemura, J. Hayakawa, S. Ikeda, R. Sasaki, H. Takahashi, H. Matsuoka, and H. Ohno. A novel SPRAM (SPin-transfer torque RAM) with a synthetic ferrimagnetic free layer for higher immunity to read disturbance and reducing write-current dispersion. In *IEEE VLSI Symposium on Technology*, pages 234 – 235, 2007.

[66] M. Durlam, P. J. Naji, A. Omair, M. DeHerrera, J. Calder, J. M. Slaughter, B. N. Engel, N. D. Rizzo, G. Grynkewich, B. Butcher, C. Tracy, K. Smith, K. W. Kyler, J. J. Ren, J. A. Molla, W. A. Feil, R. G. Williams, and S. Tehrani. A 1-Mbit MRAM based on 1T1MTJ bit cell integrated with copper interconnects. *IEEE Journal of Solid-State Circuits*, 38(5):769–773, 2003.

[67] W. Wang and Z. Jiang. Magnetic content addressable memory. *IEEE Trans. on Magnetics*, 43(6):2355–2357, June 2007.

[68] W. Xu, T. Zhang, and Y. Chen. Spin-transfer torque magnetoresistive content addressable memory (cam) cell structure design with enhanced search noise margin. In *IEEE Int. Symp. on Circuits and Systems (ISCAS)*, pages 1898–1901, 2008.

[69] H. Hasegawa K. Miura T. Fukushima S. Ikeda T. Tanaka H. Ohno M. Sekikawa, K. Kiyoyama and M. Koyanagi. A novel spram (spin-transfer torque ram)-based reconfigurable logic block for 3d-stacked reconfigurable spin processor. In *IEEE International Electron Devices Meeting (IEDM)*, pages 1–3, 2008.

[70] C.-L. Su, C.-W. Tsai, C.-W. Wu, C.-C. Hung, Y.-S. Chen, D.-Y. Wang, Y.-J. Lee, and M.-J. Kao. Write Disturbance Modeling and Testing for MRAM. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 16(3):277–288, 2008.

[71] R. Desikan, C. R. Lefurgy, S. W. Keckler, and D. Burger. On-chip MRAM as a high-bandwidth low-latency replacement for DRAM physical memories. http://www.cs.utexas.edu/ftp/pub/techreports/tr02-47.pdf, 2002.

[72] Y. Xie J. Li G. Sun, X. Dong and Y. Chen. A novel architecture of the 3d stacked mram l2 cache for cmps. In *14th International Symposium on High-Performance Computer Architecture (HPCA)*, pages 239–249, 2009.