Birla Institute of Technology and Science Pilani, Pilani Campus

Analog Assignment

Under the
Guidance of
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By

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2019B4A3PS0456P

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2020A3PS0460P

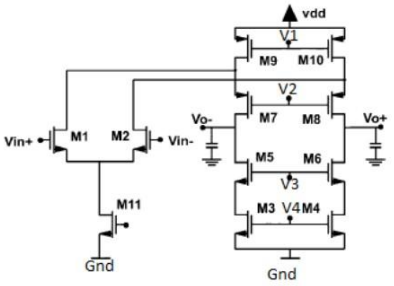
Introduction

The project aims to design a cascode operational amplifier with given specifications. Folded cascode operational amplifier, compared to the ordinary operational amplifier, is a high gain, a single-pole operational amplifier with large output swing, because compared to two stage operational amplifier or multi stage operational amplifier, the biggest advantage of single pole amplifiers is that the phase margin is very high and stable.
The schematic and simulations have been performed using LTSpice using TSMC 180nm technology.

Problem Statement

Q.71 requires us to design a folded Cascode OPAMP as shown in the figure

Q71. Design a folded Cascode OPAMP as shown in figure;



a) Analysis of all equations of your design, with a systematic derivation of all transistors W/L ratios and spectre simulation of circuit for the following specifications.
   i) UGB ≥ 300 MHz
   ii) Power Dissipation ≤ 1mW
b) Show a biasing circuitry to bias all the voltages in your design (except the input).
c) Calculate and plot the following parameters for your OPAMP: DC gain, Bode plot for AC gain and phase, ICMR plot, slew rate, Output voltage swing differential (dc + Transient), power consumption, and input and output offset voltage.

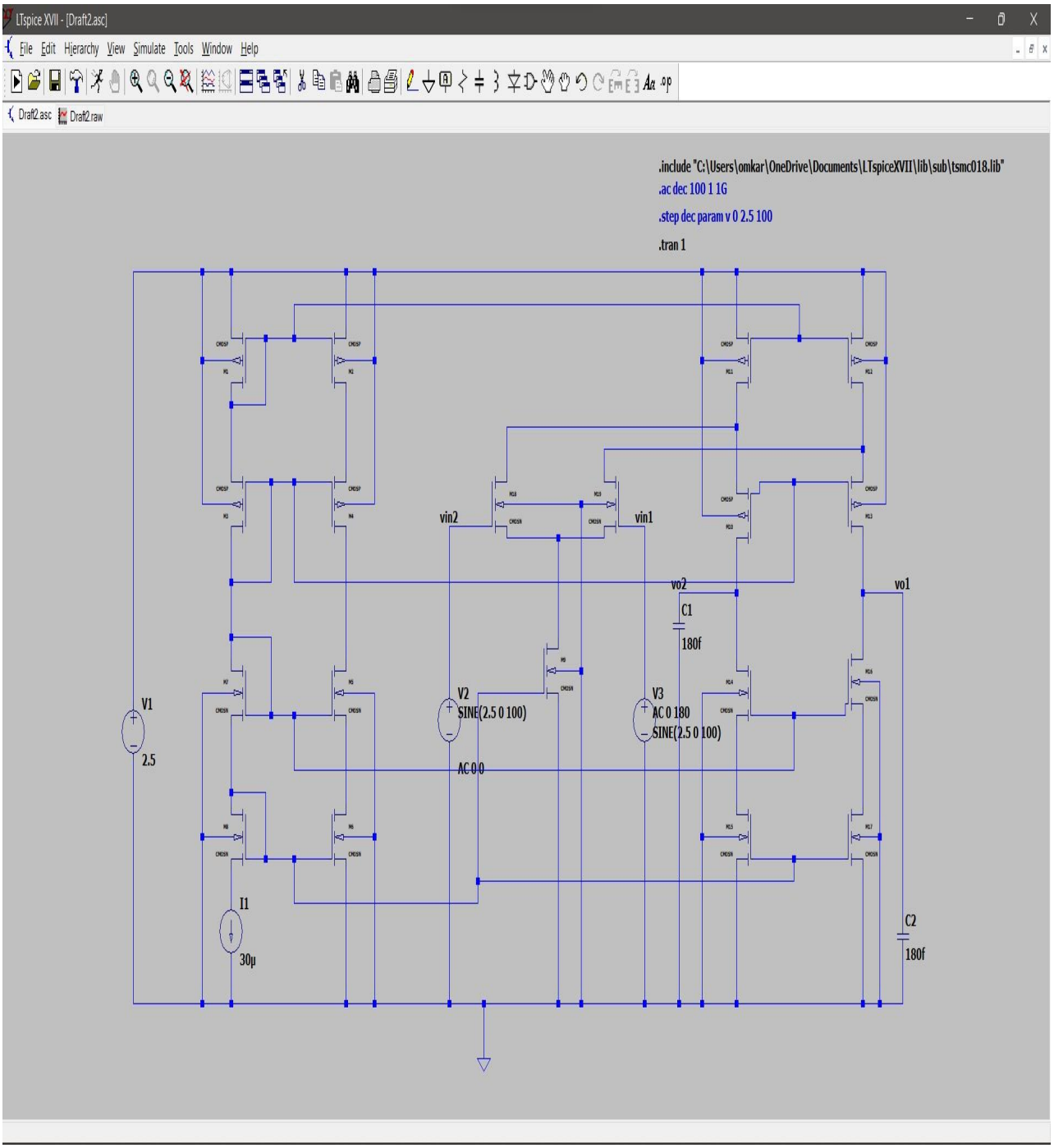
Specifications

	Values
Technology	180nm
V_{DD}	2.5V
C_L	180fF
L	1u
Reference Current	30uA
Power Dissipation	0.8925mW

Calculations

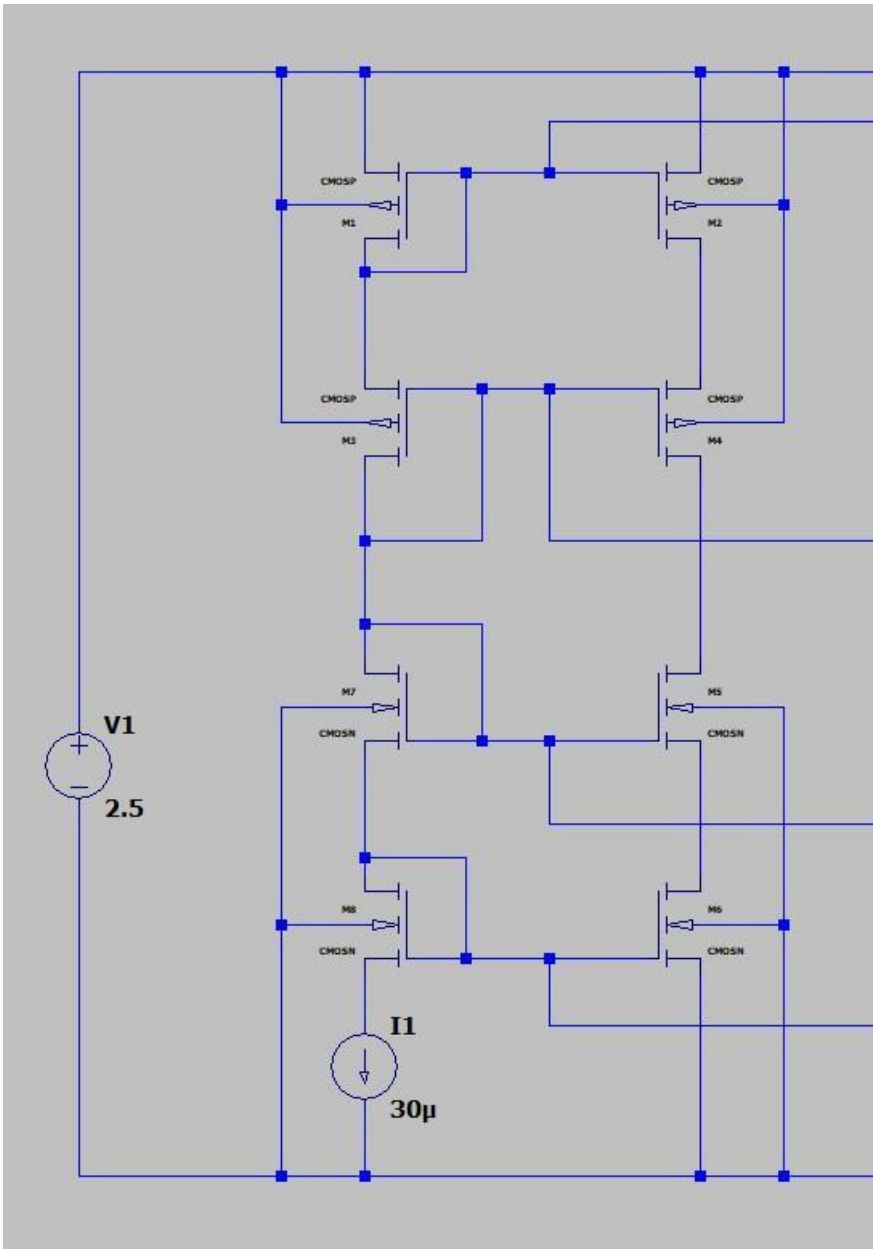
The design used requires four different biasing points. The biasing circuit has been designed to provide these. Two biasing points are for NMOS bias and two for PMOS bias. The design used requires four different biasing points. The biasing circuit has been designed to provide these. Two biasing points are for NMOS bias and two for PMOS bias. After a sequence of manual calculations and adjusting W/L ratios of the MOSFETs a suitable value of current was chosen such that all MOSFETs are in saturation and UGB requirements are met.

Schematic


LTspice XVII - [Draft2.asc]
File Edit Hierarchy View Simulate Tools Window Help
Draft2.asc Draft2.raw
.include "C:\Users\omkar\OneDrive\Documents\LTspiceXVII\lib\sub\tsmc018.lib"
.ac dec 100 1 1G
.step dec param v 0 2.5 100
.tran 1
vin2
vin1
vo2
vo1
C1
180f
V1
2.5
V2
SINE(2.5 0 100)
AC 0 0
V3
AC 0 180
SINE(2.5 0 100)
I1
30µ
C2
180f

Biasing Circuitry:

This part of the schematic shows the biasing circuitry to bias all the voltages in our design (excluding input voltages)



Parameters

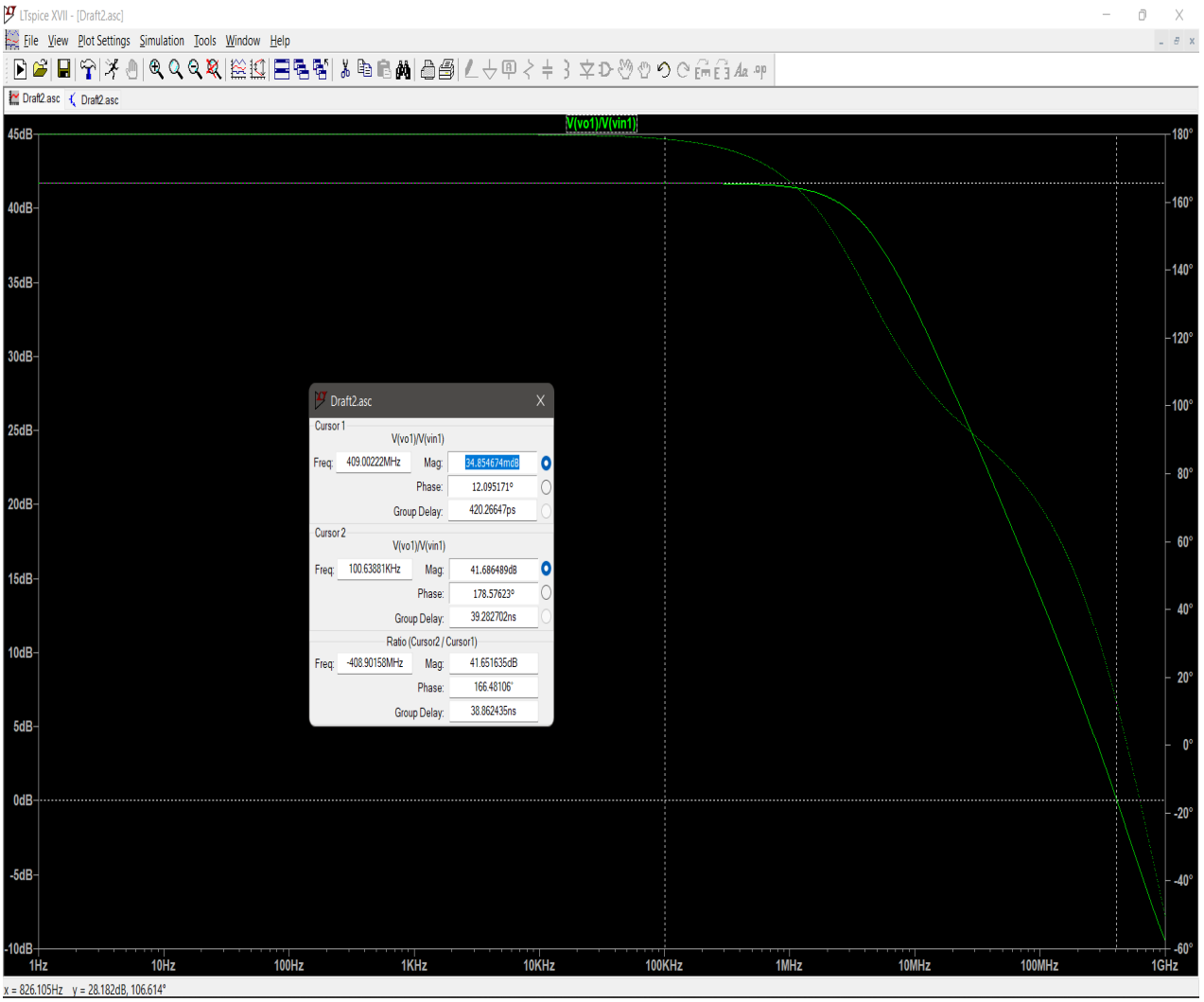
MOSFET	W	L	W/L
M1	43 μm	1μm	43
M2	43 μm	1μm	43
M3	37.019 μm	1μm	37.019
M4	37.019 μm	1μm	37.019
M5	9.25 μm	1μm	9.25
M6	30 μm	1μm	30
M7	9.25 μm	1μm	9.25
M8	30 μm	1μm	30
M9	240 μm	1μm	240
M10	21 μm	1μm	21
M11	215 μm	1μm	215
M12	215 μm	1μm	215
M13	21 μm	1μm	21
M14	16 μm	1μm	16
M15	30 μm	1μm	30
M16	16 μm	1μm	16
M17	30 μm	1μm	30
M18	30 μm	1μm	30
M19	30 μm	1μm	30

DC gain & Bode Plot

Gain = **41.69dB**

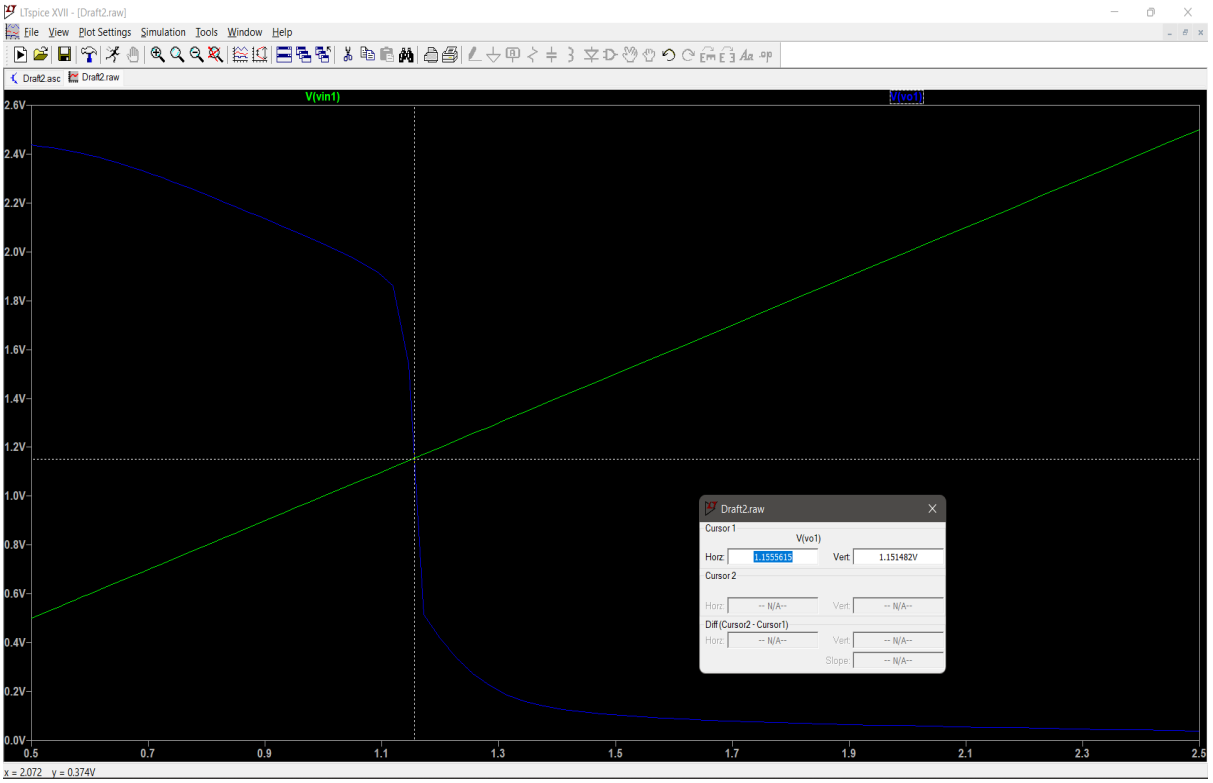
Unity Gain Bandwidth = **409MHz**

Phase margin = **12 degrees**



From Cursor 1, we can see that the Unity Gain Bandwidth (UGB) comes out to be a value of **409MHz,** which satisfies the requirement of greater than **UGB > 300MHz.**

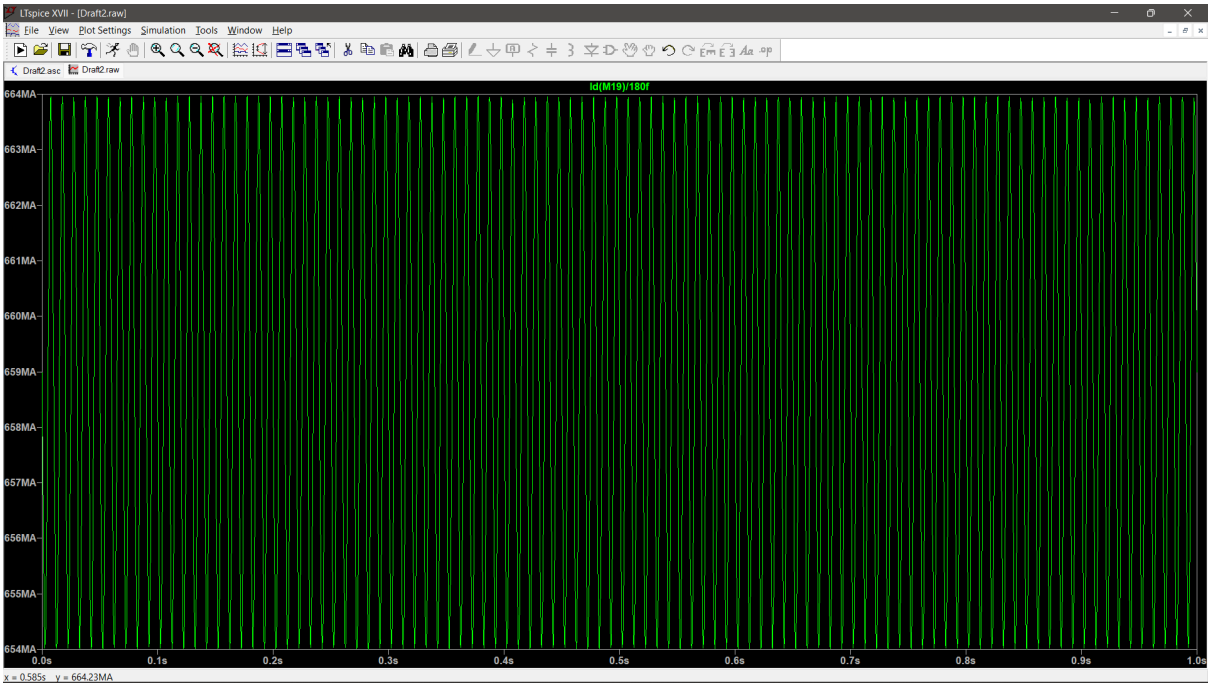
ICMR



ICMR = **1.151V**

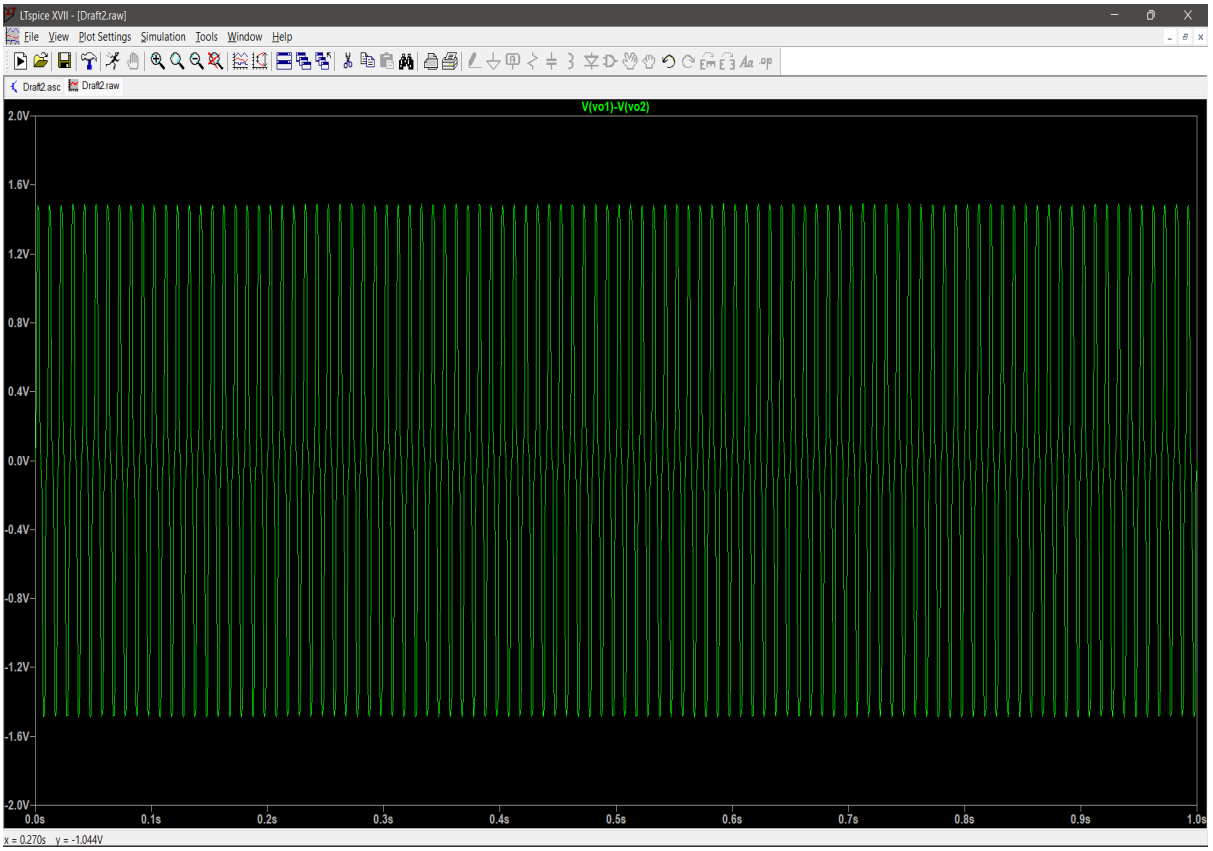
Slew Rate

Slew Rate = Id(M19) / C(Load) = **663.29 V/µs**

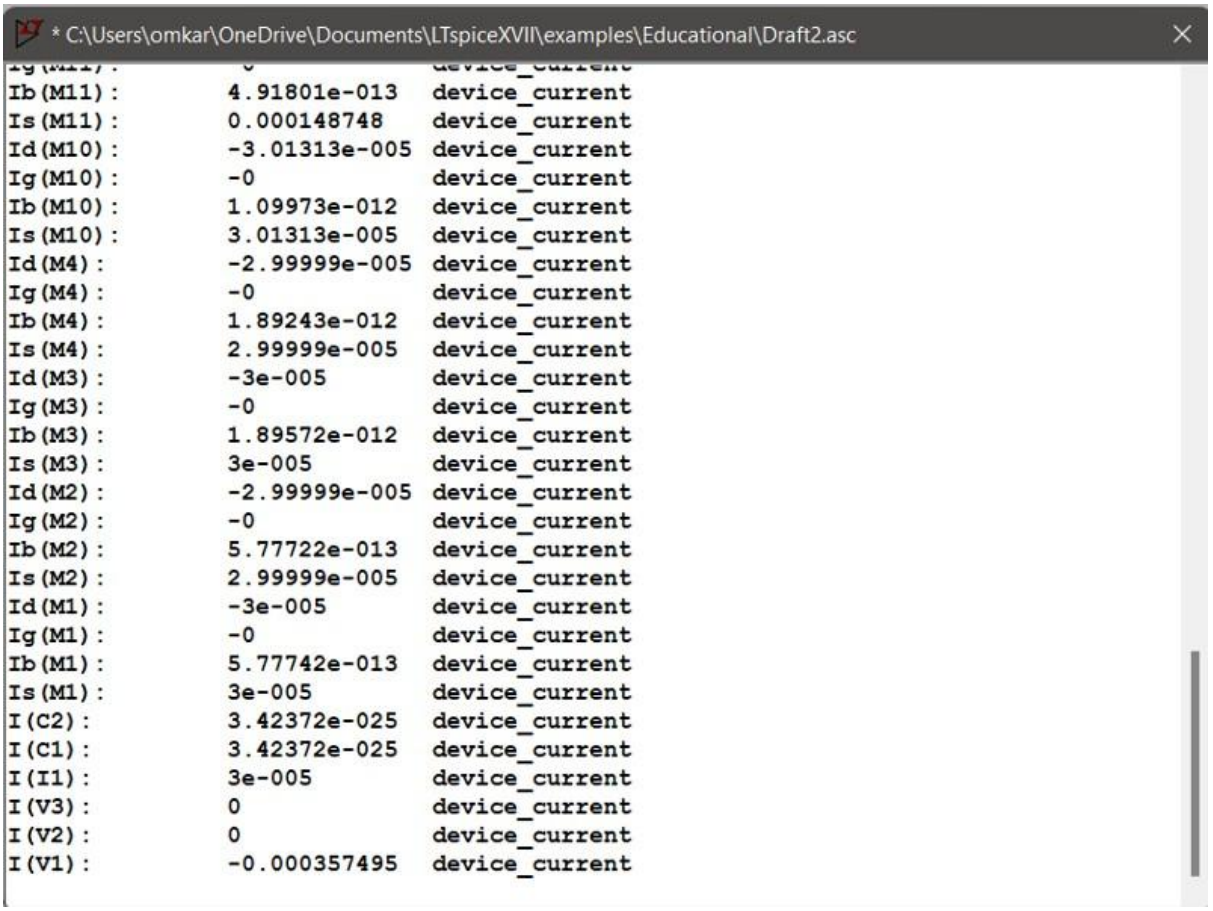


Output voltage swing differential (DC + transient)

Swing = 2.98V =**5.96V (Differential)**



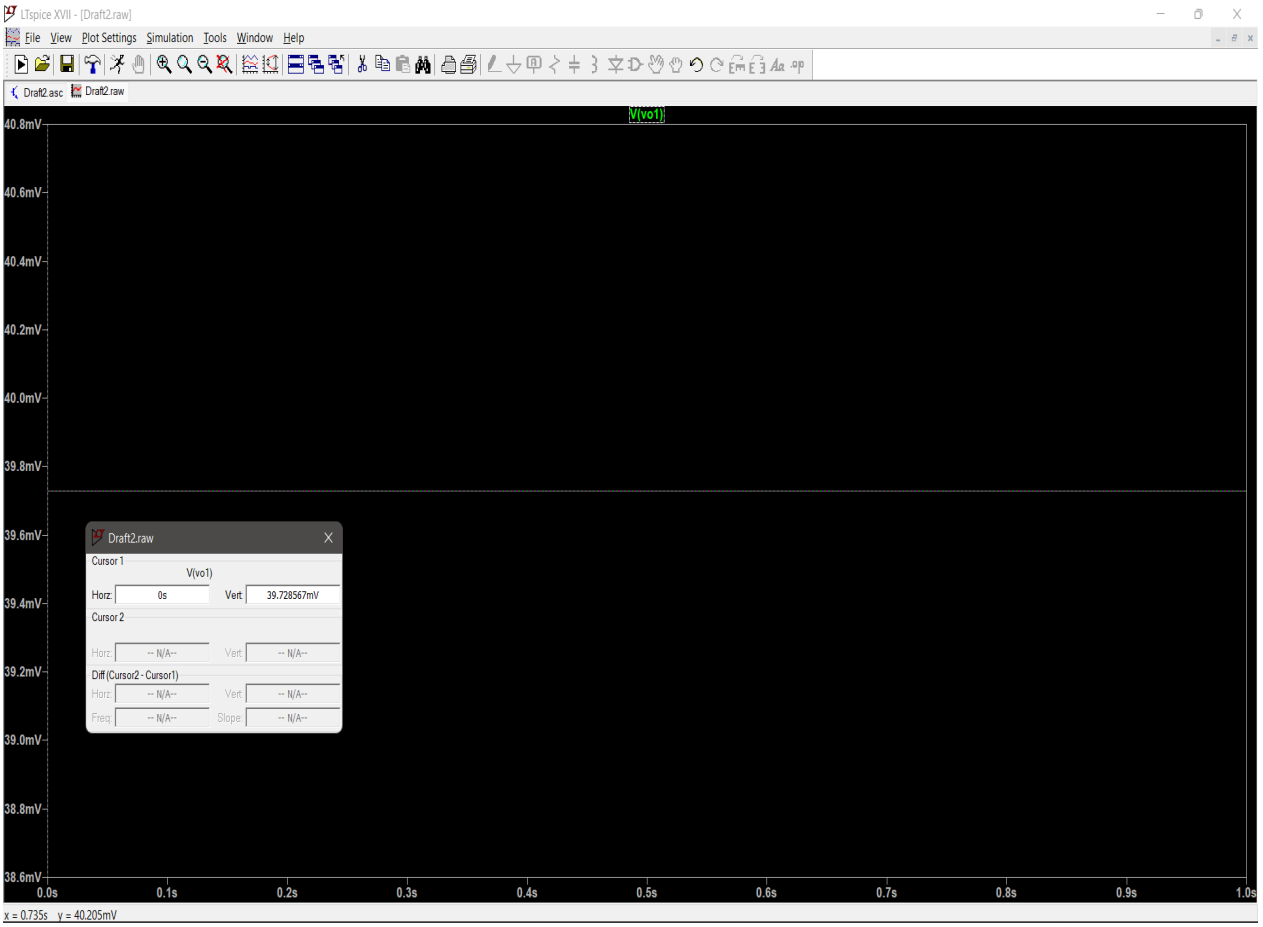
Power Consumption



From here, we know that **I(V1) = 0.000357A.**

Power = Vdd * Itotal = 2.5V * 0.357mA = **0.8925mW**

Input and output offset voltage value



Output offset voltage (as plotted) = **39.73mV**

Results

Parameter	Specification	Value (Found)
Output Offset Voltage	-	39.73mV
ICMR	-	1.151V
Power Dissipation	≤ 1mW	0.8925mW
D.C Gain	-	41.69dB
Slew Rate(V/μs)	-	663.29 V/μs
Differential Voltage Swing	-	5.96V
Unity Gain Bandwidth	>300Mhz	409MHz
Input Offset Voltage	-	0

Conclusion

We conclude that we were able to successfully obtain a design of a folded cascode operational amplifier adhering to the given constraints of unity gain bandwidth and power consumption, along with an explanation of the calculations and graphical depictions of all parameters stated such as Gain & Bode Plot, Slew Rate, ICMR, Input and Output Offset Voltage, Differential Voltage Swing and Power Dissipation.

Challenges and Innovations

When building the architecture of an OPAMP, great attention must be given to reduce power usage. When designing the architecture, the model's efficiency must be taken into consideration. To improve the architecture, the PMOS/NMOS transistors must frequently be realigned. The most ideal architecture was selected following extensive testing for accuracy and efficiency using a variety of various architectures. The folded cascode operational amplifier architecture used today has been enhanced in every way.