Birla Institute of Technology and Science Pilani
Pilani Campus

Assignment 1

Realization of a Logic Function using CPL Logic Style

Under the Guidance of
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By

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TASK-I

Realization of a logic function X = = [(A. B.F + (B+D.E.F) + H)]' using Complementary Pass Transistor Logic Style (CPL) having load capacitance of 200fF, using a minimum number of transistors.

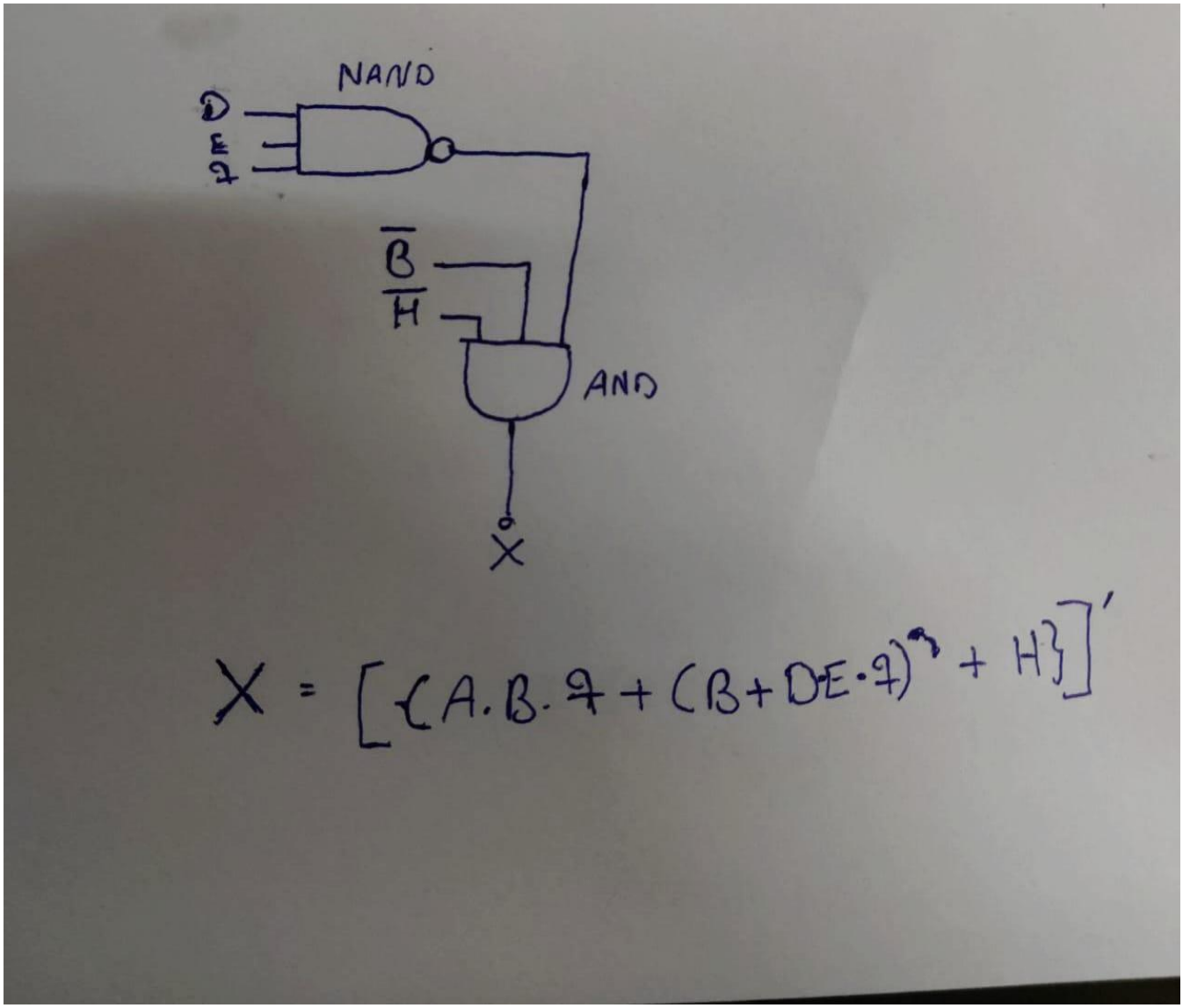


Fig. 1 Design of the Boolean Expression Realization

The Truth Table of the Expression

F= [(A. B.F + (B+D.E.F) + H)]’

a	b	d	e	f	h	Output
0	0	0	0	0	0	1
0	0	0	0	0	1	0
0	0	0	0	1	0	1
0	0	0	0	1	1	0
0	0	0	1	0	0	1
0	0	0	1	0	1	0
0	0	0	1	1	0	1
0	0	0	1	1	1	0
0	0	1	0	0	0	1
0	0	1	0	0	1	0
0	0	1	0	1	0	1
0	0	1	0	1	1	0
0	0	1	1	0	0	1
0	0	1	1	0	1	0
0	0	1	1	1	0	0
0	0	1	1	1	1	0
0	1	0	0	0	0	0
0	1	0	0	0	1	0
0	1	0	0	1	0	0

0	1	0	0	1	1	0
0	1	0	1	0	0	0
0	1	0	1	0	1	0
0	1	0	1	1	0	0
0	1	0	1	1	1	0
0	1	1	0	0	0	0
0	1	1	0	0	1	0
0	1	1	0	1	0	0
0	1	1	0	1	1	0
0	1	1	1	0	0	0
0	1	1	1	0	1	0
0	1	1	1	1	0	0
0	1	1	1	1	1	0
1	0	0	0	0	0	1
1	0	0	0	0	1	0
1	0	0	0	1	0	1
1	0	0	0	1	1	0
1	0	0	1	0	0	1
1	0	0	1	0	1	0
1	0	0	1	1	0	1
1	0	0	1	1	1	0
1	0	1	0	0	0	1
1	0	1	0	0	1	0

1	0	1	0	1	0	1
1	0	1	0	1	1	0
1	0	1	1	0	0	1
1	0	1	1	0	1	0
1	0	1	1	1	0	0
1	0	1	1	1	1	0
1	1	0	0	0	0	0
1	1	0	0	0	1	0
1	1	0	0	1	0	0
1	1	0	0	1	1	0
1	1	0	1	0	0	0
1	1	0	1	0	1	0
1	1	0	1	1	0	0
1	1	0	1	1	1	0
1	1	1	0	0	0	0
1	1	1	0	0	1	0
1	1	1	0	1	0	0
1	1	1	0	1	1	0
1	1	1	1	0	0	0
1	1	1	1	0	1	0
1	1	1	1	1	0	0
1	1	1	1	1	1	0

Minimization

[(A. B.F + (B+D.E.F) + H)]’
[B.(A.F+1)+ D.E.F + H]’
[B + D.E.F + H]'

Schematic

Specifications:

-
- C_L = **1pF**,
- $\mu_n : \mu_p$ = **1.9**
- W/L for n-MOS1, 2, 3, 4, 5, 6, 7, and 8 = **8.33**

	W	**L**	**W/L**
n-MOS	1.0µmm	0.12µm	8.33
Inverter	2.7µm	0.12µm	22.49

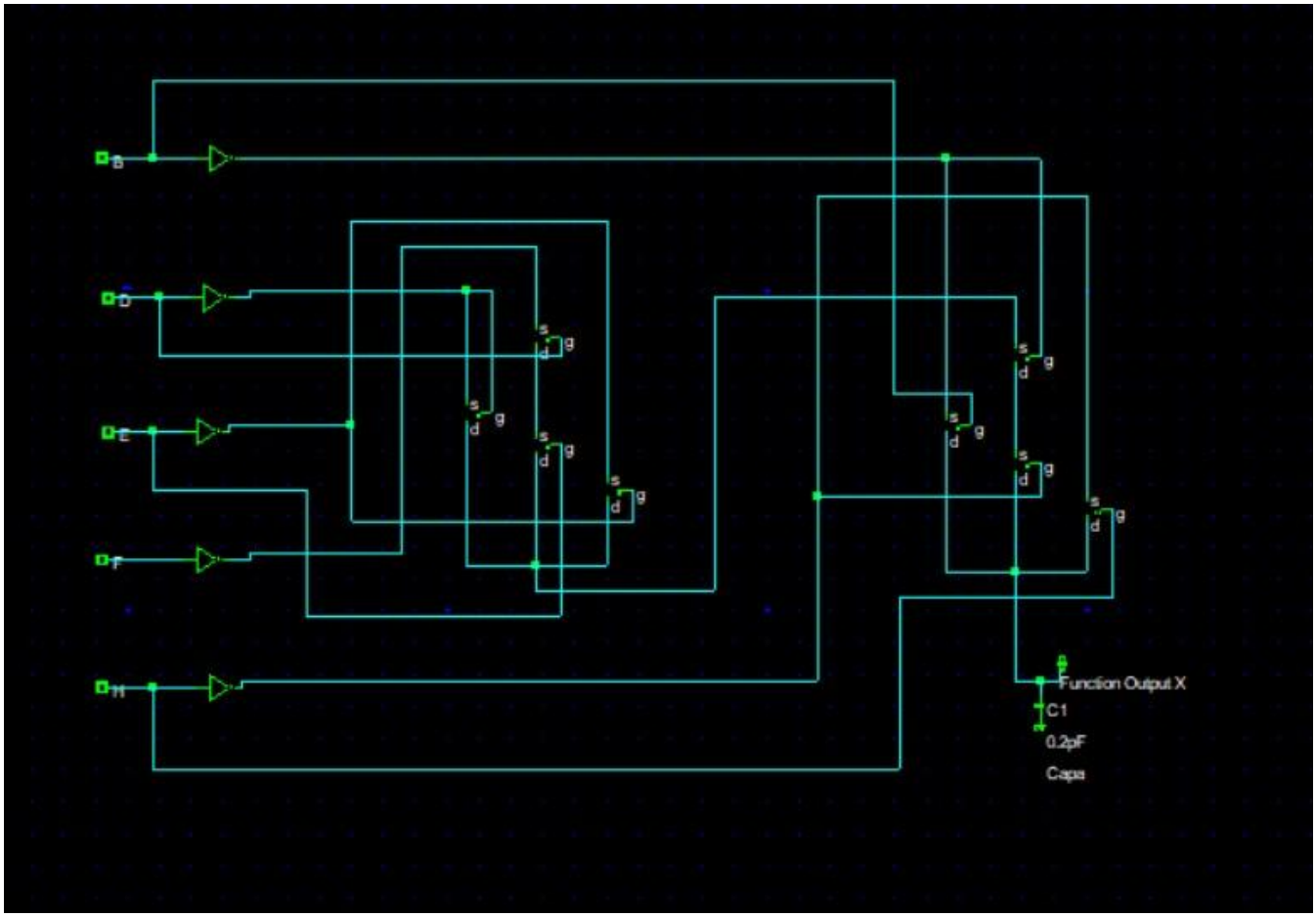


Fig 2. Schematic of the Function

Design Rule Check

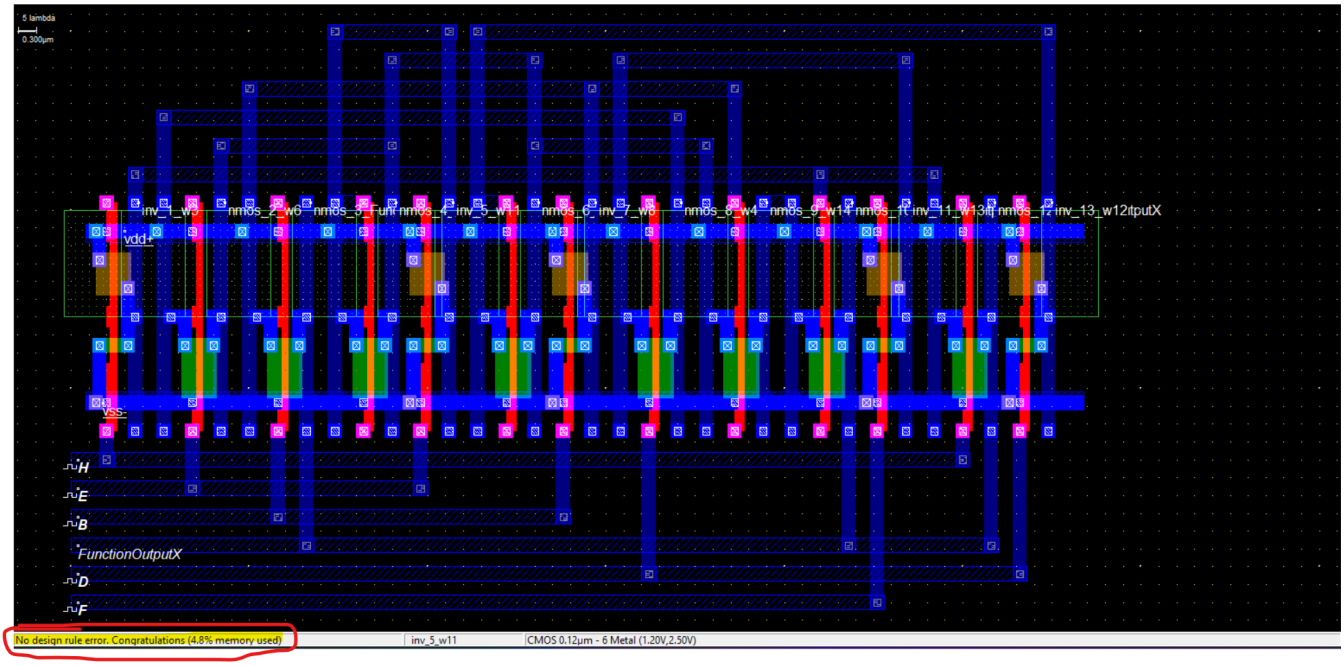


Fig 3. DRC Verification

The Final Layout

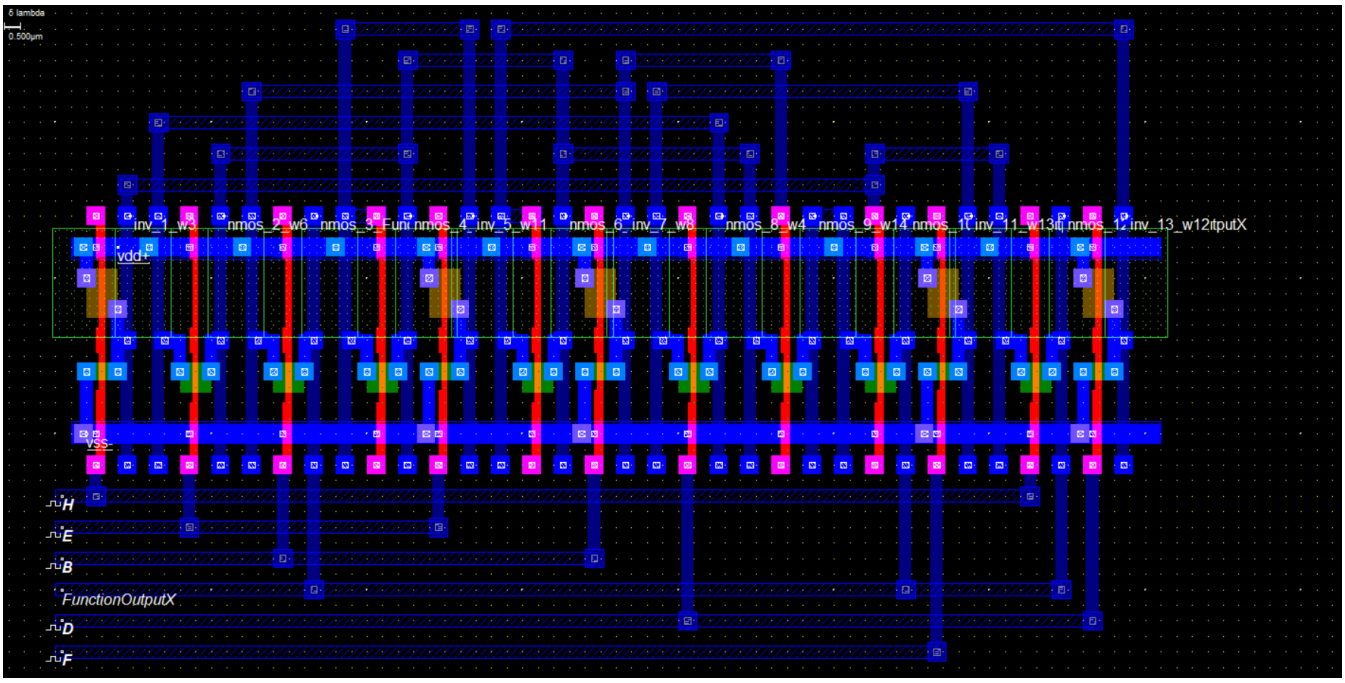
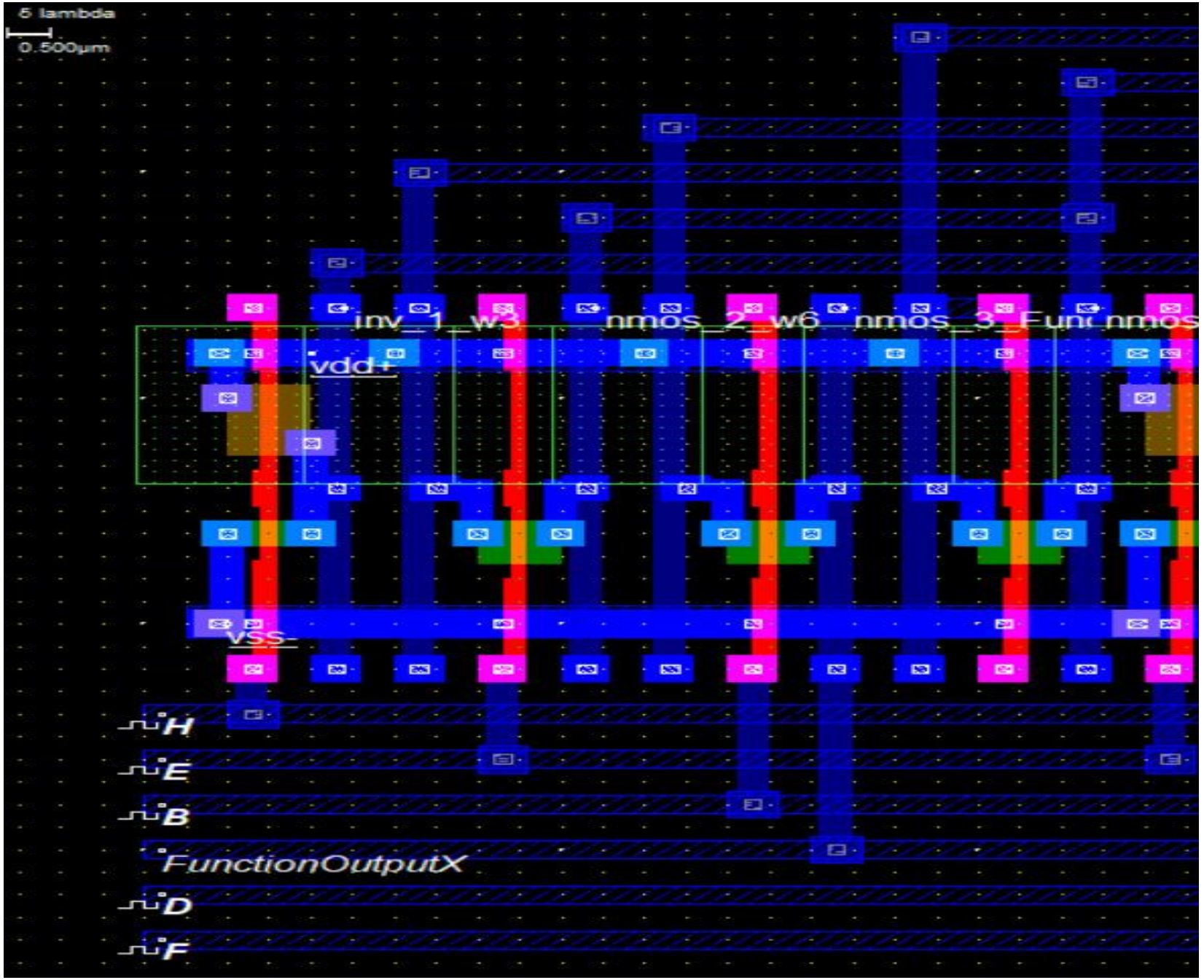
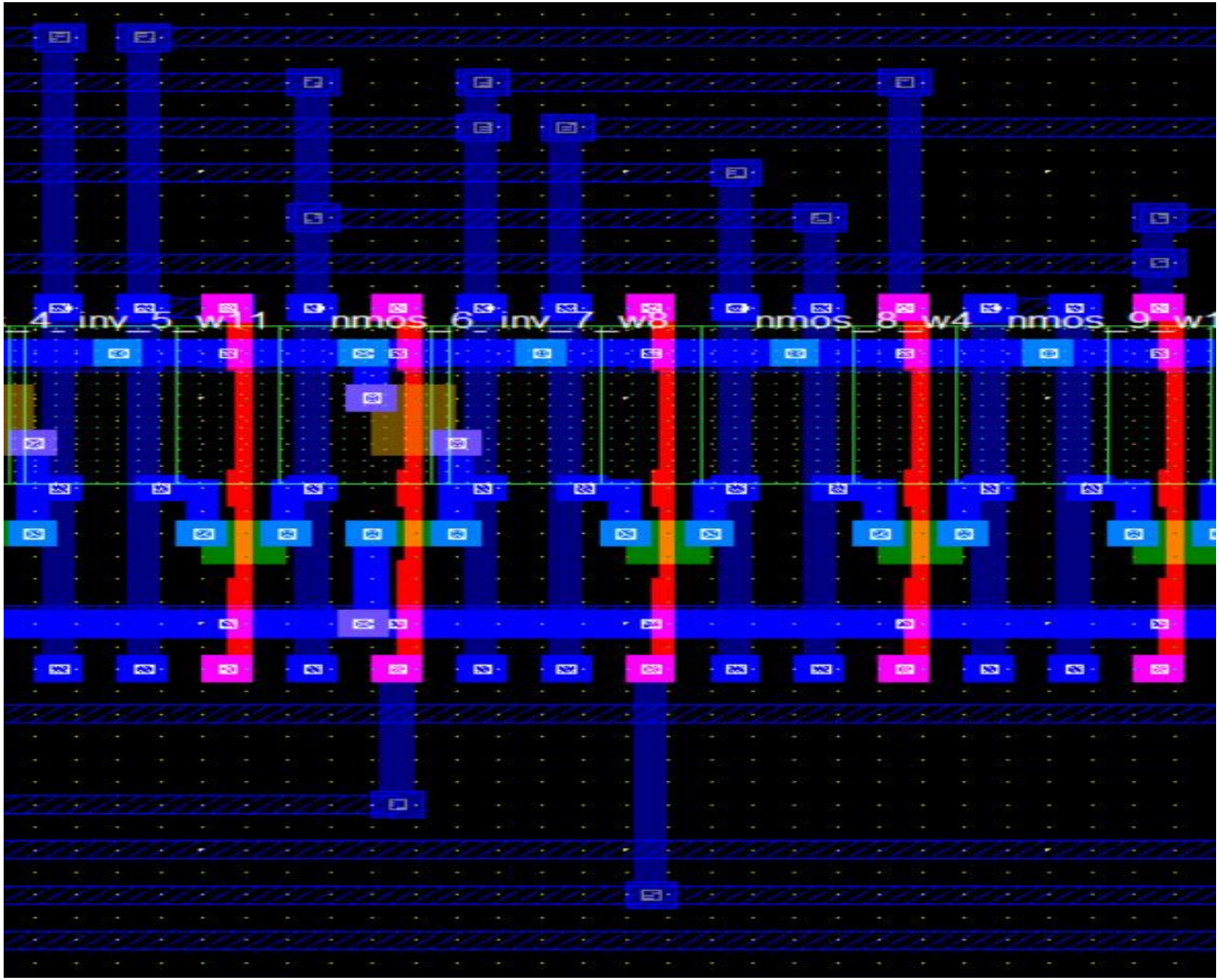


Fig. 4 Microwind layout


5 lambda
0.500µm
inv_1_w3
nmos_2_w6
nmos_3_Fun
nmos
vdd+
vss-
H
E
B
FunctionOutputX
D
F


4_inv_5_w11
nmos_6_inv_7_w8
nmos_8_w4
nmos_9_w1

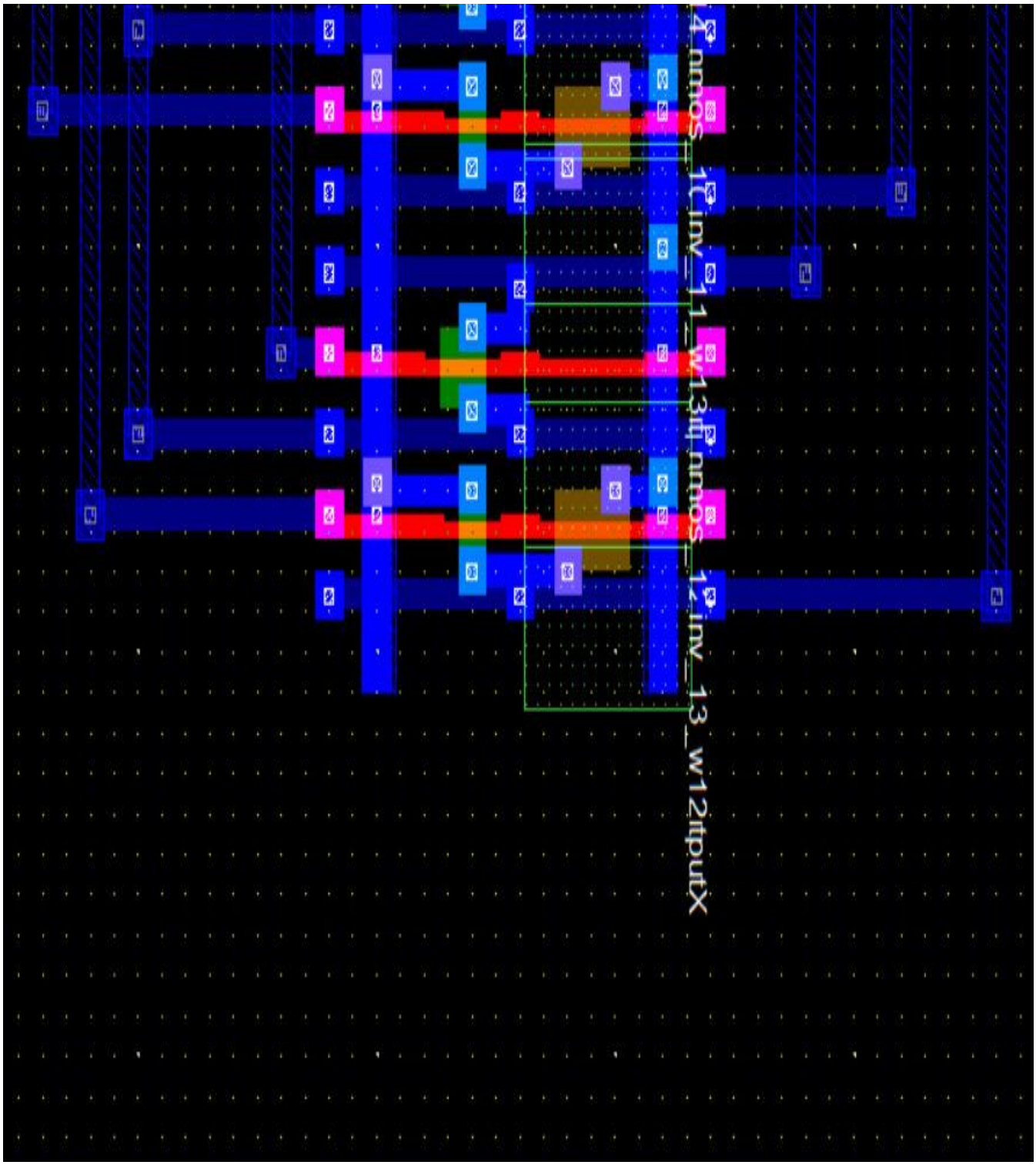


Fig. 5 Microwind layout (Zoomed in)

Output

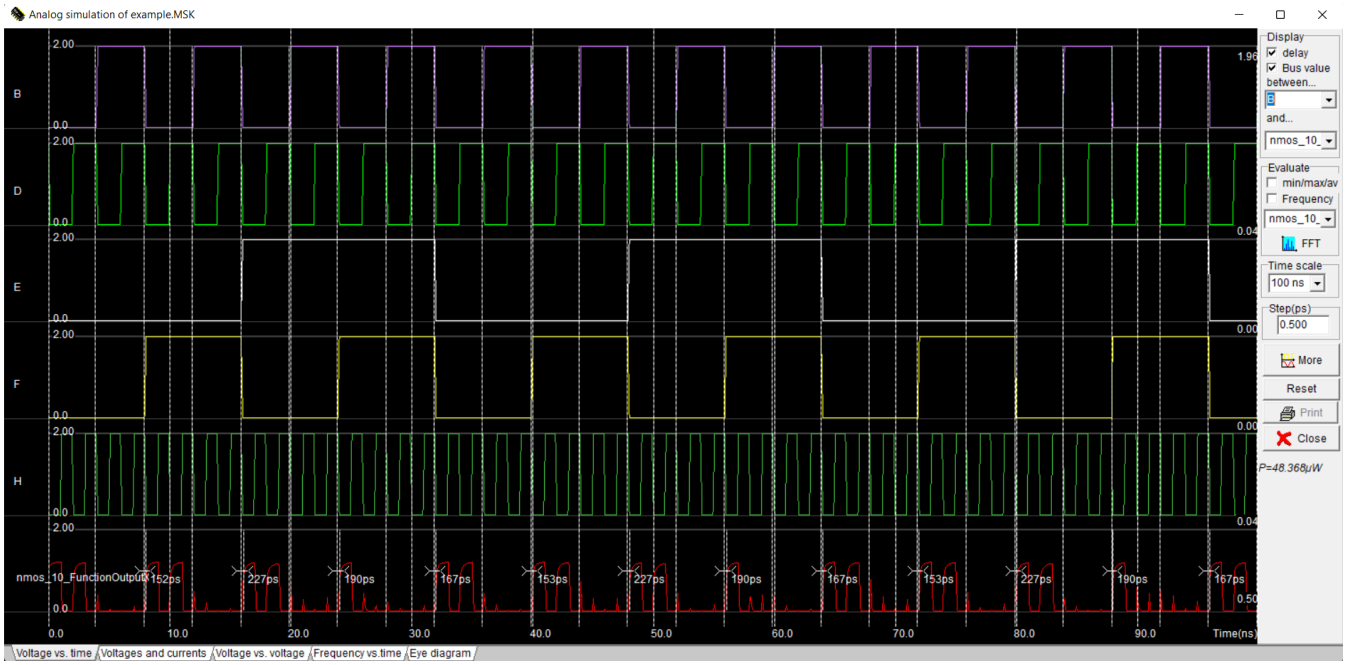


Fig. 6 Voltage v/s Time Graph generated from Microwind

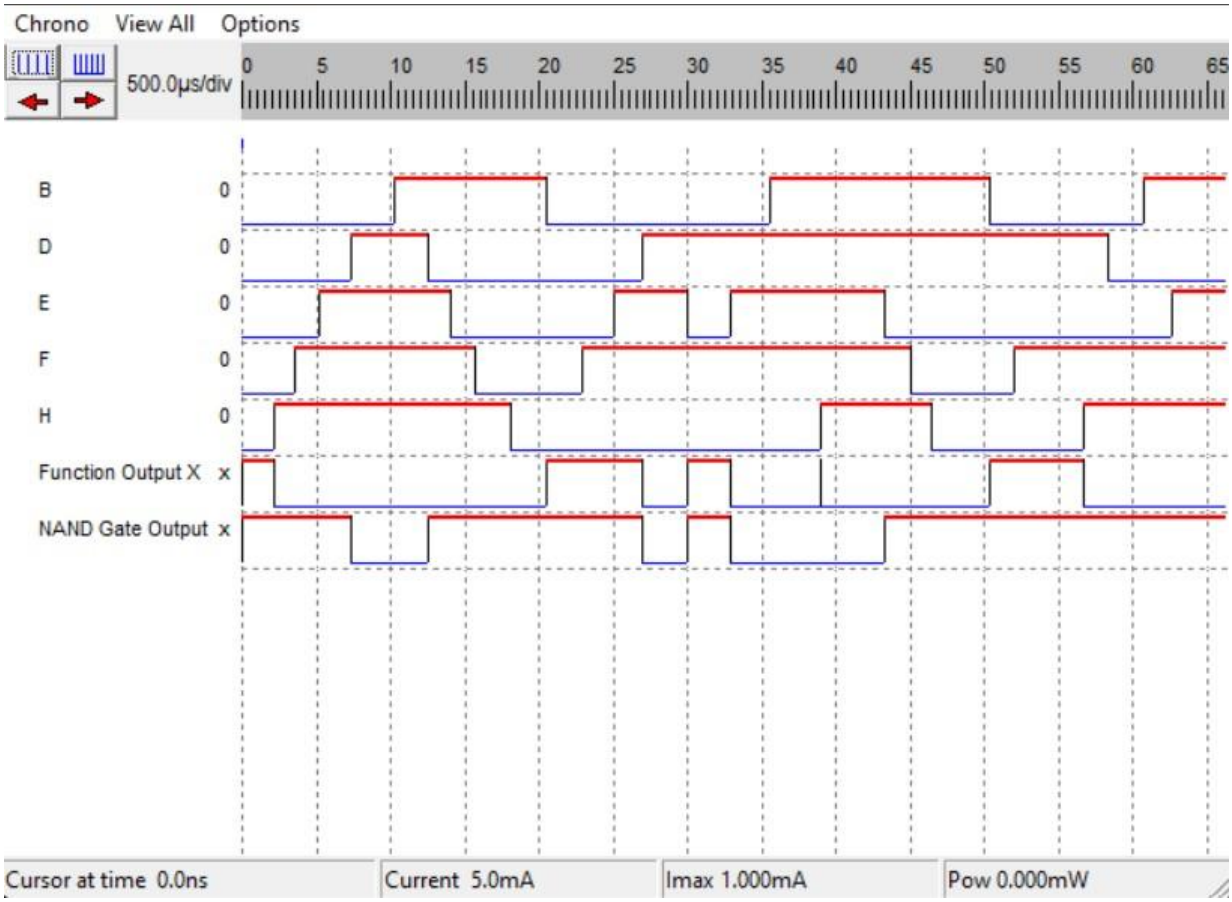


Fig. 7 Voltage v/s Time Graph generated from DSCH

Innovation

- Constructed the circuit using the DHCS tool and generated a Verilog file.
- Used the verilog file to obtain the layout for verifying the results obtained from manually designing the layout.
- Minimised the delay using logical effort ensuring that each branch of the circuit bears the same effort.

Problems and Challenges

- The Microwind software being an obsolete technology is slow to use and has limited functionality.
- We have used Logical Effort in the design of our circuit, since it provides unique insight on how to minimize the delay of a circuit. However, akin to other design methodologies, there is always a tradeoff encountered between speed, power and switching capacity.
- DSCH, being an obsolete software, only supports 256 wires, symbols and Nodes which led to problems in making the schematic diagram. The schematic diagram needs to be highly optimized in order to be supported by the software.