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School of Electronic Engineering

Coursework Submission Cover Sheet

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Title	Integration of FinFET and Planar Transistors on Silicon devices	**Hours spent on this exercise**	45

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Comments:

Integration of FinFET and planar transistors on silicon devices.

Author: OMKAR PABSHETWAR, Meng Electronics and Computer Engineering, Dublin City University, Dublin, Ireland.

Email:omkar.pabshetwar2@mail.dcu.ie

***Abstract*— The power of devices silicon-based CMOS have always been on demand over past few decades in manufacturing of integrated device. Every technology has its own limitation and as the limit of downsizing is over for the conventional CMOS it was necessary to get an alternative to CMOS which would be better in performance , less cost with high density integration. The modification done in FETs and new non planar MOSFET know as FinFET was introduced which is built over bulk or SOI i.e. Silicon on Insulator substrate. This showed better scalability options as compared to planar CMOS and has similar performance. The work represents the integration of two transistors on one substrate i.e. conventional planar MOSFET and FinFET, use of SOI Substrates and low doped fins which results in higher mobility and voltage gain. The integration of both on single wafer results based on morphological and electrical indicating perfectly filled trenches with good and reliable fin height control and performance similar to traditional planar CMOS.**

***Index Terms*— FinFET, CMOS, MOSFET, integration, DownSizing, SOC, SOI, 3D-FinFET, DG-CMOS.**

I. INTRODUCTION

The designing of integrated circuits with high-performance which are used for amplifying signal and switching purpose have “MOSFET” (metal-oxide-Semiconductor field effect transistor) as a fundamental element used. These are good and feasible when considered for integration as it can be produced on large scale because of less scaling cost, highly reliable, and power consumption is less. In current industry trends due to this features of MOSFET it has be always remained a choice for digital circuits and SOCs. Another form of MOSFET is “FinFET”, it is non-planar in nature and is obtained by elevating conducting channel of MOSFET so that gate is surrounded by 3 sides. This why FinFET can also be called as 3D implementation of MOSFET. Because of isolation and gate stack modules the architecture of planar and FinFETs are different in terms of processing sequence [1]. Based on present industrial requirments all challenges are met by FinFET as an other option for planar devices, Multiple gates are used in Regular Vt (RVT) applications to relax the CMOS gate stack engineering complexity [1].

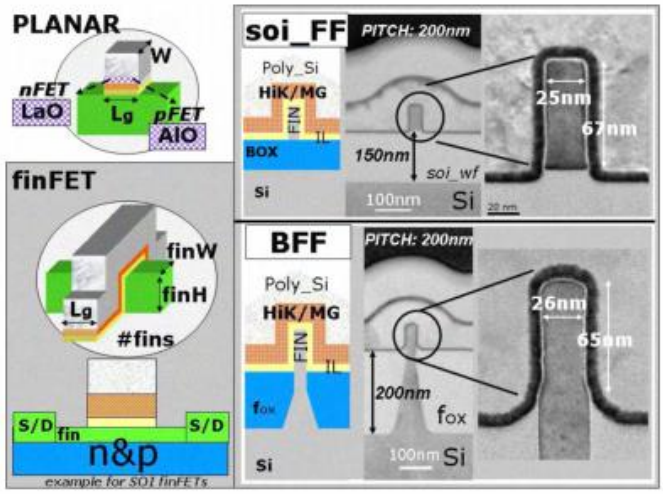


Figure 1In buk FinFET complexity of calibarating latter, based on the critical dimensioningget stacks and schematics of planar and FinFET [1].

The figure shows gate stack details built on both Silicon on insulator wafer and bulk substrates for planar and FinFETs by showing the geometry of the devices.

FinFETs has lower power consumption and higher output current when compared with Planar MOSFET. In FinFET due channel quantization the On/Off is better than MOSFET. Previously for 3 decades Si CMOS where used in IC fabrication but the main challenge to decrease physical size of planar CMOS but due to limitations in physical length 15 nm of gates the concept of bulk MOSFET was introduced, it was difficult to scale it to 10nm because of fabrication issues like leakage, degradation in mobility and electrostatics [2]. Due to the Quasi planar structure of FinFETs and its ease of fabrication the industries are more inclined for using a double gate devices i.e. FinFETs. The demonstration of flexible CMOS SOI FinFETs which are compatible to CMOS is shown in report [3], the leakage off-state voltage is reduced on multiple gates due to the electrostatic charge control. The scaling to 14nm was possible due to shift from planar to non-planar FETs. The System after full integration will be reliable and having high performance along with this the system would be able to maintain largescale integration density [3]. Due to flexible in nature CMOS SOI FinFETs uses fabrication techniques which

are compatible to CMOS for application with high-performance.D

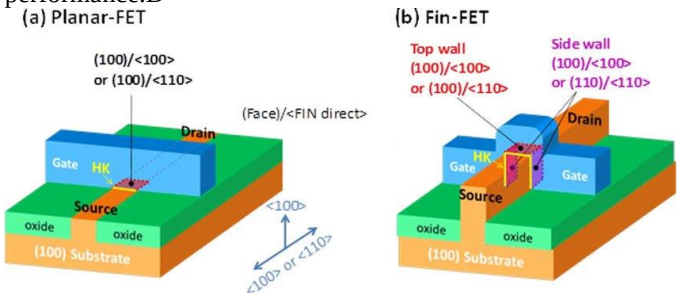


Figure 2The Schematic diagrams for Planar MOSFET and FinFET [4].

The FinFET architecture above we can see that FinFET channel has two planes which is not there in MOSFET, In FinFET channel there is low doping concentration due to which the above FinFET architecture provides better variability and device matching [4]. As the FinFET devices has 2 surface planes and properties of both surfaces need to be considered for interface. Due to special features such as transistor compactness and channel effect control FinFETs are preferred for SRAMs and analong circuit applications of technological node [5], instead of pre silicide surface clean the SMR processing technique tool that is plasma free dry oxide rmoval to integrate 20nm gate length FinFETs in the form of tri-gate FinFETs. These can be in the range from 90nm to 200nm and illustrated with an 65 nm FinFETs.

II. Scaling of Planar CMOS and its Future Technology

In terms of cost and performance Planar CMOS devices which are 28nm and 20nm are technologies which are widely used and considered for mass production of system on chip and microprocessors [6]. The variations in designing reduces when there is greater volume of device manufacturing to obtain desired performance. Processing techniques which are introduced using variety of new materials like Ultra low-k and high-k metal gates and strained Si [6], SiO2 are stopped at the size of 130nm because of gate leakage.

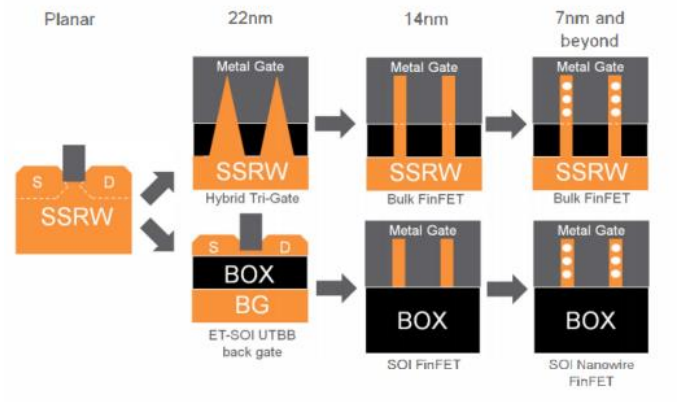


Figure 3 Evolution of CMOS with SSRW to different 3D-FinFETs based on fully depleted SOI and bulk [6].

Modification is done in strained silicon from 130nm into 20nm or 14nm by VLSI-CMOS technologies and because of this to transfer stress in transistor channel very less space is available. New Integration methods are required for 10nm and further due to existing Extreme-ultraviolet lithography, the methods such as air-gap interconnects, double and quadruple patterning etc.
To maintain the legacy of Moore's law device architectures such as three dimensional FinFETs and other new types of devices are needed for continuation of over-scaling.
The above figure shows the evolution based on Silicon on Insulator (SOI) and Bulk of CMOS devices with "Super Steep retrograde wells (SSRW)" [6] to "3D-FinFETs" until it reaches to the multi stacked nanowires inside each fin. At present for gate length of 10 nm second and third generation FinFETs electrostatics can be used. If this limit of electrostatic FinFETs exceeds it will reach to stage at which there are multiple stacked nanowires inside each FinFET's fin as shown in figure 3 below. The Final solution for both base substrates which it can be reached is more than one nanowire in each 3D-FinFET's fin.

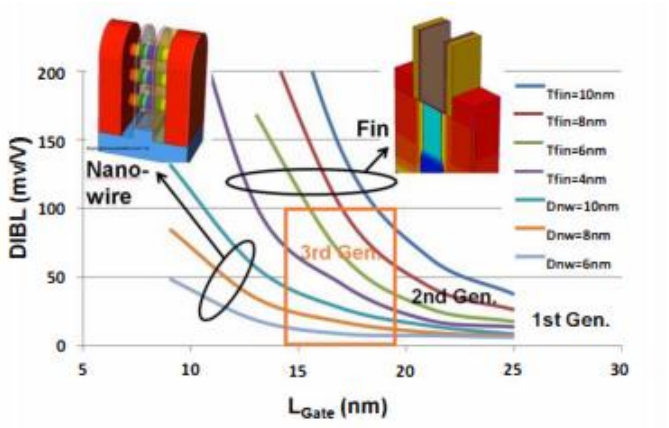


Figure 4 The figure [6] showsfor the gate length of 10nm consider by second and 3rd generation FinFETs.

III. Fabrication

The paper [2] shows the fabrication process of FinFETS along with fabrication of multiple fin devices and it also illustrates how due to narrowing of active region i.e. fin the difference between FinFETs and planar FETs is understood. Fabrication of FinFETs was done with modified MOSFETs on SOI wafers. The fabrication process of FinFET is shown below from diagram (a) to diagram (f) in figure 5. It is a double gate FinFET, scaling of this FinFET is done by decreasing the fin width or body thickness of it. The fabrication of these FinFETs is done with process of planar CMOS on Silicon on Insulator (SOI) wafers [2].
The poly-Si gates which are dual doped are used as gate electrodes, through ion implantations these gats were dual doped and activated with RTA. The gate length was reduced to 10nm with the help of a pattern reduction technique and the gate insulator used in this process was nitride oxide with physical thickness of 17A. Apart from this process also has features such as cu metallization, NiSi and source/drain annealing, Multiple fin transistor were used to fabricate CMOS inverters.
The new method in which CMOS and FinFETs are integrated

on the same substrate in fabrication flow is achieved by "Siconi" (SMR) Selective Material removal, with enhancements in fabrication steps such as trench oxide this new method can be used to fabricate FinFET by modifications in bulk silicon [5]. Trenches filled perfectly resulting in terms of electrical and Morphological and achieve better performance like CMOS and height control of FinFET's fin.

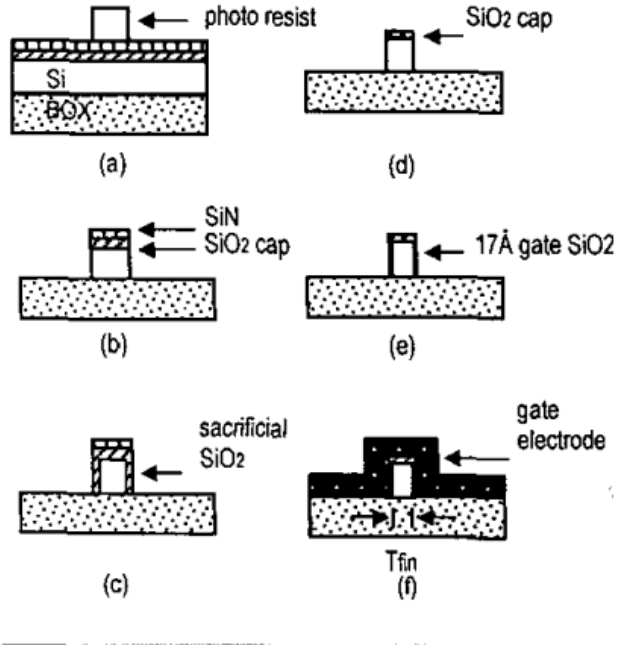


Figure 5 Fabrication process of FinFET [2].

In the (110) crystal orientation of two sidewalls of silicon fin there is formation of conducting channel, and it has cystal orientation different from (100) i.e. a planar CMOS device, on the plasma fin there is a thin layer of insulating cap [2]. The new SMR processing technique for fabrication which is known as "Siconi" is used to overcome the main challenge of fin height control in FinFETs. Each cycle is tuned with controlled amount of oxide (20nm) for sublimation of fluorosilicate and growth and used as process of removal of dry oxide i.e. Siliconi [5]as this method is least dependent on changes observed in density of oxide on side walls and transitions in less dense CVD material which giving better etching characteristic than wet etch.

A. Double gate CMOS (DG-CMOS) or FinFETs

After the limit of traditional scaling of MOSFETs the continuation of double gate CMOS scaling will be enabled, this offers gate dielectric barrier and strategies path for scaling by DGCMOS/FinFET technology further progress is halt by the atomic fluctuations [7]. The fabrication of FinFET i.e. DGCMOS is slightly different as compared to the traditional fabrication process of CMOS which helps in fast manufacturing and deployment of devices. In Double gate CMOS extra gate is added in front of the gate in conventional CMOS to overcome the challenges faced such as gate-dielectric and subthreshold leakage.

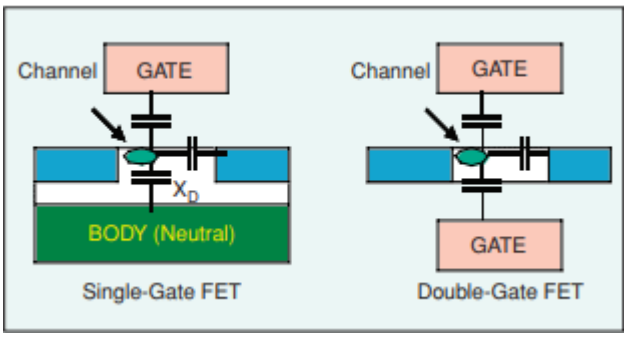


Figure 6 The intrinsics compromised by the Convetional MOSFETS and it solution by Double Gate architecture of device [7].

The above figure represents the positive effects of Double Gate MOSFET where it is not possible to off the channel current through gate due to reduction in length of channel, to protect the channel from draining short channel effect is mitigated because of the depth between the channel to the substrate is thin and gate oxide is thin [7].

There is slower turn on in the channel region due to degradation in gate influence of channel and decrease in depletion region. As there is a proximity to the channel od 2nd gate, from the source end of the channel longitudinal electric field generated by drain is screened better [7] this leads to reduced drain induced barrier lowering (DIBL), improved subthreshold swing and short channel effects are reduced Therefore, due to leakage current the scaling of CMOS is limited and this opportunity is undertaken by DG CMOS which offers performance of Single-Gate (SG) bulk silicon or PDSOI-CMOS. The ability to increase the effective width of device and improve the electrostatics had made the semiconductor industry move from planar CMOS to FinFET transistors production and many manufacturer are engaged in production of large scale14 and 16nm nodes of FinFET technology but after the gate length of 7nm the scaling problem increases beyond expected as practically there is a physical limit for scaling fin pitch and fin width due to combination pf pattering process and quantum effects [8]. Gate all around i.e. GAA devices has improved this overall limitations through designing double and triple gate FinFET devices.

B. Patterning:

To get the features of integrated circuits the technique which is used in lithographic process are used at advanced process nodes and is known as patterning. The 20nm fin width is achieved along with side wall oxidation by trimming 78nm ands 41 nm line widths into 30nm for pitch structures of 90nm and 200nm by performing lithographic process on it, there is adverse effect on gate patterning ad trench fills due to unwanted formation of nitride overhang [5]. This is avoided by lateral loss after selecting PECVD nitride film throughout process of trench etching.

It is observed in figure below for the fabrication of tri-gate FinFET profile on top is appropriate and shows the profile of fin after trench etching and fabrication of STI trench which is filled with oxide.

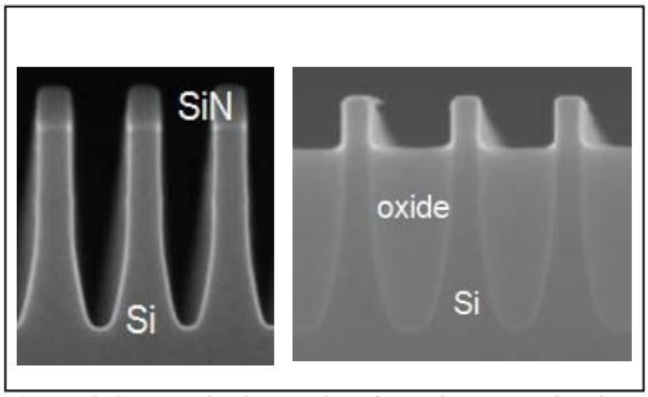


Figure 7Fin width is reduced to 20nm by Fabication with STI shown in right figure and Fin hgt 280nm , width 35nm obtained after performing dry etching as shown in the left figure [5].

C. Height Control of fin:

After the process of chemical Mechanical Planarization (CMP) used on silicon oxide to control the fin height by following few steps sequentially. The required height of fin is achieved by steps which involves settlement of field oxide until nitride bottom level, using hot phosphoric bath for removal of nitride and at the last field will be settling until the required fin height is not achieved. There is unwanted feature in the form of oxide foot while settling of field oxide after using wet etching.

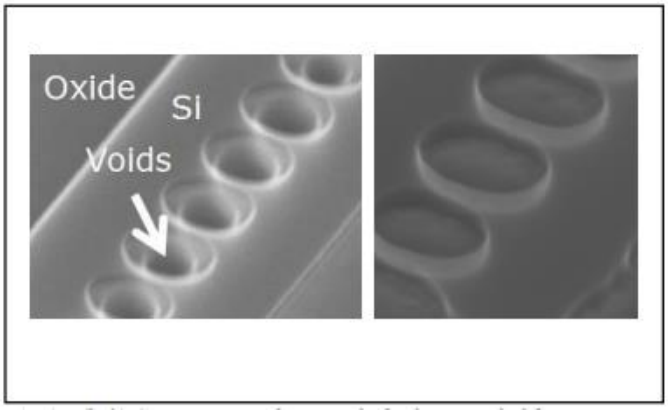


Figure 8Supress foot and void formation on the lesft side and its improvement using dry etching on the right [5].

Due to this their ca n be formation of open Voids as shown in figure 7 and this formation can be stopped by integrating Siconi (Slective removal technique) inside process sequence for removal of oxide and it does not relate to oxide density.

D. SRAM in FinFET CMOS Technology

In the paper [9] 84 Mb SRAM array is designed for second generation FinFET of size 14nm, as this is a difficult task to design at 14nm node by a bitcells of about 6T SRAM with transistors of minimum sized. In this world growth is fast in battery powered devices especially mobile phones so is the demand for low power consuming and less cost of SOC design is increased. The strongest approach now is the scaling of supply voltage for SoC design and due to rising levels of memory integration voltage scaling is also considered for die memory, there is supply of separate voltages for on-die memory as in design use of SRAM can restrict the minimum operating voltage [9]. Solution to this problem i.e. formation of reduced threshold voltage under fixed leakage constrains was given by introducing trigate devices which will be used at 22nm nodes to obtain the subthreshold slope in relation to present bulk planar. CMOS has high integration density ad performance, while FinFETs have reliable and promising structure FinFETs are known as double and triple gate MOSFETs because they have high current driving capacity, they are robust against SCE and good subthreshold swing [10]. In this paper demonstration of "fully-depleted silicon-on-insulator (FDSOI) CMOS with TiN/W interlayer contacts using "n-over-CMOS" 3-DM integration of a replacement metal gate (RMG) InGaAs n-FinFET layer" [11] and by treating unfairly these inter layer contacts we can get the circuit for "dense functional 3D-6T SRAM".

E. Subthreshold off-leakage current

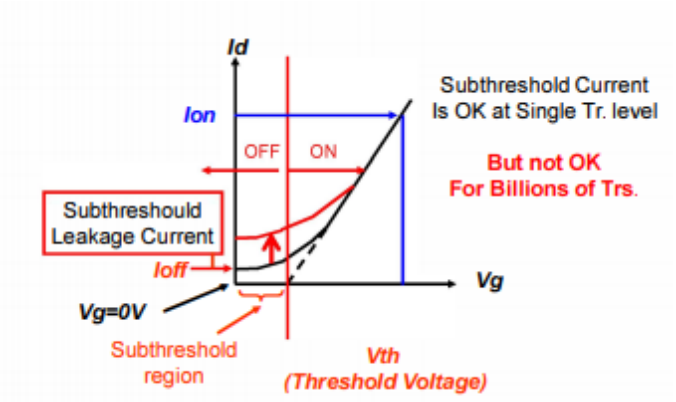


Figure 9 Id linear scale with Id-Vg characteristics [12].

The Sub-threshold off leakage current is the unavoidable component of the off-leakage current in the MOSFETs as shown the traditional Id-Vg characteristics above, the dotted line indicate that drain current is zero in the circuit operation view [12].

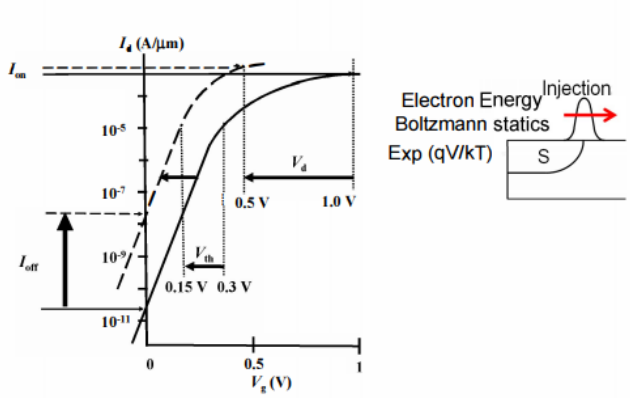


Figure 10 Id log scale with Id-Vg characteristics [12].

Boltzman distribution of electron energy which is expressed with the help of equation exp (ElkT), in which E, k and T is electron energy, Boltzmann constant and temperature, respectively, these causes exponential leakage in the subthreshold region [12]. Due to electrons having energy

greater than the barrier flow and reduction in ration of potential barrier between Source and channel to the gate bias.

The Threshold voltage ad supply voltage will be levveld down to half if the MOSFET size is assumed to be decreased to its half the present size, it relates to the parallel shift of the log /aVg curve to the left direction with 0.15 V (= 0.3 - 0.15 V) [12].
Till now we have considered only the off leakage current for the downsizing but the downsizing can be s=done upto 3nm with the help of direct tunneling technique.
Practically it is difficult to operate integrated circuits with the size of 3nm due to the off leakage current will be too high and this is why sub threshold leakage current is another limiting factor in downsizing.

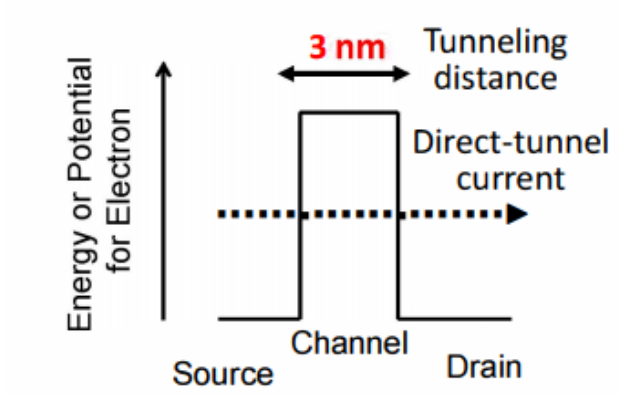


Figure 11 Direct tunneling between Source and drain [12].

The above technique will help MOSFET design to be Downsize using direct tunneling upto length of 3nm, and after reaching this 3nm the direct tunneling effect occurs were potential barrier is penetrated by the wave function of electrons.

IV. SOI EVOLUTION IN PLANAR AND FINFETS

SOI (Silicon on Insulator) advantages based on its history are High performance logical applications, Analog mixed signal applications and Embedded memories and used for FinFETs and FDSOI devices which are fully depleted. Due to constant scaling of CMOS transistors its size has become near to atomic level dur to which further modification has become challenging for this 3-dimensional integrated circuits are introduced for large scale production were stacked transistors used due to which there was reduction in 50% of area utilization and instead of interconnects with long wiring shorter vertical interconnect routing was possible [13]. The features of SoI are high speed switching with short channel effects improved, superior isolation with no requirements of well tap and latch-up free operations, variations inside die are decreased with short channel vt-roll of suppression and no deep wells in SOI i.e. no well proximity effects [14].

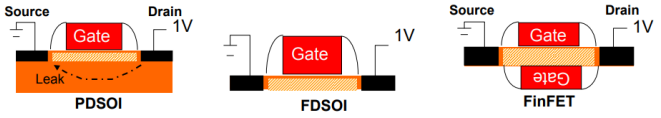


Figure 12 In the first figure gate is no able to control bottom part due to which there is leakage of current, in figure 2 there is no leakage of current in FDSOI and in 3rd figure FinFET has two gates and have more Si results in more current carrying capacity [14]no leakage.

Double gate FETs: As compared to bulk, PDSOI and UTTB - SOI Double gate CMOS is preferred having abilities such as there is no voltage divider action with wafer, with the help of two gate source is shielded from drain, improved performance, power and density. The Double date FET is considered as FinFET as it has various advantages such as for both sides source to drain there is equal front-side access, both gates has front size contact dense and these double gates are self-aligned.

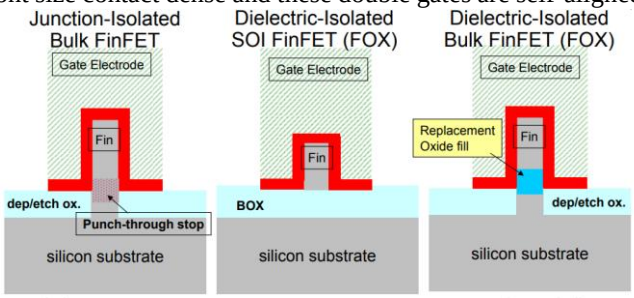


Figure 13 Isolation Schemes of FInFETs [14].

The First isolation scheme is Fin o bulk it is a complex scheme which uses bulk substrate and by ox etch fin height is controlled. Second diagram in the figure fin on SoI isolation scheme which is simple as compared to fin on bulk which uses SOI substrate and this substrate controls the fin height, third one Fin on Oxide over bulk it has a complex isolation scheme uses bulk substrate. Capacitance, leakage tradeoffs along with height control of fin are challenges faced by bulk FinFETs and there is variation in fin doping due to need of isolation doping, having Superior isolation properties planar passives are enabled by bulk FinFET [14].

V. LAYOUT AND STRUCTURE OF STACKED FIN-CMOS

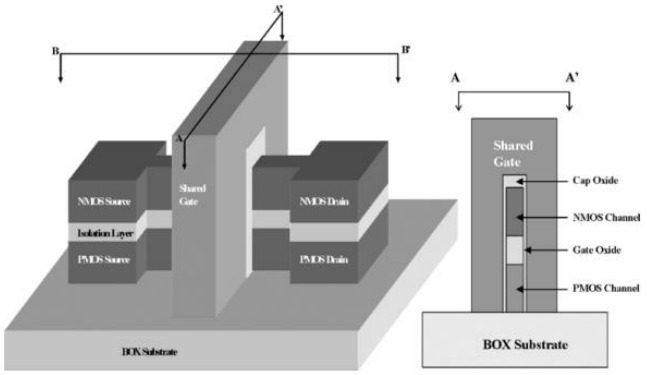


Figure 14 3D stacked Fin CMOS device schematic and cross-section [13].

The above figure represents the stacked version of Fin CMOS, fundamentally it is a vertical extension of traditional quasi planar FinFET were if nFET and pFET are put one above the other or stacked such that they are sharing self-aligned gate inside fin and inverter can be formed [13].
Due to this circuit design area utilization is reduced to half as compared to 2D designs and further SF CMOS technology can more compact structure than layer-by-layer 3D CMOS with benefits such as less masks count and lower thermal budget. DSOI that is double layer SOI substrate is developed during the design stage of stacked fin-CMOS, 2 layers of stacked transistors can be formed using single silicon film of high quality and with the help of 3D architecture various devices can be fabricated such as SRAM calls, NAND gates, IC building blocks etc.
In the figure we can see that there is shared gate between N-MOS and P-MOS in the pi-shape gate straddles, to achieve self-alignment for both N-MOS and P-MOS this shared gate is used as an implant mask [13].To insulate bottom and top of device there is isolation layer and implementation of various CMOS circuits such has multiple NAND gates and inverters is done. With appropriate changes in process there are various combinations available to stack N-MOSFET and P-MOSFET.

VI. Process of Wafer Thinning

The Effective scaling in Integrated Circuits is a very challenging part but 3D integration is favorable one for scaling as it gives greater functionality per foot print and empowers heterogenous integration, Scaled TSV sizes that is through silicon Via sizes and higher integration density.

Table 1: TSV diameter and TSV pitch based on ITRS roadmap for 3D integration [1], comparison to expected wafer thicknesses

Die to Die stacking	Ø TSV [µm]	TSV pitch [µm]	Wafer thickness [µm]
2011 - 2014	4 - 8	8 – 16	50
2015 - 2018	2 - 4	4 – 8	< 10
Wafer to wafer stacking			
2011 - 2014	1 - 2	2 - 4	5
2015 - 2018	0.8 – 1.5	1.6 - 3	< 5

It requires drastic decline in thickness of wafer for aspect ratio during etching of TSVs. For the 300nm CMOS wafers development of process flow for backside thinning down to 5 micro meter thickness.
There can be damage to the overall performance of device especially for the sensitive device's electrical front end, this damage is possible when zone of wafer gettering is decreased or removed and diffusion of metallic contents which eventually reach active area results in damage of electrical performance.
In the figure below the local interconnects to enable fine pitches are L1 and L2 these are tungsten-based Middle of line (MOL) and high k Replacement metal Gate (RMG) [15]. After processing the backend of line passivation with M1 layer to extreme thinning process for inline electrical measurements.
Based on the targeting Si thickness of 50,20,10 and 5 micro meter, grinding and Wafer backside flow of thinning process is decided. While the thicker wafers are placed fixed on the dicing tape 5 micrometer wafers are bonded on Si carrier blanket to handle thinned wafers safely [15].

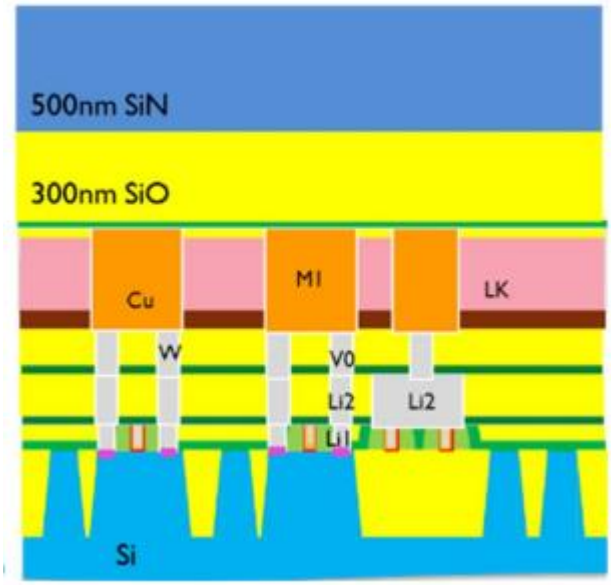


Figure 15 Layer discrption of FinFET devices and it schematic vcross section [15].

In figure below we can see that based on continuous use of Moore's law over the past 43 years the generation of integrated circuits from 10 micrometer upto the 22nm VLSI CMOS circuits, 18 generations in total [12]. By the factor of 0.5 or 0.7 there is decrease in size in terms of average width and size of MOSFETs every 2.5 years.

(1970) 10 µm → 8 µm → 6 µm → 4 µm → 3 µm → 2 µm → 1.2 µm→
0.8 µm → 0.5 µm → 0.35 µm → 0.25 µm → 180 nm → 130 nm →
90 nm → 65 nm → 45 nm → 32 nm → (28 nm →) 22 nm(2012)

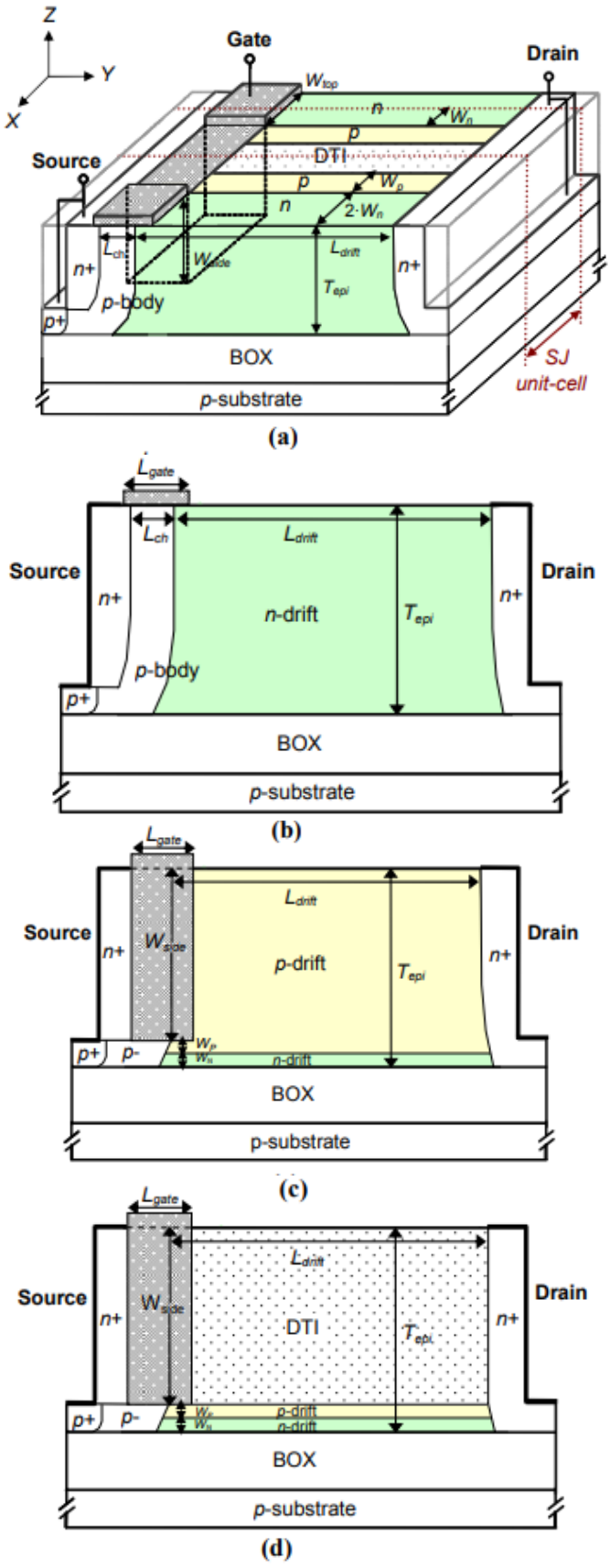
Figure 16 MOSFETs trend of downsizing over the past 43 years [12].

In period of next 10 years the market growth for integrated circuits will be increasing upto the 5 times than present and demand for high performing ICs and LSI will be more, It is surprising that the saturated market for this product is still growing.

VII. CMOS compatible Super junction FinFETs

The architecture proposed of this Super-Junction FinFET is suitable and reliable for integration and this paper discuss the challenges which can occur with applications of sub-100v, advanved SOI-CMOS and FinFET fabrication technologies are compatible with this archticeture [16]. The trade offs between break down voltage and specific on resistance is improved using the SJ-FinFET by overcoming the Si limit.
There is no degradation in breakdown voltage while SJ-FinFEt minimizes the channel and drift resistance, and there is similar n/p drift region pillars in SJ-FinFET when compared with

Planar CMOS. The proposed technology was tested on different conditions such as charge imbalance conditions, different drift region lengths.



The figure above is the schematic representation of SJ-FinFET, the drift trench regions are represented in diagram a-d and cross-sectional views along with n-drift and p-drift [16] To provide more conduction path to the drift region by simply increasing the channel width by keeping 3D corrugated trench MOS on both sides of walls and also on top surface.

The SOI substrate with high quality silicon fusion bond is considered after several attempt to achieve fully depleted region by several doping concentration of n/p pillars [16] SAD effect is minimized that is substrate assisted depletion effect.

The addition of processing modules such as deep trench, 3D trench gate, and SJ drift to realize SJ-FinFET and they must be compatible to CMOS and also do not affect overall cost. To perform gate electrode methods such as Gate lithography, gate oxidation, in-situ ndoped amorphous silicon deposition, poly-crystallization, poly-silicon etch, doping and annealing were taken into consideration and for deep trench etching extra mask is required for trench gate formation, later entire gate electrode was defined based on the use of conventional gate mask.

A. Comparison of bulk and SOI FinFETs

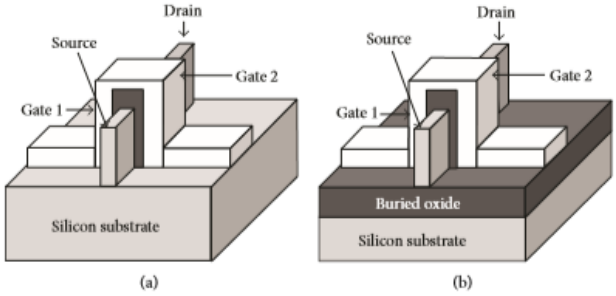


Figure 17 The cparison between Bulk and SOI FinFETs based on structure [17].

Although there is demand of FinFETs implementing of SOI substrates but FinFET can also be implemented on Bulk substrates, the figure above shows that fins in the SOI substrate are isolated as compared to the FinFET implemented on bulk substrate were all fins are taken as common Si substrates also known as bulk. Few Industries might prefer bulk FinFETs as compared to SOI because process of migration from conventional bulk to bul FinFET is simple, while other parameters such as performance, yield and cost are similar for both SOI and Bulk Substrates [17].

VIII. Conclusion

Due to limitation of Scaling in conventional Planar CMOS, FinFETs are best alternative for downsizing using the Moore's law. In terms of voltage gain and mismatch undoped SOI FinFETs are preferred. The smallest physical gate length is achieved using the fabrication technique by integration of CMOS and FinFET, but this results in complex fabrication in process of existing planar. The necessary changes considered are performance, power dissipation, scalability, density and packing for FinFET which is promising factor to scaled CMOS.

IX. References

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