

Improved Direct-Coupled High-Bandwidth Voltage Amplifier for B-H Characterization of Magnetic Materials

Syed Shahjahan Ahmad*, Aditya Raj†, G. Narayanan‡

*Dept. of Electrical Engineering
Indian Institute of Science*

Bengaluru, India

Email: *shahjahans@iisc.ac.in, †adityaraj@iisc.ac.in, ‡gnar@iisc.ac.in

Abstract—B-H characteristics of magnetic materials are an essential input to the design of electrical machines and magnetics in power converters. Wide frequency range operation of machines and converters increasingly requires experimental characterization of the magnetic core material at low as well as high frequencies. Therefore, power amplifiers having wide bandwidth, high voltage and current gains, along with low output offset are needed for characterization. Linear closed-loop multistage amplifiers are often used. Direct coupling of amplifier stages is desirable to characterize the magnetic materials at very low frequencies. The middle stage of such linear multi-stage amplifiers provides the voltage gain. A conventional common-emitter based middle voltage gain stage is reviewed first. A folded cascode amplifier with buffered output is proposed as an alternative. This is capable of direct-coupling with the input (differential), and output (current amplification) stages. The proposed amplifier is shown experimentally to yield a high gain-bandwidth product. Experimental results of the proposed voltage amplifier and the closed loop power amplifier are presented.

Index Terms—Buffered folded cascode, common emitter, direct coupling, ferrite, magnetic characterization, power amplifier, Voltage amplifier

I. INTRODUCTION

Magnetic material properties such as B-H curves and core losses are important for the design of rotating electrical machines, transformers and inductors [1]-[3]. A block diagram of transformerless magnetic characterization using ring specimen (IEC 60404-6) is shown in Fig. 1 [2]. Transformerless operation is desired for compactness and to keep the cost low. Hence, a precision linear power amplifier (LPA) with required voltage and current rating along with having negligible DC offset at its output, is used to excite the primary coil. LPA is fed by the signal $v_{in}(t)$, which is the sum of the reference sinusoidal signal $e^*(t)$ and the amplified error between the reference and actual signal $e(t)$. Under saturation conditions, peaky magnetization currents are drawn by the primary coil. Hence the proportion of error signal may be higher and non-sinusoidal signals need to be amplified by

This work was supported by the Ministry of Human Resource Development, Govt. of India, and Ministry of Power, Govt. of India, under the project titled "Design, Development and Control of High-Speed Switched Reluctance Generator for Direct-Coupled Operation with Thermal Turbo-Machinery".

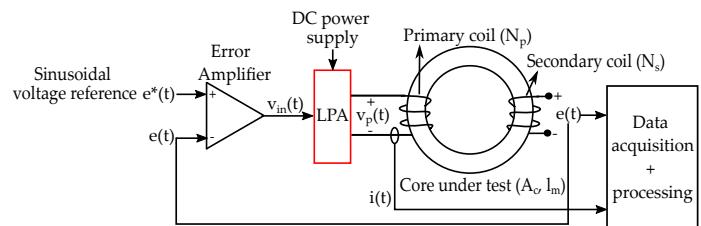


Fig. 1. Experimental setup for transformerless magnetic characterization

the LPA. Hence the LPA needs to have a wide bandwidth..

The LPA is typically composed of three stages, namely, an input differential stage, a middle voltage gain stage, and an output current gain stage [7]. Conventional capacitively coupled LPA, as shown in Fig. 2(a), cannot be used to characterize magnetic materials at low frequencies. Therefore a direct coupled amplifier, as shown in Fig. 2(b), is desirable.

The voltage gain stage determines the small signal open loop bandwidth of the overall multistage amplifier; therefore high bandwidth of voltage amplifier is critical. Further, this stage must be suitable for direct coupling to input and output stages. A typical common-emitter (CE) amplifier based voltage gain stage using a PNP transistor was used in a low-cost linear power amplifier, reported in [8]. The output stage was a conventional class AB amplifier with a V_{BE} multiplier biasing. The CE stage and the V_{BE} multiplier of output stage were designed for the same bias current. Hence, the two stages were directly coupled by using a common current source I_{Qb} to bias both of them, as shown in Fig. 3. The CE amplifier has limited bandwidth due to reduction of small signal base current due to current through collector-to-base capacitance. The bandwidth can be enhanced by cascading the CE stage with a common-base (CB) stage, i.e., cascode connection. In this paper, a folded cascode based voltage gain stage followed by a voltage buffer is proposed to achieve direct-coupling with the class AB output current gain stage. The analysis, design and experimental results using the proposed buffered folded cascode amplifier are discussed.

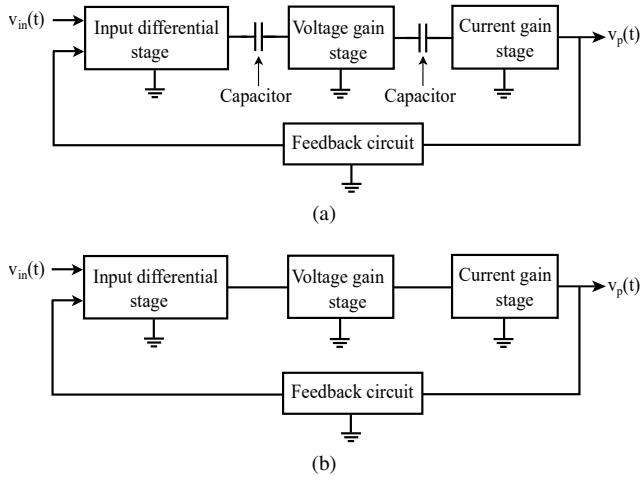


Fig. 2. Three stage linear power amplifier (LPA) for B-H characterization with (a) capacitively coupled stages (b) directly coupled stages

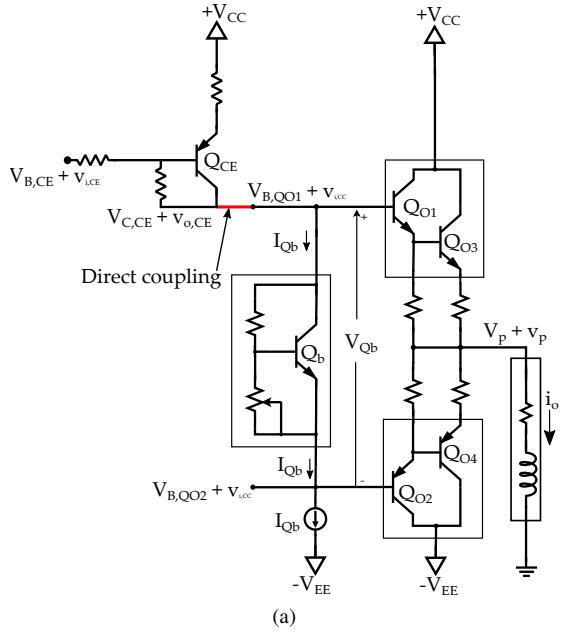


Fig. 3. CE amplifier based voltage gain stage directly coupled with output Class AB amplifier based current gain stage [8]

II. PROPOSED BUFFERED FOLDED CASCODE BASED VOLTAGE GAIN STAGE

This section proposes a folded cascode amplifier with an output buffer for the middle voltage gain stage. Analysis and design of this amplifier stage are discussed.

A. Cascode configuration and its variants

Cascode configuration is widely used to achieve a higher bandwidth [7], [9]- [10]. It consists of a common-emitter (CE) amplifier, followed by a common-base (CB) amplifier. Both the stages can be realized using NPN transistors, as shown in Fig. 4(a). Under bias condition, this configuration has a high DC voltage $V_{C,CB}$ at the collector of the common base BJT (i.e., its output), limiting the possible signal voltage swing at the output.

This issue is addressed by the folded cascode amplifier

shown in Fig. 4(b) [10], where the CE stage has an NPN transistor, while the CB stage has a PNP one. The collector to emitter voltage of PNP transistor gets subtracted from the collector to base voltage of the NPN transistor, resulting in a low DC voltage at the output. However, the CB transistor requires a low resistance from base to signal ground for higher voltage gain. Further, a high DC voltage at base of CB transistor is desirable to allow maximum voltage swing at its collector, while maintaining the transistor in active region. This is achieved in Fig. 4(b) [10] by using a resistive voltage divider for DC bias and large capacitor C_B for signal ground. This results in high impedance to the signal ground and reduces the low frequency gain. Selection of lower resistances in voltage divider branch may increase the current drawn by the branch. This branch for biasing the PNP transistor in Fig. 4(b) is modified, as shown in Fig. 4(c) [10]. The resistor R'_{B2} provides a low resistance from base to signal ground, while the voltage drop $I_2 R'_{B2}$ determines the DC voltage at base of the PNP transistor. The diode reduces the effect of temperature dependent junction voltage drop of Q_2 on the total bias current for the two transistors.

B. Proposed folded cascode amplifier with buffered output

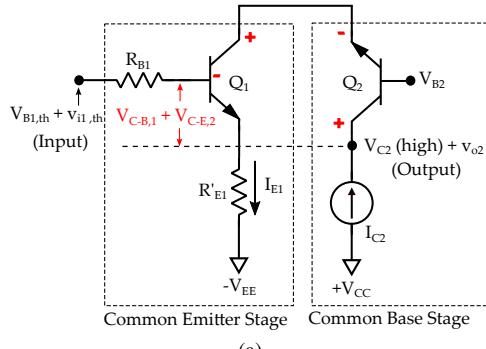
The output of the voltage gain stage needs to be connected to the input of the successive current gain stage realised using a Class AB amplifier with V_{BE} biasing. The DC voltage at the input of current gain stage need not be the same as the DC voltage at the output of CB stage. This demands a capacitive coupling between the two stages. Further, the high output resistance of CB amplifier can result in signal attenuation. The capacitor will also limit the gain at lower frequencies. In this paper, this issue is addressed by using buffered cascode configuration, discussed next. In the proposed cascode configuration, a voltage buffer is connected to the collector (and hence, at the output) of the CB stage. The voltage buffer can be realized using the transistor Q_{CC} in common-collector configuration, biased using the current source I_3 , as shown in Fig. 4(d). The voltage buffer acts as an interface between this stage and the output current gain stage. It isolates the biasing current on the two sides and eliminates the requirement of coupling capacitor to achieve direct coupling. It also offers a very high input impedance and a very low output impedance, thus reducing the loading on the voltage gain stage.

C. Small-signal voltage gain

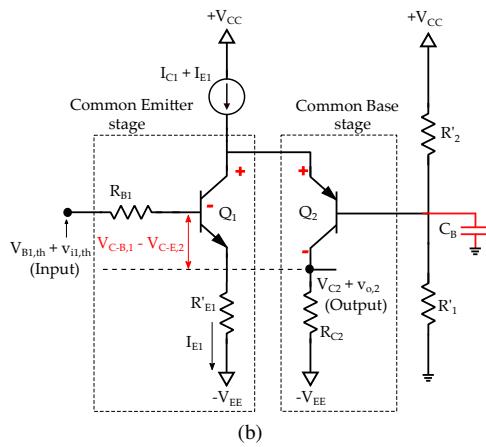
The small signal voltage gain of the amplifier can be expressed in the form of a DC gain A_{vo} , and a single pole ω_H , as

$$A_v(s) = \frac{V_o(s)}{V_{sig}(s)} = \frac{A_{vo}}{1 + \frac{s}{\omega_H}} \quad (1)$$

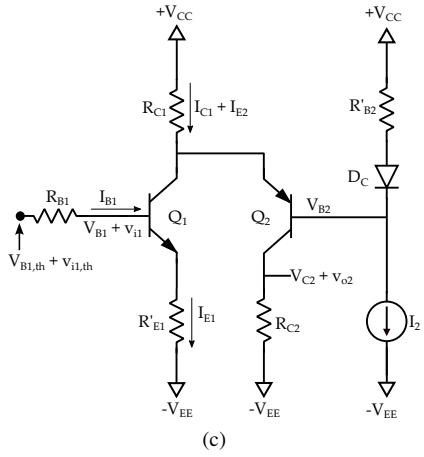
The small signal voltage gain at DC and low frequencies can be given by the small signal equivalent circuit (not shown in the paper) of Fig. 4 (d) as follows:



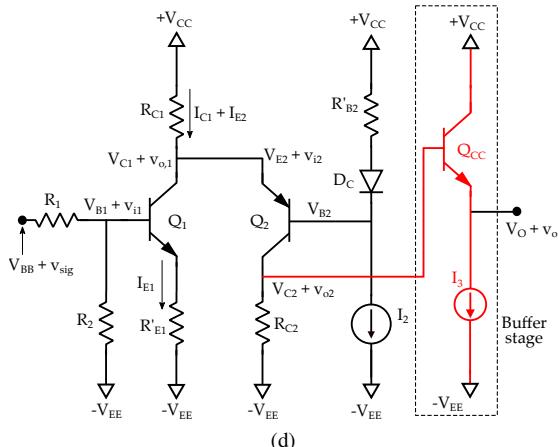
(a)



(b)



(c)



(d)

Fig. 4. (a) Conventional cascode amplifier (b) Folded cascode amplifier with conventional CB biasing (c) Folded cascode amplifier with modified CB biasing (d) Buffered folded cascode stage

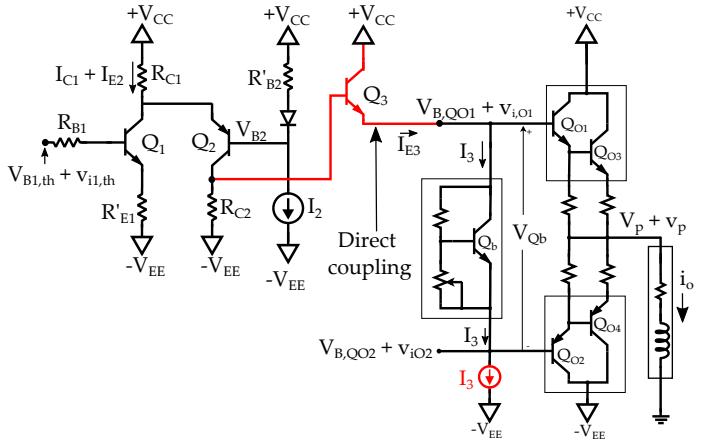


Fig. 5. Buffered folded cascode stage directly coupled with output stage

$$A_{vo} = k A_{v1} A_{v2} \quad (2)$$

$$k = \frac{R_2}{R_1 + R_2} \quad (3)$$

$$A_{v1} = -\beta_1 \frac{R_{out,1}}{R_{in,1} + R_{B1}} \quad (4)$$

$$A_{v2} = \alpha_2 \frac{R_{out,2}}{R_{in,2} + R_{out,1}} \quad (5)$$

The input and output resistances are given by

$$R_{in,1} = (\beta_1 + 1) (r_{e1} + R'_{E1}) \quad (6)$$

$$R_{in,2} = r_{e2} + \frac{(R'_{B2} + r_{DC}) / r_{out,cs}}{\beta_2 + 1} \quad (7)$$

$$R_{out,1} = R_{C1} \quad (8)$$

$$R_{out,2} = R_{C2} \quad (9)$$

where, r_{e1} and r_{e2} are the small signal emitter resistances in T-equivalent models of Q₁ and Q₂ respectively; r_{DC} is the small signal resistance of diode D_C. Hence the overall voltage gain is given by

$$A_{vo} = -k \beta_1 \alpha_2 \frac{R_{out,1}}{R_{in,1} + R_{B1}} \frac{R_{out,2}}{R_{in,2} + R_{out,1}} \quad (10)$$

Assuming that: common-emitter current gains of the BJTs i.e., β_1 and $\beta_2 \gg 1$, $R_{B1} \ll (\beta_1 + 1)(r_{e1} + R'_{E1})$, $r_{out,cs} \approx \infty$, $(R'_{B2} + r_{DC}) \ll (\beta_2 + 1)(r_{e2} + R_{C1})$. Further the bias currents are assumed high enough so that $R_{C1} \gg r_{e2}$. Hence the simplified gain is given by

$$A_{vo} \approx -k \frac{R_{C2}}{R'_{E1} + r_{e1}} \quad (11)$$

The -3 dB bandwidth f_H of the amplifier is determined from the high-frequency small signal model and is given as

$$f_H \approx \frac{1}{2\pi C_{\mu 2} R_{\mu 2}} \quad (12)$$

$$R_{\mu 2} \approx \frac{(R'_{B2} + r_{DC}) R_{C2}}{R_{C1}} + R_{C2} + (R'_{B2} + r_{DC}) \quad (13)$$

where $C_{\mu 2}$ is the collector to base capacitance of the CB

BJT. From (12) and (13), high bandwidth can be achieved by using low values for R_{B2} and R_{C2} , and high value for R_{C1} .

D. Biasing and component selection

The BJTs are biased with bipolar supply (15-0-15 V) to allow signal swing with zero DC offset at output (collector of CB BJT). From Fig. 4(d), the output voltage under peak signal condition can be given as

$$V_{C2} - v_{o2,pk} = -V_{EE} + (I_{C2} - i_{C2,pk}) R_{C2} \quad (14)$$

The amplifier design requires an initial estimate of the bias currents for the two BJTs. The peak signal voltage across base-emitter junctions of the two BJTs during maximum peak output voltage should be a small fraction of thermal voltage V_T . This is to ensure validity of small signal approximation and hence linearity over the required range of output voltage. The condition can be specified as shown below, where the fraction x could take a positive value not higher than 0.25:

$$I_{E1} > v_{o,pk} \frac{R_{in,2} + R_{out,1}}{\alpha_2 R_{out,2}} \frac{1}{\alpha_1 x R_{out,1}} \quad (15)$$

$$I_{E2} > \frac{v_{o,pk}}{\alpha_2 x R_{out,2}} \quad (16)$$

Higher bias current leads to higher bandwidth and linearity over higher peak output voltage $v_{o,pk}$. However it also leads to higher losses. Estimated value of I_{E2} is used for initial estimate of R_{C2} using (14), in order to ensure a zero voltage at output under DC conditions (i.e., $v_{o2,pk}$ and $i_{C2,pk} = 0$).

The equivalent DC voltage $V_{B1,th}$ and equivalent base resistance R_{B1} are realized using a voltage divider network consisting of R_1 and R_2 , as shown in Fig. 4(d). Hence, for $V_{BB} = 0$, $V_{B1,th}$ and R_{B1} are given as

$$V_{B1,th} = -V_{EE}(1 - k) \quad (17)$$

$$R_{B1} = R_1 // R_2 \quad (18)$$

Using KVL, the bias current of the CE BJT Q_1 is mainly decided by the resistor R'_{E1} , and the factor k . It can be given as:

$$I_{E1} = \frac{kV_{EE} - V_{BE,1}}{R'_{E1} + \frac{R_{B1}}{\beta_1 + 1}} \quad (19)$$

In order to have a stable bias current, the effect of temperature dependent terms i.e., $V_{BE,1}$ and β_1 should be minimum. This is ensured by

$$kV_{EE} \gg V_{BE,1} \quad (20)$$

$$R_{B1} \ll (\beta_1 + 1)R'_{E1} \quad (21)$$

The value of I_{C1} can be used to determine initial estimate of R'_{E1} , using (19). However, k is an unknown. Hence, a design equation is obtained by substituting k from (11) in (19), and using (21).

$$R'_{E1} = \frac{-V_{EE}(\frac{A_{vo}}{R_{C2}} \cdot r_{e1}) - V_{BE,1}}{I_{E1} + V_{EE}\frac{A_{vo}}{R_{C2}}} \quad (22)$$

R'_{E1} is estimated using I_{E1} , and a DC gain A_{vo} of 10 V/V. Thereafter k can be obtained by using the estimated values of R_{C2} and R'_{E1} using (11). R_2 and R_3 can be chosen using (21). Thereafter R'_{E1} and R_{C2} are re-estimated based on (19) and (11) respectively. R'_{E1} estimation requires some iterations and a higher value is preferred for bias stability. Thereafter the bias currents of the BJTs need to be recalculated.

The sum of bias currents of the two BJTs is set by the current source I_2 , resistances R'_{B2} , R_{C1} , and diode D_c . This is given as

$$(I_{C1} + I_{E2}) \cdot R_{C1} + V_{BE,2} = I_2 \cdot R'_{B2} + V_{D_c} \quad (23)$$

The currents and therefore, the temperatures of Q_2 and D_c are similar. Hence, their respective drops could be assumed to be equal. Hence, the total bias current becomes thermally stable, and given as

$$I_{C1} + I_{E2} = I_2 \cdot \frac{R'_{B2}}{R_{C1}} \quad (24)$$

The biasing of the BJTs should allow the required signal voltage swing at output, while maintaining the transistors in active region. The condition for collector-base junctions of Q_2 and Q_1 to be reverse biased can be specified as (25) and (26) respectively.

$$V_{CC} - V_{D_c} - I_2 R'_{B2} - V_{C2} > v_{o2,pk} \quad (25)$$

$$V_{CC} - I_2 R'_{B2} - V_{B1} > v_{o,pk} \left(\frac{1 + A_{v1}}{A_{v1} A_{v2}} \right) \quad (26)$$

The signal voltage at base of Q_2 is assumed to be negligible. Using (21), V_{B1} can be given as

$$V_{B1} = V_{B1,th} - (V_{EE} - V_{BE,1}) \frac{R_{B1}}{(\beta_1 + 1) R'_{E1}} \quad (27)$$

From (25) and (26), the voltage drop $I_2 R'_{B2}$ needs to be minimum to allow maximum signal swing at output. Further, R'_{B2} also needs to be low to achieve a higher bandwidth as per (13). Hence the highest value of I_2 is chosen and R'_{B2} is chosen to be a small value. Finally, R_{C1} is chosen to set the total bias current of the two BJTs using (24). The designed values are given in Table-I. The voltage and current ratings of the transistors are chosen to be more than the bias requirements.

III. EXPERIMENTAL RESULTS

The proposed buffered folded cascode amplifier circuit is designed and fabricated as shown in Fig. 6. The amplifier is excited using a function generator Keysight 33500B. The output signal is measured using the oscilloscope DPO2024B (200 MHz, 1 GS/s) and voltage probe TPP0200 in 10x (200 MHz, 10 MΩ, <12 pF).

TABLE I
COMPONENT VALUES FOR DESIGNED AMPLIFIER

Item	Value
Target A_{vo}	10
I_{B2}	10 mA
R_1	2.7 kΩ
R_2	150 Ω
R_{C1}	100 Ω
R_{C2}	4.7 kΩ
R'_{B2}	100 Ω
R'_{E1}	27 Ω
Q1	2N6517 (350 V, 0.5 A)
Q2	2N6519 (300 V, 0.5 A)
Q3	2N3904 (40 V, 0.2 A)

A. Measured frequency response

Fig. 9(a) shows a comparison of frequency responses of folded cascode amplifier with and without the buffer transistor. It is seen that the buffer transistor reduces the capacitive loading of the probe at higher frequencies. Fig. 9(b) compares the frequency responses of the buffered folded cascode amplifier with and without the V_{BE} multiplier in the buffer stage circuit. It is seen that the inclusion of V_{BE} multiplier does not affect the frequency response of the amplifier. Hence the buffer transistor and the V_{BE} multiplier of output stage can be biased using the same current source. Fig. 9(c) compares the frequency responses of the common emitter amplifier and the proposed buffered cascode amplifier. The V_{BE} multiplier of the output stage was connected whereas the driver transistors were disconnected. The proposed modified cascode amplifier offers improved gain-bandwidth product of 16.38 MHz, as compared to 4.51 MHz of CE amplifier.

B. Closed-loop amplifier

The fabricated cascode amplifier circuit as shown in Fig. 6 replaces the CE amplifier circuit in the middle stage of the 15 V linear power amplifier discussed in [8]. The input and output voltage waveforms of the three-stage direct-coupled LPA utilizing proposed buffered cascode based middle stage are shown in Fig. 10. The overall voltage gain of the LPA is set by the input differential stage.

C. Measured B-H characteristics

The LPA is used to characterize a ferrite core material using ring-specimen method (as shown in Fig.1) upto a peak flux density of 0.23 T at 50 Hz, 400 Hz, and 1 kHz. The complete setup is shown in Fig. 8. The experimental waveforms of secondary induced voltage, core flux-linkage, and primary coil current at 1 kHz are shown in Fig.11. The secondary voltage and primary current are used to determine the B-H loop at 1 kHz, as shown in Fig.12.

IV. CONCLUSIONS

A low-cost voltage amplifier with high gain-bandwidth product along with being suitable for direct-coupled multistage linear power amplifier is proposed, fabricated and validated.

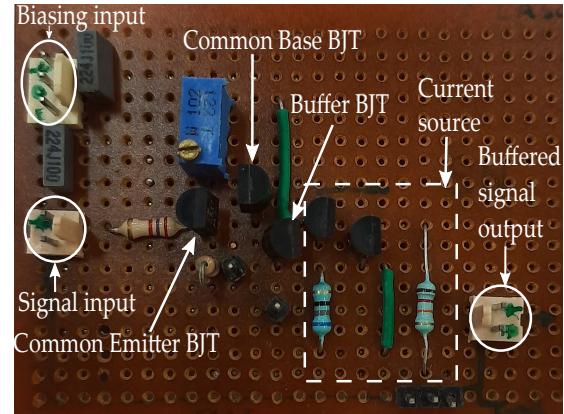


Fig. 6. Fabricated cascode board

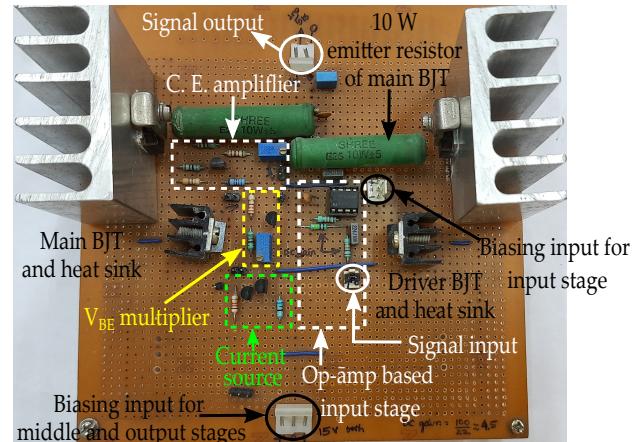


Fig. 7. Complete linear power amplifier with CE middle stage [8]

The proposed structure enables characterization of magnetic materials at both very low and high frequencies, while providing a large voltage gain. Direct coupling with Class AB current amplifier is demonstrated. The higher gain-bandwidth product of the proposed buffered folded cascode amplifier as compared to conventional CE amplifier is experimentally verified. The proposed amplifier is used in the three stage LPA to experimentally obtain the B-H characteristics of a ferrite core.

REFERENCES

- [1] R. Raj, B. S. Ram, R. Bhat, G. M. Unniachanparambil and S. V. Kulkarni, "A Novel Cost-Effective Magnetic Characterization Tool for

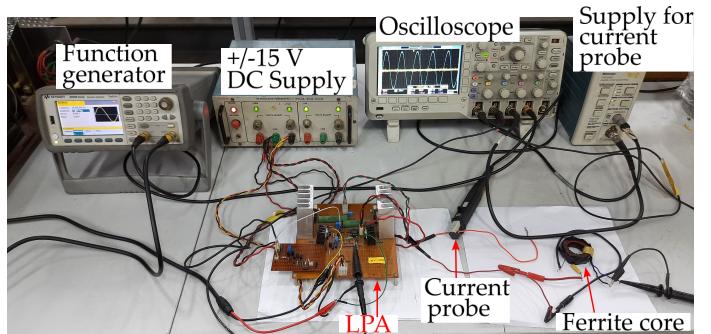


Fig. 8. Complete experimental setup

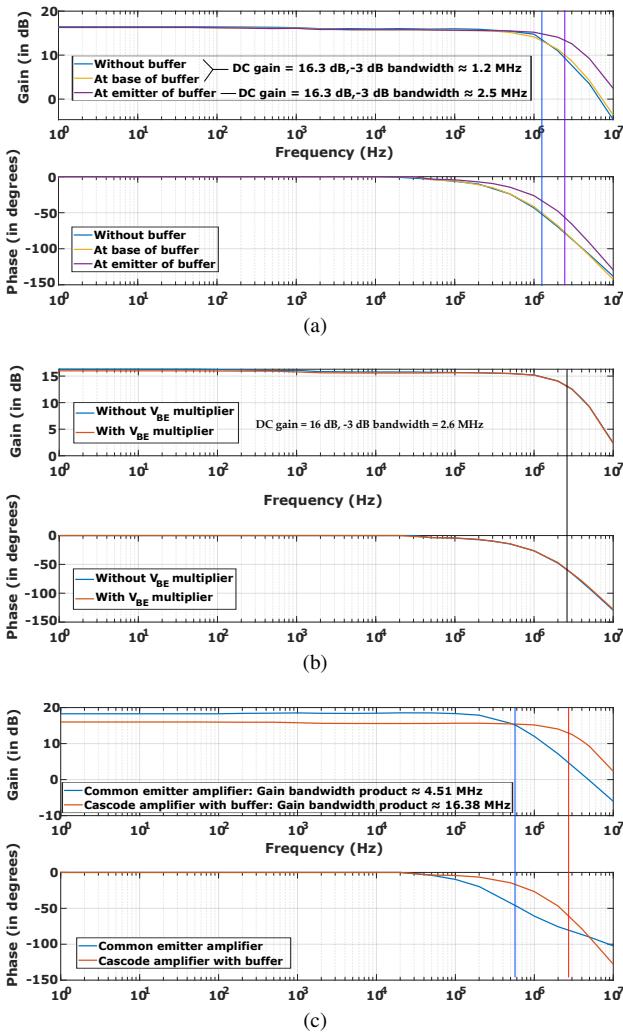


Fig. 9. Experimental frequency response of (a) Folded cascode amplifier with and without buffer stage (b) Proposed buffered cascode amplifier with and without V_{BE} multiplier (c) Common-emitter and buffered cascode amplifier with V_{BE} multiplier

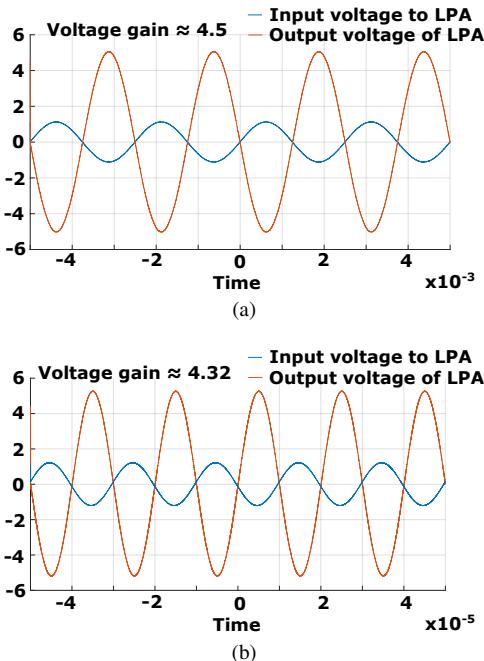


Fig. 10. Experimental closed loop output voltages at no load for (a) 400 Hz (b) 50 kHz

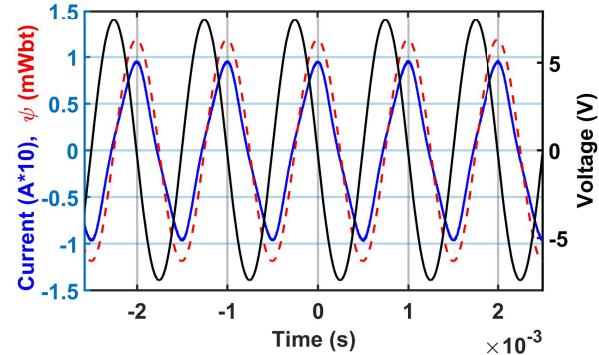


Fig. 11. Secondary induced voltage, flux linkage, and primary currents for ferrite core at 1 kHz

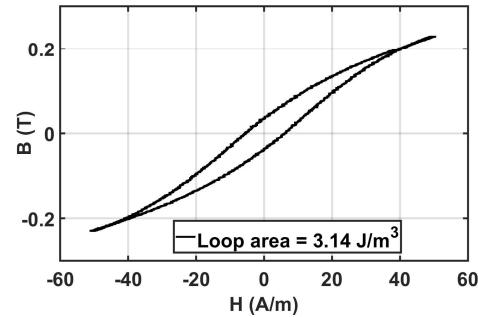


Fig. 12. Experimental B-H curve for ferrite core at 1 kHz

- Soft Magnetic Materials Used in Electrical Machines," *IEEE Trans. Instrum. and Meas.*, vol. 70, pp. 1-8, 2021, Art no. 6009508, doi: 10.1109/TIM.2021.3099558.
[2] C. Urabinahatti, S. S. Ahmad and G. Narayanan, "Magnetic Characterization of Ferromagnetic Alloys for High-Speed Electric Machines," in *IEEE Trans. Industry Appl.*, vol. 56, no. 6, pp. 6436-6447, Nov.-Dec. 2020, doi: 10.1109/TIA.2020.3023868.
[3] L. K. Rodrigues and G. W. Jewell, "Model Specific Characterization of Soft Magnetic Materials for Core Loss Prediction in Electrical Machines," *IEEE Trans. Magn.*, vol. 50, no. 11, pp. 1-4, Nov. 2014, Art no. 2105204, doi: 10.1109/TMAG.2014.2328099.
[4] J. H. J. Potgieter, F. J. Márquez-Fernández, A. G. Fraser and M. D. McCulloch, "Effects Observed in the Characterization of Soft Magnetic Composite for High Frequency, High Flux Density Applications," *IEEE Trans. Ind. Electron.*, vol. 64, no. 3, pp. 2486-2493, March 2017, doi: 10.1109/TIE.2016.2606371.
[5] S. Zurek, P. Marketos, T. Meydan and A. J. Moses, "Use of novel adaptive digital feedback for magnetic measurements under controlled magnetizing conditions," *IEEE Trans. Magn.*, vol. 41, no. 11, pp. 4242-4249, Nov. 2005, doi: 10.1109/TMAG.2005.854438.
[6] B. M. Koprivica and M. V. Plazinić, "Measurement System for Characterization of Ferromagnetic Cores Under Controlled Magnetic Field Waveform," *IEEE Magn. Lett.*, vol. 13, pp. 1-5, 2022, Art no. 8103005, doi: 10.1109/LMAG.2022.3155107.
[7] Sedra, A. S., & Smith, K. C. (1982). Microelectronic circuits. New York: Holt, Rinehart and Winston.
[8] S. S. Ahmad, A. Raj and G. Narayanan, "Low-cost Multistage Direct-Coupled Linear Power Amplifier for Characterization of Magnetic Cores at Multiple Frequencies," *2021 Nat. Power Electron. Conf. (NPEC)*, 2021, pp. 1-6, doi: 10.1109/NPEC52100.2021.9672514.
[9] Z. Pan, C. Yang, R. Feng, M. Qi, Q. Luo and M. Zhu, "The Design of a Low Distortion Power Amplifier Based on Cascode," *2019 22nd Int. Conf. Elect. Mach. and Syst. (ICEMS)*, 2019, pp. 1-4, doi: 10.1109/ICEMS.2019.8921594.
[10] D. L. Feucht. (2017, February) Cascode amplifiers. [Online]. Available: https://ieeeli/pdf/essay/cascode_amplifiers.pdf