Lambda Design Rules

n-Well

r101	Minimum well size	12 λ
r102	Between wells	12 λ
r110	Minimum well area	144 $λ^2$

R101   R101
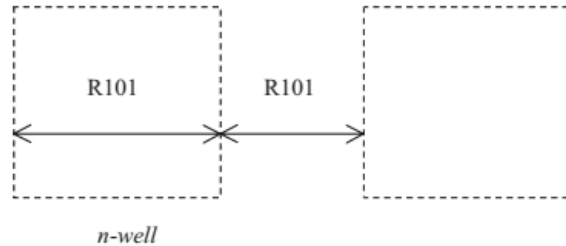
n-well

Diffusion

r201	Minimum N+ and P+ diffusion width	4 λ
r202	Between two P+ and N+ diffusions	4 λ
r203	Extra nwell after P+ diffusion :	6 λ
r204:	Between N+ diffusion and nwell	6 λ
r205	Border of well after N+ polarization	2 λ
r206	Between N+ and P+ polarization	0 λ
r207	Border of Nwell for P+ polarization	6 λ
r210	Minimum diffusion area	24 $λ^2$

Nwell Polarization

r 203   P+ diff   r 202   P+ diff   N+   r 205

r201   r206   *nwell*

r204   r207

N+ diff   P+   P+ polarization

r206
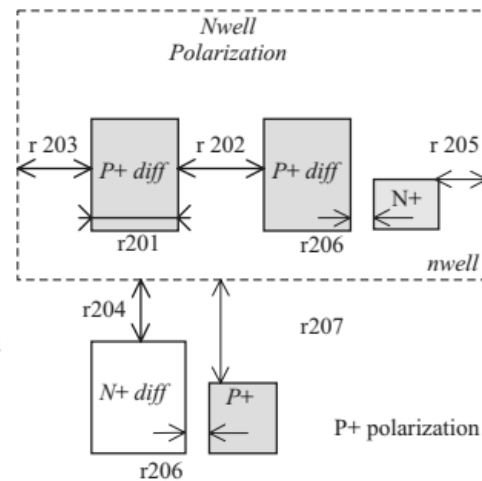
Polysilicon

r301	Polysilicon width	2 λ
r302	Polysilicon gate on diffusion	2 λ
r303	Polysilicon gate on diffusion for high voltage MOS	4 λ
r304	Between two poly silicon boxes	3 λ
r305	Polysilicon vs. other diffusion	2 λ
r306	Diffusion after polysilicon	4 λ
r307	Extra gate after polysilicon	3 λ
r310	Minimum surface	8 $λ^2$

r305

P+ diff   r306

r302

r301   r304

N+ diff   r306

r307

r303

High voltage MOS
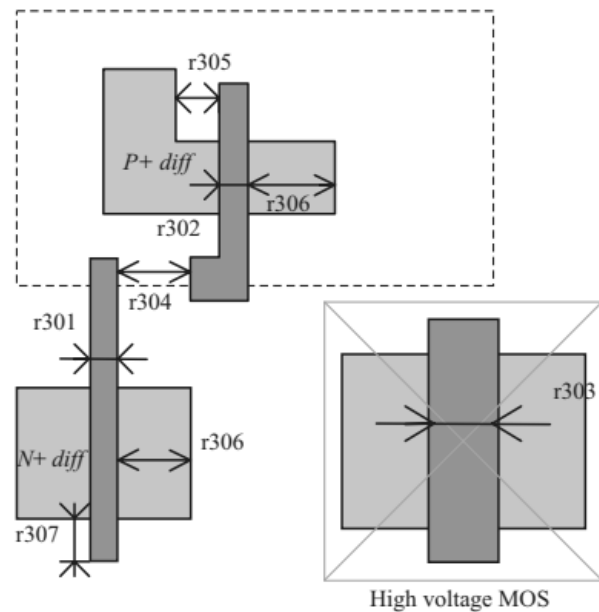
A.2.1 Second Polysilicon Design Rules

r311	Polysilicon2 width	2λ
r312	Polysilicon2 gate on diffusion	2λ
r320	Polysilicon2 minimum surface	$8\lambda^2$

MOS Option

rOpt	Border of "option" layer over diff N+ and diff P+	7λ

Contact

r401	Contact width	2λ
r402	Between two contacts	5λ
r403	Extra diffusion over contact	2λ
r404	Extra poly over contact	2λ
r405	Extra metal over contact	2λ
r406	Distance between contact and poly gate	3λ
r407	Extra poly2 over contact	2λ

Metal 1

r501	Metal width	4λ
r502	Between two metals	4λ
r510	Minimum surface	$16\lambda^2$

Via

r601	Via width	2λ
r602	Between two Via	5λ
r603	Between Via and contact	0λ
r604	Extra metal over via	2λ
r605	Extra metal 2 over via:	2λ
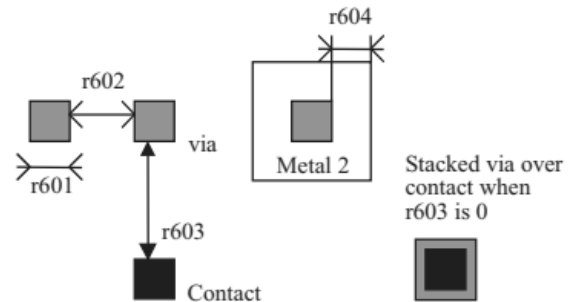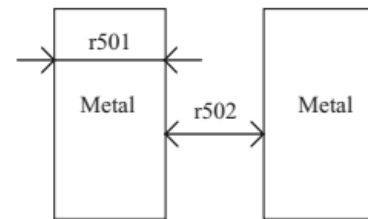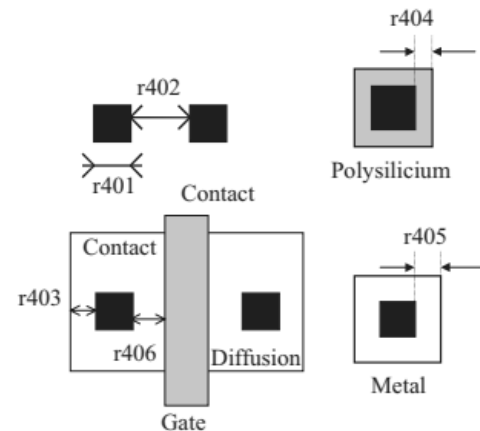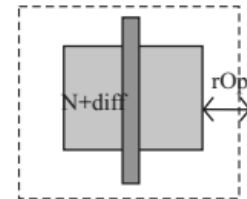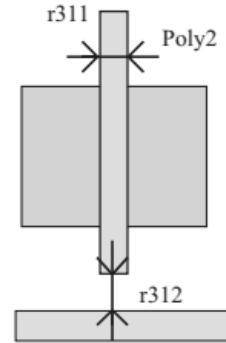
Metal 2

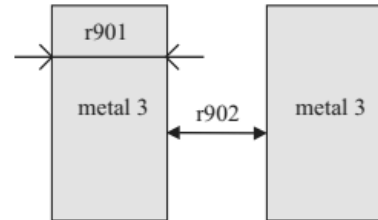|		
r701	Metal width:	4λ
r702	Between two metal 2	4λ
r710	Minimum surface	$16\lambda^2$
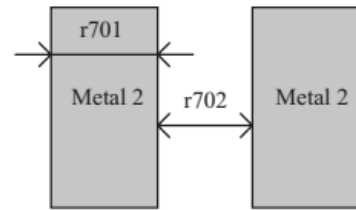
Via 2

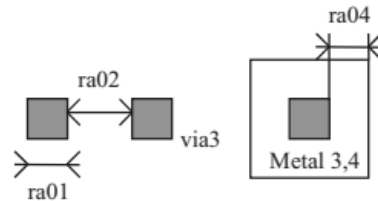|	
r801	Via2 width: 2λ
r802	Between two via2: 5λ
r804	Extra metal 2 over via2: 2λ
r805	Extra metal 3 over via2: 2λ
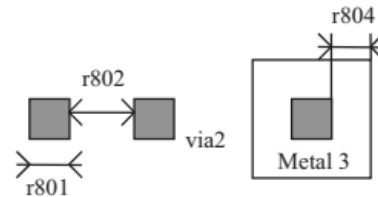
Metal 3

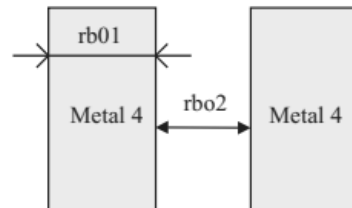|	
r901	Metal 3 width: 4λ
r902	Between two metal 3: 4λ
r910	Minimum surface: $32\lambda^2$

Via 3

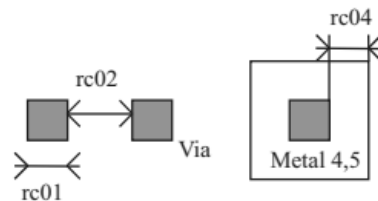|	
ra01	Via3 width: 2λ
ra02	Between two via3: 5λ
ra04	Extra metal 3 over via3: 2λ
ra05	Extra metal 4 over via3: 2λ

Metal 4

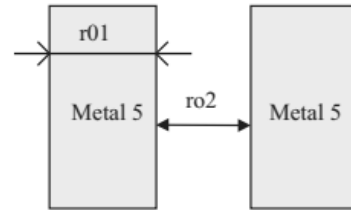|	
rb01	Metal 4 width: 4λ
rb02	Between two metal 4: 4λ
rb10	Minimum surface: $32\lambda^2$

Via 4

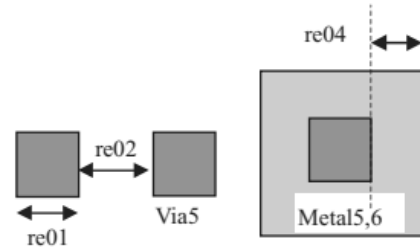|	
rc01	Via4 width: 2λ
rc02	Between two via4: 5λ
rc04	Extra metal 4 over via2: 3λ
rc05	Extra metal 5 over via2: 3λ

Metal 5

<div>

   rd01   Metal 5 width: 8 λ

   rd02   Between two metal 5: 8 λ

   rd10   Minimum surface: 100 λ^2

</div>

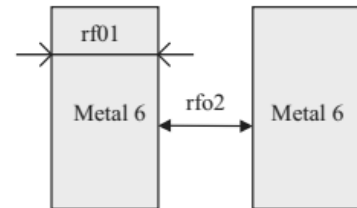**Via 5**

   re01   Via5 width: 4 λ

   re02   Between two via5: 6 λ

   re04   Extra metal 5 over via5: 3 λ

   re05   Extra metal 6 over via5: 3 λ

Metal 6

   rf01   Metal 6 width: 8 λ

   rf02   Between two metal 6: 15 λ

   rf10   Minimum surface: 300 λ^2

A.3 Pads

The rules are presented below in μm. In .RUL files, the rules are given in lambda. As the pad size has an almost constant value in μm, each technology gives its own value in λ.

   rp01   Pad width: 100 μm

   rp02   Between two pads   100 μm

   rp03   Opening in
           passivation v.s via: 5 μm

   rp04   Opening in
           passivation v.s metals: 5 μm

   rp05   Between pad and
           unrelated active area: 20 μm