Verilog Practise Assignment

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1 Half Adder

1.1 Truth Table

A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Table 1: Truth Table for Half Adder

1.2 Verilog Code

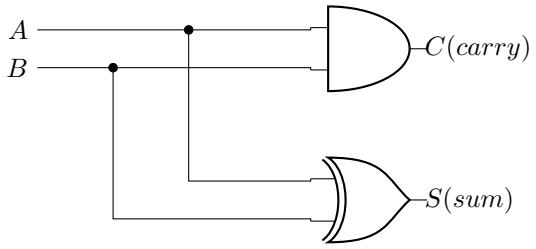
Structural Style

```
module halfadder(s,c,a,b);
    input a,b;
    output s,c;
    xor g1(s,a,b);
    and g2(c,a,b);
endmodule
```

Behavioral Style

```
module halfadder(s,c,a,b);
    input a,b;
    output s,c;
    assign s = a^b;
    assign c = a&b;
endmodule
```

1.3 Logic Diagram



2 Full Adder

2.1 Truth Table

A	B	C_0	S	C
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table 2: Truth Table for Full Adder

2.2 Verilog Code

Structural Style

```
module fulladder(s,c,a,b,c0);
    input a,b,c0;
    output s,c;
    wire t1,t2,t3;
    xor g1(t1,a,b);
    xor g2(s,c0,t1);
    and g3(t2,a,b);
    and g4(t3,t1,c0);
    or g5(c,t2,t3);
endmodule
```

Behavioral Style

```
module fulladder(s,c,a,b,c0);
    input a,b,c0;
    output s,c;
    assign s = a^b^c0;
    assign c = a&b | b&c0 | c0&a;
endmodule
```

2.3 Logic Diagram