

# Problem Set 3 Guide

## ECE636: Reconfigurable Computing



Electrical and Computer Engineering  
University of Massachusetts, Amherst

# Overview of Slides

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- These slides will provide step-by-step details on downloading the software you need to complete the assignment and the specific steps needed to run the software
- The directions here should be used in conjunction with the “assignment3.pdf” handout for the assignment
- Step 1: Download CD-ROM for your DE1-SoC board
  
- Step 2: Download and install Quartus Prime version 16.1 on your PC
  
- Step 3: Download and install Intel Monitor Program on your PC
  
- Step 4: Synthesize and simulate your fir.v design using Quartus Prime and ModelSim
  
- Step 5: Synthesize board-level fir.v design using Quartus and compile C program using Intel Monitor Program
  
- Step 6: Download and run FPGA and compiled C code to DE1-SoC using Monitor Program

# Determine the Version of Your DE1-SOC

- <http://www.terasic.com.tw/cgi-bin/page/archive.pl?Language=English&No=88>
- Determine your DE1-SOC board version

DE1-SoC Board How to distinguish rev. B, rev. C, rev. D, rev. E and rev. F board?



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## How to distinguish rev. B, rev. C, rev. D, rev. E and rev. F board?

Simply check the serial number on the board.

rev. B



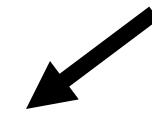
# Download CD-ROM for your DE1-SOC

- <http://www.terasic.com.tw/cgi-bin/page/archive.pl?Language=English&CategoryNo=205&No=836&PartNo=4>
- Note that you must use a 64-bit computer to compile designs for the DE1-SOC

Click on disk to download

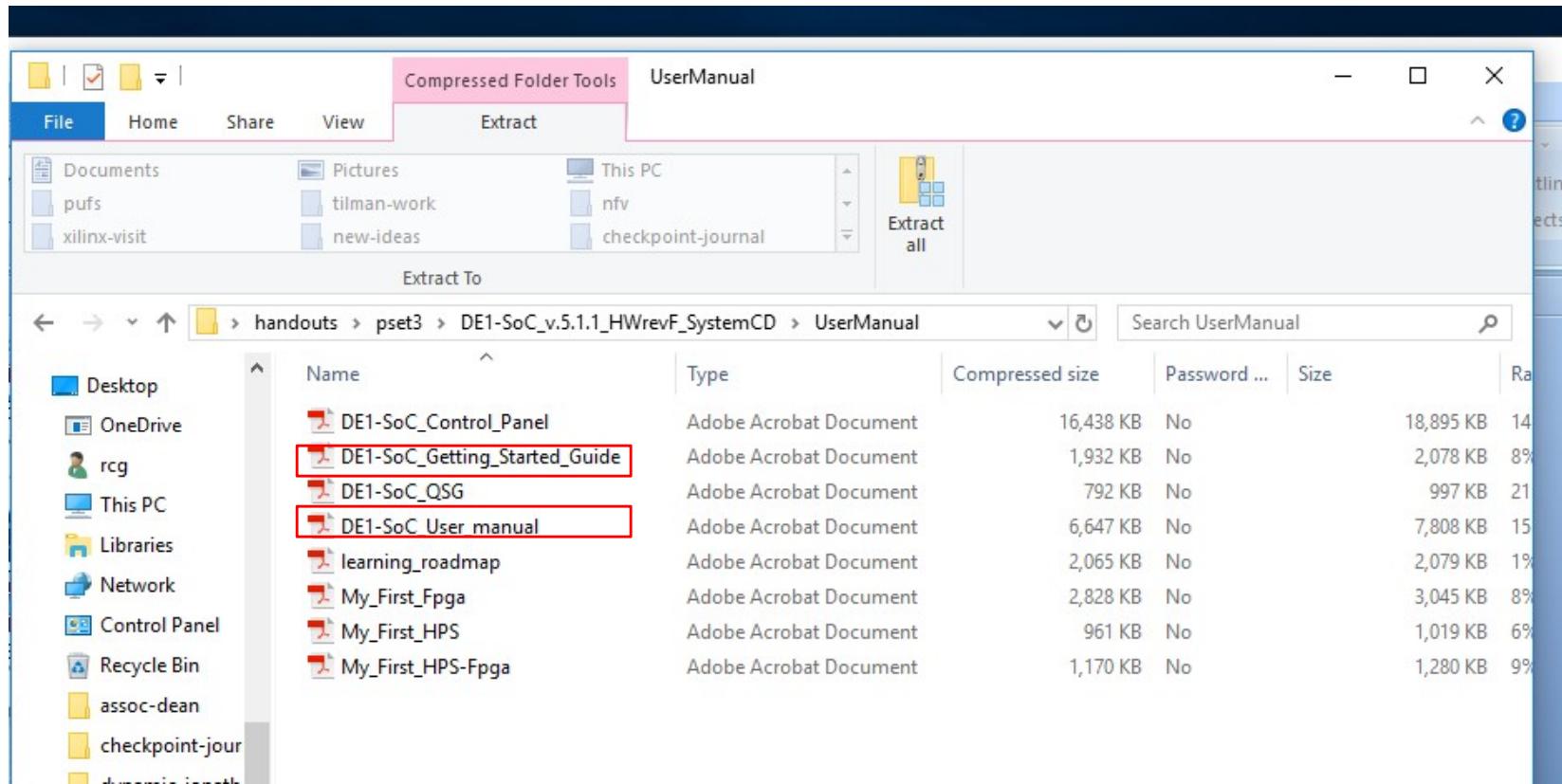
## CD-ROM

Title	Version	Size(KB)	Date Added	Download
Quartus Download			2013-12-26	
DE1-SoC System Builder	1.1.1		2016-09-02	
DE1-SoC CD-ROM (rev.B Board)	1.2.0		2014-03-25	
DE1-SoC CD-ROM (rev.C/rev.D Board)	3.1.3		2015-04-08	
DE1-SoC CD-ROM (rev.E Board)	4.0.3		2015-08-07	
DE1-SoC CD-ROM (rev.F Board)	5.1.1		2016-09-07	



( 64-bit OS and Quartus II 64-bit are required to compile projects for DE1-SoC )

# Get Users Manual and Getting Started Guide



- Locate DE1-SOC Users Manual and Getting Started Guide in CD-ROM UserManual directory. These will be used to complete the assignment 3 exercises

# Download and Install Quartus Prime v16.1

- Section 2.2 of the Getting Started Guide provides insights into installing Quartus Prime
- Go to download page for Quartus Prime
- <https://www.altera.com/downloads/download-center.html>

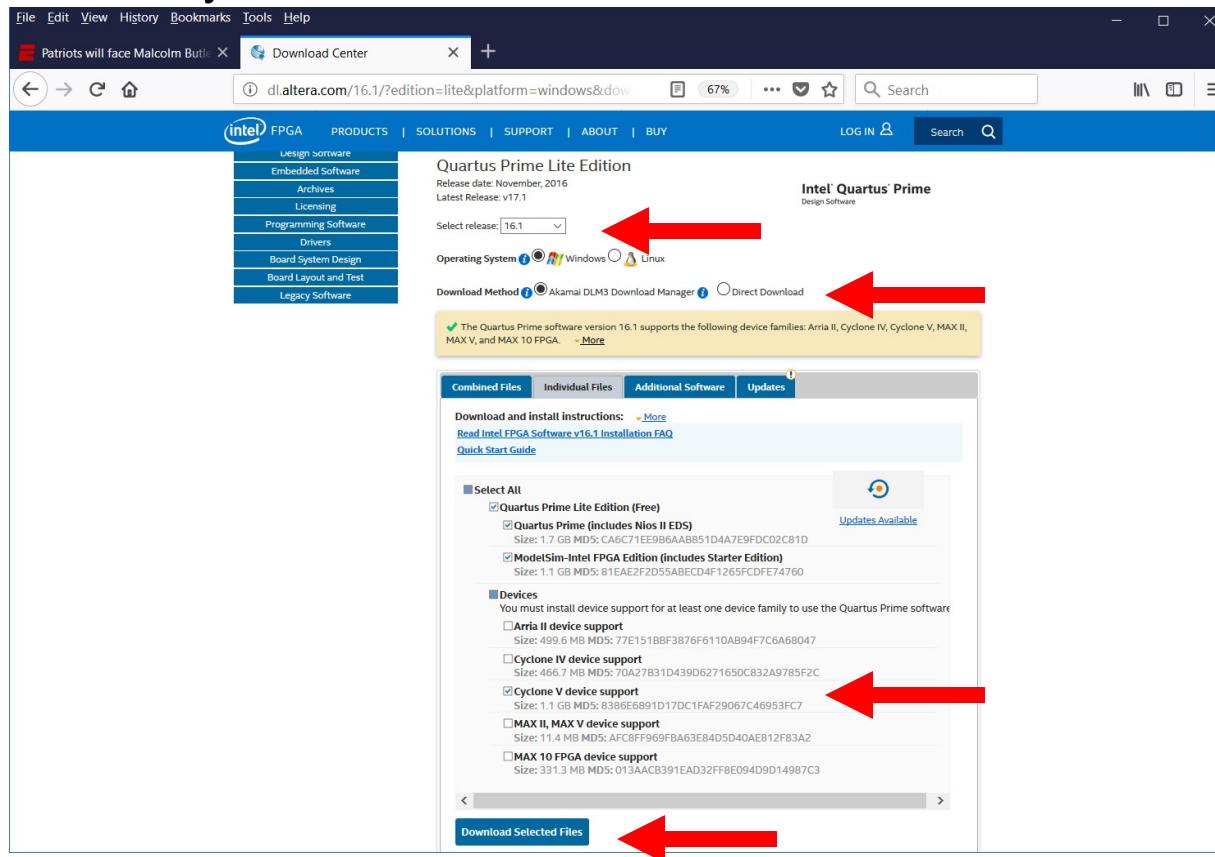
The screenshot shows a web browser window with the URL <https://www.altera.com/downloads/download-center.html>. The page is titled "Three Intel® Quartus® Prime Software Editions to Meet Your System Design Requirements". It features a sidebar with links like Design Software, Embedded Software, Archives, Licensing, Programming Software, Drivers, Board System Design, Board Layout and Test, and Legacy Software. The main content area highlights three editions:

Pro Edition <sup>1,2,3</sup>	Standard Edition <sup>1,2</sup>	Lite Edition <sup>1,4</sup>
Paid license required The Intel® Quartus® Prime Pro Edition software supports the advanced features in Intel's next-generation FPGAs and SoCs with the Intel Stratix® 10, Intel Arria® 10, and Intel Cyclone® 10 GX device families.	Paid license required The Intel Quartus Prime Standard Edition software includes extensive support for earlier device families in addition to the Intel Cyclone 10 LP device family.	FREE, no license required The Intel Quartus Prime Lite Edition software supports Intel's low-cost FPGA device families.

At the bottom, there are three "Download" buttons with arrows pointing to the right. A large black arrow points from the text "Click here" to the "Download" button for the Lite Edition.

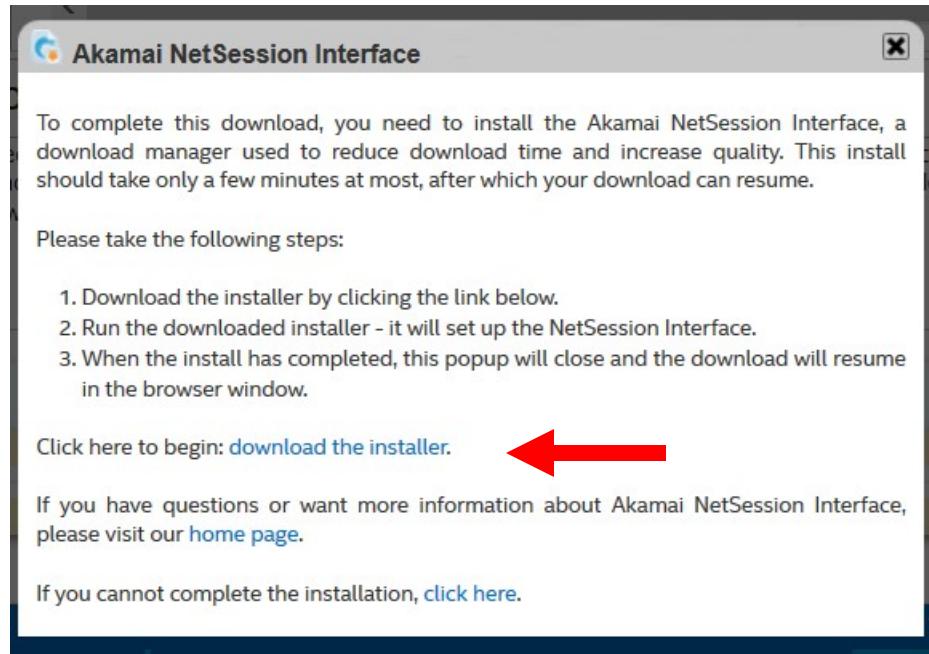
# Download Quartus Prime v16.1

- Choose Akamai download
- Only need files for Cyclone V



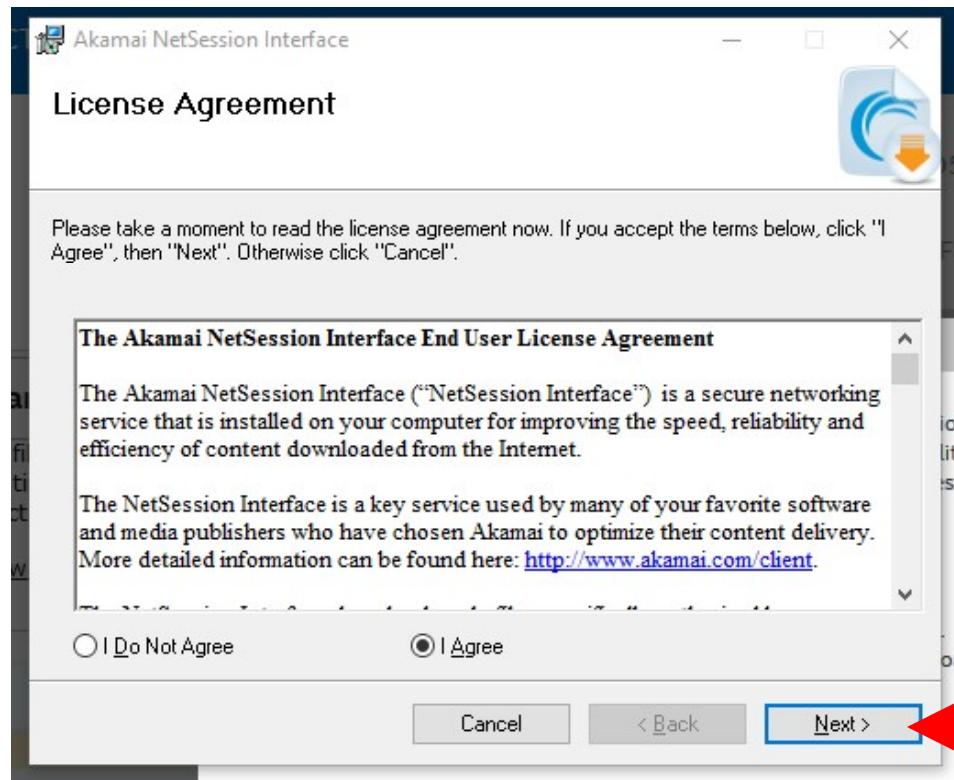
# Download Quartus Prime v16.1

- You may be prompted to enter in a user name and password to download Quartus Prime. Please create an account and enter the information
- You will need to download and install Akamai Installer software before the Quartus download starts

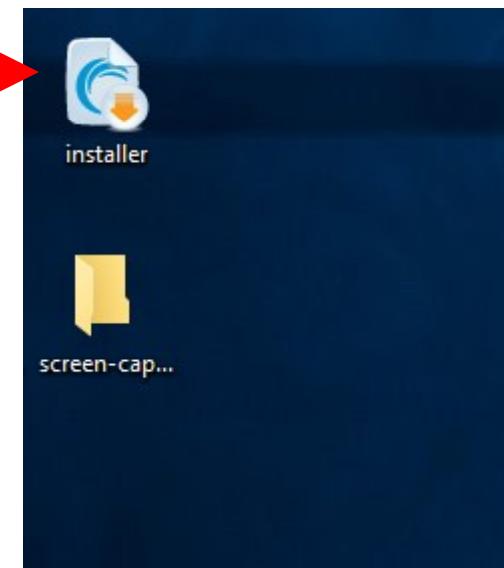


# Download Quartus Prime 16.1

- Agree to download the Akamai Installer
- Click on “installer” icon when download is finished to install the Akamai installer



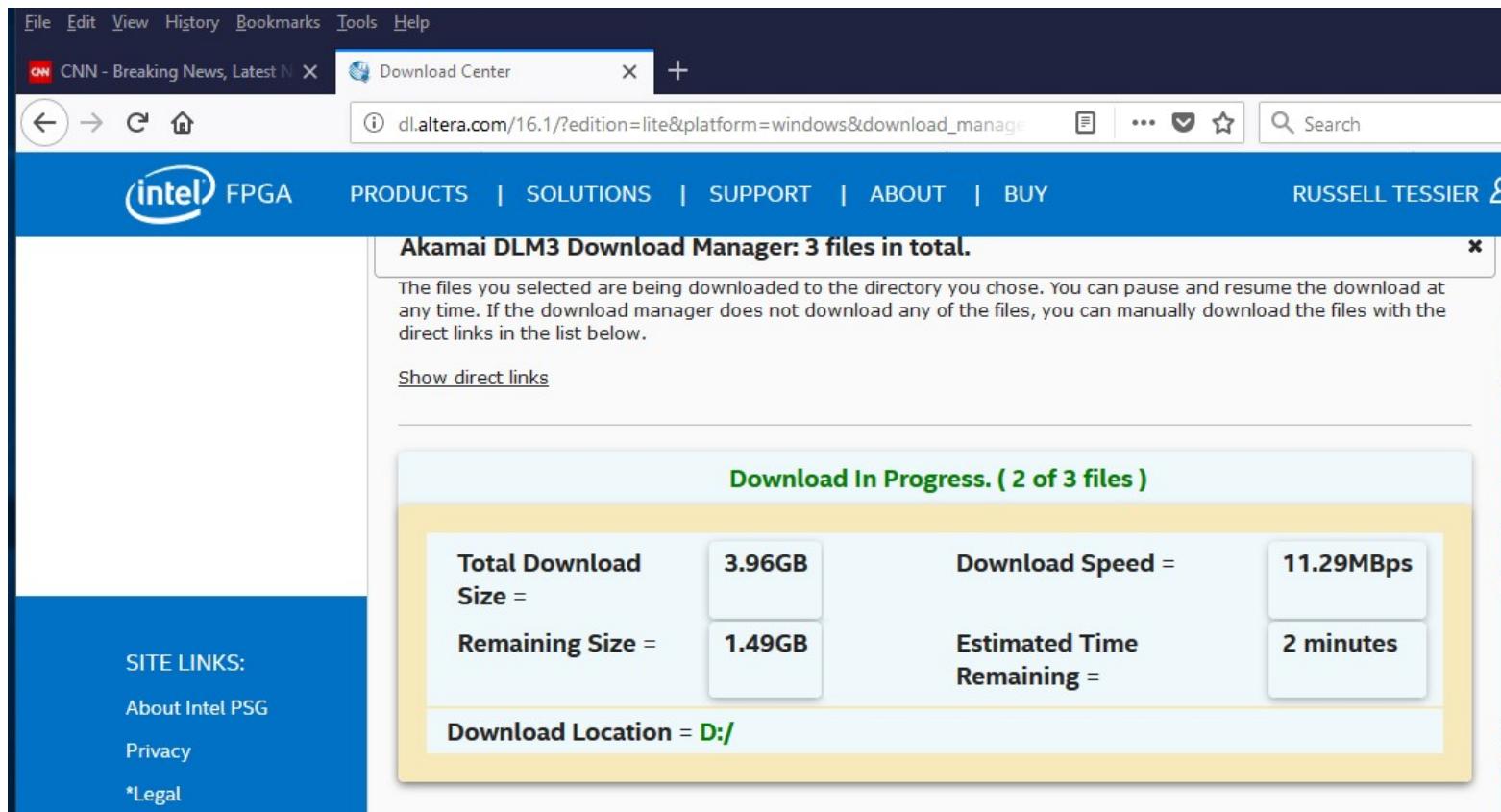
Click to install



Click to download

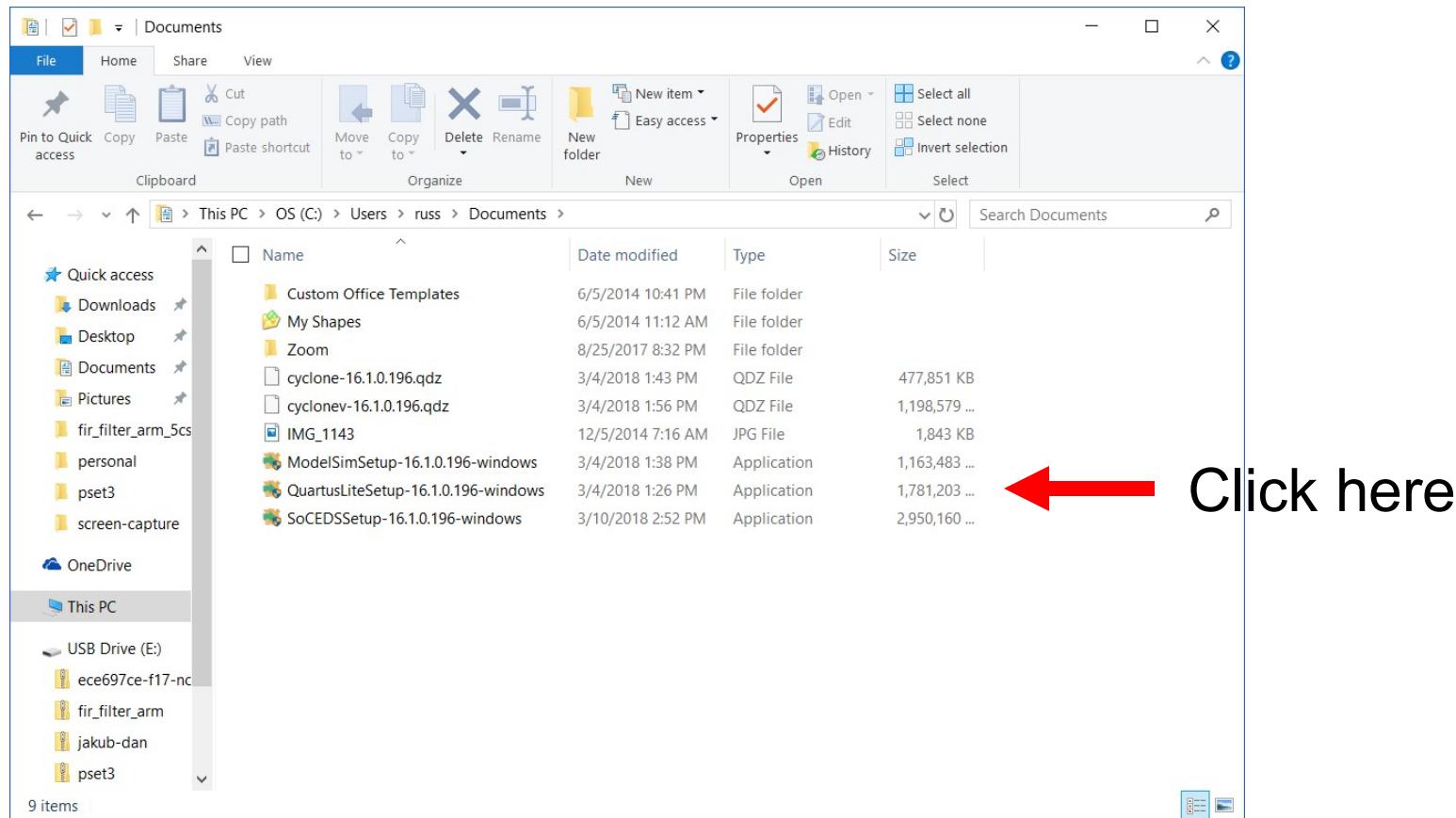
# Download Quartus Prime v16.1

- You may be asked for download directory for Quartus Prime v16.1 software
- Quartus download will start after Akamai installer finishes



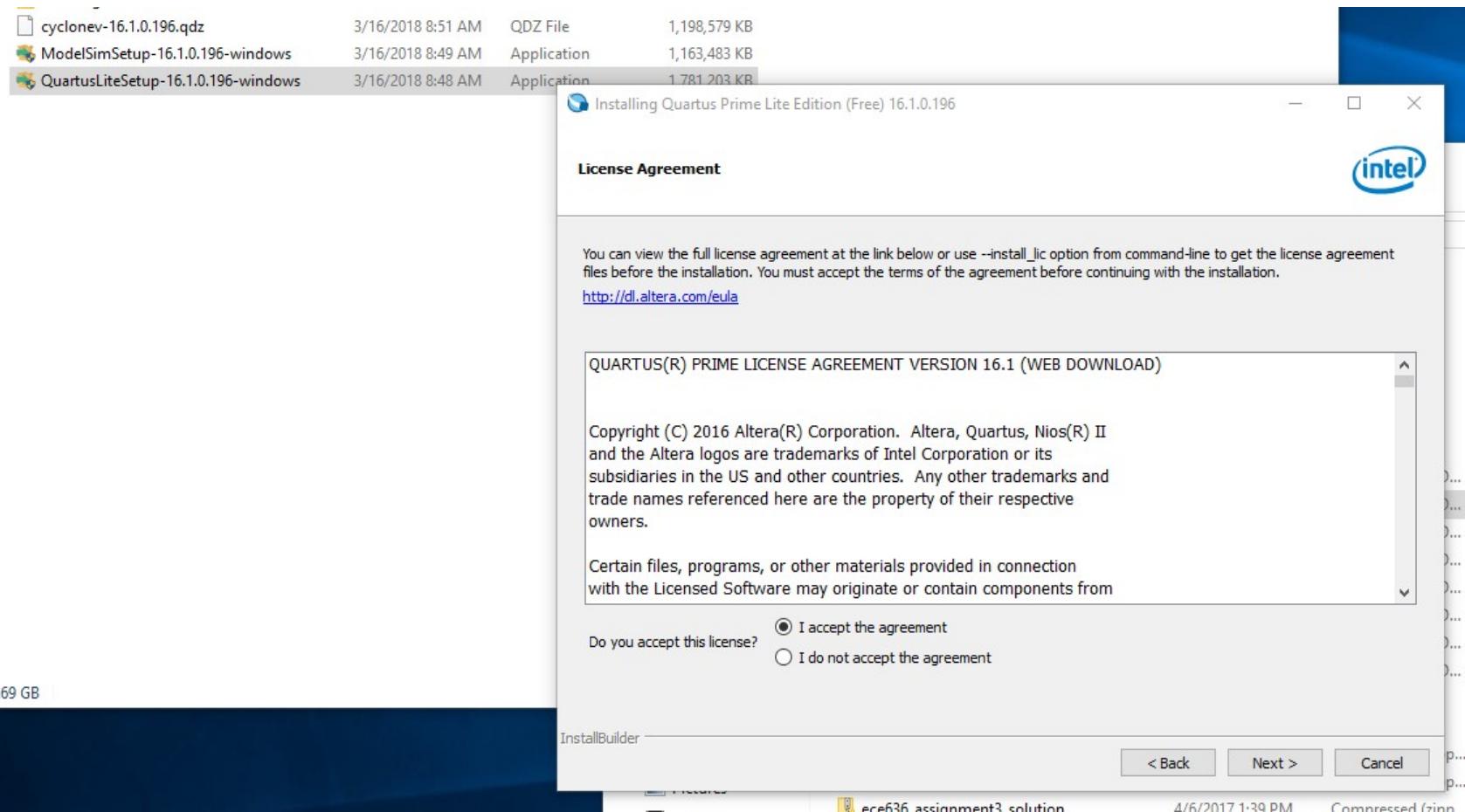
# Start Quartus Prime v16.1 Install

- Locate the Quartus Prime install file and click on it. Modelsim and USB drivers will also be installed



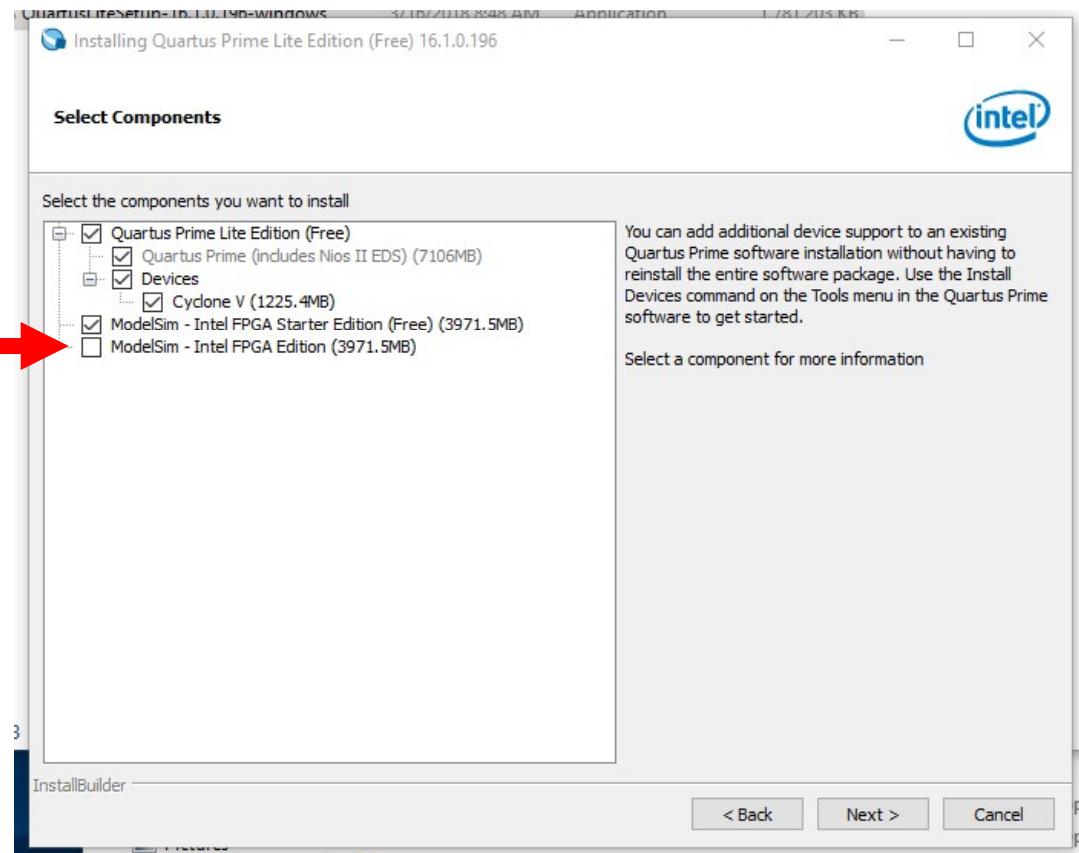
# Install Quartus Prime v16.1

- Select “I accept the agreement” and click ‘Next’ button



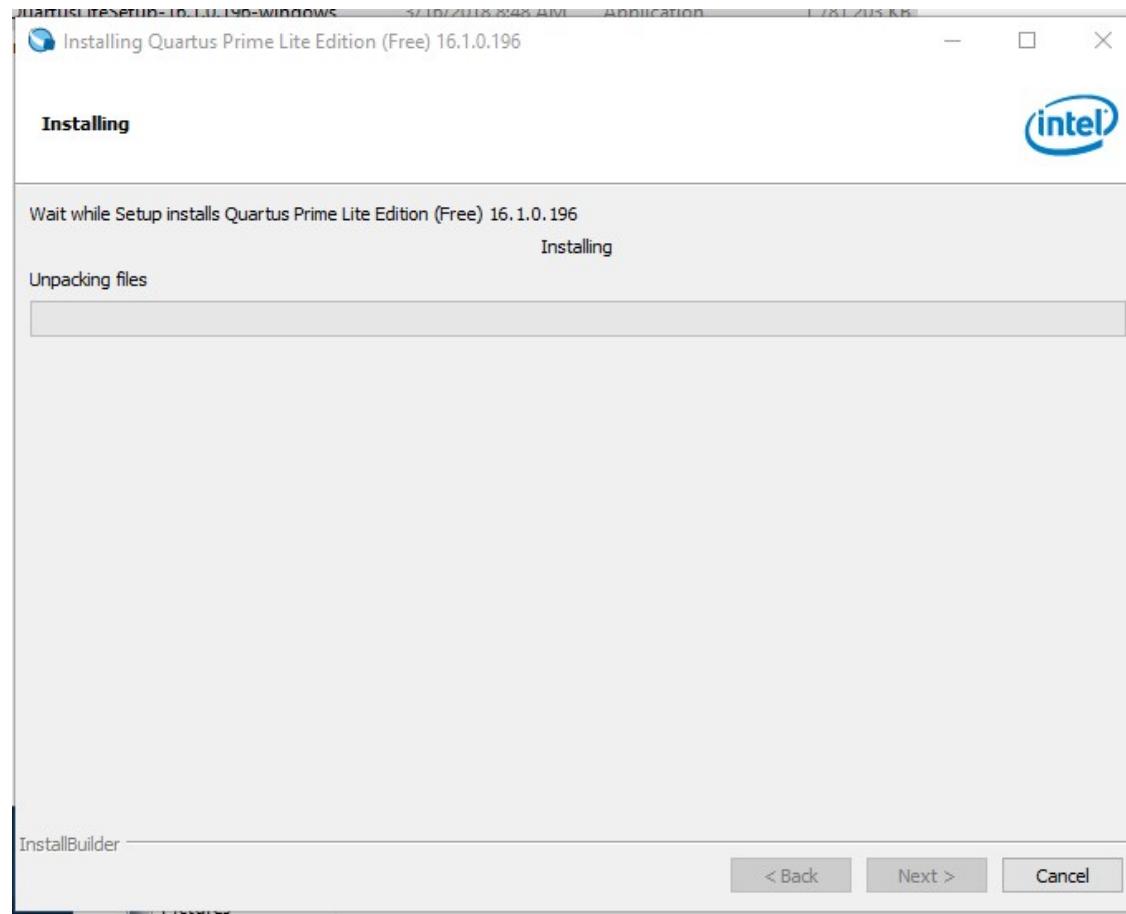
# Install Quartus Prime v16.1

- Unclick “Modelsim – Intel FPGA Edition” and click “Next”



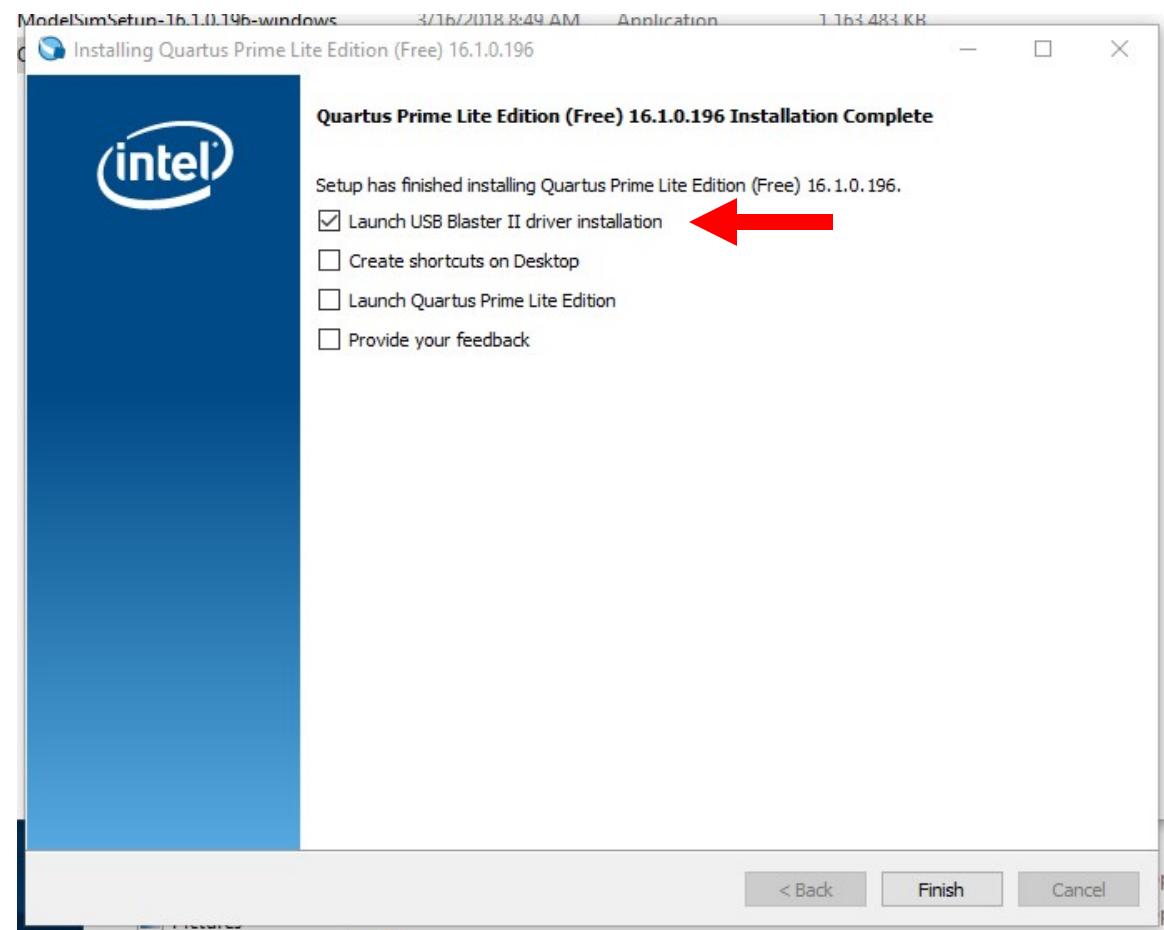
# Install Quartus Prime v16.1

- Installation will take a few minutes



# Install Quartus Prime 16.1

- Install USB Blaster II drivers and finish

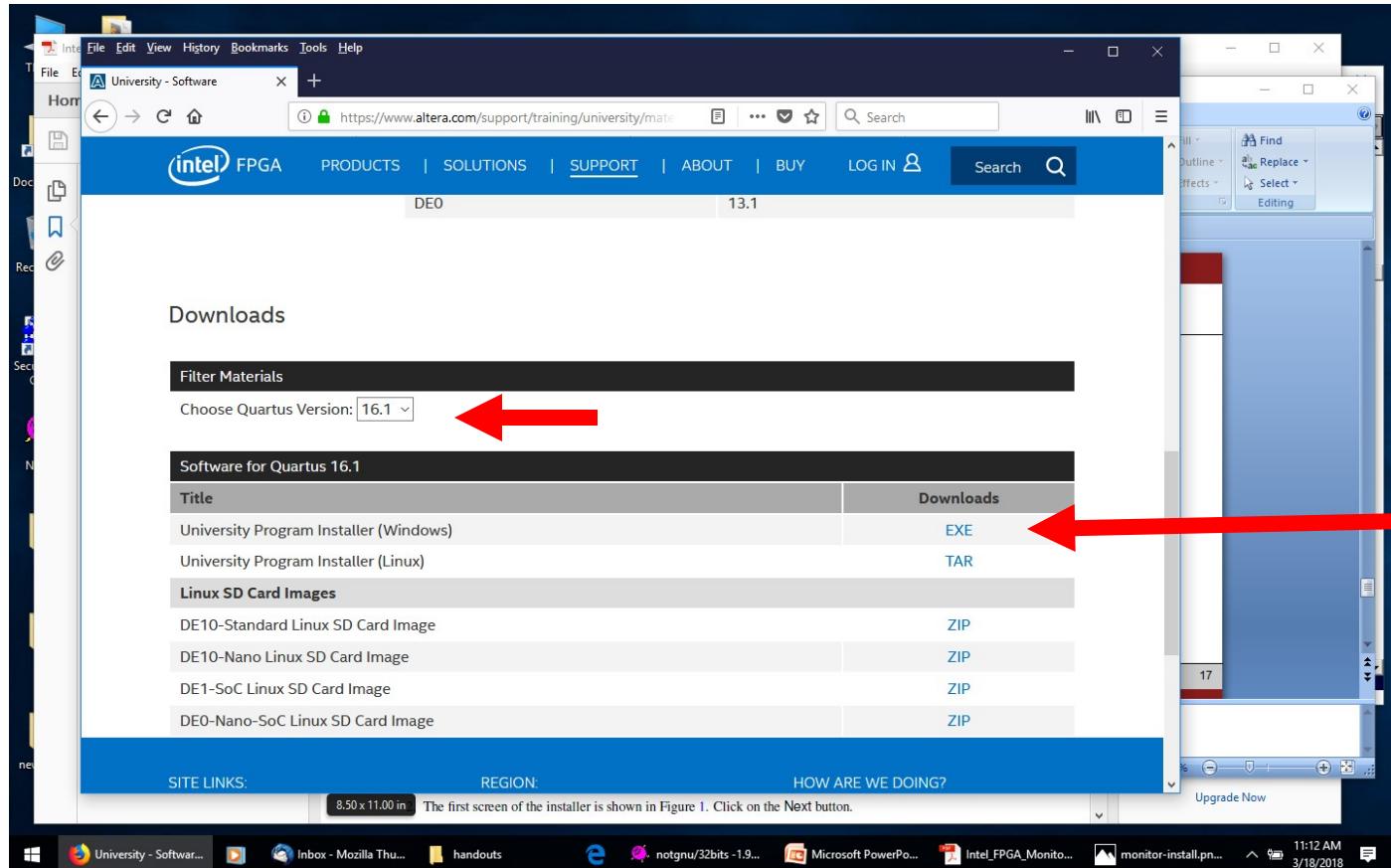


# Intel FPGA Monitor Program Download

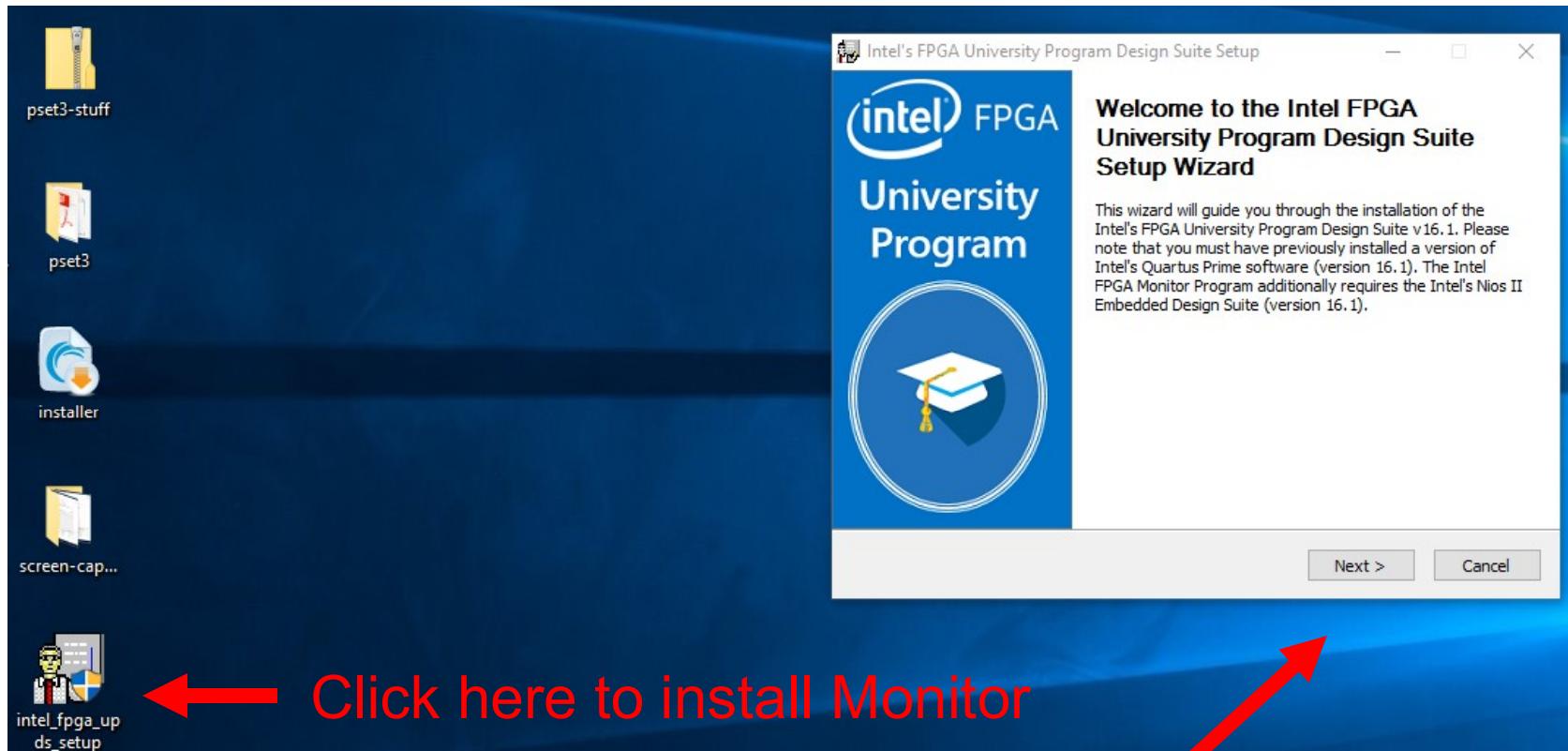
- Monitor program needed to compile and download programs to the ARM processor on the DE1-SOC
- Information about the Monitor Program can be found in [Intel\\_FPGA\\_Monitor\\_Program\\_ARM.pdf](#)
- Installation information located in Chapters 1 and 2 of the Intel FPGA Monitor Program document
- Download Monitor from the following location
  - <https://www.altera.com/support/training/university/materials-software.html>

# Intel Monitor Program Download

- Download version 16.1



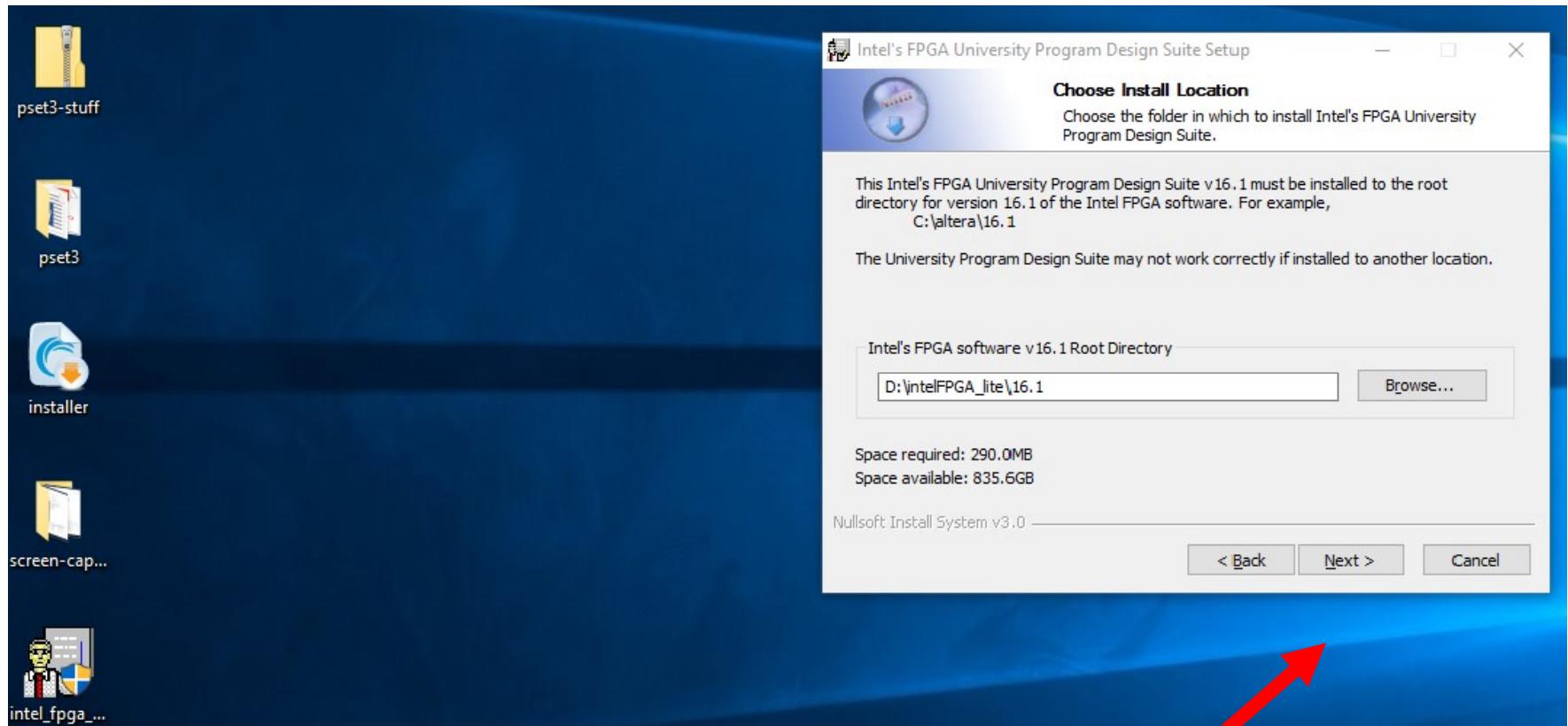
# Monitor Program Install



- Click icon to install

Click Next

# Monitor Program Install

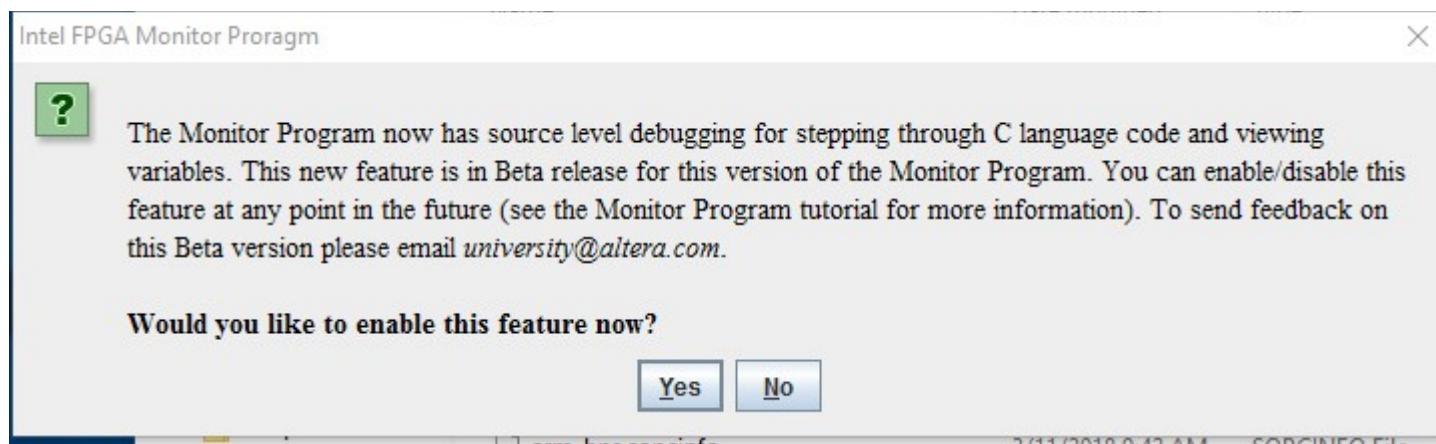
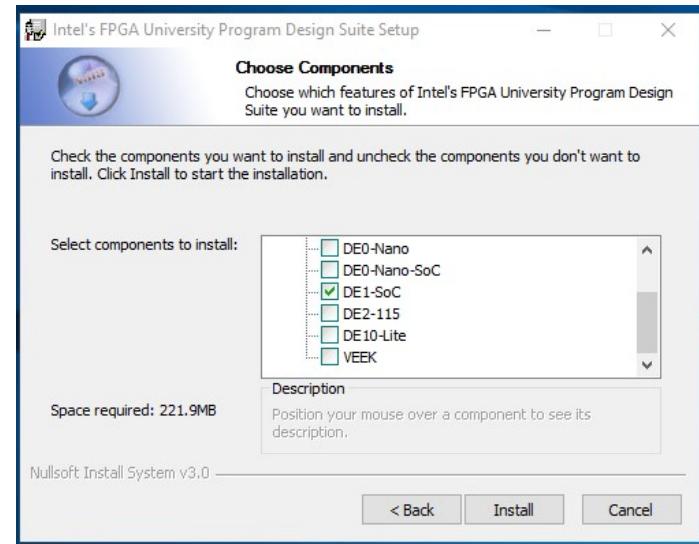


- Select an installation directory

Click Next

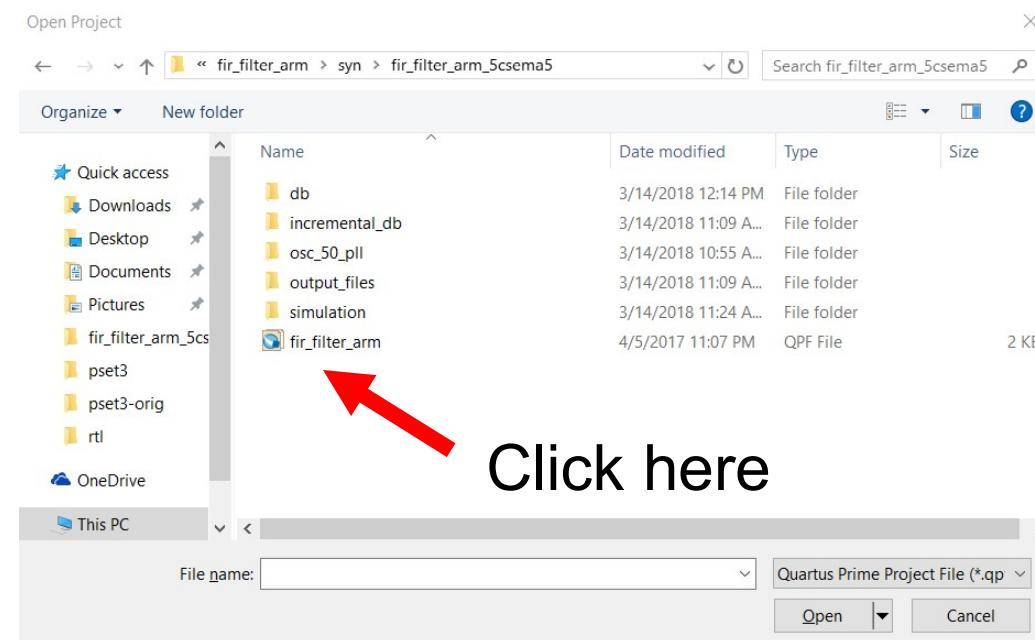
# Intel Monitor Program Download

- Only select components for the DE1-SoC and then select “Next”
- Do not enable the source-level debugger. Select “No”



# Simulating Your FIR filter

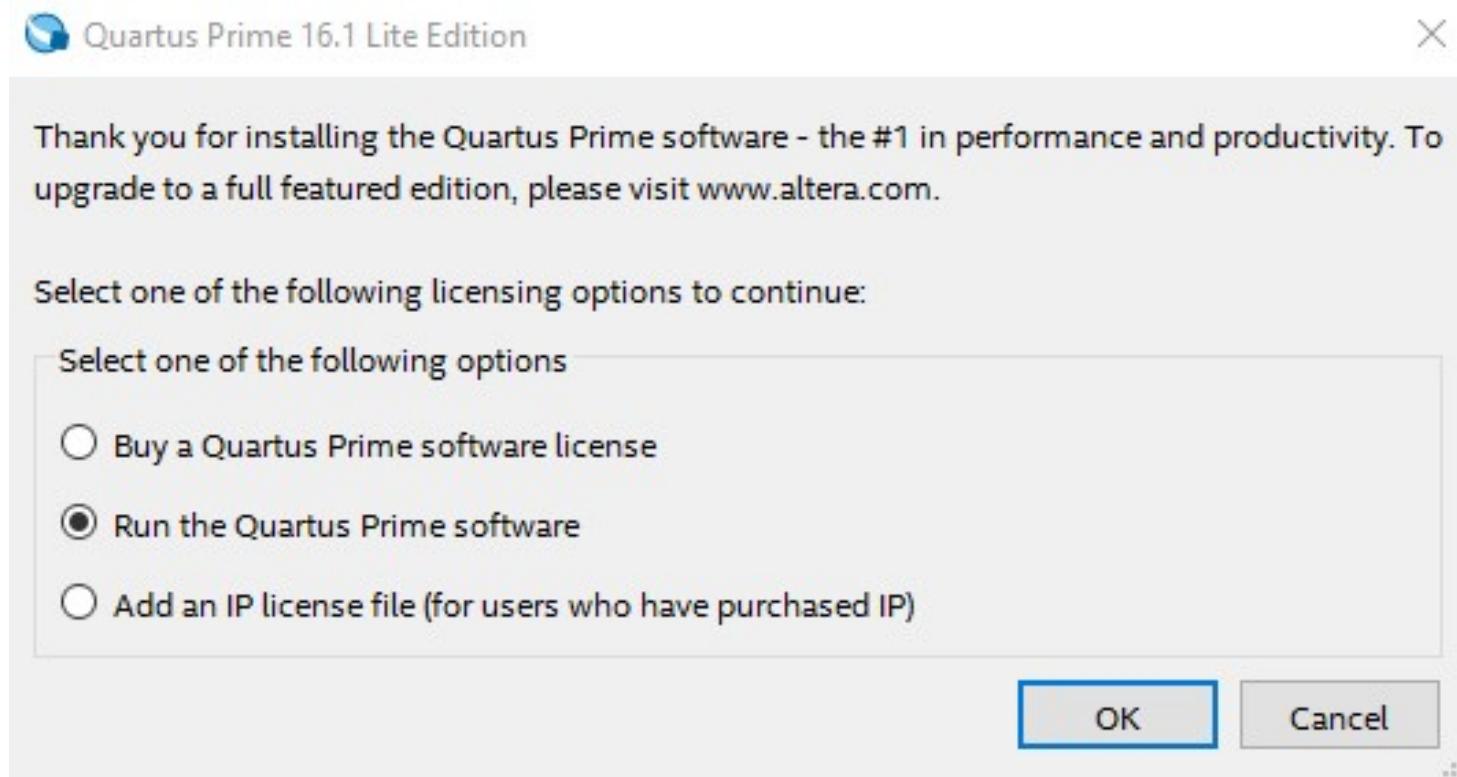
- This section of the slides will follow along with Section 2 of the “Assignment 3” document called “Debugging the Design”.
  - You should read the section as you follow these slides.
- Step 1: Put your fir.v file(s) into the directory fir\_filter\_arm/rtl
- Step 2: Open up Quartus Prime by clicking on fir\_filter\_arm\syn\fir\_filter\_arm\_5csema5\fir\_filter\_arm.qpf



Click here

# Simulating Your FIR filter

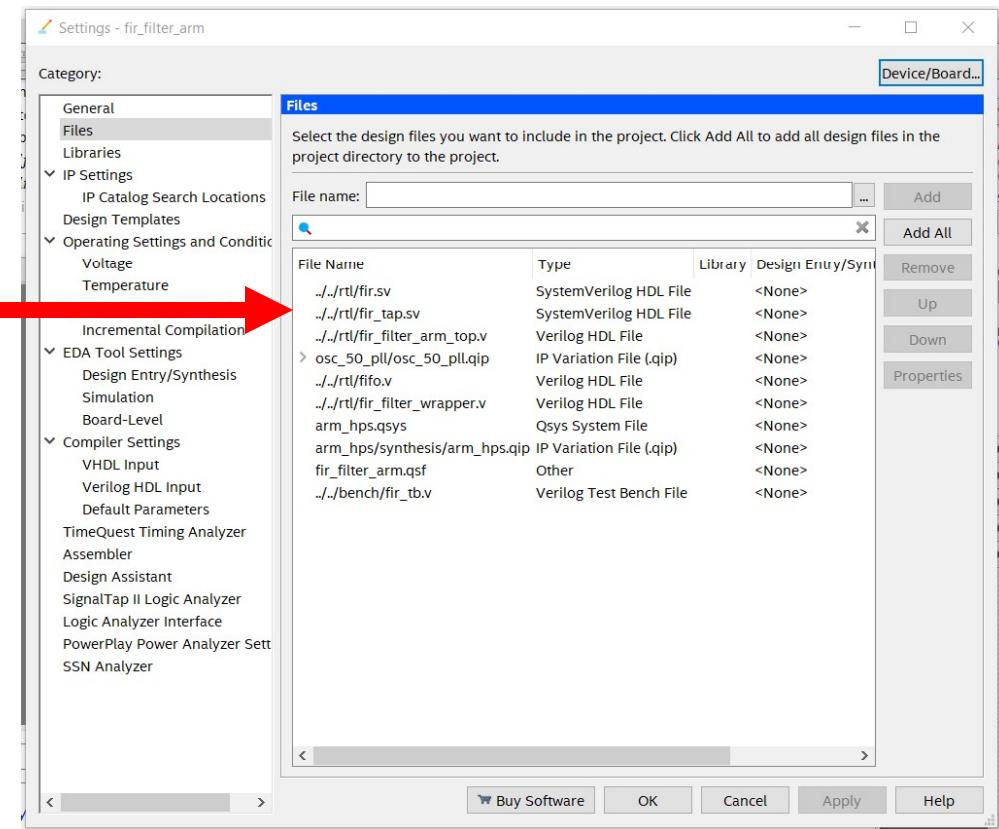
- You may be asked which version of Quartus you would like to run
- Select the middle choice and click OK



# Adding Files to Your Project

- First, add to the project the Verilog files you have written to describe the FIR filter. The module name for the top level of your design should be fir.
- In Quartus Prime, click on the “Project” menu and select the option “Add/Remove Files in Project”.

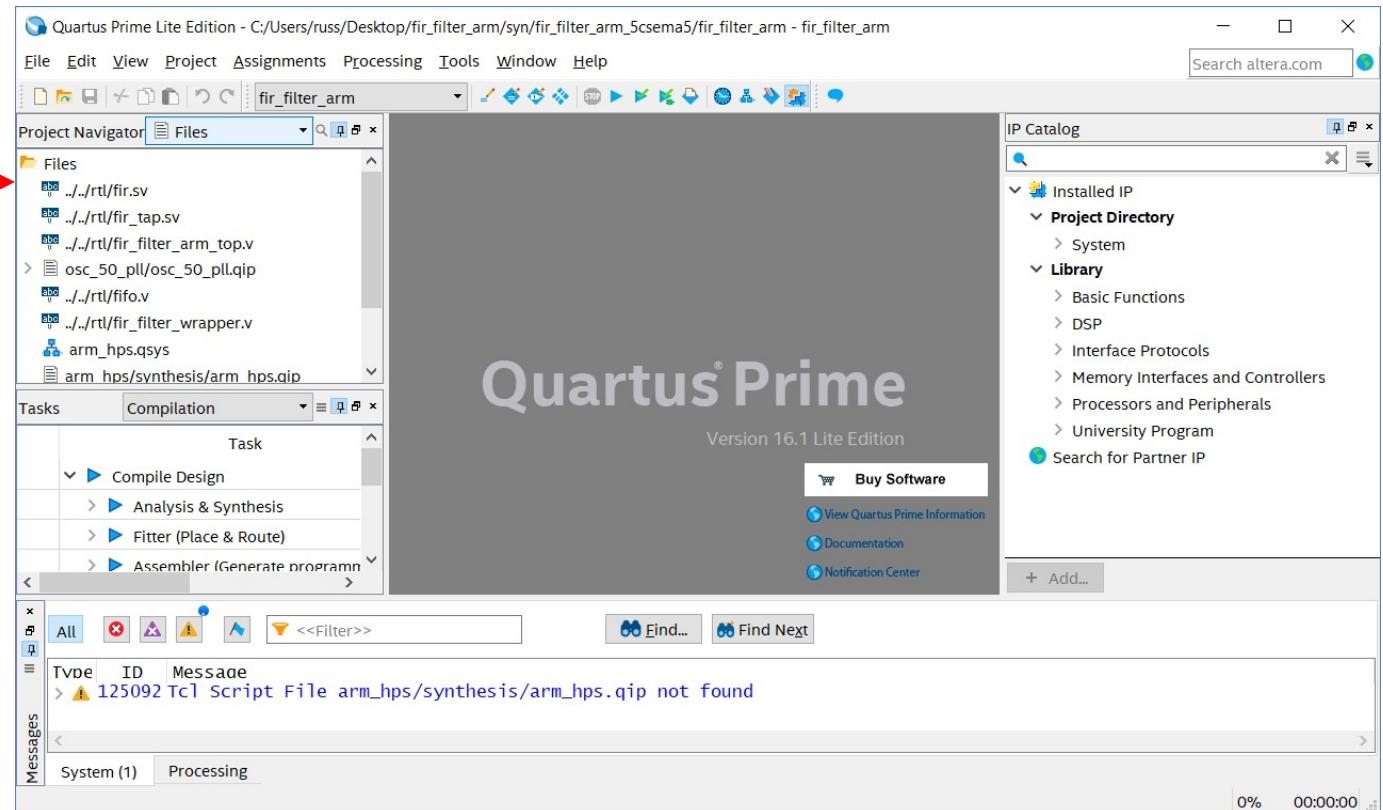
Added files “fir\_tap.sv”  
and “fir.sv”



# Select Top Level of Your Project

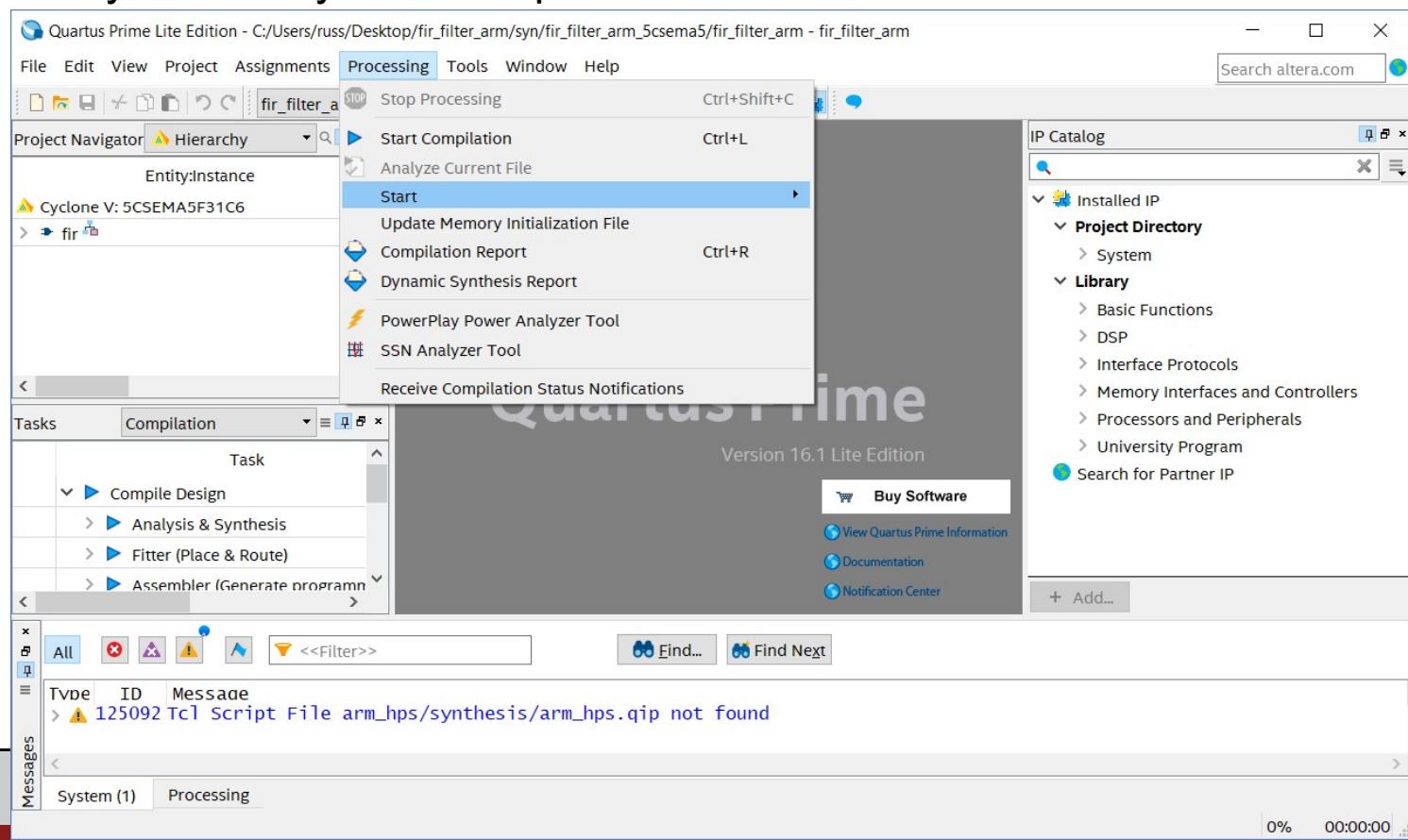
- Ensure that the top-level file of your design is the top-level entity of the Quartus project. To do so, select “Files” from the Project Navigator
- Then right click on the top-level file of your design to select the “Set as Top-Level Entity” option.

Select file 



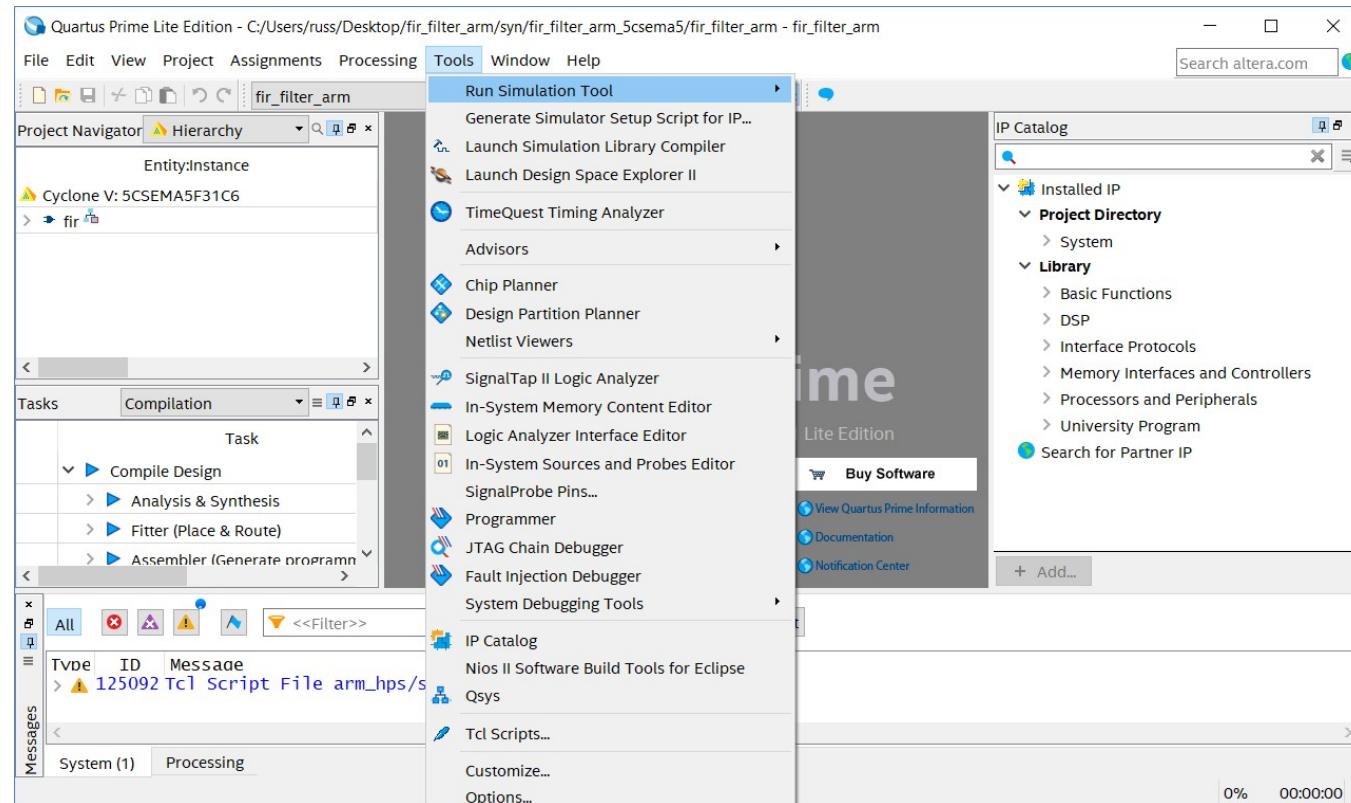
# Synthesize Your Project

- Before invoking the simulator (ModelSim – Intel FPGA Start Edition) the first time, you need to synthesize your design.
- To perform this action, open the submenu “Start” from the Processing menu and select the “Analysis and Synthesis” option.



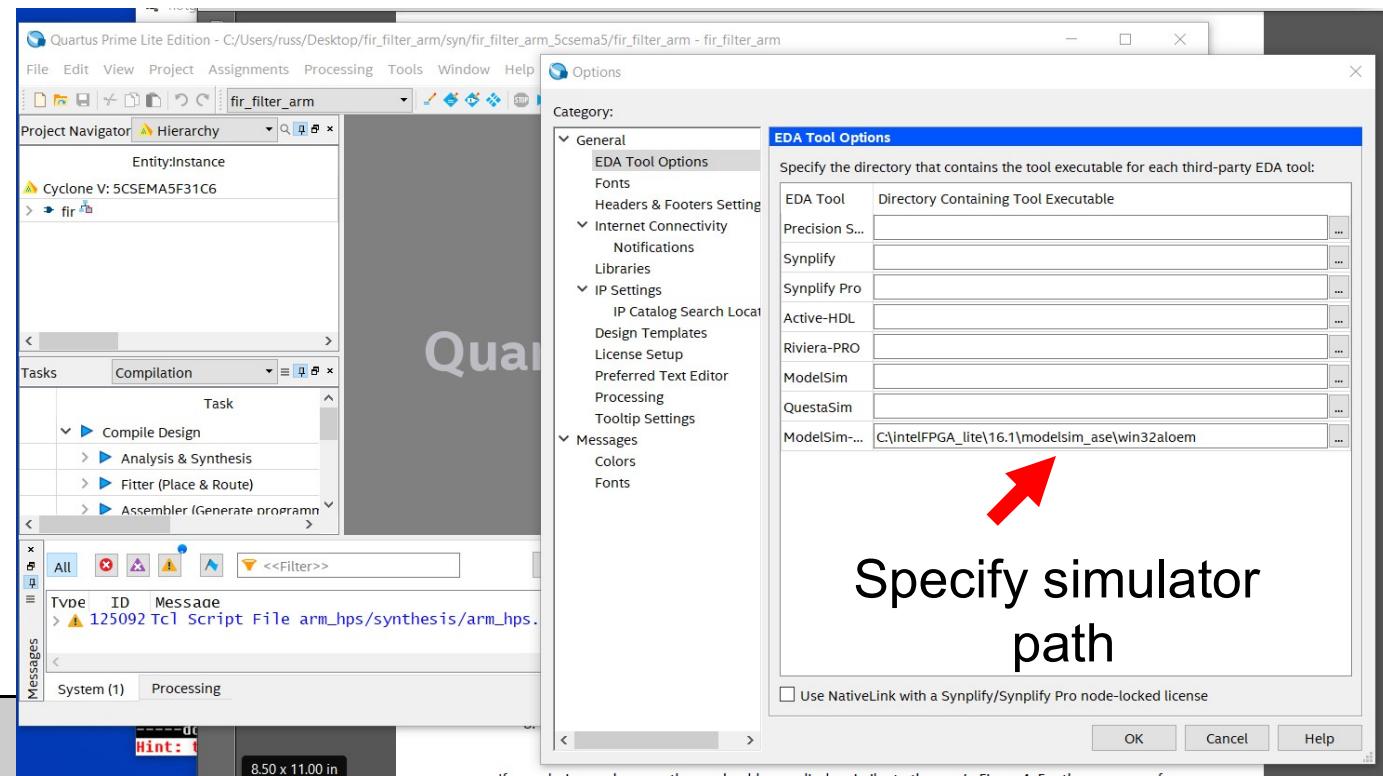
# Run the Modelsim Simulator

- To start the simulator, open the submenu “Run Simulation Tool” from the Tools menu and click on the “RTL Simulation” option
- If you receive an error message about the simulator not found, see the next slide



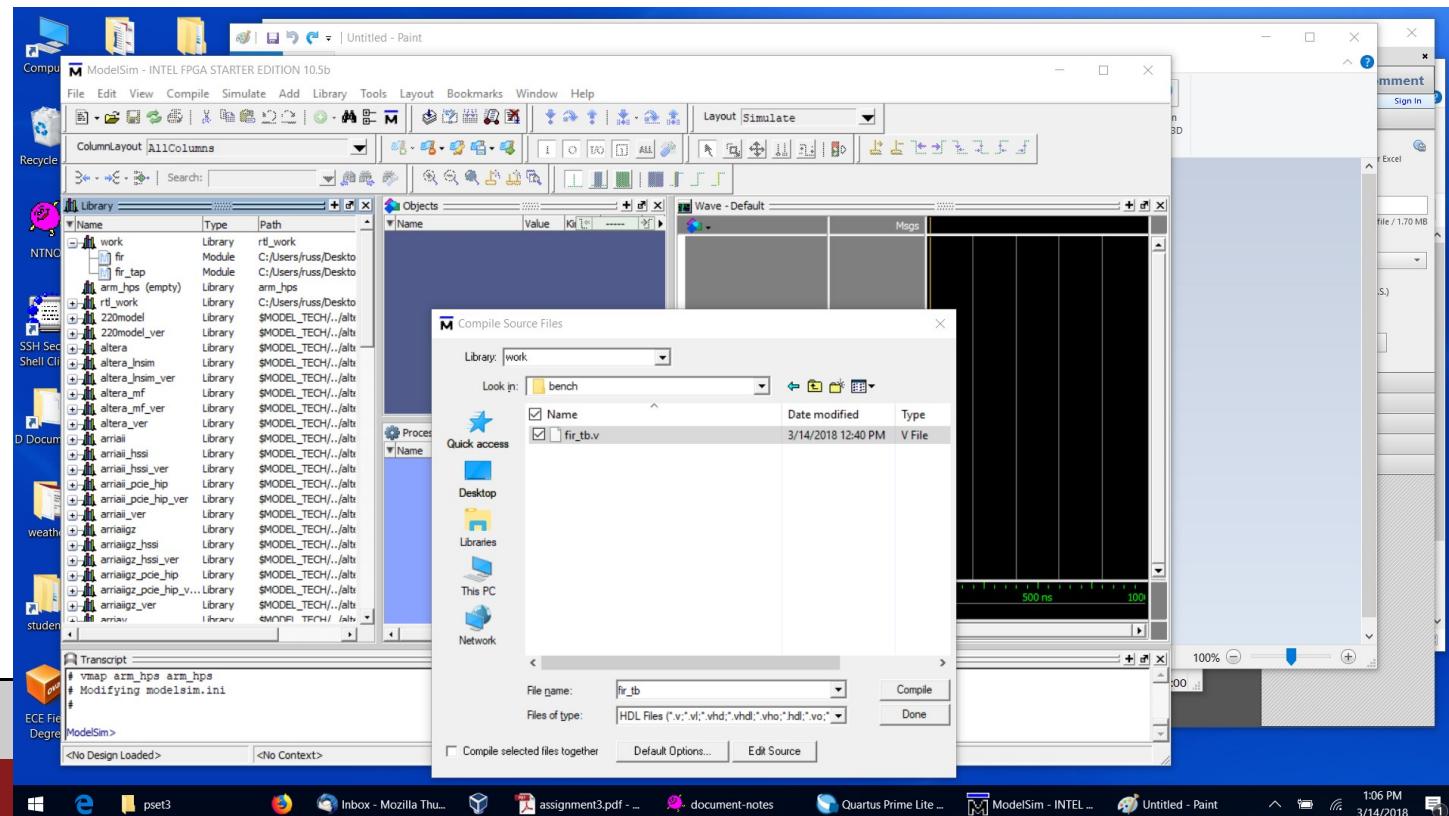
# Verifying the Path to Modelsim Tools

- In some cases, if you attempt to run the simulator you will receive an error message indicating that the simulator is not found or installed
- In this case you will need to specify the directory with the simulator binary
- Check : Tools -> Options -> EDATools
- Include directory: <your install directory>16.1\modelsim\_ase\win32aloem



# Compile the Testbench file

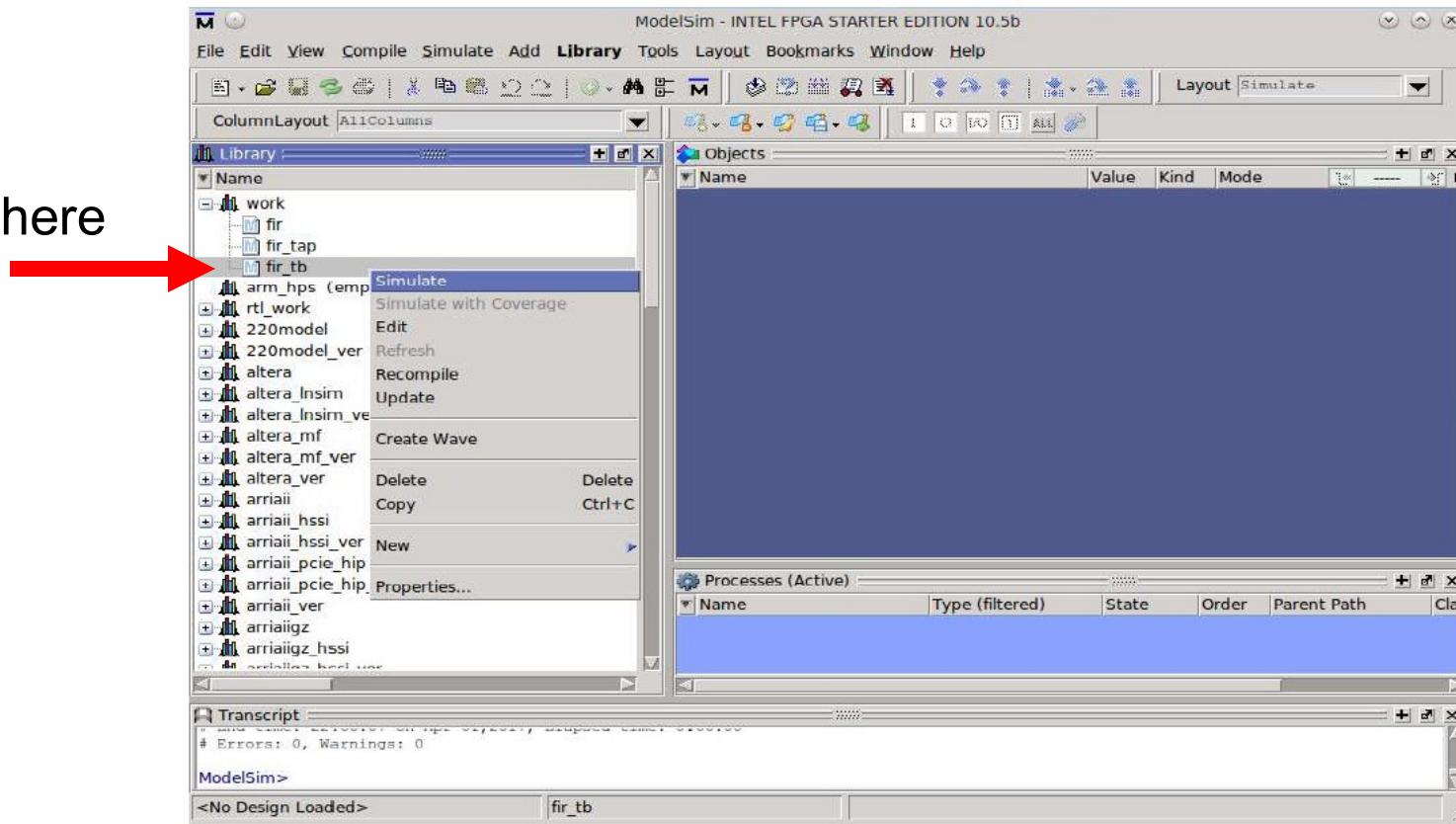
- The working library of the simulator (work) should contain all the modules of your design and the FIR test bench file fir\_tb.v.
- To add the FIR test bench, click on the “Compile” option from the top menu
  - Navigate to the location of the FIR test bench (/fir\_filter\_arm/bench/fir\_tb.v.)
  - Important: Edit fir\_tb.v to uncomment the fir module**
  - Select the file and click on the “Compile” button to compile it and then close the window.



# Start Simulation

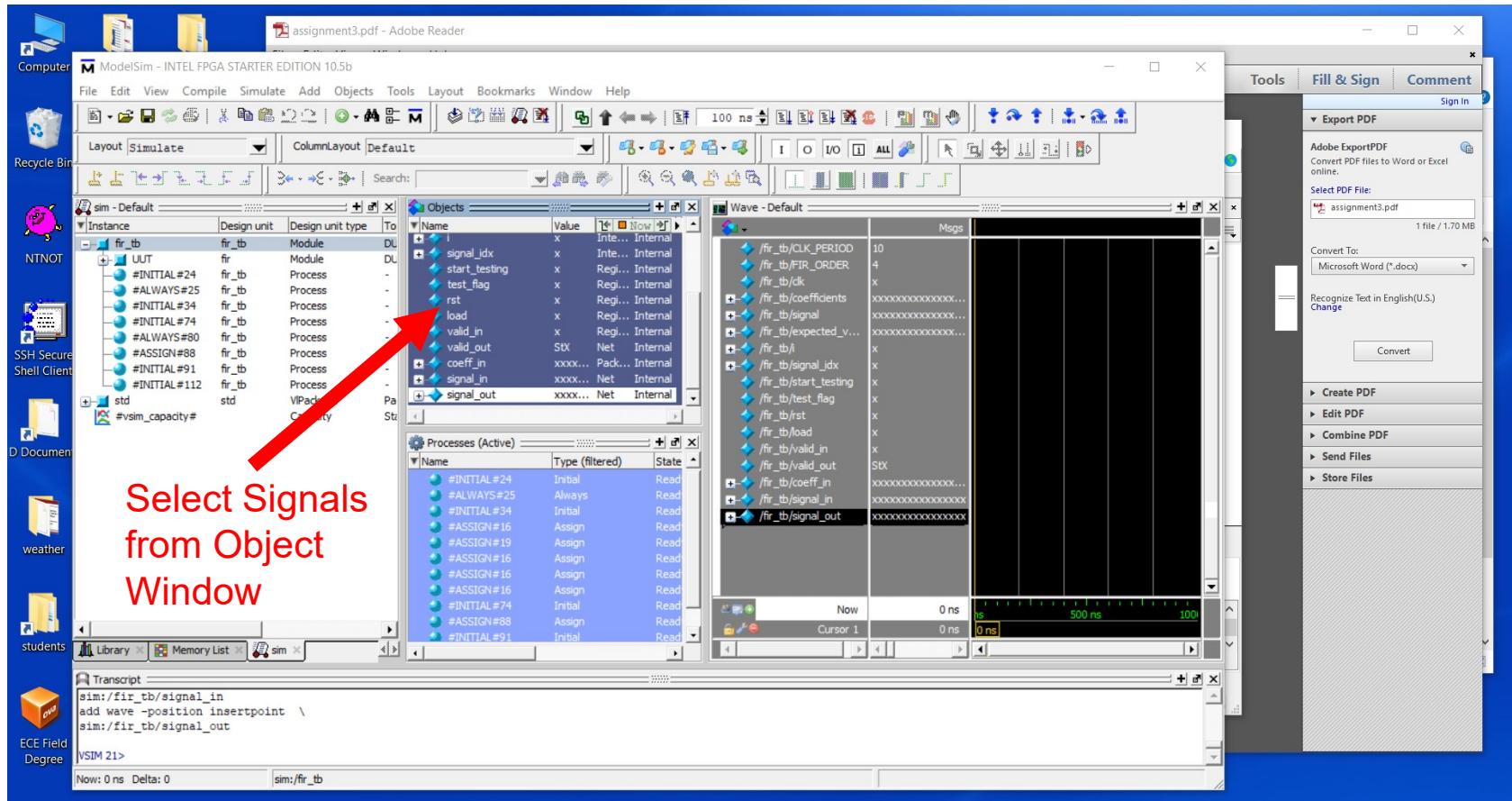
- Assuming that you have successfully compiled the implementation files and the FIR test bench you can start the simulation.
- To do so, right click on the fir\_tb.v file and select the “Simulate” option

Right click here



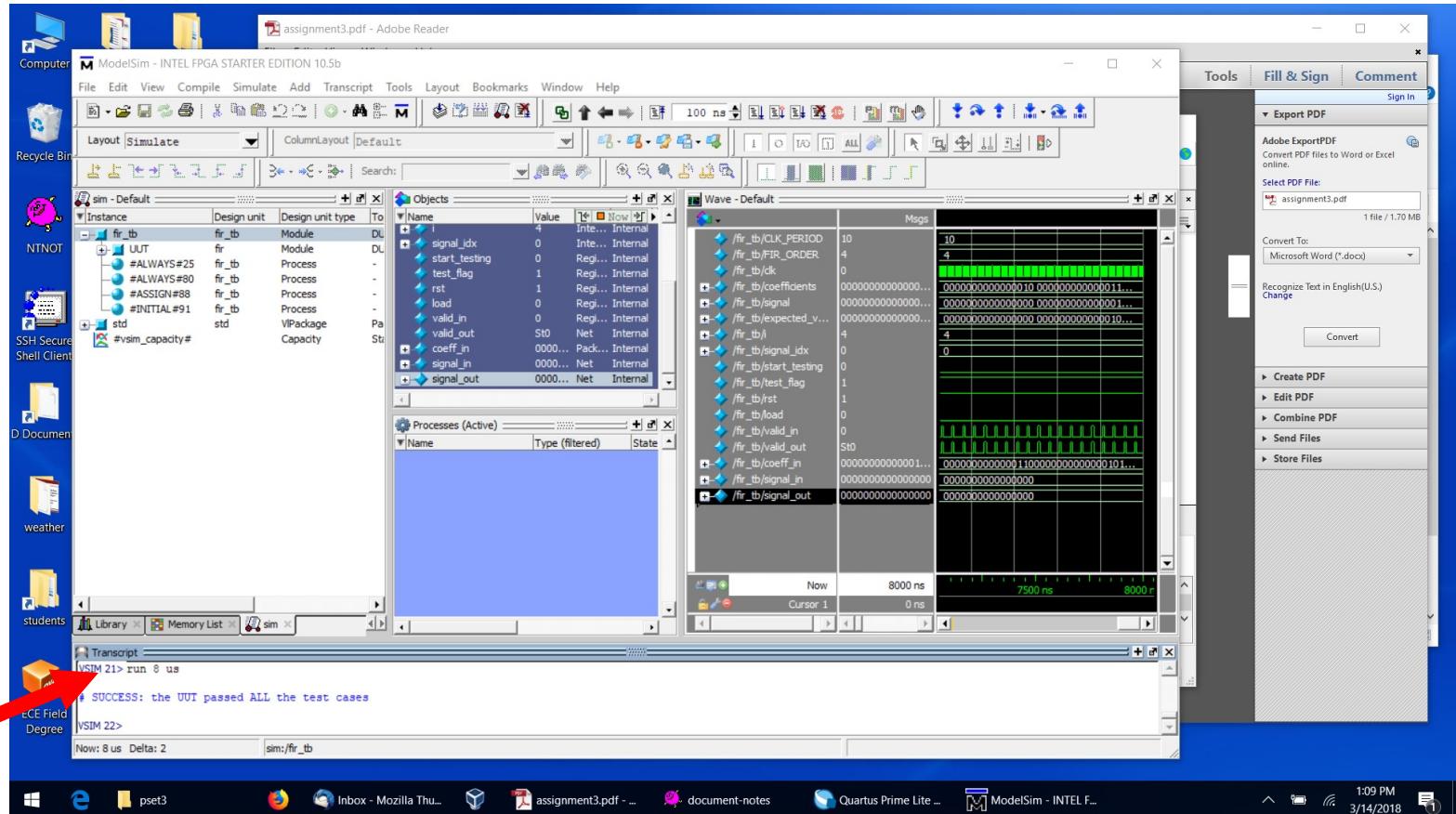
# Select Waveforms

- To use the Waveform viewer first select all the signals you want to examine from the Object window and then right click and choose the “Add Wave” option.



# Perform Simulation and Observe Waveforms

- Run the simulation by typing the following command into the Transcript pane of the simulator: run 8 us



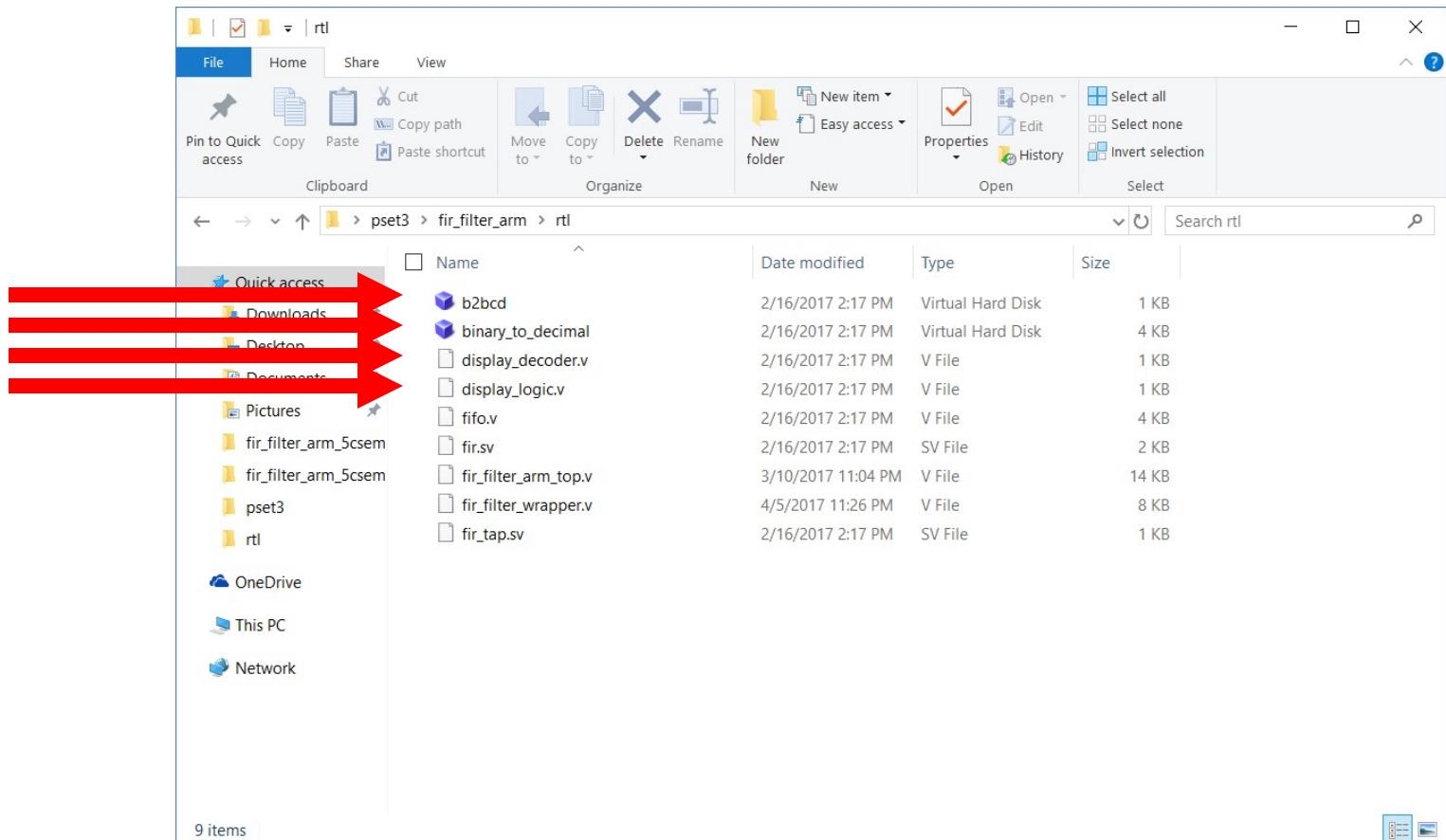
Run  
simulation

# Running Your Design on the DE1-SoC

- Once you have verified that your design works correctly in simulation, it can be compiled and run on the DE1-SoC board.
- A series of additional steps are needed to perform this action. The next few slides follow Section 3: Testing the Circuit and Section 4: Building the Project in the assignment3.pdf document.
- Please read over these sections before you perform the actions on the next few slides
- As noted in Section 3, before you can perform the on-board test, you need to write several more Verilog modules for BIN2BCD and DISPLAY LOGIC
  - You may want to simulate these designs before testing them on the board.

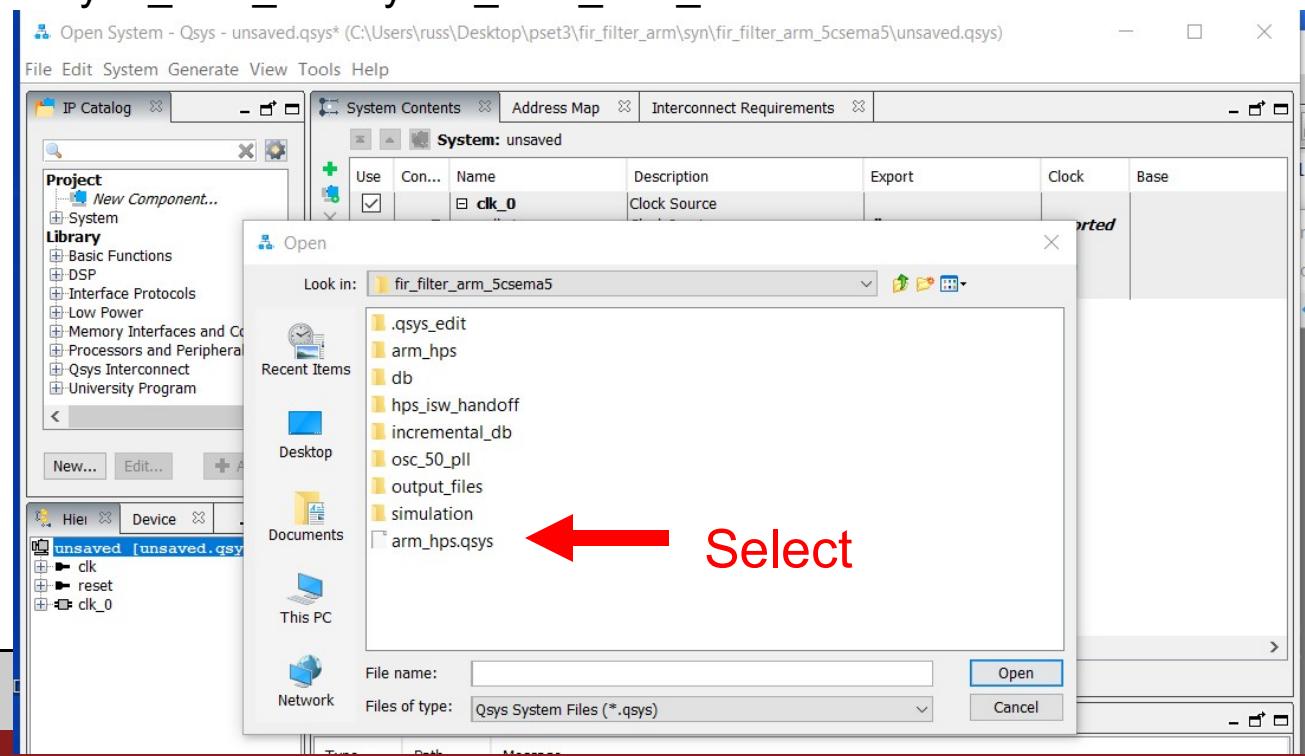
# Adding Files to Your Project

- Make sure that your new files are in the rtl directory of fir\_filter\_arm. Make sure to add the files to your Quartus project (as shown on slide 23)



# Regenerate Qsys System

- Your DE1-SoC test will include both your FIR filter implemented in the FPGA and a program implemented by the ARM processor.
  - To allow for communication, you need to create an interface
  - The Qsys system in Quartus will help you create this interface
- in Quartus Prime select “QSys” from the Tools menu and wait for QSys to launch. A window will pop up prompting you to select a .qsys file to open. Select the arm\_hps.qsys which is located in the directory fir\_filter\_arm/syn/fir\_filter\_arm\_5csema5/.

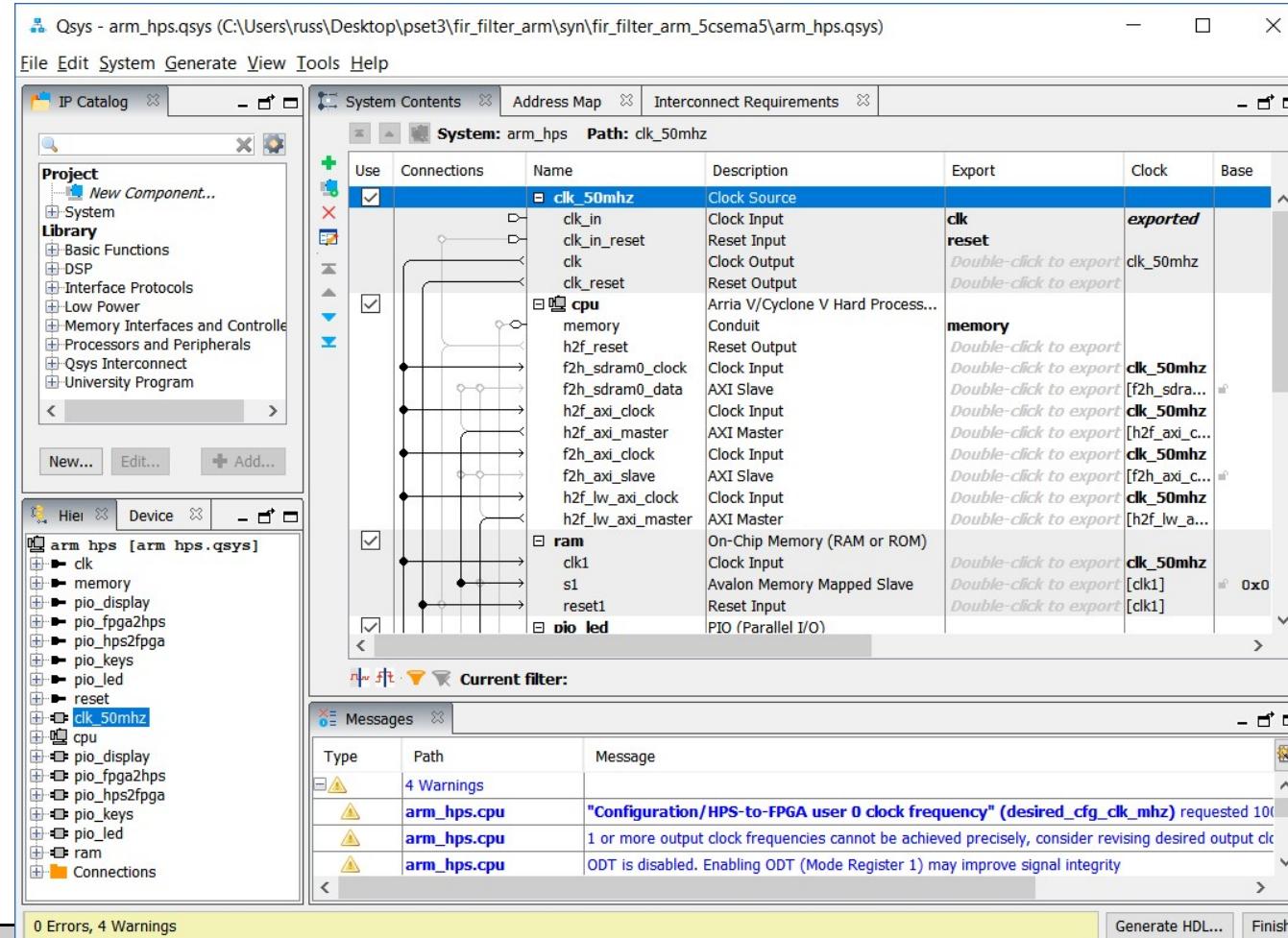


# Regenerate Qsys System

- Click “Generate HDL” at the bottom of the window to open the Generation window. In this window you can specify synthesis and simulation parameters as well as the path of the output directory.
- Keep the default settings and click on the “Generate HDL” button at the bottom. A window will pop up to inform you that your QSys project has been saved successfully.
- Select “Close” to close the window and wait for the system to generate the files needed.
- Once finished, click again on “Close” to close the generation window and press the “Finish” button at the bottom to close the QSys project.
- A window will pop up to inform you that you can add the generated .qip file to your project.
- Ignore the message by clicking on the “Ok” button since the .qip file has already been added to your project.

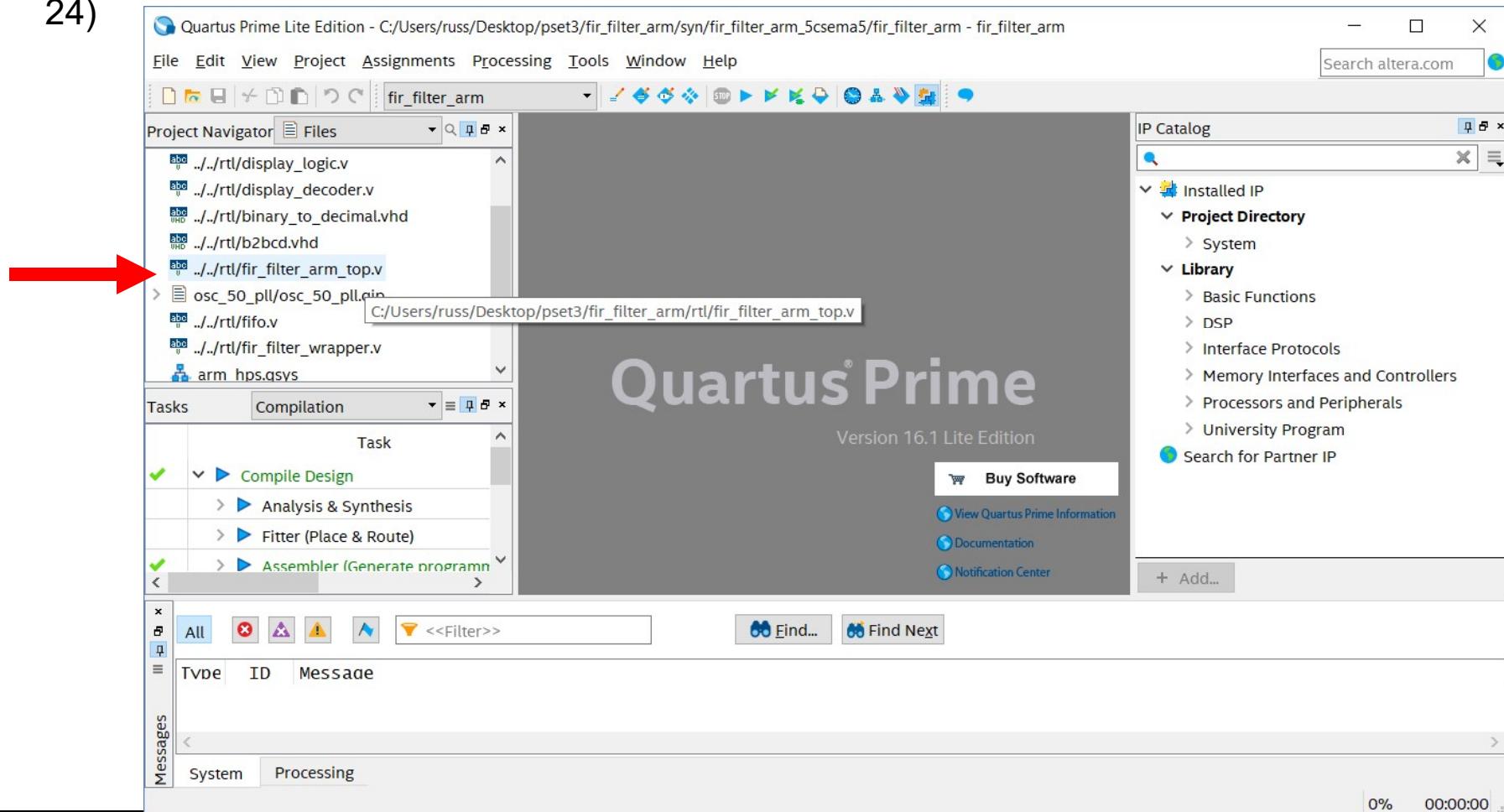
# Regenerate Qsys System

- Screenshot of Qsys window with “Generate HDL” button



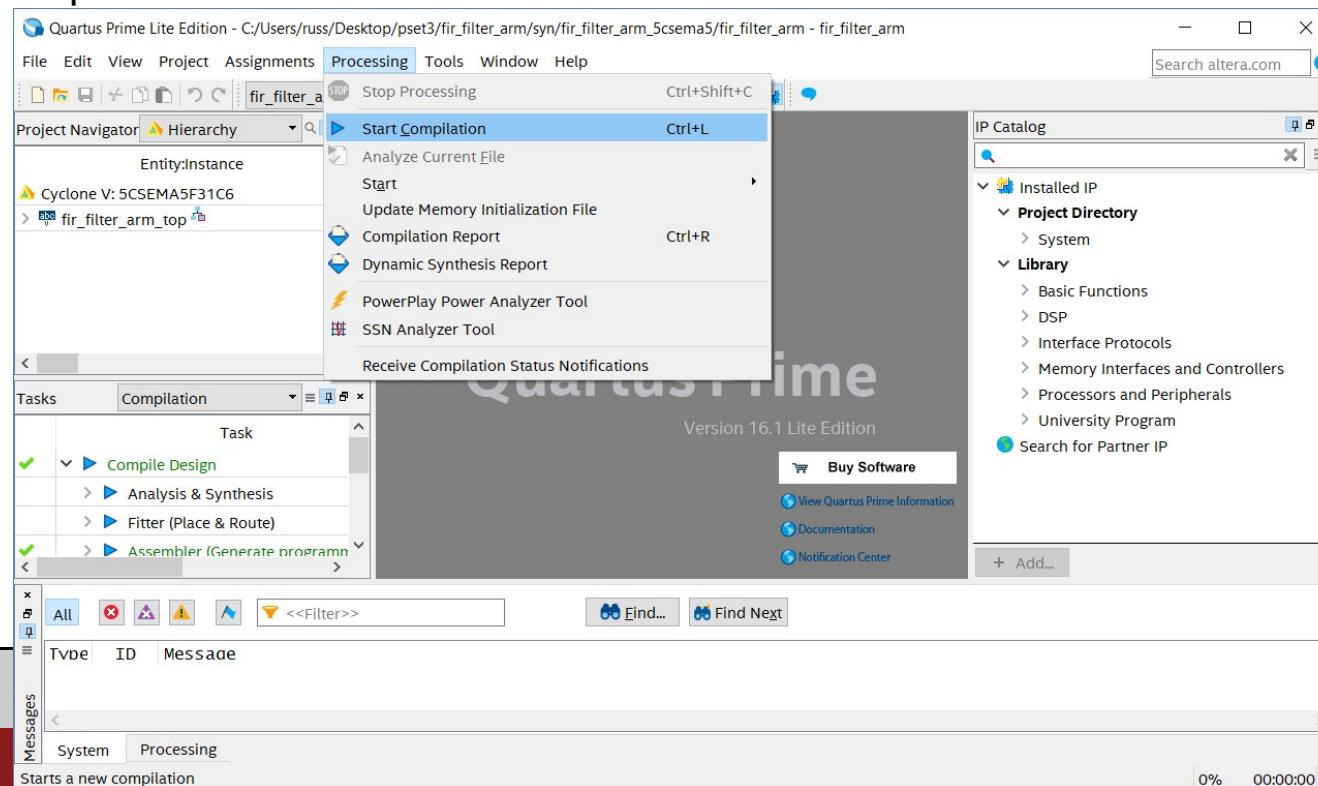
# Set Top Level Design File

- Make sure that now the fir\_filter\_arm\_top.v is the top-level entity of the project. (see slide 24)



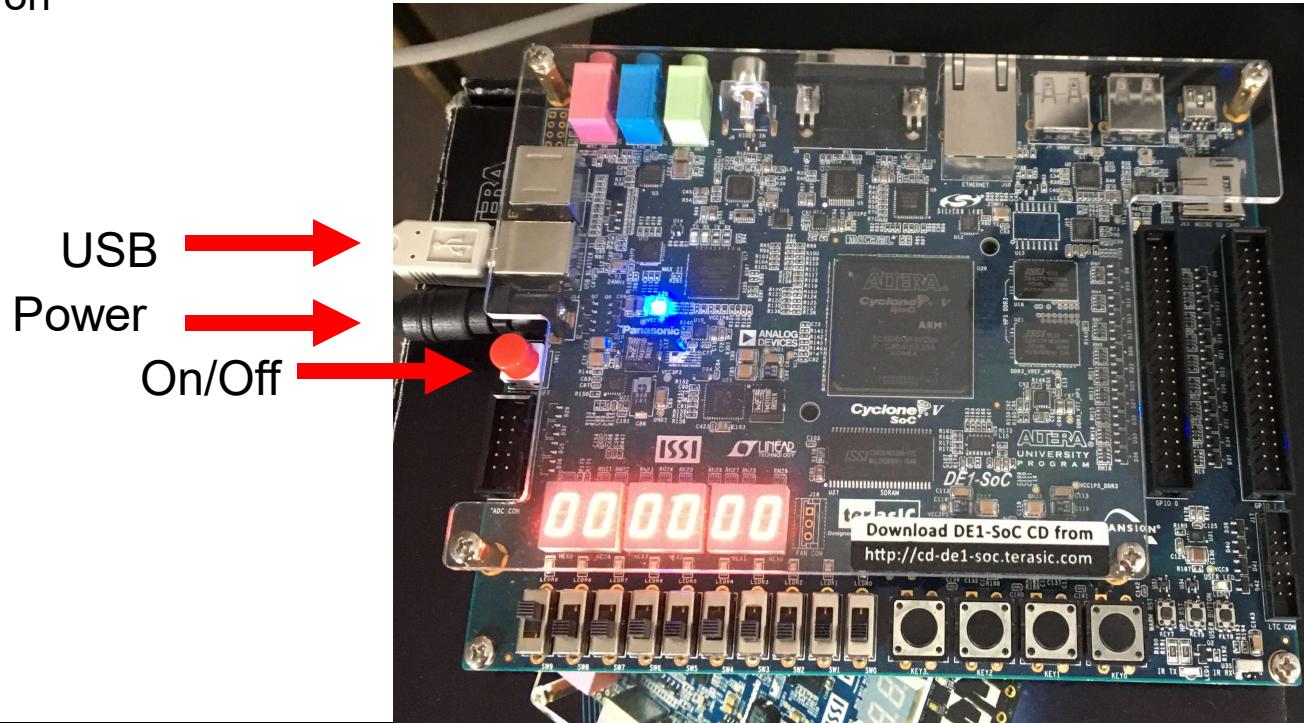
# Compile Design and Generate File for FPGA

- The final step in project building is to compile the design to generate the .sof bitstream file that will program functionality into the FPGA.
- Select “Start Compilation” from the Processing menu.
- Assuming no errors in the RTL code, compilation will finish and you will be able to program the FPGA with your design. It is safe to ignore the post compilation warnings.
- If error messages are shown during compilation, fix the errors in the Verilog code and restart the compilation.



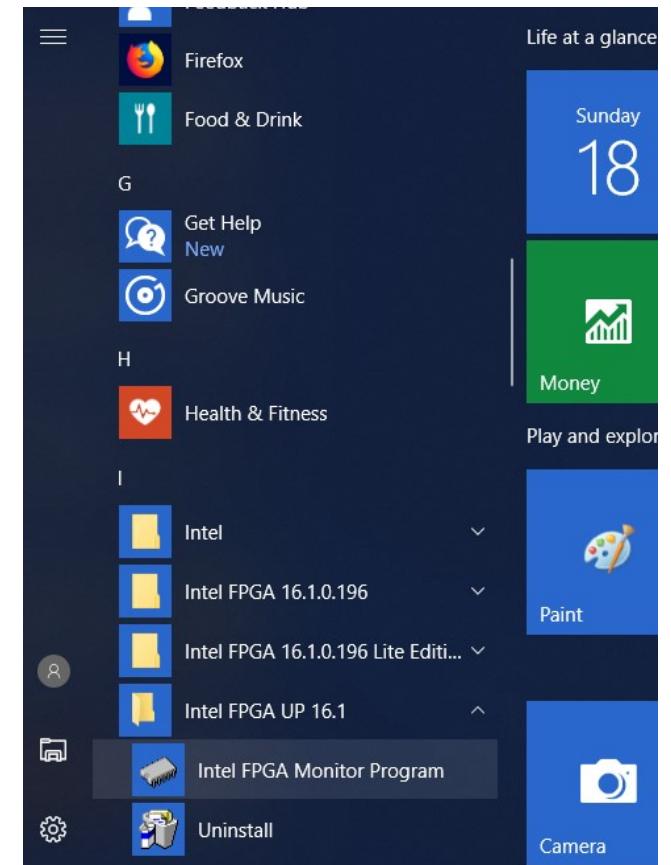
# Running the FIR Design on the DE1-SoC

- At this point your FIR design has compiled without errors and you are ready to test it on the DE1-SoC
- The following slides follow the discussion in Section 5: Running the Test Program in assignment3.pdf
- You should have cables attached to board as shown below. Pressing the red button turns the board on



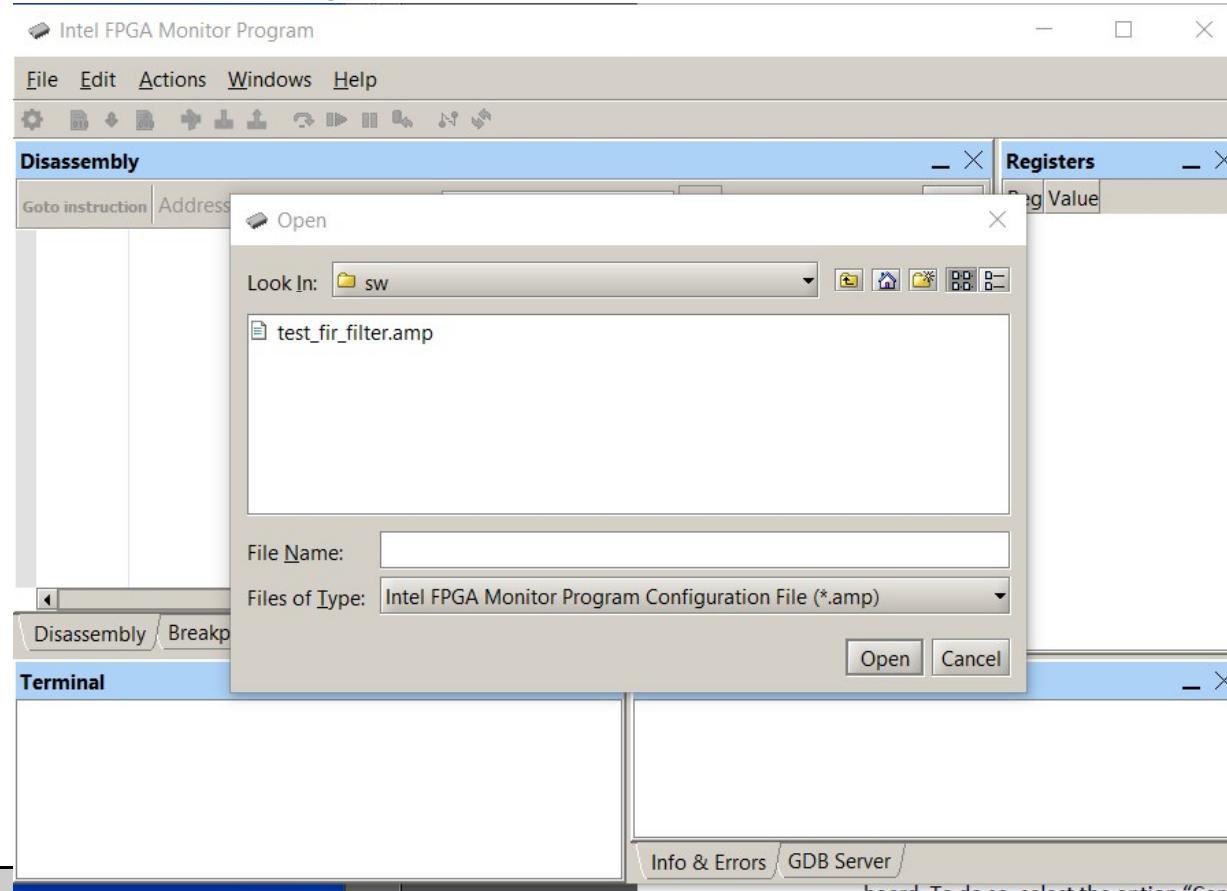
# Compile and Load C and Load FPGA Programs

- To compile, load and run the test program in the `test_fir_filter.c` source file, use the Altera Monitor Program.
- The Monitor Program is a software tool that can compile/assemble an ARM/NIOS II software application.
- Start the program by selecting it from the Windows Applications menu



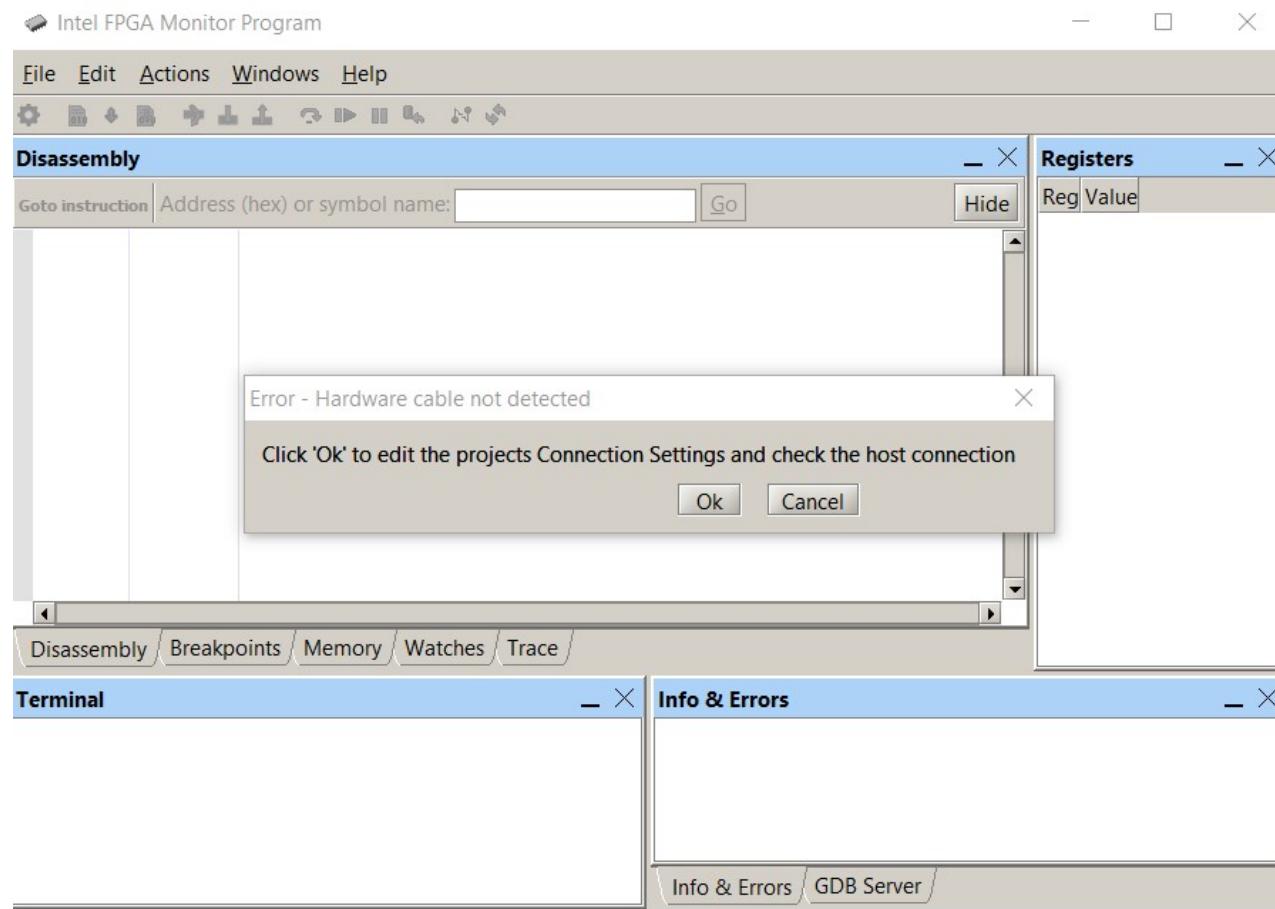
# Compile and Load C and Load FPGA Programs

- On the home screen, select “Open Project” from the File menu and locate the Monitor Program project file test\_fir\_filter.amp.
- You can find this file in the following path: /fir\_filter\_arm/sw/.



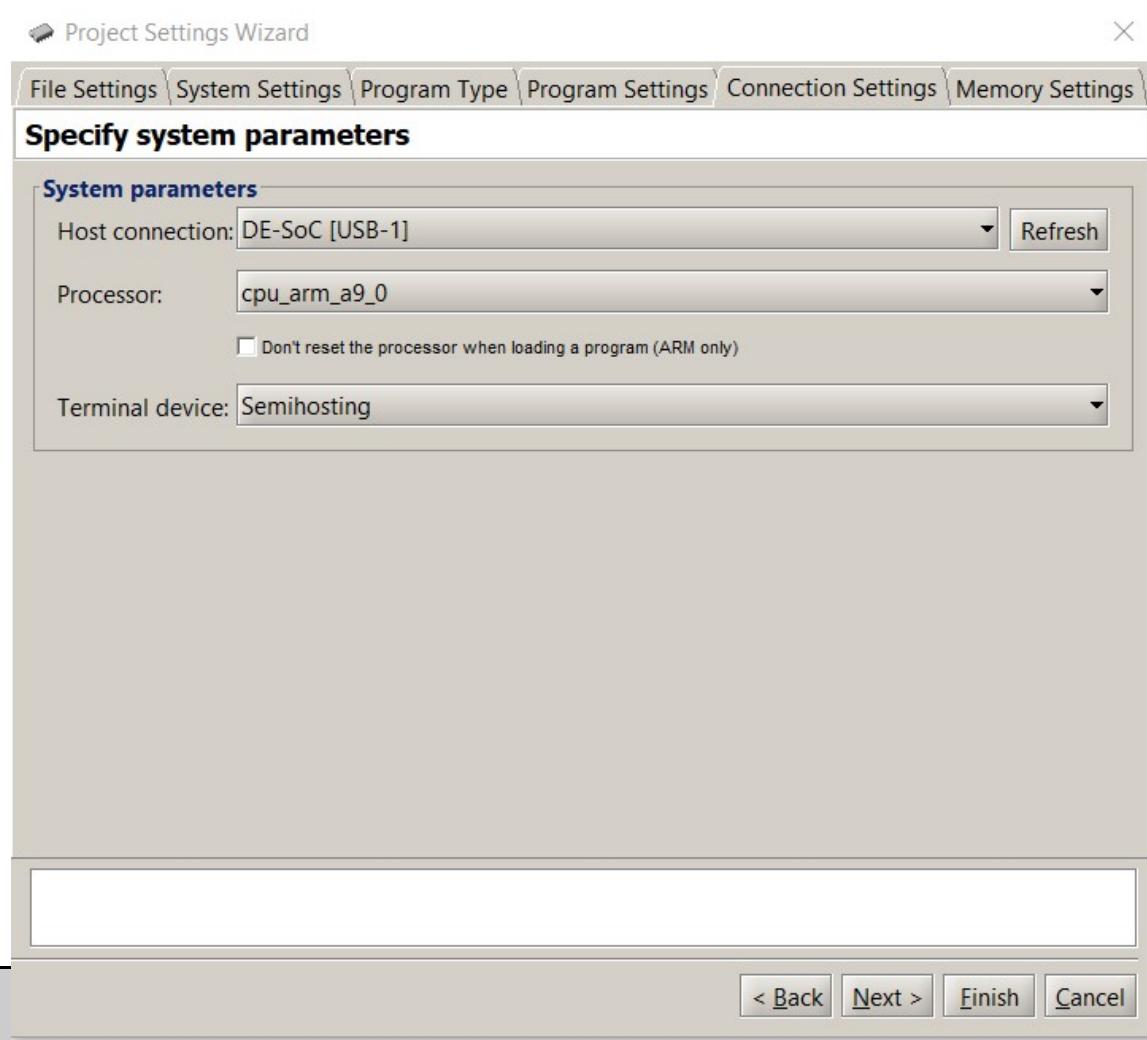
# Compile and Load C and Load FPGA Programs

- To verify the board is connected properly, select OK



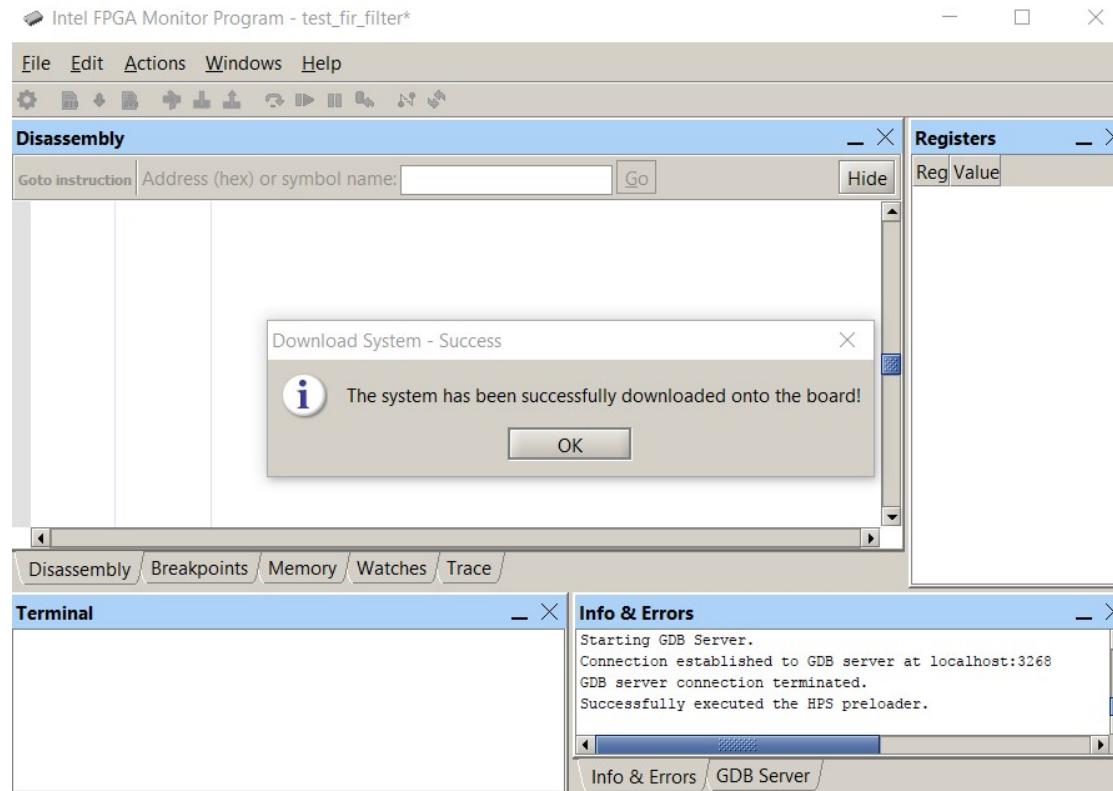
# Compile and Load C and Load FPGA Programs

- Select “Finish” to prepare for downloading



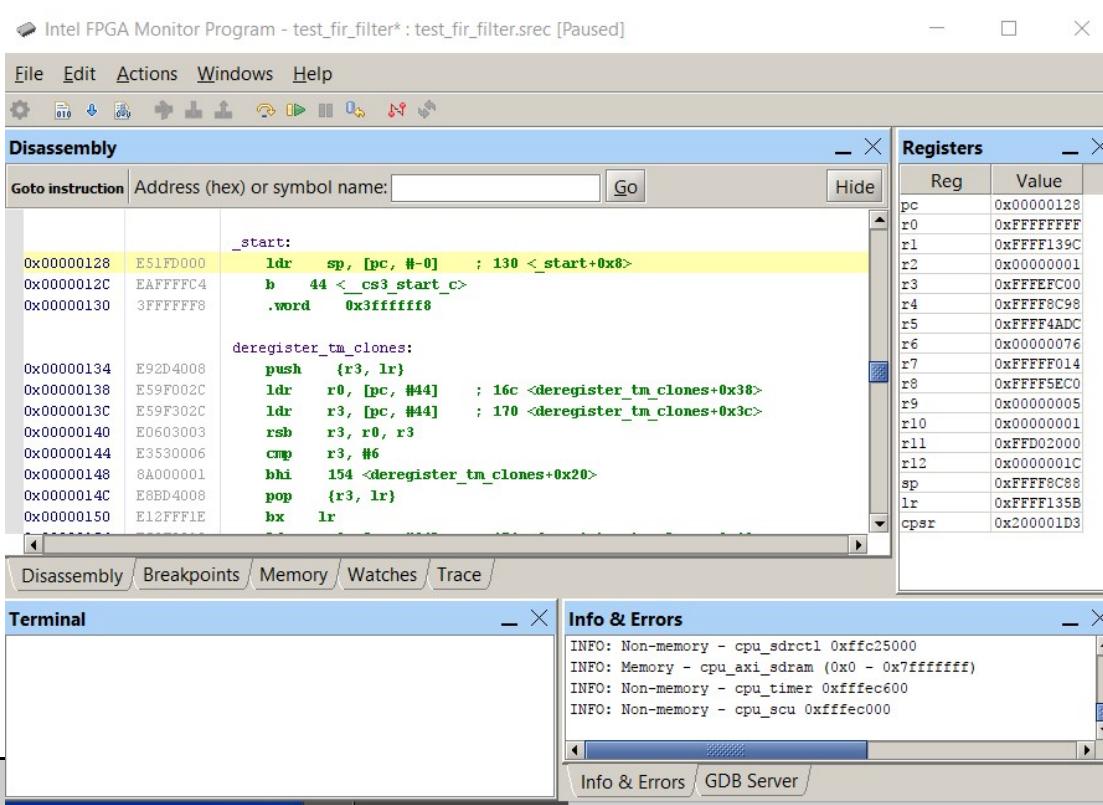
# Compile and Load C and Load FPGA Programs

- A window will pop up asking you if you want to download the system associated (fir\_filter\_arm.sof) with this project onto the board
- Click the “Yes” button once the board is powered up and connected to your computer. Once the FPGA is successfully programmed, the message show below will appear



# Compile and Load C and Load FPGA Programs

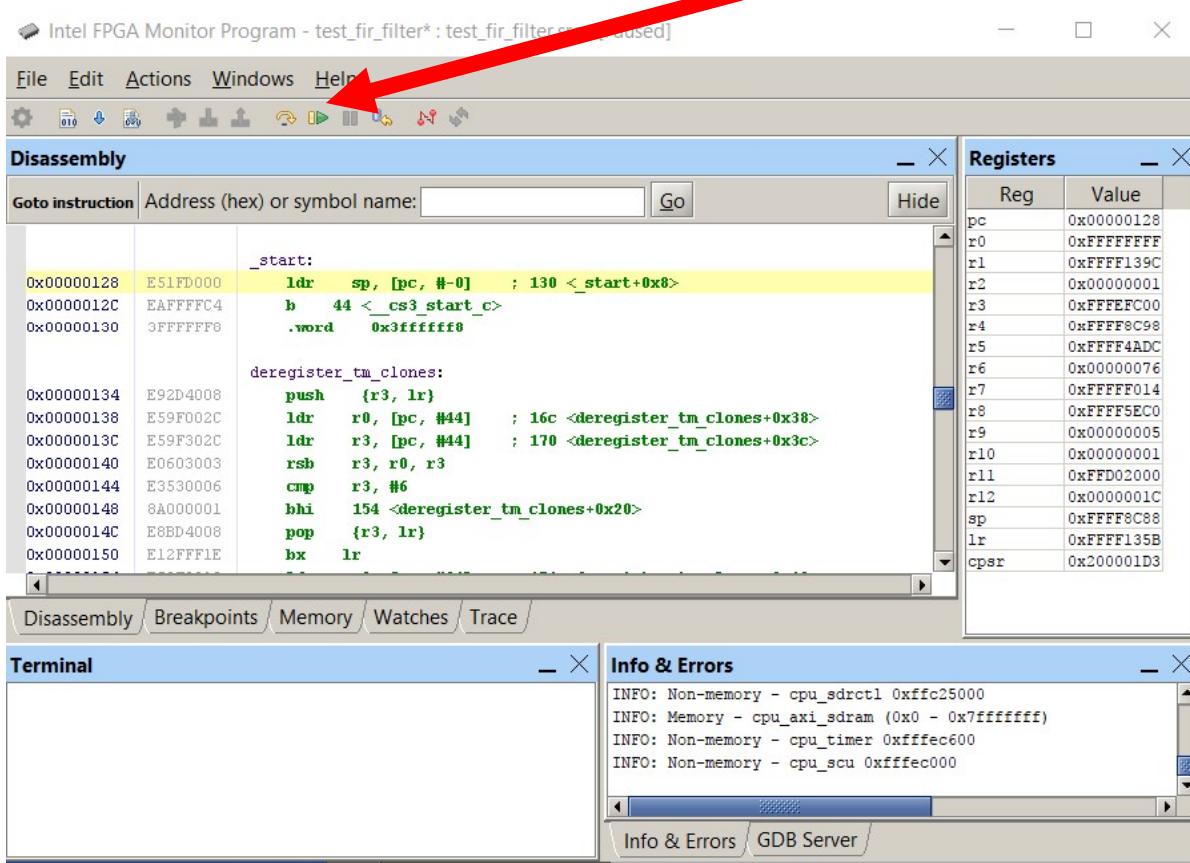
- Compile the testing program (test\_fir\_filter.c) and then load the generated SREC file onto the board. To do so, select the option “Compile & Load” from the Actions menu.
- After successfully loading the program, the processor will halt at the first instruction in the testing program. At this point, you should see a display similar to the one below where the first instruction is highlighted with yellow shading. A value of 000000 should be seen in the DE1 LEDs



# Run C and FPGA Programs

- Run the testing program by selecting the option “Continue” from the Actions menu or by clicking on the green Play button on the toolbar.

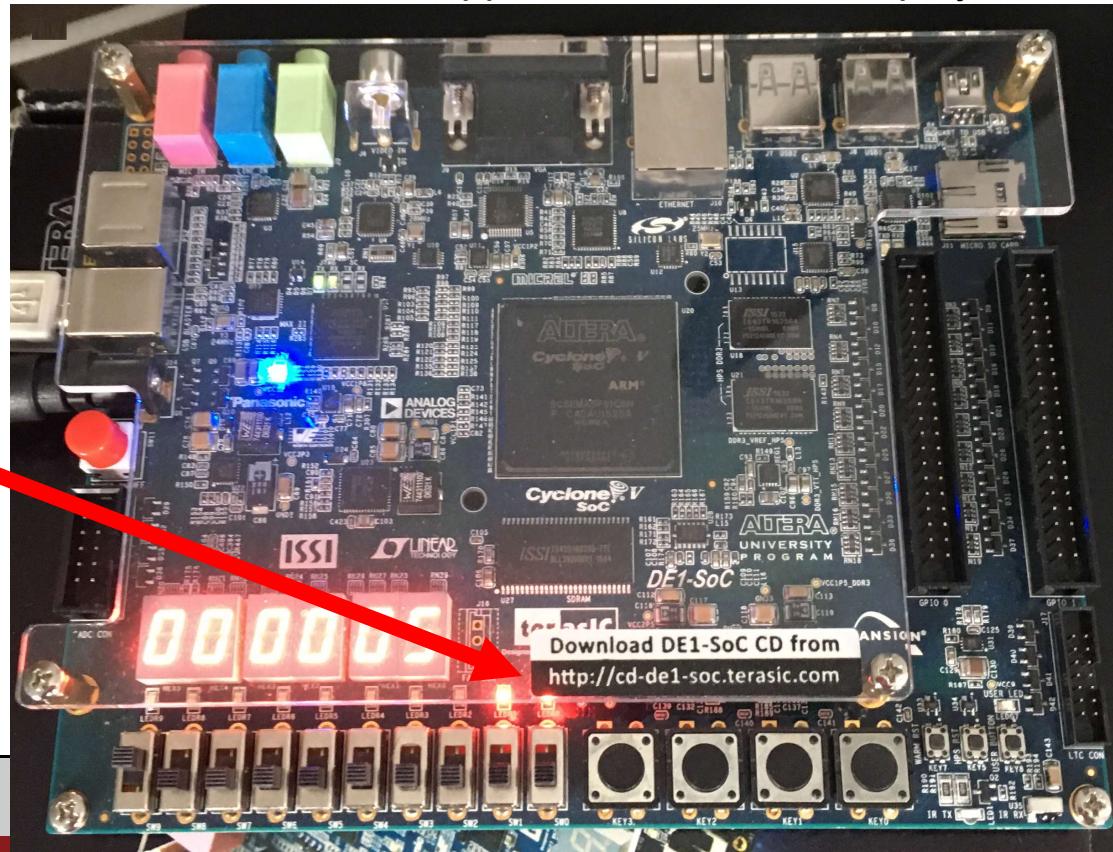
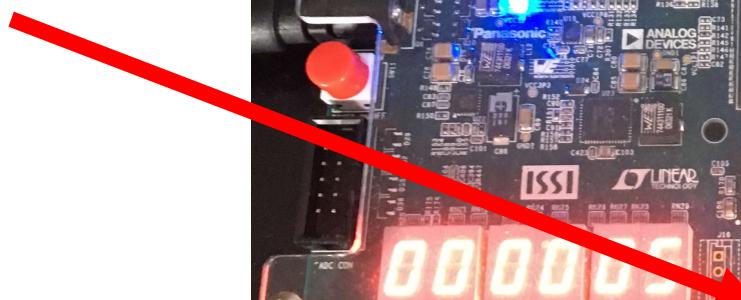
Play



# Run C and FPGA Programs

- The test program will send input signal values to the FIR module and then gather output data. It will then compare the outcomes of the FIR module with expected values.
- Upon finishing the comparison phase, the test program illuminates LED0 on the board and if all returned results match expected values, LED1 will be illuminated as well.
- After execution, the value 000005 should appear in the six hex displays

LEDs 0 and 1



# Run C and FPGA Programs

- KEY1: when the testing procedure is complete, you can tap KEY1 and the testing program will start printing the values of the filtered signal (one every second) produced by the FIR module on the HEX displays.
- You can stop the printing of the results by holding down KEY1 for two seconds.

Key 1

