# Om T. Kolhe

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## Education

2015 - Now — Dual Degree (B.Tech + M.Tech) in Electrical Engineering
Indian Institute of Technology Bombay, Mumbai, India
Master's Specialization : Microelectronics
GPA : 8.4/10.0

## Research Experience

May'19-Now — **Injection Locked Ring Oscillator (ILRO) for 5G Receivers**

**Advisor** — Prof. Maryam Shojaei Baghini, Electrical Engineering, IIT Bombay

**Background** — N-Path filters in 5G receivers requires a low phase noise multi-phase clock. Conventional way is to use a digital frequency divider with input of frequency $\frac{n}{2}f_o$. Generating clock at $\frac{n}{2}f_o$ on-chip consumes high power. A Ring Oscillator at $f_o$, injection locked with an LC oscillator is used for generation of 8 phase clock having low phase noise due to injection locking.

**Description**
- Designed a 4 stage Ring Oscillator with tuning range 0.9-2.8 GHz using sub feedback loops for increasing tuning range and improving phase noise performance
- Improved the phase noise performance of the Ring Oscillator by injection locking with a current reuse PMOS-NMOS LC Oscillator using inductance of the bondwire in the LC tank
- Modelled the bondwire in HFSS and verified obtained results against JEDEC bondwire models
- Modelling the designed ILRO to obtain an analytical expression for locking range
- Schematic and layout design in Cadence and RF parameters simulations performed in Spectre RF. Used 65 nm low leakage (**UMC65 - LL**) technology node for design and simulations.
- The design given to **Europractice** for fabrication

**Post Layout Results**
- Area of design : 560 × 840 $\mu$m (Layout Picture)
- Ring Oscillator Specifications : $f_{osc}$ = 0.9-2.8 GHz | PN = -99.4 dBc/Hz@1MHz at 2.8 GHz
- LC Oscillator Specifications : $f_{osc}$ = 1.9-2.8 GHz | PN = -120.3 dBc/Hz@1MHz at 2.8 GHz
- ILRO Specifications : Locking Range = 200 MHz | PN = -119 dBc/Hz@1MHz at 2.8 GHz

May'17-May'18 — **Receiver for IRNSS**

**Advisors** — Prof. Shalabh Gupta, Electrical Engineering, IIT Bombay
Prof. Rajesh Zele, Electrical Engineering, IIT Bombay

**Background** — Indian Regional Navigation Satellite System (IRNSS also named as **NavIC**) is navigation satellite constellation consisting of 7 satellites, completed in April 2016 - **ISRO**. The aim was to build a receiver for IRNSS as first step towards implementing NavIC for civil and military applications as an indigenous alternative to GPS.

**RF Frontend**
- Designed, fabricated and successfully tested a S-band (2.492048 GHz) right hand circularly polarized (**RHCP**) dual feed patch antenna with a branch line coupler with 16 MHz bandwidth
- Designed and successfully tested a PCB for signal conditioning and out-of-band noise rejection consisting of a Low Noise Amplifier (LNA), a SAW Filter and 2 stage RF amplifier
- Designed and fabricated a **4-layer** PCB for **amplifying** and **downconverting** the received **S-band** signal to baseband (0 Hz) using I/Q Demodulator, Fractional-N PLL and microcontroller
- Successfully received **navigation bits** from all satellites using the receiver front end

**Signal Processing**
- Implemented in MATALB FFT based acquisition methods - code phase domain & doppler frequency domain thus decreasing the acquisition time compared to the Serial Search technique
- Implemented the serial search acquisition block, digital Phase Locked Loop and Delay Locked Loop for tracking using ping-pong buffers on TM320C5515 DSP board to get navigation bits

Oct'18-May'19 — **Sensor System for Disbond Detection**

**Advisor** — Prof. Siddharth Tallur, Electrical Engineering, IIT Bombay

**Background** — The aim was to make a device for detection of disbonds in carbon fibre honeycomb structure used in launch vehicle. The PWT sensor array would record the Lamb waves reflected from the defects and preform signal processing on the recorded waves to identify the location of the defect. - Funded by Indian Space Research Organisation(**ISRO**)

**Prototype I**
- Designed an embedded system to sample Lamb waves on carbon fibre sheet using PWT sensors at 512 kHz by implementing a **ping-pong** buffer for real time signal processing on TM4C1294XL board using internal ADC
- Implemented real time 512 point Fast Fourier Transform (FFT) and 1-D Continuous Wavelet Transform (**CWT**) using Morlet wavelet

**Prototype II**

- Designed a modular 8 channel data acquisition system with each channel capable of sampling at 4 GHz using a FPGA as buffer, which will then send the sampled data serially to a DSP board for further signal processing like FFT and CWT
- Implemented the system using ADC121S101 sampling at 1GHz, **FPGA** and **Nios II** processor in Intel's Platform Designer as a proof of concept
- Implemented 1-D CWT using Morlet wavelet on TI's DSP C6678 multicore processor

## Professional Experience

Summer'18 **SDR for TV Tuner Application** | Internship
**Company** Sony Semiconductor Solutions, Japan
**Manager** Kazuhiro Shimizu, Analog LSI Bussiness Division
**Description**

- Investigated and benchmarked Automotive TV LSI solutions of competitor, against DTG and NorDig test set for digital TV platforms
- Developed an new **Software Defined Radio** (SDR) technology feature on Automotive TV LSI products by designing and testing of **USB streaming** application on Raspberry Pi platform after an extensive study of existing RTL-SDR
- Designed and successfully tested a digital down converter logic board for down sampling and interleaving IQ samples as a proof of concept demonstrator system using SONY's programmable RF tuner IC

## Academic Achievements

2019 **Awarded Undergraduate Research Award** - Study of Phase Noise in Ring Oscillators
Awarded for recognition of significant amount of research work done by undergraduate students.

2019 **Institute Technical Color**
Awarded for exceptional contribution to technical activities in the institute.

2014 **Selected for Kishore Vaigyanik Protsahan Yojana (KVPY) fellowship**
Fellowship awarded by the Department of Science and Technology, Govt. of India to encourage high school students to pursue research in science.

2015 **Scholarship for Higher Education (SHE) under INSPIRE**
Awarded by virtue of performance within the top 1% of the Board at the Class XII level.

## Select Course Projects

Spring '19 **Low Power Analog frontend for Portable Biopotential Signal Monitoring** | EE781 - IC Design for Sensor System
**Instructor** Prof. Pramod Murli, Electrical Engineering, IIT Bombay
**Description**

- Designed a Instrumentation Amplifier in UMC180, for ECG readout channel for portable biopotential signal monitoring system, with performance standards meeting ANSI-AAMI standards.
- The instrumentation amplfier consisted of two stages - input trans-conductance stage and output trans-impedance stage; with input stage capable of driving multiple output stages.
- Chopping technique was used to reduce offset and flicker noise.

Spring '18 **VCO Design and Layout** | EE619 - RF VLSI Design
**Instructor** Prof. Rajesh Zele, Electrical Engineering, IIT Bombay
**Description**

- Awarded prize for **unique design** in Layout Design Competition judged by **industry experts** from Qualcomm & Aura Semiconductor.
- Implemented an LC based PMOS cross-coupled VCO with **tail noise filtering** with a tuning range of 4.5 to 5.5 GHz.
- Used capacitor banks and varactor for frequency tuning and achieved a low Phase Noise of -118 dBc/Hz at 1MHz Offset.

Autumn'18 **4-bit 1 GS/s ADC and DAC for 16PAM Transceiver** | EE719 - Mixed Signal VLSI Design
**Instructor** Prof. Maryam Shojaei Baghini, Electrical Engineering, IIT Bombay
**Description**

- Designed Folding Flash ADC using double tail latch with offset cancellation.
- Designed a T/H circuit with clock feedthrough rejection and charge-injection compensation.
- Designed 4-bit thermometer current steering DAC for 4Gb/s data rate in 16-PAM transmitter.
- Characterized complete 16-PAM transceiver with ADC and DAC using microstrip line as channel.

Spring '18 **LNA Design and Layout** | EE619 - RF VLSI Design
**Instructor** Prof. Rajesh Zele, Electrical Engineering, IIT Bombay
**Description**

- Designed **noise cancelling** Common Source LNA with inductive source degeneration at 2.5 GHz.
- Achieved NF of 3.4dB, gain of 24.9dB, BW of 100MHz, IIP3 of -10dBm and P1dB of -21.8dBm.

Spring '18 **16-bit Rational Arithmetic Unit (RAU)** | EE705 - VLSI Design Lab
**Instructor** Prof. Sachin Patkar, Electrical Engineering, IIT Bombay
**Description**
- Designed a RAU for addition, subtraction, multiplication and division of 16-bit signed numbers.
- Implemented modified **Dadda reduction** technique for addition of partial products from **signed multiplication** of 2 or 4 numbers on FPGA thus increasing operation frequency and reducing the resources required.

## Technical Projects

Jan'16-Apr'19 **IIT Bombay Student Satellite Project**
**Background** The IIT Bombay Student Satellite Project is a landmark project taken up by the students of IIT . The objective of this project is to make IIT Bombay a respected Centre of Excellence in Satellite and Space Technology in the world. Pratham, the first satellite under this project was launched on board the PSLV C-35 on 26th September 2016. The team briefly worked on the second satellite Advitiy. Currently the team is working on various different projects in the broad domain of space technology. The team has also built an autonomous Ground-station at IIT Bombay for tracking and communicating with satellites.
**Description**
- Finalized layout for onboard communication system to interface downlink, uplink & beacon after analyzing requirements from system
- Devised the **operational modes** for the satellite system, defined switching conditions and conceptualized the framework for the **flight code** designed to coordinate between 3 microcontrollers and onboard peripherals
- Designed and implemented end-to-end link of image **transmission** and **reception** in SSTV (Slow Scan Television) protocol, establishing it as a proof of concept of Advitiy's **payload**
- Ideated the functioning of Beacon to minimize load on the communication $\mu$C by using scheduled interrupts enabling the satellite to perform other computations simultaneously
- Improvised **scheduling** of communication $\mu$C by novel use of interrupts; eliminating need of an extra $\mu$C for data handling

## Academic Services and Positions of Responsibility

Autumn'19 **Teaching Assistant** | Graduate Course : Hardware Description Languages
**Instructor** Prof. Sachin Patkar, Electrical Engineering, IIT Bombay
**Description**
- Assisted the professor in managing logistics, course plan and ensuring smooth functioning of the course
- Responsible for assisting students in in-class tasks and conducting exams for 70+ post graduate students

Jan'17-Dec'18 **Head, Communication Subsystem, IIT Bombay Student Satellite Project**
**Description**
- Spearheaded a team of **8 people** with the aim of creating a robust on-board communication system to realize the payload and increasing **reliability** by enforcing **quality assurance practices**, devised by the team.
- Organized Groundstation Workshops in 2019 and 2017 with over **80 students** and **faculty members** across India sharing knowledge on satellite communication and groundstation as part of the social goal of the project.
- Contributed to Satellite 101 wiki, a compilation of basic knowledge of satellite project with **47.1k** pageviews and **18.7k** users.
- Executed a **three-step recruitment** process to select 16 students for the subsystem, from 70+ applicants evaluating their technical ability, practical approach and teamwork.

## Key Courses and Programming Skills

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| **Analog VLSI** | RF Microelectronics Chip Design, Mixed Signal VLSI Design, Analog VLSI Design |
| **Digital VLSI** | VLSI Design, Foundations of VLSI CAD, VLSI Design Lab |
| **Sensors** | Integrated Circuit Design for Sensor Systems, Sensors in Instrumentation |
| **Devices** | VLSI Technology, Solid State Microwaves Devices, Microelectronics Simulation Lab |
| **Miscellaneous** | Design and Evaluation of Photovoltaic Power Plants, Digital Signal Processing |
| **Design Tools** | Cadence Virtuoso, Intel Quartus, HFSS, ADS, System Advisor Model, PVlib |
| **Programming** | C++, C, Python, MATLAB, VHDL, Verilog, Assembly, Java, LaTeX |

## Extracurricular Activities

- Actively **volunteered** in Green Campus, **National Service Scheme** for conservation of plant species

- Successfully qualified level 1 & 2 Tabla exams conducted by Akhil Bharatiya Gandharva Mahavidyalaya Mandal
- An avid traveller and adventure sports enthusiast - amateur **scuba diver** and **sky diver**

## References


**Prof. Maryam Shojaei Baghini**
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