Om T. Kolhe | Curriculum Vitae

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Research Interests: RF and Mixed-signal CMOS circuits, Biosensors, IoT transceivers

EDUCATION

Indian Institute of Technology Bombay *2015 - 2020*
Dual Degree (B.Tech + M.Tech) in Electrical Engineering with specialization in Microelectronics
GPA: 8.4/10

RESEARCH

Injection Locked Ring Oscillator (ILRO) for 5G Receivers *May'19 - Present*
Advisor: Prof. Prof. Maryam Shojaei Baghini, Electrical Engineering, IIT Bombay

Introduction: The aim of the project was to design, fabricate and test a fully on-chip multiphase oscillator for N-Path filters. The design targeted low phase noise with low power and area. An Injection Locked Ring VCO, locked using a on-chip LC oscillator generates the 8 phase clock.

- Designed a 4 stage Ring Oscillator with tuning range 0.9-2.8 GHz using sub feedback loops for increasing tuning range and improving phase noise performance.
- Improved the phase noise performance of the Ring Oscillator by injection locking with a current reuse PMOS-NMOS LC Oscillator using inductance of the bondwire in the LC tank.
- Modelled the bondwire in HFSS and verified obtained results against JEDEC bondwire models.
- The designed circuit taped-out in UMC 65nm Low Leakage (UMC65-LL) technology node; currently in fabrication stage. (Layout Picture)

Future Work:

- Developing mathematical model for ILRO to get expression for Phase Noise and locking range.
- Testing and measurement of the die on probe station.
- Writing a paper, to be submited for publication after completion of measurement.

Receiver for IRNSS *May'17 - May'18*
Advisors: Prof. Shalabh Gupta, Electrical Engineering, IIT Bombay and
Prof. Rajesh Zele, Electrical Engineering, IIT Bombay

Introduction: Indian Regional Navigation Satellite System (IRNSS also named as **NavIC**) is navigation satellite constellation consisting of 7 satellites, completed in April 2016 by **ISRO**. The aim was to build a receiver for IRNSS as first step towards implementing NavIC for civil applications.

RF Frontend and Antenna:

- Designed, fabricated and successfully tested a S-band (2.492048 GHz) right hand circularly polarized (RHCP) dual feed patch antenna with a branch line coupler with 16 MHz bandwidth.
- Designed and successfully tested a PCB for signal conditioning and out-of-band noise rejection consisting of a Low Noise Amplifier (LNA), a SAW Filter and 2 stage RF amplifier.
- Designed and fabricated a 4-layer PCB for amplifying and downconverting the received S-band signal to baseband (0 Hz) using I/Q Demodulator, Fractional-N PLL and microcontroller.
- Successfully decoded navigation bits from all satellites using the receiver front end.

Signal Processing:

- Implemented in MATALB FFT based acquisition methods - code phase domain & doppler frequency domain thus decreasing the acquisition time compared to the Serial Search technique.
- Implemented the serial search acquisition block, digital Phase Locked Loop and Delay Locked Loop for tracking using ping-pong buffers on TM320C5515 DSP board to get navigation bits.

Sensor System for Disbond Detection *Oct'18 - May'19*

Advisor: Prof. Siddharth Tallur, Electrical Engineering, IIT Bombay

Introduction: The aim was to make a device for detection of disbonds in carbon fibre honeycomb structure used in launch vehicle. The PWT sensor array would record the Lamb waves reflected from the defects and preform signal processing on the recorded waves to identify the location of the defect - Funded by Indian Space Research Organisation(**ISRO**.)

Prototype I:

- Designed an embedded system to sample Lamb waves on carbon fibre sheet using PWT sensors at 512 kHz by implementing a ping-pong buffer for real time signal processing on Tiva-C board using internal ADC.
- Implemented real time 512 point Fast Fourier Transform (FFT) and 1-D Continuous Wavelet Transform (CWT) using Morlet wavelet.

Prototype II:

- Designed a modular 8 channel data acquisition system with each channel capable of sampling at 4 GHz using a FPGA as buffer; FFT and CWT performed on sampled data on DSP.
- Implemented the system using ADC121S101 sampling at 1GHz, FPGA and Nios II processor in Intel's Platform Designer as a proof of concept.
- Implemented 1-D CWT using Morlet wavelet on TI's DSP C6678 multicore processor.

WORK EXPERIENCE

SDR for TV Tuner Application | **Internship, Sony Semiconductor Solutions, Japan**

Manager : Kazuhiro Shimizu, Analog LSI Bussiness Division *May'18 - Jul'18*

Introduction: Worked on automotive TV tuner ICs at Sony's Technology Centre 2, Atsugi, Japan

- Investigated and benchmarked Sony's Automotive TV LSI solutions, against DTG and NorDig test set for digital TV platforms to identify areas for improvements.
- Developed an new Software Defined Radio (SDR) technology feature on Automotive TV LSI products by designing and testing of USB streaming application on Raspberry Pi platform.
- Designed and successfully tested a digital logic board for down sampling and interleaving IQ samples as a proof of concept demonstrator system using SONY's programmable RF tuner IC.

SCHOLASTIC ACHIEVEMENTS

- **Undergraduate Research Award** (awarded to select undergraduate students for exceptional effort towards research) for study of Phase Noise in Ring Oscillators in 2019
- **Institute Technical Color** in 2019, awarded for exceptional contribution to RF system design for satellite communication in the institute.
- Awarded the **Certificate of Appreciation for Excellence in Teaching Assistantship** for the graduate level course of Hardware Description Languages in the Autumn 2019 semester.
- Selected for **Kishore Vaigyanik Protsahan Yojana** (KVPY) fellowship in 2014, awarded by the Department of Science and Technology, Govt. of India.
- **Scholarship for Higher Education (SHE) under INSPIRE** in 2105, awarded by virtue of performance within the top 1% of the Board at the Class XII level.
- **Unique Design in RF Layout Competition** in 2019, conducted as a part of graduate course - RF VLSI Design and judged by industry experts from Qualcomm and Aura Semiconductors.

PUBLICATION

O. Kolhe and C. Jain, "Microcontroller based, satellite borne Transmitter for broadcasting images using SSTV - A prototype design", Satellite Technology Day, UR Rao Satellite Centre, April 2018.

SELECT COURSE PROJECTS AND TECHNICAL PROJECTS

Low Power Analog ASIC for Portable Biopotential Signal Monitoring
Instructor: Prof. Pramod Murli, EE781 - IC Design for Sensor System, IIT Bombay *Autumn '18*

- Designed an Instrumentation Amplifier in UMC180, for ECG readout channel for portable biopotential signal monitoring system, with performance standards meeting ANSI-AAMI standards.
- The instrumentation amplfier consisted of two stages - input trans-conductance stage and output trans-impedance stage; with input stage capable of driving multiple output stages.
- Chopping technique was used to reduce offset and flicker noise.

4-bit 1 GS/s ADC and DAC for 16PAM Transceiver
Instructor: Prof. Maryam Shojaei Baghini, EE719 - Mixed Signal VLSI Design, IIT Bombay *Spring '19*

- Designed folding flash ADC using double-tail latch with offset & reference subtraction
- Designed a T/H circuit with clock feedthrough & charge-injection compensation
- Designed 4-bit thermometer differential current steering DAC for 4Gb/s data rate
- Integrated and characterized complete 16-PAM transceiver with ADC and DAC using microstrip line as channel

LNA Design and Layout
Instructor: Prof. Rajesh Zele, EE619 - RF VLSI Design, IIT Bombay *Spring '19*

- Designed noise canceling common source LNA with inductive source degeneration at 2.5 GHz.
- Achieved NF of 3.4dB, gain of 24.9dB, BW of 100MHz, IIP3 of -10dBm and P1dB of -21.8dBm.

16-bit Rational Arithmetic Unit (RAU)
Instructor: Prof. Sachin Patkar, EE705 - VLSI Design Lab, IIT Bombay *Spring '19*

- Designed 16-bit RAU for adding, subtracting, multiplying & dividing 16-bit signed numbers.
- Implemented modified **Dadda reduction** technique for addition of partial products from **signed multiplication** of 2 or 4 numbers on FPGA thus increasing operation frequency and reducing the resources required.

IIT Bombay Student Satellite Project (IITBSSP) *Jan'17 - Apr'19*
This project aims to promote excellence in satellite and space technology. The team has worked on two satellites 'Pratham' and 'Advitiy'. Pratham was launched onboard PSLV C-35 on 26th Sept 2016.

- Devised operational modes for the satellite; defined switching conditions and conceptualized the framework for the flight code to coordinate between three μC and onboard peripherals.
- Designed and implemented end-to-end link of image transmission and reception in SSTV (Slow Scan Television) protocol, establishing it as a proof of concept of Advitiy's payload.
- Ideated the functioning of Beacon to minimize load on the communication μC by using scheduled interrupts enabling the satellite to perform other computations simultaneously.
- Improvised scheduling of communication μC by novel use of interrupts; eliminating need of an extra μC for data handling.

ACADEMIC SERVICES AND POSITIONS OF RESPONSIBILITY

Graduate Teaching Assistant | Hardware Description Languages *Autumn'19*

For a class of 70 students,assisted students in in-class tasks, conducted exams and graded exams and projects. Assisted the instructor in posing the assignments and project.

Head, Communication Subsystem, IITBSSP *Jan'17 - May'18*

Responsible for envisioning and executing technical work in the 10 membered subsystem.

- Organized Groundstation Workshops attended by over 80 students and **faculty members** across India sharing knowledge on satellite communication and groundstation
- Contributed to Satellite 101 wiki, a compilation of basic knowledge of satellite project with 47.1k pageviews and 18.7k users from across the globe.
- Executed a three-step recruitment process to select 16 students for the subsystem, from 70+ applicants evaluating their technical ability, practical approach and teamwork.

KEY COURSES AND PROGRAMMING SKILLS

Analog VLSI	RF Microelectronics Chip Design, Mixed Signal VLSI Design, Analog VLSI Design
Digital VLSI	VLSI Design, Foundations of VLSI CAD, VLSI Design Lab
Sensors	Integrated Circuit Design for Sensor Systems, Sensors in Instrumentation
Devices	VLSI Technology, Solid State Microwaves Devices, Microelectronics Simulation Lab
Miscellaneous	Design and Evaluation of Photovoltaic Power Plants, Digital Signal Processing
Design Tools	Cadence Virtuoso, Intel Quartus, HFSS, ADS, System Advisor Model, PVlib
Programming	C++, C, Python, MATLAB, VHDL, Verilog, Assembly, Java, LaTeX

EXTRA-CURRICULAR ACTIVITIES

- Actively volunteered in Green Campus, National Service Scheme for conservation of plants
- Plays Tabla; Qualified exams conducted by Akhil Bharatiya Gandharva Mahavidyalaya Mandal
- An avid traveler and adventure sports enthusiast - amateur scuba diver and sky diver

REFERENCES

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